Modeling of Reverse Current Effects in Trench–Based Smart Power Technologies

Von der Fakultät für Elektrotechnik und Informatik

der Gottfried Wilhelm Leibniz Universität Hannover

zur Erlangung des akademischen Grades

Doktor–Ingenieur

genehmigte Dissertation von

Dipl.–Ing. (FH) Michael Kollmitzer, MSc.

2020

Referent:	Prof. Dr.-Ing. Erich Barke
Korreferent:	Prof. Dr.-Ing. Jürgen Scheible
Vorsitzender:	Prof. Dr.-Ing. Jörn Ostermann
Tag der Promotion:	17. Dezember 2019

Abstract

The increase in complexity in todays automotive products is driven by the trend to implement new features in the area of safety, comfort and entertainment. This significantly raises the safety requirements of new ICs and the identification of possible sources of failures gains in priority. One of these failure sources is the injection of parasitic currents into the common substrate of a chip. This does not only occur during exceptions in the operation of the IC but also affects applications which require switching of inductive loads. The difficulty to handle substrate current injection originates from its nonlocality as it potentially influences the entire IC.

In this thesis a point–to–point modeling scheme for Spice-based circuit simulation is proposed. It addresses parasitic coupling effects caused by minority carrier injection into the substrate of a deep–trench based BCD technology. Since minority carriers can diffuse over large distances in the common substrate and disturb circuits in their normal operation, a quantitative approach is necessary to address this parasitic effect early during design. An equivalent circuit based on the chip's design is extracted and the coupling effect between the perturbing devices and the susceptible nodes is represented by Verilog-AMS models. These models represent the three main components in the coupling path which are the forward biased diode at the perturbing device, the reverse biased diode at the susceptible node, and the intermediary common substrate of the chip. An automated layout extraction framework identifies the injectors of the minority carriers and the sensitive devices. Additionally, it determines the relevant parameters for the models. The curve fitting functions of the models are derived from calibrated TCAD simulations which are based on the measurement results of two dedicated test chips.

The test chips were specifically designed to provide detailed analysis capabilities of this parasitic coupling effect. This led to a design which contains several different injector nodes and a large number of susceptible nodes spread over the entire area of the chip. Additionally, the chip incorporates the most commonly used layout–based guard structures to obtain an in-depth insight on their efficiency in recent BCD technologies.

Based on the results obtained by measurements of the test chips the underlying physics of the coupling effect are discussed in detail. Minority carrier injection in the substrate is not much different to the operating principle of a bipolar transistor and the differences and similarities between them are presented. This forms the basis of the model development and explains how the equations of the Verilog-AMS models were derived. Finally, the entire simulation flow is evaluated and the simulation results are compared to measurements of the chip.

Key words: reverse current, substrate, minority carrier injection, TCAD, Verilog-AMS, circuit simulation, guard ring analysis

Kurzfassung

Produkte für den Automobilmarkt wachsen stetig in ihrer Komplexität, getrieben durch neue Innovationen im Bereich Sicherheit, Komfort und Unterhaltung. Dadurch steigen auch die Anforderungen an die Produktsicherheit neuer ICs und die frühzeitige Erkennung von Fehlerquellen gewinnt an Priorität. Eine dieser Fehlerquellen entsteht durch die Injektion parasitärer Ströme in das gemeinsame Substrat. Dieses Fehlerbild tritt nicht nur bei Störungen des normalen Betriebs auf, sondern ist ein Effekt, der auch beim Schalten induktiver Lasten zu Tage tritt. Die Herausforderung liegt in erster Linie an der Nichtlokalität dieses Effektes, welcher typischerweise den gesamten IC beeinflusst.

In dieser Dissertation wird ein Modellierungsschema für den Schaltungsentwurf vorgeschlagen, welches den parasitären Effekt durch Punkt–zu–Punkt Verbindungen erfasst und abbildet. Ein quantitativer Ansatz ist notwendig, um diesen Effekt in den Anfängen der Entwicklungsphase sichtbar zu machen, damit die Schaltungsentwickler darauf reagieren und notwendige Schritte zur Unterdrückung veranlassen können. Ladungsträgerinjektion in das Substrat zeichnet sich vor allem durch seine Fernwirkung aus, wodurch die Störquellen und die Störsenken weit voneinander entfernt liegen können. Die Quellen und Senken werden mittels Verilog-AMS-Modellen in einer Ersatzschaltung miteinander verbunden, welche der existierenden Schaltungsnetzliste hinzugefügt wird. Die Extraktion der notwendigen Schaltungsparameter aus dem Layout wird von einer eigens konfigurierten Verifikationssoftware übernommen. Die Verilog-AMS-Modelle beinhalten mathematische Funktionen, welche die physikalischen Effekte des Kopplungspfades beschreiben. Diese Funktionen basieren auf den Ergebnissen von kalibrierten TCAD-Simulationen, welche auf Messergebnissen von Testchips beruhen.

Die Testchips beinhalten mehrere potentielle Störquellen und empfindliche Bauelemente, um die Einflüsse der Substratströme messtechnisch erfassen zu können. In diesen Zusammenhang wurden auch mehrere gängige Schutzstrukturen auf dem Testchip integriert, um deren Effizienz zu bestimmen. Zur Verwendung kamen zwei aktuelle BCD-Technologien, welche über eine *Deep-Trench*-Isolationstechnik verfügen, um die einzelnen Wannen auf dem Chip voneinander zu trennen.

Die physikalischen Grundlagen der Minoritätsträgerinjektion werden basierend auf den Ergebnissen, welche aus den Messungen der Testchips und der TCAD-Simulationen gewonnen werden konnten, erklärt. Das Grundprinzip des durch Minoritätsträgerinjektion hervorgerufenen parasitären Effektes gleicht dem eines bipolaren Transistors. Die Unterschiede und Gemeinsamkeiten zwischen den beiden werden aufgezeigt. Die daraus gewonnenen Erkenntnisse bilden die Basis für die Ableitung der Simulationsmodelle. Abschliessend werden die Ergebnisse der Simulation und der Messungen miteinander verglichen und die vorgeschlagene Methodik validiert.

Schlüsselworte: Reversestrom, Substrat, Minoritätsträgerinjektion, TCAD, Verilog-AMS, Schaltungssimulation, Schutzstrukturanalyse

Acknowledgments

I would like to express my wholehearted gratitude to my supervisor Prof. Dr. Erich Barke for his guidance, his patience and his motivation through all those years. I'm also grateful to my second supervisor Prof. Dr. Jürgen Scheible for accepting me as his student and for his earnest interest in my research.

Besides my supervisors I would like to express my great appreciation to Dr. Volker Meyer zu Bexten for all the insightful discussions and his continuous support. My research would have been impossible without his aid. My sincere gratitude also goes to Dr. Markus Olbrich for his encouragement and his constructive critical feedback.

I'm grateful to my colleagues Günther Wellenzohn, Dr. Josef Schweda and Hubert Rothleitner for their assistance and for backing my research from the beginning. My gratitude also be expressed to Infineon Technologies AG for giving me the opportunity to work on this topic and to Maik Herzog and Hubert Pernull for their leadership.

This thesis was partially performed under the eRAMP project funded by grants from *ENIAC* Joint Undertaking of the EU. I have enjoyed the friendly cooperation with several institutions and individuals within the eRAMP project. I'm especially thankful for the aid given by Dr. Juraj Marek of the Slovak University of Technology in Bratislava.

While working on this thesis I was fortunate to have the encouragement and friendship of Claudia and Christoph who gave me their wholehearted support. I thank my fellow students at the IMS for their warm welcome in Hannover. I would like to thank my parents, my late mother Andrea and my father Rudolf. They have been wonderful parents and have shown a genuine interest in my life, my work and my well-being.

Finally, I take this opportunity to express my love to Claudia and to thank her for all her patience and support during this period. And my dear child Anna, who brought so much love and brightness into my life.

Hannover, February 2020 Michael Kollmitzer

Contents

Chapter 1

Introduction

1.1 Applications of Smart Power ICs

Over the past decades, Smart Power integrated circuits (ICs) have evolved into a global, billion dollar business with numerous applications especially in the automotive and industrial markets [1]. The ability to combine power electronics, analog control circuitry and digital functions monolithically on a common substrate makes this kind of ICs attractive for a wide variety of products some of which are shown in Figure 1.1. This combination of different functions fulfills the requirements to increase product reliability and system robustness by reducing the number of discrete, external components that would be necessary to provide the same functionality.

With the continuous trend to implement new features into automobiles in the area of safety, comfort, and entertainment, the overall complexity of the system increases as well as the risk to suffer from systematic or random failures [2]. With the introduction of the *ISO 26262* in late 2011, functional safety aspects are covered for the entire development process and it provides guidance on how to avoid these risks. Simulation methodologies of possible faults become mandatory in order to quantify the probabilities of an element to fail and to affect the entire system. Therefore, the importance to better understand possible sources of failures and their influence on an item continually grows.

Figure 1.2 shows a block diagram of a typical application for Smart Power ICs, an H–bridge circuit used for motor control. An IC like this contains four power stages which are configured as two half–bridges each consisting of a high–side and a low–side switch. The individual power switches are controlled by gate drivers whereas dead time generation is realized by direct connections between the power stages. This safety feature prevents the high–side and low–side power transistors from conducting at the same time which would create a low–ohmic connection between the supply and the ground network. Additional protection functions can include overvoltage lock out which switches the motor into a freewheeling state while undervoltage protection can shut down the outputs of the device entirely to prevent uncontrolled motion of the motor. Overtemperature protection requires on–chip temperature measurements for each power stage because they dissipate the highest thermal energy. Sophisticated analog circuitry is also required for current limitation features. Signals which leave the chip and have a direct connection to

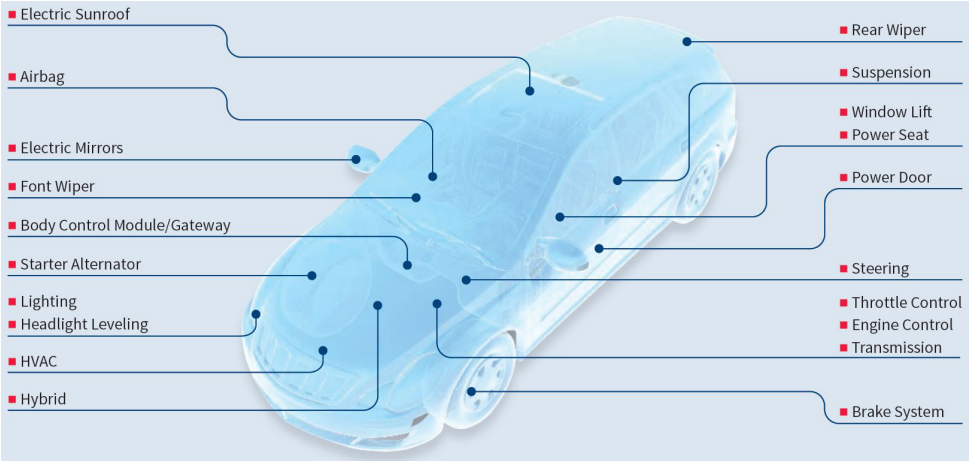


Figure 1.1: Overview of automotive applications [3]

bond pads usually have to be protected against electrostatic discharge (ESD) events by means of special diodes. Communication to the outside world can be realized by different means ranging from serial peripheral interface (SPI) to off–board bus interfaces like local interconnect network (LIN) or controller area network (CAN) for system on a chip (SoC) solutions.

Co–integration of all these functions on the same die brings several different operating domains into close proximity. While power devices have to withstand voltages of up to 60 V and currents in the range of 10 A, analog control circuits and digital logic blocks operate at voltage levels well below 5 V and high energy efficiency targets of the automotive industry forces operating currents into the low mA range. Additionally, reliable operation of the device has to be guaranteed for temperatures between $-40\ °C$ and $150\ °C$. Although Smart Power ICs are advantageous concerning electro magnetic interference (EMI), on–chip parasitic coupling effects become increasingly influential. With ever decreasing minimum feature sizes of IC technologies [4], the distance between the power devices and the control circuits is reduced as well.

A set of particularly complex coupling effects involve switching of inductive loads which causes parasitic voltages and currents to be introduced into the common substrate of the chip. Shifts in the electric potential of the substrate can easily reach hundreds of millivolts and affect low–voltage circuits in the close vicinity of the power device. Injected currents, however, can cause charge carrier diffusion that can disturb sensitive circuits even over large distances. This effect occurs in Smart Power ICs which use reverse–biased pn junctions as isolation principle between the devices on the chip. Under certain conditions, these pn junctions become forward biased and parasitic currents are directly injected into the common substrate [5]. As stated by B. Murari [1]: *"Parasitic currents enabled by inductive loads are among all the unrequired, parasitic effects, the most peculiar, by far the least predictable and the most difficult to manage."*

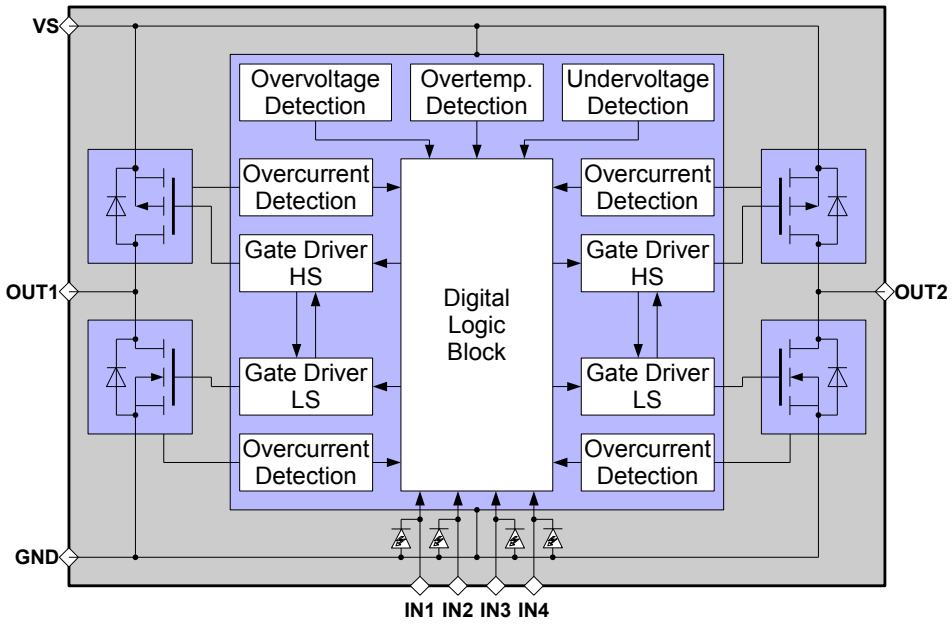


Figure 1.2: Block diagram of an H–bridge driver

1.2 Research Motivation

The high complexity of parasitic substrate current injection originates from its nonlocality. While injection takes place in a localized area of the chip, its effects can permeate the entire IC and disturb other components in their normal operation. Even currents in the range of μA at the susceptible elements can have a significant negative impact on the functionality of a chip [6]. Although this can lead to costly redesigns or even to field returns due to performance degradation, the circuit designers only have empirical methods at their disposal. These methods work reliably for simple designs with a limited number of injecting and sensitive nodes but there is always the risk to miss something.

Therefore, an automatized approach has to be provided to address this issue in products of greater complexity. However, the design tools provided by the major electronic design automation (EDA) vendors do not cover substrate current injection effects but focus on capacitive noise coupling into the substrate. This type of parasitic effect is mostly governed by majority carriers while forward biased *pn* junctions are the cause for minority carrier injection. As already stated by [7] in 2003, circuit extraction and simulation software of major EDA vendors cannot successfully model the effects of minority carriers in the common substrate. This situation has not changed since then which inspires new research activities where all aspects of the design flow have to be addressed. In the last few years two companies, Intento Design and PN Solutions, were founded which provide commercial EDA solutions concerning minority carrier injection.

The main goal of this thesis is to develop and implement a circuit design methodology which can quantitatively assess the impact of substrate minority carrier injection in an analog design environment. This includes development of a simulation model which can

process the unique geometrical properties of the parasitic device. A manual simulation setup is required to estimate the disturbance during the floor planning phase. Layout analysis by means of a back–annotation flow is mandatory to reliably identify all disturbance sources and susceptible nodes on a chip and additionally provides the necessary parameters for the model. Substrate contacts and well connections in the proximity of the affected nodes have to be taken into account as well because they show significant influence on the parasitic coupling path.

1.3 Thesis Outline

Chapter 2 gives a comprehensive introduction to the conditions that can lead to substrate coupling issues with focus on the injection of minority carriers. It contains an overview of smart power technologies (SPT) and how the inherent coupling path influences other devices on the chip. Different aspects on how to address this issue—which have been developed by other researchers over the past decades—are discussed starting from technological options to robust circuit design. In many cases, layout–based counter measures are proposed because they provide an easy way to implement suppression mechanisms. However, the main questions in circuit design are whether this parasitic effect will influence a susceptible circuit and how to implement sufficient protection. Therefore, simulation aspects of the parasitic effect become increasingly important.

The main focus of Chapter 3 is the proposal of a new simulation methodology for minority carrier injection. Basic device physics of bipolar transistors are necessary to understand the underlying coupling mechanism. Since standard bipolar transistor models for circuit simulators are not well suited to represent this parasitic effect, a new model is derived based on results of technology computer–aided–design (TCAD) simulations. Due to the unique geometrical structure of this device, limitations have to be accepted and some simplifications are required in order to obtain fast and accurate simulation results. Finally, the model is split into several separate parts each focusing on a specific subset of the parasitic coupling path. These models are then interconnected in a netlist which can be used by a Spice–based simulator. Parameter extraction is performed directly on the layout database.

In Chapter 4, an overview of two test chips which were developed during the course of this thesis is given. It contains details about the devices that are used as disturbance source, the importance of the power supply network, the influence of the substrate contacts and the connectivity of the susceptible nodes. Information about guard ring structures and their electrical design is presented and the measurement setups are discussed.

This leads to the comparison of the measurement and the simulation results which are discussed in Chapter 5. Special attention is paid to the influence of the ground and power supply network on the behavior of the parasitic effect. With these results, the influence of electric fields in the substrate is discussed and the measurement results are compared to the TCAD and circuit simulation results.

Finally, Chapter 6 draws conclusions from the research, discusses an outlook for possible enhancements in the future and illustrates the importance of additional research.

Chapter 2

On Reverse Current

2.1 Introduction to Smart Power Technologies

Smart Power Technologies were invented in the mid–eighties of the 20^{th} century driven by a growing demand of the market to integrate logic blocks, analog functions and power devices on the same chip [8, 9, 10, 11]. Pure complementary metal oxide semiconductor (CMOS) technologies have the highest layout density and are best suited for digital design but can also be used for analog circuits especially when low power consumption or high input impedance is required. However, bipolar junction transistors (BJT) are the best choice for high precision analog functions due to their high transconductance and low $1/f$ noise. Additionally, bipolar transistors are very popular in bandgap voltage reference circuits where two currents—one proportional and one complementary to absolute temperature—are compensated by each other to achieve a reference voltage with a very low temperature drift [12, 13]. The disadvantage of bipolar transistors as power switches is that with an increasing load current they also require an increasing base current causing heat dissipation and current densities to become problematic. The double–diffused MOS (DMOS) device does not require driving currents during DC conditions, has very fast switching speed and no secondary breakdown limitation [14]. A drift region between the drain implantation and the active channel region can increase the voltage capability of a MOS device [15] that makes it superior to the bipolar power transistor. The combination of all these devices on a single chip is referred to as multipower Bipolar–CMOS–DMOS (BCD) [14] and a simplified cross section is illustrated in Figure 2.1.

The manufacturing process of a typical BCD technology starts with the n^+ implant of the buried layer followed by the growth of the n–doped epitaxial layer. The epitaxial layer is utilized in two different devices, it forms the bulk of the p–channel CMOS field effect transistor (FET) and the base region of the pnp transistor. The n^+p^- junction between the buried layer and the substrate provides the vertical isolation of the epitaxial pockets and the rest of the chip. The highly n–doped sinker structure is a low–ohmic connection to the buried layer and the epitaxial layer. However, the sinker can also be entirely omitted which makes the connection to the epitaxial layer more high–ohmic. This is usually done for pure CMOS logic circuit blocks to efficiently utilize the high layout density but it increases the risk of latch–up. The p–well implant forms the body of the

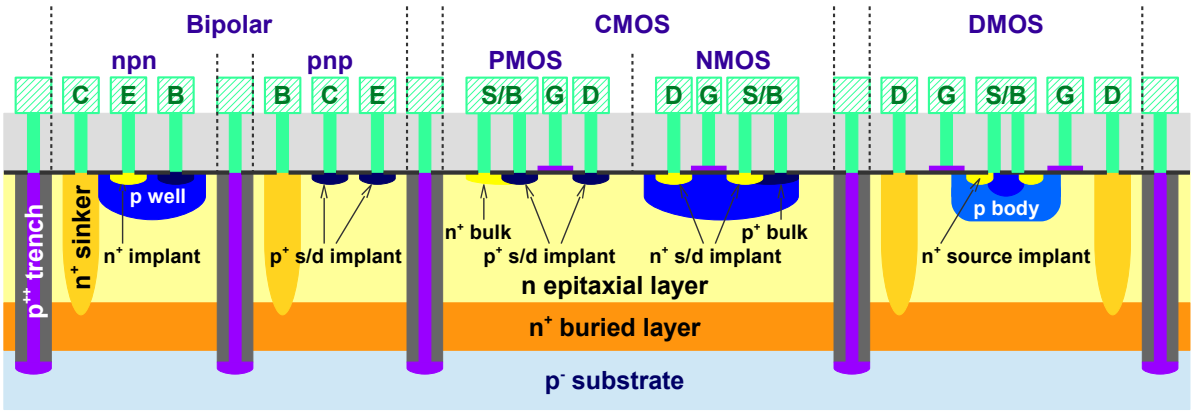


Figure 2.1: Simplified cross section of a BCD technology

n–channel CMOS and also the base of the *npn* transistor. The body of the power DMOS, labeled as p–tub in Figure 2.1, can be implanted by a separate step to obtain different doping levels to optimize the threshold voltage of the device. The on–resistance $R_{DS_{on}}$ of the DMOS is mainly determined by the layout of the core structure which is placed multiple times in parallel until the design constraints like $R_{DS_{on}}$ or current capability are met. In a lateral DMOS, the source and drain terminals are alternated and the drift region, which provides the high–voltage capability, is formed by a low n–doped region extending from the drain towards the p–body where the n–channel is generated. In a vertical DMOS, the channel also forms beneath the gate but the drift region is provided by the epitaxial layer. The buried layer and sinker structure are significantly involved in leading the current back to the silicon surface and the resistance of these layers influences the $R_{DS_{on}}$.

Heavy ion n and p surface implants are used as metallurgical connection between the tungsten plugs and the silicon. They form source and drain regions and the channel stops in the CMOS devices, base and emitter in the *npn* transistor, base and collector in the *pnp* transistor, and the source of the DMOS. Additional steps are performed in the manufacturing process to change the doping of the base region of the *npn* transistor by using the p–tub of the DMOS instead of the CMOS p–well. This changes the electrical characteristics of the bipolar *npn* transistor providing the designers with an alternative device without adding steps to the manufacturing process.

Modern BCD technologies provide a wide variety of devices which may include

- CMOS (with different voltage classes),
- vertical DMOS, lateral DMOS,
- bipolar transistors,
- diodes, zener–diodes, ESD protection,
- capacitors,
- resistors, and
- non–volatile memory (e.g. Flash, EEPROM) [16].

There are several different methods available to isolate the devices from each other although they are monolithically integrated on the same substrate. The most common isolation techniques used in Smart Power ICs are illustrated in Figure 2.2. Junction isolation was used early by the bipolar technologies where interaction of the devices is prevented by reverse biased pn junctions. These are formed laterally between the n epitaxial layer or the n^+ sinker structure and the p–doped top and bottom isolations and vertically by the n^+p^- junction of the buried layer and the substrate. This imposes an important constraint on the electric potentials of the different layers because they have to stay reverse biased at all times to ensure proper isolation.

The deep–trench isolation structure provided additional size reduction of the devices because there is no out–diffusion of the p isolation and the SiO_2 trench abuts the base and collector contact regions. Connection to the common substrate is now provided by polycrystalline silicon (poly-Si) layer which extends from the top of the chips surface down into the substrate. Although the lateral isolation of the devices is now formed by a dielectric, the vertical isolation is still formed by a reverse biased pn junction and the afore mentioned constraint about the electric potentials is still valid. The test chips designed during the course of this thesis are all based on the deep–trench isolation technique and will be discussed in Chapter 4.

The last isolation technique—which is referred to as silicon–on–insulator (SOI)—utilizes a dielectric insulation on the periphery of the devices as well as at the bottom. In the example shown in Figure 2.2, oxygen ions are implanted into an n–doped silicon followed by a high temperature annealing step. In this way the silicon and oxygen form an SiO_2 dielectric layer. The entire n epitaxial layer becomes electrically separated from the other devices [17] and all parasitic effects related to pn junctions like leakage currents and direct charge carrier injection are non–existent. However, capacitive coupling caused by fast voltage transients dV/dt via the sidewalls or the substrate still remains an issue. Other disadvantages are the cost factor and the higher thermal resistance of the dielectric which significantly reduces its applicability for power devices.

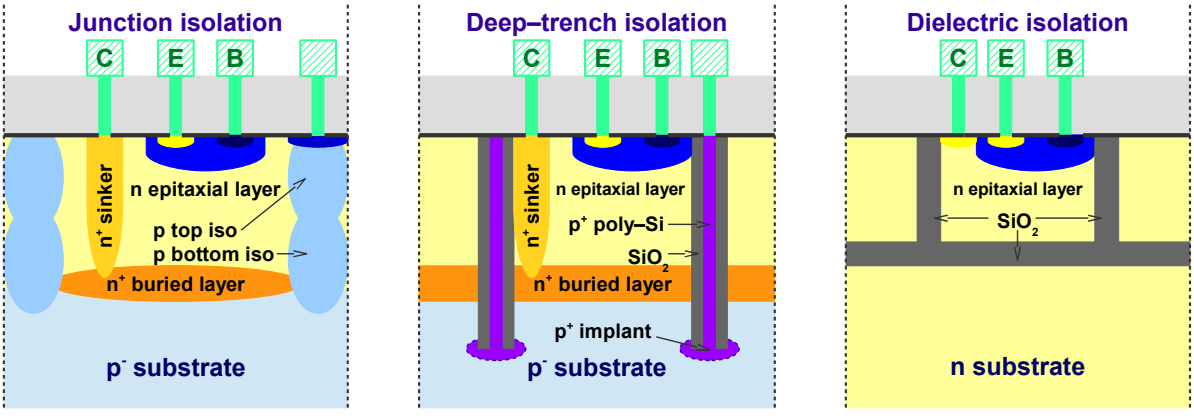


Figure 2.2: Simplified cross sections of isolation techniques

2.2 Substrate Coupling Effects

There are several different coupling effects which can disturb susceptible devices via the common substrate [18, 19] of ICs. It is important to differentiate between the underlying physical mechanisms because this has significant impact on the transmission of the disturbance in the substrate as well as on the observed behavior at the sensitive nodes. Some parasitic coupling effects like impact ionization in the CMOS channels [20] do not have a direct connection to the substrate of a Smart Power IC but may still influence devices in the same epitaxial well. However, disturbance sources that do not affect the substrate but remain within the confines of the epitaxial well are beyond the scope of this thesis.

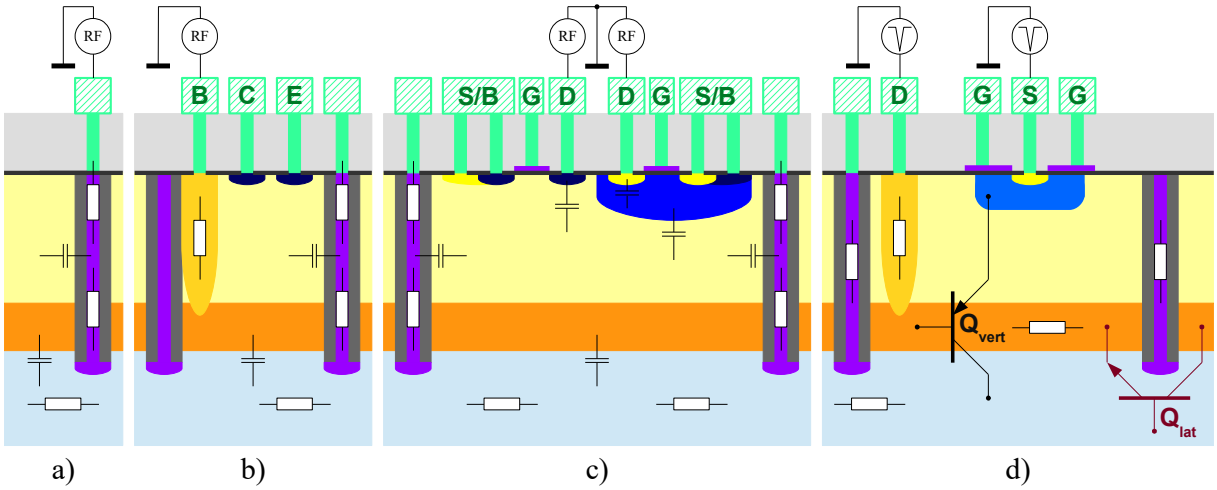


Figure 2.3: Parasitic coupling paths

2.2.1 Direct Current Injection

Direct current injection occurs when the substrate contacts of the chip have a different electric potential Φ and introduce equalizing currents into the substrate. Conduction in the substrate is caused by the applied electric field and the resulting drift current is

$$J = \sigma \cdot \overrightarrow{\mathbf{E}} \tag{2.1}$$

where σ is the electrical conductivity of the semiconductor determined by

$$\sigma = q \cdot (\mu_n \cdot n + \mu_p \cdot p)\,. \tag{2.2}$$

q is the elementary charge, μ_n and μ_p are the mobilities of the electrons and holes, and n and p are the charge carrier densities in the semiconductor. The electric field is determined by the spatial gradient of the electric potential written as

$$\overrightarrow{\mathbf{E}} = -\nabla\Phi. \tag{2.3}$$

Under static conditions, the different electric potentials Φ in the substrate have no negative impact on the devices' operation but switching in the digital parts [21, 22] can introduce dynamic potential shifts. These can be coupled into the epitaxial wells via the capacitance of the depletion region between the substrate and the buried layer (see Figure 2.3a). The disturbance of the circuit depends on the connectivity of the epitaxial well and the devices in the well. For example, if the epitaxial well has a low–ohmic connection to the supply network the substrate noise may "only" cause voltage spikes on the supply lines while a high–ohmic connection of a *pnp* transistors' base terminal (see Figure 2.1) will be amplified and disturb the circuit's operation. Although this effect is mostly governed by majority carriers in the substrate it still has to be taken into account because introducing electric fields in the substrate via the deep–trench contacts is actively pursued in several layout–based protection structures which will be discussed in detail in Chapter 2.6.3.

2.2.2 Capacitive Substrate Coupling

Capacitive coupling effects are caused by fast voltage transients at the devices of the IC and can introduce significant noise into the substrate. Possible sources of radio frequency (RF) noise are illustrated in Figure 2.3b for bipolar devices and in 2.3c for CMOS devices. The coupling effect is mainly governed by majority carriers moving in and out of the depletion region of the reverse–biased *pn* junctions attached to the noise source which generate changes in the potential of the substrate. The voltage gradient is related to the resistive properties of the semiconductor material and the current density can be calculated by solving Equation 2.1. As discussed in [19, 23], substrate doping levels have significant impact on the noise propagation behavior. A lowly doped substrate shows an almost linear decline of the noise voltage over the distance while a heavily doped substrate distributes the noise over large distances although it has a higher decrease rate at close ranges to the source.

An additional coupling path can be formed via the ground and power supply network that is connected to the bulk nodes (wells) of the devices. Any disturbances at the wells can affect the devices in two different ways. The first path is through the depletion region capacitances of the drain and source regions. The second path is by means of the body effect, causing shifts in the threshold voltage V_t [24]. For Smart Power ICs with deep–trench isolation technique, direct capacitive coupling between the interconnect and the substrate as described in [22, 25] cannot occur because the substrate is not directly accessible at the top of the silicon.

2.2.3 Parasitic Bipolar Transistors

The parasitic coupling effects associated with the bipolar transistors which are formed between the different n and p regions on the chip become active under certain biasing conditions. Figure 2.3d shows two bipolar transistors, Q_{vert} and Q_{lat}, which are inherent for Smart Power ICs.

The *vertical parasitic pnp transistor* Q_{vert} is formed by the source, drain and substrate terminal of a power DMOS. Usually, all of these *pn* junctions are reverse biased and isolate

the different regions from each other. The coupling path implemented by Q_{vert} becomes active when the potential at the source terminal of the DMOS becomes lower than the one at the drain terminal. In this case, the base–emitter diode of Q_{vert} becomes forward biased and injects *holes* into the n epitaxial region of the DMOS. These minority carriers diffuse towards the depletion region of the reverse biased pn junction between the buried layer and the substrate. This causes injection of a *hole* current into the substrate which in turn introduces a positive potential shift [1]. The observed effects are similar to capacitively coupled majority carrier injection as described in [19, 23, 24] but can also activate a parasitic $pnpn$ thyristor device causing latch–up [5].

The *lateral parasitic npn transistor* Q_{lat} is the main source of minority carrier injection into the substrate and is activated when the applied potential at the drain terminal is lower than the substrate potential. This means the base–emitter structure of the bipolar transistor Q_{lat} is formed by the forward biased pn junction between the buried layer and the substrate. The *electrons* move from the n–doped buried layer into the p substrate and introduce a negative potential shift. Additionally, these injected minority carriers can diffuse laterally over large distances to reverse biased pn junctions between the buried layer and the substrate which form the base–collector regions of the parasitic bipolar device. The minority carriers move through the depletion regions into the epitaxial wells and introduce parasitic currents and potential shifts [18, 5]. Details about the operating conditions which activate the parasitic bipolar transistors are discussed in detail in the following chapters.

2.3 H–Bridge Driver as Motor Control

A typical application for Smart Power ICs is the H–bridge driver used for motor controls. This example perfectly illustrates the parasitic coupling effect responsible for minority carrier injection into the substrate. During switching events of power devices with inductive loads, the terminals *OUT1* and *OUT2* illustrated in Figure 2.4 can reach electric potentials beyond the power rails of the circuit [5]. During the *on* state, the current I_{on} passes through the transistors *HS1* and *LS2* and the motor—represented by R and L in the Figure—is running. An overview of all possible operating modes of an H–bridge is given in Table 2.1. The parasitic effect can occur when the motor is running, either actively in clockwise or counter–clockwise rotation or passively in freewheeling mode and the H–bridge is switched into breaking mode.

When the transistors are turned on and the motor is accelerating, the current I_{on} can be determined by solving

$$V_S - V_{DS,HS1} - V_{DS,LS2} - I_{on}(t) \cdot R - L \cdot \frac{dI_{on}(t)}{dt} = 0 \tag{2.4}$$

which leads to

$$I_{on}(t) = I_{max} \cdot \left(1 - e^{-\frac{R}{L} \cdot t}\right) \tag{2.5}$$

Table 2.1: H-bridge driver operating modes

HS1	LS1	HS2	LS2	Operating Mode
off	off	off	off	breaking, clamping
on	off	off	**on**	clockwise rotation
off	**on**	**on**	off	counter–clockwise rotation
on	off	**on**	off	freewheeling
off	**on**	off	**on**	freewheeling
on	**on**	off	off	
off	off	**on**	**on**	supply short circuit
on	**on**	**on**	**on**	

and an estimated maximum current at the turn–off time t_{off} of

$$I_{max} = I_L\left(t = t_{off}\right) = \frac{V_S - V_{DS,HS1} - V_{DS,LS2}}{R}. \tag{2.6}$$

The voltage between the terminals *OUT1* and *OUT2* is governed by the supply voltage V_S of the circuit and the drain–source voltages V_{DS} of the two active transistors. The dominant device characteristic in this application is the on–resistance $R_{DS_{on}}$ of the two power switches as they are operated in the linear (ohmic) region and V_{DS} can be determined by solving Ohm's law. When the power transistors are switched off, the energy stored in the magnetic field of the motor's inductance dissipates.

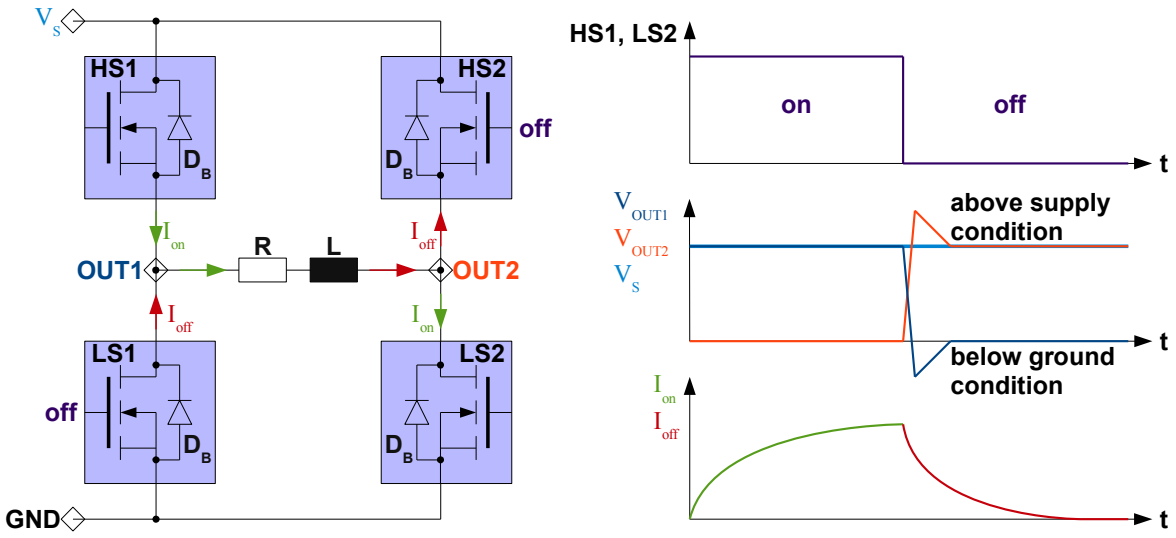


Figure 2.4: H–bridge driver as motor control

The current I_{on} is cut off by the transistors *HS1* and *LS2* and is forced to continue as I_{off} as shown in Figure 2.4. In many applications, explicit freewheeling diodes are

omitted as a cost factor since the area of the power devices on the chip is large enough to handle the dissipation energy of the inductor L. However, the current I_{off} is forced to pass through the inherent body–diodes D_B of the power devices *HS2* and *LS1* and can be calculated by solving

$$L \cdot \frac{dI_{off}(t)}{dt} - I_{off}(t) \cdot R - V_S - 2 \cdot V_D(t) = 0 \tag{2.7}$$

where V_D is the forward voltage of D_B. It can be determined by solving the *Shockley ideal diode equation* which is

$$I_D(t) = I_S \cdot \left(e^{\frac{V_D(t)}{n \cdot V_T}} - 1 \right) \tag{2.8}$$

where I_S is the reverse bias saturation current, V_T is the thermal voltage and n is the emission factor. Combining 2.8 and 2.7 leads to

$$L \cdot \frac{dI_{off}(t)}{dt} - I_{off}(t) \cdot R - V_S - 2 \cdot n \cdot V_T \cdot \ln\left(\frac{I_{off}(t) + I_S}{I_S} \right) = 0. \tag{2.9}$$

This equation shows that I_{off} is subject to the internal resistance of the two freewheeling diodes, the power source, and L and R. Under the assumption that the internal resistances of the diodes and the power source are very small, the time constant can be simply written as

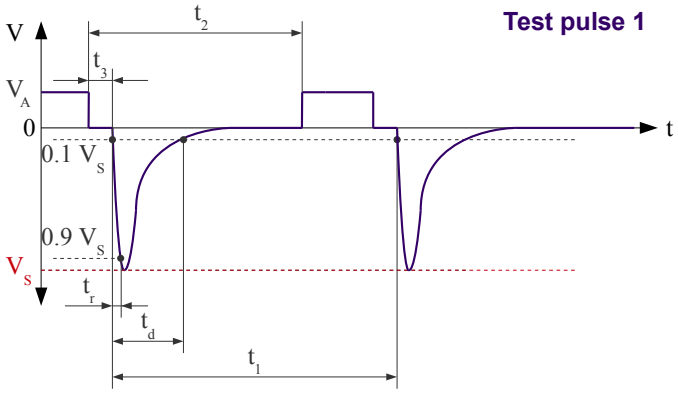
$$\tau_{off} = \frac{L}{R}. \tag{2.10}$$

Since the energy stored in an inductor is dissipated faster by a large resistance, this equation represents the slowest case of the circuit in terms of dissipation time. For automotive applications—where values of L and R are in the range of *Ohms* and tens of *mH*—it means the current I_{off} is active for several milliseconds before it reaches zero.

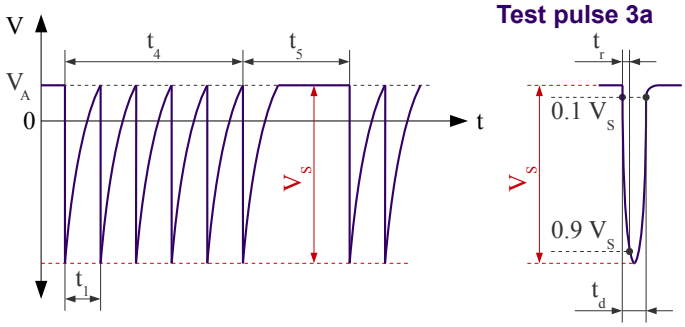
This example illustrates that situations which activate parasitic coupling paths cannot always be avoided but can be an inevitable, reoccurring event specific to a certain application. In this particular case, the parasitic effect is triggered at every *on–off* cycle of the H–bridge.

2.4 Automotive Test Pulses

Besides the circumstances in an H–bridge application which lead to the activation of the parasitic bipolar transistors, the *ISO 7637* [26] defines a set of test pulses which can also result in carrier injection into the substrate. The test pulses shown in Figure 2.5 are *Test Pulse 1* and *Test Pulse 3a* and they are applied to the power and ground supply network of the printed circuit board (PCB) in the application. This means there are additional electrical components between the terminals of the PCB and the IC which partially attenuate the test pulses. Depending on the maximum ratings of the technology it can be necessary to provide additional protection outside the IC. The manufacturer of the vehicle is responsible to define the requirements on the behavior of the IC during the exposure to the test pulses. Safety relevant systems need to withstand these pulses without loss of operation or system failure.



Parameters	12 V System
V_S	-75 V to -150 V
t_d	2 ms
t_r	1 µs [0, -0.5 µs]
t_1	≥0.5 s
t_2	200 ms
t_3	<100 µs



Parameters	12 V System
V_S	-112 V to -220 V
t_d	150 ns ± 45 ns
t_r	5 ns ± 1.5 ns
t_1	100 µs
t_4	10 ms
t_5	90 ms

Figure 2.5: *ISO 7637* test pulses [26]

2.5 Definition of Reverse Current

For the duration of the test pulses in Figure 2.5, the drain or source terminals of the DMOS (see Figure 2.6) can be pulled below the electric potentials of the terminals in the vicinity. The same situation occurs during each *on–off* cycle of the H–bridge in Figure 2.4 and the devices *HS2* and *LS1* are subjected to the current I_{off}. While the *ISO 7637* test pulses have a duration of 2 *ms* the magnetic energy stored in the inductor requires approximately five times of τ_{off} to abate. The dissipation time is larger than the dielectric relaxation time and the minority carrier lifetime, hence carrier injection can be assumed to be static. The direction of the current I_{off} through the devices is *reversed* to the way how it is intended to pass through the devices which leads to the name *reverse current*. When the transistors are turned off, the current is forced through the path provided by the bulk diodes D_B which become forward biased when the negative voltage transient has a sufficient magnitude to pull the drain potential below the source potential. For discrete power electronics where every switch is in its own separate package, this is the

only available path for the current. However, in a Smart Power IC other paths become active as well and the occurring effects have to be discerned between the low–side and the high–side switch. The common factor for both cases is the connection to the substrate which is tied to ground by the poly-Si filled deep–trench structure shown as R_{DTI} in Figure 2.6. The resistor R_{DTI} does not refer to one single substrate connection but represents the resistance of the entire deep–trench structure.

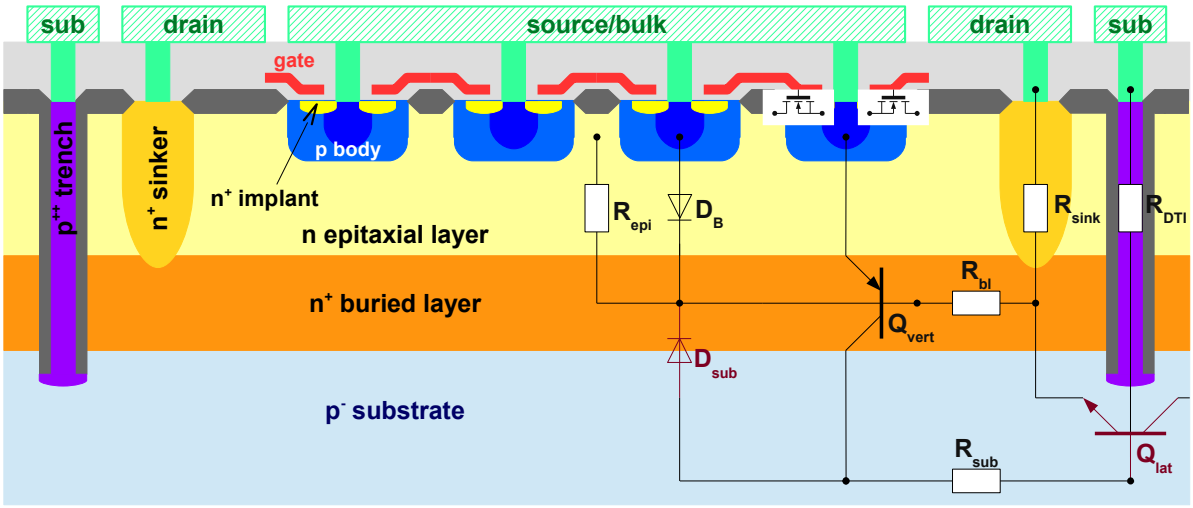


Figure 2.6: Cross section of an n–channel power DMOS including equivalent circuit

For the low–side switch, the n^+ buried layer is pulled below the ground potential by the drain terminal which causes D_B and D_{sub} to become forward biased. For simplicity it is assumed that no alternative paths exist and the current I_{off} is equal to $I_{reverse}$. The current is split into two parts, I_1 and I_2, where I_1 is essentially the current flowing through the bulk diode D_B of the power transistor shown in Figure 2.7. The ratio between I_1 and I_2 cannot be generalized because it is highly dependent on the geometry of the DMOS itself and on its surrounding ground network. The diodes D_B and D_{sub} are part of the base–emitter structures of the bipolar transistors Q_{vert} and Q_{lat}. For Q_{vert}, the emitter is tied to ground by the source/bulk node of the DMOS but the base is at a lower electric potential which activates the transistor. However, the amplification factor of this *pnp* transistor is very low due to the high doping levels in the buried layer.

The emitter of Q_{lat} is the drain node of the DMOS which is pulled below ground while the base terminal is tied to ground by the substrate network. Therefore, Q_{lat} becomes active as well and injects an *electron* current into the substrate. The current I_{sub} is a combination of the *hole* current caused by Q_{vert} and the *electron* current caused by Q_{lat}. The high doping level of the buried layer keeps the *hole* current low compared to the *electron* current. Additionally, the *electrons* are minority carriers in a lowly doped p substrate and can diffuse over large distances to other epitaxial wells where they appear as the parasitic current I_{sense} [5]. To develop a circuit simulation methodology that determines the relationship between $I_{reverse}$ and all the possible sense currents I_{sense} throughout the entire chip is a key aspect of this thesis.

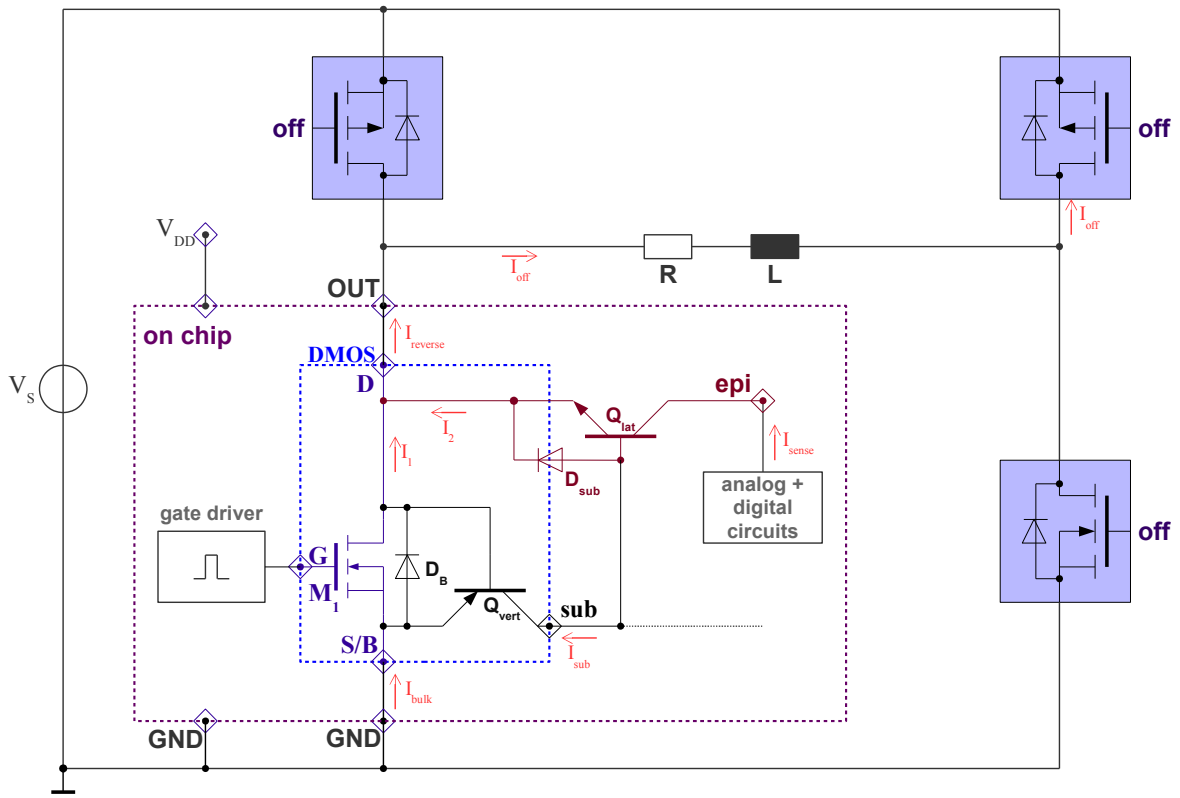


Figure 2.7: Low–side power DMOS and associated currents during the turn–off phase

The equivalent circuit of the high–side DMOS (see Figure 2.8) shows the current I_{off} traversing through the device. Same as above, for simplicity it is assumed that there are no alternative paths available for the current which makes I_{off} equal to $I_{reverse}$. The electric potential of the source/bulk node of the DMOS is higher than the supply voltage at the drain node (see Figure 2.4) and activates the bulk diode D_B. This diode is part of the base–emitter structure of the vertical *pnp* transistor Q_{vert} and the base node is formed by the epitaxial well, the sinker and the buried layer. The amplification factor of this transistor can be kept low by a highly doped epitaxial well or buried layer. In that case, most of the minority carriers injected from the source/bulk node into the epitaxial well will recombine before they reach the space charge region (SCR) of the base–collector diode which is formed by the $p^- n^+$ junction between the buried layer and the substrate. This transistor is the main cause for *hole* injection into the substrate but it has an amplification factor $\beta \ll 1$ which causes $I_1 \gg I_{sub}$. In this example, holes are majority carriers in the substrate and they primarily introduce a voltage shift inside the substrate which dissipates spatially following Ohm's law.

The lateral *npn* transistor has its base terminal tied to ground potential by the substrate contacts in the vicinity of the power device and the emitter terminal is connected to the supply voltage V_S. The base–emitter diode (D_{sub}) of Q_{lat} remains reverse–biased and no minority carrier injection occurs. Hence, the high–side DMOS is not an injector node during the described switching event but can be used as an intentional victim.

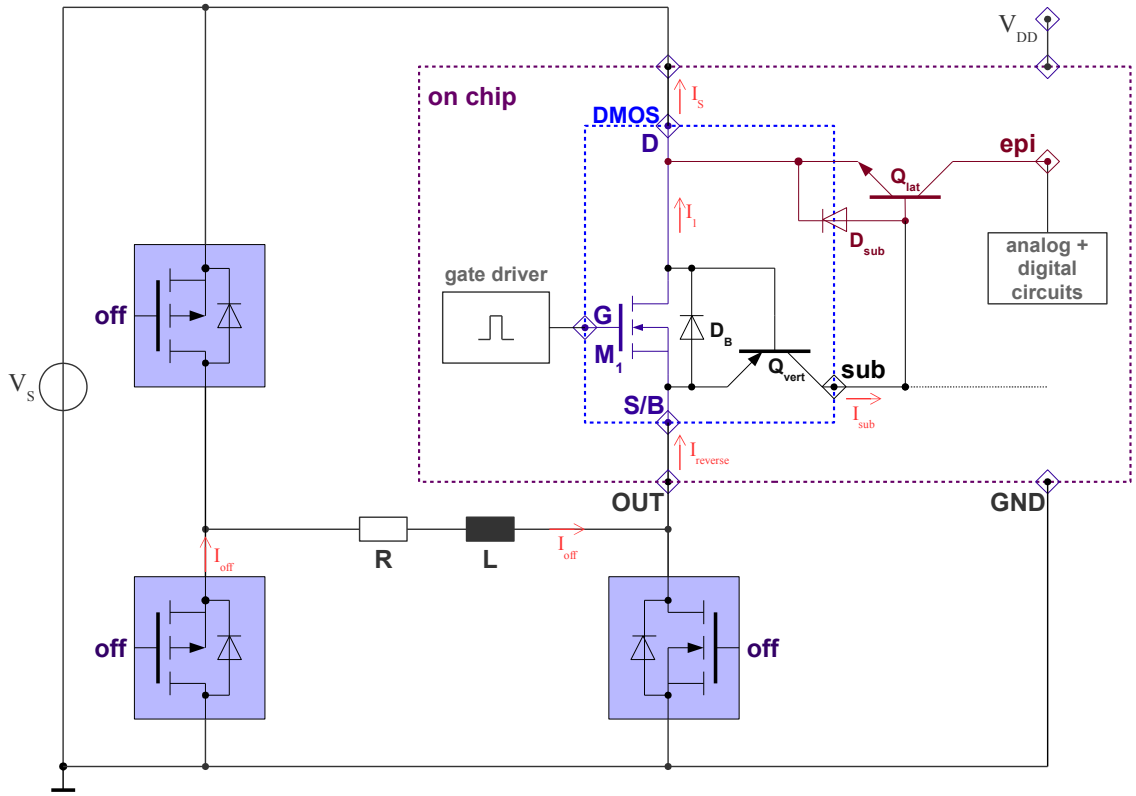


Figure 2.8: High–side power DMOS and associated currents during the turn–off phase

2.6 Possible Counter Measures

Over the past decades, a lot of research was carried out in the field of substrate coupling effects and many different aspects were covered such as

- prevention of substrate currents in the application,
- substrate noise insensitive circuit design,
- reduction of carrier injection by technological means,
- suppression of currents by counter measures in the layout, and
- estimation of parasitic currents by empirical or simulation methods.

Due to the importance for high–speed communication devices and processors the focus was mainly directed towards capacitive coupling effects and the main EDA vendors provide a wide variety of tools to analyze and simulate those parasitic effects. However, the interference caused by minority carriers injected into the substrate are still not covered by commercial software and circuit design has to rely on empirical data. In the worst case a full chip redesign can be necessary which is time consuming and expensive. Despite these limitations in circuit analysis significant advancements were made to implement robust designs for minority carrier injection. However, a quantitative approach is necessary due to increasing safety requirements.

2.6.1 Technological Efforts

As already mentioned in Chapter 2.1, technologies based on the SOI process can easily prevent injection of carriers caused by forward biased *pn* junctions but at significantly higher wafer costs. The epitaxial wells are surrounded by a silicon dioxide layer that isolates the wells from each other and the substrate. Parasitic effects are reduced to capacitive coupling which can easily induce latch–up due to higher capacitances caused by the thin dielectric layer [27] and leakage currents through the insulator material. However, thermal conductivity K is a key parameter for power devices and bulk silicon dioxide has a value of 1.4 $W/(m \cdot K)$ which is approximately two orders of magnitude less than silicon with a value of 149 $W/(m \cdot K)$ [28]. Further research has shown that layers with a thickness of less than 250 nm have an even lower thermal conductivity due to impurities, thermal boundaries and scattering effects at the material interfaces [29, 30] which cause values to drop below 0.5 $W/(m \cdot K)$ for typical buried oxide layer thicknesses.

Another technological possibility to influence the effects of substrate coupling is to alter the diffusion lengths of the charge carriers. The *electron* diffusion length L_n directly affects the lateral npn transistor Q_{lat} and the *hole* diffusion length L_p affects the vertical pnp Q_{vert}. The minority carriers have to diffuse through the base regions of the bipolar transistors in order to reach the reverse biased base–collector depletion region. The less carriers reach this region, the smaller the parasitic current is. The diffusion length of the charge carriers is determined by

$$L_n = \sqrt{D_n \cdot \tau_n} \tag{2.11}$$

$$L_p = \sqrt{D_p \cdot \tau_p} \tag{2.12}$$

where D_n and D_p are the diffusion coefficients, and τ_n and τ_p are the minority carrier lifetimes. The diffusion coefficients are related to the carrier mobility μ by the Einstein relation

$$D = \frac{k_B \cdot T}{q} \cdot \mu \tag{2.13}$$

where k_B is the Boltzmann constant, T is the temperature, and q is the unit charge [31]. The carrier lifetime [32, 33] and the carrier mobility [34] are both dependent on the doping concentration of the layer and can therefore be easily changed during the fabrication process. High doping concentration reduces the carriers' lifetime and mobility which suggests that a highly doped epitaxial well reduces hole injection by Q_{vert} into the substrate and a highly doped substrate reduces lateral electron diffusion in the base region of Q_{lat}. To achieve diffusion lengths of less than 10 μm doping levels have to be in the order of 10^{19} cm^{-3} (see Figure 2.9). In this case the minority carriers recombine within short distances from the disturbance source and the current is largely supplied by the base contact in the form of majority carriers. Only a small portion of the minority carriers remains to diffuse into the base–collector depletion regions. This approach is effectively pursued for the buried layer but mainly to reduce the resistivity of the connection to the epitaxial layer which is required for the performance of the DMOS and the intentional bipolar devices. The resistivity of silicon at these doping levels is in the range of 10^{-2} $\Omega \cdot cm$

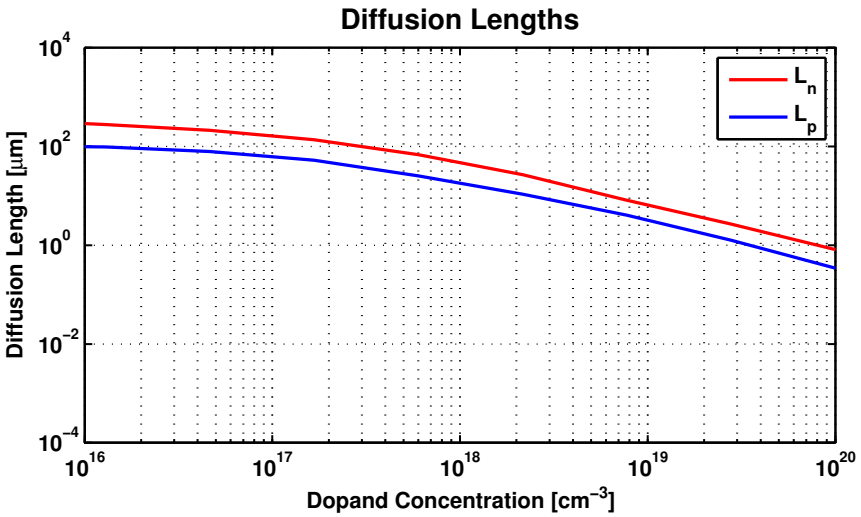


Figure 2.9: Diffusion length of electrons and holes [33]

and when it is used for the substrate the direct and capacitive coupling effects [35] increase significantly.

Inhomogeneous doping of the silicon substrate is another approach proposed in [36] to reduce the lateral diffusion of minority carriers in the substrate. A high breakdown voltage of the epi–to–substrate junction is ensured by low surface doping and a high minority carrier recombination rate is provided by high–level substrate doping in the depth of the die. The effectiveness of this approach was analyzed by [19] and showed that RF noise distribution is dependent on the depth of the p^-p^+ interface and remains constant after a certain distance from the disturbance source which is undesirable. An additional disadvantage of this approach is the higher fabrication effort and therefore increased wafer costs.

Improved manufacturing processes of the crystalline silicon ingots reduced impurities in the substrate significantly and recombination centers for the charge carriers are becoming sparse which leads to high minority carrier lifetimes [37]. Even top– and backside passivation of the wafers can influence minority carrier lifetimes by a factor of 40 [38]. Instead of changing the properties of the substrate itself, the authors of [7, 39] analyzed the effects of the backside interface on the diffusion behavior. The backside metalization forms a Schottky contact in case of a lowly doped substrate and an Ohmic contact with a highly doped interface. When the injected minority carriers reach the Schottky backside contact they can move easily into the metal but the metalization cannot provide any holes for recombination. Although it is indicated that Schottky type contacts improve the situation the study also shows that top–side substrate contacts have a much higher impact on the parasitic effect. Thinning of the silicon substrate from typical wafer thicknesses of $> 300\ \mu m$ down to $50\ \mu m$ is an additional approach to decrease lateral minority carrier diffusion [40]. This decrease is achieved by introducing surface deformations in the crystalline silicon that provides additional carrier recombination traps effectively reducing the minority carrier lifetimes. Substrate thinning can be performed by a chemical–mechanical

polishing (CMP) process step on the wafers' backside. However, the backside of the chip is subjected to constraints dependent on the packaging process and has to fulfill mechanical, thermal and chemical requirements which can make solutions for design issues secondary.

2.6.2 Concepts in Circuit Design

There are several possibilities in circuit design to reduce the effects of minority carrier injection. In [41] two additional pull–down MOS transistors are used to control the gate of a high–side power DMOS to effectively reduce the turn–off time when switching inductive loads. The reverse battery protection problem is solved by introducing a MOS transistor in series with the control circuit which prevents the parasitic epi–to–substrate diode from ever becoming active. Another protection circuit for the reverse battery condition proposes a MOSFET in series with the power DMOS to control its gate in a way to turn–off during the reverse current phase [42]. The main disadvantage is the size of the chip because the MOSFET in series with the power device must have the same current capabilities and also increases the on–resistance. In contrast to adding additional MOSFETs to explicitly turn off the current through the power devices it is also possible to explicitly turn the power devices back on. The load current is then distributed between the channel of the power transistor, the bulk diode and the epi–to–substrate diode which does not prevent injection into the substrate but at least decreases the level of injection.

A completely different approach is discussed in [43]. A detection circuit is integrated in the chip to detect hazardous voltage levels at the output terminal. The idea is to actively connect the substrate to the output terminal when necessary and to pull–down the electric potential of the substrate to reduce the forward voltage of the epi–to–substrate *pn* junction. The concept of determining the power DMOS drain potential is also used in [44] but in this case an active protection structure in the layout is either tied to ground or left floating. When the structure is tied to ground, the low–ohmic substrate connection improves RF injection while in the floating condition the layout structure locally suppresses minority carrier diffusion.

An example for robust circuit design is discussed in [6]. A bandgap reference circuit has to provide a stable reference voltage over a wide temperature range and many functions implemented on chip depend on its accuracy and stability. Instead of using typical circuit topologies [45, 46] which leave the epitaxial well of the bipolar transistors in susceptible positions, the authors of [47] connect the collectors directly to the power supply. When minority carriers diffuse through the substrate into the collector regions they only introduce a higher supply current instead of disturbing the performance of the reference circuit.

2.6.3 Layout–based Structures

Counter measures against the effects of minority carrier injection into the substrate can be easily implemented in the layout and are favored by designers because they don't require any changes to the technology. The simplest approach to influence the dissipation behavior of minority carriers is achieved by the placement of substrate contacts [39, 7].

This makes it necessary to consider two mechanisms. Substrate contacts placed in the vicinity of the injecting well (see Figure 2.10, *inner trench ring*) reduce the series resistance between the *pn* junction and the ground network. Hence, the injected minority carrier current increases due to the low–ohmic connection to the substrate and the local potential is not influenced as much which, in turn, increases the forward voltage of the D_{sub} and more carriers get injected. This is a very unpleasant situation concerning minority carrier injection. The series resistance between the substrate contacts and the injector is proportional to their distance and therefore reduces the injected minority carrier current. The substrate in the vicinity of the injector gets significantly pulled below ground potential and introduces an electric field accelerating the minority carriers towards the sensitive circuit parts which leads to disturbances over large distances from the injector. Additionally, any low ohmic substrate contact also attracts minority carriers and should not be placed close to sensitive devices.

Placement of deep trenches surrounding an injecting well can be an effective measure against substrate currents [48]. In this particular case, multiple isolation trenches are used to force the injected electrons deeper into a highly doped *p*–substrate layer. The innermost *p*–doped ring (the *inner trench ring* in Figure 2.10) is used as a substrate contact to provide a sufficient hole current for carrier recombination. This approach depends on the presence of a highly doped substrate layer with low carrier lifetimes and does not work successfully in a process like the one shown in Figure 2.1.

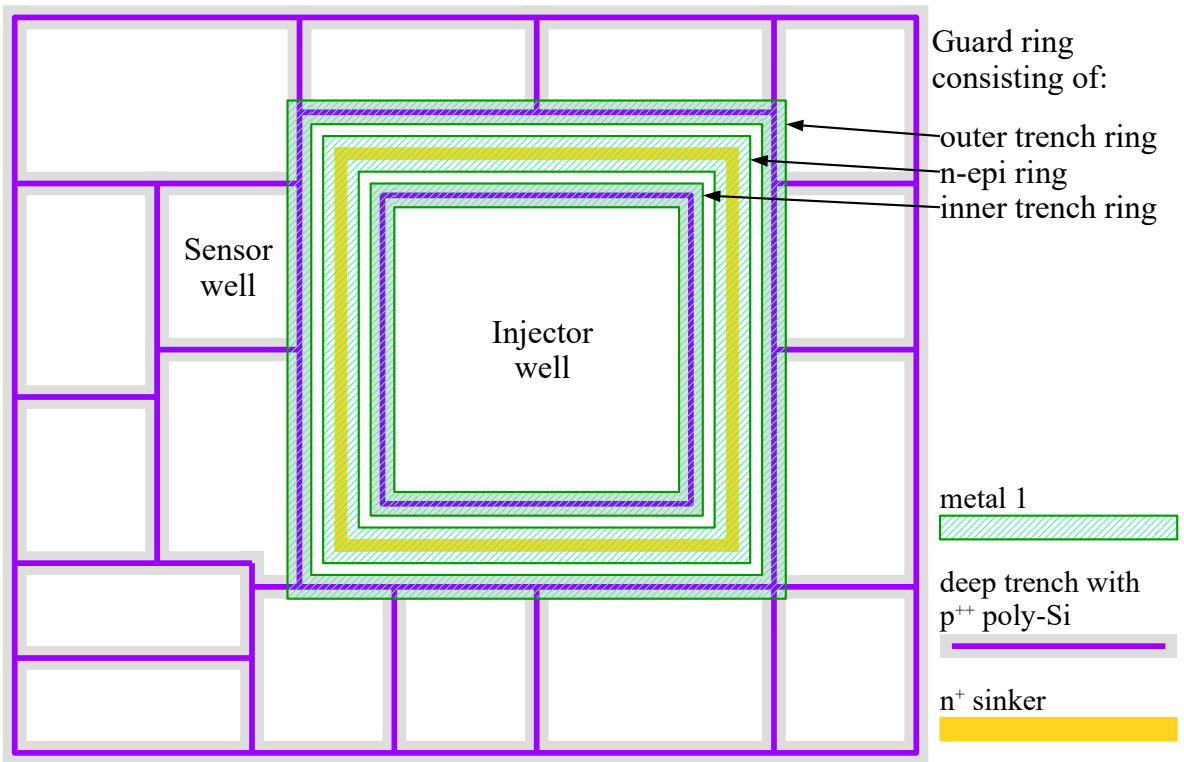


Figure 2.10: Top view of layout–based counter measures (contact shapes are omitted for visibility reasons)

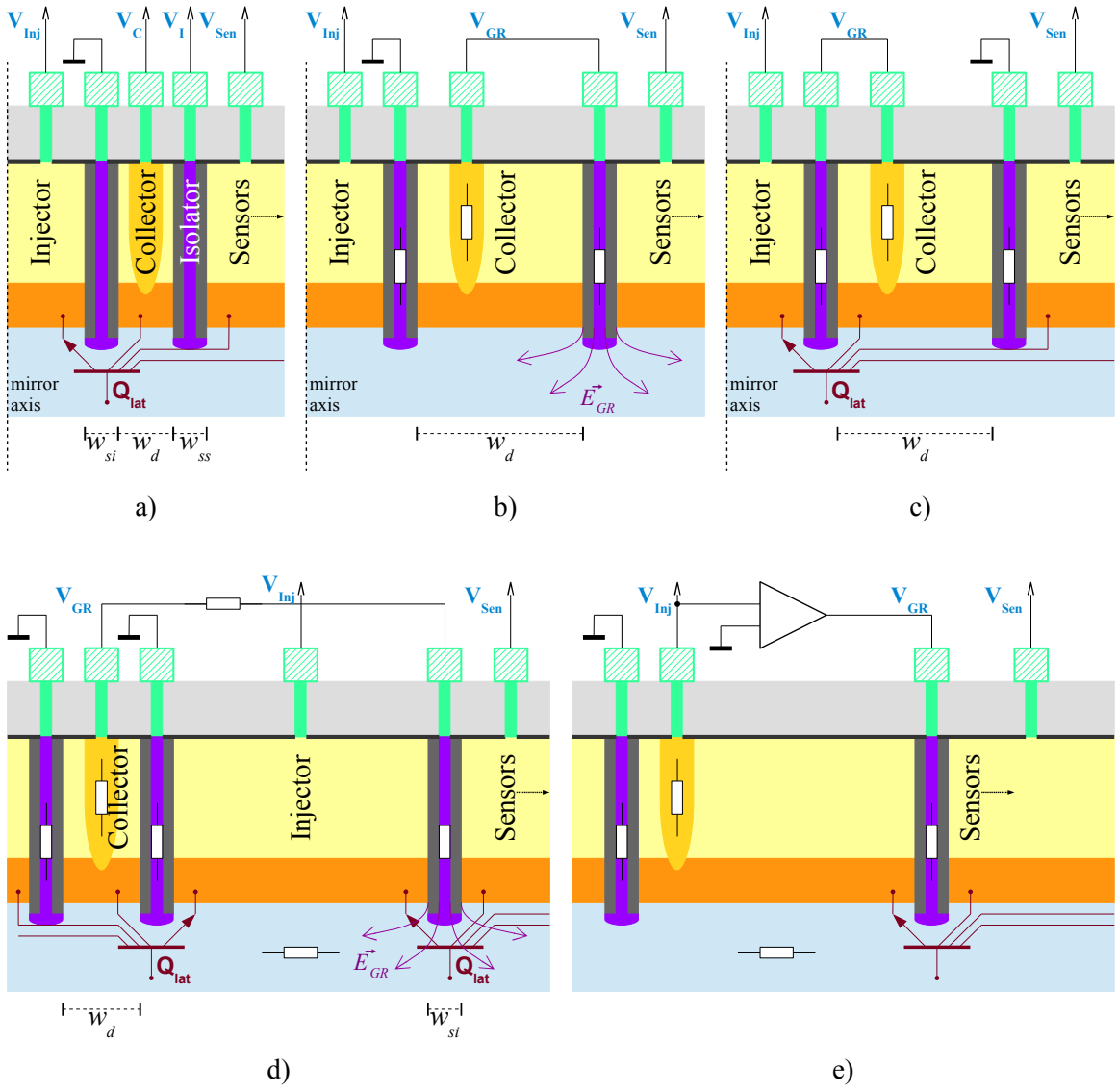


Figure 2.11: Cross-sectional view of layout–based counter measures

Suppressing the effects of minority carrier injection cannot be realized through the placement of substrate contacts alone because of the high diffusion lengths in lowly doped substrates. Minority carriers can either recombine with holes (in the bulk or at the surfaces) or be collected at reverse biased *pn* junctions acting as collectors [5]. A top view of such a guard ring is shown in Figure 2.10. Both, the *inner* and the *outer trench rings* are connected to ground and the *n–epi ring* is utilized as collector. An analysis of collecting n–rings by [49] shows that the coupling effect between the injector and the sensitive well is inversely proportional while the current through the inner guard ring is independent of the guard rings' width. This effect can be explained by analysis of the minority carrier densities which are highest close to the injector and therefore dominate the overall current through the ring. The dissipation of the current at the collector node is

largely dependent on the distance between the injector and the outer ring. In ICs distance is a luxurious commodity and different approaches had to be found.

A combination of n–wells and substrate guard rings is proposed by [50] and illustrated in Figure 2.11a. Directly adjacent to the injector is a structure comprised of two substrate regions with an n–well "collector" region in between. In Figure 2.10 the *inner* and *outer trench ring* form the substrate regions and the *n–epi ring* acts as the "collector". The n–well is connected to the power supply and acts as an intentional victim for the minority carriers while the inner substrate contact ensures a low–ohmic connection to the base of the lateral npn transistor. The outside ring labeled as "Isolator" protects the adjacent sensor structure from direct crosstalk of the "Collector". The authors of [50] came to the conclusion that a sufficiently designed substrate contact close to the injector can provide enough majority carriers for recombination with the minority carriers suppressing the effect entirely. This is in contradiction to the results presented in this thesis and to the conclusions drawn by [51]. The effect of lateral diffusion cannot be entirely avoided due to the high minority carrier lifetimes. In the measurements discussed in [51] it is shown that even at distances of $w_d = 200\ \mu m$, 5 % of the injected carriers are collected by the sensitive node. The coupling effect can also be influenced by the applied potentials at V_C and V_I for traditional junction isolation technologies due to depletion region modulation [52]. The main design parameters of these structures are the widths w_{si}, w_d, and w_{ss} of the different regions as well as the electric potentials applied to them. w_{si} and w_{ss} cannot be chosen freely in a deep–trench isolation technology because the trench etch process is strictly defined.

Additional studies have been performed on *unbiased, self–activating* guard ring structures which rely on the principle to intentionally collect some of the parasitic substrate current and to *re–inject* it in a way to obtain a counteracting effect to the initial disturbance. Figure 2.11b shows the structure proposed by the authors of [53] who named it Multi–Ring Active Analogic Protection (MAAP). Instead of tying the electric potentials of the rings to specific voltages, the MAAP connects the center *n*–ring labeled as "Collector" to the outer *p*–isolation ring while the inner *p*–isolation is tied to ground. In Figure 2.10 the *inner trench ring* is connected to ground while the *n–epi ring* and the *outer trench ring* are shorted. A very similar approach is discussed by the authors of [54] who utilize *n*–wells and *p*–wells of a different technology for the same purpose. Both papers show that self–activating guard rings are capable of suppressing minority carrier coupling effects by 2 to 4 orders of magnitude depending on the layout of the protection rings. These structures collect minority carriers at the *n*–doped region between the substrate rings which forces the collector region below ground potential ($V_{GR} < V_{GND}$). This potential is connected by metalization to the substrate ring facing the sensitive *n*–wells and introduces a negative potential shift in the substrate. This shift causes an electric field $\overrightarrow{E}_{GR}$ which counteracts the diffusion current of the electrons in the substrate. Inducing an electric field works best in a lowly doped substrate [55] because the high–ohmic material inhibits the effects of other substrate contacts in the vicinity.

The authors of [56] propose a guard ring structure that suppresses the rate of injection at the source of the disturbance. When minority carriers get injected they diffuse to the collector ring and lower its electric potential (the *n–epi ring* in Figure 2.10). The inner *p*–

doped guard ring is connected to the collector ring and locally forces the substrate below ground reducing the forward voltage of the injecting pn junction counteracting the current through the substrate (see Figure 2.11c). Substrate contacts connected to ground need to be placed at a great distance from the floating inner rings to let this structure work efficiently. This means the width w_d of the structure influences the amount of carriers that are collected and influences the resistance between the inner p–doped guard ring and the substrate ring adjacent to the n–doped collector.

The layout–based protections discussed above are implemented in the form of rings surrounding the injection well. The authors of [57, 58] show a layout design which is split into two parts. The collecting well is placed on one side of the injector while the substrate suppressor connection is facing the sensitive nodes (see Figure 2.11d). It provides a combination of introducing an electric field $\overrightarrow{E}_{GR}$ into the substrate while at the same time lowering the injection rate of the minority carriers in proximity to the sensitive nodes by locally pulling the substrate potential below ground. It is—when well designed—a combination of the MAAP and the concept of the guard ring proposed in [56]. The main difficulty is to estimate the balance between the different resistances involved in this approach. In [57] it is also suggested to put the high–side switches of an H–bridge design between the low–side switches and the sensitive devices to gain some additional distance and also to utilize any injected majority carriers of the high–side switches to recombine with the minority carriers in the substrate.

A combination of circuit design and layout–based counter measure is discussed in [59] and illustrated in Figure 2.11e. A circuit—in the design shown in [59] this is performed by a dedicated bipolar transistor—detects the voltage at the injecting node and generates a voltage V_{GR} that is applied to the substrate contact. The suppression mechanism works just as discussed for the unbiased, self–activating guard rings.

All the approaches have one fundamental problem in common which is that the efficiency of the protection cannot be easily determined during the design phase. TCAD simulation can help but requires a high effort for the simulation setup and is very time consuming hence a new set of tools is required.

2.7 Quantitative Approaches

Any attempt to address substrate coupling effects during the design phase of a chip requires some form of methodology which confirms whether the implemented counter measures are adequate or require additional adjustment. In an experienced design team this can be handled in the form of reviews to assess the risk of parasitic effects on sensitive circuit blocks. However, a level of uncertainty remains if all the disturbance sources and sensitive elements are taken into account. Manual consideration of all coupling paths is a tedious and error–prone task especially when it comes to minority carrier injection. Thus a reliable and efficient methodology has to be established. As already stated in Chapter 2.2, differentiation between the underlying physical coupling mechanisms is necessary and has an impact on the feasibility of the modeling methodologies.

2.7.1 Simulation of RF Substrate Noise

Many publications focus on modeling of the substrate for direct and capacitive substrate noise injection which is dominant in digital and mixed–signal IC designs. The coupling path between the disturbance source and the sensitive circuit can be split into three parts which are

- the connection to the substrate,
- the substrate itself, and
- the connection to the sensitive circuit.

TCAD solvers can be used to directly model the entire coupling path with all the necessary technological details [19, 60, 61] and are able to predict the influence of doping levels, different substrate geometries and guard rings on the propagation path. They utilize the finite element method (FEM) to calculate the electric potential and the current densities in the simulation domain and show good agreement with measurement results. However, in all three publications equivalent circuits are derived to obtain fast approximations by means of circuit simulation. Full chip TCAD simulations are time consuming and creating a properly configured setup is a challenging task.

Another possibility is to model the three parts of the coupling path separately. The voltages and currents that are injected into the substrate can be calculated by mathematical expressions or equivalent circuits which represent the connection to the substrate. A resistive model can be sufficient for direct injection through substrate contacts and coupling via the depletion region can be modeled by a capacitance. The model of the substrate requires more attention due to its unique geometrical characteristics. [62, 63, 64] use a dedicated extraction and modeling tool for the substrate that generates a three dimensional RC network by determining the admittance matrix of the substrate utilizing the finite differences method (FDM). This 3D network is used in SPICE simulations in combination with the circuit of the design to calculate the RF noise. This type of noise analysis is not always feasible for large circuits or digital designs which led to the development of an approach based on macro models [65] containing current injection information for all switching events in a digital cell. The entire digital circuit is combined in a single substrate model enabling substrate and power supply noise analysis. For high–speed circuits, in [66] a frequency dependent model for the substrate which enables accurate simulation up to 40 GHz has been developed. An equivalent circuit of lumped RC elements is used to describe the paths between the critical elements on top of the surface and inductances model the influence introduced by the metalization.

Instead of FDM/FEM based substrate extraction, in [67, 68, 69, 70] extraction and modeling strategies based on the boundary element method (BEM) have been proposed. They use different optimizations to determine the admittance matrix of the substrate. The number of nodes can be significantly reduced in comparison to the FDM/FEM approach which decreases extraction time. Noise coupling analysis is then performed by applying the noise stimuli to the obtained equivalent circuit and monitoring the response at the nodes of the sensitive elements. For larger designs it becomes increasingly important to perform layout–to–circuit extraction and to reduce the number of interacting boundary

nodes. Instead of connecting all the boundary nodes N to each other—which results in an $\frac{1}{2}N \cdot (N-1)$ network—Delaunay triangulation is used to identify neighboring nodes [71] and only those are connected by the resistive network. It is noted in the paper that circuit simulation will require more time when this substrate extraction algorithm is applied.

Nowadays, a wide variety of commercial tools is available which can extract an R/RC equivalent network of an IC's substrate and create an enhanced circuit simulation netlist for mixed–signal substrate noise analysis. However, most of the methodologies described in this chapter are unsuitable to simulate coupling effects of parasitic bipolar transistors with the exception of TCAD simulations.

2.7.2 Simulation of Parasitic Bipolar Transistors

There are numerous different bipolar transistor models available for circuit simulation but they were developed for a different purpose—to simulate the characteristics of an *intentional* bipolar device with a narrow base region and a manageable amount of collector terminals. When it comes to Q_{vert}, some of the model parameters can be determined but an arbitrarily shaped epitaxial well as the base terminal and the substrate of an entire chip as the collector cause serious problems. The geometry of Q_{lat} is even worse because the base terminal is the chip's substrate and there can easily be several thousand collector terminals at distances of up to some mm. Traditional modeling strategies clearly fall short and different approaches need to be investigated.

The modeling setup proposed by [72, 73] provides a combination of a linear equivalent network representing the resistive behavior and additional non–linear elements for the bipolar transistors connected to the substrate. The model can be used in a SPICE simulation environment for substrate crosstalk analysis but the non–linear elements are limited to adjacent devices. An analytical model is used by [74] to describe the current density in the base region of a lateral parasitic transistor in a p–well process. It describes the influence of the minority carrier lifetime on the behavior of the parasitic element and differentiates between low and high level injection in the base region. The analytical equation is solved by applying the boundary conditions between the emitter and the collector terminal although long distance diffusion was neglected because the excess hole carrier distribution at the collector $p'(W_b)$ is set to zero. This assumption is only valid in a confined space which inhibits free minority carrier diffusion. The effect of the carrier lifetimes on the amplification factor of the device is illustrated by the introduction of additional recombination centers in the bipolar transistors' base region by ionic impurities.

The propagation of stray minority carriers in the substrate was analyzed by [75] and 2D TCAD simulations were performed for different guard ring structures but only qualitative agreement between measurement and simulation was achieved. As stated in [7], substrate doping levels, external resistors, back side metalization and minority carrier lifetimes have a significant influence on the accuracy of the simulation results. Measurements on dedicated test chips were performed to calibrate the technology parameters for 3D TCAD simulations and the authors of [76] successfully simulated the surface potential distribution during minority carrier injection for an entire chip. This can only be achieved by complexity reduction of the simulation structure and simplifications of the layout but it

introduces some risk to miss influential geometries when it is done manually. This issue is addressed in [77] where the use of an automation scheme for layout–to–TCAD extraction is proposed. The setup requires the layout of the design and technological parameters to generate the inputs for commercial TCAD solvers. Additional data reduction is done by replacing uncritical npn collectors by Schottky junctions to obtain a feasible simulation mesh.

The complexity and the high computational effort reduces the applicability of 2D/3D TCAD simulations during circuit design and the effects of minority carrier injection cannot be determined in a typical analog design flow. The author of [78] focused on this particular problem and a new behavioral model for circuit simulation was developed. It was derived from the drift–diffusion semiconductor equations and simplified regarding carrier density dependent mobility and recombination rates. The influence of the electric field in the substrate was omitted as well which limits its applicability for active guard ring simulations. Nevertheless, diffusion currents and carrier densities were modeled as well as high–injection capability including the influence of substrate contacts between the disturbance source and the sensitive element. In [79] the accuracy of the model for static and dynamic injection was proven. The model itself is comprised of several current sources which provide the connections to the different terminals of the parasitic device.

Instead of using point–to–point connections between the injector and the sensitive element the author of [80] followed the lumped model approach. The limitation of linear lumped models is overcome by implementing an enhanced diode and resistor model to calculate the effects for majority and minority carrier currents simultaneously. The ohmic component represents the majority carriers and a diffusion resistance is introduced that considers minority carrier propagation and recombination. Simulation time is reduced by three orders of magnitude in comparison to full TCAD simulations and the circuit simulation results agree with the TCAD results [81]. The work is continuously improved in [82, 83, 84] and optimized regarding different aspects. In [82] discretization effects on the accuracy of the model in a 1D coupling setup are analyzed showing only minor deviations between TCAD and the enhanced model. An automatic layout extraction methodology is developed in [83]. It illustrates how the enhanced resistor model is connected to the enhanced diode models in a 3D layout. The limitations of the model to static injection conditions is addressed in [84] by detailed analysis of capacitive effects in the substrate. The already existing diode and resistor model described in [80] is enhanced by capacitances for the minority carrier propagations in the substrate and validated by TCAD simulations.

The issue of substrate coupling effects has firstly been addressed on a large scale for RF noise injection in mixed–signal designs. With growing markets for Smart Power ICs and increasing safety requirements in the automotive business more exotic substrate coupling effects come into focus. The importance of a complete EDA framework addressing layout extraction and back–annotation, modeling and circuit simulation is on the rise since the past decade.

Chapter 3

Model Development

3.1 Basic EDA Framework

The primary objective is to develop a complete EDA framework for analog circuit simulation which provides a quantitative approach to assess the influence of minority carrier injection into the common substrate of a chip. The framework requires a certain degree of automation to increase the reliability of identifying possible disturbance sources and susceptible nodes on the IC. In the past, the identification of critical devices was done manually which is an error-prone task and needs to be improved in addition to the development of the circuit simulation model. Based on these requirements the methodology illustrated in Figure 3.1 was devised.

Essentially, the EDA framework consists of two different parts. The main part is shown on the right hand side in Figure 3.1 and addresses the circuit simulation flow. It is—considering its principle—similar to the commonly used *RC* extraction flow. In an *RC* extraction flow, the layout and schematic information is processed by means of an LVS check and a subsequent extraction run that creates an extended netlist. This netlist includes the resistors, capacitors, and inductances added to the circuit by the metalization layers of the chip. Regarding the work discussed in this thesis, the LVS is executed with an enhanced rule deck instead of a plain LVS rule deck. It contains configuration statements that change the behavior of the LVS software to extract and store complementary information of the design's devices. Additionally, circuit devices that are sensitive to substrate coupling effects are identified and parameters that govern the effect are extracted. Hence, the LVS netlist still contains all the devices of the design and is enhanced by extensive information relevant to the parasitic effect. The result of this LVS run is then post-processed by a newly developed analysis tool. Based on the netlist information and the geometric details of the layout it generates an enhanced netlist to be used for circuit simulation. However, the simulation setup itself has to be provided by the chip designer and cannot be created automatically.

The second part of the EDA framework is focusing on the calibration of the circuit simulation model. This part is primarily based on the measurement results of two test chips which will be discussed in detail in Chapter 4. These results are used to calibrate a TCAD simulation setup which is necessary to analyze the physical effects of minority

carrier injection. During the measurements the underlying physical principle can only be indirectly observed by the current and electric potential at the sensor nodes. The carrier densities, however, remain unobservable and this is where TCAD simulations fill the gap. Based on a calibrated setup a whole series of TCAD simulations were performed to obtain a physically accurate description of the charge carrier density distribution of the chip's substrate. These results provide the reference data for the curve fitting functions of the behavioral model which is utilized for circuit simulations.

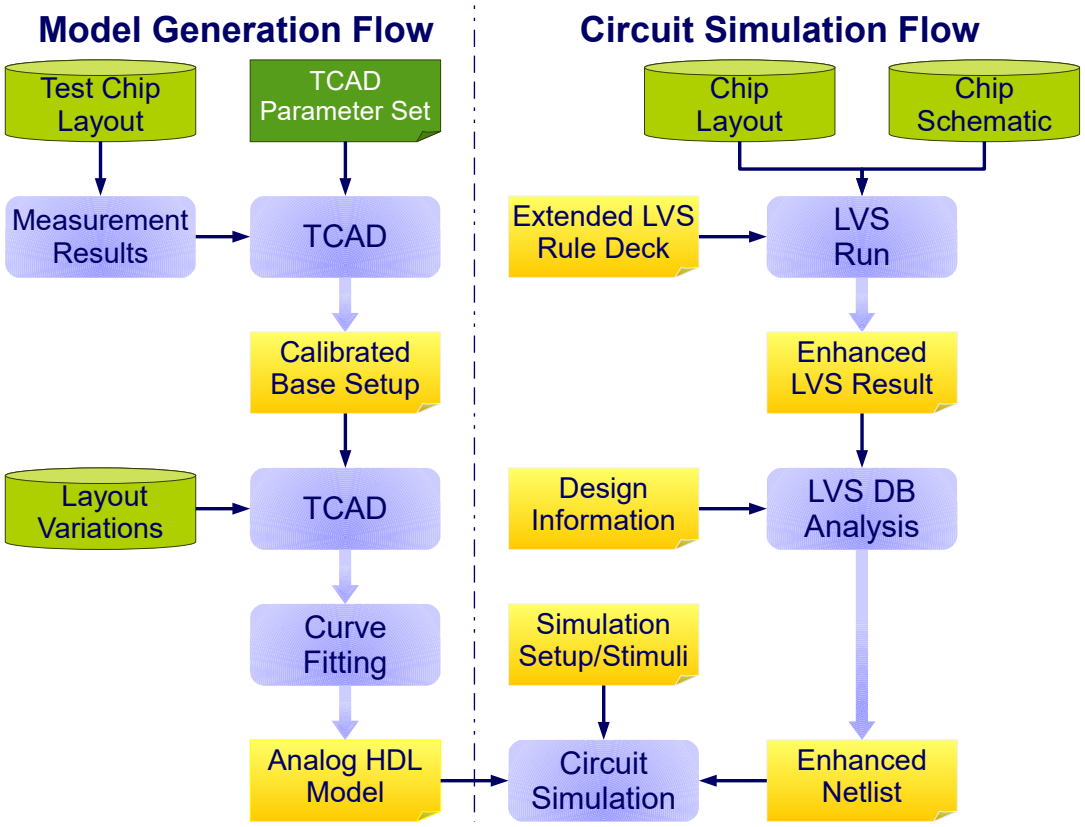


Figure 3.1: Overview of the model calibration and simulation methodology

Direct application of TCAD simulations was also considered but disregarded for several reasons. The main goal was to provide a framework to the circuit design engineers to quantify the effect minority carrier injection has on their designs. From the beginning, the intention was to extend an already existing flow instead of introducing an entirely new one. While TCAD simulations provide accurate results regarding this coupling effect, the findings need to be transfered to the circuit design flow in order to determine the impact on the design. The circuit designer would benefit from TCAD simulations but still has to identify the disturbance sources and susceptible nodes manually on the chip. The second option is to simulate the substrate in conjunction with the circuit elements which is provided by some commercial TCAD solvers already. In this scenario, the designers need to transfer their circuits from the circuit design flow to the TCAD domain. Depending on the complexity of the circuits this endeavor becomes highly impractical.

3.2 A Point–to–Point Modeling Scheme

The decision to use a point–to–point modeling scheme was made in the early stages of the concept phase. The reasons for this decision are primarily based on the geometrical parameters that govern this parasitic effect. Firstly, it is a top-level coupling effect which means it affects the entire design and cannot be broken down to block-level like RC coupling. Hence, it has an impact on the entire chip and not just a small area of it. Secondly, the size of the smallest, repeatedly used structure on the design defines the mandatory fracturing or in other words, the density of a simulation mesh. Considering the worst case scenario, it was assumed that all devices are placed in separate epitaxial pockets and each pocket is surrounded by a deep–trench isolation structure. The size of the epitaxial pocket was defined to have a length and width of 50 μm. Considering a 2D mesh (see Figure 3.2) connecting the center of each pocket to the surrounding deep–trench structure, each of these cells add additional nodes and devices R_{sub} to the simulation. The lateral and vertical components of the trench ($R_{tr,lat}$ and $R_{tr,vert}$) have to be considered in the simulation netlist as well. A quadratic chip with 1 mm^2 in size would require $\approx 2,000$ additional nodes and devices with such a rudimentary 2D lumped modeling approach. An improved version is discussed in [81]. The authors state that a 3D equivalent schematic of a test design containing four critical structures regarding minority carrier injection requires less than 100 parasitic devices which represents ≈ 0.25 mm^2 of silicon area. Although this reduction is very impressive it was decided to reduce this number even further. Since critical nodes can be identified by their connection within the design the decision was to connect injecting nodes and susceptible nodes directly to each other and to disregard non-critical structures. This leads to a parasitic netlist which size is directly related to the number of critical nodes while it is independent of the physical size of the chip. An $M \times N$ network is generated where M is the number of injectors in the design and N is the number of sensors. The depth of the substrate is taken into account by the Verilog-AMS model as a device parameter and does not influence the size of the netlist. Considering the test chip discussed in Chapter 4, a simulation setup containing all the injectors and susceptible nodes leads to a simulation netlist of approximately 300 parasitic devices. Details about the identification of the critical structures in the layout will be discussed in detail in Chapter 3.8.

This simplification of the parasitic network imposes some restrictions on the design of the chip. Independent of any technological constraints, the ground network of the chip needs to be connected to the substrate as homogeneously as possible. The technologies that were used for this thesis utilize a deep–trench filled with poly-Si (see Figure 2.1) which is connected to the substrate over its entire extent. However, the connection to the metalization is part of the chip design and can be influenced by the physical design engineer. Each connection between the metalization and the substrate via the trench can be represented by a vertical trench resistor $R_{tr,vert}$ as shown in Figure 3.2. However, when the susceptible epitaxial pocket and the nearest connection between the metalization and the deep–trench are spatially separated, the lateral component of the trench $R_{tr,lat}$ becomes dominant. The substrate connections in close proximity to susceptible epitaxial pockets can influence the coupling behavior and an example is shown in Chapter 5.3. With the limitation of only connecting the disturbance sources and the susceptible nodes

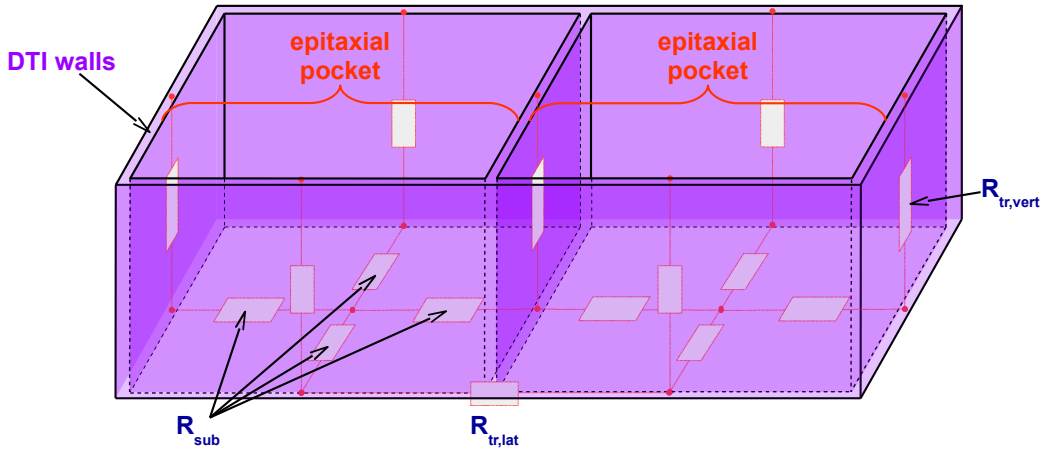


Figure 3.2: Simplified lumped network of the trench surrounding the epitaxial pocket

directly, the influence of the substrate connections can only be averaged and not fully captured by the simulation.

The same limitation is valid for the epitaxial pockets. Any connected epitaxial pocket contributes to the reduction of minority carriers in the substrate. Contrariwise, an electrically floating pocket can propagate minority carriers to distant locations and have a negative impact on the coupling effect. Both effects cannot be reproduced by this approach because each injector–sensor pair is individually simulated without any information about the surrounding area in the layout. Details about these influences on the behavior of the charge carriers will be discussed in the following pages.

3.3 Recalling Device Physics

As described in Chapter 2.5, the parasitic effect shows strong similarities to the operating principle of a bipolar transistor. However, there are some very distinct differences in their mode of operation. This is mainly caused by the unusual geometry concerning the base region of the lateral parasitic *npn* transistor which engulfs the entire substrate of the chip. Additionally, this bipolar transistor can have several simultaneously forward biased emitter–base diodes and contains numerous collectors spread over a large area. A bipolar transistor that is intended to be used as a device in circuit design is constructed differently and the characteristics will be discussed in the following pages.

3.3.1 The Bipolar Transistor as Device

The author of [85] describes the design of a typical *npn* bipolar transistor in a bipolar technology process which is similar to the technologies used for this thesis. In an intentional *npn* bipolar transistor, the emitter is highly doped (n^{++}) while the base and collector regions are doped at lower impurity concentration levels (p and n respectively).

Figure 3.3 shows a sketch of an *npn* bipolar transistor. The impurity concentrations are simplified by step junctions where n–type and p–type doping changes abruptly at the metallurgical junction [86]. The reversible ionization reaction of the most commonly used impurity atoms can be written as

$$\begin{array}{rcl} As^0 & \Leftrightarrow & As^+ + e^- \\ P^0 & \Leftrightarrow & P^+ + e^- \\ B^0 + e^- & \Leftrightarrow & B^- \end{array} \tag{3.1}$$

where As^0 is a non-ionized Arsenic atom, As^+ is an Arsenic ion and e^- is a free electron in the crystal. Under the assumption of complete ionization, the electron density in the n^{++}–doped emitter region is $n_{E0} = N^+_{D,E}$, the hole density in the p–doped base region is $p_{B0} = N^-_{A,B}$, and the electron density in the n–doped collector region is $n_{C0} = N^+_{D,C}$. $N_{A,r}$ and $N_{D,r}$ refer to the acceptor and donor densities in the region of the transistor denoted by the index r. The minority carrier densities at thermodynamic equilibrium can be determined by solving the np-product $p \cdot n = n^2_{int}$ where n_{int} is the intrinsic carrier concentration. This leads to p_{E0} for the emitter, n_{B0} for the base, and p_{C0} for the collector respectively (see Figure 3.3).

In *active mode*, the emitter–base diode becomes forward biased and an electron current $I_{E,n}$ starts to flow from the base region into the emitter region [31] as shown in Figure 3.3. This means electrons are injected into the base region by the emitter. As minority carriers they can diffuse freely in the base region and reach the reverse biased pn junction of the base–collector diode. Some of the electrons recombine with holes causing the hole current $I_{B,p}$ that is supplied by the base terminal of the device as part of the current I_B. Similar to the electron current $I_{E,n}$ the hole current $I_{E,p}$ is caused by biasing the emitter–base diode in forward direction and $I_{E,n} \gg I_{E,p}$ is desirable to achieve high gain. In *active mode* the hole current $I_{C,p}$ is related to the leakage current of the reverse biased base–collector diode.

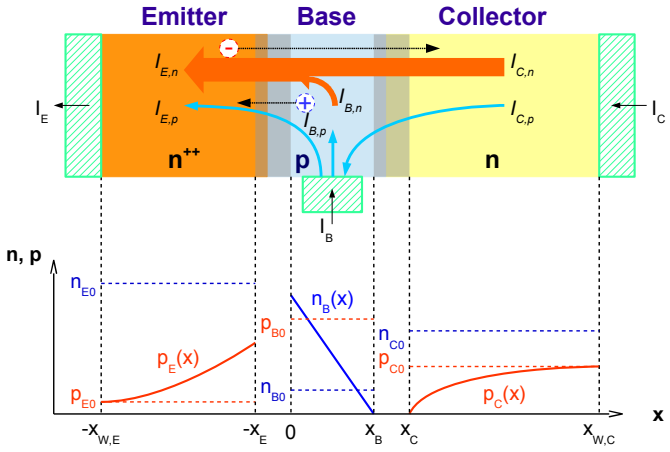


Figure 3.3: Active operation mode of an *npn* bipolar transistor

3.3.2 Selection of the Carrier Transport Model

To determine the currents at the terminals of a bipolar transistor in a simulation environment, the physical behavior inside the semiconductor material has to be determined mathematically. Over the past decades many different models were developed focusing on different physical properties of the semiconductor material and a decision had to be made which one of these models is best suited to ascertain the behavior of the parasitic bipolar transistor. These models can be split in two main groups, the semi-classical models and the quantum models [87]. The first decision was whether quantum models are necessary to describe this parasitic effect. In this case, the feature size of the devices used during circuit design is not the relevant factor because the governing structures of the parasitic device are the epitaxial layer and the substrate as shown in Figure 2.3. Quantum-mechanical effects become relevant when the variation of the electric potential is in the range of the *de Broglie* wavelength. An estimation of the electron's *de Broglie* wavelength in silicon is given by

$$p = \hbar \cdot k = \hbar \cdot \frac{2 \cdot \pi}{\lambda_B} \tag{3.2}$$

where p is the crystal momentum, $\hbar$ is the reduced Planck constant, and k is the wavevector of the electron given by $2 \cdot \pi / \lambda_B$. To solve this equation for λ_B, the energy E of the electron

$$E = \frac{p^2}{2 \cdot m_e^*} \tag{3.3}$$

can be determined using the parabolic band estimation. In this equation m_e^* is the effective mass of the electron. Near equilibrium, the average kinetic energy of an electron in the conduction band can be calculated by

$$E = \frac{3}{2} \cdot k_B \cdot T \tag{3.4}$$

which leads to an average thermal *de Broglie* wavelength for electrons of

$$\lambda_B = \sqrt{\frac{4 \cdot \pi^2 \cdot \hbar^2}{3 \cdot m_e^* \cdot k_B \cdot T}}. \tag{3.5}$$

For electrons in silicon at room temperature $\lambda_B(300\ K) \approx 7\ nm$ while the minimum size of the bipolar transistor is in the range of several micrometers. Therefore, the model domain can be reduced to the semi-classical transport models which treat the charge carriers as particles instead of waves.

The two primary categories regarding the semi-classical models are the microscopic and the macroscopic transport models. The microscopic transport models are the *Liouville* equation, the *Vlasov* equation, and the *Boltzmann Transport Equation* (BTE). The semi-classical *Liouville* equation [87] is given by

$$\partial_t f(x,k,t) + \frac{1}{\hbar} \cdot \nabla_k E \cdot \nabla_x f(x,k,t) + \frac{q}{\hbar} \cdot \nabla_x V \cdot \nabla_k f(x,k,t) = 0 \tag{3.6}$$

where $f(x,k,t)$ is the distribution function of the charge carriers. $x \in \mathbb{R}^{3M}$ is the position vector, $k \in B^{3M}$ is the pseudo-wave vector, B is the *Brillouin zone* of the lattice and M is the amount of particles that contribute to the simulated effect. The products $\nabla_k E \cdot \nabla_x f$ and $\nabla_x V \cdot \nabla_k f$ in the equation lead to a 6-dimensional phase space for every single particle. Under consideration of the doping concentrations in the regions of the transistor and the size of the affected area, the effort to numerically solve the semi-classical *Liouville* equation for a particle ensemble of this magnitude is very high and impractical. Additionally, the *Liouville* and the *Vlasov* equation are both collision-less models which means that scattering effects of the charge carriers are not taken into account. Hence, both models were excluded because the parasitic bipolar transistor is significantly larger than the *mean free path* [31]. The *mean free path* is the average distance a particle travels until it interacts with either the lattice or another particle. It can be calculated by solving

$$l_c = v_{th} \cdot \tau_c. \tag{3.7}$$

The *mean free time* τ_c is the average time between collisions and is governed by

$$\tau_c = \frac{m_e^* \cdot \mu_n}{q} \tag{3.8}$$

where m_e^* is the conductivity effective mass of the electron. For an electron in silicon at room temperature $m_e^* = 0.26 \cdot m_e$ where $m_e = 9.109 \cdot 10^{-31}\ kg$ [86]. The mobility of an electron in silicon at low doping concentration is $\mu_n \approx 1,400\ cm^2/Vs$ [88] and $\tau_c \approx 200\ fs$. The average thermal velocity v_{th} can be determined by

$$v_{th} = \sqrt{\frac{3 \cdot k_B \cdot T}{m^*}} \tag{3.9}$$

which leads to $v_{th} = 2.3 \cdot 10^7\ cm/s$ resulting in a *mean free path* $l_c \approx 50\ nm$. Hence, the minimum size of the parasitic bipolar transistor exceeds l_c by at least a factor of 100.

The *Boltzmann equation* [87] is another candidate in the set of microscopic transport models and is given by

$$\partial_t f(x,k,t) + v(k) \cdot \nabla_x f(x,k,t) + \frac{q}{\hbar} \cdot \nabla_x V \cdot \nabla_k f(x,k,t) = Q\big(f\,(x,k,t)\,\big). \tag{3.10}$$

In contrast to Equation (3.6) collisions of the charge carriers are included by setting $\frac{df}{dt} = Q(f)$ instead of 0. The physical interpretation of this assumption is that the probability density f changes over time which means the particles' trajectories change as well. The primary collision events are electron–phonon scattering, ionized impurity scattering, and carrier-carrier scattering [87]. Each of these scattering events contributes to the collision operator $Q(f)$ and is dependent on the actual properties of the semiconductor material. For example, ionized impurity scattering is mainly influenced by the doping concentration. Doping the semiconductor material creates an ionized charged impurity in the crystal lattice and introduces a free electron or hole as Equation (3.1) shows. These scattering events are also implemented in the commercial TCAD solver that was available for this work [89]. However, the semiconductor *Boltzmann equation* describes the

behavior of a single particle and has to be run multiple times to simulate a system that involves a larger ensemble of charge carriers. For example, the commercial TCAD software performs a single-particle Monte Carlo simulation [89] that needs to be preceded by a drift-diffusion simulation to obtain an initial solution for the electric field and the charge carrier distribution. Since Monte Carlo simulations significantly increase the simulation effort this approach was eliminated from the list of available candidates.

3.3.3 The Drift-Diffusion Model

The domain of macroscopic transport models can be split into two main categories, the diffusive and the hydrodynamic models and the main difference between those categories concerns the scaling of the *Boltzmann Equation* (3.10). Both sets of equations are derived under the assumption that the *mean free path* given by Equation (3.7) is much smaller than the characteristic size of the device $\alpha = l_c/l \ll 1$ and the particle experiences many collisions while traversing the device. The difference between the individual models in each category is dependent on the number of moment or weight functions that are considered by the model. To give a few examples, the weight functions can involve the particle density, current density, and the energy density. The more weight functions a model includes the higher is the order of the model. The authors of [87] provide an extensive insight on the derivation and the properties of each model. However, the focus for this thesis is to develop a circuit simulation flow and the TCAD simulation is mainly used as a basis to analyze arbitrary layout structures that were not available for measurement in the lab. Therefore, the decision was to use the simplest model first and determine whether it provides results that are accurate enough to calibrate the circuit simulation model. Under consideration of the device's operating conditions the drift-diffusion model satisfies the requirements. The electric potential applied to the device's terminals can be kept in a low voltage domain and a low-field model is applicable. The temperature range of the device is between $-40\ ^\circ C$ and $150\ ^\circ C$ and the current density at the *emitter* terminal is in the range of several hundred A/cm^2. The drift-diffusion equations were first introduced by the authors of [90] and only contain a single weight function which is the density of the particles. They are given by the following equations.

$$\frac{\partial n}{\partial t} - \frac{1}{q}\nabla \cdot \vec{J_n} = G_n - R_n \tag{3.11}$$

$$\frac{\partial p}{\partial t} + \frac{1}{q}\nabla \cdot \vec{J_p} = G_p - R_p \tag{3.12}$$

$$\vec{J_n} = q \cdot \mu_n \cdot n \cdot \vec{E} + q \cdot D_n \cdot \nabla n \tag{3.13}$$

$$\vec{J_p} = q \cdot \mu_p \cdot p \cdot \vec{E} - q \cdot D_p \cdot \nabla p \tag{3.14}$$

$$-\nabla^2\Phi = \frac{q}{\epsilon_{Si}} \cdot \left(p - n + N_D^+ - N_A^-\right) \tag{3.15}$$

Equations (3.11) and (3.12) are the so-called continuity equations which describe the temporal evolution of the charge carrier densities in the semiconductor. The right-hand side of the equations contain the thermal generation rates G_n and G_p which express the rates at which electrons and holes are generated within a certain volume of the semiconductor material. The terms R_n and R_p are their counterpart and determine the rate of carrier recombination. These rates can be influenced by changing the temperature of the material or by exposing it to a light source.

Equations (3.13) and (3.14) are the current density equations containing the drift and diffusion terms of the charge carriers. They describe the average motion of the charge carriers caused either by an electric field or by a spatial imbalance of the carrier densities in the semiconductor. The diffusion term is dependent on the spatial gradients ∇n and ∇p of the charge carriers and the diffusion constants D_n and D_p of the material. The drift term depends on the electric field $\vec{E}$ and the charge carrier mobilities μ_n and μ_p. The total current density is obtained by taking the sum of the electron and the hole current density which yields

$$\vec{J} = \vec{J_n} + \vec{J_p} = (q \cdot \mu_n \cdot n + q \cdot \mu_p \cdot p) \cdot \vec{E} + q \cdot D_n \cdot \nabla n - q \cdot D_p \cdot \nabla p. \tag{3.16}$$

The drift term is related to *Ohm's law* $\vec{E} = \rho\vec{J}$ where ρ is the resistivity of the material. By using the conductivity σ as the reciprocal of the resistivity Ohm's law becomes $\vec{J} = \sigma\vec{E}$ and the conductivity of the semiconductor is given by

$$\sigma \approx q \cdot \mu_n \cdot n + q \cdot \mu_p \cdot p. \tag{3.17}$$

Poisson's Equation (3.15) for semiconductors is derived from *Maxwell's* equations (specifically *Gauss's law*) $\nabla \cdot D = \rho$ and $D = \epsilon E$, where D is the displacement field, ϵ stands for the permittivity of the material and ρ is the charge density. This is not to be confused with the resistivity used by Ohm's law. The relationship between the electric potential Φ and the electric field is given by $E = -\nabla\Phi$ and leads to Poisson's equation in its general form given by

$$\nabla \cdot (\epsilon\nabla\Phi) = -\rho. \tag{3.18}$$

For semiconductors the total charge density ρ is split into several parts which represent the fixed charges and the free charges inside a unit volume of the material. The fixed charges N_D^+ and N_A^- are introduced to the material by means of doping and refer to ionized charges in the crystal lattice as shown by Equation (3.1). This also creates free charges n and p that represent the electrons and holes in the semiconductor which are available for electric conduction. Based on these equations the first estimations about the behavior of the parasitic bipolar transistor were performed and are discussed in the following pages.

3.3.4 Carrier and Current Densities in a 1D Bipolar Transistor

Depending on the design of the base region and its material properties the amount of minority carriers reaching the base–collector diode can be influenced. For example, a higher doping rate in the base region also increases the density of the recombination centers and therefore reduces the amount of carriers diffusing to the collector. Another possibility is to change the width x_B of the base region. The curves $p_E(x)$, $n_B(x)$, and $p_C(x)$ show the minority carrier densities in each of the regions of the transistor [31, 86]. To determine the current density in the individual regions of the transistor, the carrier concentrations have to be determined [91]. The electron current in the base of the transistor is governed by Equation (3.11). When all dynamic processes have settled down and the transistor is in steady-state the continuity equation can be simplified by setting

$$\frac{\partial n}{\partial t} = 0. \tag{3.19}$$

The devices charge carrier generation and recombination $G_n - R_n$ is represented by the *Shockley-Read-Hall* term [92]

$$R_{SRH} = \frac{n \cdot p - n_{int}^2}{\tau_p \cdot (n + n_d) + \tau_n \cdot (p + p_d)}, \tag{3.20}$$

where τ_n and τ_p are the carrier lifetimes and n_d and p_d are the free-carrier concentrations [93] in an intrinsic semiconductor. They are defined as

$$\begin{aligned} n_d &= N_c e^{\left(\frac{E_t - E_c}{k_B \cdot T}\right)}, \\ p_d &= N_v e^{\left(\frac{E_v - E_t}{k_B \cdot T}\right)}. \end{aligned} \tag{3.21}$$

In this equation E_t is the energy level of the charge carrier trap in the forbidden band region, E_c and E_v are the energy levels of the conduction and the valence band, and N_c and N_v are the effective density of states. The non-equilibrium carrier densities n and p can be expressed as

$$\begin{aligned} n &= n_0 + \delta n, \\ p &= p_0 + \delta p. \end{aligned} \tag{3.22}$$

n_0 and p_0 are the carrier densities at equilibrium and δn and δp are the excess carrier concentrations. The *Shockley-Read-Hall* term can be rewritten as

$$R_{SRH} = \frac{(n_0 + \delta n) \cdot (p_0 + \delta p) - n_{int}^2}{\tau_p \cdot (n_0 + \delta n + n_d) + \tau_n \cdot (p_0 + \delta p + p_d)}. \tag{3.23}$$

If the energy level of the trap E_t is in the center of the forbidden band—which represents the highest recombination rate—then $n_d = p_d = n_{int}$ [93]. Additionally, under low-level injection $\delta n \ll n_0$ and $\delta p \ll p_0$ this leads to

$$R_{SRH} = \frac{n_0 \cdot \delta p + p_0 \cdot \delta n}{\tau_p \cdot (n_0 + n_{int}) + \tau_n \cdot (p_0 + n_{int})}. \tag{3.24}$$

The assumptions

$$\begin{aligned} &p_0 > n_{int} > n_0, \text{and} \\ &p_0 \cdot \delta n \gg n_0 \cdot \delta p \end{aligned} \tag{3.25}$$

apply to a p–type semiconductor and the *Shockley-Read-Hall* term for the minority carriers in the base becomes

$$R_{SRH,n} = \frac{p_0 \cdot \delta n}{\tau_n \cdot (p_0 + n_{int})} = \frac{\delta n}{\tau_n} = \frac{n - n_0}{\tau_n}. \tag{3.26}$$

The second part of the solution approach is related to the current density equation

$$\vec{J_n} = q \cdot \mu_n \cdot n \cdot \vec{E} + q \cdot D_n \cdot \nabla n. \tag{3.27}$$

Under the assumption that the electric field across the base region $\vec{E} = 0$ and therefore the drift component becomes negligible, the current density equation is reduced to

$$\vec{J_n} = q \cdot D_n \cdot \nabla n. \tag{3.28}$$

Applying Equations (3.19), (3.26), and (3.28) to Equation (3.11), the continuity equation for minority carriers in the base region becomes

$$-\frac{1}{q} \cdot \nabla \cdot (q \cdot D_{B,n} \cdot \nabla n) = -\frac{n - n_0}{\tau_{B,n}}. \tag{3.29}$$

The B in the index denotes that the variables apply to the physical properties of the base region. For a 1D structure as it is illustrated in Figure 3.3 the continuity equation becomes

$$\frac{d^2 n_B(x)}{dx^2} - \frac{n_B(x) - n_{B,0}}{L_{B,n}^2} = 0, \tag{3.30}$$

where $L_{B,n} = \sqrt{D_{B,n} \cdot \tau_{B,n}}$ is the diffusion length of the electrons in the base region. The general solution for this differential equation is

$$n_B(x) = n_{B,0} + C_1 \cdot e^{-\frac{x}{L_{B,n}}} + C_2 \cdot e^{\frac{x}{L_{B,n}}}, \tag{3.31}$$

where C_1 and C_2 are the integration constants. These constants can be determined by choosing the boundary conditions [86] as

$$\begin{aligned} n_B(0) &= n_{B,0} \cdot e^{\frac{q \cdot V_{BE}}{k_B \cdot T}}, \\ n_B(x_B) &= n_{B,0} \cdot e^{\frac{q \cdot V_{BC}}{k_B \cdot T}} = 0. \end{aligned} \tag{3.32}$$

By applying these boundary conditions the solution for the electron density in the base region is

$$\begin{aligned} n_B(x) = &- \frac{n_{B,0} \cdot e^{\frac{x}{L_{B,n}}} \cdot \left(e^{\frac{q \cdot V_{BE}}{k_B \cdot T}} \cdot e^{-\frac{w_B}{L_{B,n}}} - e^{-\frac{w_B}{L_{B,n}}} + 1 \right)}{e^{\frac{w_B}{L_{B,n}}} - e^{-\frac{w_B}{L_{B,n}}}} \\ &+ \frac{n_{B,0} \cdot e^{-\frac{x}{L_{B,n}}} \cdot \left(e^{\frac{q \cdot V_{BE}}{k_B \cdot T}} \cdot e^{\frac{w_B}{L_{B,n}}} - e^{\frac{w_B}{L_{B,n}}} + 1 \right)}{e^{\frac{w_B}{L_{B,n}}} - e^{-\frac{w_B}{L_{B,n}}}} \\ &+ n_{B,0}, \end{aligned} \tag{3.33}$$

and by substituting $\sinh(x) = \frac{1}{2} \cdot (e^x - e^{-x})$ the equation can be rewritten as

$$n_B(x) = n_{B,0} \cdot \left(1 - \frac{\sinh\left(\frac{x}{L_{B,n}}\right)}{\sinh\left(\frac{w_B}{L_{B,n}}\right)} + \left(e^{\frac{q \cdot V_{BE}}{k_B \cdot T}} - 1 \right) \cdot \left(\frac{\sinh\left(\frac{w_B - x}{L_{B,n}}\right)}{\sinh\left(\frac{w_B}{L_{B,n}}\right)} \right) \right). \tag{3.34}$$

The majority carrier current density of the emitter and the collector region are based on the spatial gradient of the minority carrier density in the base region at the region boundaries. This is valid when the space charge region is assumed to be free of any changes in the carrier density and therefore the current density remains unchanged as well. The equation for the emitter electron current is given by

$$\begin{aligned} J_{E,n} &= q \cdot D_{B,n} \cdot \left. \frac{dn_B(x)}{dx} \right|_{x=0} \\ &= q \cdot \frac{D_{B,n}}{L_{B,n}} \cdot n_{B,0} \cdot \left(\frac{\cosh\left(\frac{w_B}{L_{B,n}}\right)}{\sinh\left(\frac{w_B}{L_{B,n}}\right)} \cdot \left(1 - e^{\frac{q \cdot V_{BE}}{k_B \cdot T}} \right) - \frac{1}{\sinh\left(\frac{w_B}{L_{B,n}}\right)} \right) \end{aligned} \tag{3.35}$$

and the collector electron current is

$$\begin{aligned} J_{C,n} &= q \cdot D_{B,n} \cdot \left. \frac{dn_B(x)}{dx} \right|_{x=x_B} \\ &= q \cdot \frac{D_{B,n}}{L_{B,n}} \cdot n_{B,0} \cdot \left(\frac{1}{\sinh\left(\frac{w_B}{L_{B,n}}\right)} \cdot \left(1 - e^{\frac{q \cdot V_{BE}}{k_B \cdot T}} \right) - \frac{\cosh\left(\frac{w_B}{L_{B,n}}\right)}{\sinh\left(\frac{w_B}{L_{B,n}}\right)} \right). \end{aligned} \tag{3.36}$$

Similarly, the minority carrier current densities of the emitter and collector terminal are solved by calculating the gradient of the minority carrier concentrations at the interfaces of the base region. The boundary conditions for the minority carriers of the emitter region are

$$\begin{aligned} p_E(-x_{E,w} \to \infty) &= p_{E,0} \\ p_E(-x_E) &= p_{E,0} \cdot e^{\frac{q \cdot V_{BE}}{k_B \cdot T}} \end{aligned} \tag{3.37}$$

and Equation (3.12) becomes

$$\frac{d^2 p_E(x)}{dx^2} - \frac{p_E(x) - p_{E,0}}{L_{E,p}^2} = 0, \tag{3.38}$$

where $L_{E,p} = \sqrt{D_{E,p} \cdot \tau_{E,p}}$ is the diffusion length of the holes in the emitter region. With the solution for the minority carrier density in the emitter region, the current density can be calculated by

$$\begin{aligned} J_{E,p} &= -q \cdot D_{E,p} \cdot \left. \frac{dp_E(x)}{dx} \right|_{x=-x_E} \\ &= -q \cdot \frac{D_{E,p}}{L_{E,p}} \cdot p_{E,0} \left(\frac{\cosh\left(\frac{w_E}{L_{E,p}}\right)}{\sinh\left(\frac{w_E}{L_{E,p}}\right)} \right) \cdot \left(e^{\frac{q \cdot V_{BE}}{k_B \cdot T}} - 1 \right). \end{aligned} \tag{3.39}$$

This solution can be simplified since $\coth(\alpha) = \cosh(\alpha) / \sinh(\alpha)$ and assuming $w_E \gg L_{E,p}$ this leads to $\coth(w_E) \approx 1$ and the hole current for the emitter becomes

$$J_{E,p} = -q \cdot \frac{D_{E,p}}{L_{E,p}} \cdot p_{E,0} \cdot \left(e^{\frac{q \cdot V_{BE}}{k_B \cdot T}} - 1 \right). \tag{3.40}$$

Likewise, the boundary conditions for the collector region are

$$\begin{aligned} p_C(x_{w,C} \to \infty) &= p_{C,0} \\ p_C(x_C) &= p_{C,0} \cdot e^{\frac{q \cdot V_{BC}}{k_B \cdot T}} = 0 \end{aligned} \tag{3.41}$$

and Equation (3.12) becomes

$$\frac{d^2 p_C(x)}{dx^2} - \frac{p_C(x) - p_{C,0}}{L_{C,p}^2} = 0. \tag{3.42}$$

In this case $L_{C,p}$ is the diffusion length of the holes in the collector region. This leads to the solution for the collector hole current which is

$$J_{C,p} = -q \cdot D_{C,p} \cdot \left. \frac{dp_C(x)}{dx} \right|_{x=x_C} = q \frac{D_{C,p}}{L_{C,p}} \cdot p_{C,0}. \tag{3.43}$$

The source code of the symbolic calculations that were used to perform the derivations of the equations in this chapter can be found in Appendix C.

The cross sectional area of the transistor is denoted by A and assumed to be the same for the emitter and the collector region. This is not necessarily the case for an on-chip bipolar transistor which is illustrated by the *npn* device in Figure 2.1. In this example the current at the collector and the emitter can be determined by the sum of the electron and hole current density multiplied by the area which yields

$$I = A \cdot (J_n + J_p) \tag{3.44}$$

and the base current is simply determined by

$$I_B = I_E - I_C. \tag{3.45}$$

In this 1D example there is no dedicated boundary available that reflects the base terminal and the base current can only be deduced by the difference of the collector and emitter current. In higher dimensional simulations the base terminal has its own boundary conditions and the current is determined by the carrier gradient within the region. However, concerning the basic operating principle a 1D model already provides sufficient insight.

3.3.4.1 The Long-Base Bipolar Transistor

The solutions given by the Equations (3.35), (3.36), (3.40), and (3.43) show the major influences on the performance of a bipolar transistor. The collector and the emitter currents are both dependent on the design of the base region. If the width of the base

satisfies $x_B > L_{B,n}$, then a significant amount of minority carriers recombines within the base region and the carrier density given by Equation (3.34) looks as illustrated in Figure 3.4. This means most of the electrons that are injected from the emitter into the base never reach the base–collector pn junction. The electron recombination in the base region has to be sustained by a hole current $I_{B,p}$ and therefore reduces the efficiency of the bipolar transistor. A transistor of this design is not desirable as device but its base region shows similarities to the structure of the parasitic bipolar transistor.

The boundary conditions for the base region are stated in Equation (3.32) and show that the minority carrier density $n_B(0)$ of the forward biased base–emitter diode is mainly governed by the applied electric potential difference between the two terminals. The minority carrier density at the base–collector diode however is equal to zero. The assumption is that all minority carriers that diffuse into the space charge region of the reverse biased pn junction get extracted from the base and traverse into the collector region. When a sufficient amount of carriers reach the collector its boundary condition $p_C(x_c)$ becomes zero as well as stated in Equation (3.41). Similarly to $n_B(0)$, $p_E(-x_E)$ is related to the applied voltage V_{BE} as shown by the boundary conditions described by Equation (3.37). Both, the collector and the emitter width are larger than their respective diffusion lengths of the regions ($x_{w,C} \to \infty$ and $x_{w,E} \to \infty$). Under these conditions, the minority carrier gradients are small and the diffusion currents are at their minimum. This can be influenced by changing the width of the regions.

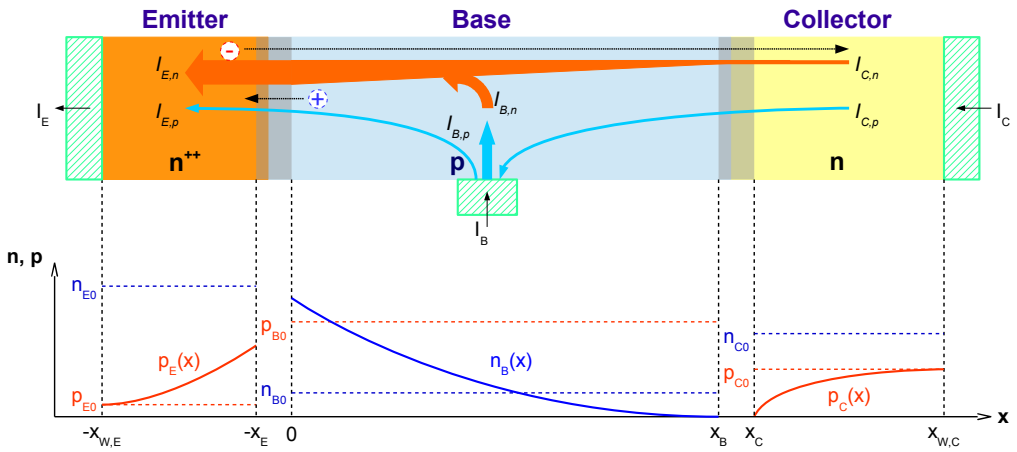


Figure 3.4: Active operation mode of an npn bipolar transistor with long base

3.3.4.2 The Short-Base Bipolar Transistor

In an intentional bipolar transistor as it is shown in Figure 3.3, the base width is smaller than the diffusion length of the minority carriers and $x_B < L_{B,n}$ applies. In this case the carrier recombination rate becomes very low $R_n \to 0$ and Equation (3.30) becomes

$$\frac{d^2 n_B(x)}{dx^2} = 0 \tag{3.46}$$

which leads to $J_n = constant$. This means the slope of the minority carrier gradient in the base region is linear. As stated in [31], Equation (3.34) can be linearized by substituting $\sinh(\lambda) \approx \lambda$ which leads to

$$n_B(x) = n_{B,0} - n_{B,0} \cdot \frac{x}{w_B} + n_{B,0} \cdot e^{\frac{q \cdot V_{BE}}{k_B \cdot T}} \cdot \frac{w_B - x}{w_B} - n_{B,0} \cdot \frac{w_B - x}{w_B}. \tag{3.47}$$

Finally, the linearized equation of the minority carrier density becomes

$$n_B(x) = n_{B,0} \cdot e^{\frac{q \cdot V_{BE}}{k_B \cdot T}} \left(1 - \frac{x}{w_B}\right) \tag{3.48}$$

and the minority carrier density in the base becomes a straight line as show in Figure 3.3. Since $J_{E,n}$ and $J_{C,n}$ are both dependent on the gradient of $n_B(x)$ and the width of the base region can be used to influence the efficiency of the bipolar transistor.

Another important factor regarding the performance of a bipolar transistor is the *emitter efficiency* [31, 86] which is defined as the ratio between the majority carrier current and the total current of the emitter given as

$$\gamma_E = \frac{I_{E,n}}{I_E} = \frac{1}{1 + \frac{D_{E,p} \cdot L_{B,n} \cdot p_{E,0}}{D_{B,n} \cdot L_{E,p} \cdot n_{B,0}} \cdot \frac{\sinh\left(\frac{w_B}{L_{B,n}}\right) \cdot \coth\left(\frac{w_E}{L_{E,p}}\right) \cdot \left(e^{\frac{q \cdot V_{BE}}{k_B \cdot T}} - 1\right)}{1 + \cosh\left(\frac{w_B}{L_{B,n}}\right) \cdot \left(1 + e^{\frac{q \cdot V_{BE}}{k_B \cdot T}}\right)}} \tag{3.49}$$

While for a typical bipolar transistor this is just one performance factor amongst many it is a key factor describing the efficiency of the parasitic bipolar transistor. Equation (3.49) shows which of the physical parameters of the transistor's regions influences the ratio between the total emitter current and its contribution by the base region's minority carriers. This describes the ratio of injection caused by the source of disturbance on the chip. For example, a highly n–doped emitter region causes $p_{E,0}$ to become very low which increases the efficiency and therefore worsens the parasitic effect. In addition, when $w_B \ll L_{B,n} \implies \sinh\left(\frac{w_B}{L_{B,n}}\right) \to 0$ and the emitter efficiency $\gamma_E \to 1$. Concerning the parasitic coupling effect the desire is to keep the injection efficiency as low as possible. Judging by Equation (3.49) the circuit designer is basically left with only two possibilities:

- change the distance between the injector and the sensor $w_B \sim d_{Inj,Sen}$, and/or
- change the injection level by means of $V_{BE} \sim V_{Inj}$.

3.3.5 The Bipolar Transistor as Parasitic Element

The situation increases in complexity considering the parasitic element while the underlying physical principle remains the same. For the time being the regions of the transistor are still ideal and no voltage drops occur. Under this assumption the first analysis is purely based on the behavior of the minority carriers in each region. Figure 3.5 shows a 2D cross section of an active injector and illustrates the corresponding minority carrier

distributions in the different regions of the parasitic device. The minority carrier injection into the substrate occurs at the forward biased base–emitter junction and the same boundary conditions of Equation (3.37) apply. With the n–doped epitaxial pocket being engulfed by the deep–trench isolation the path from the top of the silicon down to the *pn* junction can be simplified to a one-dimensional structure. However, this simplification neglects all the influences caused by the Si/SiO_2 interface and also the sidewall capacitances between the epitaxial pocket and the poly-Si inside the trench and has therefore limited capability regarding dynamic processes.

The same simplifications are utilized regarding the base–collector junctions. In contrast to the examples in the previous chapters, the transistor now consists of numerous base–collector junctions. Considering the operating conditions of a bipolar transistor as device, the parasitic transistor is usually operated in *active mode*. In this case the base–emitter junction is forward biased and the base–collector junction is reverse biased. Under these conditions, the boundary conditions of Equation(3.41) are still valid although $p_C(x_C)$ may not necessarily become zero. The applied voltage V_{BC} at the collector is mainly relevant when the transistor is operated in *saturation mode* and the base–collector junction becomes forward biased. However, when V_{BC} is small enough and the base–collector junction remains reverse biased the minority carrier density p_C at the interface to the space charge region is not 0. By applying these boundary conditions the hole current density $J_{C,p}$ of the collector and $J_{E,p}$ of the emitter can be determined.

The base region becomes subjected to multiple boundary conditions and it cannot be reduced to a 1D simulation domain any more. The boundary condition $n_B(0)$ of Equation (3.32) still defines the base–emitter interface. It remains valid as long as the voltage drop in the substrate and the epitaxial pocket is negligible. However, the second boundary condition $n_B(x_B)$ needs to be applied to every base–collector interface and the position coordinate x_B needs to be adapted to the coordinate system of the substrate's simulation domain. For a 2D setup in a Cartesian coordinate system Equation (3.30) becomes

$$\frac{\partial^2 n_B\left(x,y\right)}{\partial x^2} + \frac{\partial^2 n_B\left(x,y\right)}{\partial y^2} - \frac{n_B\left(x,y\right) - n_{B,0}}{L_{B,n}^2} = 0 \tag{3.50}$$

and the electron current density for the i-th collector is governed by

$$J_{Ci,n} = q \cdot D_{B,n} \cdot \left(\frac{\partial n_B(x,y)}{\partial x}\hat{\mathbf{x}} + \frac{\partial n_B(x,y)}{\partial y}\hat{\mathbf{y}} \right)\Bigg|_{x=x_i, y=y_i}. \tag{3.51}$$

With increasing distance from the injector, the gradient decreases and the parasitic current at the epitaxial pockets becomes smaller. This is illustrated in Figure 3.5 by the decline of $n_B(x,y)$ over the distance from the injector. The minority carrier densities $p_{C1}(y)$ to $p_{C5}(y)$ in the collector regions are considered to be independent of the collected electron current coming from the base region.

While the analysis of the minority carriers provides a good phenomenological description of the parasitic bipolar transistor it is insufficient to accurately cover its behavior. For example, at the emitter it is difficult to argue that the electric field in the substrate remains negligible considering the size of the base region. With dimensions in the range of

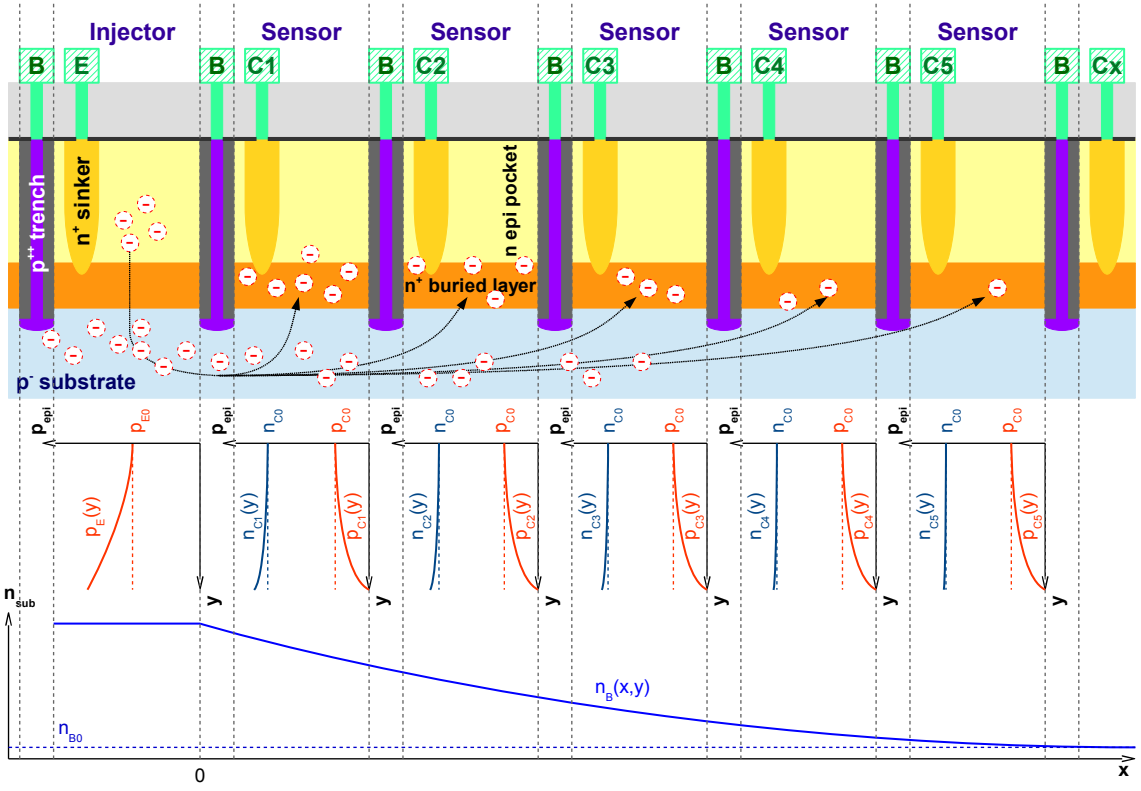


Figure 3.5: The parasitic *npn* transistor in active operation mode

several millimeters there will be a significant resistance and the electric potential will be inhomogeneous. Therefore, the boundary conditions of Equation (3.37) need to include the voltage drop in the base region. This cannot be performed in an analytical manner due to the size and complexity of the overall structure.

Also at the base–collector interface the boundary conditions of Equation (3.41) have to be improved. When the electrons traverse the space charge region they "become" majority carriers and are shown as $n_{C1}(y)$ to $n_{C5}(y)$ in Figure 3.5. This causes a deviation from the thermal equilibrium that existed between the charge carriers in the collector region. There are basically two processes available to regain equilibrium conditions which are carrier recombination or dielectric relaxation. The governing factor for carrier recombination is the carrier lifetime. The carrier lifetimes τ_n and τ_p for silicon are somewhere between 1 ns and 1 ms depending on the dopant concentration of the material. The dielectric relaxation time for electrons in an n–doped material [88] is defined as

$$\tau_{diel,n} = \frac{\epsilon_0 \cdot \epsilon_{Si}}{q \cdot \mu_n \cdot n_0} \tag{3.52}$$

where ϵ_0 is the vacuum permittivity and ϵ_{Si} is the relative permittivity of silicon given as 11.68. Solving this equation for typical doping concentrations leads to values for the dielectric relaxation between 1 fs and 1 ns. While the relaxation time describes the temporal decay of the charge carrier imbalance, the *Debye length* [88] describes the spatial

reduction of the majority carrier imbalance and is defined as

$$L_{Debye,n} = \sqrt{\frac{\epsilon_0 \cdot \epsilon_{Si} \cdot k_B \cdot T}{q^2 \cdot n_0}}. \tag{3.53}$$

The carrier imbalance caused by the electrons moving into the collector regions locally changes the electric potential and introduces an electric field. This field influences the transport of the majority carriers but also attracts minority carriers as a balance to the increased majority carrier density close to the space charge region. This effect can be determined by solving Poisson's Equation (3.18) which relates the electric potential Φ to the fixed ionized charges N_D^+ and N_A^- and the free charges n and p. This shows that the carrier transport phenomenon in the collector region is governed by relaxation and drift since these two processes are significantly faster than carrier recombination.

In the previous examples ambipolar current transport was not taken into account and only the behavior of the minority carriers was considered. Additionally, in this example the base region of the parasitic transistor is only subjected to a single boundary condition that causes a flux of electrons into the region while all other boundaries extract carriers from it. In a numerical solver this setup does not show the real behavior because the two closest collectors extract all the electrons and the carrier density in the remaining region becomes zero. The balance within the base region needs to be provided by adding the majority carriers to the domain and relate the carrier densities to each other by Poisson's equation. Under these aspects the properties of the base region need to be addressed in more detail.

3.3.6 The Common Substrate

The base region of the parasitic bipolar transistor is formed by the substrate of the chip. The two test chips that were developed during the course of this thesis (see Chapter 4) utilize boron–doped *CZ*-grown silicon wafers. *CZ*-grown silicon crystals have very low crystalline defect rates and contamination levels are also very low. Considering the boron dopant concentration of the substrate the diffusion length of the electrons was expected to be several hundred micrometers. The highly n–doped buried layer is introduced by a shallow *seed* implantation at the surface of the substrate before the epitaxial layer is grown on top of it [1]. The thermal conditions in the following process steps cause diffusion of the dopant ions and influences the final doping profile of the buried layer. The *n*–doped epitaxial layer is separated by the deep–trench etch process. The final deep–trench reaches from the top of the silicon surface down into the substrate and the poly-Si provides the electrical connection to the substrate. Hence, the substrate is subject to several different interfaces as illustrated in Figure 3.8.

The interface with the largest area is formed by the back side of the chip. There are several possibilities what kind of connection can be made to the back side. There are products that require a metalization layer to be deposited on the back side and the chip is fixed inside the package by means of soldering. Depending on the doping concentration of the silicon and the type of metal this connection can either be a Schottky or an ohmic

contact. Another option was used regarding the two test chips. The back sides of the test chips were cleaned and oxidized and both were glued to the lead frame of the ceramic package by a non-conductive adhesive. In this case, the surface recombination velocity of the Si/SiO_2 interface is the dominant parameter and is expected to be at $\approx 600\ cm/s$ [94]. The type of back side connection needs to be addressed individually for each design because the requirements differ from product to product.

Another significant interface to the parasitic coupling effect is formed by the side walls of the chip. This interface comes into existence very late in the chip production when the die is cut into separate ICs. There are several different dicing processes available but what all of them have in common is that the surface of the cut is not as smooth as the back side of the chip. In addition, the side wall is not being processed any further except that the IC is mounted into the package and some of the adhesive may cover the sides of the chip as well. However, even at room temperature a thin layer of SiO_2 is created by natural oxidation measuring a few $\mathring{A}$. The distance between the chip edge and any active devices depends on the layout of the seal ring and the saw street. Surface recombination velocity is the governing parameter of the chip edge but due to the defects caused during the wafer dicing it is expected to contain more recombination centers than a smooth silicon surface. Based on the results for oxidized and bare silicon shown by the authors of [94] the surface recombination velocity is expected to be $600\ cm/s < S_n < 50,000\ cm/s$. However, no measurements were performed to confirm these values.

The substrate comes into contact with two different materials at the deep–trench. The side walls of the trench are covered by SiO_2 and the inside of the trench is filled with a highly p–doped poly-Si. As far as the SiO_2 is concerned it can be modeled similarly to the interface of the chip's back side since the trench etch process also causes a very smooth surface between the silicon and the poly-Si. However, even after thermal annealing the silicon inside the trench will remain polycrystalline and the recombination rate is higher than in crystalline silicon. The dopant diffuses outward into the substrate resulting in a gradient in the dopant concentration reaching from the trench into the surrounding substrate.

The remaining area of the substrate's surface is connected to the highly doped n–epitaxial layer which either becomes a base–emitter or a base–collector pn junction dependent on the biasing conditions of the epi pocket. When the base–emitter diode becomes forward biased electrons get injected into the substrate and at the same time holes get injected into the epitaxial pocket. Inside the epitaxial pocket the minority carriers are restricted in their movement by the confines of the surrounding deep–trench. They recombine with the majority carriers which are constantly supplied by the connection to the metalization of the chip. In the substrate the injected minority carriers are free to move into all three dimensions. They recombine with the holes in the substrate which are supplied by the deep–trench network connecting the substrate to the ground potential of the chip. However, the assumption that the resistance of the substrate is negligible is not valid any more and the injected electrons will locally decrease the electric potential of the substrate. Under these conditions an electric field $\vec{E}$ is introduced to the substrate. This electric field causes an additional drift current besides the diffusion current which is generated by the charge carrier's gradients. These effects are illustrated in Figure 3.6.

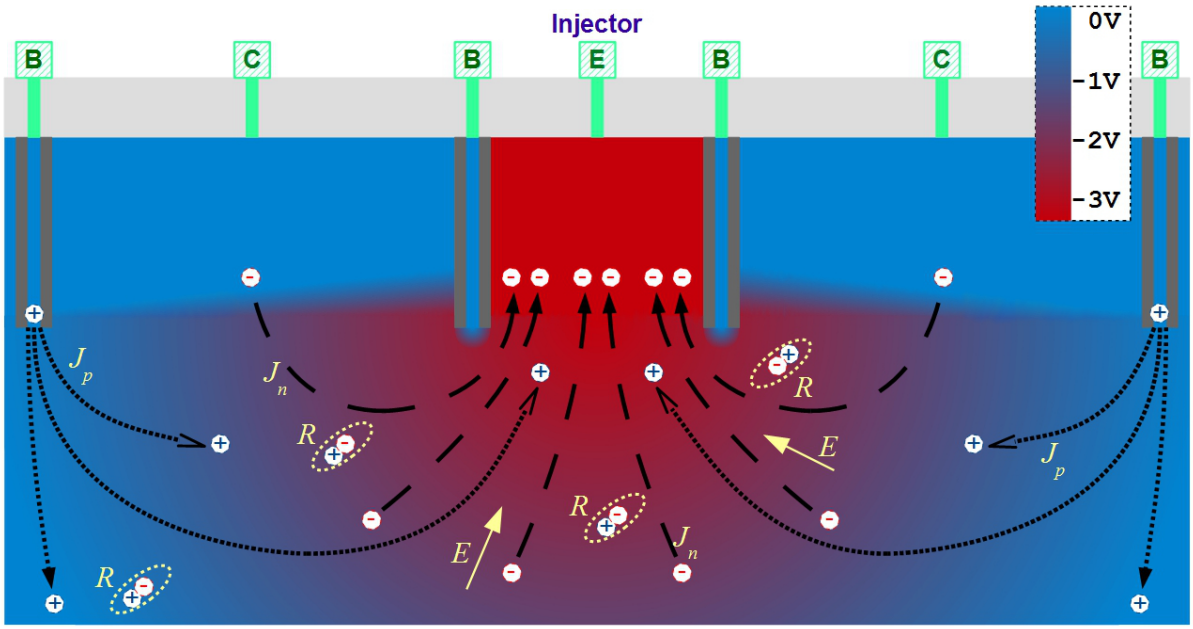


Figure 3.6: Electric potential and current densities under injection condition

The arrows labeled as J_p and J_n in Figure 3.6 show the direction of the electron and the hole current density. The electric field $\vec{E}$ is directed from the regions of higher electric potential towards the injector region where the potential is pulled below 0 V by the surplus of negative charge carriers. The electric field in combination with the electron density gradient accelerates the electrons outward into the substrate and at the same time attracts holes to move towards the region underneath the injector to balance the excess electrons. In the entire structure there are two effects that reduce the surplus of minority carriers. The first effect refers to carrier recombination which is given by Equation (3.20). The main factor of carrier generation and recombination is calculated by the carrier density product $n \cdot p$ which becomes positive in the case of excess carriers and negative in case of deficient carriers. The two terms in the denominator determine the recombination rate for each of the carriers individually. The governing factor is the deviation of the equilibrium carrier concentration multiplied by the carrier lifetime.

The second part that contributes to the reduction of the excess electrons are the reverse biased base–collector pn junctions. Basically every electron that diffuses into the space charge region of a collector is one less electron that recombines within the substrate area. The measurement results in Figure 3.7 show the influence caused by the connectivity of the epitaxial pockets on the charge carrier distribution in the substrate. The measurement labeled as $M1$ was performed with all collectors connected to the ground potential. This is the usual case for most product ICs although some technologies do not require all their epitaxial pockets to be connected which might seriously degrade reverse current performance of a design. Contrariwise, the measurement labeled as $M2$ had all the collectors floating.

The difference between those two measurements can be explained by considering what

happens inside the collector in those cases. Any electron that traverses the space charge region of any electrically well connected collector gets extracted by the connection to the metalization. In the second case when the epitaxial pocket is floating the electrons that pass through the depletion region remain in the collector. They lower the electric potential of the pocket until the space charge region dissipates. The epitaxial pocket assumes the same voltage level as the substrate underneath and the electrons move "freely" between both regions. In this case the electron ensemble diffuses primarily through the substrate and is only subjected to recombination. By taking the results for the minority carrier lifetime in boron doped CZ bulk silicon provided by the authors of [95] under consideration $\tau_n \approx 1\ ms$ for the two test chips. In this case the diffusion length of the minority carriers $L_n \approx 1\ mm$. This experiment was performed to establish whether recombination is the dominant factor of the spatial decay of the minority carriers or if there are other factors present as well. It confirms low recombination rates in qualitatively high CZ silicon substrate and shows that a significant amount of minority carriers is extracted by the base–collector junctions. On a productive IC it is very unlikely that all epitaxial pockets are electrically floating and this effect will not be included in the final circuit simulation model.

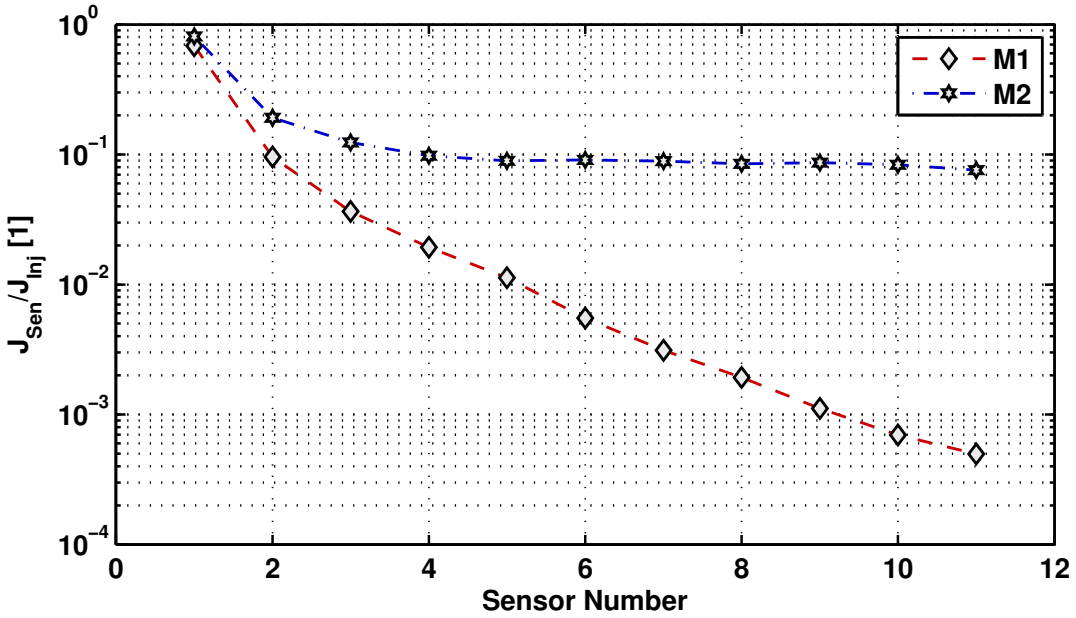


Figure 3.7: Influence on the electron current by the connection of the collectors

Some additional information needs to be provided about this measurement. The measurement setup is discussed in Chapter 4.4.1. The applied voltage at the injector V_{Inj} had to be increased by $\approx 30\ \%$ to obtain the same injection current I_{Inj} for the results labeled as $M2$. The reason is that the series resistance at the substrate side of the measurement increases due to the missing contribution of epitaxial pockets. This also increases the voltage drop inside the substrate and for the first sensor rows the current transport is not purely diffusive which explains the strong deviation at the first three sensor nodes.

Outside of the electric field's influence, the current transport becomes primarily diffusive. The measurement itself also influences the behavior inside the substrate because the sensor node used for the measurement had to be connected. However, this influence is very low because the size of a single sensor node is $\approx 2,900\ \mu m^2$ while the entire test chip has an area of $\approx 2\ mm^2$.

3.4 Splitting the Bipolar Transistor

Due to the size of the affected area and the arbitrary amount of terminals it is necessary to split the parasitic device into smaller fragments. One possible setup for such an approach is illustrated in Figure 3.8. It contains one-dimensional simulation domains for the emitter and the collector regions and a 2D domain representing the substrate. The cross section through the area affected by the parasitic coupling effect is primarily split at the *pn* junction of the epitaxial well and the substrate. The basic concept discussed in Chapter 3.3.4 about how to determine the current densities can be applied to the individual regions in this setup as well. The simulation domain Ω_E represents the emitter region and is bounded by Γ_E and Γ_{Em}. The two primary collector regions are Ω_{C1} and Ω_{C2} and the main difference between them is the dopant concentration of the epitaxial layer. Ω_{C1} contains a low ohmic connection to the buried layer while Ω_{C2} has a connection with a higher resistance. The boundaries Γ_{C1} and Γ_{C2} are exemplary for all the collector–substrate interfaces. The third possibility is to keep an epitaxial well electrically floating which is represented by Ω_{Cf} and the boundary at the pocket–substrate interface is denoted as Γ_{Cf}. With this basic setup the emitter and the collector regions can be simulated separately as long as the boundary conditions are set up properly.

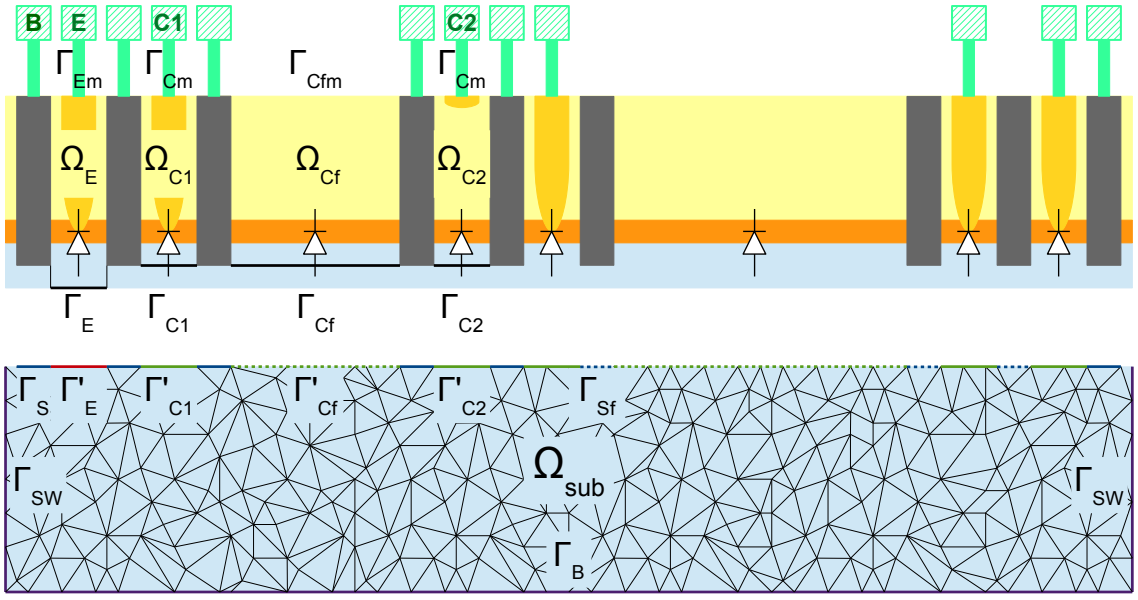


Figure 3.8: Mixed 1D–2D modeling approach

The third simulation domain Ω_{sub} is the substrate which shares some of its boundaries with the collector regions. The emitter's boundary Γ'_E is at a different position than Γ_E of Ω_E. The electrical connection of the substrate to the ground potential is provided at Γ_S and a high ohmic or even floating interface to the deep–trench network is at Γ_{Sf}. As discussed in the previous chapter, the back side of the chip and the side walls form boundaries of the substrate and are labeled as Γ_B and Γ_{SW}.

To fully determine the drift-diffusion model given by Equations (3.11) to (3.15) and to consider ambipolar carrier transport the boundary conditions described in Chapter 3.3.4 have to be enhanced to include the majority carriers and the electric potential. The boundary conditions for the individual simulation domains can be given as *Dirichlet* or *Neumann* boundary conditions. Each boundary condition $\partial\Omega$ for a given boundary Γ consists of a set of three values. These values can either be the carrier densities n and p, and the electric potential Φ, or their spatial gradients ∇n and ∇p, and the electric field $\vec{E}$.

The one-dimensional emitter's simulation domain Ω_E is enclosed by the boundaries Γ_E and Γ_{Em}. Γ_{Em} is an ohmic contact where the carrier concentrations are fixed and no charges are trapped at the interface. This means the dopant and carrier concentrations at the surface are balanced and $p_s - n_s + N^+_{D,s} - N^-_{A,s} = 0$. The quasi-Fermi potentials Φ_n and Φ_p of the electrons and holes are equal to the applied bias voltage V_{BE} at the terminal. By using the Boltzmann-Maxwell distribution [86] the surface potential of the interface is given as

$$\Phi_s = \Phi_n + \frac{k_B \cdot T}{q} \cdot \ln\left(\frac{n_s}{n_{int}}\right) = \Phi_p + \frac{k_B \cdot T}{q} \cdot \ln\left(\frac{p_s}{n_{int}}\right). \tag{3.54}$$

The electron density of the n–doped emitter region is determined by $n_s = N^+_{D,s}$ and the minority carrier concentration can be calculated by using the pn product which leads to $p_s = n^2_{int}/n_s$. The same concept is used for the boundary Γ_E which resides a few micrometers beneath the pn junction. The boundary is shifted inside the substrate to emulate the substrate's behavior to obtain reasonable boundary conditions for the virtual substrate boundary Γ'_E. The boundary conditions for Ω_E are

$$\partial\Gamma_{Em} \begin{cases} n_s &= N^+_{D,s} \\ p_s &= n^2_{int}/n_s \\ \Phi_s &= \Phi_n + \frac{k_B \cdot T}{q} \cdot \ln\left(\frac{n_s}{n_{int}}\right) \end{cases} \tag{3.55}$$

for the n–doped boundary at the chip's surface and

$$\partial\Gamma_E \begin{cases} n_s &= n^2_{int}/p_s \\ p_s &= N^-_{A,s} \\ \Phi_s &= 0 \end{cases} \tag{3.56}$$

for the p–doped boundary inside the substrate.

The boundary condition $\partial\Gamma_{Cm} = \partial\Gamma_{Em}$ for the ohmic contact of the collector nodes. The interface Γ_{C1} to the substrate is subjected to boundary conditions based on the

substrate's simulation results and are mixed boundary conditions. A pure diffusion current requires

$$-\hat{\mathbf{y}} \cdot \nabla\Phi = \hat{\mathbf{y}} \cdot \vec{E} = 0 \tag{3.57}$$

where $\hat{\mathbf{y}}$ denotes the normal to the boundary Γ_{C1}. As a first-order approximation the hole current is also assumed to be zero which leads to

$$\partial\Gamma_{C1} \begin{cases} n_s &= n_{sub}|_{\Gamma'_{C1}} \\ \hat{\mathbf{y}} \cdot \nabla p_s &= 0 \\ \hat{\mathbf{y}} \cdot \nabla\Phi_s &= 0 \end{cases} \tag{3.58}$$

defining the electron current of the collector Ω_{C1}.

The boundary Γ_{Cfm} at the chip's surface of the floating collector region Ω_{Cf} represents an interface between silicon and an insulator and the assumption $J_n = J_p = 0$ is valid. If surface charges are ignored the *Neumann* boundary conditions for such an interface are all set to 0 and no current is flowing in or out of the boundary Γ_{Cfm} which imposes the same requirement for Γ_{Cf}. Hence, the boundary conditions of the chip's surface can also be applied to the substrate's boundary Γ'_{Cf} which become

$$\partial\Gamma'_{Cf} \begin{cases} \hat{\mathbf{y}} \cdot \nabla n_s &= 0 \\ \hat{\mathbf{y}} \cdot \nabla p_s &= 0 \\ \hat{\mathbf{y}} \cdot \nabla\Phi_s &= 0 \end{cases} \tag{3.59}$$

representing an ideal reflective interface. These assumptions are only valid under static conditions and when there are no significant contributions caused by leakage currents at all the epitaxial pocket's interfaces.

The boundary Γ'_E of the substrate domain Ω_{sub} geometrically overlaps with the emitter domain Ω_E and uses the simulation results of Ω_E as boundary conditions $\partial\Gamma'_E$ which are

$$\partial\Gamma'_E \begin{cases} \hat{\mathbf{y}} \cdot \nabla n_{sub} &= \hat{\mathbf{y}} \cdot \nabla n_E|_{\Gamma'_E} \\ \hat{\mathbf{y}} \cdot \nabla p_{sub} &= \hat{\mathbf{y}} \cdot \nabla p_E|_{\Gamma'_E} \\ -\hat{\mathbf{y}} \cdot \nabla\Phi_{sub} &= -\hat{\mathbf{y}} \cdot \nabla\Phi_E|_{\Gamma'_E}\,. \end{cases} \tag{3.60}$$

Hence, the one-dimensional simulation results provided by Ω_E are mapped on every grid point of the boundary Γ'_E. By using the spatial derivatives of the charge carrier concentrations and the electric potential this boundary defines the electron's and hole's drift and diffusion currents.

The substrate's side of the collector boundary Γ'_{C1} is treated differently than Γ_{C1}. At this boundary we also assume that the entire hole current and additionally the drift component of the electron current is zero. However, all electrons that reach the depletion region are extracted from the substrate and move into the collector. The boundary conditions become

$$\partial\Gamma'_{C1} \begin{cases} n_{sub} &= 0 \\ \hat{\mathbf{y}} \cdot \nabla p_{sub} &= 0 \\ \hat{\mathbf{y}} \cdot \nabla\Phi_{sub} &= 0. \end{cases} \tag{3.61}$$

The ohmic contact at the top of the trench structure was mapped directly at the surface of the substrate to simplify the geometrical setup of Ω_{sub}. The resistance contribution of the trench and the increased carrier recombination rate inside the poly-Si was not included in this model. The ohmic contact was set up similarly to $\partial\Gamma_E$. Any floating or high-ohmic trench contacts were also assumed the be ideal reflective surfaces like Γ'_{Cf}. Finally, the remaining boundaries Γ_{SW} and Γ_B were also assumed to be reflective for the first feasibility study of the simulation setup.

3.5 FDM/FEM Feasibility Study

The concept discussed in the previous chapter is based on simulating the parasitic coupling effect at a cross section through the chip. The axis of the cross section passes through the closest points of the injector node and the susceptible node of interest. The question that needs to be answered is whether the point–to–point modeling scheme is applicable to accurately analyze the effect observed on the available test chips. The first approach that was investigated is based on a simplified one-dimensional solver that was intended to be implemented directly in a circuit simulation model. At the injector side of the setup a 1D model of the emitter–base diode determines the electric potential and carrier densities at a certain depth underneath the epitaxial pocket. The collector–base diode uses the carrier density information of the substrate and calculates the parasitic coupling current at the sensor side. These two parts of the coupling path are connected by a 2D representation of the substrate which covers the spatial propagation of the charge carriers.

3.5.1 1D FDM Diode Model

To numerically solve the Equations (3.11) to (3.15) some adaptations have to be made. The charge carrier densities in Poisson's Equation (3.15) are replaced by terms based on the quasi-Fermi levels [93] given as

$$n = n_{int} \cdot e^{\frac{q\cdot(\psi-\phi_n)}{k_B\cdot T}} \tag{3.62}$$

and

$$p = n_{int} \cdot e^{\frac{q\cdot(\phi_p-\psi)}{k_B\cdot T}}, \tag{3.63}$$

where n_{int} is the intrinsic carrier concentration, ϕ_n and ϕ_p are the quasi-Fermi levels, and ψ is the electrostatic potential. Hence, Poisson's equation becomes

$$\nabla^2\psi = \frac{n_{int}\cdot q}{\epsilon_{Si}} \cdot \left(e^{\frac{q\cdot(\psi-\phi_n)}{k_B\cdot T}} - e^{\frac{q\cdot(\phi_p-\psi)}{k_B\cdot T}} + \frac{N_A^- - N_D^+}{n_{int}} \right). \tag{3.64}$$

At equilibrium the quasi-Fermi levels are equal to zero [96] and only the externally applied bias causes ψ to deviate from the intrinsic value. Using the thermal voltage given as

$\Phi_T = k_B \cdot T/q$ and replacing $\overline{\psi} = \psi/\Phi_T$ Equation (3.64) can be written as

$$\nabla^2\overline{\psi} = \frac{1}{L_{DI}^2} \cdot \left(e^{\overline{\psi}} - e^{-\overline{\psi}} + \overline{N}\right), \tag{3.65}$$

where L_{DI} is the intrinsic Debye length [86] given by

$$L_{DI} = \sqrt{\frac{\epsilon_{Si} \cdot k_B \cdot T}{q^2 \cdot n_{int}}}. \tag{3.66}$$

In Equation (3.65), $e^{\overline{\psi}}$ and $e^{-\overline{\psi}}$ are the scaled carrier densities $\overline{n} = n/n_{int}$ and $\overline{p} = p/n_{int}$. $\overline{N}$ is the scaled dopant concentration given as $(N_A^- - N_D^+)/n_{int}$.

Since the capabilities of the programming languages provided by circuit simulators are rather limited a FDM solver was chosen to be implemented for the feasibility study. The initial implementation was done in Matlab® to evaluate the basic concept and to debug the model more easily. Using the second-order central difference [97] for $\nabla\overline{\psi}$, Equation (3.65) can be written as

$$\frac{\partial^2\overline{\psi}}{\partial y^2} = \frac{\overline{\psi}_{i-1} - 2 \cdot \overline{\psi}_i + \overline{\psi}_{i+1}}{(\Delta y)^2} = \frac{1}{L_{DI}^2} \cdot \left(e^{\overline{\psi}_i} - e^{-\overline{\psi}_i} + \overline{N}\right). \tag{3.67}$$

Using *Gummel's Iteration Scheme* [98], the solution of ψ is calculated iteratively by

$$\overline{\psi}^{k+1} = \overline{\psi}^k + \overline{\delta\psi} \tag{3.68}$$

which yields

$$\frac{\overline{\psi}_{i-1} - 2 \cdot \overline{\psi}_i + \overline{\psi}_{i+1}}{(\Delta y)^2} + \frac{\overline{\delta\psi}_{i-1} - 2 \cdot \overline{\delta\psi}_i + \overline{\delta\psi}_{i+1}}{(\Delta y)^2} = \frac{1}{L_{DI}^2} \cdot \left(e^{\overline{\psi}_i} - e^{-\overline{\psi}_i} + \overline{N}\right). \tag{3.69}$$

For small changes in $\overline{\delta\psi}$ the equation can be linearized [99] by $e^{\pm\overline{\delta\psi}} \approx 1 \pm \overline{\delta\psi}$ and Equation 3.69 can be solved for $\overline{\delta\psi}$ which yields

$$\begin{aligned} &\overline{\delta\psi}_{i-1} - \overline{\delta\psi}_i \cdot \left(2 + \tfrac{(\Delta y)^2}{L_{DI}^2} \cdot \left(e^{\overline{\psi}_i} + e^{-\overline{\psi}_i}\right)\right) + \overline{\delta\psi}_{i+1} = \\ &-\overline{\psi}_{i-1} + 2 \cdot \overline{\psi}_i - \overline{\psi}_{i+1} + \tfrac{(\Delta y)^2}{L_{DI}^2} \cdot \left(e^{\overline{\psi}_i} - e^{-\overline{\psi}_i} + \overline{N}\right). \end{aligned} \tag{3.70}$$

In matrix form $\mathbf{A} \cdot \mathbf{x} = \mathbf{f}$ this equation can be rewritten as

$$\begin{pmatrix} a_1 & b_1 & 0 & \dots & 0 \\ c_1 & a_2 & b_2 & & \vdots \\ 0 & c_2 & \ddots & \ddots & 0 \\ \vdots & & \ddots & \ddots & b_{n-1} \\ 0 & \dots & 0 & c_{n-1} & a_n \end{pmatrix} \cdot \begin{pmatrix} \overline{\delta\psi}_1 \\ \overline{\delta\psi}_2 \\ \vdots \\ \overline{\delta\psi}_{n-1} \\ \overline{\delta\psi}_n \end{pmatrix} = \begin{pmatrix} f_1 \\ f_2 \\ \vdots \\ f_{n-1} \\ f_n \end{pmatrix}. \tag{3.71}$$

The parameters of matrix $\mathbf{A}$ are calculated by

$$\begin{aligned} a_i &= 2 + \frac{(\Delta y)^2}{L_{DI}^2} \cdot \left(e^{\overline{\psi}_i} + e^{-\overline{\psi}_i} \right), \\ b_i &= 1, \\ c_i &= 1, \end{aligned} \tag{3.72}$$

and the forcing function given by the $\mathbf{f}$ vector is determined by

$$f_i = -\overline{\psi}_{i-1} + 2 \cdot \overline{\psi}_i - \overline{\psi}_{i+1} + \frac{(\Delta y)^2}{L_{DI}^2} \cdot \left(e^{\overline{\psi}_i} - e^{-\overline{\psi}_i} + \overline{N} \right). \tag{3.73}$$

$\mathbf{A}$ in Equation (3.71) is a tridiagonal matrix and the Gaussian elimination method utilizing an LU decomposition [100] is used to numerically solve this equation for vector $\mathbf{x}$ (see Chapter 3.5.1.1).

As described by the authors of [96], the gradients of the carrier concentration ∇n and ∇p and the gradient of the electric potential $\nabla \psi$ are determined at the midpoint between the mesh grids. Derived from Equations (3.13) and (3.14) the electron current density becomes

$$\begin{aligned} J_{n,i+1/2} &= \frac{q \cdot \Phi_T \cdot D_{n,i+1/2}}{\Delta y} \left(n_{i+1} \mathbf{B}\left(\overline{\psi}_{i+1} - \overline{\psi}_i \right) - n_i \mathbf{B}\left(\overline{\psi}_i - \overline{\psi}_{i+1} \right) \right) \\ J_{n,i-1/2} &= \frac{q \cdot \Phi_T \cdot D_{n,i-1/2}}{\Delta y} \left(n_i \mathbf{B}\left(\overline{\psi}_i - \overline{\psi}_{i-1} \right) - n_{i-1} \mathbf{B}\left(\overline{\psi}_{i-1} - \overline{\psi}_i \right) \right) \end{aligned} \tag{3.74}$$

and the hole current density is given by

$$\begin{aligned} J_{p,i+1/2} &= \frac{q \cdot \Phi_T \cdot D_{p,i+1/2}}{\Delta y} \left(p_{i+1} \mathbf{B}\left(\overline{\psi}_{i+1} - \overline{\psi}_i \right) - p_i \mathbf{B}\left(\overline{\psi}_i - \overline{\psi}_{i+1} \right) \right) \\ J_{p,i-1/2} &= \frac{q \cdot \Phi_T \cdot D_{p,i-1/2}}{\Delta y} \left(p_i \mathbf{B}\left(\overline{\psi}_i - \overline{\psi}_{i-1} \right) - p_{i-1} \mathbf{B}\left(\overline{\psi}_{i-1} - \overline{\psi}_i \right) \right). \end{aligned} \tag{3.75}$$

The term $\mathbf{B}(x)$ refers to the *Bernoulli* function [96, 98] which is defined as

$$\mathbf{B}(x) = \frac{x}{e^x - 1}. \tag{3.76}$$

Equations (3.11) and (3.12) can be rewritten for the 1D FDM solver under steady state conditions [99] as

$$\begin{aligned} &\tfrac{\Phi_T \cdot D_{n,i+1/2}}{(\Delta y)^2} \cdot \mathbf{B}\left(\overline{\psi}_{i+1} - \overline{\psi}_i \right) \cdot n_{i+1} - \\ &\left(\tfrac{\Phi_T \cdot D_{n,i-1/2}}{(\Delta y)^2} \cdot \mathbf{B}\left(\overline{\psi}_i - \overline{\psi}_{i-1} \right) + \tfrac{\Phi_T \cdot D_{n,i+1/2}}{(\Delta y)^2} \cdot \mathbf{B}\left(\overline{\psi}_i - \overline{\psi}_{i+1} \right) \right) \cdot n_i + \\ &\tfrac{\Phi_T \cdot D_{n,i-1/2}}{(\Delta y)^2} \cdot \mathbf{B}\left(\overline{\psi}_{i-1} - \overline{\psi}_i \right) \cdot n_{i-1} \end{aligned} \quad = G_{n,i} - R_{n,i} \tag{3.77}$$

and

$$\begin{aligned} &\tfrac{\Phi_T \cdot D_{p,i+1/2}}{(\Delta y)^2} \cdot \mathbf{B}\left(\overline{\psi}_i - \overline{\psi}_{i+1} \right) \cdot p_{i+1} - \\ &\left(\tfrac{\Phi_T \cdot D_{p,i-1/2}}{(\Delta y)^2} \cdot \mathbf{B}\left(\overline{\psi}_{i-1} - \overline{\psi}_i \right) + \tfrac{\Phi_T \cdot D_{p,i+1/2}}{(\Delta y)^2} \cdot \mathbf{B}\left(\overline{\psi}_{i+1} - \overline{\psi}_i \right) \right) \cdot p_i + \\ &\tfrac{\Phi_T \cdot D_{p,i-1/2}}{(\Delta y)^2} \cdot \mathbf{B}\left(\overline{\psi}_i - \overline{\psi}_{i-1} \right) \cdot p_{i-1} \end{aligned} \quad = G_{p,i} - R_{p,i}. \tag{3.78}$$

These equations are scaled in the same manner as Poisson's Equation (3.69) and the boundary conditions are adapted accordingly. The carrier generation and recombination

terms $G_{n,i} - R_{n,i}$ and $G_{p,i} - R_{p,i}$ are replaced by the *Shockley-Read-Hall* term [92] shown in Equation (3.20).

The FDM solver consists of three parts based on the *Gummel Iteration Scheme* described by the authors of [98]. The solver initialization is the first part which

1. performs the domain setup and meshing,
2. defines the material parameters, and
3. calculates the initial guess of $\overline{\psi}$.

The setup of the simulation domain utilizes lookup tables (LuT) which define the dopant concentrations at certain points of the domain. During the definition of the doping profile the maximum value of the charge carrier concentration is determined and the *Debye length* given by Equation (3.53) is calculated. The distances between the mesh points of the simulation domain have to be smaller than L_{Debye} in order for the solver to work properly. For each mesh point the dopant concentration is interpolated by a *Piecewise Cubic Hermite Interpolating Polynomial* as described by [101]. The initial guess for $\overline{\psi}$ is based on the dopant concentration and is determined by $-log(\overline{N}_A^-)$ for the p–doped material and $log(\overline{N}_D^+)$ for the n–doped side of the pn junction.

The initialization step is followed by the equilibrium solver loop which iteratively solves Poisson's Equation (3.69) to calculate the electric potential $\overline{\psi}_0$ of the unbiased simulation domain. The equilibrium solver uses *Neumann* boundary condition on the p–doped side of the diode and *Dirichlet* boundary condition on the n–doped part of the diode. This setup of the boundary conditions was chosen because the p–doped substrate is defined as the reference potential of the test chips. Any external bias of the injector diode is applied at the n–doped epitaxial pocket. The matrix parameters (3.72) and forcing function (3.73) are calculated and an LU decomposition [100] determines $\overline{\psi}_0$.

The solution of $\overline{\psi}_0$ is the basis for the non-equilibrium solver and is used in the first iteration to determine the electron and hole densities of the simulation domain. The non-equilibrium solver continuously performs the following steps:

1. Solve Poisson's equation
   (a) Define electric potential boundary conditions
   (b) Calculate matrix parameters a, b, c and f
   (c) Do an LU decomposition
   (d) Determine convergence and evaluate break condition
2. Solve continuity equations
   (a) Define charge carrier boundary conditions
   (b) Calculate field dependent parameters e.g. μ_n and μ_p
   (c) Calculate matrix parameters a_n, b_n, c_n and f_n

(d) Calculate matrix parameters a_p, b_p, c_p and f_p

(e) Do an LU decomposition for electrons

(f) Do an LU decomposition for holes

(g) Determine convergence and evaluate break condition

For each iteration of the Poisson's equation solver and the continuity equation solver the convergence rate is determined and the break condition of the loop is evaluated. Only when all three LU decompositions reach convergence the next set of boundary conditions is determined and applied to the simulation domain.

3.5.1.1 LU Decomposition

$\mathbf{A}$ of Equation (3.71) is an n x n matrix which is decomposed into

$$\mathbf{A} = \mathbf{L} \cdot \mathbf{U} \tag{3.79}$$

where $\mathbf{L}$ is a lower triangular matrix and $\mathbf{U}$ is an upper triangular matrix [102]. The elements l_{ij} of $\mathbf{L}$ satisfy $l_{ij} = 0$ $(\forall\ i < j)$ and respectively the elements u_{ij} of $\mathbf{U}$ satisfy $u_{ij} = 0$ $(\forall\ i > j)$. By using forward substitution the system

$$\mathbf{L} \cdot y = f \tag{3.80}$$

is solved for y and

$$\mathbf{U} \cdot x = y \tag{3.81}$$

is solved for x using backward substitution. The source code shown in Appendix D.1 is a fast solver for tridiagonal matrices where a contains the elements of the main diagonal, b is the upper diagonal, and c is the element vector of the lower diagonal as shown in Equation (3.71).

3.5.1.2 Model Calibration

A key parameter of the drift-diffusion model is the charge carrier mobility. The mobility properties of silicon which are implemented in the FDM solver are based on the results obtained by the authors of [33, 103] and are illustrated in Figure 3.9. The mobility μ is dependent on the doping concentration and varies significantly between the n–doped and the p–doped material. During the initialization step of the solver the mobility properties are calculated for the entire simulation domain. Additionally, at every iteration of the equilibrium and non-equilibrium solver the electric field $\vec{E}$ is calculated and the mobility is updated in dependence of $\vec{E}$ as stated by [34].

The second parameter which significantly influences the drift-diffusion model is the lifetime of the charge carriers which is utilized as a part of the *Shockley-Read-Hall* term [92] given by Equation (3.20). The values of τ_n and τ_p are also governed by the dopant concentration and are based on the work of the authors of [33]. An overview of the mobility and lifetime parameters used by the 1D FDM is shown in Figure 3.9.

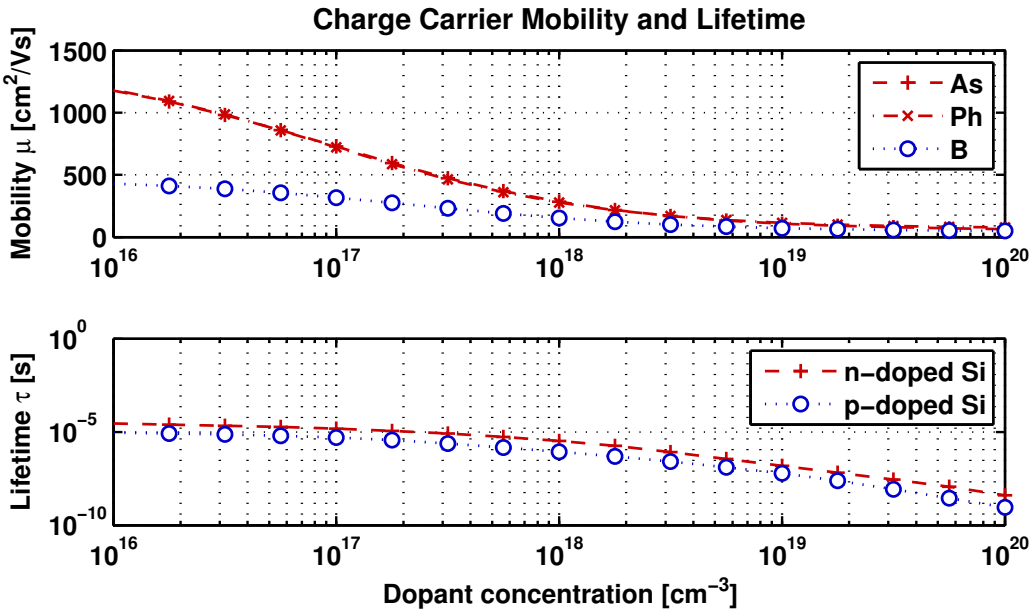


Figure 3.9: Material properties for the 1D FDM solver [33, 103]

3.5.1.3 1D Diode Model Evaluation

The setup of the injector model iteratively ramps up the externally applied electric potential ψ_S as given by the boundary conditions stated in Equation (3.55). In order for the FDM solver to converge the increment of the external bias is constrained by $\Delta\psi_S \ll \Phi_T$. The graph on the left hand side of Figure 3.10 shows the result of the injector diode after calibrating the 1D FDM solver as discussed earlier. The relative error between the measurement results and the diode model reaches ≈ 75 %. Additionally, the simulation time of the model in Matlab® was also quite high which is caused by the necessity to ramp up the external bias in iterations of $\ll \Phi_T$.

The boundary conditions of the model at the susceptible part of the coupling path is governed by changing the minority carrier density n_s as stated by Equation 3.58. The convergence requirement is $\Delta n_s \ll n_0$ where n_0 is the minority carrier density of the equilibrium state. The results shown on the right hand side of Figure 3.10 indicate an almost linear behavior between the minority carrier density and the current density of the sensor. However, also for this part of the model the simulation time took several minutes and under consideration of the number of susceptible nodes the performance is insufficient for a full chip analysis. In an earlier concept the 1D FDM model was intended to be implemented in Verilog-A and utilized for circuit simulation. This decision was discarded due to the calculation effort this model imposes on the circuit simulator. Hence, the charge carrier densities at the injector's and sensor's boundary are obtained from the simulation results of a commercial TCAD solver and are used in an empirical model.

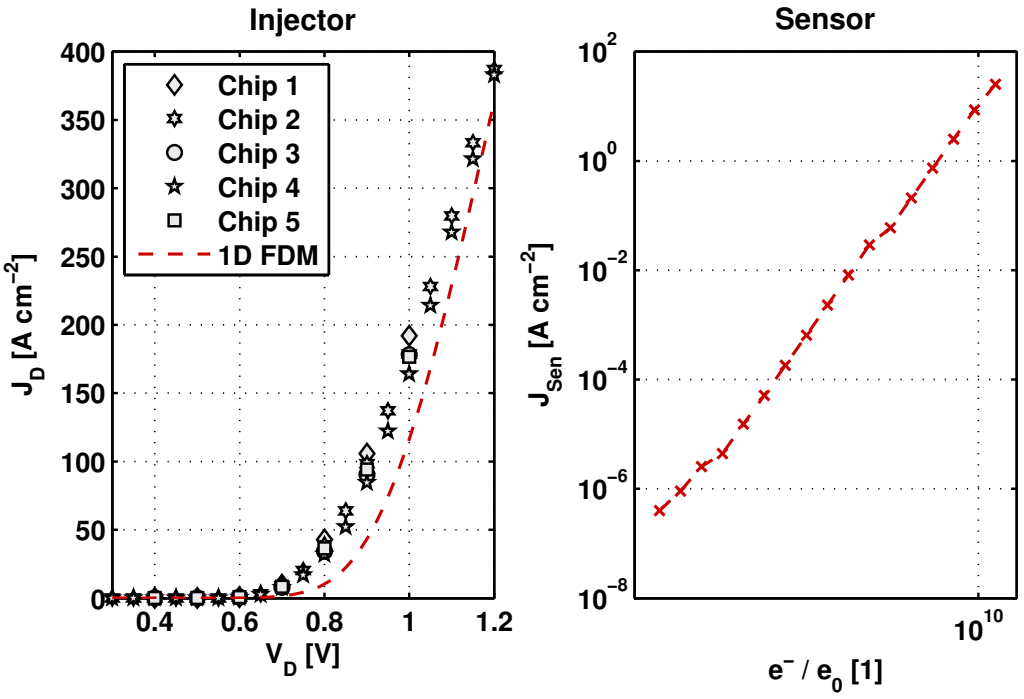


Figure 3.10: 1D FDM model results

3.5.2 2D FEM Substrate Model

The emitter and collector part of the coupling path are attached to the substrate at well defined interfaces. Unfortunately, the substrate cannot be reduced to a single dimensional simulation domain but needs to be at least two dimensional because the extension into the substrate influences the coupling behavior. On the other hand, the primary requirement for a 2D cross section to be valid is that there are no dependencies to structures within the third, unobservable dimension. This imposes the limitation that any structure which does not directly lie on the cross sectional plane is disregarded in the simulation. Another limitation of this approach is that the coupling effect is unidirectional. This means the emitter influences the collector(s) but not vice versa. However, the interaction between multiple sensors can be covered as long as the boundary conditions at the collectors can be clearly established. Effects such as the influence of the connections to the epitaxial well as shown in Figure 3.7 can be observed with the proper setup but the increase in substrate resistance at the emitter will not be covered.

The 2D FEM solver uses the Matlab® *PDE Toolbox*™ [101] and Equations (3.11) to (3.15) have to be adapted accordingly. Elliptic equations are expected by the *PDE Toolbox*™ to be provided in the form of

$$-\nabla \cdot (c \cdot \nabla u) + a \cdot u = f \tag{3.82}$$

and Poisson's Equation (3.15) in its scaled form is given by

$$-\nabla \cdot \left(L_{DI}^2 \cdot \nabla \overline{\Psi}\right) = e^{\overline{\Psi}} - e^{-\overline{\Psi}} + \overline{N}. \tag{3.83}$$

The continuity equations are parabolic equations and need to be provided as

$$d \cdot \frac{\partial u}{\partial t} - \nabla \cdot (c \cdot \nabla u) + a \cdot u = f. \tag{3.84}$$

However, when the current density equations (3.13) and (3.14) are substituted into the continuity equations (3.11) and (3.12) the divergence term $\nabla \cdot (c \cdot \nabla u)$ contains two terms which are dependent on u. The drift part of the model was moved to the right hand side of the equations and is determined as a part of coefficient f. Since the generation and recombination rates are already dependent on u (which means the charge carriers in general) the coefficient $f(u)$ has to be calculated for each iteration of the solver. The scaled equations for the 2D FEM are

$$\begin{aligned} \frac{\partial \overline{n}}{\partial t} - \nabla \cdot (D_n \cdot \nabla \overline{n}) &= \overline{G}_n - \overline{R}_n + \nabla \cdot \left(\mu_n \cdot \overline{n} \cdot \vec{E} \right) \\ \frac{\partial \overline{p}}{\partial t} - \nabla \cdot (D_p \cdot \nabla \overline{p}) &= \overline{G}_p - \overline{R}_p + \nabla \cdot \left(\mu_p \cdot \overline{p} \cdot \vec{E} \right). \end{aligned} \tag{3.85}$$

3.5.2.1 Solver Setup and Calibration

The 2D FEM solver is set up similarly as the 1D FDM solver and also utilizes the *Gummel Iteration Scheme* [98] to numerically solve the drift-diffusion equations. The simulation domain is primarily governed by its boundaries which are defined by the emitter, the collectors, the substrate contacts, and the interfaces to the chip's package. The mesh of the domain is generated by an independent script prior to the main simulation run. This mesh generator calls the function `pdemesh` which creates a triangular mesh within a confined area. Additionally, some vectors are initialized which contain the material parameters and solver coefficients. Afterwards, the 2D FEM solver is executed and performs the following simulation steps:

1. Read mesh and define the simulation setup
2. Initialize boundary conditions
3. Solve
   (a) Solve Poisson's equation
      i. Call `pdenonlin`
      ii. Calculate $\vec{E}$ and update dependent parameters
      iii. Calculate $\nabla \cdot \left(\mu_n \cdot \overline{n} \cdot \vec{E} \right)$ and $\nabla \cdot \left(\mu_p \cdot \overline{p} \cdot \vec{E} \right)$
   (b) Solve continuity equations
      i. Call `parabolic` for the electrons
      ii. Call `parabolic` for the holes
      iii. Calculate J_n and J_p
   (c) Store every n-th iteration

The 2D FEM solver reads the previously generated mesh information and the definition of the simulation setup. The simulation setup provides the details about the external

stimuli and needs to declare what kind of boundary conditions apply to each individual boundary segment. The different types of boundary conditions can be found in Chapter 3.4. During the first run of the solver the boundary conditions are set to initial values which only reflect the carrier densities caused by the dopant concentrations without any external bias. The only voltage which is defined at this point is the reference potential for the upcoming simulation steps.

The main solver loop calls the tool box functions *pdenonlin* and `parabolic` to numerically solve the partial differential equations on the defined mesh. Both functions in turn call user defined sub-functions which return the simulation coefficients and apply the boundary conditions at each simulation step. The coefficients can either be given as scalars in which case they apply to the entire domain or they can be given as vectors in which case every point in the mesh is applied its individual value. This provides the opportunity to apply doping concentration dependent material parameters. Additionally, also solution dependent parameters like the recombination rate can be calculated and immediately applied at the next iteration step of the solver. However, some of these updates to the coefficients interfered with the internal algorithms and dampening functions had to be introduced.

The calibration of the solver used the same material parameters as the 1D FDM solver which are discussed in Chapter 3.5.1.2. Even prior to the simulation it was fairly clear that the material parameters which are used for the epitaxial regions may not reflect the physical behavior inside the substrate. This hypothesis is based on the different parameters of the crystalline silicon material. The substrate is a very pure silicon crystal with a very low defect density. In contrast the epitaxial layer is grown on top of a highly doped buried layer. This layer is subjected to ion implantation which causes significant damage to the crystal structure. Additionally, the deep trench is etched into the epitaxial layer and its sidewalls are covered with SiO_2 which introduces an interface between two different materials. Finally, the n–doped sinker structure is implanted which reaches down to the buried layer and the defect density becomes even higher. Regardless of the quality of the calibration the overall concept can still be validated and even provided fair results.

3.5.2.2 2D Model Evaluation

The simulation result in Figure 3.11 shows the normalized electron density through a partial cross section of the substrate. The depth coordinate is the distance to the epi-to-substrate *pn*-junction located at the top of the substrate and the width is the cut line running through the emitter and sensor nodes. At the center of the structure is the emitter boundary which injects carriers into the substrate and the carrier density declines over the distance from the emitter. At each side of the emitter there are boundaries in collector configuration which extract electrons from the substrate. The carrier density gradient is used to determine the current density at each individual collector node and the results are shown in Table 3.1.

The 2D FEM relied on the carrier density information obtained by the 1D FDM injector diode simulation and determined the spatial propagation of the charge carriers through a cross section of the substrate. At the sensor side of the model the spatial

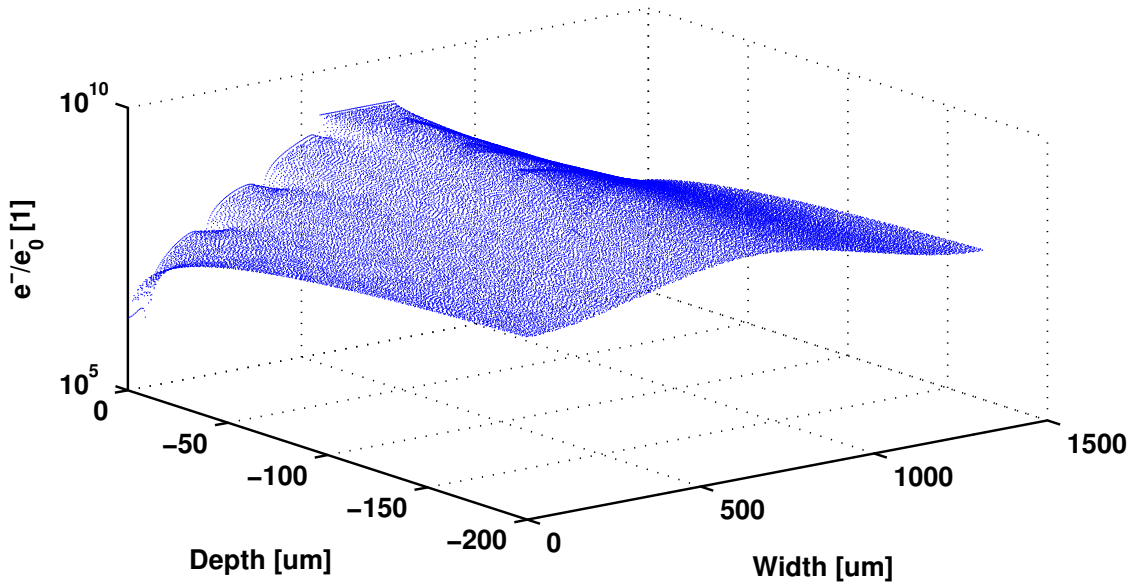


Figure 3.11: 2D FEM electron density results

gradient of the electron concentration was used to determine the parasitic current. While the results given in Table 3.1 are satisfactory at close range the relative error δx increases significantly with increasing distance between the emitter and the collector node.

Table 3.1: Comparison between measurement and simulation [104]

	$I_{Sen}[\mu A]$		
Distance $[\mu m]$	Simulation	Measurement	$\delta x[\%]$
20	108.13	99.39	8.8
230	2.25	1.35	66.6
400	0.16	0.04	350.0

Initially, the concept was to directly derive the substrate model provided by the carrier density distributions of the 2D FEM. The effort to implement additional features to the 2D FEM solver in order to increase its accuracy outweighs the benefit of processing all the simulation data in Matlab®. Hence, a commercial TCAD solver was investigated in more detail. Besides the expected improvement in accuracy it had to be evaluated whether the necessary data for the substrate model can be obtained from the results.

3.6 TCAD Simulation Setup

Even with the switch to a commercial TCAD solver the basic concept of the circuit simulation flow remains the same. This means in the circuit simulation model the coupling

path between the injector and the sensors is still split into three separate parts. However, the TCAD solver *Sentaurus™ Device* of *Synopsys®* provided different capabilities than the combination of the 1D FDM and the 2D FEM solver which were developed during the course of this thesis. The mixed modeling approach shown in Figure 3.8 was changed into a setup which contains the entire cross section of the design. The simulation setup of the commercial TCAD solver is illustrated in Figure 3.12. It can contain several emitter regions Ω_E and collector regions Ω_C which are connected by their respective boundaries on top of the silicon surface. The surface boundaries are metal-to-silicon interfaces and are labeled as Γ_{Cm} and Γ_{Em}. The electrical connection to the substrate is realized by the poly-filled deep trench which is connected by the boundaries labeled as Γ_{Sm}. Also these boundaries are formed by metal-to-silicon interfaces. The last two boundaries are formed by the sidewalls Γ_{SW} and the backside of the wafer Γ_B. The boundary Γ_{surf} does not physically exist but it denotes the position where the data regarding the carrier densities and the electric potential are collected. These data provide the basis of the circuit simulation model.

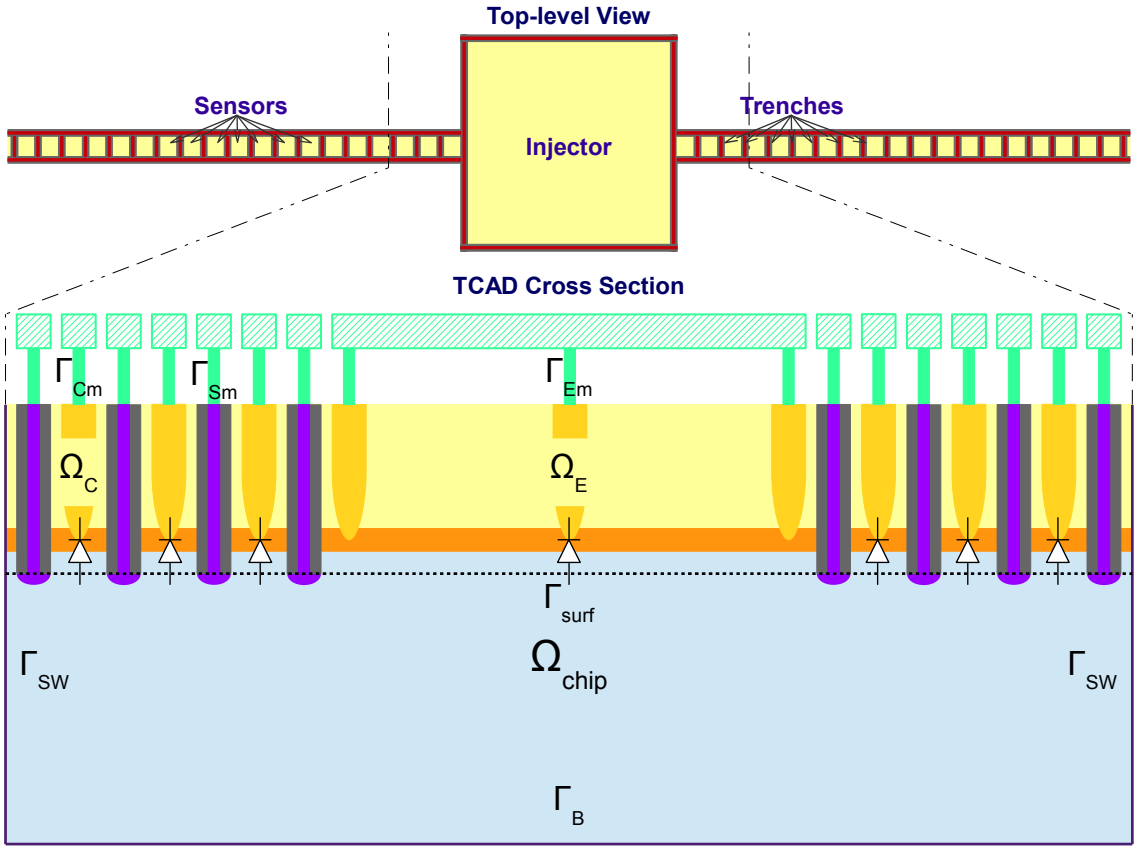


Figure 3.12: Cross section of the 2D TCAD simulation setup based on the test chip

The cross section through the entire length of the test chip (see Chapter 4.2 for details) is several millimeters long and a few hundred micrometers high. The smallest structure on the test chip is the poly-Si inside the trench which is less than a micrometer thick.

Hence, some simplifications had to be made to keep the simulation mesh at a reasonable size. The width and depth of the deep trench as well as the SiO_2 sidewalls are structured properly. The transition between the highly doped poly-Si and the lowly doped p–type substrate requires a substantial amount of mesh nodes to sufficiently capture the carrier concentration gradient. Additionally, the doping profile of the epitaxial layer sets the requirements at the mesh density of the emitter and collector region. The mesh density of the substrate region needs to be higher close to the pn junction between the epitaxial pockets and the substrate. The reason is that during an injection event the carrier concentration can exceed the equilibrium density significantly. The deeper into the substrate the less dense is the simulation mesh. The entire mesh consists about $150,000$ points containing 15 collector nodes at each side of a single emitter node. This setup covers a cross sectional area of $\approx 0.3\ mm^2$.

The input file of the TCAD solver contains different sections. In the first part all relevant geometrical parameters and material constants are stored in variables. This enables fast changes to the geometry of the simulation domain and it simplifies parameter modifications significantly. This section is followed by the definition of the simulation domain and the creation of the mesh. Every x and y coordinate that is relevant to the simulation structure is specifically defined and the source code in Listing 3.1 gives an example on how the deep trench is modeled.

The variables `dtioxsw` and `dtipw` contain the width of the SiO_2 sidewall and poly-Si inside the trench. The variables `msdtiox` and `msdtipo` define the number of mesh points to be generated between `x.min` and `x.max` [105]. The x axis definition of the trench is repeated several times starting at a different position given by the sensor width `sendist` and a multiplier. Similarly, the y axis is defined by the depth of the epitaxial pocket `npocd`, the depth of the trench's sidewalls `dtid` and the extension of the poly-Si inside the trench `dtipd` reaching into the substrate. The number of mesh points for each of the segments is defined by `msnpocd`, `msdtid`, and `msdtipd`. The mesh section is followed by the definition of the different regions of the simulation domain shown in Listing 3.2.

The entire cross sectional silicon area is defined by four regions which are named `npoc`, `bulkt`, `bulkm`, and `bulkb`. `npoc` defines the area of the n–doped epitaxial pocket including the buried layer as illustrated in Figure 3.12. The doping profile is assigned later on by the `PROFILE` statement [105]. The bulk area is split into three separate parts. The region `bulkt` physically belongs to the p–doped substrate but is subjected to out-diffusion of donor dopants of the highly n–doped buried layer. The regions `bulkm` and `bulkb` cover the remaining area of the substrate down to the backside of the chip. The split between these regions is primarily used to influence the re-meshing algorithm of the solver and reduce the number of grid points in the lower part of the substrate.

The deep trenches are used to separate the epitaxial pockets from each other and need to be defined as a combination of the `oxide` and `polysili REGION` statements. This is shown in Listing 3.2. The poly-Si has to slightly extend into the substrate region to ensure that both regions become electrically connected.

The `ELECTRODE` and `CONTACT` statements are used to define the electrical interfaces to the structure and to define the contact resistances associated with each of the electrical connections. In addition, the silicon region is extended by an insulator region (see Listing

3.3) which enables the utilization of surface recombination which occurs at the saw street of the wafer and the backside of the die. Without this extension the definition of the surface recombination parameter remained dormant.

Listing 3.1: Deep trench mesh definition

```
$ ===== x-axis =====
x.mesh x.min=@sendist*1
+      x.max=@sendist*1+@dtioxsw*1
+         h1=@dtioxsw/@msdtiox
x.mesh x.min=@sendist*1+@dtioxsw*1
+      x.max=@sendist*1+@dtioxsw*1+@dtipw
+         h1=@dtipw/@msdtipo
x.mesh x.min=@sendist*1+@dtioxsw*1+@dtipw
+      x.max=@sendist*1+@dtioxsw*2+@dtipw
+         h1=@dtioxsw/@msdtiox
$ ===== y-axis =====
y.mesh y.min=0.0     y.max=@npocd  h1=@npocd/@msnpocd
y.mesh y.min=@npocd  y.max=@dtid   h1=(@dtid-@npocd)/@msdtid
y.mesh y.min=@dtid   y.max=@dtipd  h1=(@dtipd-@dtid)/@msdtipd
```

Listing 3.2: Region overview

```
region name=npoc  silicon  y.min=0.0     y.max=@npocd
+                          x.min=0.0     x.max=@xeodie
region name=bulkt silicon  y.min=@npocd  y.max=@dtid
+                          x.min=0.0     x.max=@xeodie
region name=bulkm silicon  y.min=@dtid   y.max=@dtidm
+                          x.min=0.0     x.max=@xeodie
region name=bulkb silicon  y.min=@dtidm  y.max=@died
+                          x.min=0.0     x.max=@xeodie
region name=riw1  oxide    y.min=0.0     y.max=@dtid
+                          x.min=@sd1b   x.max=@sd1e
region name=rpow1 polysili y.min=0.0     y.max=@dtipd
+                          x.min=@sd1pb  x.max=@sd1pe
```

Listing 3.3: Insulator defining the chip's surrounding area

```
region name=iso   insulato y.min=0.0  y.max=@died+2.0
+                          x.min=-2.0 x.max=@xeodie+2.0
$ Silicon sidewall and bottom
interface x.min=-0.1         x.max=0.1
+         y.min=-0.1         y.max=@died+0.1
+         s.n=@srvsisw       s.p=@srvsisw
interface x.min=@xeodie-0.1  x.max=@xeodie+0.1
+         y.min=-0.1         y.max=@died+0.1
+         s.n=@srvsisw       s.p=@srvsisw
interface x.min=-0.1         x.max=@xeodie+0.1
+         y.min=@died-0.1    y.max=@died+0.1
+         s.n=@srvsi         s.p=@srvsi
```

3.6.1 Calibration of the TCAD Setup

After the geometry specification and mesh generation of the simulation domain the `PROFILE` statements provide the doping information to the individual regions as shown in Listing 3.4. The three bulk regions are all uniformly p–doped and represent the chip's substrate. The dopant concentration of the epitaxial layer is given by a single statement concerning the entire `npoc` region. The numerical values are provided by an ASCII file containing three columns which specify the donor and acceptor concentration at a certain depth. The last row shows an example for a single poly-Si region of the deep trench. It creates a homogeneous dopant concentration `dtipdop` down to the extent of `dtipd`. Since the bulk and the poly-Si in the trench are both p–doped an electrical connection is formed between those regions. This statement has to be repeated for every deep–trench of the simulation domain.

Listing 3.4: Dopant concentration specification

```
$ ===== Doping Profile Specification =====
profile region=bulkt  p-type  n.peak=@subdop   uniform
+ out.file=tc_2d_base094.ps
profile region=bulkm  p-type  n.peak=@subdop   uniform
profile region=bulkb  p-type  n.peak=@subdop   uniform
profile region=npoc   n-type  n.peak=@npocdop
+ in.file=tc_2d_base094.dop  1d.asciis y.column=1 n.column=2 p.column=3
profile region=rpow1  p-type  n.peak=@dtipdop  y.char=@dtipd
```

Based on these parameters the first simulation run was performed and the results are illustrated in Figure 3.13 by the curves labeled as *default*. They show the primary characteristics of the coupling effect which are the I-V curve of the injector diode and the distance characteristic between the injector and the sensors. Considering the default case the diode characteristic is off by a factor of ≈ 2. The distance characteristic declines with one order of magnitude per width of eight sensors while the default TCAD setup declines six orders of magnitude. Both characteristics deviate from the measurements and additional calibration steps were necessary to improve the simulation.

Under consideration of the 1D analyses discussed in Chapter 3.3.4, the charge carriers' lifetimes and their mobility are the parameters with the greatest influence on the coupling effect. This led to the first set of adaptations to the TCAD setup shown in Listing 3.5. The *Philips Unified Mobility Model* described by the authors of [106, 107] was selected based on its capability to model bipolar transistors. As stated in [105], this mobility model works best in combination with bandgap narrowing `bgn` and the suggested values shown at the `MATERIAL` statements for `silicon` and `polysili` in Listing 3.5.

The selected recombination models are the *Auger* and the dopant concentration dependent *Shockley-Read-Hall* model. However, simulations based on the default value of $\tau_n \approx 100\ ns$ [108] did not show much improvement in the accuracy of the simulation. The values provided by the authors of [108] are for diffused layers and are therefore not feasible for simulations of pure silicon substrates. The highest value for the minority carrier lifetime $\tau_n \approx 1\ ms$ is given by the authors of [109] for ultrapure silicon. This value on the other hand proved to be too large. Hence, the distance characteristic became very shallow which overestimated the effect at large distances between the injector and the

sensor nodes. Better results were obtained based on the value $\tau_n \approx 30\ \mu s$ provided by [110, 33] but the overall accuracy was still not good enough. With such a large range for a key parameter of the simulation it was necessary to determine the value by measurements on the test chip.

Listing 3.5: Model selection and lifetime calibration

```
$ ===== Simulation Setup =====
models   phumob  consrh  bgn  auger
material silicon      v0.bgn=6.92e-03  n0.bgn=1.3e17  con.bgn=0.5
+ taun0=@Si0taun   taup0=@Si0taup
material polysili     v0.bgn=6.92e-03  n0.bgn=1.3e17  con.bgn=0.5
+ taun0=@PoSitaun  taup0=@PoSitaup
material region=bulkm
+ taun0=@Sitaun    taup0=@Sitaup
material region=bulkb
+ taun0=@Sitaun    taup0=@Sitaup
```

Under the following conditions,

$$\begin{aligned} \frac{\partial n}{\partial t} &= 0, \\ \vec{E} &= 0, \\ G_n &= 0, \end{aligned} \tag{3.86}$$

and using the simplest expression for the recombination

$$R_n = \frac{n - n_0}{\tau_n} \tag{3.87}$$

the spatial decay of a localized density perturbation caused by minority carrier injection can be determined from

$$D_n \frac{\mathrm{d}^2 \Delta n}{\mathrm{d}x^2} - \frac{\Delta n}{\tau_n} = 0 \tag{3.88}$$

as

$$\Delta_n(x) = \Delta n(0) \cdot e^{\left(-\frac{x}{L_n}\right)} \tag{3.89}$$

which leads to an electron diffusion length of

$$L_n = \sqrt{D_n \cdot \tau_n}. \tag{3.90}$$

The conditions stated in Equation (3.86) can be satisfied during the measurement of the test chip by injecting a constant current over a long period of time to ensure all time related effects have reached steady-state conditions. Additionally, the injected current has to be small enough to prevent localized shifts in the electric potential in the substrate. This can also be achieved by performing the measurements at larger distances from the injector where the electric field is small enough to satisfy $\vec{E} \approx 0$.

An electron diffusion length of $L_n \approx 45\ \mu m$ was obtained by measurement which leads to a minority carrier lifetime of $\tau_n \approx 4\ \mu s$ [33]. However, this value does not correlate

to the lifetimes provided by the authors of [33, 109, 110] for the dopant concentration of the silicon substrate wafer. Hence, additional effects [95] can degrade the minority carrier lifetime in boron–doped Cz silicon which maybe the reason for the deviation. Several independent studies were performed by an external partner within the *eRamp project* of the *ENIAC Joint Undertaking* funded by the EU. Different methods were used to determine the lifetime of the minority carriers which were based on the I-V characteristic of the injector diode, C-V measurements of the diffusion admittance, analysis of the reverse recovery time and a deep level transient fourier spectroscopy (DLTFS) [111]. These analyses were performed on an unprocessed sample of the substrate as well as on the test chip and the results are reported in [112]. The lifetimes of the charge carriers got confirmed and the TCAD simulation results of this calibration step are shown in Figure 3.13 labeled as *carrier lifetimes*.

Listing 3.6: Interface and trap specifications

```
$ ===== Simulation Setup =====
material insulato   permitti=1.0
$ Silicon sidewall and bottom
interface x.min=-0.1        x.max=0.1
+         y.min=-0.1        y.max=@died+0.1
+         s.n=@srvsisw      s.p=@srvsisw
interface x.min=@xeodie-0.1 x.max=@xeodie+0.1
+         y.min=-0.1        y.max=@died+0.1
+         s.n=@srvsisw      s.p=@srvsisw
interface x.min=-0.1        x.max=@xeodie+0.1
+         y.min=@died-0.1   y.max=@died+0.1
+         s.n=@srvsi        s.p=@srvsi
$interface material=(silicon,insulato) s.n=@srvsi  s.p=@srvsi

$ Silicon-oxide interfaces
interface material=(silicon,oxide) s.n=@srvsiox  s.p=@srvsiox

$ Electron Traps (V-a, Pt-a/Pd-a, Pt-a, Pd-4)
traps    e1=0.17  n.total="5.5e13"   taun=@Sitaun
traps    e2=0.23  n.total="9.5e13"   taun=@Sitaun
traps    e3=0.27  n.total="4.1e13"   taun=@Sitaun
traps    e4=0.25  n.total="3.7e13"   taun=@Sitaun
$ Hole Traps (Pd-4, Mn-d, V-d)
traps    e5=0.25  n.total="-3.7e13"  taup=@Sitaup
traps    e6=0.43  n.total="-2.9e13"  taup=@Sitaup
traps    e7=0.46  n.total="-2.9e13"  taup=@Sitaup
```

This TCAD setup still shows deviations of the measurements close to the injector and at large distances from the injector. This suggests that additional recombination effects occur which have not yet been accounted for. The interface of the substrate and the oxidized walls of the trench were identified as a possible source of the deviation. The surface recombination velocities of silicon to SiO_2 are given by the authors of [94] and are included in the setup shown in Listing 3.6. Additionally, the *insulato* material has to be specified to enable surface recombination velocities at the boundaries of the substrate and the surrounding air inside the ceramic package. The electron and hole traps were again provided by studies performed by an external partner [112] and were added to the TCAD

setup. The results are shown in Figure 3.13 labeled as *Interfaces, Traps*. The sidewalls and backside surface recombination velocities improved the TCAD simulation at larger distances from the injector. Nevertheless, the impact of the interface between the trench and the substrate was not the cause of the deviation in close proximity to the injector.

After extensive review of the simulation setup one simplification proved to be the reason for the deviation close to the injector. Initially, the *npoc* doping specification was reduced to a minimum of four depth–to–dopant concentration pairs in order to reduce the number of grid points at the top of the chip. This turned out to be insufficient and the slope of the dopant concentration was improved by adding additional points to the dopant input file. In order to represent these values inside the simulation domain some grid points in the deep substrate were removed and shifted to the epitaxial layer region. This final calibration step is shown by the curve labeled *Doping profiles* in Figure 3.13.

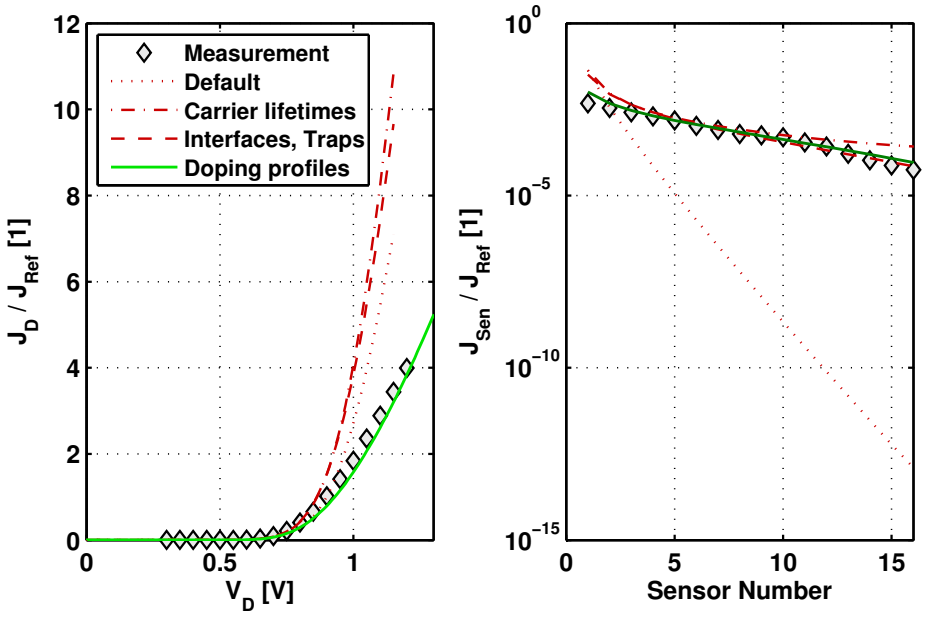


Figure 3.13: Calibration results for the commercial TCAD solver

The complexity of the TCAD calibration is caused by the interdependency of two very different characteristics. The I-V characteristic focuses on the behavior of a *pn* junction with a very unusual anode geometry and the distance characteristic determines the spatial propagation properties of charge carriers inside a large silicon area. The biggest influence on the distance characteristic was the calibration step of the minority carrier lifetimes. However, this caused the I-V characteristic to deviate even more from the measurements than the *default* setup. The specification of the interfaces' surface recombinations and the carrier traps improved the results but the I-V characteristic still showed a mismatch by a factor of at least three. The update of the dopant profile increased the series resistance inside the epitaxial layer and also decreased the minority carrier concentration during an injection event. Finally, an accurate TCAD setup was obtained that provides the basis for the circuit simulation model.

3.7 Circuit Simulation Model

The circuit simulation model representing the parasitic coupling effect connects the injector and the sensor at dedicated terminals. Which terminal of the device a connection is established to depends on the technological configuration of the device. The n and p–doped layers determine the function of the device and their electrical interaction with the n–doped epitaxial layer defines which device terminals are susceptible to disturbances via the substrate. Figure 3.14 illustrates the differences between the connections to the injector and sensor terminals.

In this example, the injector is an n–channel power DMOS M_{DMOS} and the voltage at the drain terminal D becomes negative with respect to the ground potential causing the current $I_{Reverse}$ to flow through the device. When the power DMOS is turned off, the current $I_{Reverse}$ is split into two parts. One part flows through the bulk diode D_B which is formed by the n–type drain region and the bulk of the DMOS. The second part flows through the substrate diode D_{sub} which is formed by the drain region and the substrate as shown in Figure 2.6. In modern product development kits (PDKs), the model of any circuit device also contains all its parasitic elements which means the parasitic diodes D_B and D_{sub} are an integral part of the M_{DMOS} model. Detailed knowledge about the content of the models in the PDK is mandatory because it has significant impact on the applicability of the parasitic device model itself. For example, if the model of the substrate diode D_{sub} is not well calibrated regarding DC injection effects, the entire coupling path can deviate from reality. An alternative solution is to connect the parasitic model directly to the drain terminal D and emulate the behavior of D_{sub} internally. This solution is also used in cases when the terminal *sub* of M_{DMOS} is not directly accessible during circuit simulation. Figure 3.14 illustrates the case when the sensing terminal *inj* of device X_{AM} is directly connected to the *sub* terminal of M_{DMOS} and measures the substrate current I_{Inj}.

The sensor Q_{npn} shown in Figure 3.14 is a bipolar transistor and its cross section is illustrated in Figure 2.1. The n–doped epitaxial layer is the collector terminal C of the device and therefore susceptible to coupling effects via the substrate. Although this device also has a terminal *sub* representing the substrate, the parasitic device model cannot use it as a connection. The reason for this is the setup of the transistor's model. The *sub* terminal is connected to the anodes of two diodes, D_{sub} and the base–collector diode of Q_{pnp}. When the current I_{Sen} is pulled out of this node during the simulation, the voltage at terminal *sub* will decrease until the breakdown voltage of one of the diodes is reached. This, however, is not what is happening in reality. The parasitic current I_{Sen} increases the leakage current of the diode D_{sub} and the electrons traverse directly into the collector node. Hence, connecting the output terminal *sen* of the parasitic device model directly to the susceptible node is the reasonable choice.

The parasitic device model is split into three separate modules illustrated in Figure 3.14 which represent the coupling path between the injector and the sensor. This setup is primarily based on the three major components that contribute to this effect which are the injector diode, the silicon substrate, and the sensor diode. The injector and sensor model translate current density into charge carrier densities and vice versa while the substrate

model handles the spatial propagation of the charge carriers. The model of the coupling path is unidirectional which means the flow of information moves from the input to the output of each part without any feedback.

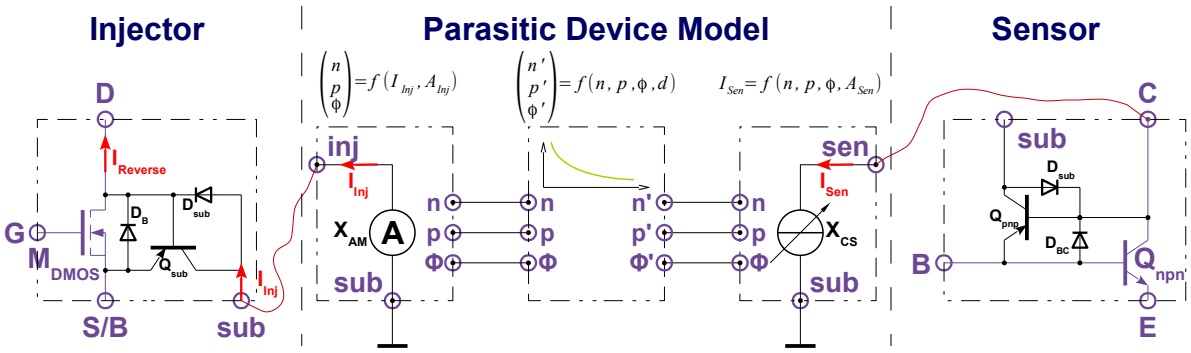


Figure 3.14: Concept of the circuit simulation model

Originally, the parasitic device model was based on an LuT approach that contained dedicated values describing the coupling factor between the injector and the sensor as discussed in [104]. This concept of the parasitic device model had to be discontinued because of convergence issues with the circuit simulation software. The model was based on a piecewise linear interpolation between the points specified in the LuT. This interpolation caused discontinuities in higher-order derivatives causing reduced performance in some of the simulation software. This issue was overcome by changing from a pre-calculated macro model approach to an empirical approach which utilizes curve fitting functions for the carrier densities as well as the electric potential.

3.7.1 The Injector Model

In its simplest version the Verilog-AMS model of the injector diode contains an ideal ammeter X_{AM} in the branch between the *inj* and the *sub* terminal as illustrated in Figure 3.15. It measures the substrate current I_{Inj} of the injector M_{DMOS} directly and calculates the current density by solving

$$J_{Inj} = \frac{I_{Inj}}{A_{Inj}} \tag{3.91}$$

where A_{Inj} is the area of the injector's epitaxial pocket. The parameter A_{Inj} needs to be measured in the layout of the chip by means of an extraction process that is explained in Chapter 3.8. Alternatively, when the substrate node is inaccessible the current density J_{Inj} is determined by sensing the voltage V_{Inj} applied at the drain terminal D of M_{DMOS}. In this version of the model the branch between the *inj* and the *sub* contains an ideal voltmeter X_{VM}.

The value measured by the voltmeter X_{VM} is used in a curve fitting function that

models the behavior of the diode D_{sub}. The equation is

$$\log\left(J_{Inj}(V_{Inj}, T)\right) = \frac{p_1 \cdot V_{Inj}^3 + p_2 \cdot V_{Inj}^2 + p_3 \cdot V_{Inj} + p_4}{V_{Inj}^3 + q_1 \cdot V_{Inj}^2 + q_2 \cdot V_{Inj} + q_3} \tag{3.92}$$

where p_1 to p_4 and q_1 to q_3 are the fitting parameters. The parameters are calculated by the *Curve Fitting Toolbox*™ of Matlab® and are dependent on the temperature. The fit was applied at the logarithmic values of J_{Inj} which provided better results. The goodness of fit is shown in Table 3.2 at the end of this chapter and the results of the fitting function are shown in Figure 3.16. The TCAD simulation results of the large injector are in good agreement with the measurement results while the small injector reflects the maximum current density. This can be achieved for example by using a sensor node to inject current into the substrate. Hence, the current density is at its maximum because the substrate's series resistance of the anode is at its minimum which represents the worst case. The circuit simulation model was chosen to be pessimistic regarding the large injector but not as high as the worst case. This prevents circuit designs with an unreasonably high safety margin. The spread of the measurement results of the three main injectors is caused by minor differences in their layout. The metal wiring is slightly different for all three injectors as well as their size and the connection to the surrounding substrate area.

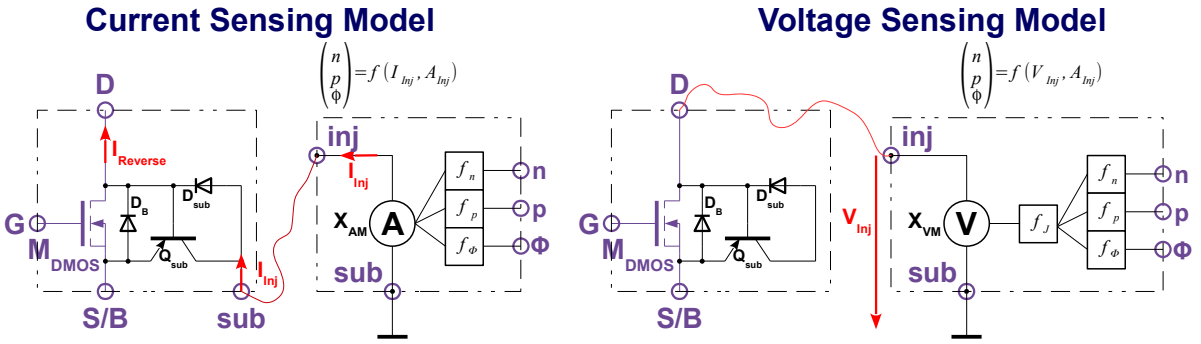


Figure 3.15: Current and voltage sensing injector circuit model

The output signals of the injector diode model are calculated by three separate curve fitting functions based on the current density J_{Inj}. The electron density is calculated by

$$\log\left(n_{Inj}\right) = a_n \cdot J_{Inj}^{b_n} + c_n \tag{3.93}$$

where a_n, b_n, and c_n are the curve fitting parameters. The hole density is determined by

$$\log\left(p_{Inj}\right) = a_p \cdot e^{b_p \cdot J_{Inj}} + c_p \cdot e^{d_p \cdot J_{Inj}} \tag{3.94}$$

and the curve fitting parameters are a_p, b_p, c_p, and d_p. The electron and the hole density both used logarithmic values of the carrier densities because the fitting function provided better results. The third and last curve fitting function for the injector diode determines the electric potential Φ_{Inj} directly underneath the pn junction and utilizes a second order exponential function given by

$$\Phi_{Inj} = a_\Phi \cdot e^{b_\Phi \cdot J_{Inj}} + c_\Phi \cdot e^{d_\Phi \cdot J_{Inj}} \tag{3.95}$$

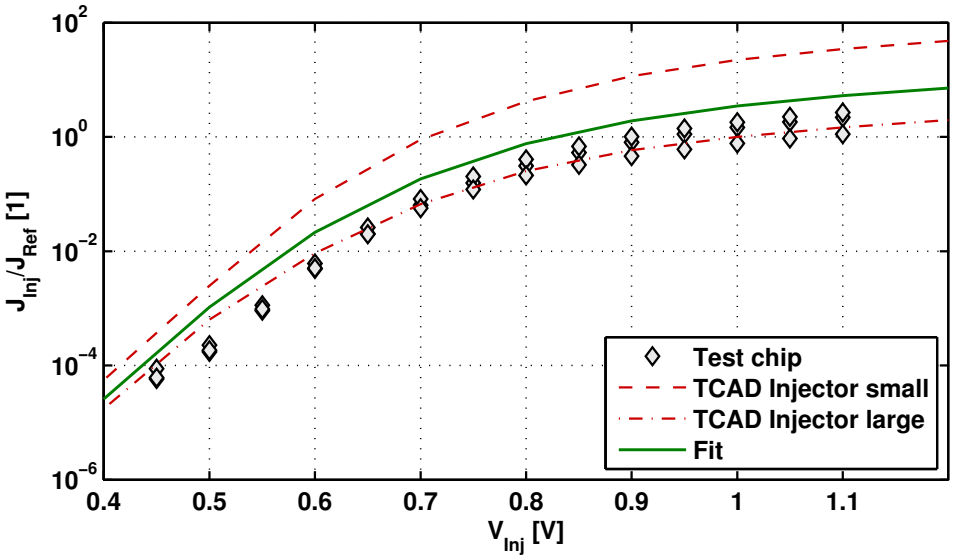


Figure 3.16: Influence of the injector diode area on the current density

where a_Φ, b_Φ, and c_Φ, and d_Φ are the fitting parameters. The goodness of fit is given in Table 3.2 for all three functions and the results are shown in Figures 3.17 and 3.18 respectively. The curve fitting in these three cases was performed purely on the results of the calibrated TCAD simulations because the carrier densities are unobservable during the measurements. Hence, the accuracy of the parasitic device model can only be determined for the entire coupling path and not for its intermediary values.

Considering the physics of a bipolar transistor as described in Chapter 3.3.4 and the operating principle of the parasitic element as described in Chapter 3.3.5 it is obvious that the coupling effect in its most primitive form can be described purely by the minority carrier concentration in the substrate. However, the circuit simulation model is intended to represent the simulation results of the drift-diffusion model and this includes the distribution of the majority carriers as well as the electric potential. Dependent on future requirements, this model can be enhanced to represent other substrate coupling effects as well. Additionally, the electric potential is necessary for the analysis of active guard structures.

Listing 3.7: Verilog-AMS carrier density signal

```
1 // ===== Nature and Discipline Declaration =====
2 nature Density
3   units  = "cm-3";
4   access = D;
5   abstol = 1;
6   blowup = 1e24;
7 endnature
8
9 discipline carrier
10   potential Density;
11 enddiscipline
```

Verilog-AMS does not provide any default signal type that represents charge carrier concentrations in a semiconductor. Hence, a new *nature* and a new *discipline* shown in Listing 3.7 are used to connect the different parts of the parasitic device model. The carrier density in Verilog-AMS is modeled like a *potential* and the definition of a *flow* component is omitted considering the concept of the parasitic device model.

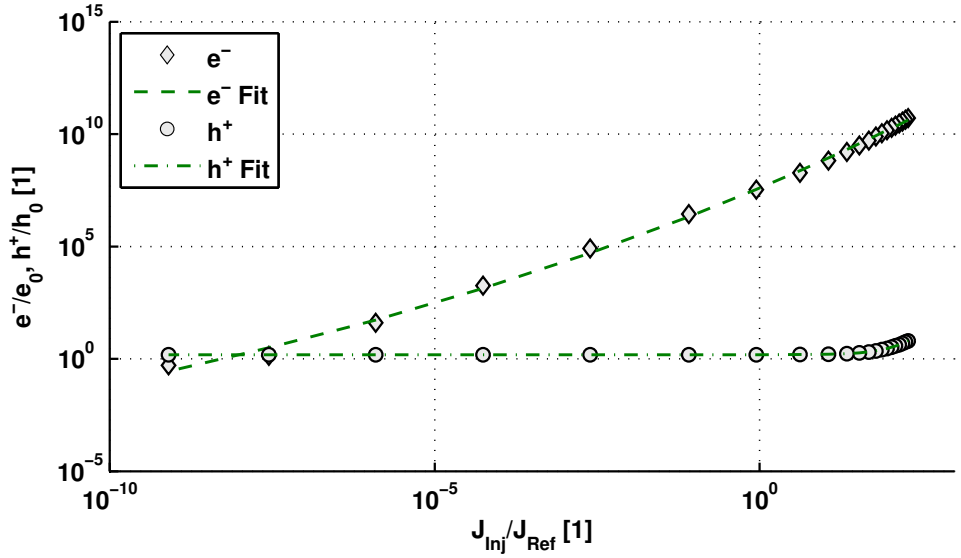


Figure 3.17: Carrier densities underneath the injector

3.7.2 Substrate Model

The substrate model receives its input data of the charge carrier densities n and p and the electric potential Φ from the injector model and determines the spatial propagation of the carrier densities and the electric potential in the substrate. The distance d between the two closest edges or corners is the dominant factor in the equations that describe the substrate behavior. However, the epitaxial wells of the injector and sensor are not constricted to purely quadratic shapes which means the minimum distance between the shapes and the area of the involved devices is not enough to accurately simulate the coupling effect. As illustrated in Figure 3.21, the coupling factor between sensor *S1* and the injectors *I1* and *I2* is different because the adjacent edges of *S1* and *I2* are larger than between *S1* and *I1* and therefore a higher coupling ratio is achieved. This is accounted for by additionally extracting the distance between the center of the sensor shape and the closest edge of the injector and calculating a weighted geometric mean by solving

$$\overline{d} = \left(\prod_{i=1}^{n} d_i^{w_i} \right)^{\frac{1}{\sum_{i=1}^{n} w_i}} . \tag{3.96}$$

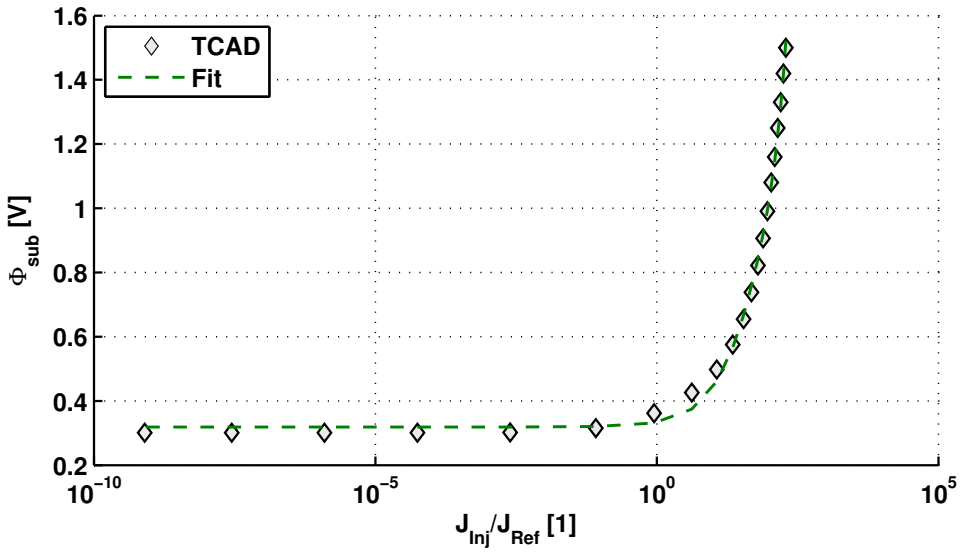


Figure 3.18: Electric potential underneath the injector

The weighted distance $\overline{d}$ is used in the subsequent equations to determine the spatial decay of the carriers. Nevertheless, this approach does not account for arbitrarily shaped geometries of the epitaxial wells and additional improvements are required.

The spatial decay of the electron current density shows an almost ideal exponential behavior without considering the influence of the drift component. Hence, the substrate model is based on Equation (3.89) to determine the carrier density under these conditions. However, when the electric field $\vec{E} \neq 0$ the current density Equations (3.13) and (3.14) have to be used. As stated by the authors of [79] the influence of the electric field cannot be easily calculated during circuit simulation but it is possible to apply the electric potentials at the substrate contacts and the injector as boundary conditions for the current density equations and a similar approach is applicable to Equation (3.89). The electric potential Φ_C of the substrate contact introduces an electric field which dissipates over the distance with $\vec{E}(r) \sim 1/r^2$ or—as a first order approximation—linearly towards the next substrate contact connected to ground potential. With this approach, the curve fitting functions for the spatial carrier decay can be enhanced by an additional term which emulates the influence of an electric field in the vicinity of a sensor node by either increasing or decreasing the values of the carrier densities. This leads to

$$\begin{aligned} \Delta_n &= f_n(\overline{d}, d_C, \Phi_C) \cdot \Delta n(0) \cdot e^{\left(-\frac{\overline{d}}{L_n}\right)} \\ \Delta_p &= f_p(\overline{d}, d_C, \Phi_C) \cdot \Delta p(0) \cdot e^{\left(-\frac{\overline{d}}{L_p}\right)} \end{aligned} \tag{3.97}$$

where d_C is the distance between the sensor and the substrate contact and Φ_C is the applied potential. This offers additional simulation capabilities to quantify the efficiency of simple active protection structures. However, the automatic identification of such structures has not been implemented yet and some of the parameters need to be defined manually in the simulation setup.

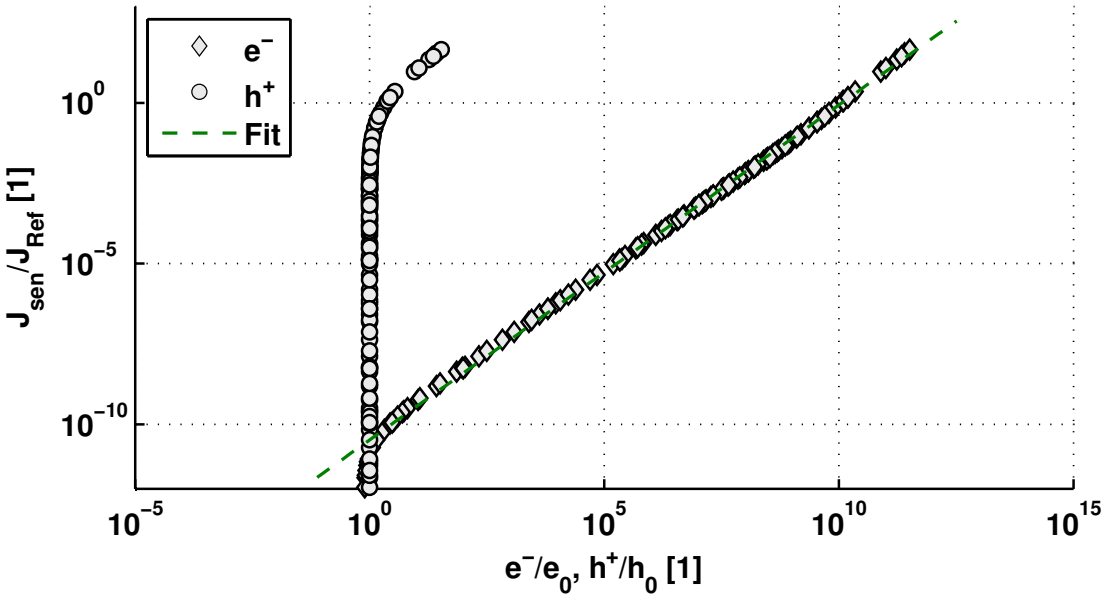


Figure 3.19: Sensor current density as a function of the minority carrier density

3.7.3 Sensor Diode

The parasitic current I_{Sen} is mainly caused by minority carriers that diffuse into the space charge region of the reverse biased D_{sub} of the susceptible devices. The electric field in the space charge region accelerates the minority carriers—in this case electrons—which traverse into the epitaxial well. If the epitaxial well is electrically floating its electric potential is lowered by the additional electrons or in case of an electrical connection the additional charge carriers cause a parasitic current to flow. The current I_{Sen} at the sensitive device is governed by the spatial gradient of the carrier densities which can be calculated by solving

$$\begin{aligned} \vec{J_n} &= q \cdot D_n \cdot \nabla n, \\ I_{Sen} &= A_{Sen} \cdot \vec{J_n}. \end{aligned} \tag{3.98}$$

However, results from TCAD simulations indicated that the electron density at the boundary of the space charge region is related to the current density of the sensor which is shown in Figure 3.19. Instead of solving a complex set of equations the electron densities obtained from the substrate model are used in another curve fitting function to approximate J_{sen}. The hole density in the substrate can be omitted because the hole current in the sensor is almost zero. The current I_{sen} is generated by a controlled current source and is connected to the sensitive node of the device. It can, however, not be attached to the *sub* node of the device Q_{npn} as shown in Figure 3.14 because the reverse–biased diode D_{sub} would prevent the current to flow causing the reverse voltage to increase until the simulator stops with an error.

The results shown in Table 3.2 are the goodness of fit for each of the curve fitting

functions used inside the parasitic device model. The values of the *sum of squares due to error* (SSE) and *R-square* are directly reported by the *Curve Fitting Toolbox*™ of Matlab®. The injector current density shows the largest deviation of the measurement data. It was decided to overestimate the injected current density to obtain an overall conservative model. The model is currently based on only a few measurements which were performed manually in a lab. Additional measurements on dedicated test structures are planned for the future and the model parameters will be updated accordingly.

Table 3.2: Goodness of fit for the curve fitting functions

Fit Function	**SSE**	**R-square**
Injector current density	$2.75 \cdot 10^{+01}$	0.984
Injector electron density	$3.52 \cdot 10^{-01}$	0.998
Injector hole density	$2.81 \cdot 10^{-04}$	0.999
Injector electric potential	$9.17 \cdot 10^{-03}$	0.997
Sensor electron density	$5.10 \cdot 10^{+00}$	0.998

3.7.4 Temperature Dependency

The temperature dependency of the parasitic effect has not yet been confirmed by measurements but only by means of TCAD simulation. Hence, Figure 3.20 shows the theoretical behavior of the current density of the injector dependent on the temperature of the IC. The parasitic device model applies the parameters of the curve fitting functions during the initialization step of the solver. Equation (3.92) is the curve fitting function that determines the injectors current density. Dependent on the temperature setting of the circuit simulation, the parameters p_1 to p_4 and q_1 to q_3 are scaled accordingly and the curve fitting function perfectly matches to the results of the TCAD simulation as illustrated in Figure 3.20.

The same approach is applied to all the curve fitting functions as given by the Equations (3.93) to (3.95) concerning the injector model. The substrate model is governed by the diffusion length L_n of the minority carriers and the *Debye* length L_p of the majority carriers as given by Equation (3.97). Both parameters are scaled based on the results of TCAD simulations.

3.8 Layout Extraction

Minority carrier injection is a top-level design issue which requires the analysis of the complete chip involving all the circuit components of the design. To enable a comprehensive risk assessment an automated extraction and back-annotation methodology which identifies all possible injectors and sensors on a chip was developed and implemented [113]. There are several possibilities how to identify the injectors and sensors of a circuit.

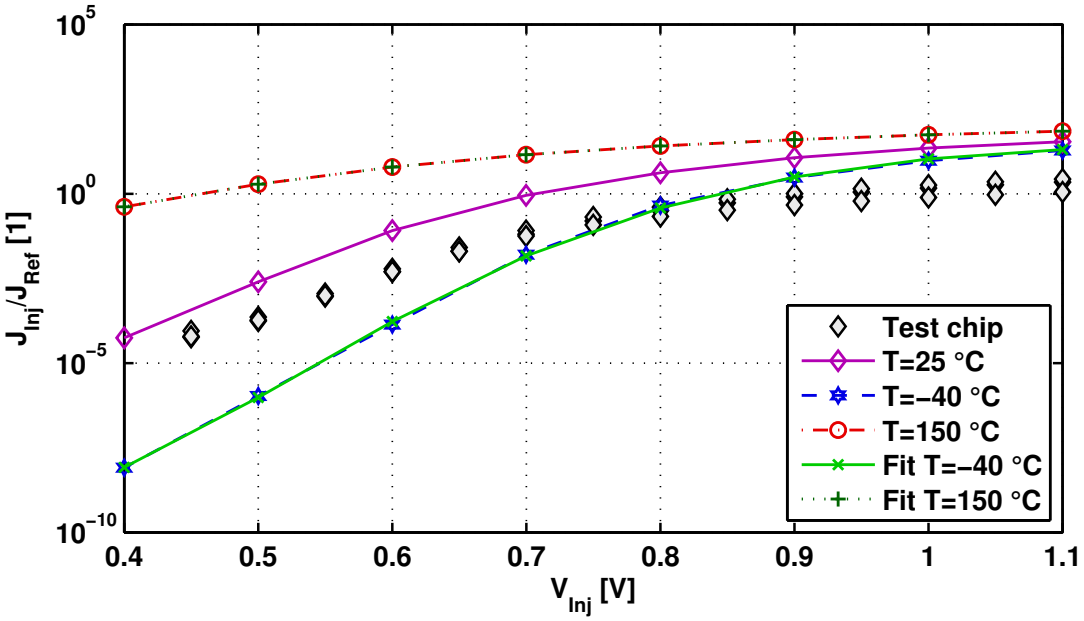


Figure 3.20: Temperature dependency of the current density

One possibility is to mark the injectors and sensors manually in either the schematic or the layout view. This approach poses the risk of missing critical structures and it requires extensive technological knowledge of the circuit designer. An automated approach based purely on the layout information has the advantage to identify all epitaxial pockets but has the disadvantage of generating a very large netlist. A similar approach is described by the authors of [114, 115] which works very well in conjunction with lumped models. However, is not well suited for the point–to–point model methodology discussed in this thesis. Every sensor needs to be connected to every injector which causes a large amount of interactions between all the epitaxial pockets. This is the primary reason why a different injector and sensor identification methodology had to be developed.

The example shown in Figure 3.21 illustrates how possible injectors and sensors can be distributed across the layout of a product IC. This makes device identification and especially parameter extraction a challenging task. The layout versus schematic (LVS) check typically extracts all the devices in a design and compares all critical parameters of the layout and the schematic database. It is used to verify that the design of the schematic and the layout are electrically equivalent and the chip does not contain any faulty connections. An already well established parasitic extraction flow which focuses on resistance, capacitance and inductance extraction of the designs metalization uses the LVS information as basis to create a simulation netlist as well. This is one of the reasons why the rule deck of the LVS was chosen to be enhanced to also determine the parasitic network for the substrate coupling effect. All the steps described in this chapter were performed by using Calibre® from Mentor Graphics®.

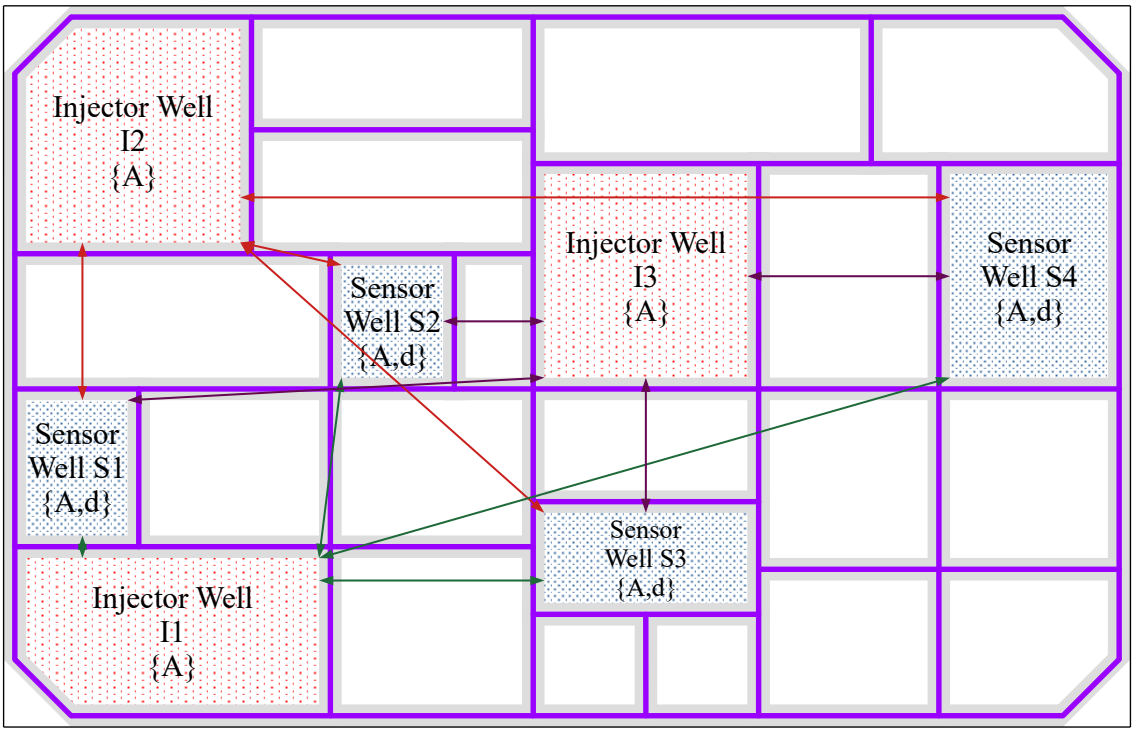


Figure 3.21: Simplified top-level view of a Smart Power IC

3.8.1 Identification of Injectors and Sensors

A purely layer-based extraction setup causes too many nodes to be extracted which have to be interconnected because basically every epitaxial well can be an injector or sensor of minority carriers. For example, Figure 3.21 contains a total of 24 epitaxial pockets and all of them need to be connected together. Using the point–to–point connection scheme the parasitic netlist would contain 24 injector connections and every one of them is connected to the remaining 23 possible sensor nodes. The number of connections can be determined by $n \cdot (n-1)$ and this small example already requires 552 connections.

The first step to reduce the amount of connections is to filter the epitaxial pockets by their technological connection to the designs devices. Using the same example shown in Figure 3.21, only 3 injector nodes and 4 sensor nodes remain causing the extracted parasitic network to contain 42 connections with the condition that every possible injector can also be a sensor node. If the injector nodes are—from a design point of view—robust enough to sustain collected parasitic currents the connections can be reduced to 12. However, while these reductions work well in this example the network created for the test chip contains approximately 1500 additional simulation nodes. Hence, the filtering of the network needs further improvement.

The implemented methodology utilizes a net-based approach where each connection to an epitaxial pocket is traced through the network of the design. This means the connection is not only filtered by its technological interaction but also by its connection

inside the circuit and the following net-based filtering rules are applied:

- Power supply/ground nets are considered to be safe
- Nets connected to I/O pads are potential injector nets
- All internal signal nets are susceptible
- Resistors propagate negative voltages
- Forward biased diodes propagate negative voltages

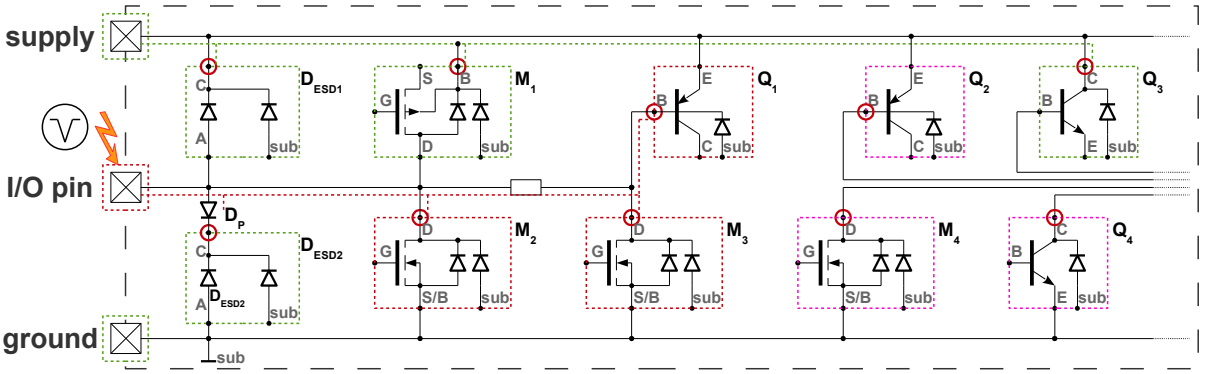


Figure 3.22: Principle of parasitic device identification

These filtering rules are combined with the technological interactions of the epitaxial pockets inside the device recognition of the LVS rule deck. From an LVS connectivity point of view, each epitaxial pocket is traced by its net information to all the other devices connected to the same net. As soon as a connection to a bonding pad is detected the net is marked as a potential injector net and all pockets attached to it are possible injectors. The main argument is that only inductances outside of the chip are large enough to pull down a node beneath the ground potential. Additionally, test pulses as discussed in Chapter 2.4 are applied at the application level and are also propagated into the chip from the outside. In the example shown in Figure 3.22 this is the case for the devices M_2, M_3 and Q_1. The *drain* terminal of M_2 and M_3 is connected to an I/O pin and can inject minority carriers into the substrate. Considering the cross section shown in Figure 2.1 also the *base* terminal of the bipolar transistor Q_1 is directly connected to the epitaxial pocket. The series resistance in the schematic between M_2 and M_3 does not stop the net propagation because it only attenuates the negative voltage but does not entirely inhibit it. However, the diode D_P protects the ESD structure D_{ESD2} and it does not count as an injector.

Direct connections of the epitaxial pocket to the power or ground network are discarded. Usually, the supply nets are very low ohmic and any disturbances caused by parasitic coupling via minority carriers only increase the power consumption of the chip. Any negative impact on the performance of the design should be negligible. For very sensitive nodes, however, the script can be adapted to include specific devices for detailed extraction. The example shown in Figure 3.22 contains the devices D_{ESD1}, M_1 and Q_3 which are assumed to be unaffected although their susceptible device terminals are formed by the epitaxial well.

The remaining devices M_4, Q_2 and Q_4 are identified as sensitive devices because their susceptible terminals are connected to internal nets of the chip. The filtering criteria inside the LVS is mainly based on the absence of bonding pads and a negative matching check concerning the supply network. The rule deck of the parasitic extractor performs the following steps:

1. Execute standard LVS
2. Create reverse current relevant connectivity stack
3. Predefine list with technologically susceptible devices
4. Filter *supply* network as given by the standard LVS
5. Filter nets connected to bonding pads
6. Create full chip device with injectors and sensors as terminals
7. Store net information and position parameters

While the first five steps are straight forward Steps 6 and 7 require some additional explanation. Device recognition shapes that overlap in the extraction stage of the LVS are merged into one single shape. This causes the individual injector–sensor pairs to become part of a single device recognition shape and the different pairs cannot be distinguished from each other any more. Hence, the approach is to define a recognition shape that engulfs the entire area of the chip and all the epitaxial pockets become *virtual* terminals of the device. However, any device in the LVS needs to be properly specified and an arbitrary number of terminals cannot be handled. The implemented solution is to utilize a single terminal which is the global substrate and to determine all other necessary data as parameters of the chip-wide device. An example of the source code is shown in Listing 3.8. The *"..."* in the source code are used to shorten the content. There are many more parameters extracted for each part of the parasitic device but they are not required to illustrate the concept of the layout extraction.

Listing 3.8: LVS source code of the reverse current device

```
1 // Chip - with DFM properties
2 revi_dfm_chp = DFM PROPERTY revi_chip revi_epi_net_inj
3                 revi_epi_net_sen revi_chip_ext OVERLAP MULTI
4 [ ni   =      COUNT( revi_epi_net_inj )   ]
5 [ ns   =      COUNT( revi_epi_net_sen )   ]
6 ...
7 // Injector - with DFM properties
8 revi_dfm_inj  = DFM PROPERTY revi_epi_net_inj revi_chip
9                   revi_enc_inj_all OVERLAP MULTI
10 [ net   =      NETID(      revi_epi_net_inj )   ]
11 [ posx  =     VECTOR( EWX( revi_enc_inj_all ) ) ]
12 [ posy  =     VECTOR( EWY( revi_enc_inj_all ) ) ]
13 [ sizex = PERIMETERX(      revi_epi_net_inj )/2 ]
14 [ sizey = PERIMETERY(      revi_epi_net_inj )/2 ]
15 // Sensor - with DFM properties
```

```
16 revi_dfm_sen  = DFM PROPERTY revi_epi_net_sen revi_chip
17                 revi_enc_sen_all OVERLAP MULTI
18 ...
19 // The full-chip parasitic device
20 DEVICE zrevi_full revi_chip revi_psub(sub)
21        <revi_dfm_chp> <revi_dfm_inj> <revi_dfm_sen>
22 [
23 PROPERTY chp_ni, chp_ns, inj_net, inj_posx, inj_posy, inj_sizex, ...
24 chp_ni         = DFM_NUM_VAL( revi_dfm_chp, "ni"    )
25 chp_ns         = DFM_NUM_VAL( revi_dfm_chp, "ns"    )
26 inj_net_       = DFM_NUM_ARR( revi_dfm_inj, "net"   )
27 inj_posx_      = DFM_VEC_ARR( revi_dfm_inj, "posx"  )
28 inj_posy_      = DFM_VEC_ARR( revi_dfm_inj, "posy"  )
29 inj_sizex_     = DFM_NUM_ARR( revi_dfm_inj, "sizex" )
30 inj_sizey_     = DFM_NUM_ARR( revi_dfm_inj, "sizey" )
31 ...
32 inj_net        = tvf_str_fun::revi_func::get_netvec( inj_net_   )
33 inj_posx       = tvf_str_fun::revi_func::get_vecarr( inj_posx_  )
34 inj_posy       = tvf_str_fun::revi_func::get_vecarr( inj_posy_  )
35 inj_sizex      = tvf_str_fun::revi_func::get_array(  inj_sizex_ )
36 inj_sizey      = tvf_str_fun::revi_func::get_array(  inj_sizey_ )
37 ...
38 ]
39 // Remove device
40 LVS FILTER zrevi_full OPEN LAYOUT
```

3.8.2 Parameter Extraction

As shown in Listing 3.8 the device parameters representing the parasitic coupling path are not directly extracted by the LVS. The LVS is used to determine the positions and geometrical properties of each individual injector and sensor. However, the LVS needs to be executed in flat mode to ensure the coordinate system represents the entire chip and not just hierarchical fragments of it. This is the main disadvantage because it increases the run time of the LVS. In addition to the geometrical properties every injector and sensor needs connectivity properties about its electrical connections inside the circuit. The LVS uses the net tracing information to differentiate between injectors, sensors and insusceptible nodes and additionally stores the nets of the circuit. These are used later on to generate the interactions between the injectors and sensors in the enhanced netlist. The information of the net tracing feature enables additional filtering capabilities during the simulation netlist generation which is performed by an additional script.

The extracted parameters of the injectors and sensors are primarily stored as *DFM Properties* during the LVS run. It is very important to ensure that each shape has exactly one data set for each parameter since all these data are later on converted to vectors being attached to the full-chip parasitic device. If a single value is missing, the vector information becomes corrupted and the results are incomprehensible.

In the final device statement specifying the full-chip parasitic device the injectors and sensors individual properties are converted to property vectors by *Tcl* procedures. The procedures `tvf_str_fun::revi_func::get_netvec`, `tvf_str_fun::revi_func::get_vecarr`, and

`tvf_str_fun::revi_func::get_array` are implemented to handle one type of data and its return values are attached to the device as parameters. This way an arbitrary amount of connections can be handled which is not possible by using dedicated device terminals. Finally, the verification database contains a single device representing all necessary parameters and netlist information to be processed further.

3.8.3 Netlist Generation

The final step which generates the enhanced circuit simulation netlist is implemented as a Perl script. It accesses the information generated by the enhanced LVS by means of the Calibre® *Query Server*. The two primary queries are stated in Listing 3.9. Line 3 and 4 instruct the results of the query to be written to an output file which is read by the Perl script. The script uses the cross reference between the schematic and layout net names to create a circuit simulation netlist which uses the namespace of the schematic. This feature only provides easier access for the designer to probe nets directly in the schematic and get the data displayed in the results viewer.

Listing 3.9: Source net name and layout netlist query

```
1 layout netlist names none
2 layout netlist hierarchy flat
3 layout net xref write $revi_args{file_cqr}
4 layout netlist  write $revi_args{file_cqr}
```

At first, the design hierarchy is reconstructed by the script and a complete simulation netlist of the chip's top-level is created and stored inside a hash. In the final lines of the query's output the information of the full-chip parasitic device is located. A simplified example of the format is shown in Listing 3.10. The device contains the complete list of properties as stated by the LVS device recognition statement in Listing 3.8. The Perl script parses the information and stores all the necessary data for each injector and sensor. The parasitic coupling network is generated depending on the filtering criteria applied to the total netlist. The coupling parameters of the Verilog-AMS models are calculated by this script which includes the weighted distance $\overline{d}$ as given by Equation (3.96) and the area of the injectors and sensors epitaxial pockets. The results are appended to the circuit simulation netlist and an example is shown in Listing 3.11.

Listing 3.10: Source net name and layout netlist query

```
1 X738 1 zrevi_full chp_x=1436.4 chp_y=1336.4 chp_a=1.88026e+06
2 chp_ni=17 chp_ns=571
3 inj_a="138449.88 # 6721.53 # 25309.08 # ..."
4 inj_net="3.0 # 4.0 # 5.0 # ..."
5 inj_posx="416.95 , 0.0 , 543.35 , 0.0 # ..."
6 inj_posy="0.0 , 993.65 , 0.0 , 51.95 # ..."
7 inj_sizex="476.1 # 89.8 # 206.1 # ..."
8 inj_sizey="290.8 # 74.85 # 122.8 # ..."
9 sen_a="4304.39 # ..."
10 sen_net="241.0 # ..."
11 sen_posx="355.7 , 0.0 , 1032.9 , 0.0 # ..."
12 sen_posy="0.0 , 231.2 , 0.0 , 1015.15 # ..."
```

```
13 sen_sizex="47.8 # ..."
14 sen_sizey="90.05 # ..."
```

The parasitic device `XRevI_IS01` is connected to an injector which consists of several power devices (`XM8` to `XM11`) connected in parallel by `net6`. The sensor is formed by a zener diode `XD0` connected by `net0751`. The voltage at the injector terminal is measured and when it becomes negative with respect to the `GND` node a current is pulled from the sensor terminal. The current is dependent on the area of the injector and sensor given by the parameters `areai` and `areas` and the distance specified by parameter `dc`. All other injector–sensor pairs are included in the circuit simulation in the same way.

Listing 3.11: Circuit simulation netlist including injector–sensor pairs

```
1 XM8    net6  GATE_LS  net06  GND  mn4 n='7268'
2 XM9    net6  GATE_LS  net06  GND  mn4 n='6478'
3 XM10   net6  GATE_LS  net06  GND  mn4 n='6242'
4 XM11   net6  GATE_LS  net06  GND  mn4 n='5945'
5 XRevI_IS01  net6  GND  net0751  GND
6   zrevi_injsen  areai='138449.88'  areas='4304.39'  dc='336.62'
7 XD0  GNDD  net0751  GND  zdx n='1'
```

In addition to the filtering capabilities of the LVS rule deck as described in Chapter 3.8.1 the Perl script provides the opportunity to specifically select a single or multiple injector nets. In this case the enhanced circuit simulation netlist contains all injector pockets attached to these nets and only generates the injector–sensor pairs associated with it. The substrate coupling analysis of a typical Smart Power IC can be split up into several smaller independent simulations. Experience showed that most parasitic netlists can be reduced to a few hundred parasitic injector–sensor elements and the impact on the simulation time is minimal.

Chapter 4

Test Chip Design and Measurement Setup

4.1 Necessity of a Test Chip

To calibrate the TCAD simulation and validate the proposed method, it was necessary to perform measurements of minority carrier injection on a chip. In order to derive a simulation model the following analyses had to be enabled:

- Spatial decay of the effect over distances of up to 1 mm
- Current injection directly by the epi–to–substrate diode
- Analysis on the applicability of reverse current guard rings
- Influence of the electric potential of epitaxial wells
- Simultaneously active injectors
- Susceptibility of low– and high–ohmic sensors
- Sensors and injectors with different areas

Although minority carrier injection also occurs in productive ICs, measurements performed on products provide only limited information about the underlying physical behavior. The first limitation originates from the fact that all devices on a product are interconnected and parasitic currents pass through the circuit on arbitrary paths. This makes it extremely difficult to determine the exact magnitude of the disturbance and only its effects on the design can be monitored. For a few selected devices—those with direct connection to the epitaxial well—it is possible to directly measure the parasitic current under the condition that these nodes are accessible from the outside. Secondly, the available space on a product IC is very limited and adding dedicated structures for measurements of a parasitic effect is a costly task. Using a product also adds restrictions to the degree of freedom regarding the placement of the sensitive nodes and the requirements listed above could not be entirely satisfied. With this in mind it was decided in the early phase of this thesis to design dedicated test chips for two technologies.

Both technologies are based on the deep–trench isolation technique and show similar behavior when it comes to minority carrier coupling effects through the substrate. The

doping concentration of the substrate is the same but the trenches are different. The trench of test chip A has a higher doping concentration of the poly–Si which reduces the contact resistance to the substrate. Any differences which influence the coupling effect will be discussed in the following chapters whenever it is necessary to distinguish between both chips. However, the main design concept for the test chips is the same.

4.2 Main Features of the Test Chip

Figures 4.1 and A.2 show the top level view of the test chips that were developed during the course of this thesis. Their main focus is to provide an insight to the governing physical parameters of minority carrier injection. For simplification, *Test Chip A* will be discussed in detail because it was the first one to be developed, manufactured and also measured.

From past experience it is known that the effect is very sensitive to the electrical bias of structures in the vicinity of the injector and the sensors. Therefore, special attention was given to the design of the substrate network and the epitaxial pockets. These pockets usually contain the devices of the design as shown in Figure 2.1. On the test chip, three of these pockets contain DMOS devices which are utilized as the main injectors. They are located at the vertical center of the test chip to minimize any possible effects caused by the edges of the chip. Each injector can sustain continuous currents of up to 1 A. Usually the reverse current is split between the bulk diode D_B and the substrate diode D_{sub} (see Figure 2.6) which leads to a substrate current of approximately 200 mA. However, the source/bulk terminal can be left unconnected and the entire drain current is forced to pass through D_{sub}. In order to have a good carrier injection capability, the substrate connection in the close vicinity of the injectors is as low–ohmic as possible which reduces the series resistance at the anode of D_{sub}.

The other epitaxial wells are either utilized as susceptible nodes or they are connected to each other in several independent clusters. All of them can be separately biased which introduces additional analysis capabilities. Every single sensor node is directly connected to one of the bonding pads of the chip and can be accessed directly during the measurements. The size of the sensors varies between 625 μm^2 and $10,000$ μm^2 and the distance between injector and sensor is up to 1.5 mm. The sensors are designed with low– and high–ohmic connections to the buried layer. This is achieved by either adding or omitting the n–doped sinker structure (see Figure 2.6) for the sensor wells.

Every epitaxial pocket is surrounded by a deep–trench ring and these conjoined trench rings form the substrate network of the test chip. In selected areas the trenches are connected by metal wires to different bonding pads on the test chip. In addition, the metal wires are split up into independent groups which enables localized substrate areas which can be biased with different potentials. This is necessary for guard ring concepts which rely on introducing electrical fields in the substrate in order to influence the motion of the charge carriers. Since the trench itself is filled with doped poly–Si (see Figure 2.1), it forms an ohmic connection on top of the silicon substrate and puts a limit on the performance of some guard rings.

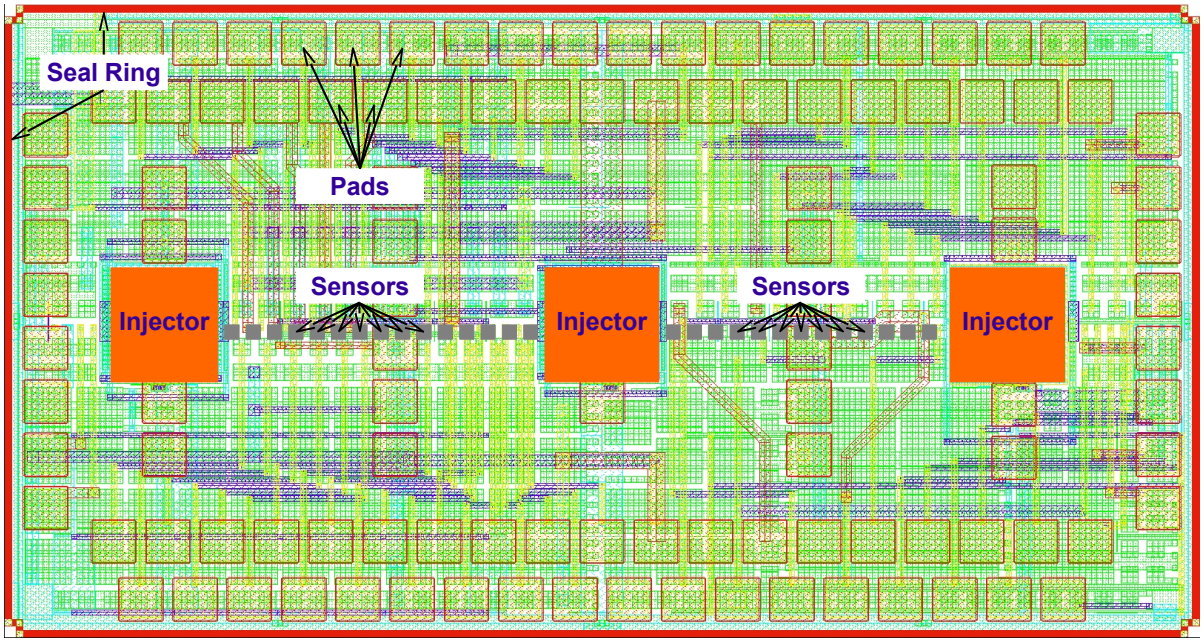


Figure 4.1: Test chip for substrate minority carrier injection

Based on this concept for the test chip, the total number of pads increased to 115 for test chip *A* and 94 for test chip *B* (see Table 4.1). While the absolute minimum number of concurrently connected pads is 3—which connects one injector, the substrate and a single sensor or cluster—many of the pads have to be connected to obtain results that reflect the behavior on a product IC. For example, connecting the substrate via a single bonding pad leads to a high series resistance for the *p*–doped anodes of the substrate diodes D_{sub}. Additionally, in product ICs the substrate network is as low–ohmic as possible to prevent ground potential shifts in the design. To provide measurement results which are as close as possible to the behavior of a product IC, the smallest number of connected pads has to involve the entire ground network, the epitaxial pocket clusters, and most of the sensors. This leads to approximately 40 simultaneously connected pads during the measurements.

Table 4.1: Test chip pin list

Bonding Pad Type	**Number of Pads on Test Chip**	
	A	***B***
Independent sensors	86	43
Pocket clusters	9	16
Ground network	12	12
Main injectors	3	3 (+5)
Guard structures	5	15

With a needle probe station in the lab only a few electrical connections to the test

structures can be made at once, especially when the positioning of the needles is done manually. This constraint reduced the number of available options concerning the measurement concept of the test chip. To design a probe card and implement a test program for a wafer prober makes sense when many measurement series have to be performed for example when statistical data are needed. However, such a requirement did not exist at the early stage of this thesis and the cheapest option was to mount the chip in a ceramic package.

Additional requirements and limitations on the design were raised because the test chip is part of a shared reticle and the final wafers will be diced. Hence, the chip had to became more like a typical product IC and any negative impact on the accuracy of the measurements had to be avoided. Instead of just having a reserved area on the wafer for the measurement structures, the chip also needed a complete seal ring structure surrounding it. This forms a mechanical and electrical barrier between the design area and the scribe line on the final wafer. It also contains a permanent connection to the substrate by a trench ring and one of the ground pads is only connected to this ring.

The available space for the chip also limits the number of bonding pads that can be used and a trade–off between design costs and bonding capability had to be found. It was decided to mount the test chip in a 144 pin ceramic package and the bonding diagram is shown in Figure 4.2. However, the total number of pins could not be utilized due to bonding constraints and only a significant increase in chip area could have solved this issue. Finally, the test chip was bonded with 50 μm gold bond wires which have a fusing current capability of greater than 1.5 A. This exceeds the maximum DC current of the measurements which is less than 200 mA. The maximum resistance contribution of the bond wires is

$$R_{Bond,max} = \rho \cdot \frac{\ell}{A} = 2.2 \cdot 10^{-8}\ \Omega m \cdot \frac{5\ mm}{2500\ \mu m^2} = 56.02\ m\Omega\,(@T = 23\ ^\circ C) \tag{4.1}$$

and has to be taken into account at the measurements.

4.3 Basic Measurement Setup

The basic measurement setup for minority carrier injection is illustrated in Figure 4.3. The Device–under–Test (DuT) is plugged into the socket at the center of the laboratory board and every pin of the IC is connected to the banana jacks at the edge of the PCB. Standard 4 mm lab cables are used to connect the test board to the lab appliances.

In the most simple setup only two power supplies are necessary to provide the necessary voltages for the measurements. The power supply V_{Sup} provides the reference potential and is connected to the epitaxial pocket clusters which span a large area of the test chip. This is similar to the situation in product ICs where most of the epitaxial pockets are connected to the supply voltage to keep the substrate diode D_{sub} reverse biased (see Figure 2.6). Since the pocket clusters are not interconnected inside the test chip, all connections have to be handled at the PCB level.

The power supply V_{Sup} is operated as a voltage source and without any injector current,

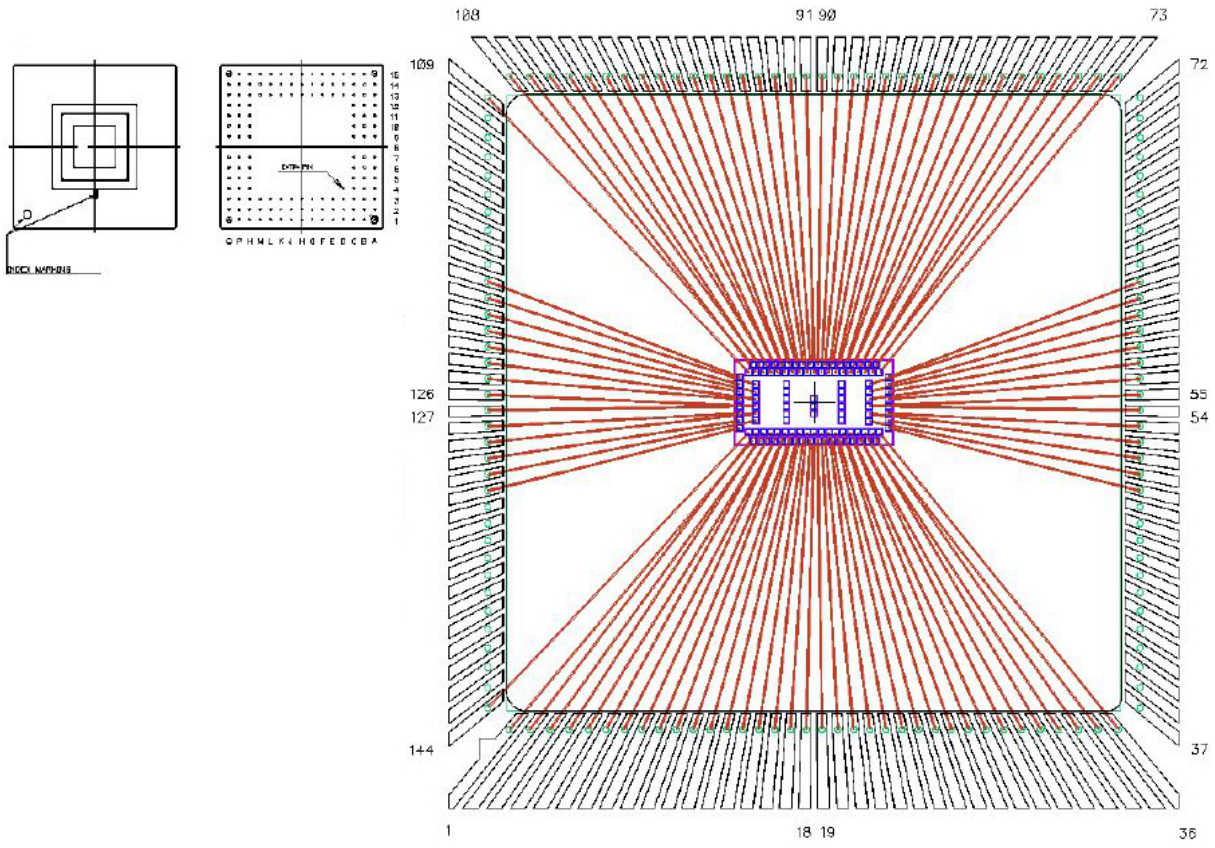


Figure 4.2: Bonding diagram for the ceramic package

the current $I_{Sup} \approx 0\ A$. Since all substrate diodes are reverse biased, I_{Sup} is the sum of all leakage currents of these diodes. This situation changes when I_{Inj} is turned on.

The second power supply is operated as a current source and creates the injection current I_{Inj}. The plus terminal of the injector supply is connected to the reference network and the minus terminal is connected to the injector node which pulls the cathode of the substrate diode D_{sub} below the ground potential and minority carriers are injected into the substrate of the test chip. The voltage V_{Inj} adjusts itself according to the overall impedance of the measurement structure and the forward voltage of D_{sub}.

Although both power supplies display voltage and current directly, they are additionally connected to digital multimeters for accuracy reasons. Especially for very small injection currents the internal ammeter of the power supply was not accurate enough.

The parasitic currents I_{Sen} occur when the injector current I_{Inj} is turned on. The sensor nodes can either be connected to the ground network or the power supply rail to measure I_{Sen}. This also enables the possibility to analyze the influence of the epitaxial pocket potential on the collected parasitic current.

The third option is to leave the sensor node unconnected or connected to a high impedance node which is illustrated by the voltmeter V_{Sen} in Figure 4.3. In this case, the parasitic current through this node is approximately 0 A but the epitaxial pocket of the

sensor is charged to V_{Sen} by the charge carriers diffusing into the pocket.

Due to the limited number of available multimeters the measurements of the 86 sensors were performed consecutively and only a few sensors were attached to multimeters at any time. The other sensors were connected to the same network node as those with the multimeters to ensure that all sensors are biased in the same way. An overview of the lab equipment is given in Table 4.2.

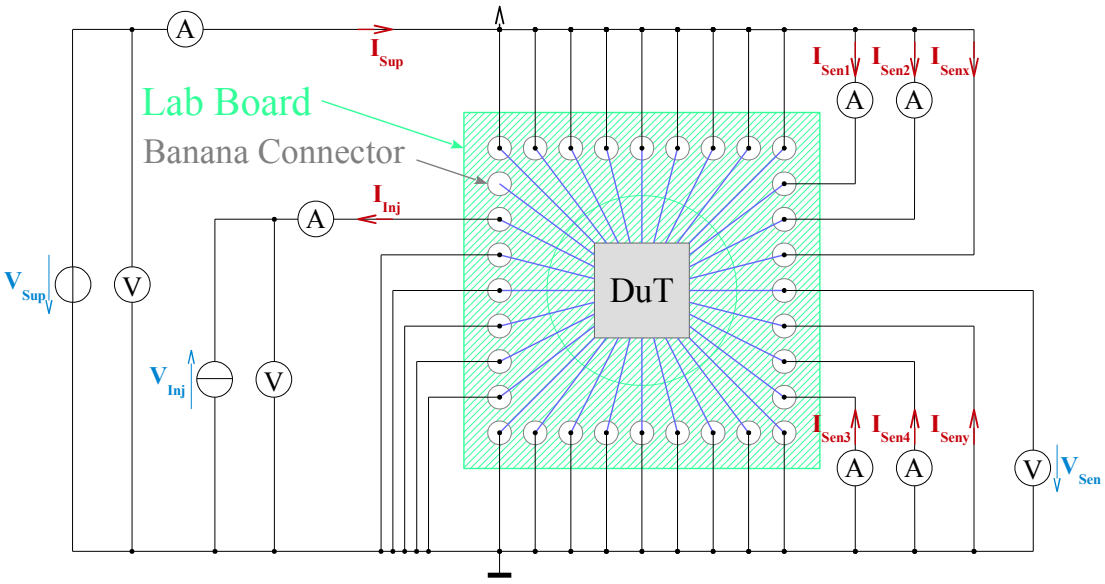


Figure 4.3: Basic measurement setup with the device under test

Table 4.2: Lab equipment overview

Equipment type	Appliance used
Main power source (e.g. injector)	HP E3632A
Secondary power source (e.g. supply)	TTi EX752M
Digital multimeter	Keithley 2000 Keithley 2001 Keithley 199 Iso-Tech IDM-62T
Oscilloscope	Agilent DSO-X 3034A

Photographs of the lab setup and the test board are shown in Figure 4.4. The test board was not specifically designed for this test chip but is a general purpose lab board which was reused for the measurements performed for this thesis. In addition to the banana connectors there is a ring of jumpers available surrounding the DuT. Depending on the measurement setup, the jumpers were used to connect several pins of the test

chip to the ground potential. This option significantly reduced the number of lab cables needed to connect the chip.

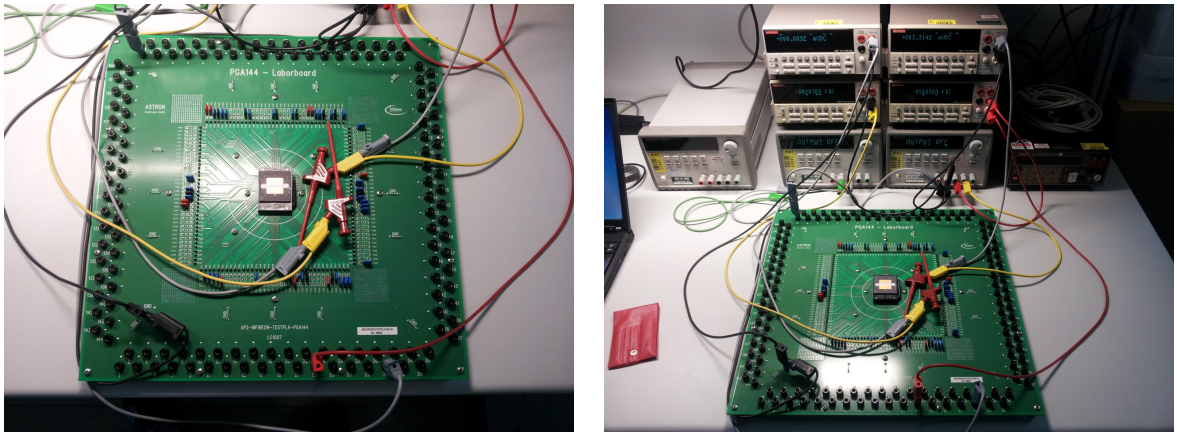


Figure 4.4: Test board and measurement setup

4.3.1 Resistance Contributions

Experience from the past showed that the quality of the measurement results is highly dependent on the resistance of the connections to the epitaxial pockets and the substrate network. Therefore, a detailed analysis on the resistance contributions of the measurement setup was performed and the maximum resistance values are shown in Table 4.3. The lines with the highest contribution to the overall resistance are marked in red.

The ground network of the test board was measured with an ohmmeter for each pin and the maximum value is 15 $m\Omega$. The lab cables contribute another 45 $m\Omega$ when the cable is less than a meter long. The metalization of the PCB is also considerably small with 75 $m\Omega$. The highest resistance is actually caused by the ammeter [116, 117] but can be avoided by changing the measurement range. For larger current ranges, the inner series resistance of the ammeter is only 100 $m\Omega$. In that case, the overall resistance becomes dominated by the n–doped epitaxial well with the n–doped sinker and the resistance of the on chip metalization.

The resistance of the sinker is an estimated value determined by

$$R_{sink} = \rho \cdot \frac{\ell}{A} \tag{4.2}$$

where ρ is the resistivity of the doped silicon, A is the area of the sinker and ℓ is the depth of the structure. The resistance of the chip metalization was determined by layout R–extraction and back–annotation. The range of the metalization resistance is between 0.9 Ω and 6.7 Ω with a mean value of 2.3 Ω. The bonding wire including the die bump adds another 130 $m\Omega$ to the total resistance and the contribution of the C-PGA package is approximately 1 Ω. If only a single connection to the chip's substrate is used, the contribution of the deep trench is less than 5.0 Ω.

The resistances of the lab setup and all the cables including the metalization resistances of the package and the chip are in the 10 Ω region while the inner resistance of the ammeter is either 10 Ω, 100 $m\Omega$ [116], or 20 Ω [117]. This means for higher current measurement ranges, the error caused by the ammeter is negligible. Also on a product chip the impedance of the net that is connected to the susceptible pocket will be much higher because the metalization of the test chip was designed to have a high current capability and a very low impedance. This means the measurement results provided by this thesis can be considered to be the worst case scenario.

Table 4.3: Resistances of the measurement setup

Resistance cause	**Resistance, max.**
Lab board ground network	15 $m\Omega$
Inner resistance ammeter	20 Ω
Lab wiring	45 $m\Omega$
PCB wiring	75 $m\Omega$
IC Package, est.	1 Ω
Bonding wire with die bump	130 $m\Omega$
Chip metalization, extracted	6.7 Ω
Well resistance, est.	10 Ω
Trench resistance, est.	5 Ω

4.4 Detailed Measurement Setups

The measurement setup discussed in Chapter 4.3 forms the basis for all the measurements performed in the course of this thesis. The following chapters contain elaborate information about the objective of the measurements and details about each of the setups. The content of the figures is simplified and shows only relevant aspects. The cross section emphasizes the region of interest which usually is the geometrical relation of the injector and the sensors on the test chip. Any additional information is contained in the description of the measurement.

4.4.1 Spatial Decay of the Sensor Current

The most commonly question asked by the design community was at what distance is a susceptible node unaffected by minority carrier injection. To answer this question, the measurement setup shown in Figure 4.5 was designed. One of the main injector nodes is pulled below ground potential and the parasitic current at the sensor nodes is measured consecutively. This will provide data on how the parasitic current decays over the distance from the injector. One condition for this measurement to work properly is to connect all

substrate and supply pads to prevent any substrate potential shifts except the one caused by the main injector. The main injectors are almost quadratic with $w_{inj} \approx 250\ \mu m$.

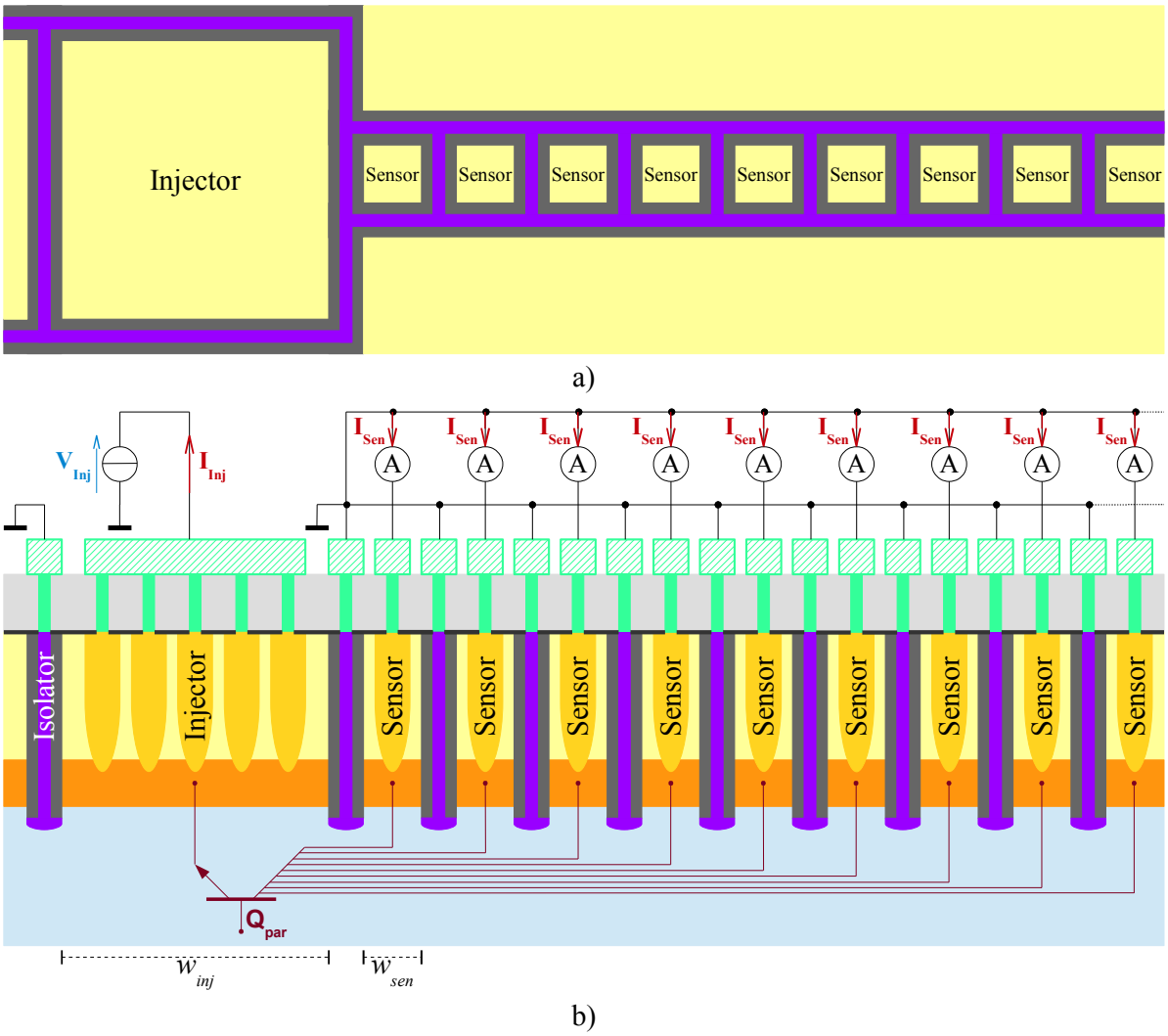


Figure 4.5: Measurement setup for the sensor current decay

The sensors are organized in several arrays along the vertical centerline of the chip (see Figure 4.1). The shape of the sensors is quadratic and $w_{sen} = 25\ \mu m$ for the smallest sensors that are available on the test chip. The maximum distance that can be achieved between the main injectors and the sensors is 1.5 mm. However, the expected parasitic current at such distances is in the fA range and measurements of such small currents are not feasible with this equipment. All three ammeters have approximately the same limits considering the requirements of the measurement setup. For example, at 10 nA resolution (20 mA range), the burden voltage is 0.4 V which translates to a resistance of 20 Ω [117]. At this measurement range, the ammeter contributes $\approx 2/3$ of the total series resistance of the measurement setup. With 1 nA resolution, the resistance of the ammeter is at 155 Ω and already significantly higher than all other resistances. Therefore, the minimum

resolution available for these measurement is 10 nA which corresponds to an estimated distance between injector and sensor of 500 μm at an injection current of 100 mA.

4.4.2 Superposition of Injectors

There are many possibilities how multiple injectors can become active at the same time on a product IC. For multichannel switches, several independent power devices can get pulled below ground by simultaneously switching inductive loads. However, it doesn't need multiple power devices to end up in a situation where multiple injectors become active. In modern ICs the power devices are connected to many different circuit parts which—for example—handle diagnostic functions. When the drain net of the power DMOS gets pulled below ground potential the devices connected to that net can become injectors as well. This situation is illustrated in Figure 3.22. The question of the chip designers is about the behavior of the parasitic current at the susceptible nodes.

Since the main injectors of the test chip can be biased separately two of them were connected to individual current sources (I_{Inj1} and I_{Inj2} in Figure 4.6). Both injectors force minority carriers into the substrate which then diffuse to the space charge regions of the reverse biased sensors. The currents I_{Sen} for each sensor are measured consecutively again. However, the power supplies of the injectors are not just permanently switched on but the pattern shown in Table 4.4 is used. This way, the results of the spatial decay analysis can be reconfirmed for another injector and the individual and combined influence of the injectors on the sensors can be analyzed.

Just like in the setup discussed earlier, all other epitaxial pockets are connected to V_{Sup} and the complete substrate network is tied to the ground potential. The sensor nodes are located between the two injectors and connected to the power supply rail with ammeters in between.

Table 4.4: Power supply pattern for the superposition measurement

Status of		**Expected Measurement Result**
I_{Inj1}	I_{Inj2}	
Off	Off	Leakage current caused by V_{Sup}
On	Off	Parasitic current $I_{Sen,1}$ caused by I_{Inj1}
Off	On	Parasitic current $I_{Sen,2}$ caused by I_{Inj2}
On	On	Superposition of $I_{Sen,1}$ and $I_{Sen,2}$

4.4.3 Connectivity Options of Epitaxial Pockets

Considering Figure 2.3, any epitaxial pocket can potentially act as a source of disturbance or become a susceptible node. It all depends on the electrical bias of the epitaxial pocket and where it is connected to. As already stated in Chapter 3.8.1, connecting the

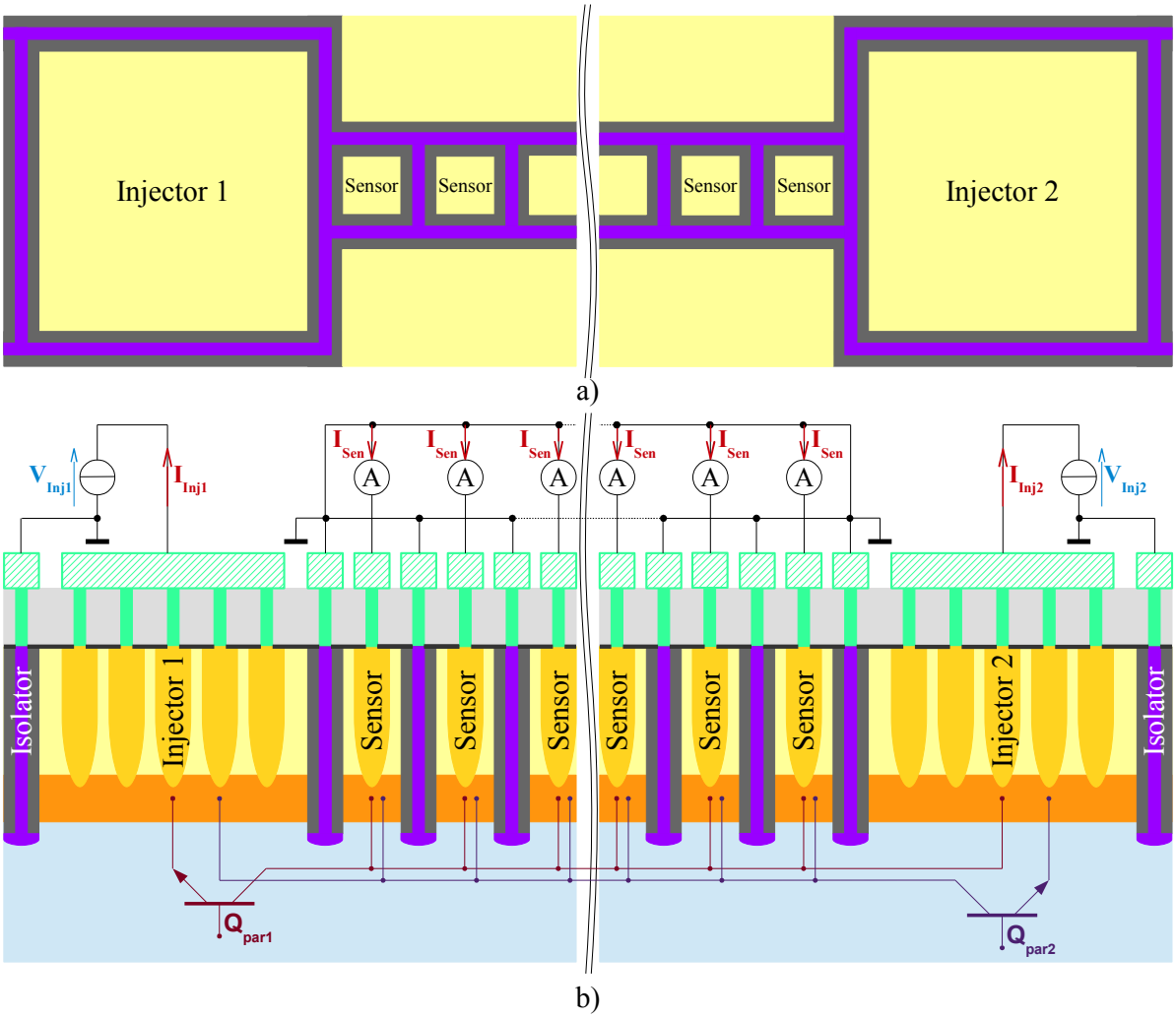


Figure 4.6: Superposition measurement setup

susceptible nodes to the ground network or the power supply usually does not negatively influence the operation of the circuit but only increases the supply current. The question is whether the electric potential and the change in width of the depletion region influences the collection of minority carriers. Additionally, a pocket at a higher bias voltage might also attract more carriers and could be utilized as protection. Therefore, three connectivity options of the epitaxial pocket clusters were explored in detail.

4.4.3.1 Connected to the Ground Potential

Connecting an epitaxial pocket to the ground potential is certainly enough to keep D_{sub} in reverse direction. However, if there are devices placed in that pocket, other *pn* junctions can become forward biased and the device will not function normally. This is the reason why the epitaxial pocket is usually connected to the highest electric potential any of the devices' terminals will reach during operation. However, it is the simplest form of

a layout–based protection structure available and was already discussed in Chapter 2.6.3. The measurement setup is based on Figure 4.5 and all epitaxial pockets—sensors and the clusters—are connected to ground. This should determine whether such a protection approach is feasible in this technology.

4.4.3.2 Different Supply Voltages

The typical setup for a product IC implies that the epitaxial pocket is connected to the supply voltage of the circuit. The question is if the electric potential applied to the pocket has an impact on the amount of the collected parasitic current. The reason for this question is based on the width modulation of the space charge region in dependence on the applied bias voltage [86] which can be estimated by solving

$$w_{DR} = \sqrt{\frac{2 \cdot \epsilon_r \cdot \epsilon_0}{q} \cdot \left(\frac{N_A + N_D}{N_A \cdot N_D} \right) \cdot (\Phi_0 - V_{ext})}. \tag{4.3}$$

N_A and N_D are the doping levels of the diode, n_i is the intrinsic carrier density and V_{ext} is the external bias voltage. The built–in potential of a pn junction is determined by

$$\Phi_0 = \frac{k \cdot T}{q} \cdot \frac{N_A \cdot N_D}{{n_i}^2}. \tag{4.4}$$

For D_{sub} the unbiased width of the depletion region is $< 1\ \mu m$ and with $12\ V$ reverse biased voltage the width becomes $\approx 3\ \mu m$.

Considering the distances for which this test chip was designed, the effect should be observable for sensors that are close to the injector but at distances of $500\ \mu m$, the influence is expected to be negligible. Additionally, the $3\ \mu m$ increase in the depletion region does not even exceed the depth of the deep trench. The measurement setup again is based on Figure 4.5 with all epitaxial pockets connected to V_{Sup} which will be set to different voltages.

4.4.3.3 High–Impedance Node

The third option is to keep the epitaxial pockets floating. The expected behavior is that the minority carriers will diffuse towards the depletion region and get collected by the floating pocket. These carriers will charge the pocket to a negative electric potential. When this potential gets closer to the potential of the substrate underneath, the electric field along the depletion region will diminish and no more carriers get collected.

The measurement setup works like those mentioned previously but all the pockets remain unconnected except for the one that is being measured. Additionally, the electric potential of the floating wells will be determined by voltmeter. This setup will confirm or disprove the expectations about the behavior of floating nodes.

4.4.4 Externally Applied Substrate Voltage

Instead of changing the connectivity of the epitaxial pockets, this setup is the first attempt to change the connection of the deep trench stripes which connect the substrate of the test chip. As illustrated in Figure 4.7 the deep trenches directly adjacent to the injector are connected to a pair of coupled power supplies. The voltage V_{GR} is applied to these trenches and introduces the electric field $\vec{E_{GR}}$ in the substrate underneath the injector. Since the poly–Si filled trenches form a resistive connection on top of the substrate, the other substrate contacts close to the injector remain unconnected. This is the only way to ensure the electric field $\vec{E_{GR}}$ can be introduced to the substrate without having another substrate contact limiting the voltage V_{GR}.

The third power supply injects the current I_{Inj} and the sensor nodes are again connected to ammeters which measure the current I_{Sen}. Depending on V_{GR}, the current at the sensor nodes is expected to change. However, V_{GR} also influences the forward voltage of D_{sub} of the injector. On one side of the injector V_{GR} has a negative bias with respect to the ground potential while on the other side it has a positive bias. This also means that one part of the *pn* junction experiences less forward voltage than the other part and V_{Inj} has to be changed to keep the injected current at the same magnitude.

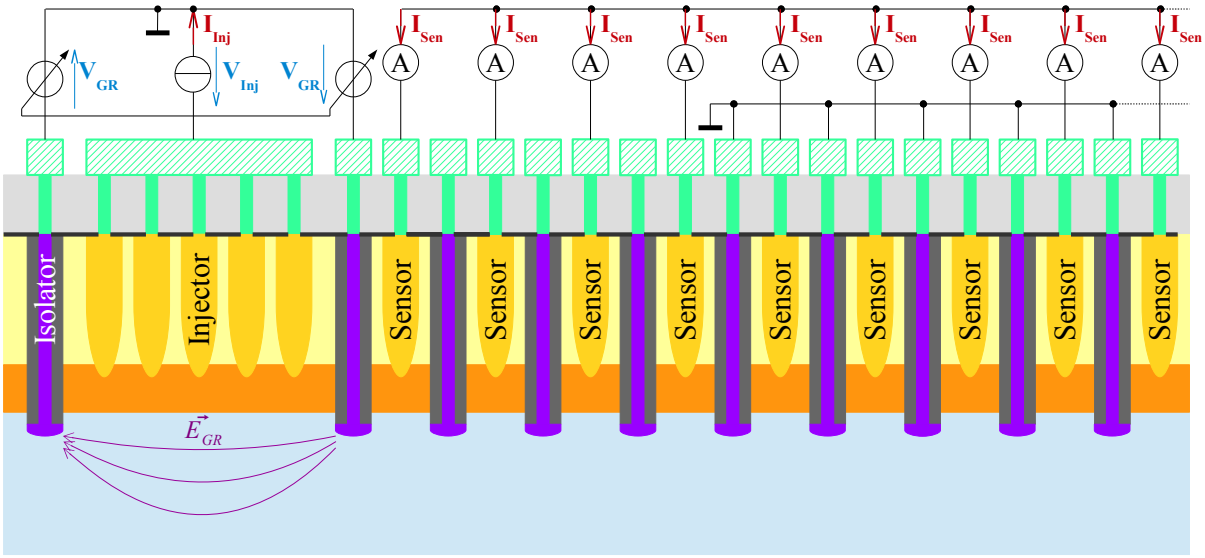


Figure 4.7: Externally biased deep–trench connection

4.4.5 Active Protection Structure

The final measurement setup addresses the performance of self–sustaining protection structures. They are directly adjacent to one of the main injectors and each structure consists of an epi pocket which acts as an intentional victim for the minority carriers in the substrate. The second part involves a segment of the deep–trench structure that surrounds the injector. The victim and the segment of the deep–trench are connected by

metal lines. A simplified overview of both structures is given in Figure 4.8. The structure is self–sustaining because it does not require any external biasing voltage to work but purely depends on the minority carrier collection capability of the *victimized* epitaxial pocket. The setup of the structure is based on the work proposed by [57] but had to be adapted for technologies based on the deep–trench isolation technique. This involved special attention to the substrate network surrounding the area of the injector. Since the trenches are filled with poly–Si, an additional resistive network forms on top of the substrate. For this test chip, a 100 μm long trench exhibits a lateral resistance of $\approx 40\ \Omega$. Since several of these trenches are connected to the surrounding network of trenches, the resistance of the substrate becomes small and limits the voltage drop capability of the guard structure. This situation was already known before the design and substrate contacts were avoided within a 200 μm radius around the edges of the injector.

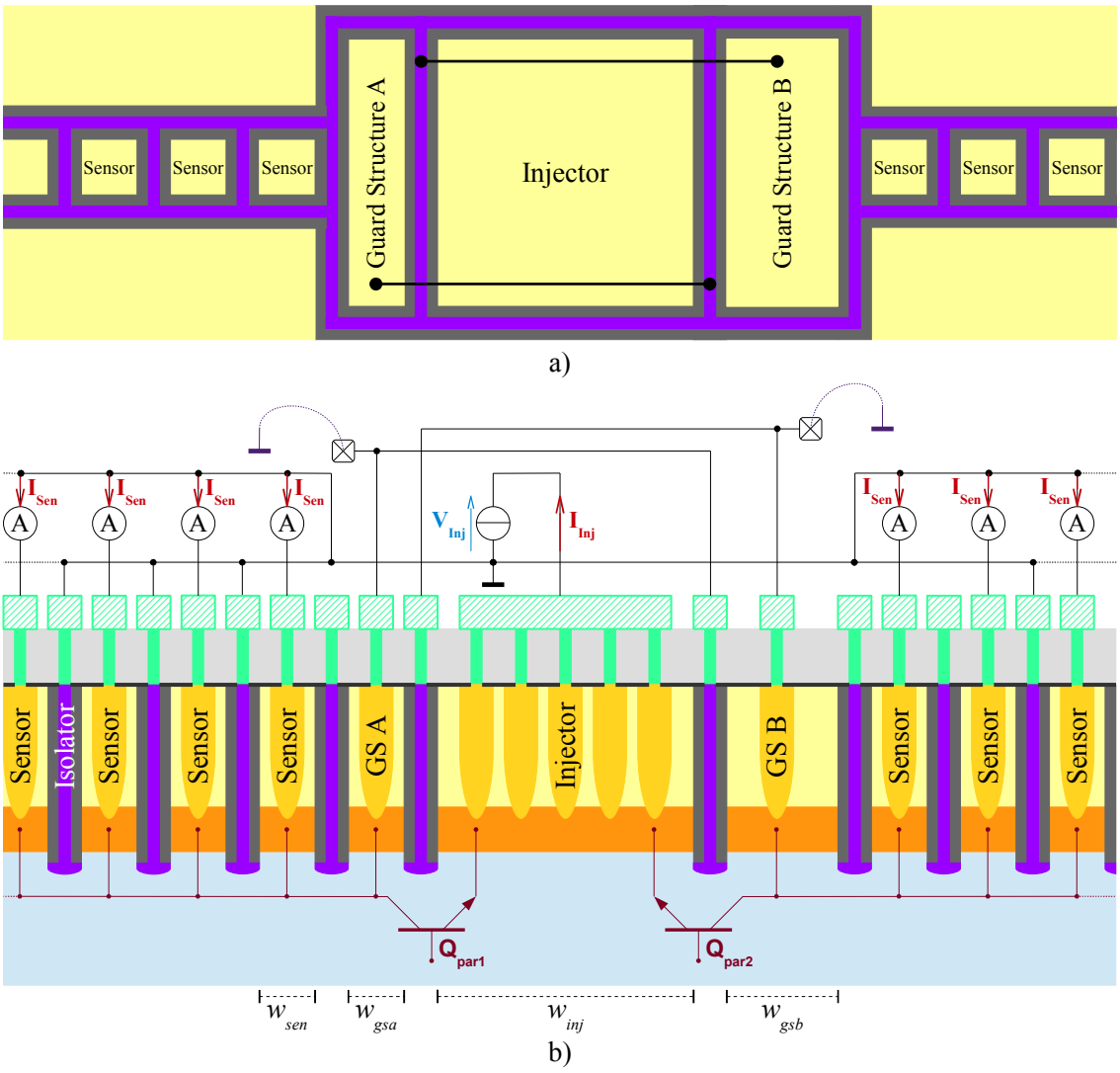


Figure 4.8: Internally biased deep–trench connection

In Figure 4.8, the epitaxial pocket of *Guard Structure A* is located at the left of the injector and has a width $w_{gsa} = 25\ \mu m$. As already stated, the efficiency of the structure should be as high as possible. Since the technological features cannot be changed at that point, only the geometry and the electrical bias remains. Hence, the epitaxial pocket spans the entire length of the injector in order to collect as many minority carriers as possible. The epitaxial pocket is connected by wide metal lines to the trench on the right hand side of the injector. Additionally, these metal lines are connected to a dedicated pad which enables external control on the behavior of the design.

For high efficiency, the electrical biasing has not been discussed yet because it is intertwined with a part of *Guard Structure B*. The substrate connection between the injector and the *victimized* epitaxial pocket (labeled as *GS A* in Figure 4.8) can be biased by the bonding pad of *Guard Structure B*.

The setup is mirrored for *Guard Structure B* which means the pocket is at the right side of the injector and the deep–trench is on the left. Additionally, the width of *Guard Structure B's* pocket $w_{gsb} = 50\ \mu m$. This was implemented to see if a small stripe of epitaxial pocket is sufficient for this protection structure to work properly or if a larger pocket is necessary. With the intertwined layout of these structures also here the substrate connection between the injector and the epitaxial pocket can be biased by the bonding pad of *Guard Structure A*. This layout leads to several interesting biasing possibilities.

4.4.5.1 Biasing of the Protection Structure

When *Guard Structure A* and *Guard Structure B* are connected to ground—with an ammeter in between—it is possible to measure the collected parasitic current of the corresponding epitaxial pocket which allows analysis of larger sensors directly adjacent to the injector. However, the connection to the substrate introduces a parallel current path that influences the accuracy of the measurement.

When *Guard Structure A* is kept floating and *Guard Structure B* is connected to ground, then *A* is working as protection structure as discussed by [57] and the sensors on the right side of the injector should see a reduced parasitic current. This reduction is caused by the voltage shift in the substrate which is introduced by the deep–trench connection. When the connection to the structures is inverted, then the sensors to the left should see the reduction effect.

When both guard structures are connected to each other without any external bias voltage, the resulting setup becomes a distorted version of [56] (see Chapter 2.6.3 for details). It is distorted, because the top and bottom side of the injector are not covered by the structure and the left and right side have different widths. Nevertheless, the underlying principle is the same and both pockets collect some minority carriers and get negatively charged. This charge is transferred to both trench structures between the injector and the pockets and pull the substrate below ground. The amount is dependent on the overall resistive network in the vicinity of the structure.

With an external positive bias, the epitaxial pockets remain reverse biased and the depletion region is modulated by the externally applied voltage. The deep–trench contact, however, introduces an electric field in the substrate similar to the setup described in

Chapter 4.4.4.

An external negative bias is also possible but its voltage capability is limited by the substrate diode of the epitaxial pocket. When the diode becomes forward biased, the epitaxial pocket turns into an injector. However, if the bias voltage is kept well below that level the structure can also be utilized to introduce an electric field in the substrate.

Chapter 5

Measurement and Simulation Results

The results shown in this chapter are based on calibrated TCAD simulations (see Chapter 3.6) and circuit simulations that utilize the Verilog-AMS model which is described in detail in Chapter 3.7. These simulation results are compared to measurements performed on the test chips which are discussed in Chapter 4. The temperature for the TCAD simulations was set to 300 $°K$, the circuit simulation was set to 21 $°C$ and the measurements were performed at room temperature ($\approx$ 21 $°C$). Each result focuses on a specific aspect of the parasitic effect and shows the capabilities and limitations of the proposed methodology.

5.1 Injector *pn* Junction

The first part of the parasitic coupling path is governed by the substrate diode D_{sub} which is formed between the epitaxial pocket and the substrate (see Figure 2.6). It determines the injected current I_{Inj} which is the main input for the Verilog-AMS model in the circuit simulation. Its performance is very important to the overall accuracy of the model because deviations in I_{Inj} cause shifts in all subsequent curve fitting functions. As described in Chapter 3.7.1, this diode may already be part of the PDK's device model or the substrate node may be inaccessible in the simulation netlist. In this case, V_D can be used as input and I_D is determined by an additional curve fitting function. The result of this fitting function is shown in Figures 5.1 and 5.2 as the blue colored curve labeled *Model*. The relative error [118] can be calculated by

$$\delta x = \frac{x_0 - x}{x} \tag{5.1}$$

and is ± 0.11 for the diode model at $V_D = 1.0\ V$. The result of this fitting function is used as I_{Inj} in the successive parts of the Verilog-AMS model.

The magenta colored curve labeled as *Diode* (Figure 5.1 and 5.2) shows an example of a substrate diode model that is part of a PDK. The diode is part of several components

(see Figure 2.6) representing parasitic coupling paths. At approximately 0.8 V, a series resistance of approximately 2.5 Ω becomes dominant and the simulated diode current I_D deviates from the measurements. Therefore, it cannot be used as direct input for the Verilog-AMS model.

The red curve labeled *TCAD* shows the result of the TCAD simulation. Starting at $V_D \approx 0.6\ V$, the current becomes lower than the measurement results. The relative error of the TCAD model is $\delta I_D \approx -0.21$. Although the simulation domain approximates the structure of the test chip, trade-offs had to be made due to limitations on the number of nodes ($< 150,000$) and its impact on the simulation runtime. One of these trade-offs concerns the simplification of the doping profile of the epitaxial pocket which is mainly responsible for the deviation from the measurements. Additionally, the metalization was not included in the setup and only the contact resistances were modeled. In a spatially reduced setup with accurate doping profiles, the TCAD simulation showed good agreement with the measurement. A detailed description of the TCAD setup can be found in Chapter 3.6.

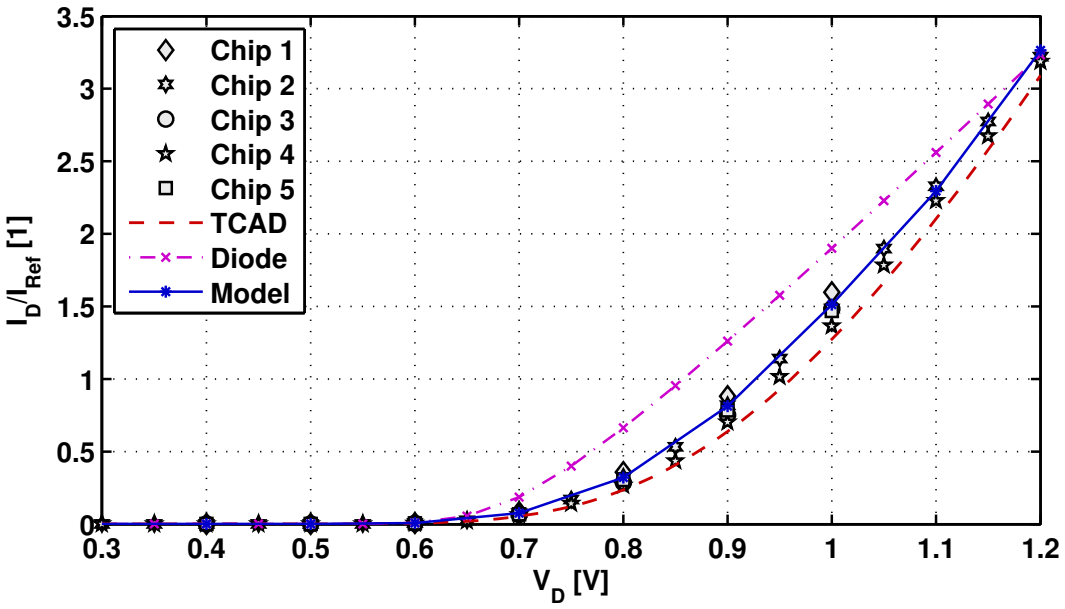


Figure 5.1: I-V characteristic of the injector diode

The measurements which are shown as black colored markers in Figure 5.1 were performed on five different test chips, all of them came from the same manufacturing lot. The minimum value for I_D at a bias voltage of 1 V is 82.7 mA and the maximum is 96.7 mA. This shows that even for such a small sample the differences between the test chips are very high. The fitting function of the Verilog-AMS model was configured to be within the minimum and the maximum values of the measurement. For example, at $V_D = 1\ V$, $I_{D,Model}$ is 91.6 mA.

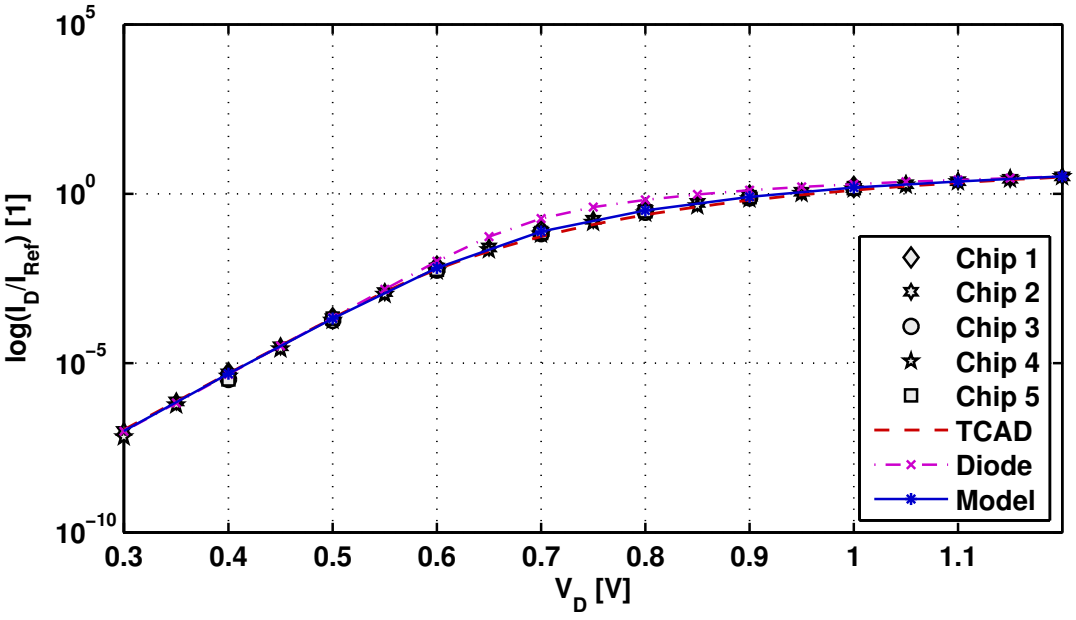


Figure 5.2: I-V characteristic of the injector diode (logarithmic scale)

5.2 The Parasitic Bipolar Transistor

The parasitic bipolar transistor is usually operated in common base configuration as illustrated in Figure 5.3. Two different measurements were performed to determine its main properties and to calibrate the TCAD simulation. The output characteristic was measured using the single collector setup. The injector–sensor pair that was used in the measurements is only separated by the deep trench isolation structure. The I_C–I_E characteristic—which relates the output current to the input current—was measured using single collector and multiple collector setups. The different setups are illustrated in Figure 5.3.

The voltage V_{CE} was not generated by a dedicated power supply but was the result of V_{Inj} and V_{Sen} respectively. It is governed by

$$\begin{aligned} V_{CE,x} - V_{Inj} - V_{Sen,x} &= 0 \\ V_{CE,x} &= V_{Inj} + V_{Sen,x}. \end{aligned} \tag{5.2}$$

The x in the index denotes that V_{Sen} can be different for each sensor node x and $V_{CE,x}$ has to be calculated separately for the multiple collector setup. During the single collector measurements only one epitaxial sensor pocket was connected and all other nodes were kept floating.

In the single collector setup the injector current is equivalent to the transistor's emitter current I_E and the sensor current is equivalent to the collector current I_C. However, the base current I_B is split into several smaller currents by the trench network. During the measurements, only the overall base current I_B can be determined either by direct

measurement of the ground network or by solving

$$I_B = I_C - I_E. \tag{5.3}$$

Gaining access to the smaller currents flowing through the trench network is inexpedient and was not pursued. Concerning the multiple collector setup, each collector current $I_{Sen,x}$ was measured by a dedicated Ammeter as discussed in Chapter 4.3.

Regarding the TCAD simulation, the situation is quite different. Every electrode in the setup has specific bias conditions and the current at each electrode is determined. To obtain the total current of the base and collector of the parasitic transistor every electrode needs to be taken into account. This is achieved summing up all the currents of the base and collector electrodes as shown in the following equations.

$$\begin{aligned} I_B &= \sum I_{sub,y} \\ I_C &= \sum I_{Sen,x} \\ I_E &= I_{Inj} \end{aligned} \tag{5.4}$$

The y in the index refers to the current of the base electrodes and the x refers to the collector electrodes. Only the emitter current I_E is directly related to the injectors current I_{Inj}.

The circuit simulation model is focusing purely on the relationship between the injector current I_{Inj} (or I_E) and the sensor current $I_{Sen,x}$ (or $I_{C,x}$). The information about the substrate current I_{sub} (or I_B) is not determined by the model itself but has to be calculated in the simulation environment by solving Equation (5.3). Every sensor node that has to be simulated is represented by an individual injector-sensor pair in the simulation setup.

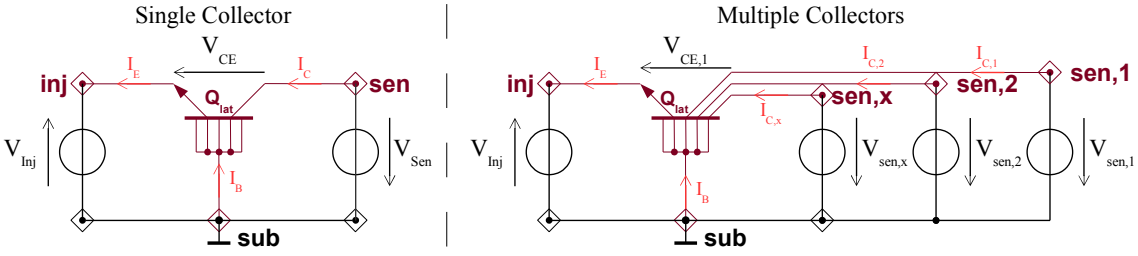


Figure 5.3: The parasitic bipolar transistor in common base configuration

5.2.1 Output Characteristics

The results shown in Figure 5.4 are based on a hypothetical scenario which usually does not occur in a productive IC but was very important regarding the calibration of the TCAD and the circuit simulation. The injector pocket was connected to the - terminal of the power supply and all the substrate contacts were connected to the + terminal. All epitaxial pockets were kept floating except for a single connection which represents the collector of the bipolar transistor and $I_C = I_{Sen}$. The transistor practically never reaches

saturation mode because $V_C > 0\ V$ and therefore $V_{CB} >= 0\ V$. Saturation mode only occurs when carriers are injected into the base region from both sides, the emitter and the collector. Regarding the parasitic bipolar transistor, this situation has been neglected because it is not relevant to the design analysis.

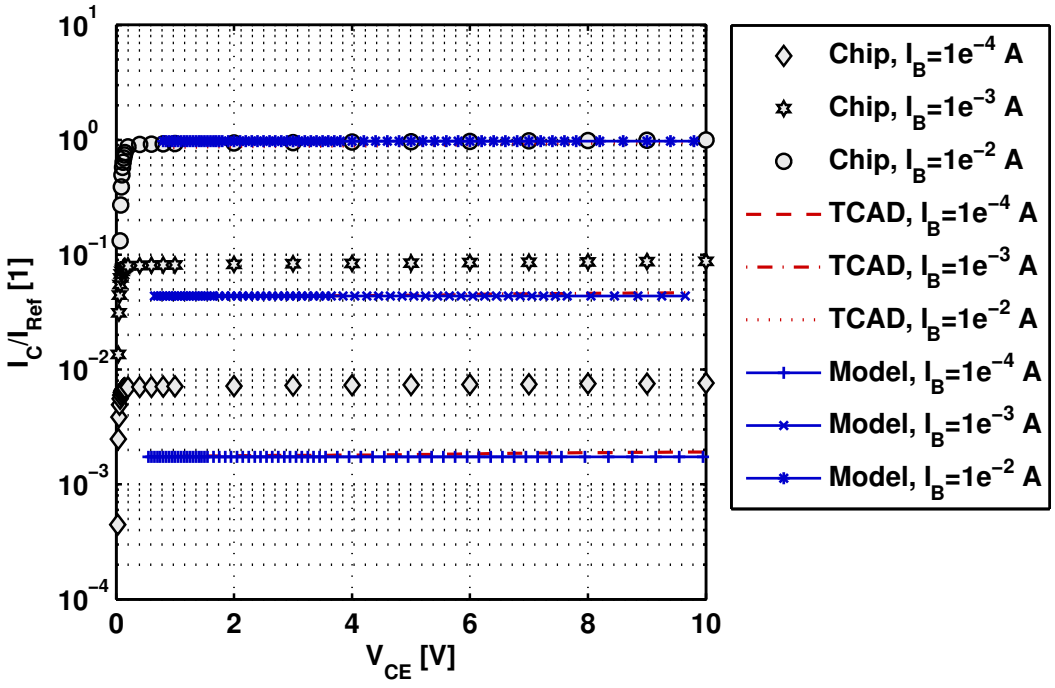


Figure 5.4: Output characteristic of the parasitic bipolar transistor

For small base currents I_B the TCAD simulation setup overestimates the recombination rate in the substrate which leads to a significantly lower collector current I_C compared to the measurement results. The relative error given by Equation (5.1) between the measurement and the simulation is $\delta_I \approx -0.8$ for a base current of 100 μA. However, with increasing base current the deviation decreases to $\delta_I \approx 0.1$. These deviations are acceptable because this setup was only used as an intermediary step in the model calibration. It has only minor relevance to parasitic analyses of product ICs since these conditions never occur during normal operation. The simulations are based on the calibration setup discussed in Chapter 3 and it cannot be used to accurately determine the parasitic coupling effect for singularly connected epitaxial sensor pockets. This output characteristic of a single parasitic bipolar transistor exemplifies the limitations of this approach.

The circuit simulation model does not include the influence of the base–width modulation because according to the measurements, the *Early effect* does not have such a huge impact on the sensor current. This was also confirmed by TCAD simulation as shown in Figure 5.4. At collector voltages $V_C = 12\ V$, the space charge region only extents $\approx 3\ \mu m$ into the base region of the parasitic bipolar transistor. However, the effective width of the base region cannot be determined so easily since the entire substrate of the chip is practically the base region. Additionally, the value of V_E is not available to the

sensor model during circuit simulations and therefore V_{CE} could only be approximated by $V_C \approx V_{CE}$. Finally, the curve fitting functions of model were designed to fit to $V_C = 5\ V$.

5.2.2 Current Characteristics

The most important characteristic of this parasitic effect is how much sensor current I_{Sen} is caused by an injector current I_{Inj}. In terms of an *npn* bipolar transistor in common base configuration, the relation between I_C and I_E is referred to as *common base current gain* [31]

$$\alpha_0 \equiv \frac{I_{Cn}}{I_E}, \tag{5.5}$$

where I_E is the emitter current and I_{Cn} is the electron current of the collector. In Figure 5.5, I_{Cn} is approximated by I_C because the collector hole current $I_{Cp} \ll I_{Cn}$.

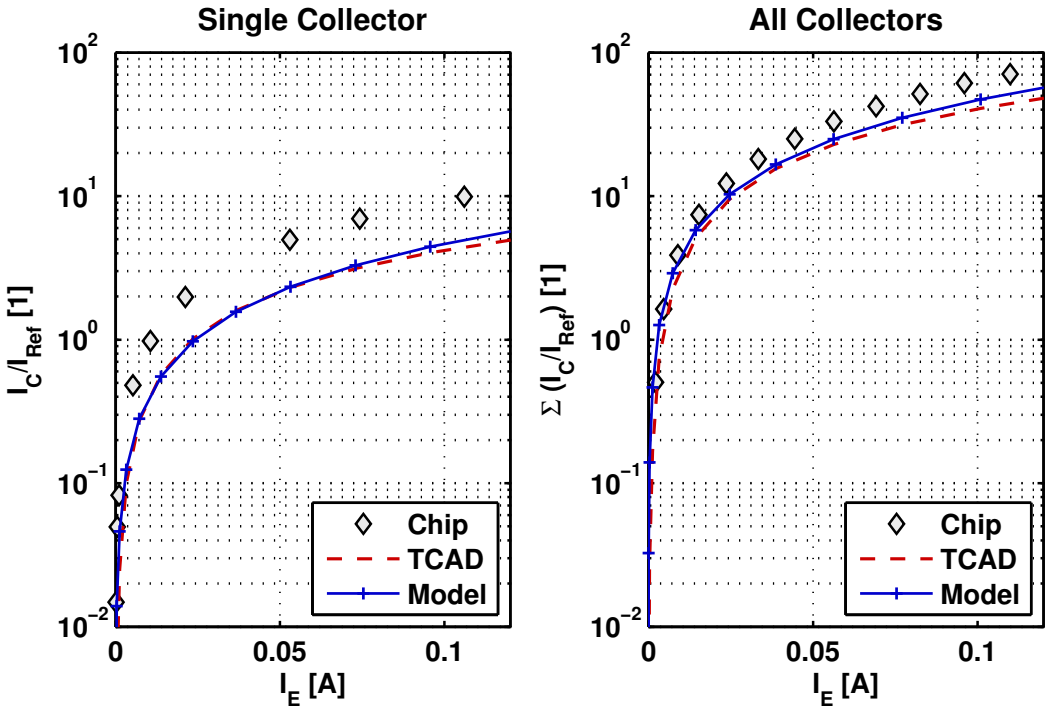


Figure 5.5: I_C–I_E characteristic of the parasitic bipolar transistor

On the left hand side of Figure 5.5 the parasitic bipolar transistor had only a single collector connected to an Ammeter and all other collector nodes were kept floating. Similar to the results discussed in Chapter 5.2.1, the results show that most of the injected electrons recombine in the substrate and only a small portion diffuses to the adjacent epitaxial well. The current is focused in a small region around the emitter well, the collector well and the substrate contacts in close proximity to the emitter and collector. In this region the TCAD simulation overestimates the recombination rate resulting in a

relative error of the collector current $\delta_I \approx -0.6$. Such a large diviation is only acceptable since this situation does not occur on product ICs.

The second part of Figure 5.5 shows the results when all collectors are connected to the ground potential. This reflects the actual situation on product ICs. At 100 mA injection current, approximately 40 % of the current diffuses to the collector nodes while 60 % are provided to the base as hole current that recombines with the injected electrons in the substrate of the chip. Also for this comparison the TCAD simulation shows a relative error of $\delta_I \approx -0.58$ while $\delta_I \approx -0.29$ of the circuit model. The circuit simulation setup contained a dedicated model for each sensor node on the test chip and a model for every cluster of epitaxial pockets. This lead to approximately 100 Verilog-AMS models for the circuit simulation. While the results of the smaller sensor pockets are in good agreement with the measurements, the combined epitaxial pockets showed some deviations. The reason is that the geometric center of the combined pockets was used to calculate the distance from the injector and the area parameter was the sum of all areas of each individual pocket in the cluster. However, for a full chip assessment involving approximately 100 Verilog-AMS models the accuracy of the results is high. This means even a full chip analysis provides accurate results for the parasitic coupling effect.

5.3 Spatial Decay Characteristic

The spatial decay characteristic is another representation of the transistor's common base current gain. Similar to Figure 5.5, the relationship between I_E and I_C is of interest. However, in Figure 5.6 the distance between the edge of the injector and the center of the sensor pocket is used as x–axis. It provides important information to the design community about how much current is collected by a sensitive node at a certain distance from the injector ($\alpha_0 = f\,(I_{Inj}, d)$).

The measurement results shown in Figure 5.6 were performed on two different test chips using the injector on the left hand side of the test chip and at the center. The sensor array for the measurements was always the one located between the left and the center injector (see Figure 4.1 for details). The minimum distance between the injectors and the sensor array differs slightly which can be seen at the different starting positions of the curves labeled *Chip 1,* $I_{Inj} = 100\ mA$ and *Chip 2,* $I_{Inj} = 100\ mA$.

The relative error between the model and the measurement at $I_{Inj} = 100\ mA$ is between 1 % and 65 %. This large deviation originates from the influence of the resistive network of the substrate. The measurement result of *Chip 1* at 100 mA shows two depressions (at $\approx 150\ \mu m$ and $\approx 450\ \mu m$) deviating from an ideal exponential decay. In the vicinity of these depressions, the resistance of the substrate connection was higher than close to the injectors (at $d = 0\ \mu m$ and $d = 670\ \mu m$). Additionally, there was a low ohmic connection to the substrate located at $d \approx 300\ \mu m$. Regarding the measurement labeled as *Chip 2,* $I_{Inj} = 100\ mA$, the ground network was optimized to compensate for the higher resistance and the result is very close to an ideal exponential decay. This compensation was achieved by adding additional series resistances to the connections with lower resistance values to get a homogeneously distributed resistive ground network.

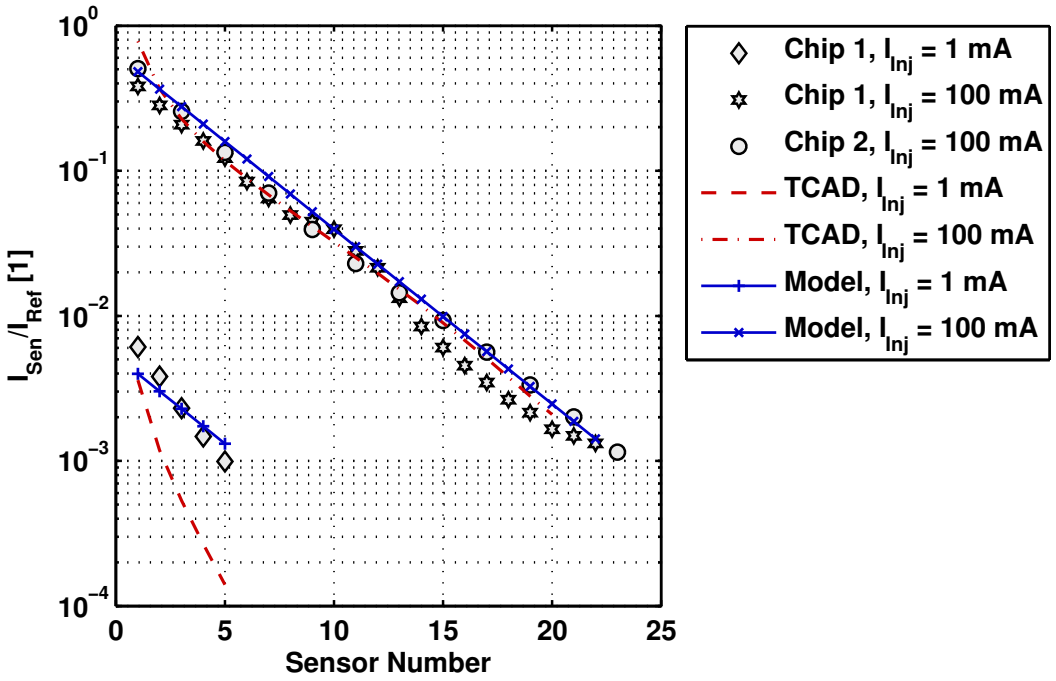


Figure 5.6: Spatial decay characteristic

The quality of the circuit simulation model can be better expressed by calculating the square of the correlation coefficient r^2 [119] of the spatial decay characteristic. It can be calculated by solving

$$r^2 \equiv \frac{SSR}{SSR + SSE}, \tag{5.6}$$

where SSR is the sum of squared residuals

$$SSR \equiv \sum_i^n (\hat{y}_i - \overline{y})^2 \tag{5.7}$$

and SSE is the sum of squared errors

$$SSE \equiv \sum_i^n (y_i - \hat{y}_i)^2 . \tag{5.8}$$

y_i is the value of the n data point of the measurement results and $\hat{y}_i$ is the value provided by the circuit simulation. $\overline{y}$ is the mean value of the measurement results which is defined as

$$\overline{y} = \frac{1}{n} \sum_i^n y_i. \tag{5.9}$$

The square of the correlation coefficient r^2 of the spatial decay function at an injection level of $I_{Inj} = 100\ mA$ is ≈ 0.93 and a value of 1 is a perfect match between y_i and $\hat{y}_i$ for $\forall i$ [119].

Regarding the measurement with 1 mA of injector bias, the Verilog-AMS model underestimates the effect close to the injector by a factor of ≈ 1.5. However, the gradient of the decay depends on the injection current and lower currents show an increased decay rate. Therefore, the model matches after approximately 100 μm of distance from the injector and even overestimates the effect for larger distances.

The TCAD simulation is perfectly capable to calculate the parasitic effect for the sensor adjacent to the injector for low and high injection levels. However, even with the calibration of several key parameters, the electron diffusion still shows a significant mismatch in the decay gradient at low injection levels. The charge carriers do not diffuse as deeply into the substrate at low injection levels and the recombination effects at the top of the substrate are overrated. Nevertheless, the accuracy at higher injection was given priority and the TCAD setup was not calibrated for this circumstance. While the measurements show an almost ideal exponential decline of the sensor current, TCAD shows a slightly decreasing gradient of the carrier recombination rate within the first 100 μm distance of the injector.

On a product IC, several injectors may become active at the same time. While directly adjacent injectors connected by the same net can be considered as a single larger injector combining both areas, two geometrically separated injectors introduce separated electron diffusion currents. It was speculated that the current at the sensors can be determined by simply taking the sum of two independent injections. This setup was used to determine the influence of this situation and evaluate the model capability at the same time.

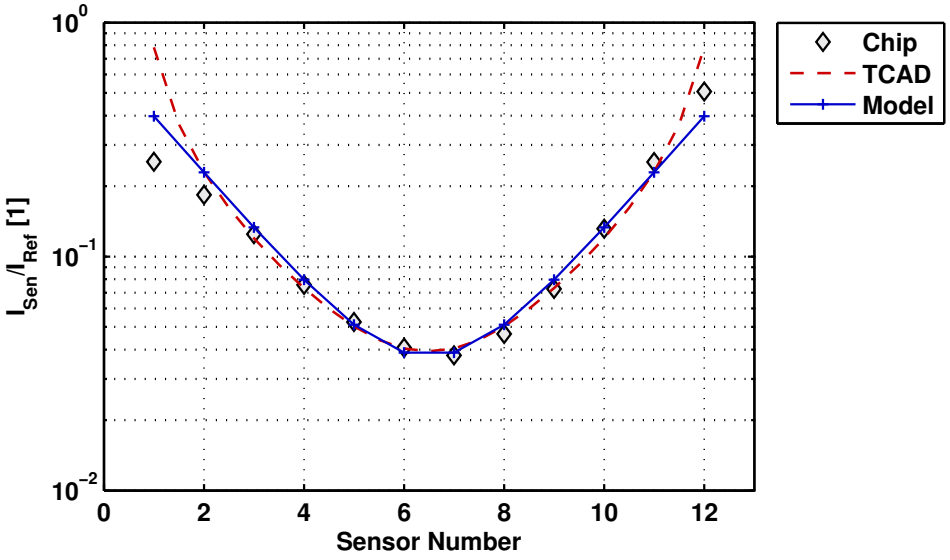


Figure 5.7: Superposition characteristic

The measurement was performed with the injector at the left side and the center of

the test chip and the sensor array was located in between (see Figure 4.6). Both power supplies were set up and the measurements were performed while switching the power supplies *on* and *off*. The results are shown as the black colored markers in Figure 5.7.

The TCAD simulation setup reflects the measurement setup and showed the same level of accuracy as for the single injector analysis. The coupling effect is overestimated in close proximity to the injector by a factor of 3 but shows good agreement to the measurement at a distance of $> 150\ \mu m$ between injector and sensor. The superposition of two simultaneous injections matches the expectation.

The circuit simulation contained two sensor models per sensor node and each node was connected to the ground network by a small series resistance to prevent a short-circuit. The current source of each model forced their respective sensor current at each node causing the total sum to represent the superposition of two simultaneously occurring injections. The deviation between measurement and circuit simulation close to the injectors can again be explained by the missing information about the local substrate potential in the Verilog-AMS model. However, the accuracy of the results is satisfactory and the results can be used for circuit design.

5.4 Electric Field in the Substrate

The measurements and simulations of the electric field influence and the active guard structure were performed on the second test chip (see Figure A.2) that was developed during the course of this thesis. It was chosen for its increased performance of the active guard structure. The results are more distinct in comparison to the test chip shown in Figure A.1. The technological reason for this is the higher resistance of the deep trench structure in the second test chip. This simplifies the introduction of electric fields in the substrate. Considering equal distances between the substrate contacts of the guard structure and the contacts connected to the ground network, the same electric potential requires less driving current capability due to the increased load resistance. However, the substrate itself has similar properties and the electron diffusion only shows minor differences between both technologies.

Figure 5.8 shows the simulation and measurement results of the measurement setup discussed in Chapter 4.4.4. The externally applied voltage V_{ext} at each side of the injector has two major effects. Firstly, the diode forward voltage V_D differs between the two sides which—in turn—causes an inhomogeneous current injection. At $V_D = 0.9\ V$, I_D is $\approx 50\ mA$ and at $V_D = 1.1\ V$ the injector diode causes $\approx 140\ mA$ (see Figure 5.1). However, during the measurement the total injected current was held constantly at $100\ mA$.

The second effect is caused by the electric field which is created between the two substrate connections by the externally applied substrate bias voltage. A simplified estimation shown in Equation (5.10) is an indicator for the influence of the electric field. The TCAD simulation of the injector diode was used to provide some values concerning

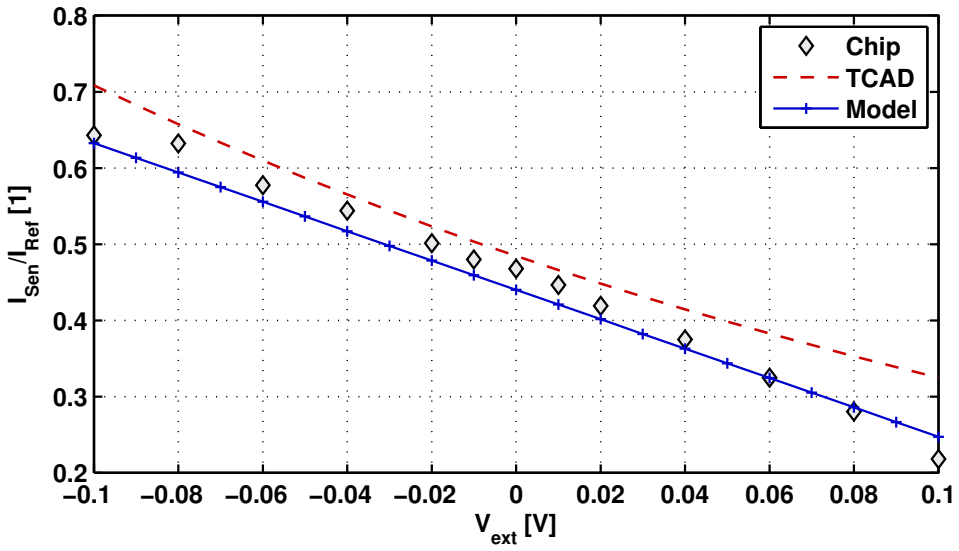


Figure 5.8: External substrate bias

the carrier density and the electric potential underneath the epitaxial pocket.

$$\begin{aligned}
\vec{J}_n &= q \cdot \mu_n \cdot n \cdot \vec{E} + q \cdot D_n \cdot \nabla n \\
\vec{J}_{n,Drift} &= 1.602 \cdot 10^{-19}\ C \cdot 458\ \tfrac{cm^2}{Vs} \cdot 6.0 \cdot 10^{16}\ cm^{-3} \cdot -6.4\ \tfrac{V}{cm} \\
\vec{J}_{n,Diff} &= 1.602 \cdot 10^{-19}\ C \cdot 11.83\ \tfrac{cm^2}{s} \cdot 2.64 \cdot 10^{18}\, \tfrac{cm^{-3}}{cm} \\
\vec{J}_n &= -28.18\ \tfrac{A}{cm^2} + 5.00\ \tfrac{A}{cm^2} \\
\vec{J}_n &= -23.18\ \tfrac{A}{cm^2}
\end{aligned} \tag{5.10}$$

The diffusion component $\vec{J}_{n,Diff}$ was calculated by determining the electron densities n at the corner of the deep trench structure beneath the epitaxial pocket at $V_D = 0.9\ V$ and $1.1\ V$. Additionally, the electric potentials were determined by applying a $200\ mV$ offset to the deep trench structures on the left and the right side of the injector. This leads to the solution for the drift component $\vec{J}_{n,Drift}$. The results show that the electron current caused by the gradient of the carrier density is lower than the current introduced by the externally applied electric field.

The TCAD simulation result in Figure 5.8 shows a similar gradient regarding the influence of the electric field. However, there is a slight curvature in the TCAD simulation result but it is not caused by the electric field. The root cause for this deviation from a linear relationship is the reduction of the injected current at different biasing voltages V_{ext}. At first V_{Inj} is ramped up until I_{Inj} reaches its target value and then V_{ext} is applied to the substrate contacts. This introduces a shift of $\approx 7\ \%$ in I_{Inj}. Nevertheless, the TCAD simulation results show acceptable accuracy and can be used for analysis of externally applied bias voltages to the substrate. The result of the Verilog-AMS model is even closer to the measurement result provided the information about the nearest substrate contact

connected to ground is available to the model. This enables the designer to estimate protection structures which use this principle in their operation.

5.5 Active Protection Structure

As already mentioned in the previous chapter, the active protection structure was also measured on the second test chip (see Figure A.2). The measurement setup is described in detail in Chapter 4.4.5 and the results shown in Figures 5.9 and 5.10 were obtained by keeping *Guard Structure A* floating. At these conditions, any injected current I_{Inj} causes electrons to diffuse to the epitaxial pocket of the guard structure, which in turn pulls the ground connection of the guard structure below ground. The higher the injected current, the larger is the observed effect. This can be seen by comparing the sensor current suppression of Figure 5.9 to 5.10.

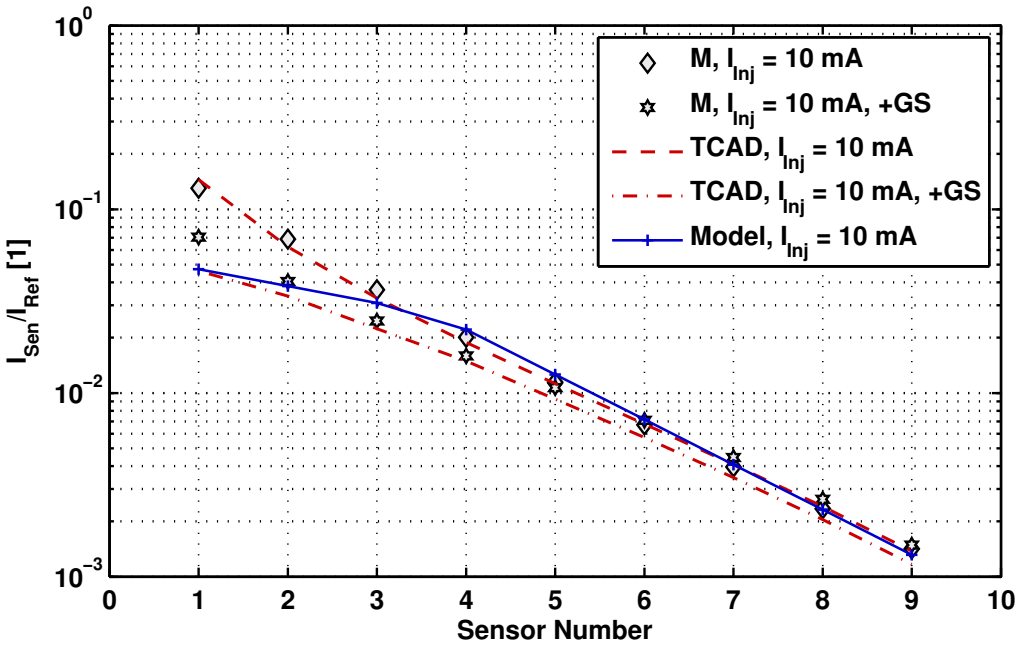


Figure 5.9: Guard structure at $I_{Inj} = 10\ mA$

In Figure 5.9 the current at the sensor closest to the injector is at 78.7 μA with a deactivated guard structure and at 43.7 μA with the structure being activated. This is equivalent to a suppression factor of ≈ 1.8. However, in Figure 5.10 the difference between the deactivated and activated guard structure is $1,430\ \mu A$ to 3.8 μA which is a factor of ≈ 375. Such a huge suppression effect cannot be explained only by the localized reduction of the injector current, instead the drift component caused by the electric field becomes the dominant factor. Additionally, the minority carriers get forced deeper into the substrate by the electric field and due to the low recombination rate, they diffuse to the sensor nodes outside of the guard structure's area of influence. This causes an

increase in the parasitic current at the remaining sensors. However, the circuit simulation model cannot account for this effect because each model is entirely on its own and does not have any information about the other Verilog-AMS models in the design. Therefore, it does not know whether an adjacent model is subjected to a suppression effect or not (see Chapter 4.4.5 for details).

At low injection rates (Figure 5.9), the circuit simulation model overestimates the suppression effect by a factor of 2 in close proximity to the injector. The suppression level is overrated because the charge carrier densities provided by the TCAD simulation are slightly too low. This difference can also be seen in the sensor currents in close proximity to the injector shown in Figure 5.6. The 1 mA TCAD result is by a factor of ≈ 2 lower than the measurements and by a factor of ≈ 2 higher for the 100 mA injection. This mismatch in the injection ratio causes the shift in the suppression model. However, the trend of the protection structure is represented nicely and for low injection levels the accuracy is acceptable.

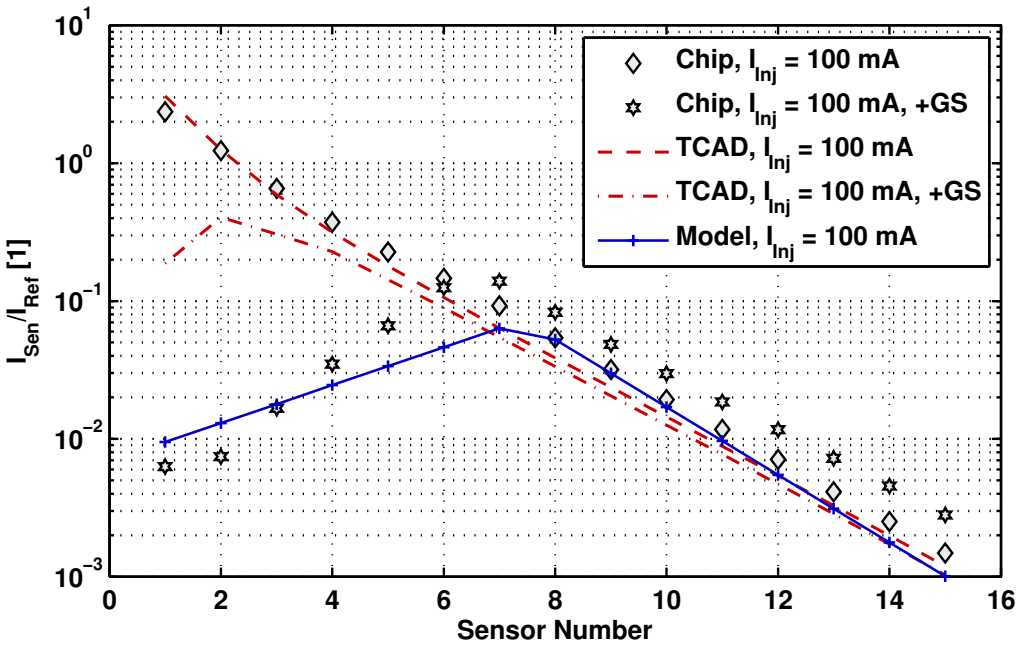


Figure 5.10: Guard structure at $I_{Inj} = 100\ mA$

At high injection rates (Figure 5.10), the suppression effect become more prominent and TCAD shows a deviation by a factor of ≈ 15 at the nearest sensor node. This mismatch is mainly caused by the limitations of reducing a $3D$ structure into a large $2D$ TCAD simulation. At such a high injection level the resistive balancing of the n–doped victim pocket and the p–doped deep trench becomes dominant. The magnitude of the electric field in the substrate is underestimated because the influence of the adjacent substrate contacts is too large. The Verilog-AMS model, however, estimates the suppression effect of the guard structure quite nicely. In this case, the curve fitting functions of the carrier densities inside the Verilog-AMS model were adapted to fit to the measurements

instead of to the TCAD simulation. With this adaptation, it does not match to the exact values. Nevertheless, the area of the effect is properly represented and the accuracy of the suppression level for the individual sensors is satisfactory.

Chapter 6

Conclusion and Outlook

In the course of this thesis the parasitic coupling effect caused by minority carrier injection into the common substrate of a chip was analyzed. A circuit simulation framework was developed that enables a quantitative assessment of the impact on a circuit. Its central element is a Verilog-AMS model which utilizes several curve fitting functions to estimate the coupling path between a single injector and a single sensor node representing the parasitic *npn* transistor's emitter and collector, respectively. The internal components of the behavioral model reflect the three main parts of the coupling path—the injector diode, the sensor diode, and the intermediary substrate region. The curve fitting functions describe the path starting at the injector diode, translating the injected current into carrier densities and the electric potential of the substrate located directly underneath the injector. This part is followed by the spatial propagation of the charge carriers through the substrate all the way to the reverse biased *pn* junction of the sensor. At this point, the current at the susceptible terminal of the sensor device is calculated by the Verilog-AMS model. This current is caused by minority carriers that diffuse into the space charge region of the sensor. This effect does not only affect devices in close proximity to each other but spreads throughout an entire IC. The Verilog-AMS model only covers the effect between an individual injector and a single sensor essentially representing a point–to–point modeling scheme. However, when the model is applied with an automated extraction approach, the connections between all possible injectors and sensors on a chip can be determined.

The curve fitting functions of the Verilog-AMS model utilize the charge carrier densities and the distribution of the electric potential provided by calibrated TCAD simulations, which in turn are based on measurements performed on two dedicated test chips. This approach was chosen because the underlying physical behavior of this parasitic effect is not directly accessible by means of measurement. TCAD simulations provide the necessary insight about the semiconductor physics that govern this effect. Additionally, there are limitations to the amount of layout structures that can be placed on a test chip and TCAD provides an easy way for analysis of different designs.

An automated extraction and back-annotation methodology forms the backbone of the simulation framework. Instead of using a purely layout-based extraction approach, the proposed methodology uses network tracing to follow critical electrical paths through the design hierarchy and identifies injectors and sensors not only based on their technological

features but also by their connection inside the design. Based on this information, an enhanced simulation netlist is generated which contains all critical coupling paths between the injectors and sensors. This significantly reduces the risk of missing susceptible nodes in the design. In addition, it reduces the amount of parasitic devices in the simulation netlist.

Finally, the proposed methodology is verified by comparing the circuit and TCAD simulation results to the measurement results. The two dedicated test chips were designed to be similar to a productive IC while providing access to all the relevant layout structures for measurements. The test chips contain numerous sensors, several large injectors and some selected layout–based protection structures. The automated extraction and back-annotation setup was applied to the test chip's layout. After the extraction run the circuit simulation was performed utilizing the Verilog-AMS model. The overall accuracy regarding all key characteristics satisfies the expectations. The new methodology provides valuable risk assessment for the circuit designer about this parasitic effect. For the first time also an active protection structures can be quantified during circuit simulation.

The research of minority carrier injection into the common substrate of an IC is not concluded yet. In the past years several efforts were made to provide circuit simulation capabilities to the design community. However, there are still many possibilities to optimize the design of guard structures and to quantify the effectivness of these structures directly during the design phase. Additionally, the technological options to influence the behavior of the minority carriers are still an open topic especially with regard to new emerging technologies.

Bibliography

[1] B. Murari, F. Bertotti, and G. Vignola, *Smart Power ICs: Technologies and Applications*. Advanced Microelectronics, Springer-Verlag, 2002. http://www.springer.com/us/book/9783540432388.

[2] International Organization for Standardization, "Road Vehicles – Functional Safety – Part 5: Product Development at the Hardware Level," ISO 26262-5:2011, Geneva, Switzerland, November 2011. http://www.iso.org/iso/catalogue_detail?csnumber=43464.

[3] Infineon Technologies AG, "Automotive Power Selection Guide," October 2014. http://www.infineon.com/automotivepower.

[4] G. Moore, "Cramming More Components onto Integrated Circuits," *Electronics*, Vol. 38, pp. 114–117, April 1965.

[5] R. J. Widlar, "Controlling Substrate Currents in Junction-Isolated ICs," *IEEE Journal of Solid-State Circuits*, Vol. 26, pp. 1090–1097, August 1991.

[6] W. Horn and H. Zitta, "A Robust Smart Power Bandgap Reference Circuit for Use in an Automotive Environment," *IEEE Journal of Solid-State Circuits*, Vol. 37, pp. 949–952, July 2002.

[7] M. Schenkel, *Substrate Current Effects in Smart Power ICs*. PhD thesis, ETH Zürich, 2003. http://e-collection.library.ethz.ch/eserv/eth:26285/eth-26285-02.pdf.

[8] R. Gallager, "Single Chip Carries Three Technologies," *Electronics Week*, p. 28, December 1984.

[9] S. Krishna, J. Kuo, and I. Gaeta, "An Analog Technology Integrates Bipolar, CMOS, and High-Voltage DMOS Transistors," *IEEE Transactions on Electron Devices*, Vol. 31, pp. 89–95, January 1984.

[10] M. Adler, K. Owyang, B. Baliga, and R. Kokosa, "The Evolution of Power Device Technology," *IEEE Transactions on Electron Devices*, Vol. 31, pp. 1570–1591, November 1984.

[11] C. Cini, C. Contiero, C. Diazzi, P. Galbiati, and D. Rossi, "A New Bipolar, CMOS, DMOS Mixed Technology for Intelligent Power Applications," in *15th European Solid–State Device Research Conference, ESSDERC 1985, Aachen, Germany*, September 1985.

[12] D. Hilbiber, "A New Semiconductor Voltage Standard," in *Solid-State Circuits Conference. Digest of Technical Papers. 1964 IEEE International*, Vol. VII, pp. 32–33, February 1964.

[13] R. J. Widlar, "New Developments in IC Voltage Regulators," *IEEE Journal of Solid-State Circuits*, Vol. 6, pp. 2–7, February 1971.

[14] A. Andreini, C. Contiero, and P. Galbiati, "A New Integrated Silicon Gate Technology Combining Bipolar Linear, CMOS Logic, and DMOS Power Parts," *IEEE Transactions on Electron Devices*, Vol. 33, pp. 2025–2030, December 1986.

[15] J. D. Plummer, "Monolithic MOS High Voltage Integrated Circuits," in *Electron Devices Meeting, 1980 International*, Vol. 26, pp. 70–74, December 1980.

[16] B. Murari, C. Contiero, R. Gariboldi, S. Sueri, and A. Russo, "Smart Power Technologies Evolution," in *Industry Applications Conference, 2000. Conference Record of the 2000 IEEE*, Vol. 1, pp. 10–19, October 2000.

[17] G. S. May and S. M. Sze, *Fundamentals of Semiconductor Fabrication*. John Wiley & Sons, 1^{st} ed., 2004. http://eu.wiley.com/WileyCDA/WileyTitle/productCd-0471232793.html.

[18] W. F. Davis, "Bipolar Design Considerations for the Automotive Environment," *IEEE Journal of Solid-State Circuits*, Vol. 8, pp. 419–427, December 1973.

[19] D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 28, pp. 420–430, April 1993.

[20] J. Briaire and S. Krisch, "Principles of Substrate Crosstalk Generation in CMOS Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 19, pp. 645–653, June 2000.

[21] A. J. van Genderen and N. P. van der Meijs, "Modeling Substrate Coupling Effects using a Layout-to-Circuit Extraction Program," in *ProRISC IEEE 8th Annual Workshop on Circuits, Systems and Signal Processing*, pp. 193–200, November 1997.

[22] E. Chiprout, "Interconnect and Substrate Modeling and Analysis: An Overview," *IEEE Journal of Solid-State Circuits*, Vol. 33, pp. 1445–1452, September 1998.

[23] R. Singh, "A Review of Substrate Coupling Issues and Modeling Strategies," in *Custom Integrated Circuits, 1999. Proceedings of the IEEE 1999*, pp. 491–499, May 1999.

[24] J. M. Casalta, X. Aragones, and A. Rubio, "Substrate Coupling Evaluation in BiCMOS Technology," *IEEE Journal of Solid-State Circuits*, Vol. 32, pp. 598–603, April 1997.

[25] F. Martorell, D. Mateo, and X. Aragones, "Modeling and Evaluation of Substrate Noise Induced by Interconnects," in *Design, Automation and Test in Europe Conference and Exhibition, 2003*, pp. 524–529, March 2003.

[26] International Organization for Standardization, "Road Vehicles – Electrical Disturbances from Conduction and Coupling – Part 2: Electrical Transient Conduction Along Supply Lines Only," iso 7637-2:2011, Geneva, Switzerland, March 2011. http://www.iso.org/iso/catalogue_detail?csnumber=50925.

[27] E. N. Stefanov, G. Charitat, N. Nolhier, and P. Rössel, "Transient Behaviour of Isolation Architectures in Smart Power Integrated Circuits," in *European Conference on Power Electronics '97, Trondheim*, pp. 3.036–3.041, March 1997.

[28] D. Lide, *CRC Handbook of Chemistry and Physics*. CRC Press, Internet Version ed., 2015. http://hbcponline.com.

[29] M. G. Burzo, P. L. Komarov, and P. E. Raad, "Thermal Transport Properties of Gold-Covered Thin-Film Silicon Dioxide," *IEEE Transactions on Components and Packaging Technologies*, Vol. 26, pp. 80–88, March 2003.

[30] A. Delan, M. Rennau, S. Schulz, and T. Gessner, "Thermal Conductivity of Ultra Low-k Dielectrics," *Microelectronic Engineering*, Vol. 70, pp. 280–284, November 2003.

[31] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. John Wiley & Sons, 3rd ed., 2006.

[32] J. Dziewior and W. Schmid, "Auger Coefficients for Highly Doped and Highly Excited Silicon," *Applied Physics Letters*, Vol. 31, pp. 346–348, August 1977.

[33] M. E. Law, E. Solley, M. Liang, and D. E. Burk, "Self-Consistent Model of Minority-Carrier Lifetime, Diffusion Length, and Mobility," *IEEE Electron Device Letters*, Vol. 12, pp. 401–403, August 1991.

[34] D. M. Caughey and R. E. Thomas, "Carrier Mobilities in Silicon Empirically Related to Doping and Field," *Proceedings of the IEEE*, Vol. 55, pp. 2192–2193, December 1967.

[35] X. Aragones and A. Rubio, "Experimental Comparison of Substrate Noise Coupling using Different Wafer Types," *IEEE Journal of Solid-State Circuits*, Vol. 34, pp. 1405–1409, October 1999.

[36] W. Werner, "Integrierte Treiberschaltungsanordnung für ein induktives Lastelement." European Patent Office, EP 0 676 808 B1, issued 11^{th}, March 1998.

https://data.epo.org/publication-server/rest/v1.0/publication-dates/19960605/patents/EP0616189NWB1/document.pdf.

[37] J. E. A. Maurits, H. J. Dawson, and C. H. Weaver, "The Effect of Polysilicon Impurities on Minority Carrier Lifetime in Cz Silicon Crystals," in *Photovoltaic Specialists Conference, 1991., Conference Record of the Twenty Second IEEE*, Vol. 1, pp. 309–314, October 1991.

[38] X. J. Meng, Z. Q. Ma, P. Lv, Z. S. Yu, and F. Li, "Affirmation of Minority Carrier Lifetime during Industrial Process of Crystalline Silicon Solar Cell by Microwave Phtonconductance Decay Method," in *2009 16th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits*, pp. 511–514, July 2009.

[39] Mixed Signal Design Cluster, ed., *Proceedings on the Workshop on Substrate Effects in Smart–Power ICs*, 31st European Solid–State Device Research Conference ESSDERC, Nuremberg, 2001.

[40] C. Lochot, J. Lainé, M. Bafleur, A. Cazarré, and J. Tasselli, "Potentialities of Substrate-Thinning Technique to Control Minority Carrier Injection in Smart Power IC's," *Microelectronics Journal*, Vol. 37, pp. 804–811, August 2006. http://www.sciencedirect.com/science/article/pii/S0026269205003836.

[41] K. Sakamoto, Y. Nunogawa, K. Satonaka, T. Kouda, and S. Horiuchi, "An Intelligent Power IC with Reverse Battery Protection for Fast-Switching High-Side Solenoid Drive," *IEEE Transactions on Electron Devices*, Vol. 46, pp. 1775–1781, August 1999.

[42] K. Sakamoto, N. Fuchigami, K. Takagawa, and S. Ohtaka, "A Three-Terminal Intelligent Power MOSFET with Built-In Reverse Battery Protection for Automotive Applications," *IEEE Transactions on Electron Devices*, Vol. 46, pp. 2228–2234, November 1999.

[43] M. Feldtkeller and J. Tihanyi, "Schaltungsanordnung zur Verhinderung der Injektion von Minoritätsträgern in das Substrat." Deutsches Patentamt DE 199 28 762 C1, issued 23^{rd}, November 2000.

[44] M. Kollmitzer and W. Horn, "Halbleiterbauelementeanordnung und Verfahren zu deren Betrieb." Deutsches Patentamt DE 102 55 862 B3, issued 17^{th}, June 2004.

[45] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. John Wiley & Sons, 1997.

[46] W. M. C. Sansen, *Analog Design Essentials*. Springer-Verlag, 2008.

[47] W. Horn, "Schaltungsanordnung zur Konstantspannungs- und/oder Konstantstromerzeugung." Deutsches Patentamt, DE 100 06 950 C1, issued 24^{th}, January 2002.

[48] V. Parthasarathy, V. Khemka, R. Zhu, I. Puchades, T. Roggenbauer, M. Butner, P. Hui, P. Rodriquez, and A. Bose, "A Multi Trench Analog+Logic Protection (M–TRAP) for Substrate Crosstalk Prevention in a 0.25 μm Smart Power Platform with 100 V High–side Capability," in *Power Semiconductor Devices and ICs, 2004. Proceedings. ISPSD '04. The 16th International Symposium on*, pp. 427–430, May 2004.

[49] C.-Y. Huang and M.-J. Chen, "Design Model and Guidelines for n-Well Guard Ring in Epitaxial CMOS," *IEEE Transactions on Electron Devices*, Vol. 41, pp. 1806–1810, October 1994.

[50] V. Venkatesan, Q. Nguyen, A. Bose, and P. Parris, "DC Substrate Coupling between LDMOS and CMOS Devices in Hyperintegration I Technology," in *Bipolar/BiCMOS Circuits and Technology Meeting, 1998. Proceedings of the 1998*, pp. 57–60, September 1998.

[51] O. Gonnard, G. Charitat, P. Lance, E. Stefanov, M. Suquet, M. Bafleur, N. Mauran, and A. Peyre-Lavigne, "Substrate Current Protection in Smart Power IC's," in *Power Semiconductor Devices and ICs, 2000. Proceedings. The 12th International Symposium on*, pp. 169–172, May 2000.

[52] W. W. T. Chan, J. K. O. Sin, and S. S. Wong, "A Novel Crosstalk Isolation Structure for Bulk CMOS Power IC's," *IEEE Transactions on Electron Devices*, Vol. 45, pp. 1580–1586, July 1998.

[53] O. Gonnard, G. Charitat, P. Lance, M. Suquet, M. Bafleur, J. P. Laine, and A. Peyre-Lavigne, "Multi-ring Active Analogic Protection for Minority Carrier Injection Suppression in Smart Power Technology," in *Power Semiconductor Devices and ICs, 2001. ISPSD '01. Proceedings of the 13th International Symposium on*, pp. 351–354, June 2001.

[54] S. Gupta, J. C. Beckman, and S. L. Kosier, "Improved Latch-Up Immunity in Junction-Isolated Smart Power ICs with Unbiased Guard Ring," *IEEE Electron Device Letters*, Vol. 22, pp. 600–602, December 2001.

[55] V. Khemka, V. Parthasarathy, R. Zhu, A. Bose, and T. Roggenbauer, "Trade-Off Between High-Side Capability and Substrate Minority Carrier Injection in Deep Sub-Micron Smart Power Technologies," in *Power Semiconductor Devices and ICs, 2003. Proceedings. ISPSD '03. 2003 IEEE 15th International Symposium on*, pp. 241–244, April 2003.

[56] M. Feldtkeller, "Integrierte Schaltungsanordnung zur Vermeidung von Minoritätsträgerinjektion." Deutsches Patentamt DE 42 09 523 C1, issued 11^{th} March 1993, March 1993.

[57] R. Peppiette, "A New Protection Technique for Ground Recirculation Parasitics in Monolithic Power ICs," *Sanken Technical Report*, Vol. 26, pp. 91–97, November 1994.

[58] R. Peppiette, R. Cooper, and R. Stoddard, "Epitaxial Island with Adjacent Asymmetrical Structure to Reduce Collection of Injected Current from the Island into other Islands." US Patent US 5514901 A, issued 7^{th} May 1994, May 1994.

[59] J. P. Laine, O. Gonnard, G. Charitat, L. Bertolini, and A. Peyre-Lavigne, "Active Pull-Down Protection for Full Substrate Current Isolation in Smart Power IC's," in *Power Semiconductor Devices and ICs, 2002. Proceedings of the 14th International Symposium on*, pp. 273–276, June 2002.

[60] X. Aragones, F. Moll, M. Roca, and A. Rubio, "Analysis and Modelling of Parasitic Substrate Coupling in CMOS Circuits," *IEEE Proceedings - Circuits, Devices and Systems*, Vol. 142, pp. 307–312, October 1995.

[61] K. Joardar, "Substrate Crosstalk in BiCMOS Mixed Mode Integrated Circuits," *Solid-State Electronics*, Vol. 39, pp. 511–516, April 1996.

[62] N. Verghese, D. J. Allstot, and S. Masui, "Rapid Simulation of Substrate Coupling Effects in Mixed-Mode ICs," in *Custom Integrated Circuits Conference, 1993., Proceedings of the IEEE 1993*, pp. 18.3.1–18.3.4, May 1993.

[63] F. J. R. Clement, E. Zysman, M. Kayal, and M. Declercq, "LAYIN: Toward a Global Solution for Parasitic Coupling Modeling and Visualization," in *Custom Integrated Circuits Conference, 1994., Proceedings of the IEEE 1994*, pp. 537–540, May 1994.

[64] T. Blalack, J. Lau, F. J. R. Clement, and B. A. Wooley, "Experimental Results and Modeling of Noise Coupling in a Lightly Doped Substrate," in *Electron Devices Meeting, 1996. IEDM '96., International*, pp. 623–626, December 1996.

[65] M. van Heijningen, M. Badaroglu, S. Donnay, M. Engels, and I. Bolsens, "High-Level Simulation of Substrate Noise Generation Including Power Supply Noise Coupling," in *Design Automation Conference, 2000. Proceedings 2000*, pp. 446–451, June 2000.

[66] M. Pfost and H. M. Rein, "Modeling and Measurement of Substrate Coupling in Si-Bipolar IC's up to 40 GHz," *IEEE Journal of Solid-State Circuits*, Vol. 33, pp. 582–591, April 1998.

[67] T. Smedes, N. P. van der Meijs, and A. J. van Genderen, "Extraction of Circuit Models for Substrate Cross-Talk," in *Computer-Aided Design, 1995. ICCAD-95. Digest of Technical Papers., 1995 IEEE/ACM International Conference on*, pp. 199–206, November 1995.

[68] N. K. Verghese and D. J. Allstot, "SUBTRACT: A Program for the Efficient Evaluation of Substrate Parasitics in Integrated Circuits," in *Computer-Aided Design, 1995. ICCAD-95. Digest of Technical Papers., 1995 IEEE/ACM International Conference on*, pp. 194–198, November 1995.

[69] R. Gharpurey and R. G. Meyer, "Modeling and Analysis of Substrate Coupling in Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 31, pp. 344–353, March 1996.

[70] A. Sharma, P. Birrer, S. K. Arunachalam, C. Xu, T. S. Fiez, and K. Mayaram, "Accurate Prediction of Substrate Parasitics in Heavily Doped CMOS Processes Using a Calibrated Boundary Element Solver," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 13, pp. 843–851, July 2005.

[71] A. J. van Genderen, N. P. van der Meijs, and T. Smedes, "Fast Computation of Substrate Resistances in Large Circuits," in *European Design and Test Conference, 1996. ED TC 96. Proceedings*, pp. 560–565, March 1996.

[72] M. Klemme and E. Barke, "Modellierung und Simulation von Substratkopplungen in bipolaren integrierten Schaltungen," *Tagungsband Mikroelektronik 97, München*, pp. 61–66, March 1997.

[73] M. Klemme and E. Barke, "An Extended Bipolar Transistor Model For Substrate Crosstalk Analysis," in *Custom Integrated Circuits, 1999. Proceedings of the IEEE 1999*, pp. 579–582, May 1999.

[74] L. Deferm, C. Claeys, and R. Mertens, "Parasitic Lateral Bipolar Transistors in CMOS," *Solid-State Electronics*, Vol. 32, pp. 103–109, February 1989.

[75] G. de Cremoux, E. Dubois, S. Bardy, and J. Lebailly, "Simulations and Measurements of Cross-Talk Phenomena in BiCMOS Technology for Hard Disk Drives," in *Electron Devices Meeting, 1996. IEDM '96., International*, pp. 481–484, December 1996.

[76] M. Schenkel, P. Pfaffli, S. Mettler, W. Reiner, and W. D. Aemmer, "Measurements and 3D Simulations of Full-Chip Potential Distribution at Parasitic Substrate Current Injection," in *Solid-State Device Research Conference, 2000. Proceeding of the 30th European*, pp. 600–603, September 2000.

[77] E. Gnani, V. Giudicissi, R. Vissarion, C. Contiero, and M. Rudan, "Automatic 2-D and 3-D Simulation of Parasitic Structures in Smart-Power Integrated Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 21, pp. 791–798, July 2002.

[78] J. Oehmen, *Modellierung lateraler parasitärer Transistoren in monolithischen Smart–Power–Schaltungen*. PhD thesis, Gottfried Wilhelm Leibniz Universität Hannover, 2006.

[79] J. Oehmen, M. Olbrich, L. Hedrich, and E. Barke, "Modeling Lateral Parasitic Transistors in Smart Power ICs," *IEEE Transactions on Device and Materials Reliability*, Vol. 6, pp. 408–420, September 2006.

[80] F. L. Conte, *Substrate Current Modeling for High Temperature Smart Power BCD Technology*. PhD thesis, École Polytechnique Fédérale de Lausanne, 2012. https://infoscience.epfl.ch/record/182630.

[81] F. L. Conte, J. M. Sallese, M. Pastre, F. Krummenacher, and M. Kayal, "Global Modeling Strategy of Parasitic Coupled Currents Induced by Minority-Carrier Propagation in Semiconductor Substrates," *IEEE Transactions on Electron Devices*, Vol. 57, pp. 263–272, January 2010.

[82] P. Buccella, C. Stefanucci, J. M. Sallese, and M. Kayal, "Spice Simulation of Substrate Minority Carriers Propagation with Equivalent Electrical Circuit," in *Mixed Design of Integrated Circuits Systems (MIXDES), 2014 Proceedings of the 21st International Conference*, pp. 347–350, June 2014.

[83] H. Zou, Y. Moursy, R. Iskander, M. M. Louërat, and J. P. Chaput, "A Novel CAD Framework for Substrate Modeling," in *Ph.D. Research in Microelectronics and Electronics (PRIME), 2014 10th Conference on*, pp. 1–4, June 2014.

[84] C. Stefanucci, P. Buccella, M. Kayal, and J. M. Sallese, "Modeling Minority Carriers Related Capacitive Effects for Transient Substrate Currents in Smart Power ICs," *IEEE Transactions on Electron Devices*, Vol. 62, pp. 1215–1222, April 2015.

[85] K. Hoffmann, *System Integration: From Transistor Design to Large Scale Integrated Circuits*. John Wiley & Sons, 2004.

[86] J.-P. Colinge and C. Colinge, *Physics of Semiconductor Devices*. Springer-Verlag, 1 ed., 2002.

[87] A. Jüngel, *Transport Equations for Semiconductors*. Lecture Notes in Physics, Springer-Verlag, 2009. https://books.google.at/books?id=COlsCQAAQBAJ.

[88] R. Sauer, *Halbleiterphysik: Lehrbuch für Physiker und Ingenieure*. Oldenbourg Wissenschaftsverlag, 2009. https://books.google.at/books?id=_pxcHH4uDz4C.

[89] Synopsys, Inc., *Sentaurus™Device Monte Carlo User Guide*, j-2014.09 ed., September 2014.

[90] W. V. Roosbroeck, "Theory of the Flow of Electrons and Holes in Germanium and Other Semiconductors," *The Bell System Technical Journal*, Vol. 29, pp. 560–607, October 1950.

[91] T.-J. K. Liu, "Lecture Notes, EE130/230A: Integrated Circuit Devices." https://inst.eecs.berkeley.edu/~ee130/sp13/lecture.html, 2013. Accessed: 2018-01-17.

[92] W. Shockley and W. T. Read, "Statistics of the Recombinations of Holes and Electrons," *Physical Review Journal*, Vol. 87, pp. 835–842, September 1952.

[93] K. F. Brennan, *The Physics of Semiconductors: With Applications to Optoelectronic Devices*. Cambridge University Press, 1999.

[94] D. Baek, S. Rouvimov, B. Kim, T.-C. Jo, and D. K. Schroder, "Surface Recombination Velocity of Silicon Wafers by Photoluminescence," *Applied Physics Letters*, Vol. 86, no. 11, 2005.

[95] S. W. Glunz, S. Rein, J. Y. Lee, and W. Warta, "Minority Carrier Lifetime Degradation in Boron-doped Czochralski Silicon," *Journal of Applied Physics*, Vol. 90, pp. 2397–2404, September 2001.

[96] S. Selberherr, *Analysis and Simulation of Semiconductor Devices*. Springer-Verlag, 1984.

[97] R. LeVeque, *Finite Difference Methods for Ordinary and Partial Differential Equations*. Society for Industrial and Applied Mathematics, 2007.

[98] H. Gummel, "A Self-Consistent Iterative Scheme for One-Dimensional Steady State Transistor Calculation," *Electron Devices, IEEE Transactions on*, Vol. 11, pp. 455–465, November 1964.

[99] D. Vasileska, "Drift-Diffusion Modeling and Numerical Implementation Details." https://nanohub.org/resources/9092, June 2010. Accessed: 2018-01-17.

[100] J. Li and Y.-T. Chen, *Computational Partial Differential Equations using Matlab*. CRC Press, 2008. https://www.crcpress.com/Computational-Partial-Differential-Equations-Using-MATLAB/Li-Chen/p/book/9781420089042.

[101] MathWorks®, "MATLAB® R2018a Product Documentation." https://uk.mathworks.com/help/index.html, 2018. Accessed: 2018-04-21.

[102] I. Bronstein, K. Semendjajew, G. Musiol, and H. Mühlig, *Taschenbuch der Mathematik*. Verlag Harri Deutsch, 1999.

[103] G. Masetti, M. Severi, and S. Solmi, "Modeling of Carrier Mobility against Carrier Concentration in Arsenic-, Phosphorus-, and Boron-doped Silicon," *IEEE Transactions on Electron Devices*, Vol. 30, pp. 764–769, July 1983.

[104] M. Kollmitzer, M. Olbrich, and E. Barke, "Analysis and Modeling of Minority Carrier Injection in deep-trench based BCD Technologies," in *Proceedings of the 2013 9th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, pp. 245–248, June 2013.

[105] Synopsys®, *Taurus™ Medici User Guide*, March 2013. Version H-2013.03.

[106] D. Klaassen, "A Unified Mobility Model for Device Simulation-I. Model Equations and Concentration Dependence," *Solid-State Electronics*, Vol. 35, pp. 953–959, July 1992. http://www.sciencedirect.com/science/article/pii/0038110192903257.

[107] D. Klaassen, "A Unified Mobility Model for Device Simulation-II. Temperature Dependence of Carrier Mobility and Lifetime," *Solid-State Electronics*, Vol. 35, pp. 961–967, July 1992. http://www.sciencedirect.com/science/article/pii/0038110192903268.

[108] D. J. Roulston, N. D. Arora, and S. G. Chamberlain, "Modeling and Measurement of Minority-Carrier Lifetime versus Doping in Diffused Layers of n^+-p Silicon Diodes," *IEEE Transactions on Electron Devices*, Vol. 29, pp. 284–291, February 1982.

[109] R. Häcker and A. Hangleiter, "Intrinsic Upper Limits of the Carrier Lifetime in Silicon," *Journal of Applied Physics*, Vol. 75, pp. 7570–7572, June 1994.

[110] M. S. Tyagi and R. van Overstraeten, "Minority carrier recombination in heavily-doped silicon," *Solid State Electronics*, Vol. 26, pp. 577–597, June 1983.

[111] S. Weiss and R. Kassing, "Deep Level Transient Fourier Spectroscopy (DLTFS)—A technique for the Analysis of Deep Level Properties," *Solid-State Electronics*, Vol. 31, pp. 1733–1742, December 1988. http://www.sciencedirect.com/science/article/pii/0038110188900718.

[112] eRamp Consortium, "D2.3.4: Report on TCAD and Spice Models for Smart Power Technologies." eRamp Project, ENIAC Joint Undertaking, March 2016.

[113] M. Kollmitzer, M. Olbrich, and E. Barke, "A Circuit Simulation Flow for Substrate Minority Carrier Injection in Smart Power ICs," in *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, pp. 171–174, May 2017.

[114] C. Stefanucci, P. Buccella, E. Seebacher, A. Steinmair, M. Kayal, and J. M. Sallese, "Analysis of Substrate Currents Propagation in HVCMOS Technology," in *2016 46th European Solid-State Device Research Conference (ESSDERC)*, pp. 319–322, September 2016.

[115] P. Buccella, C. Stefanucci, H. Zou, Y. Moursy, R. Iskander, J. M. Sallese, and M. Kayal, "Methodology for 3-D Substrate Network Extraction for SPICE Simulation of Parasitic Currents in Smart Power ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 35, pp. 1489–1502, September 2016.

[116] I. Keithley Instruments, *Model 2000 Multimeter, User's Manual*, 2010. Document Number: 2000-900-01 Rev. J.

[117] I. Keithley Instruments, *Model 2001 Multimeter, Operator's Manual*, 2009. Document Number: 2001-900-01 Rev. H.

[118] M. Abramowitz and I. A. Stegun, *Handbook of Mathematical Functions with Formulas, Graphs, and Mathematical Tables, 9th Printing*. Dover, 1972.

[119] E. W. Weisstein, *CRC Concise Encyclopedia of Mathematics, 2nd Edition*. Chapman and Hall/CRC Press, 2002.

List of Figures

List of Tables

List of Code Listings

Glossary

B

BCD	Bipolar, CMOS, DMOS
BEM	Boundary Element Method
BJT	Bipolar Junction Transistor
BTE	Boltzmann Transport Equation

C

CAD	Computer Aided Design
CAN	Controller Area Network
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical–Mechanical Polishing

D

DLTFS	Deep Level Transient Fourier Spectroscopy
DMOS	Double–diffused Metal Oxide Semiconductor
DuT	Device under Test

E

EDA	Electronic Design Automation
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge

F

FDM	Finite Difference Method
FEM	Finite Element Method
FET	Field Effect Transistor

I

IC	Integrated Circuit
ISO	International Organization for Standardization

L

LIN	Local Interconnect Network
LuT	Lookup Table
LVS	Layout versus Schematic

M

MAAP	Multi–Ring Active Analogic Protection
MOS	Metal Oxide Semiconductor

P

PCB	Printed Circuit Board
PDK	Product Development Kit
poly-Si	Polycrystalline Silicon

R

RF	Radio Frequency

S

SCR	Space Charge Region, also Depletion Region
Si	Silicon
SiO_2	Silicon Dioxide
SoC	System on a Chip
SOI	Silicon on Insulator
SPI	Serial Peripheral Interface
SPT	Smart Power Technology
SSE	Sum of Squares due to Error

T

TCAD	Technology Computer Aided Design

Symbols

Constants

Constant	Name	Value
ϵ_0	Permittivity of free space	$8.85418 \cdot 10^{-12}\ F \cdot m^{-1}$
h	Planck constant	$6.62607 \cdot 10^{-34}\ J \cdot s$
$\hbar$	Reduced Planck constant	$1.05457 \cdot 10^{-34}\ J \cdot s$
k_B	Boltzmann constant	$1.38066 \cdot 10^{-23}\ J \cdot K^{-1}$
m_e	Electron rest mass	$9.10938 \cdot 10^{-31}\ kg$
π	Pi	$3.14159 \cdot 10^{0}$
q	Unit electron charge	$1.60218 \cdot 10^{-19}\ C$

Variables

Symbol	Name	Unit
$\vec{D}$	Electric displacement field	$C \cdot m^{-2}$
D_n, D_p	Diffusion coefficient for electrons and holes	$m^2 \cdot s^{-1}$
E	Energy	J
E_t, E_c, E_v	Energy level of trap, conduction, and valence band	J
$\vec{E}$	Electric field	$V \cdot m^{-1}$
ϵ_0	Absolute permittivity	$F \cdot m^{-1}$
ϵ_{Si}	Relative permittivity of silicon	1
G_n, G_p	Generation rate for electrons and holes	$m^{-3} \cdot s^{-1}$
γ_E	Emitter efficiency	1
I	Electric current	A
J	Current density	$A \cdot m^{-2}$
$\vec{J_n}$, $\vec{J_p}$	Current density for electrons and holes	$A \cdot m^{-2}$
K	Thermal conductivity	$W \cdot m^{-1} \cdot K^{-1}$
k	Wave-vector	m^{-1}
k_B	Boltzmann constant	$J \cdot K^{-1}$
L	Inductance	H
L_{Debye}	Debye length	m
L_{DI}	Intrinsic Debye length	m

Symbol	Name	Unit
L_n, L_p	Diffusion length for electrons and holes	m
l_c	Mean free path	m
λ_B	de Brodlie wavelength	m
m_e^*	Effective mass of an electron	kg
μ_n, μ_p	Mobility of electrons and holes	$m^2 \cdot V^{-1} \cdot s^{-1}$
N_A^-, N_D^+	Density of acceptor and donor ions	m^{-3}
N_c, N_v	Density of conductor and valence band states	m^{-3}
n	Diode emission factor	1
n_0, p_0	Density of electrons and holes at equilibrium	m^{-3}
n, p	Density of electrons and holes	m^{-3}
n_d, p_d	Density of free electrons and holes	m^{-3}
n_{int}	Intrinsic carrier density	m^{-3}
n_s, p_s	Density of electrons and holes at the surface	m^{-3}
p	Crystal momentum	$kg \cdot m \cdot s^{-1}$
Φ	Electric potential	V
Φ_n, Φ_p	Quasi-Fermi potentials of electrons and holes	V
Φ_S	Quasi-Fermi potential at the surface	V
Φ_T	Thermal voltage	V
ψ	Electric potential	V
q	Unit electron charge	C
R	Resistance	Ω
R_n, R_p	Recombination rate for electrons and holes	$m^{-3} \cdot s^{-1}$
R_{RSH}	Shockley-Read-Hall recombination rate	$m^{-3} \cdot s^{-1}$
ρ	Electrical resistivity	$\Omega \cdot m$
S_n	Surface recombination velocity for electrons	$m \cdot s^{-1}$
σ	Electrical conductivity	$S \cdot m^{-1}$
T	Temperature	K
t	Time	s
τ_c	Mean free time	s
τ_n, τ_p	Carrier lifetimes for electrons and holes	s
τ_{on}, τ_{off}	Time constant for the on- and off-time	s
V	Voltage	V
V_T	Thermal voltage	V
v_{th}	Average thermal velocity of a particle	$m \cdot s^{-1}$
w_B	Width of the base	m
w_d, w_{si}, w_{ss}	Width of on-chip structures	m

Vector Analysis

x, y, z	Cartesian coordinates
$\hat{\mathbf{x}}$, $\hat{\mathbf{y}}$, $\hat{\mathbf{z}}$	Unit vectors parallel to the x, y, and z axes
f	Scalar field $f(x, y, z)$ for each point in Cartesian space (x, y, z)
∇f	Gradient of scalar field f
	$\nabla f \equiv \frac{\partial f}{\partial x}\hat{\mathbf{x}} + \frac{\partial f}{\partial y}\hat{\mathbf{y}} + \frac{\partial f}{\partial z}\hat{\mathbf{z}}$
$\overrightarrow{\mathbf{F}}$	Arbitrary vector field $\overrightarrow{\mathbf{F}}$ expanded in terms of the unit vectors is
	$\overrightarrow{\mathbf{F}} = F_x \cdot \hat{\mathbf{x}} + F_y \cdot \hat{\mathbf{y}} + F_z \cdot \hat{\mathbf{z}}$
	where F_x, F_y, F_z are the components of $\overrightarrow{\mathbf{F}}$.
$\nabla \cdot \overrightarrow{\mathbf{F}}$	Divergence of vector field $\overrightarrow{\mathbf{F}}$
	$\nabla \cdot \overrightarrow{\mathbf{F}} \equiv \frac{\partial F_x}{\partial x}\hat{\mathbf{x}} + \frac{\partial F_y}{\partial y}\hat{\mathbf{y}} + \frac{\partial F_z}{\partial z}\hat{\mathbf{z}}$
$\nabla \times \overrightarrow{\mathbf{F}}$	Curl of vector field $\overrightarrow{\mathbf{F}}$
	$\nabla \times \overrightarrow{\mathbf{F}} \equiv \left(\frac{\partial F_z}{\partial y} - \frac{\partial F_y}{\partial z}\right)\hat{\mathbf{x}} + \left(\frac{\partial F_x}{\partial z} - \frac{\partial F_z}{\partial x}\right)\hat{\mathbf{y}} + \left(\frac{\partial F_y}{\partial x} - \frac{\partial F_x}{\partial y}\right)\hat{\mathbf{z}}$

Appendix A

Test Chip Overview

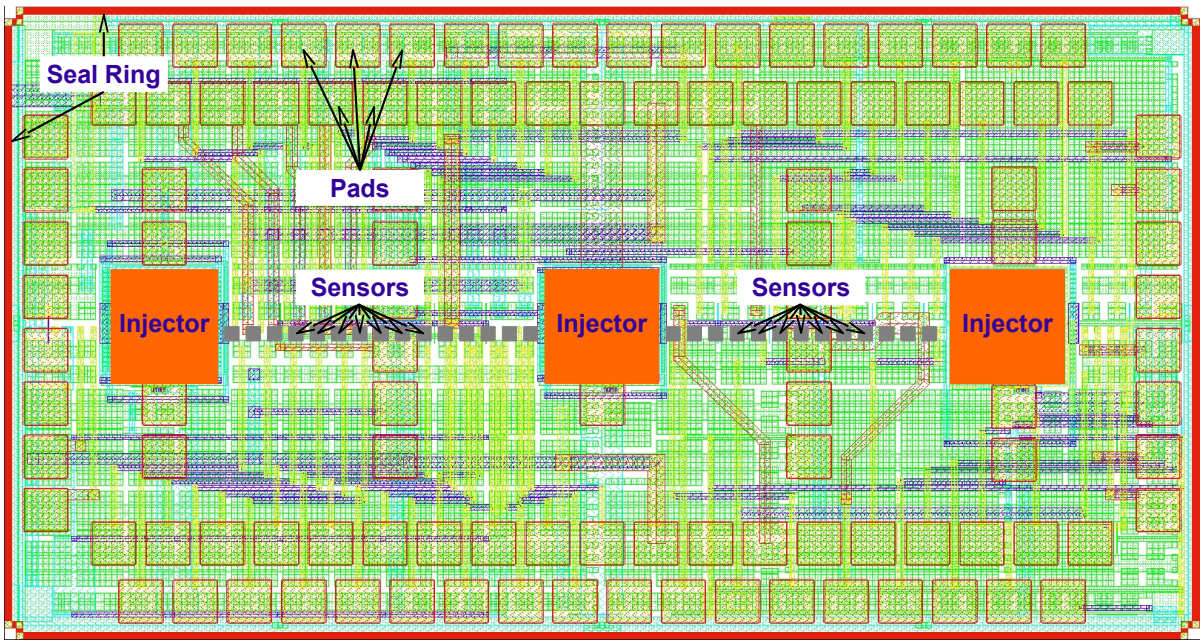


Figure A.1: Layout view of test chip *A*

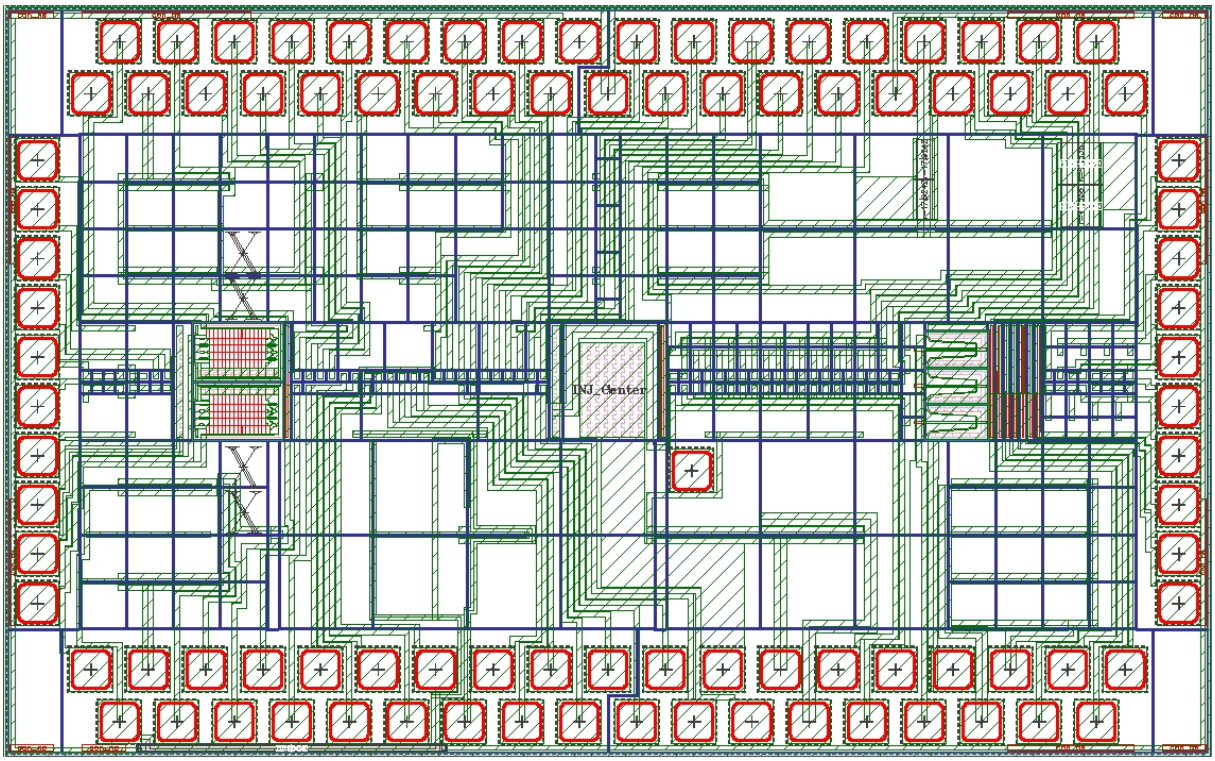


Figure A.2: Layout view of test chip *B*

Appendix B

Used Measurement Equipment

Table B.1: Laboratory equipment list

Equipment type	**Appliance used**
Main power source (e.g. injector)	HP E3632A
Secondary power source (e.g. supply)	TTi EX752M
Digital multimeter	Keithley 2000 Keithley 2001 Keithley 199 Iso-Tech IDM-62T
Oscilloscope	Agilent DSO-X 3034A
Current probe	Tektronix TCP2020

Appendix C

Symbolic Calculations

Listing C.1: Base carrier and current density

```
restart;
odeinp := diff(n(x), `$`(x, 2))-(n(x)-n0)/Ln^2 = 0;
odesol := dsolve(ode);
odeics := n(0) = n0*exp(q*VBE/(k*T)), n(w) = 0;
odes00 := dsolve({odeics, odeinp});
sims00 := simplify(odes00);
sims01 := algsubs(exp(w/Ln)-exp(-w/Ln) = 2*sinh(w/Ln), sims00);
sims02 := algsubs(exp(-x/Ln)-exp(x/Ln) = 2*sinh(-x/Ln), sims01);
sims03 := algsubs(exp(-(-x+w)/Ln)-exp((-x+w)/Ln) = 2*sinh(-(-x+w)/Ln),
          sims02);
sims04 := algsubs(-exp((x*k*T-w*k*T+q*VBE*Ln)/(Ln*k*T))+exp((-x*k*T+
          w*k*T+q*VBE*Ln)/(Ln*k*T)) = 2*exp(q*VBE/(k*T))*
          sinh((-x+w)/Ln), sims03);
sims05 := simplify(sims04);
dsol01 := diff(sims05, x);
dsol02 := simplify(dsol01);
```

Listing C.2: Collector carrier and current density

```
restart;
odeinp := diff(p(x), `$`(x, 2))-(p(x)-p0)/Lp^2 = 0;
odesol := dsolve(odeinp);
odeics := p(0) = 0, p(w) = p0;
odes00 := dsolve({odeics, odeinp});
sims00 := simplify(odes00);
sims01 := algsubs(exp(w/Lp)-exp(-w/Lp) = 2*sinh(w/Lp), sims00);
sims02 := algsubs(exp((-x+w)/Lp)-exp(-(-x+w)/Lp) = 2*sinh((-x+w)/Lp),
          sims01);
sims03 := simplify(sims02);
dsol01 := diff(sims03, x);
dsol02 := simplify(dsol01);
```

Listing C.3: Emitter carrier and current density

```
restart;
odeinp := diff(p(x), `$`(x, 2))-(p(x)-p0)/Lp^2 = 0;
odesol := dsolve(odeinp);
odeics := p(0) = p0*exp(q*V[BE]/(k*T)), p(w) = p0;
odes00 := dsolve({odeics, odeinp});
sims00 := simplify(odes00);
sims01 := algsubs(exp(w/Lp)-exp(-w/Lp) = 2*sinh(w/Lp), sims00);
sims02 := algsubs(exp((-x+w)/Lp)-exp(-(-x+w)/Lp) = 2*sinh((-x+w)/Lp),
          sims01);
sims03 := algsubs(-exp((k*T*x-w*k*T+Lp*q*V[BE])/(Lp*k*T))+exp((-k*T*x+
          w*k*T+Lp*q*V[BE])/(Lp*k*T)) = 2*exp(q*V[BE]/(k*T))*
          sinh((-x+w)/Lp), sims02);
sims04 := simplify(sims03);
dsol01 := diff(sims04, x);
dsol02 := simplify(dsol01);
```

Listing C.4: Emitter efficiency Maple source code

```
# based on the carrier density results for the base and the emitter
# w[B] and w[E] need to be used accordingly
currEn  := J[En] = (unapply(simplify(q*D[Bn]*(diff(rhs(basesims05),
           x))),x))(0);
currEp  := J[Ep] = (unapply(simplify(q*D[Ep]*(diff(rhs(emitsims04),
           x))),x))(0);
# substitutions
CDJEn00 := algsubs(cosh(w[B]/Ln)/sinh(w[B]/Ln) = coth(w[B]/Ln),
           expand(basecurrEn));
simfn   := Zeta[n] = q*D[Bn]/Ln;
CDJen   := simplify(algsubs(rhs(simfn) = lhs(simfn), CDJEn00));
CDJEp00 := algsubs(cosh(w[E]/Ln)/sinh(w[E]/Ln) = coth(w[E]/Ln),
           expand(emitcurrEp));
simfp   := Zeta[p] = q*D[Ep]/Lp;
CDJep   := simplify(algsubs(rhs(simfp) = lhs(simfp), CDJEp00));

tmp01   := algsubs(cosh(w[E]/Lp)/sinh(w[E]/Lp) = coth(w[E]/Lp),
           simplify(rhs(CDJep)/rhs(CDJen)))
Eeff    := gamma[E]=1/(1+tmp01);
```

Appendix D

Matlab Source Codes

Listing D.1: LU decomposition

```
function [x] = LU_deco(a,b,c,f)
% LU decomposition function
  % Sanity check
  if( (length(a) ~= length(b)) || (length(b) ~= length(c)) || ...
      (length(c) ~= length(f)) || (length(f) ~= length(a)) )
    error('LU_deco: input parameters must have same length');
  end
  n_max = length(a);

  % prepare alpha and beta
  beta  = zeros(1,n_max);
  alpha = zeros(1,n_max);

  % Determine rows of L
  alpha(1) = a(1);
  for i=2:n_max
    beta(i)  = c(i)/alpha(i-1);
    alpha(i) = a(i)-beta(i)*b(i-1);
  end

  y = zeros(1,n_max);
  % Solution of L*y = f %
  y(1) = f(1);
  for i=2:n_max
    y(i) = f(i) - beta(i)*y(i-1);
  end

  x = zeros(1,n_max);
  % Solution of U*x = y %
  x(n_max)       = y(n_max)/alpha(n_max);
  for i = (n_max-1):-1:1
    x(i)       = (y(i)-b(i)*x(i+1))/alpha(i);
  end
end
```

Curriculum Vitae

Education

2007-2009	**M.Sc.** Carinthia University of Applied Sciences, Integrated Systems and Circuits Design (part time study program)
2000-2004	**Dipl. Ing. (FH)** Carinthia University of Applied Sciences, Electrical Engineering (part time study program)
1993-1998	**University Entrance Qualification** Federal Higher Technical Institute, Electronics and Telecommunications

Theses, Publications

2017	**ISPSD Conference** A Circuit Simulation Flow for Substrate Minority Carrier Injection in Smart Power ICs
2013	**PRIME Conference** Analysis and Modeling of Minority Carrier Injection in Deep–Trench Based BCD Technologies
2009	**Master Thesis** Extraction of Layout Structures for Reverse Current Simulation
2004	**Dipl. Ing. (FH) Thesis** Interconnect Resistance Extraction and Modeling of RC Parasitics for a BCD Technology

Work Experience

2011-now	**Research Substrate Coupling, Infineon Technologies** Development of a circuit simulation flow for parasitic coupling caused by minority carrier injection in power ICs. Research included test chip design in several technologies as well as measurement in the lab. Dedicated TCAD simulations were used to analyze the effect in detail and to quantify the effectiveness of guard ring structures.
2004-now	**Physical Verification Engineer, Infineon Technologies** Development and implementation of DRC, ERC, LVS, and Lapo rule decks for several power technologies as well as supporting the physical designers regarding design verification. Additionally, setting up the extraction rule decks for the metalization's parasitic RC devices.
2000-2004	**Analog Physical Design Engineer, Infineon Technologies** Full custom physical design of analog and digital blocks for Smart Power ICs with focus on multichannel switches. Responsibilities included top-level floorplanning, creating bonding diagrams, block- and top-level layout and verification.
1999-2000	**Database Developer, Professional Clinical Software** Development of relational database software for hospitals using Progress. Interface development with VisualBasic and VisualC/C++ for communication between medical equipment and the patient database.

Erklärung

Ich erkläre hiermit, dass ich die vorliegende Dissertation selbstständig verfasst und noch nicht anderweitig zu Prüfungszwecken vorgelegt habe. Sämtliche benutzte Quellen und Hilfsmittel sind angegeben, wörtliche und sinngemäße Zitate sind als solche gekennzeichnet.

Villach, 19.02.2020

Ort, Datum

Michael Kollmitzer