Polycrystalline silicon / monocrystalline silicon junctions and their application as passivated contacts for Si solar cells

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Kurzzusammenfassung

Im Rahmen dieser Arbeit wird ein Prozess zur Herstellung eines Schichtsystems aus polykristallinem Silizium / Silizium-oxid / kristallinem Silizium (poly-Si / SiO_x / c-Si) für die Verwendung als passivierter Kontakt für hocheffiziente kristalline Silizium Solarzellen entwickelt. Der Einfluss der einzelnen Prozessschritte der poly-Si Kontakt Herstellung, wie das Wachstum des Grenzflächenoxids, die thermische Behandlung und der Dotierprozess auf die mikroskopischen und makroskopischen Eigenschaften des poly-Si Kontakts werden untersucht. Basierend auf diesen Untersuchungen wird schrittweise eine Verbesserung der Kontaktqualität erreicht. Die resultierenden poly-Si Kontakte erreichen Sättigungsstromdichten $J_{0,\mathrm{poly}}$ von 0,66 fA/cm^2 für n-Typ poly-Si Kontakte und 4,4 fA/cm^2 für p-Typ poly-Si Kontakte. Dies sind die niedrigsten bisher publizierten Werte für poly-Si Kontakte.

Mit diesen Kontakten werden die ersten veröffentlichten voll poly-Si kontaktierten Solarzellen hergestellt. Diese erreichen eine offene Klemmspannung von 714 mV und einen Serienwiderstand von 0.6 Ω cm^2. Es wird gezeigt, dass Letzterer größtenteils durch das Metall-Layout verursacht wird und nicht durch den Kontaktwiderstand ρ_{int} der poly-Si Schicht.

Basierend auf den beobachteten Abhängigkeiten des Kontaktwiderstands zwischen der poly-Si Schicht und dem Wafer von den Prozessparametern werden die existierenden Modelle für den Ladungsträgertransport durch das Grenzflächenoxid diskutiert und bewertet. Weiterhin werden, für das Pinhole-Modell, 3D Bauteil-Simulationen durchgeführt um die Plausibilität dieses Modells zu bestätigen.

Gegendotieren mittels in-situ maskierter Ionenimplantation in c-Si Wafer wird als Methode für die Herstellung von Rückseiten-sammelnden Rückkontaktsolarzellen (BJBC) evaluiert. Die Rekombinationscharakteristik der mit diesem Prozess hergestellten hochdotierten sich berührenden p- und n-Typ Gebiete wird mit Dioden-Teststrukturen untersucht. Es wird kein schädlicher Einfluss von trap-assisted-tunneling, Band zu Band Tunneln oder Schockley Read Hall Rekombination beobachtet. 156 mm × 156 mm große mittels Gegendotieren mit maskierter Ionenimplantation hergestellte c-Si BJBC Solarzellen erreichen Effizienzen von 22,1 %.

Es wird gezeigt, dass eine Kombination der beiden Technologien, poly-Si Kontakte und Gegendotieren mittels Ionenimplantation, möglich ist und für Bor implantierte Schichten welche ganzflächig mittels Phosphor-Implantation überkompensiert werden, $J_{0,\mathrm{poly}}$ und ρ_{int} Werte von 1.0 fA/cm^2 und 250 mΩ cm^2 erreicht werden können. Diese Werte sind Vergleichbar mit den Werten von nur Phosphor implantierten Referenzen von 1.0 fA/cm^2 und 80 mΩ cm^2.

Für maskiert überkompensierte poly-Si Kontakte wird gezeigt, dass der laterale pn-Übergang in der defektreichen poly-Si Schicht eine parasitäre Rekombination erzeugt, welche die Leistung der hergestellten Bauteile beeinträchtigt. Basierend auf Bauteilsimulationen wird ein Modell zur Beschreibung der Rekombinationscharakteristik entwickelt und mit dem Ziel die parasitäre Rekombination zu reduzieren, werden am lateralen pn-Übergang in der poly-Si Schicht speziell konzipierte Dioden hergestellt.

Ohne Überkompensation hergestellte BJBC Solarzellen mit einem poly-Si back surface field zeigen Effizienzen von 21,7 %. Die offene Klemmspannung der besten Zelle beträgt 673,6 mV und der zugehörige Kontaktwiderstand hat einen Wert von 0,4 Ω cm^2.

Schlagworte: Polykristallines Silizium, passivierte Kontakte, Solarzellen

Abstract

In this thesis a process for the fabrication of polycrystalline silicon / silicon oxide / crystalline silicon (poly-Si / SiO_x / *c*-Si) junctions as passivated contacts for high efficiency crystalline silicon solar cells is developed. The influence of the individual process steps of the poly-Si contact fabrication, such as the growth of the interfacial oxide, the thermal treatment and the doping process on the microscopic and macroscopic properties of the poly-Si contacts are investigated. Based on these investigations a subsequent improvement of the junction quality is achieved, resulting in poly-Si contacts with a saturation current density $J_{0,\mathrm{poly}}$ of $0.66\,\mathrm{fA/cm^2}$ for *n*-type poly-Si contacts and $4.4\,\mathrm{fA/cm^2}$ for *p*-type poly-Si contacts. These are the lowest published values for poly-Si contacts so far.

With these junctions, the first published full poly-Si contacted solar cell is fabricated, exhibiting an open circuit voltage of 714 mV and a series resistance of $0.6\,\Omega\,\mathrm{cm^2}$. The latter is shown to be mainly dominated by the metalization layout instead of the interface contact resistivity ρ_{int} of the poly-Si contact.

Based on the observed dependencies of the interface contact resistance between the poly-Si layer and the *c*-Si wafer on the process parameters, the existing models for the carrier transport through the interface oxide are discussed and evaluated. Further, for the pinhole model, 3D device simulations are conducted to confirm the plausibility of this model.

Counterdoping with in-situ patterned ion implantation in *c*-Si wafers is evaluated as a method for the lean fabrication of back junction back contacted (BJBC) Si solar cells. The recombination characteristics of the highly doped touching *p*- and *n*-type regions created with this process are investigated with diode test structures. No detrimental influence of trap assisted tunneling, band to band tunneling or Shockley Read Hall (SRH) recombination is observed. $156\,\mathrm{mm} \times 156\,\mathrm{mm}$ large *c*-Si BJBC solar cells fabricated with counterdoping via in-situ patterned ion implantation reach conversion efficiencies of 22.1 %.

It is shown that the combination of the two technologies, poly-Si contacts and counterdoping with ion implantation is possible and results in $J_{0,\mathrm{poly}}$ and ρ_{int} values of $1.0\,\mathrm{fA/cm^2}$ and $250\,\mathrm{m\Omega\,cm^2}$ for boron implanted layers, overcompensated with a full area phosphorus implantation. These values are comparable to values of only phosphorus implanted references of $1.0\,\mathrm{fA/cm^2}$ and $80\,\mathrm{m\Omega\,cm^2}$.

For patterned counterdoped poly-Si contacts, the lateral *pn*-junction in the highly defective poly-Si layer is shown to induce a parasitic recombination, limiting the performance of the fabricated devices. Based on device simulations, a model, describing the measured recombination characteristics, is developed and specially designed diodes at the lateral *pn*-junction in the poly-Si layers are fabricated with the aim to reduce the parasitic recombination.

BJBC solar cells, fabricated without counterdoping and featuring a poly-Si back surface field exhibit efficiencies up to 21.7 %. The open circuit voltage of the best cell is 673.6 mV and the corresponding series resistance has a value of $0.4\,\Omega\,\mathrm{cm^2}$.

Key words: Polycristalline silicon, passivated contacts, solar cells

Contents

Chapter 1

Introduction

In order to be competitive with other methods of electric energy generation, photovoltaic modules have to generate as much energy as possible for a price, as low as possible. This ratio over the lifetime of a photovoltaic module is called levelized costs of electricity and is measured in US$/kW h. Today a typical price for photovoltaic electricity generation is 0.093 US$/kW h [1]. The share of the solar cell manufacturing process costs amounts to only 6 % of the total cost of the PV system. The latter includes the costs of the Si material, wafering, module integration, installation and the inverter [1]. Therefore, as the solar cell manufacturing costs are relatively low and the larger part of the other costs is area dependent, not power dependent, one approach to further reduce the levelized costs of electricity is to increase the energy conversion efficiency of the solar cells.

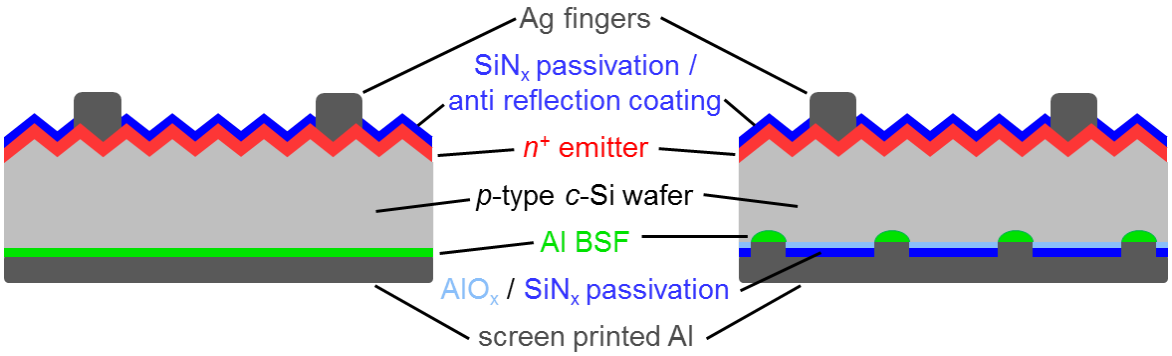

Figure 1.1.: Sketch of an Al-BSF solar cell (left) and a PERC solar cell (right).

Figure 1.1 shows a sketch of two crystalline silicon (c-Si) solar cell types that are in production nowadays. These solar cells will now be used to describe, what the main loss mechanisms are in typical solar cells and how the light conversion efficiency of a solar cell can be improved. First, some part of the incoming light is reflected, either at the metal contacts on the front side, at the front surface between the metal contacts, or (for the long wavelength light) on the rear surface from which a part may leave the cell again. Reducing the reflection losses will mainly increase the short circuit current density J_{sc}. Then, from the part of the light that is absorbed in the solar cell, electron-hole-pairs are generated that have to be collected at the contacts. Before they reach the contacts there is a certain possibility that they recombine, either in the bulk of the cell, at the non-metalized surface, or a the metal contacts. Reducing the recombination will mainly increase the open circuit voltage V_{oc}. A further important parameter is the series resistance, with the main contribution from the metal / silicon contact and laterally along the metal contacts. Reducing the series resistance results in an increase of the so called fill-factor FF. The product of the three values per incident power P_{in} gives the conversion efficiency η of the solar cell:

$$\eta = J_{\mathrm{sc}}\, V_{\mathrm{oc}}\, FF \,/\, P_{\mathrm{in}} \tag{1.1}$$

For silicon solar cells, reducing the recombination offers the largest potential for efficiency increases [2], [3]. This will be the focus of this work. Most contributors to the recombination of a solar cell can be described by a diode equation:

$$J_{\mathrm{rec}}(V) = J_0 \left(\exp\left(\frac{qV}{kT}\right) - 1 \right), \tag{1.2}$$

with $J_{\mathrm{rec}}(V)$ the voltage dependent recombination current, J_0 the saturation current density, q the elementary charge, V the voltage, k the Boltzmann constant, and T the temperature. Table 1.1 shows the saturation current densities for the main contributors to the recombination in an Al-BSF solar cell and a PERC solar cell. The name Al-BSF cell originates from the full area Al back surface field (BSF) denoting an Al doped region under the contact at the rear side of the cell. This full area metalized surface represents the main contribution to total recombination of the cell. PERC stands for passivated emitter and rear cell and is the advanced version of the Al-BSF cell, as here not only the emitter at the front, but also the rear is passivated. Even though in typical PERC cells most of the rear is passivated with only local Al-BSF contacts (see figure 1.1), recombination at the metal contacts is still a major loss mechanisms. Also, the recombination at the front side is mainly determined by the emitter diffusion that is needed for a good contact.

Different approaches have been made to reduce the recombination at the metal contacts. One is to locally increase the dopant density under the metal contacts in order to reduce the minority carrier density at the unpassivated surface [6], [7], while at the same time

name	bulk	passivated front	metalized front	passivated rear	metalized rear	total
Al-BSF	80 fA/cm^2	110 fA/cm^2	30 fA/cm^2	-	540 fA/cm^2	760 fA/cm^2
PERC	80 fA/cm^2	100 fA/cm^2	20 fA/cm^2	10 fA/cm^2	50 fA/cm^2	260 fA/cm^2

Table 1.1.: Typical saturation current density contributions of different regions of Al-BSF and PERC solar cells. The values are reprinted from [4], [5]

reducing the dopant density at the non-metalized regions and thus reducing the Auger recombination at the passivated surface.

An alternative approach is to use carrier selective contacts, that are "transparent" for one type of charge carriers, while blocking the other type of charge carriers. One prominent example are hydrogen rich amorphous silicon (*a*-Si:H) / crystalline silicon (*c*-Si) heterojunction (HET) solar cells [8]–[10]. HET solar cells typically exhibit J_0 values of 5 fA/cm^2 per surface, even in the metalized regions. This enables V_{oc}-values as high as 750 mV and efficiencies of 25.6 % [11]. In general *a*-Si heterojunction solar cells are fabricated by the use of numerous plasma enhanced chemical vapor deposition (PECVD) steps and require the deposition of transparent conducting oxides (TCOs), which both are regarded as expensive. Additionally the passivation quality of *a*-Si:H / *c*-Si interfaces is not stable at temperatures above 300 °C [12], which complicates the metalization processes of solar cells.

Different other approaches for carrier selective contacts or passivated contacts have been investigated, including *a*-Si HET layers with SiO_x interlayer [13]–[15], thin passivation layers under the metal contact [16]–[18], transparent conductive oxides with dielectric interlayers [19]–[25], or other approaches [22], [26]–[29].

In this work another type of carrier selective contacts will be investigated: the poly-crystalline silicon (poly-Si) / SiO_x / *c*-Si contact. Benefits over HET contacts are the possibility to deposit the layers via low pressure chemical vapor deposition (LPCVD) in high throughput tube furnaces, which is possibly more cost efficient than PECVD deposition. Also beneficial is the high thermal stability of the layers. During the fabrication of poly-Si contacts temperatures of typically 800 °C-1050 °C are reached, therefore additional processes with lower thermal budgets have limited impact on the passivation quality of the layers.

The high thermal stability of the poly-Si contacts on one hand offers the possibility to apply standard screen printing technologies for the contact formation instead of the more costly and less conductive low temperature silver screen printing pastes as required for HET solar cells. Another advantage of the high thermal stability is the possibility to apply doping techniques other than in-situ doping during the deposition. This is especially useful for the fabrication of back junction back contacted (BJBC) solar cells, where both

dopant polarities are located at the rear side of the solar cell. The major advantage of BJBC solar cells over both side contacted solar cells is the avoidance of the front contact shading.

1.1. Structure of this work

Chapter 2 will give an overview of the current state of the art regarding poly-Si contacts and poly-Si contacted solar cells.

Chapter 3 presents the working principle of poly-Si contacts including a comparison between different transport models. Finally, the main measurement methods used in this work are introduced, including a new method developed in frame of this work, to estimate an upper limit for the contact resistance between two conducting layers.

Chapter 4 covers the optimization of the different process parameters and the characterization of poly-Si contacts. It also shows the application of the poly-Si contacts on a simple both side contacted solar cell demonstrator and structural investigations with the aim to improve the understanding of the current transport mechanism through the poly-Si / Si contact.

Chapter 5 presents the fabrication of BJBC test structures and an investigation of the recombination properties in the highly doped lateral *pn*-junctions, first on conventional *c*-Si test structures without poly-Si contacts and then on poly-Si passivated test structures. For the poly-Si case methods to reduce the recombination in the lateral *pn*-junction are evaluated and numeric device simulations are performed to identify the main influences on the *pn*-junction recombination.

Chapter 6 presents the application of poly-Si contacts in a hybrid BJBC solar cell, with a poly-Si BSF and a diffused *c*-Si emitter.

Chapter 2

State of the art

In this section a short review over the literature regarding poly-Si contacts to mono-crystalline silicon is given. First in order to define what is meant with poly-Si: In general, the term poly-Si describes any Si material consisting of many crystalline grains (of any size) with different orientations, in contrast to mono-crystalline Si where ideally all Si atoms are arranged in one large lattice. The term poly-Si is used for different approaches, in photovoltaic technology this term is also used to describe the silicon feedstock material for the growth of monocrystalline silicon ingots and sometimes also to describe the more commonly named "multicrystalline" silicon wafers used as a base material for solar cells. In this work, "poly-Si contact" always means a layer of poly-Si used as a contact to a silicon wafer. Typically also an interface oxide is present between the poly-Si layer and the Si wafer.

Poly-silicon contacts and the related SIPOS (semi-insulating polycrystalline silicon) contacts have been studied extensively by several groups working on bipolar junction transistors (BJTs) [30]–[38]. It was found that by substituting the emitter of a *n/p/n*-BJT with a *n*-type poly-Si contact, the current gain of the BJT can be increased by more than one order of magnitude [39]. Studies investigating the cause of this increase have shown that the formation of a thin, intentionally or unintentionally grown interfacial oxide between the poly-Si and *c*-Si interface is crucial to obtain high performance devices [36]–[38]. It has also been shown that a thermal treatment can enhance the properties of poly-Si contacted BJT, unless the thermal budget is not chosen too high [35], [39]. Due to this increase in the current gain, poly-Si contacts are since many years state of the art for BJTs.

The feature of an increase of the gain of BJTs can analogously be used to increase the performance of *c*-Si solar cells. The current gain of a BJT is the ratio of the collector current to the base current, i.e., for the case of a $n/p/n$-BJT it is mainly the ratio of the electrons injected from the emitter into the base and of the holes injected from the base into the emitter. In a solar cell a high collector current corresponds to a low "internal" series resistance and a low base current to a low emitter recombination current, i.e., a good emitter surface passivation. The adaption of poly-Si contacts to solar cells has already been proposed in the 1980s by Fossum and Shibib [40]. Since then, several groups have investigated poly-Si contacts specifically for *c*-Si solar cell applications [41]–[46]. Even though the passivation quality has been greatly improved with poly-Si contacts, resulting for instance in a SIPOS solar cell with an outstanding V_{oc} of 720 mV [43], a good combination of low series resistance and high V_{oc} has not been achieved with the first poly-Si contacted *c*-Si solar cells [43], [44]. Therefore only few work has been published after the 90s.

Nevertheless, recently many groups regained interest in poly-Si contacts or related technologies. This new interest has among other things been provoked by the achievement of a 24.2 % efficient back contacted solar cell with "passivated contacts" by Sunpower Corp. [47], together with numerous patent applications in the field of poly-Si / SiO_2 / *c*-Si junctions by this company (see e.g., [48], [49] and the references therein). Further improvements of the cell fabrication process have resulted in a conversion efficiency of 25.0 % [50].

Inspired by these results, several groups succeeded in fabricating solar cells with noteworthy conversion efficiencies. A selection of published data is shown in table 2.1. The first to publish high conversion efficiencies with passivated contacts were Feldmann *et al.* [55] from the Fraunhofer Institute for Solar Energy Systems (F-ISE). They used chemically

Group	Area [cm^2]	η [%]	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	$J_{0,\mathrm{poly}}$ [mA/cm^2]	$J^a_{0,\mathrm{front}}$ [mA/cm^2]	$J^b_{0,\mathrm{front}}$ [mA/cm^2]
Sunpower [47]	155.1	24.2	721	40.5	82.9	n/a	n/a	n/a
F-ISE [51]	4	25.1	718	42.1	83.2	7	13	15
NREL [52]	n/a	21.5	693	39.6	78.4	2.1	17.1	n/a
ANU [53]	4	20.8	675	38.4	80.4	9	38	80
GT [54]	132	20.9	683	39.4	77.6	3-5	10	n/a

Table 2.1.: Solar cell parameters of the supposedly poly-Si passivated cells fabricated by the company Sunpower and the poly-Si passivated cells of several institutes. Listed are the cell area (or for the smaller cells the active area), solar energy conversion efficiency η, open circuit voltage V_{oc}, short circuit current density J_{sc} and fill factor FF and the saturation current densities of the poly-Si passivated rear surface $J_{0,\mathrm{poly}}$ and of the front surface before metalization $J^a_{0,\mathrm{front}}$ and after metalization $J^b_{0,\mathrm{front}}$.

grown oxides and in-situ doped plasma enhanced chemical vapor deposited (PECVD) *a*-Si. Due to the incorporation of not specified impurities, the *a*-Si layers stay amorphous at high temperature anneals. Even though the layers are not polycrystalline, they will be compared with the other poly-Si contacts in this work. The researchers named their layer system "TOPCon". The application of an *n*-TOPCon layer on the rear side of a high efficiency solar cell with a boron diffused emitter on the front side resulted in an impressive conversion efficiency of 23.0 % with a V_{oc}-value of 698 mV and a fill factor of 81.1 % [55], confirming that a low series resistance and high passivation quality is achievable with this technology. Further improvements in the cell processing have lead to an efficiency of 25.1 % [56].

In reference [57] the TOPCon-concept was also implemented on an BJBC solar cell with both polarities passivated with TOPCon-layers. The authors report high V_{oc}-values of 682 mV, but due to problems with the contact formation, the series resistance-values are not mentioned.

The solar cells described in the following are all in principle similar to the F-ISE solar cell: They exhibit a boron diffused emitter at the front side and a poly-Si passivated BSF at the rear side. While different processes and technologies for the fabrication of the poly-Si BSF have been used, so far no other institute reported on the incorporation of additional impurities, so the resulting layers after high temperature processing should all be polycrystalline. Even though the achieved poly-Si saturation current densities $J_{0,poly}$ all vary slightly, the open circuit voltage V_{oc} of the cells is in all cases dominated by recombination at the (compared to the cell of F-ISE) less optimized front side (see table 2.1).

- The researchers of the group at the National Renewable Energy Laboratory (NREL), use in-situ doped PECVD *n*-type poly-Si as BSF on the rear side. Stradins *et al.* [52] presented an efficiency of 21.5 %.

- In the group at the Australian National University (ANU) [53] the PECVD *a*-Si was deposited undoped and then doped via $POCl_3$-diffusion. The best achieved conversion efficiency of 20.8 % was mainly limited by recombination at the metalized contacts on the front side and optical losses due to a less optimized front side process compared to the NREL process.

- Also very noteworthy is the work performed at the Georgia Institute of Technology (GT). Upadhyaya *et al.* [54] presented a 132 cm^2 large solar cell. The achieved efficiency of 20.9 % was limited by contact recombination at the front metal contacts, leading to a drop of the $V_{oc,impl}$-value from 727 mV before metalization to a V_{oc}-value of 683 mV after metalization. With the implementation of a selective emitter, they plan to reach V_{oc}-values above 700 mV and efficiencies above 22 %.

Alongside with the development of poly-Si passivated solar cells, the struggle to understand the mechanisms enabling the extraordinary characteristics of this material has lead to numerous publications, including parameter studies and fundamental investigations. The influence of the interface oxide on the passivation quality and on the contact resistance of test structures has been investigated by varying the growing oxides: For wet chemically grown oxides, different chemical baths, temperatures and process times have been investigated [53], [54], [58]–[61], for dry oxides, grown in an ozone ambient, also the process times has been varied [58], [59], and for thermally grown oxides, the influence of the annealing temperature and time have been investigated [53], [60]. The resulting oxides have been shown to differ not only in their thickness, but also in their stoichiometry [58], [59]. Yan *et al.* also investigated SiO_x/SiN_x stacks as interface layers. [62] It was found that thicker oxide interface layers exhibit a better passivation quality than thinner oxides and moderate thermal annealing of the oxides leads to an improvement of the passivation quality, while too high thermal budgets result in a strongly degraded passivation quality [53], [54], [62], [63]. Another finding was that the contact resistance of test structures decreases with a decreasing thickness of the interface oxide and that for thick oxides with a high contact resistance, thermal annealing can reduce the contact resistance [53].

Despite numerous investigations on poly-Si contacts, the physical mechanism reducing current injection from the *c*-Si into the poly-Si, while not reducing the injection from the poly-Si into the *c*-Si is still not fully understood. Several models have been proposed to explain the improved performance. An overview of the models is shown in section 3.1.2.

2.1. Classification of this work

Due to the current strong interest in poly-Si contacts for photovoltaic applications and the intense research on this topic, several aspects of this work can also be found in publications of other researches. Therefore, it has to be stated that the beginning of this work was slightly before the onset of the new interest on poly-Si contacts. The first publication extracted from this work [64] was published simultaneously with the first publication on poly-Si contacts of Frauenhofer ISE. The results presented in the next chapters have been obtained before similar work has been published by other researchers. Further, parts of this work have been published as the first of their kind, e.g. in reference [65] the first full poly-Si contacted solar cells have been shown and in reference [66] the first works on ion implantation for the doping of poly-Si contacts were presented. Also, the passivation quality of the junctions presented in reference [67] is the best reported so far for both, *p*- and *n*-type poly-Si layers.

Chapter 3

Theory

3.1. Working principle

In this section, the working principle of the polycrystalline silicon / monocrystalline silicon junctions (poly-Si contacts) will be discussed. As already mentioned in the introduction (chapter 1), poly-Si contacts are one approach among others to create passivated contacts (also called carrier selective contacts), i.e., a contact that is "transparent" for one charge carrier type, while blocking the other charge carrier type. The first aspect is important for the realization of a good contact, i.e., a low contact resistivity. The second aspect ensures a good passivation, i.e., low recombination of charge carriers at the contact.

3.1.1. Passivation

In general two mechanisms exist that reduce recombination on surfaces. The first one deals with the reduction of defects naturally occurring at a crystal surface (or here at the interface to a passivation layer), by saturating dangling silicon bonds. This can be achieved for example with silicon dioxide layers [68], [69] or atomic hydrogen from hydrogen rich layers like PECVD-deposted silicon nitride (SiN_x) [70], [71]. The second mechanism comprises the reduction of one type of charge carriers near the surface by inducing appropriate band offsets or an appropriate bending. The latter is accompanied with the existence of an electric field. In most cases the electric field arises from fixed charges in the passivation layers or at the silicon interface. Aluminum oxide (AlO_x) for example exhibits a very high density of fixed negative charges. These charges result in a bending of the energy bands in the silicon and a depletion of electrons and an accumulation

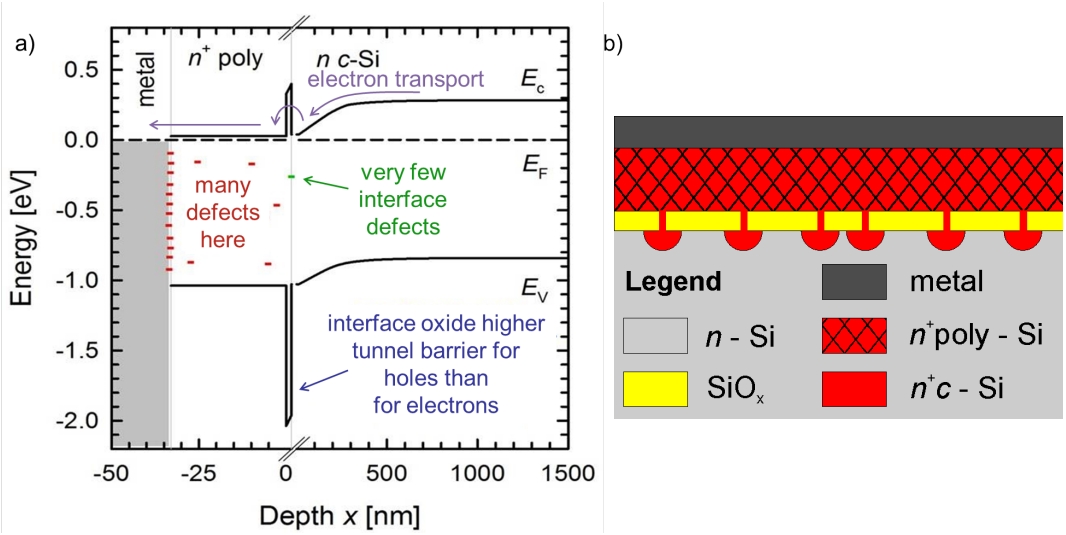

Figure 3.1.: a) Sketch of the band diagram of a poly-Si contact, including purple arrows showing the transport of the electrons as explained within the tunneling model. In this figure, the tunneling barrier heights of 0.3 eV and 1 eV [39] are used for the conduction and valence band offsets between SiO_2 and Si. b) Sketch of poly-Si contact, including pinholes in the interface oxide and semi-spherically doped regions in the c-Si as predicted by the pinhole model.

of holes. As for the recombination both charge carrier types are needed, the reduction of one charge carrier type leads to a reduction of the surface recombination. Another method to realize an electric field at the surface is to create a doped layer, that also reduces the amount of the respective minority charge carrier type. As a layer with high doping density also increases the recombination rate within this layer, mainly due to Auger recombination, here a compromise for the doping density has to be made. Most kinds of dielectric passivation layers exhibit a combination of the saturation of surface defects and fixed charges. In conventional solar cells, e.g., in a PERC solar cell, the metal contacts are in direct contact to the Si wafer, so that on this area the dielectric passivation layer has to be removed. In contrast to the passivation layers, the metal usually increases the amount of surface defects. In order to reduce the contact recombination usually a doped layer is created under the contacts.

For the case of poly-Si contacts, the surface defects are passivated by an interfacial SiO_x layer and an electric field is created by a highly doped poly-Si layer on top of the oxide. Figure 3.1 a) shows a sketch of the band diagram of a metal / n+ poly-Si / n c-Si junction. While one type of charge carriers (here electrons) can pass the oxide and be collected by the metal, the other charge carrier type (here holes) is blocked and therefore, can not recombine at the defects in the poly-Si layer and at the metalized surface. The interface oxide with the low interface defect density, together with the bend bending caused by the high doping density in the poly-Si layer reduces the recombination at the interface. It is

ideally assumed that nearly no minority charge carriers can reach the poly-Si layer (see next section), therefore the recombination properties of this layer itself can be ignored. In contrast to a doped layer in the silicon wafer, a strong doping in the poly-Si does not result in enhanced recombination. As a consequence the doping density can be chosen as high as practically possible.

3.1.2. Transport

In contrast to the passivation mechanism, the transport mechanism of the poly-Si contact is not well understood. Since the first observation of an increased current gain in bipolar junction transistors until now several models have been proposed to explain this behavior:

- The grain boundary model [72]–[74] explains the reduction of the recombination by a reduced mobility at the grain boundaries of the poly-Si and at the poly-Si / *c*-Si interface.
- The segregation model [75]–[77] uses a segregation of dopants at the poly-Si / *c*-Si interface and the resulting potential barrier to explain the reduction of the recombination.
- The oxide tunneling model [78]–[80] uses different band offsets between SiO_2 and Si and therefore different tunneling properties for electrons and holes to explain the carrier selective transport through the interface oxide.
- The pinhole model [66], [81], [82] postulates a transport through tiny disturbances in the interface oxide and explains the carrier selectivity with doped regions under the pinholes.

While the grain boundary model and the segregation model, both do not need an interface oxide to explain the carrier selectivity, it has been shown [36]–[39], [83], that the interface treatment with oxidizing solutions, or HF to remove oxides, has a strong impact on the performance of poly-Si contacts. In newer publications, both models are not mentioned any more.

In recent literature the most common assumption is that the transport is dominated by tunneling of charge carriers through the oxide [52]–[54], [56], [80] (see figure 3.1 for the case of a n^+ poly-Si / n *c*-Si junction). One assumption often made to model bipolar $n/p/n$ transistors with poly-Si contacts is that the tunneling barrier is lower for electrons than for holes, with the result that the electron transport is not affected very much by the oxide, whereas the hole transport and therefore the recombination is strongly reduced. For example, often values of 0.3 eV for the tunneling barrier height of the electrons and 1 eV for the tunneling barrier height of the holes are assumed [38], [39]. In contrast, the

experimentally determined conduction band offset between silicon and silicon dioxide has a value of 3.2 eV and the valence band offset a value of 4.7 eV [84]. As already pointed out by Post *et al.* [38] if this assumption would be true, poly-Si contacts would be detrimental for $p/n/p$ transistors, which is contrary to the observations that $p/n/p$ transistors also benefit from poly-Si contacts [45], [85], [86] and also to the finding of low $J_{0,\mathrm{poly}}$ values for both, p- and n-type poly-Si contacts in the work of Gan and Swanson [81].

In a recent publication of Steinkemper *et al.* [80] the n-TOPCon layers together with n-type poly-Si layers were investigated by means of numerical device simulations. Even though the tunneling barrier heights used by the authors are not explicitly stated in the paper, the diagrams imply that "real" (consisting with experimentally determined values) band offsets have been used. Nevertheless, one main parameter that was adapted in order to match the simulations with their experiments was the effective tunneling mass ($m_{\mathrm{t,e}}$ for electrons and $m_{\mathrm{t,h}}$ for holes) in SiO_2. The authors state that literature values range from 0.3 to 0.95 m_0 (where m_0 is the electron rest mass) and write that values of $m_{\mathrm{t,e}} = m_{\mathrm{t},} = 0.4\, m_0$ were "found to describe the experimentally determined cell results quite well". Unfortunately in this publication, the model has not been applied to p-TOPCon or p-type poly-Si layers. Future publications may show, if the model is applicable for both polarities with one set of input parameters.

The pinhole model assumes that the transport through the oxide is not dominated by tunneling, but rather by ohmic transport through tiny pinholes in the oxide layer, leading to a direct contact between poly-Si and c-Si. The first evidences for pinholes in the interface oxide have been observed in the 80's by transmission electron microscopy (TEM) investigations of poly-Si contacts [39], [87], [88]. The investigations have shown that a thermal treatment of the contacts can result in a "breaking up" of the oxide and, depending on the thermal budget, the breaking up can result in small pinholes with a diameter of ~ 1 nm, or in extreme cases, in a nearly complete disintegration of the oxide [87]. Gan and Swanson suggested that depending on the size and density of these pinholes, the transport through the pinholes should be much higher than the transport due to tunneling [81]. Hamel et al. [82] used two-dimensional network simulations to verify that very low contact resistances are possible even with a low fraction of broken up area, if there are many small pinholes. With the aim to show that a density of pinholes, high enough for a low contact resistivity, can simultaneously provide low contact recombination, Peibst *et al.* [66] performed analytical calculations of an idealized poly-Si contact. The work shows that based on the assumption of circular pinholes in the oxide and semi-spherical highly doped regions in the underlying c-Si layer, it is possible to obtain pairs of low contact resistance and contact recombination, compatible with the excellent values of the work of Gan and Swanson [81].

With the assumption that semi-spherically doped regions are formed under the pinholes, a poly-Si contacted solar cell becomes in principal similar to the rear side of a PERC solar cell (see figure 1.1 and the description in the introduction): The major part of the surface is passivated and at the contacted regions a strong diffusion leads to a carrier selectivity by depleting one carrier type and accumulating the other carrier type. The major difference to a PERC cell is the decoupling of the metal contact from the wafer surface: In PERC solar cells the relatively high contact resistance of Al to Si ($3\,\mathrm{m\Omega\,cm^2}$ for highly doped Al-BSFs [89], [90]) limits the minimal contact area fraction to typically 10 % [89]. In contrast for poly-Si contacts, the metalization can be applied on a large area of the poly-Si layer, while the contact resistance is limited by the series resistance through the highly doped Si in the small oxide pinholes, so that much lower "contact" area fractions are possible (much less than 1 %, possibly $\sim 0.01\,\%$ [66]). The lower contact area fraction not only leads to a reduced recombination at the contacts, but also to reduced recombination in the highly doped regions under the contacts. While a typical PERC contact exhibits large (typically 3 - 6 μm thick [91]) highly recombinative Al-BSFs (see table 1.1), a poly-Si contact consist of many small (radius of $\sim$0.1 - 1 μm) phosphorus or boron doped regions with only negligible total Auger recombination in the doped area.

Summarizing, both models, the oxide tunneling model and the pinhole model can be used to explain the carrier selectivity of poly-Si contacts. In this work, the pinhole model is favored, because it seems to be universally applicable, where the oxide tunneling model might have some weaknesses.

3.2. Measurement techniques

3.2.1. Photoconductance decay

The photoconductance decay (PCD) technique [92], [93] is a fast method for the determination of the effective charge carrier lifetime τ_{eff} for a wide range of excess charge carrier densities Δn. This offers the possibility to compare the lifetimes of different samples at a fixed injection level and also to obtain information about other important parameters. E.g. the recombination at highly doped surfaces can be extracted from the injection dependence in high level injection (HLI) and typical implied IV parameters can be obtained by calculating a suns vs. implied open circuit voltage (suns($V_{\mathrm{oc,impl}}$)) curve from the $\tau(\Delta n)$ curve [94].

In this work a Sinton Instruments WCT-120 lifetime tester is used for the PCD-measurements. The measurement setup is sketched in 3.2. A test structure is placed on a temperature controlled table, while the conductance of the sample is measured by a coil that is part of an RF-bridge. The lifetime of the sample is measured by generating excess

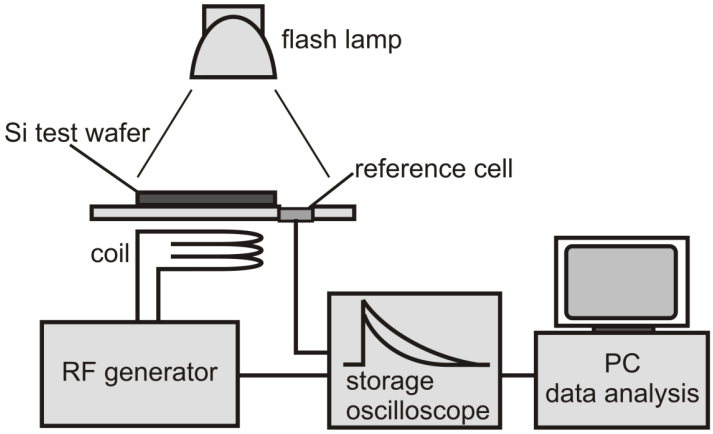

Figure 3.2.: Sketch of the PCD measurement setup taken from [95].

charge carriers with a short flash. Both, the light intensity and the sample conductance are recorded over time. Due to the generation of excess charge carriers, the conductance is enhanced and after the flash is over, the conductance decreases again. The excess charge carrier density Δn can be calculated from the photoconductance by

$$\Delta\sigma = q\,W(\mu_\mathrm{n} + \mu_\mathrm{p})\Delta n \ , \tag{3.1}$$

where $\Delta\sigma$ is the photoconductance, obtained by subtracting the dark conductance from the measured conductance, q is the elementary charge, W the sample thickness and μ_n and μ_p are the electron and hole mobilities, respectively. The effective lifetime of the sample can then be calculated by

$$\tau_\mathrm{eff} = \frac{\Delta n}{G - \partial\Delta n/\partial t} \ , \tag{3.2}$$

where G is the photogeneration. For a transient measurement, where a short flash with a decay time ($\sim 30\,\mu$s) much smaller than the lifetime of the sample is used, the generation can generally be neglected for the evaluation of the measurement data. For an alternative measurement mode, the quasi steady state photoconductance decay (QSSPC), where a longer flash (decay time $\sim 25\,$ms) is used, or for the evaluation under HLI, where the light intensity is still larger than zero, the photogeneration has to be taken into account. The generation is obtained with

$$G = \frac{J_\mathrm{gen}}{qW} \ , \tag{3.3}$$

where the generation current density J_gen is the light intensity in units of suns, obtained by a calibrated reference cell, multiplied with an idealized short circuit current density and

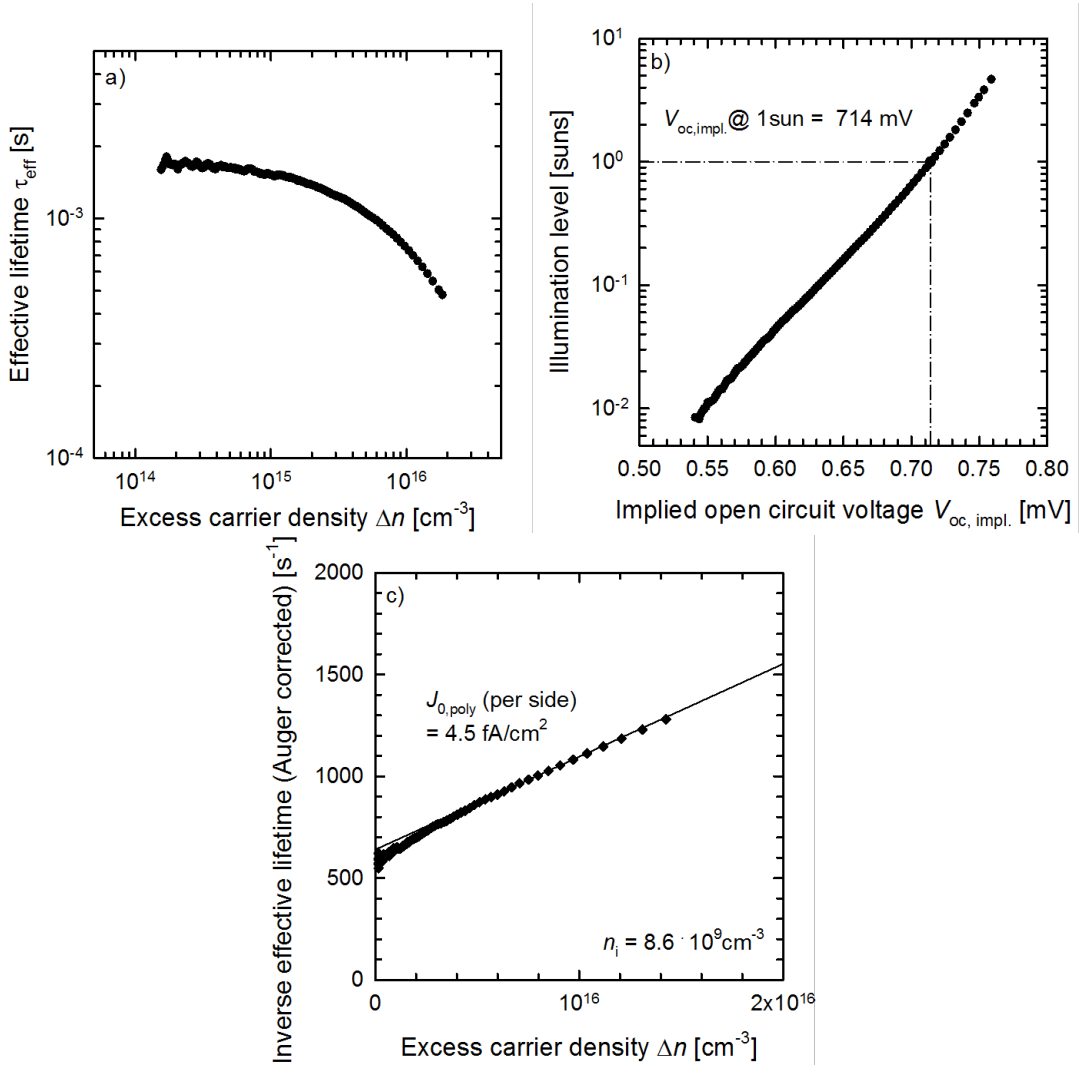

Figure 3.3.: Example of a PCD measurement of a poly-Si contacted test structure, composed of data from a transient and a quasi steady state measurement a) $\tau_{\mathrm{eff}}(\Delta n)$ curve, b) suns($V_{\mathrm{oc,impl}}$) curve and c) $J_{0,\mathrm{poly}}$ determination with the method of Kane and Swanson.

an optical factor to account for the reflectivity of the sample. An example of a measured $\tau_{\text{eff}}(\Delta n)$ curve is shown in figure 3.3 a.

As some of the processes responsible for the recombination in the sample can be modeled by diode equations (see equation 1.2) it is often helpful to translate the $\tau_{\text{eff}}(\Delta n)$-curve into a recombination current-over-implied open circuit voltage ($V_{\text{oc,impl}}$)-diagram. The recombination current is calculated with

$$J = \frac{q\,W\Delta n}{\tau} \tag{3.4}$$

and the implied open circuit voltage with

$$\frac{n\,p}{n_{\text{i}}^2} = \exp(\frac{qV}{kT}) \ , \tag{3.5}$$

where n and p are the electron and hole densities, respectively, n_{i} is the intrinsic charge carrier density, k is the Boltzmann constant and T the sample temperature. Often, for this type of diagrams, the generation in suns is plotted on the Y-axis instead of the recombination current, resulting in a suns($V_{\text{oc,impl}}$) curve. The suns are calculated by again making use of the optical factor of the sample. An example of a measured suns($V_{\text{oc,impl}}$) curve is shown in figure 3.3 b.

For samples exhibiting a surface diffusion or a passivation layer that enhances the carrier density at the surface e.g., due to fixed charges or, as in the case of poly-Si contacts, a doped Si layer, the surface saturation current density $J_{0,\text{surf}}$ can be extracted with the method of Kane and Swanson [96]. The basic principle of this method is to use the $\tau_{\text{eff}}(\Delta n)$ data of the PCD measurement at $\Delta n > 10 \times N_{\text{dop}}$, so that the base is in high level injection (HLI) and the surface recombination term becomes

$$J_{\text{surf}} = J_{0,\text{surf}}\frac{\Delta n^2}{n_{\text{i}}^2} \ [96] \ . \tag{3.6}$$

Equation 3.6, together with equation 3.4 can be inserted in the following equation:

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{bulk}}} + \frac{1}{\tau_{\text{Auger}}} + \frac{1}{\tau_{\text{surf}}} \ , \tag{3.7}$$

where τ_{eff} is composed of τ_{bulk}, the Schockley Read Hall (SRH) lifetime of the bulk, τ_{Auger}, the lifetime implied by the Auger and radiative recombination, and τ_{surf}, the lifetime implied by the surface recombination. The resulting equation

$$\frac{1}{\tau_{\text{eff}}} - \frac{1}{\tau_{\text{Auger}}} = \frac{1}{\tau_{\text{bulk}}} + 2J_{0,\text{surf}}\frac{\Delta n}{qWn_{\text{i}}^2} \ , \tag{3.8}$$

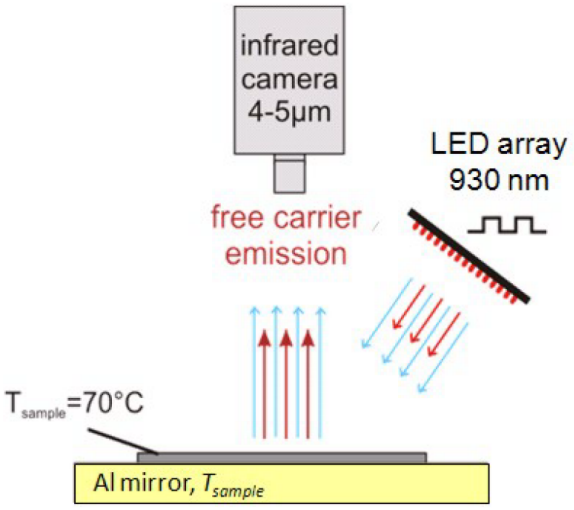

Figure 3.4.: Sketch of the dyn.-ILM setup taken from [98]. The sample is placed on a heated infrared mirror and excess charge carriers are generated by an LED array. A camera records the infrared emission of these free charge carriers.

can then be used to extract $J_{0,\mathrm{surf}}$ from the slope of the Auger corrected $1/\tau_{\mathrm{eff}}(\Delta n)$ curve. An example is shown in figure 3.3 c.

3.2.2. Dynamic infrared lifetime mapping

In order to obtain information about the lateral lifetime distribution of silicon wafers, the dynamic infrared lifetime mapping (dyn.-ILM) method [97] can be used. For this method the infrared emission of the free charge carriers of a sample is measured by an infrared camera (see measurement setup in figure 3.4). Images are collected at different times while switching on and off a LED light source. With this approach the effective lifetime can be obtained calibration free from the transient behavior of the excess charge carriers. To increase the signal to noise ratio, the measurements used in this work are performed at a temperature of 70 °C. A more detailed description of the method can be found in [97].

3.2.3. Photoconductance-calibrated photoluminescence lifetime imaging

The photoconductance-calibrated photoluminescence lifetime imaging (PC-PLI) method is another camera based method to measure the lifetime distribution of a Si sample. Excess charge carriers are generated with an infrared diode laser beam, that is widened and homogenized, while the photoluminescence (PL) signal is detected by a Si CCD camera. The reflected laser excitation light with a central wavelength of 808 nm is blocked by

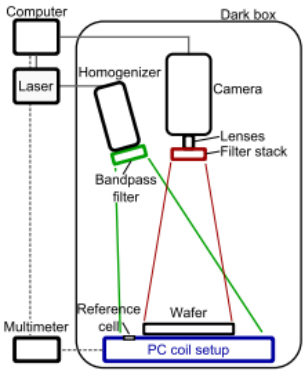

Figure 3.5.: Sketch of the PC-PLI setup taken from [99]. The sample is placed on a PCD table and excess charge carriers are generated by an homogenized laser. A camera records the luminescence of the sample.

a stack of filters, while the band-to-band photoluminescence can pass the filters. The detected PL signal I_{PL} can be converted into the excess charge carrier density by

$$I_{\mathrm{PL}} = C_{\mathrm{PL}}(\Delta n N_{\mathrm{dop}} + \Delta n^2), \tag{3.9}$$

where N_{dop} is the doping density of the sample and C_{PL} depends on the specific optical properties of the measurement setup and the sample. In order to obtain C_{PL} the carrier density of the sample can be measured with the coil of the PCD table for different laser intensities. The resulting curve of the average PL signal in the coil-region over the measured excess charge carrier density should resemble a second order polynomial, where fitting gives the C_{PL}-value. The lifetime is calculated analogously to the PCD measurements (see equation 3.2), but as the laser intensity is constant during each measurement, the time derivative term $\frac{\partial \Delta n}{\partial t}$ in equation 3.2 is omitted. Further details on the method can be found in [99].

3.2.4. Lifetime measurements in this work

Generally all samples in this work have been characterized with the PCD technique, as it is a fast technique and in many cases it provides all lifetime information needed to evaluate the electrical potential of the investigated test structures. Nevertheless, most of the samples have been characterized additionally with the dyn.-ILM method, to investigate the lateral homogeneity. Many of the characterized samples did exhibit small point-like areas that are likely process-induced and no feature of the special test structure (see the example in figure 3.6 a)). For a better comparability of the PCD-data of these test structures, a region without these artifacts has been chosen for the PCD measurements.

In contrast to the PCD and dyn.-ILM measurements a PC-PLI measurement is much more time-consuming. Therefore, it is only used as a substitute for PCD measurements

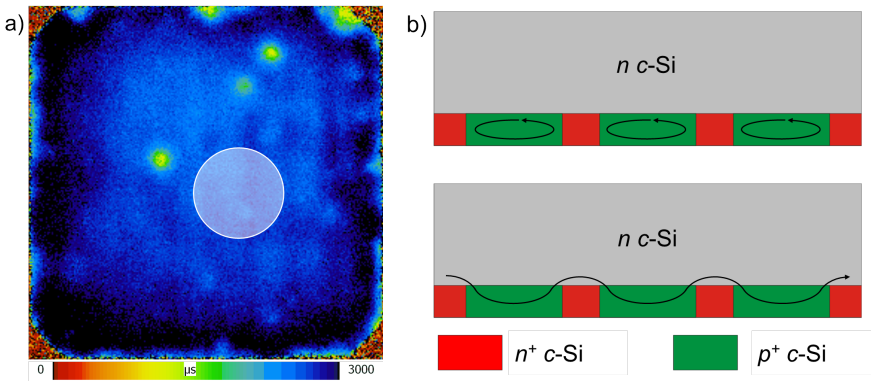

Figure 3.6.: a) Example of a typical dyn.-ILM measurement performed on a poly-Si passivated test structure based on a 156 mm × 156 mm large wafer. The white filled circle indicates the position, where the PCD measurement is performed in order to omit the statistical influence of small low lifetime regions. b) Schematic of the current flow during PCD measurement on a laterally inhomogeneous doped test structure. For the non-illuminated sample (upper picture) the hole eddy current is restricted to the single p^+ regions. For the illuminated case (lower picture), where holes are injected into the base, the p^+ regions become electrically connected, resulting in a completely different hole eddy current flow.

for some samples that can not be characterized properly with coil-based methods. In this work this is the case for laterally inhomogeneously doped test structures: Holst [100] and Juhl *et al.* [101] have observed, that PCD measurements on test structures with laterally alternating doping polarity can result either in an underestimation [100] or an overestimation [101] of the lifetime. Figure 3.6 b) shows a wafer with such a problematic structure. The inaccuracies are most probably caused by different paths of the minority charge carrier eddy current (in the picture the holes) in the dark and in high injection. In the dark the resistivity of the separated highly doped regions is underestimated, while it is measured correctly in high injection. During the transition from the wrong measurement regime to the correct measurement regime the evaluation of Δn and therefore also of τ_{eff} will be incorrect. Thus, for these test structures, references with similar thickness, substrate doping and front side processing, but a homogeneously doped rear side are used to calibrate the PL signal and the inhomogeneously doped test structures are then measured with this calibration.

3.2.5. Electrochemical Current Voltage

The electrochemical current voltage (ECV) technique is a method for the determination of doping profiles. The doping density is obtained by a determination of the capacitance of the space charge region (SCR) of a semiconductor electrolyte contact. The depth profile is

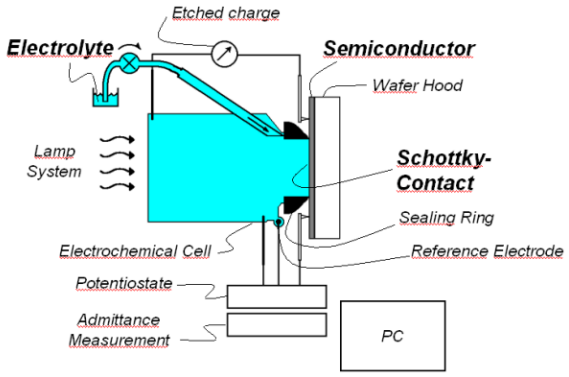

Figure 3.7.: Schematic of the ECV measurement setup, taken from [102].

achieved by sequentially electrochemically etching the sample. The measurment setup is shown in figure 3.7.

Describing the capacitance of the SCR region as a plate capacitor, the voltage dependent capacitance $C(V)$ can be described by the Mott equation:

$$\frac{1}{C^2} = \frac{-2}{e\epsilon_0\epsilon_\mathrm{R}A^2N}(V - V_\mathrm{fb}) \ , \tag{3.10}$$

where e denotes the elementary charge, ϵ_0 the vacuum permittivity, ϵ_R the relative permittivity of the sample, A the electrolyte-semiconductor contact area, N the charge carrier concentration and V_fb the flat band potential.

By varying the applied voltage, N can be determined from the slope of the $1/C^2$ curve by

$$N = \frac{-2}{e\epsilon_0\epsilon_\mathrm{R}A^2\frac{d(1/C^2)}{dV}} \ . \tag{3.11}$$

The electrochemical etching is performed with a 0.1 molal NH_4F solution. As for the etching process holes are needed at the semiconductor surface, a light source can be used to create electron hole pairs for the measurement of n-type surfaces.

Further information on ECV measurements can be found in the review article of Blood [103].

3.2.6. Four point probe

The four point probe (4PP) is a tool for the measurement of resistivities. In particular it can be used to measure the sheet resistance of a thin layer at a surface. The measurement setup consists of four probes in a row that are brought into contact with a sample. During the measurements a current is forced through the two outer probes, while the resulting

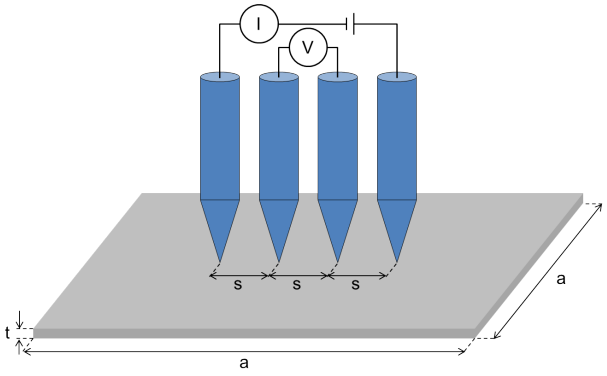

Figure 3.8.: Schematic of a 4PP measurement setup, showing the arrangement of the probes and the connection of the current source I and the voltmeter V.

voltage between the two inner probes is measured (see figure 3.8). If the probes are equidistant, the sheet resistivity can be calculated by

$$\rho_{\mathrm{s}} = \frac{V}{I} \cdot \frac{\pi}{\ln 2} \text{ [104]}, \tag{3.12}$$

if the requirements $a \geq 40s$ and $t \leq s/2$ are fulfilled, with a denoting the diameter of a circular sample or the width of a square sample, t the thickness of the sample and s the distance between the probes. If these requirements are not fulfilled, correction factors have to be applied to account for changed current paths [92], [104].

3.2.7. Qualitative determination of the interface contact resistance

Generally most methods to measure the contact resistance require more or less complex test structures, exhibiting structured metal-contacts and for accurate measurements also structured poly-Si areas. Further, most methods require, in one or the other way, a subtraction of the wafer conductance from the measured conductance. Therefore, in order to improve the measurement accuracy, samples with a low base resistivity are required, making the use of lifetime test structures with a generally rather high base resistivity unsuitable for further processing to contact resistance test structures.

Therefore in this work a new, fast and non-destructive method for the evaluation of the interface contact resistance between to layers has been developed. By comparing sheet resistances measured with the 4PP technique with sheet resistances measured inductively (with the PCD setup, see figure 3.2), a qualitative statement on the contact resistance can be made. With the inductive measurements, performed with the Sinton lifetime tester used also for PCD measurements, the total sheet resistance of the test structure R_{tot} i.e. the reciprocal sum of the sheet resistances of the wafer R_{bulk} and the sheet resistances of the poly-Si layers R_{poly}, is measured. By determining R_{bulk} on references without poly-Si, the

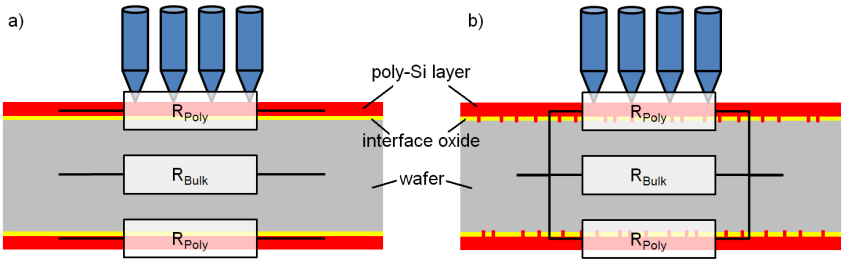

Figure 3.9.: Schematic drawing of a four point probe measurement on a J_0 test structure and the corresponding equivalent circuit diagram a) for the case of a well-insulating interface oxide and b) for a low interface contact resistance, indicated by holes in the interface oxide.

value of R_{poly} can be calculated. On test structures with a well-insulating interface oxide between the poly-Si layer and the wafer, a 4PP measurement will result in a measured value R_{4PP} comparable to R_{poly} (see figure 3.9 a)). On test structures with a negligibly low interface contact resistance, the 4PP measurement will yield a value R_{4PP} comparable to R_{total} (see figure 3.9 b)). For an easier comparison, the results of 4PP measurements on test structures with different sheet resistances are normalized by defining a relative contact resistance ρ_{rel} that becomes zero for $R_{\mathrm{4PP}} = R_{\mathrm{total}}$ and one for $R_{\mathrm{4PP}} = R_{\mathrm{poly}}$:

$$\rho_{\mathrm{rel}} = \frac{R_{\mathrm{4PP}} - R_{\mathrm{total}}}{R_{\mathrm{poly}} - R_{\mathrm{total}}} \tag{3.13}$$

3.2.8. Improving the qualitative determination with device simulations

With the method discussed above it is not possible to state how low the interface contact resistance has to be in order to obtain a low value of ρ_{rel} and how high it is for a value near one. In order to get quantitative informations from these measurements, 3D device simulations of the 4PP measurements have been performed with SENTAURUS DEVICE [105]. The simulation has been set up with a graphical user interface (GUI) programmed with the software MATLAB. The simulation domain consists of a $1\,\mathrm{mm} \times 4\,\mathrm{mm}$ large part of a wafer with the thickness and resistivity of the test structure used in the experiment. With the applied GUI the implementation of a contact resistivity is only possible at metal contacts and not between two touching regions in the device. Therefore the contact resistance between poly-Si and wafer is implemented by applying a thin layer with high resistivity on both sides of the wafer, representing the oxide. On top of the oxide layers, regions with a lower resistivity corresponding to the poly-Si layers are added. On one side of the structure, four metal contacts with a distance of 1 mm between neighboring contacts are attached onto the top layer, corresponding to the four probes of the 4PP setup used in the experiments.

An exact physical representation of the experimental test structure is hardly possible in the simulations. First, the current transport mechanism across the interfacial oxide is not fully understood so far. A physically correct reproduction of the experiment would require the modeling of the oxide as a stoichiometric SiO_2 layer (described by band offsets, relative dielectric constant, effective masses etc.) and the application of tunneling models. Also the description of oxide pinholes with a dimension of few nanometers but an area density of $\sim 10^7\,\mathrm{cm}^{-2}$ would require a non-feasible meshing. Additionally, the doping levels and charge carrier mobilities in the poly-Si layers are not exactly known. Beyond the technical problems of an exact simulation of the microscopic processes, here the important property for the valuation of the poly-Si layers is the macroscopic interface contact resistance. Therefore the test structure is simplified by modeling both, the poly-Si layer and the interface oxide as "silicon". The thicknesses of the oxide and the poly-Si layers are set to 10 nm and 10 μm respectively. Lower and more realistic values have been seen to cause inconsistent sheet resistances or contact resistances in test simulations. These are possibly caused by the high mobility offsets and meshing problems at the boundaries. The unrealistic input parameters are supposed to cause only minor inaccuracies, as the current flow through the oxide region will be approximately one-dimensional and therefore only the product of oxide thickness and mobility is important for the contact resistance, while lateral currents can be neglected. Contrarily, the current flow in the poly-Si region is on the large scale nearly only lateral, so only the quotient of mobility and thickness i.e. the sheet resistance is important for the current flow, while currents in the z-direction can be neglected. For further simplicity a constant doping density is used for all layers. The sheet resistance of the poly-Si layer and the interface contact resistance are defined by varying the respective charge carrier mobilities in the poly-Si and oxide layers.

The macroscopic current flow during a 4PP-measurement can now be modeled by setting the potential between the outer two metal contacts so that a current of 0.1 mA is forced through these contacts and by setting the potential of both inner contacts so that no current is flowing through these contacts. The calculation of $R_{4\mathrm{PP}}$ is done with the formula for small samples:

$$R_{4\mathrm{PP}} = V/I \cdot C \text{ [104]}, \tag{3.14}$$

where V is the potential difference of the two inner probes, I the current through the outer two probes and C is a correction factor, dependent on the sample geometry. In these simulations the simulation domain has a width of s and a length of $4\,s$, where s is the distance between two adjacent probes. The resulting correction factor C then amounts to a value of 0.9994 [104]. In the experiment, the measured area is much larger, therefore $R_{4\mathrm{PP}}$ can be calculated with the approximation for infinite sample size:

$$R_{4\mathrm{PP}} = V/I \cdot \pi/\ln(2) \text{ [104]}. \tag{3.15}$$

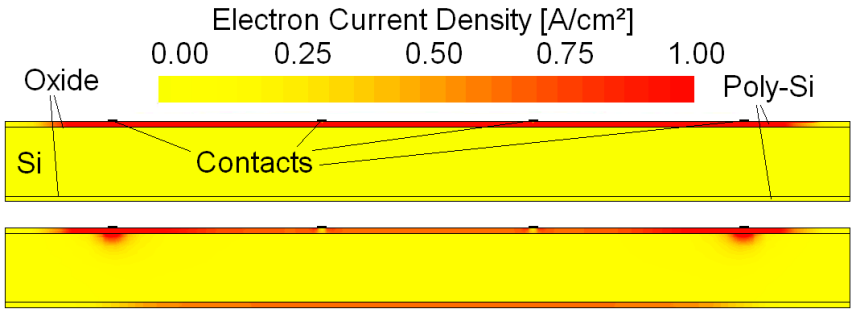

Figure 3.10.: Cut through the middle of the simulation domain, showing the current density distribution for a test structure with a high interface contact resistance (upper figure) and for a test structure with a low interface contact resistance (lower figure). In the upper figure the current density is highest in the front poly-Si layer, while in the lower figure also a significant current is flowing through the rear poly-Si layer and (less visible) through the bulk.

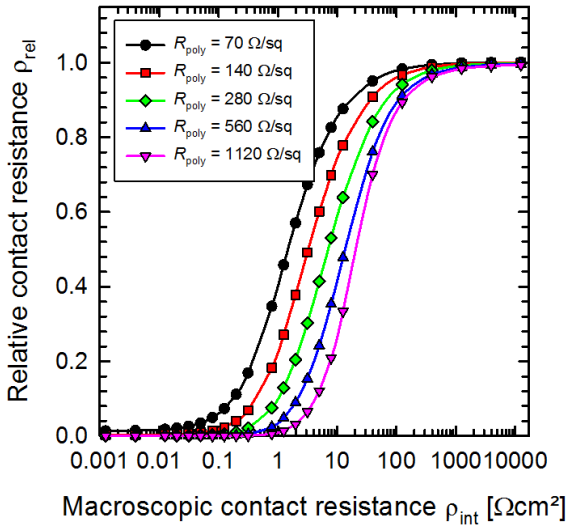

Figure 3.11.: Relative contact resistance ρ_{rel} obtained by simulating 4PP measurements of a 150 μm thick test structures with a base resistivity of 9 Ω cm. Varied are the interface contact resistance ρ_{int} and the poly-Si sheet resistance R_{poly}. The lines are guides to the eye.

In figure 3.10 the current distributions for the extreme cases of a test structure with a high interface contact resistance (upper figure) and a low interface contact resistance (lower figure) are depicted. In the first case the current flows only through the upper poly-Si layer, and in the second case also through the wafer and the lower poly-Si layer. The calculated relative contact resistance values of simulations with varying interface contact resistance are plotted in figure 3.11 for test structures with poly-Si sheet resistances between 70 and 1120 $\Omega/\square$. Here, the thickness of the wafer is 150 μm and the resistivity is 9 Ω cm. For these test structures a value of ρ_{rel} below 0.05 corresponds to an interface contact resistance ρ_{int} between 0.1 and 5 $\Omega\,\mathrm{cm}^2$, depending on the sheet resistance of the poly-Si

layer. For lower values of ρ_{int} the relative contact resistance value saturates. Therefore, for these test structures only an upper limit for the contact resistance can be given. For a more precise determination of ρ_{int} more complicated methods are required.

Chapter 4

Polycrystalline / monocrystalline silicon junctions

In this chapter the key features influencing the properties of poly-Si contacts are evaluated. In section 4.1 chemically and thermally grown oxides are fabricated, the former with different chemical baths, and the latter with varying processes, leading to different thicknesses. Further, the annealing process and the doping mechanism ($POCl_3$ or BBr_3 furnace diffusion) are varied. In section 4.2 the process order of the annealing step and the doping step is investigated. Section 4.3 reports on the influence of the dopant density in the poly-Si layers on the device performance, especially on the passivation quality. Section 4.4 gives a more in depth analysis of the injection dependent lifetime and the implied IV-curves of some of the optimized poly-Si test structures in order to identify the limiting recombination sources. After the optimization of the poly-Si deposition parameters, the influence of metalization processes will be investigated in section 4.5 by means of dyn-ILM measurements. In section 4.6, solar cell demonstrators are fabricated in order to demonstrate the high V_{oc} potential of the poly-Si contacts and to verify the low contact resistances on device level. In section 4.7, results from structural investigations with the aim to detect pinholes in the interface oxide layer are shown. Finally, in section 4.8 numerical simulations of poly-Si contacted wafers are conducted.

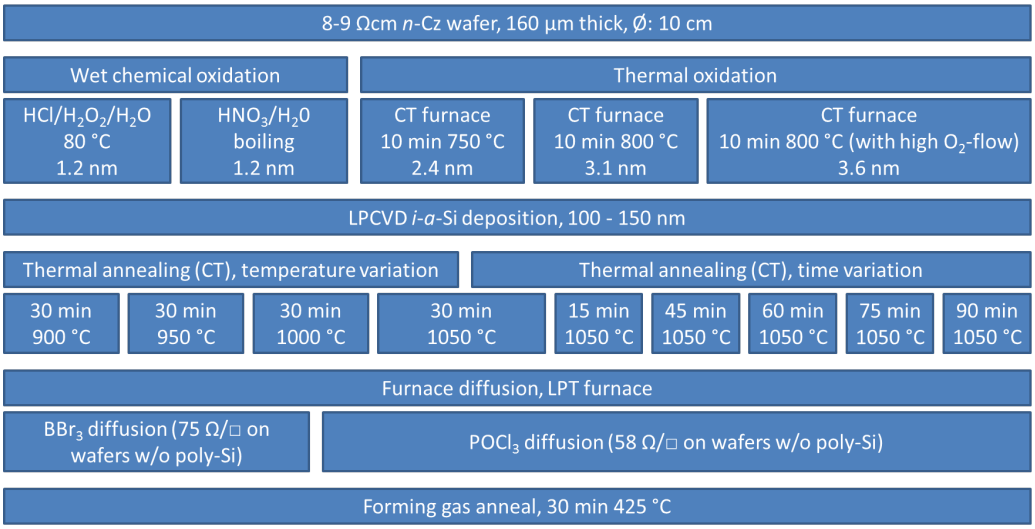

Figure 4.1.: Simplified process flow for the fabrication of poly-Si test structures with different oxide types and thicknesses. Also varied are the annealing process and the doping mechanism ($POCl_3$ or BBr_3 furnace diffusion).

4.1. Influence of the interface oxide type on the properties of the poly-Si contact

As described earlier (see section 3.1), the interfacial oxide is an important feature of the poly-Si contact. It is responsible for the low interface defect density between oxide and wafer. Kerr *et al.* [68] have shown that with thermally grown oxides very low interface defect densities can be obtained. Schmidt *et al.* [69] also used thin thermally grown oxides and Yeng *et al.* [106] thin wet chemically grown oxides under a SiN_x passivation layer to enhance the passivation quality of the layer. Due to the low oxygen diffusion constant in SiO_2, chemically grown oxides usually exhibit only low thicknesses $< 2\,\mathrm{nm}$. Using thermal growth processes, thicker oxides can be obtained due to the increase of the diffusion constant at higher temperatures [107].

In order to investigate different ways to fabricate the interface oxide, test structures with otherwise identical features are fabricated. The process flow for the samples is shown in figure 4.1; a detailed list of the varied process steps and of the measurement results of each sample shown in this section can be found in the tables A.2 and A.1 in Appendix A. For this experiment 160 μm thick n-type Czochralski grown (Cz) silicon wafers with a diameter of 10 cm and a resistivity of $8 - 9\,\Omega\,\mathrm{cm}$ (after high temperature processing) have been used. After saw-damage etching and RCA cleaning, the oxide is grown either in a wet chemical bath, or in an oxidation furnace. The bath consists in one case of a standard cleaning solution containing HCl and H_2O_2 and in the other case of a HNO_3 solution. The resulting thickness of these oxides is for both solutions determined to 1.2 nm by ellipsometry and

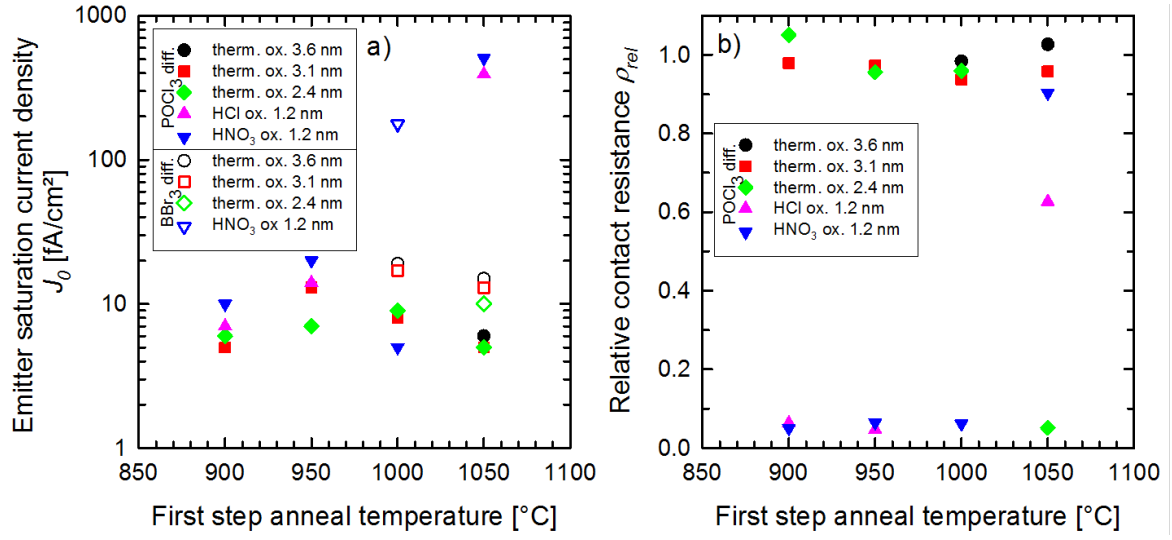

Figure 4.2.: a) J_0 and b) ρ_{rel} values of poly-Si test structures with different wet-chemically and thermally grown interface oxides, annealed for 30 min at different temperatures. Results for n-type (filled symbols) and p-type (open symbols) poly-Si layers are shown.

TEM measurements. The thermal oxides are fabricated with different processes resulting in oxide thicknesses of 2.4 nm to 3.6 nm. Subsequently, 100 - 200 nm thick layers of undoped amorphous silicon are deposited in a low pressure chemical vapor deposition (LPCVD) furnace, followed by a high temperature annealing step in an oxidation furnace in nitrogen atmosphere. The plateau temperature and the corresponding process durations are varied. Doping of the poly-Si layers is conducted either by a $POCl_3$ or a BBr_3 based furnace diffusion step resulting in n- and p-type poly-Si layers, respectively. The target sheet resistances on wafers without poly-Si are 58 Ω/□ and 75 Ω/□ for the $POCl_3$ and the BBr_3 diffusion, respectively. After forming gas annealing (FGA) the saturation current density and relative contact resistance of the test structures are determined.

Figure 4.2 a) shows for various oxide types the influence of the annealing temperature on the J_0 values of the test structures. Here the annealing duration is fixed to 30 min. The lowest J_0 values are achieved for thermally grown oxides. All samples with thermal oxides reach J_0 values below 20 fA/cm² for all temperatures investigated. In contrast, for the samples with a chemical oxide, J_0 increases to values larger than 300 fA/cm² at temperatures $\geq$ 1050 °C (n-type poly-Si). The J_0 value of the boron doped sample with a chemical oxide is already increased at 1000 °C.

Figure 4.2 b) shows the values of ρ_{rel} for the same samples, determined by the method described in section 3.2.7 and section 3.2.8. As only n-type wafers have been used in this experiment, only the ρ_{rel} values of the n-doped poly-Si layers could be determined. For temperatures between 900 °C and 1050 °C, the ρ_{rel} values remain close to one for almost all samples with a thermal oxide. The only exception is the sample with the lowest oxide

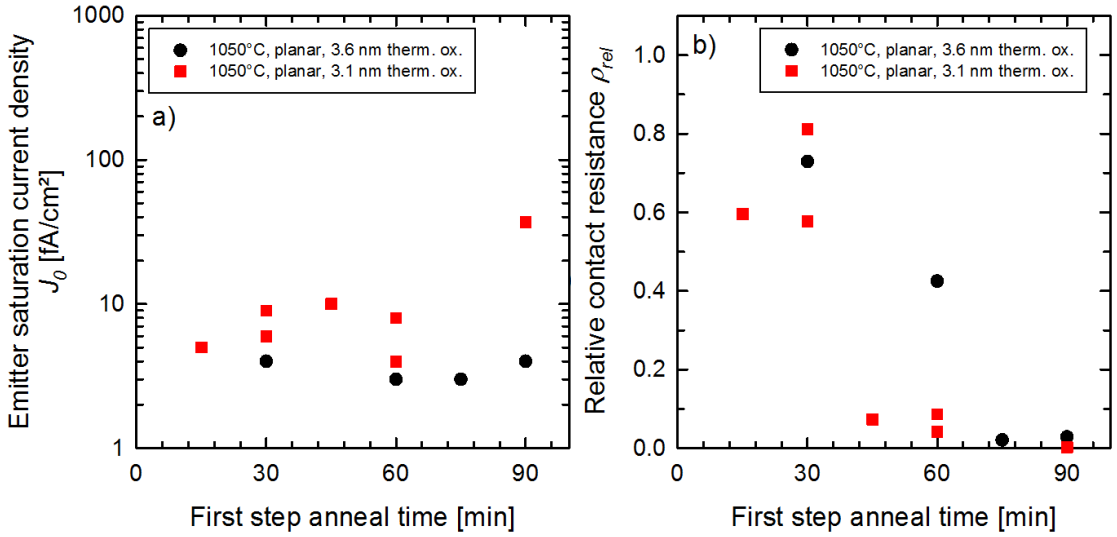

Figure 4.3.: a) J_0 and b) ρ_{rel} values of poly-Si test structures with different thermally grown interface oxides, annealed at 1050 °C for varied durations (all n-type poly-Si).

thickness of 2.4 nm, for which ρ_{rel} drops to almost zero at 1050 °C. For the chemical oxides, all samples show a low relative contact resistance up to a temperature of 1000 °C and an increase at higher temperatures.

Annealing temperatures above 1050 °C are not possible with the available furnaces, therefore, in order to obtain low contact resistances, the samples with the 3.1 nm and 3.6 nm thick oxides are additionally annealed for longer durations at 1050 °C. Figure 4.3 shows the corresponding J_0 and ρ_{rel} values of these test structures. For durations up to 60 min, the J_0 values are equal or below 10 fA/cm^2. For higher annealing durations J_0 increases for the 3.1 nm thick oxide. The value of ρ_{rel} on the other hand decreases with increasing annealing duration, reaching values close to zero after 45 min and after 75 min for the 3.1 nm and 3.6 nm thick oxides, respectively.

The decrease of the interface contact resistance at high thermal budgets has also been observed by other researchers (see section 2). While not commented in other works, it supports the theory that the current transport across the junction is dominated by a current flow through pinholes in the oxide and that high temperatures are important for the “cracking” of the oxide, at least for the samples with thermally grown oxides. The increase of the interface contact resistance of the samples with chemically grown oxides at 1050 °C annealing temperature is unexpected and cannot be explained either with tunneling or pinholes in the oxide. The high J_0 values of these samples indicate that the interface properties are substantially degraded. This could go hand in hand with the disintegration of the oxide on larger scale, together with strong in-diffusion of dopants,

oxide type	thermal budget	relative contact resistance	"combined" contact resistance
thermal oxide 2.4 nm	30 min 900 °C	1.05	$56 \pm 10\,\Omega\,\mathrm{cm}^2$
thermal oxide 2.4 nm	30 min 1050 °C	0.051	$0.10 \pm 0.01\,\Omega\,\mathrm{cm}^2$
thermal oxide 3.1 nm	60 min 1050 °C	0.042	$0.07 \pm 0.01\,\Omega\,\mathrm{cm}^2$
HCl oxide 1.2 nm	30 min 950 °C	0.047	$0.012 \pm 0.007\,\Omega\,\mathrm{cm}^2$

Table 4.1.: "Combined" contact resistances, measured on metalized J_0 test structures.

which possibly violates the requirements for accurate 4PP measurements (e.g. if these effects occur inhomogeneously).

For all interface oxides, a degradation of the passivation quality (if observed) occurs at higher thermal budgets than required for the formation of a good contact ($\rho_{\mathrm{rel}} < 0.05$). According to the simulations shown in figure 3.11 this corresponds to an upper limit of $\sim 0.7\,\Omega\,\mathrm{cm}^2$ for the absolute value of the interface contact resistance.

Since the interface contact resistances of the best samples are obviously below the resolution limit of the method, additional investigations for the determination of ρ_{int} are performed. These investigations are based on two-terminal IV-measurements (with two probes on each terminal). For this purpose, further processing on some of the test structures is performed, including a metalization on both sides with a stack of sputtered indium tin oxide (ITO) and evaporated Al. For the definition of the contact area these samples are cut into pieces with a size of 25 mm × 25 mm. Cutting is done with a chip saw instead of a laser to prevent edge currents due to melting of the poly-Si at the laser cut regions.

The measured IV-characteristics show an ohmic behavior. With these rather simple two-terminal measurements not only the interface contact resistance of the poly-Si / c-Si junction is measured (as with the method used above), but also the contact resistance between poly-Si and ITO and between ITO and Al, as well as the wafer resistivity. By subtracting the latter, a "combined" contact resistance, i.e., the sum of the resistances of the poly-Si / c-Si junction itself and the contact resistance between poly-Si and ITO and between ITO and Al is obtained. For representative samples, these values are given in table 4.1.

The measurements on metalized samples support the validity of the 4PP-method. The values of ρ_{rel} of ~ 0.05, which corresponds to an upper limit of $\sim 0.7\,\Omega\,\mathrm{cm}^2$ for ρ_{int}, are consistent with the "combined" contact resistances down to $0.012\,\Omega\,\mathrm{cm}^2$. In order to estimate the influence of the measured contact resistances on the solar cell conversion efficiency, a simple diode model (equation 1.2) can be used. For a contact resistance of

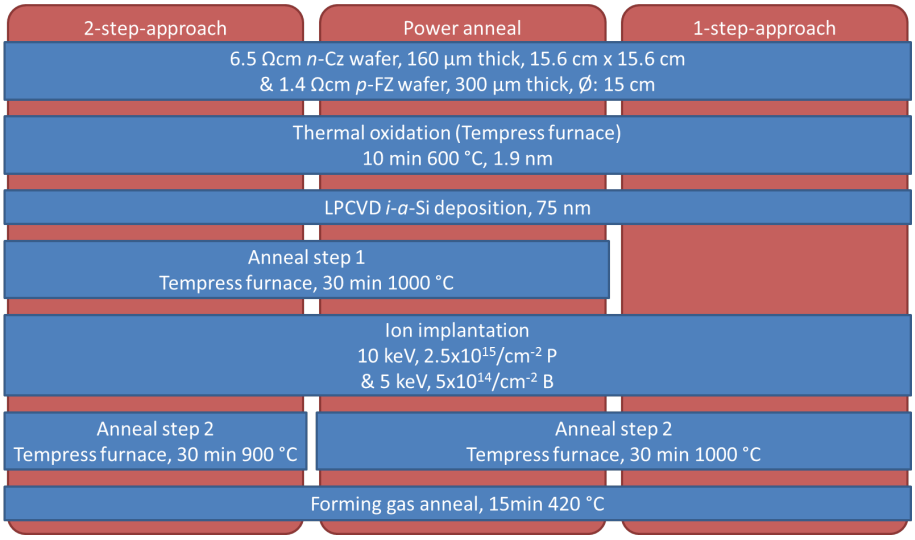

Figure 4.4.: Simplified process flow for the fabrication of poly-Si test structures with different annealing concepts. Also varied are the wafer material and the dopant type (P and B implantation).

$0.1\,\Omega\,\mathrm{cm}^2$ an efficiency loss of 0.16 % absolute has to be expected (assuming a solar cell with an ideal J_{sc} value of $42\,\mathrm{mA/cm}^2$ and a total J_0 of $10\,\mathrm{fA/cm}^2$).

4.2. Influence of the process order on the properties of the poly-Si contact

In the last section the samples have been fabricated by first applying a high temperature step to crack the interfacial oxide and then doping the intrinsic poly-Si using a much smaller thermal budget compared to the breaking-up process. The reason was to find an optimal temperature process for the contact formation independently from the doping process. Also, the risk of a strong diffusion of dopants into the wafer, which would be accompanied by enhanced Auger-recombination in this regions, could be reduced with this process sequence. Nevertheless, reducing the two high temperature steps (contact formation and doping) to one would reduce process complexity and does not necessarily degrade the properties of the poly-Si contact.

Therefore, a comparison between the two options is conducted. From the results of the last section it can be seen that the thermal oxides provide slightly better passivation quality than the chemical oxides. Hence only one thermal oxide type is used in this experiment. In a not shown experiment similar to the one of the last section, thermal oxides grown in a newer furnace (Tempress furnace) with generally better process homogeneity have been investigated. The best performance has been achieved with a 1.9 nm thick oxide, grown at 600 °C for 10 min and an annealing for 30 min at 1000 °C. Such annealing temperatures are

much higher than typical temperatures for BBr_3 or $POCl_3$ furnace diffusions. Therefore it could be necessary to either adapt the phosphosilicate and borosilicate glass growth processes to the higher temperatures during the dopant drive-in or to remove the respective glass before applying the high temperature process, which would hinder the reduction of process complexity. Ion implantation however provides a method to incorporate a controlled amount of dopants independently from the annealing processes applied. The test structures in this experiment are therefore produced with the process sequence shown in figure 4.4; a detailed list of the varied process steps, and of the measurement results of each sample shown in this section can be found in table A.3 in Appendix A. In order to measure the relative contact resistance (see section 3.2.7) of n-type and p-type poly-Si layers, not only n-type wafers, but also p-type wafers are included in the experiment. The wafers of the process group for the evaluation of the "1-step-approach" skip annealing step 1 and are annealed for 30 min at 1000 °C in annealing step 2 after the implantation step. A control group "2-step-approach" is annealed for 30 min at 1000 °C in annealing step 1 before the implantation and for 30 min at 900 °C in annealing step 2 for the activation and diffusion of the implanted dopants. A second control group "power anneal" is annealed for 30 min at 1000 °C in both annealing steps.

In figure 4.5 a) the J_0 values of the three groups are shown. The extremely low values (compare the J_0 values in table 1.1 for typical passivated phosphorus diffusions and in table 2.1 for representative n-type poly-Si values) for both, phosphorus (below 1 fA/cm^2) and boron (below 10 fA/cm^2) implanted poly-Si layers are achieved due to an optimized dopant density (see next section). As can be seen, the simplification to the 1-step-approach does not degrade the performance of the poly-Si contacts, but instead slightly increases it compared to the 2-step-group. For the n-type poly-Si samples, the J_0 values of the 1-step-process are the lowest, while the values of the power anneal group lie in between the values of the other two groups. Comparing the 1-step-approach with the power anneal, it can be concluded that the additional thermal budget during anneal step 1 is not beneficial for the surface passivation. This fits into the oxide break up model, as a higher thermal budget should result in stronger breaking up of the oxide. When comparing power anneal with 2-step-approach, it can be found that a higher thermal budget for anneal step 2 is beneficial. This points to the conclusion that at least for the chosen process parameters, Auger recombination of dopants, diffused into the Si-wafer during the annealing of the samples, does not dominate the surface recombination. Additionally, these findings hint that a diffusion of dopants into the wafer seems to increase the passivation quality. As already pointed out in section 3.1.1, this effect is known from high recombining surfaces, like metal contacts, where the introduction of dopants under the contacts reduces the surface recombination. For the poly-Si layers this can similarly be interpreted as a shielding from minority carriers from the pinholes, even overcompensating the detrimental effect of

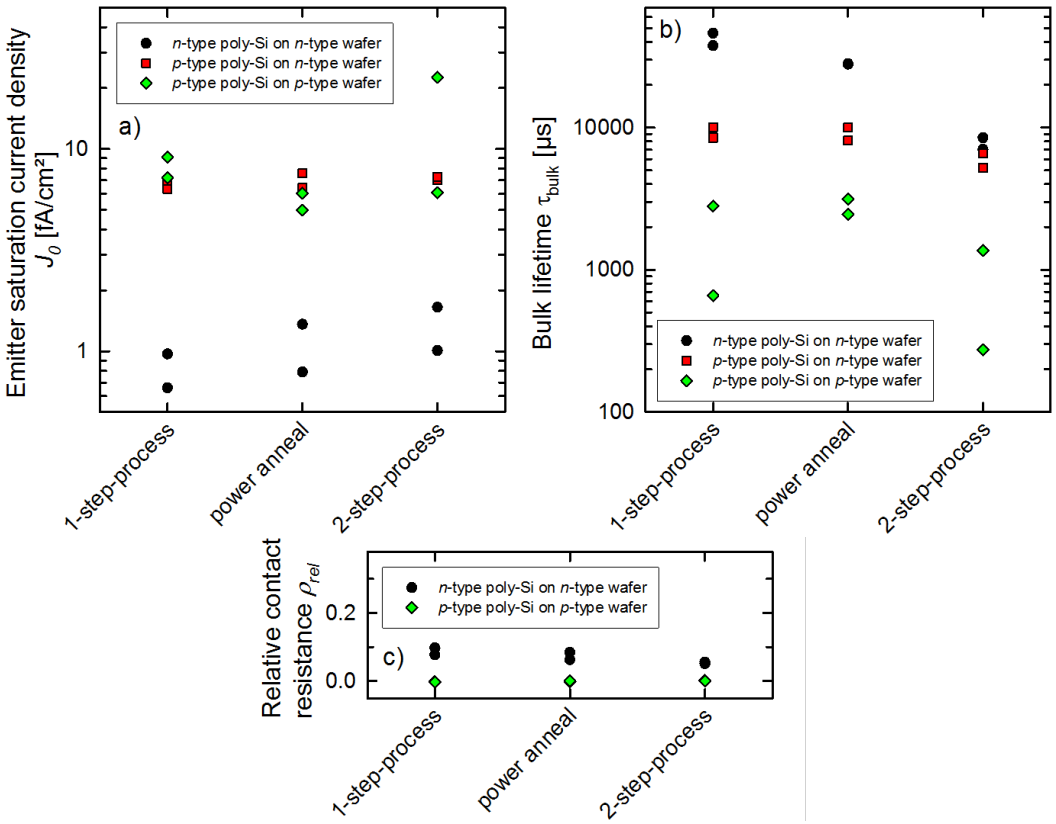

Figure 4.5.: a) J_0, b) τ_{bulk} and c) ρ_{rel} values of poly-Si test structures annealed with different annealing concepts. In this experiment two samples are used for each variation.

a possibly stronger breaking up of the oxide due to higher thermal budget. In figure 4.5 b) the bulk lifetime values obtained by subtracting the surface recombination part from the measured lifetime at low injection levels are plotted. As can be seen, not only the surface passivation, but also τ_{bulk} is influenced by the annealing process. Regardless of the dopant type, a high thermal budget after the doping process seems to strongly improve the lifetime of the wafer. A plausible explanation for this observation is gettering of residual impurities in the wafers by the poly-Si layers. This hypothesis is again discussed in section 4.4. The general lower bulk lifetime of the p-type float zone (FZ) wafers used in this experiment is commonly observed after high temperature processing. The cause of this decrease, compared to the lifetime of the wafers before high temperature processes is not known. Therefore in this work p-type poly-Si layers are always processed on both, p-FZ and n-Cz wafers, but where process capacities are limited n-type Cz is preferred over p-FZ, even if this means that no ρ_{rel} measurements can be conducted. The ρ_{rel} values shown in figure 4.5 c) are all rather low, indicating low contact resistivities for all processes. If there is an influence of the evaluated annealing processes, it can not be dissolved with this method.

4.3. Influence of the doping density on the properties of the poly-Si contact

Surface passivation and relative contact resistance

According to the introduction in section 3.1.1 not only the properties of the interfacial oxide are important for the passivation quality of the poly-Si contact, but also the band-bending caused by the strong doping of the poly-Si layers compared to wafer doping.

In order to investigate the influence of the doping density on the passivation quality, poly-Si test structures doped via ion-implantation are fabricated. Compared to furnace diffusion, ion-implantation offers an easy way to control the amount of incorporated dopants. The samples are processed with the 1-step-approach (see section 4.2 and the upper part of table A.4 in appendix A). Only n-type wafers are used, the thermally grown interfacial oxide used in this experiment has a thickness of 2.4 nm and the annealing step is extended to 80 min at 1050 °C.

Figure 4.6 a) shows the $J_{0,\text{poly}}$-values in dependence of the implantation dose for both, boron and phosphorus implanted test structures. For the case of phosphorus doped poly-Si, as expected, a strong improvement of the passivation quality with increasing implantation dose can be observed. However, for a very high dose of $7.5 \times 10^{15}\,\text{cm}^{-2}$ $J_{0,\text{poly}}$ increases, resulting in an optimal dose at $5 \times 10^{15}\,\text{cm}^{-2}$ with a $J_{0,\text{poly}}$-value of $1.0 \pm 1.1\,\text{fA/cm}^2$. For boron doped poly-Si the behavior is similar, but in this case the increase in $J_{0,\text{poly}}$ with

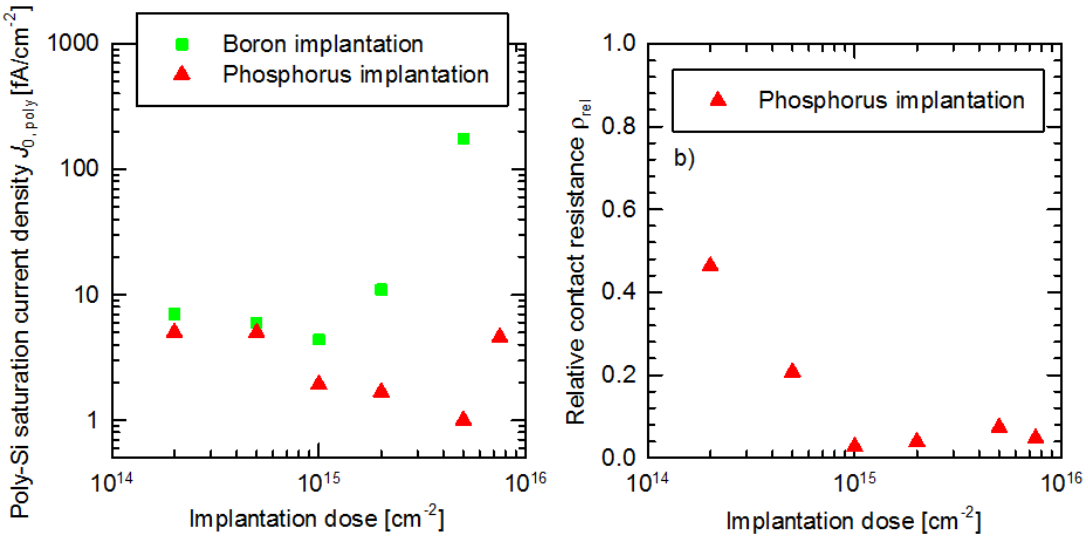

Figure 4.6.: a) $J_{0,\mathrm{poly}}$-values of poly-Si test structures implanted with different doses of boron (green squares) or phosphorus (red triangles). b) Relative contact resistance values ρ_{rel} of the phosphorus implanted test structures.

increasing dose is stronger and is already observable at lower doses. The lowest $J_{0,\mathrm{poly}}$-value of $4.4 \pm 1.1\,\mathrm{fA/cm^2}$ for boron doping is obtained for a dose of $1 \times 10^{15}\,\mathrm{cm^{-2}}$.

Figure 4.6 b) shows the ρ_{rel} values for the phosphorus implanted test structures. The ρ_{rel} value of the test structure with the lowest $J_{0,\mathrm{poly}}$ value corresponds to an upper limit of the interface contact resistance of $80\,\mathrm{m\Omega\,cm^2}$. For doses lower than $1 \times 10^{15}\,\mathrm{cm^{-2}}$, the interface contact resistance of the phosphorus doped poly-Si test structure increases to values higher than at least $1000\,\mathrm{m\Omega\,cm^2}$. The decreasing contact resistance with increasing implantation dose can be explained in agreement with the pinhole-model [66]: For a higher doping concentration in the poly-Si layer, the doping concentration in the pinholes and in the doped regions in the c-Si underneath the pinholes is expected to increase, which results in a reduced current crowding for the majority charge carriers near the pinholes and therefore a reduced contact resistance.

Doping profiles

While the decrease of the $J_{0,\mathrm{poly}}$ values with increasing dose can be explained by an enhanced field effect passivation, the reason for the increase of $J_{0,\mathrm{poly}}$ at too high doses is unexpected. In order to further analyze this increase, the doping profiles are analyzed by ECV measurements and for some samples also by secondary ion mass spectrometry (SIMS). The profiles are shown in figure 4.7 and 4.8. Further details on the SIMS measurements and the difference between the ECV and SIMS profiles are given in Appendix B. For the case of the boron doped test structures (figure 4.7 b)) a significant diffusion of the dopants into the wafer is observable, whereas for the phosphorus doped test structures

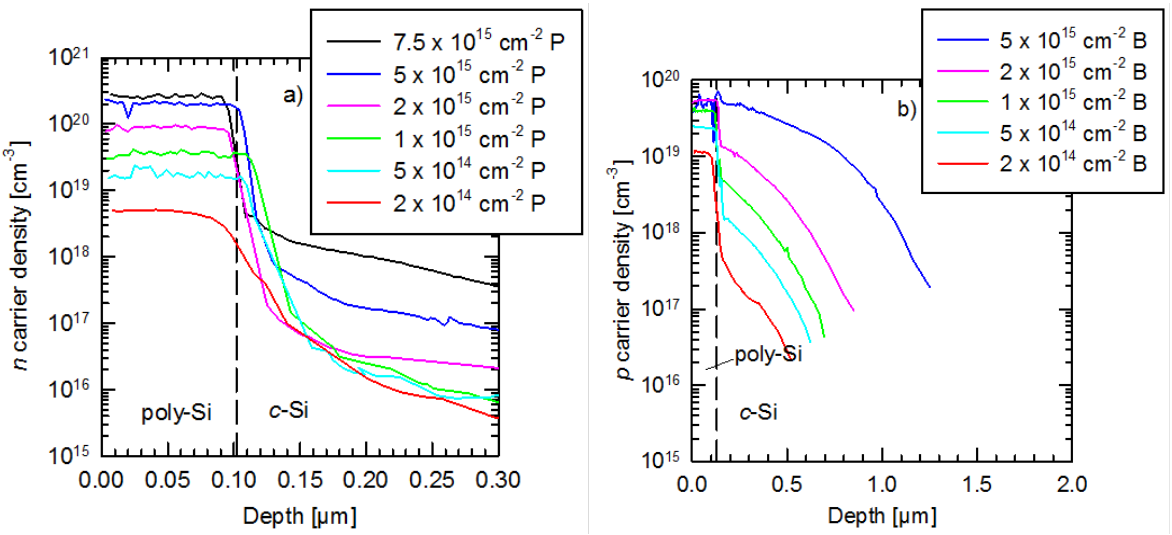

Figure 4.7.: ECV profiles of a) poly-Si test structures implanted with different phosphorus doses and b) poly-Si test structures implanted with different boron doses. The dashed lines mark the poly-Si / c-Si interface. (Note the different scales for both doping species.)

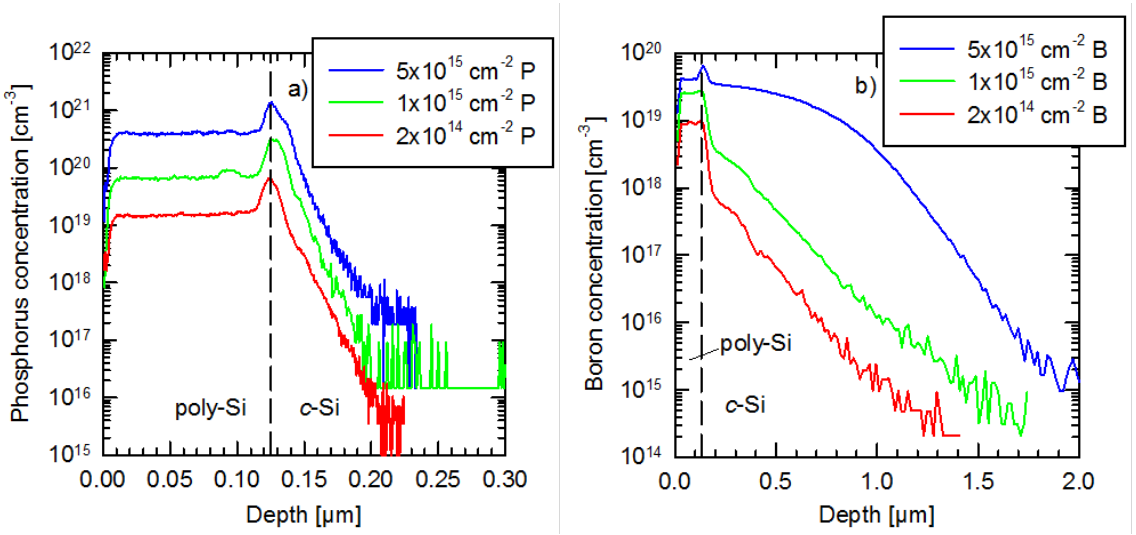

Figure 4.8.: SIMS profiles of a) poly-Si test structures implanted with different phosphorus doses and b) poly-Si test structures implanted with different boron doses. The dashed lines mark the poly-Si / c-Si interface. (Note the different scales for both doping species.)

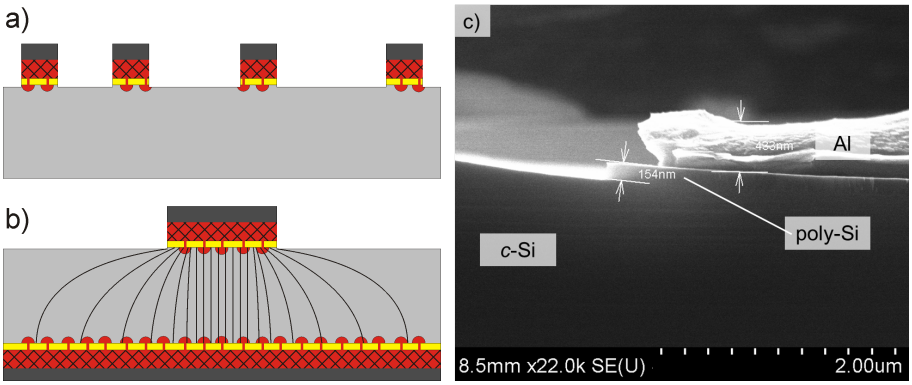

Figure 4.9.: Schematic cross sections of a) the TLM test structures and b) the Cox and Strack test structures. For the latter, the current paths are indicated by lines. c) SEM cross-section image of a TLM test structure after RIE.

(Fig. 4.7 a)) only a small amount of dopants diffuses from the poly-Si layer into the *c*-Si wafer. Despite the high thermal budgets used in this experiment (80 min at 1050 °C) the thin interface oxide acts as a good diffusion barrier for the phosphorus atoms. The exact amount of phosphorus diffused into the wafer can not be determined accurately, as the SIMS measurements have been conducted on samples with non-polished surfaces that were etched in a KOH solution. This results typically in a surface exhibiting steps with heights of some micrometers, which leads to a blurring of the measured signal. Additionally for steep dopant gradients both methods are not very accurate. Nevertheless, for the boron doped samples, the J_0-contribution of the dopants diffused into the wafer can be determined by using the part of the measured doping profiles that lies in the *c*-Si region. For these calculations the free web-tool EDNA2 has been used [108]. In order to obtain only the J_0-contribution of the dopants, the surface recombination value at the interface oxide is set to zero. For the highest boron dose investigated, the calculated J_0 has a value of 28 fA/cm^2, whereas the measured value is 175 fA/cm^2. This finding points to the conclusion that for the test structures with a high boron density in the poly-Si layer the passivation quality of the interfacial oxide is altered. An increase of the interface state density of the SiO_x / Si interface caused by boron diffusion through the oxide layer has also been observed in PMOS technology [109], [110].

Contact resistance measurements

In order to verify the 4PP results and to obtain quantitative interface contact resistance values, instead of an upper limit, two additional methods for the determination of ρ_{int} are used: the transfer length method (TLM) and the Cox and Strack method.

In order to apply the transfer length method [111], [112], 25 mm × 25 mm large pieces are laser cut from the n^+ poly-Si / n *c*-Si / n^+ poly-Si test structures. The metalization is conducted via thermal evaporation of 3.4 μm Al and subsequent sputtering of 80 nm

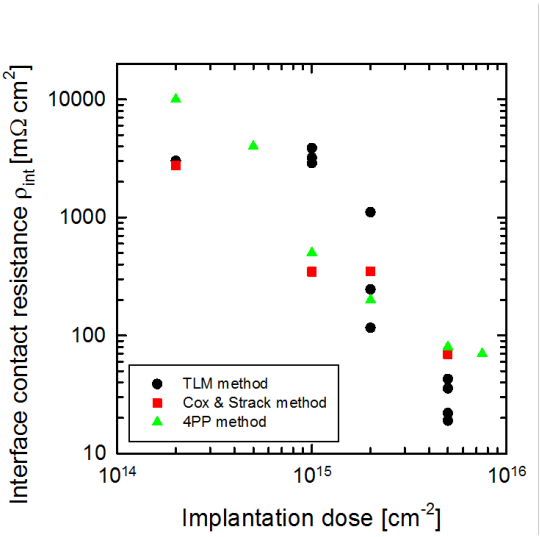

Figure 4.10.: ρ_{int} values measured by TLM, with the method of Cox and Strack and extracted from the 4PP-method.

SiO_2. The TLM fingers are defined by laser structuring the SiO_2 layer and etching the Al layer with a phosphoric acid solution. The resulting fingers have widths of 470 μm and lengths of 20 mm. The distance between two adjacent fingers varies from 0.64 mm to 1 mm. In order to avoid lateral current flow through the poly-Si layer between the fingers, the Al-fingers are used as a etch mask in a reactive ion etching (RIE) step. An SF_6 plasma is used to etch the 150 nm thick poly-Si layer, in the non-masked areas. A sketch of the resulting test structure is depicted in figure 4.9 a) and an SEM cross-section image is shown in figure 4.9 c).

For the Cox and Strack method [113] 25 mm × 25 mm large pieces from the same test structures are full area Al metalized on both sides. At the Centre for Sustainable Energy Systems at the Australian National University (ANU) circular pads with diameters ranging from 0.983 mm to 7.983 mm are defined by photolithography. The Al is etched by HCl and the poly-Si by TMAH. A sketch of the resulting test structure is depicted in figure 4.9 b).

The measurement results of both methods are shown in the graph in figure 4.10. In order to account for two dimensional current flow, the TLM measurements are evaluated with the approach of Eidelloth and Brendel [114]. For the TLM method more than one sample has been prepared from each test structure. The graph shows a strong deviation between these measurements. This might originate from processing inaccuracies during the laser definition of the fingers or during the Al etching step, resulting in inhomogeneous finger widths, and therefore undefined distances between the fingers. Smaller feature sizes and more precise patterning methods (e.g. photolithography) could possibly increase the accuracy of the method. Also the SEM investigations show that at some regions the interface oxides stops the RIE process (like in figure 4.9 c)) and at some regions on the same

test structure, more than 2 μm of silicon are removed. As some dopants diffuse through the oxide into the poly-Si layer (see section 4.3), this can result in slightly inhomogeneous lateral conductivities between different contact fingers and thus also affect the measurement results. Despite the large variation of the contact resistance measured with the TLM method, a clear trend towards lower values of ρ_{int} with increasing phosphorus implantation dose can be observed. For the highest investigated dose of $5 \times 10^{15}\,\mathrm{cm}^{-2}$ values between 19 and 43 $\mathrm{m\Omega\,cm^2}$ are measured.

The contact resistances measured with the Cox and Strack method show a similar trend as the TLM measurements: With increasing phosphorus doping density, the contact resistance decreases. The lowest values measured with this method are with 68 $\mathrm{m\Omega\,cm^2}$ nevertheless much higher than the values obtained with the TLM method. This may be implied by the high resistance of the wafer (6.3 $\Omega\,\mathrm{cm}$) and the arising resolution limit of this method of $\sim 100\,\mathrm{m\Omega\,cm^2}$ [115].

The 4PP method-values are obtained by comparing the ρ_{rel} values shown in figure 4.6 with values from device simulations similar to the ones shown in section 3.2.8. The resulting ρ_{int} values are comparable with the values obtained with the other two methods, showing the reliability of the 4PP method.

In order to estimate the influence of the measured contact resistances on the solar cell conversion efficiency, a simple diode model can be used. For the best passivating n-poly-Si layer and the worst case scenario of a contact resistance of 100 $\mathrm{m\Omega\,cm^2}$ an efficiency loss of 0.16 % absolute has to be expected (assuming a solar cell with an ideal J_{sc} value of 42 $\mathrm{mA/cm^2}$ and a total J_0 of 10 $\mathrm{fA/cm^2}$). For lower implantation doses, the contact resistances of some 100 $\mathrm{m\Omega\,cm^2}$ up to over 1 $\Omega\,\mathrm{cm^2}$, imply very high contributions to the series resistance of a solar cell and huge efficiency losses. For BJBC solar cells, it has to be noted that only a fraction of the solar cell is contacted by each polarity, typically the emitter is contacted on a larger fraction than the BSF. This implies even higher requirements on the contact resistivity of the poly-Si layers.

4.4. Analysis of the injection dependent recombination behavior

The very low $J_{0,\mathrm{poly}}$ values of the optimized poly-Si contacts indicate an excellent potential for the application in solar cells. Nevertheless, the $J_{0,\mathrm{poly}}$ value (extracted at high charge carrier injection levels) is not the only parameter of importance for the recombination characteristics of a solar cell. In order to identify the solar cell conversion efficiency potential of the poly-Si contacts, it is necessary to evaluate the recombination characteristics at the maximum power point (MPP). In this section, this is done by examining the injection dependent effective charge carrier lifetime measurements and the illumination dependent implied open circuit voltage suns-$V_{\mathrm{oc,impl}}$ curves of selected test structures.

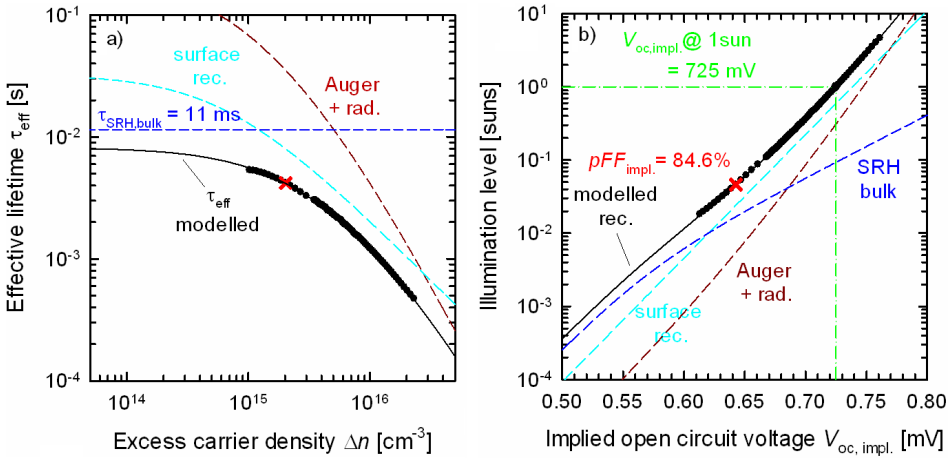

Figure 4.11.: a) τ_{eff}-Δn curve and b) suns-$V_{\text{oc,impl}}$ curve of a full area boron implanted poly-Si test structure. The filled circles are measured values, the lines modeled. The red cross marks the implied maximum power point (MPP_{impl}).

Figure 4.11 a) shows the measured injection dependent effective lifetime of a $p^+ / n / p^+$ test structure contacted with full area boron-implanted poly-Si layers with a dose of $1 \times 10^{15}\,\text{cm}^{-2}$. Additionally plotted are the combined Auger and radiative recombination (Auger + rad.), the surface recombination and the Shockley Read Hall lifetime in the bulk ($\tau_{\text{SRH, bulk}}$). The Auger and radiative recombination are modeled according to the parametrization of Richter *et al.* [116]. The surface recombination, i.e., the recombination at the poly-Si / c-Si junction, is calculated from the measured $J_{0,\text{poly}}$-value according to

$$\tau_{\text{surf}}^{-1} = \frac{2\,J_{0,\text{poly}}}{n_i^2\,q\,W}(N_{\text{dop}} + \Delta n)\,, \tag{4.1}$$

with τ_{surf} denoting the lifetime corresponding to the surface recombination, n_i ($8.6 \times 10^9\,\text{cm}^{-3}$) the intrinsic charge carrier density and W ($160\,\mu\text{m}$) and N_{dop} ($6.5 \times 10^{14}\,\text{cm}^{-3}$) denoting the thickness and doping density of the wafer, respectively. The SRH lifetime of the bulk is assumed to be injection independent and is determined by reciprocally subtracting the lifetimes accounting for Auger and radiative recombination and for the surface recombination from the measured effective lifetime in low level injection. The rather simple model (with $\tau_{\text{SRH, bulk}}$ as the only "fit parameter") to describe the injection dependent recombination behavior, matches the measured curve quite well over the whole injection range.

Despite the low $J_{0,\text{poly}}$-value of $4.4 \pm 1.1\,\text{fA/cm}^2$, the boron-implanted test structure is mainly limited by surface recombination at the implied maximum power point MPP_{impl} (red cross).

In figure 4.11 b) the suns-$V_{\text{oc,impl}}$-curve is plotted, together with its decomposition into the single contributions from the SRH recombination of the bulk, the surface recombination, and the Auger and radiative recombination. At one sun illumination, the implied open

circuit voltage of 725 mV is the highest value reported so far for p^+ doped poly-Si contacts (comparable values presented by other researchers are 694 mV [117]). It has to be noted that in contrast to a high efficiency solar cell, these test structures are fabricated on rather thick (160 μm) base material, and do not feature an anti-reflection coating or a surface texture. Assuming a short-current density J_{sc} of 42 mA/cm^2 in a BJBC solar cell, the V_{oc} limit exclusively implied by a full-area p^+ doped poly-Si emitter with $J_{0,poly} = 4.4$ fA/cm^2 would be 760 mV. The calculated pFF_{impl} of the curve has a value of 84.6 %. The limitation of a diode with an ideality factor $n = 1$ set by the value of $V_{oc,impl}$ is 85 %. This difference is due to a contribution from the SRH recombination of the bulk in high level injection with an ideality factor $n > 1$. Hence, in order to exploit the full pFF potential, even higher bulk lifetimes than 11 ms would be required to reduce the absolute amount of SRH recombination current.

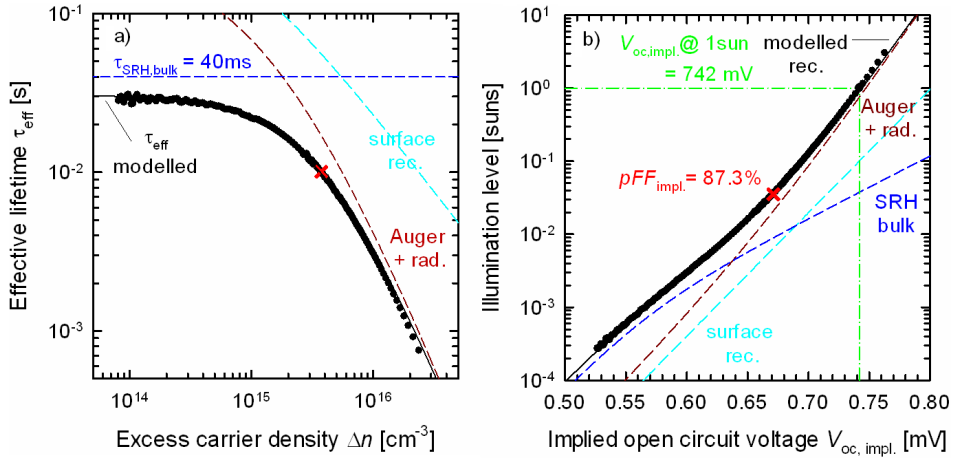

Figure 4.12.: a) τ_{eff}-Δn curve and b) suns-$V_{oc,impl}$ curve of a full area phosphorus implanted poly-Si test structure. The filled circles are measured values, the lines modeled. The red cross marks the implied maximum power point (MPP_{impl}).

Figure 4.12 a) shows the measured effective lifetime of a $n^+ / n / n^+$ test structure contacted with full area phosphorus-implanted poly-Si layers with a dose of 5×10^{15} cm^{-2}. Due to the very low $J_{0,poly}$ value of 1.0 fA/cm^2 the surface recombination contribution does not limit the total recombination at any injection level. In contrast, at MPP$_{impl}$ the test structure is mainly by Auger recombination in the c-Si base.

Figure 4.12 b) shows the suns-$V_{oc,impl}$ curve of this test structure. Since the bulk lifetime of this sample has a value 40 ms, the absolute amount of SRH recombination current in the bulk is small. The ideality factor > 1 implied by the high level injection does therefore not compromise the implied pFF. Rather, Auger recombination is dominating at MPP_{impl} with an ideality factor of $n \approx 2/3$. Accordingly, the pFF_{impl} reaches a very high value of 87.3 %.

The reason for the lower $\tau_{\mathrm{SRH,bulk}}$ value of the boron-implanted test structure compared to the phosphorus-implanted test structure is not known. Control wafers without poly-Si show $\tau_{\mathrm{SRH,bulk}}$ values of 10-15 ms after similar high temperature processes. Therefore it is reasonable to conclude that the boron implanted test structure does not show reduced lifetimes, but rather the phosphorus implanted test structure exhibits a higher lifetime than usual. A plausible explanation is that impurities in the wafer are gettered by the poly-Si layer during the high temperature annealing step and that the gettering efficiency differs for the differently doped regions. Both, heavily phosphorus doped layers, as well as poly-Si layers are known for their good gettering properties (see section 6 in reference [118]).

Assuming a BJBC solar cell, contacted with the two just presented poly-Si layers, each on 50 % of the cells rear side, the resulting implied efficiency, would be $\eta_{\mathrm{impl}} = 26.4\,\%$, for a bulk lifetime of 11 ms and $\eta_{\mathrm{impl}} = 26.7\,\%$, for a bulk lifetime of 40 ms. The respective $V_{\mathrm{oc,impl}}$ and pFF_{impl} values would be 739 and 740 mV and 85.1 and 86.0 %. For these calculations a high quality front side passivation with a J_0 value of 4 fA/cm^2 (as determined on wafers with an alkaline texture and an AlO_x/SiN_x passivation stack) is assumed, together with a current generation of 42 mA/cm^2. The difference between the theoretical considerations here and actual BJBC-like test structures will be shown in section 5.2.

4.5. Influence of the metalization on the properties of the poly-Si contact

In section 3 it was considered that the poly-Si contacts are applicable to solar cells without further losses due to the metalization. In this section this is verified by metalizing symmetric $n^+/n/n^+$ test structures via thermal Al evaporation. Figure 4.13 shows dyn.-ILM measurements of poly-Si test structures before metalization (large pictures) and after metalization (insets). 25 mm × 25 mm large samples, laser cut from test structures of the experiment in section 4.3, are used. The metalization is conducted via the evaporation of 1 μm Al on the full area of the rear side. From the ILM measurements no decrease in the lifetime (and therefore in the passivation quality) after metalization can be observed. The reduced lifetime at the edges of the metalized samples are most probably implied by the laser cutting. For this experiment 150 nm thick poly-Si layers are used, Nemeth *et al.* [60] have observed a thickness dependent degradation of the poly-Si passivation quality after e-beam Al evaporation: For 20 nm thick poly-Si layers the passivation quality of their samples is reduced, while no degradation is observed for 40 nm thick layers.

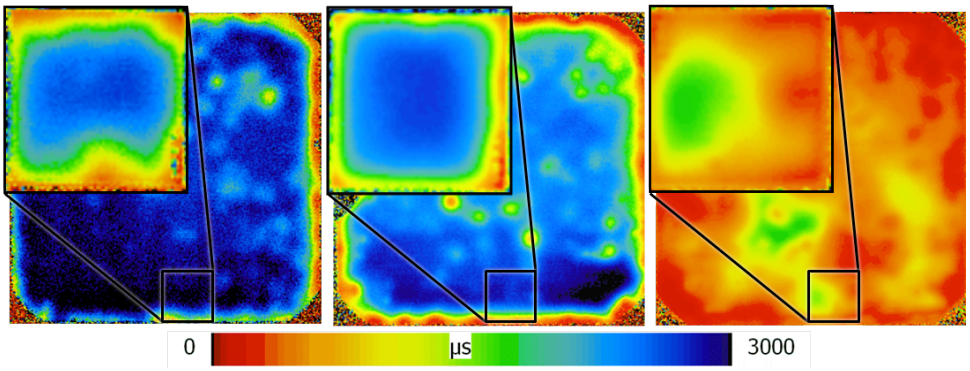

Figure 4.13.: Dyn.-ILM measurements of 156 mm × 156 mm large n^+ poly-Si / n c-Si / n^+ poly-Si test structures before metalization. The samples are doped with ion implantation (implantation doses from left to right: $5 \times 10^{15}\,\mathrm{cm}^{-2}$, $2 \times 10^{15}\,\mathrm{cm}^{-2}$ and $5 \times 10^{14}\,\mathrm{cm}^{-2}$). The insets show the lifetime after full area Al evaporation on 25 mm × 25 mm large pieces, laser cut from the marked areas.

4.6. Solar cell demonstrator

In order to demonstrate the applicability of the poly-Si contacts on solar cells, proof-of-principle solar cells are fabricated. The aim of this experiment is not the demonstration of highest efficiencies, but to show the high V_{oc} potential of the poly-Si contacts without a drawback in the series resistance. Therefore the front side is not optimized with respect to the optical properties.

The solar cells are fabricated using the two step approach described in section 4.1. The (planar) wafers are oxidized with a 2.4 nm thick thermal oxide and a layer of intrinsic LPCVD poly-Si is deposited on top of the oxide (on both sides). The samples are then annealed for 30 min at 1050 °C in an inert atmosphere. The doping of the rear poly-Si layers is conducted by depositing a PECVD SiN_x protection layer on the front side of the samples before applying a BBr_3 furnace diffusion. After diffusion the nitride layer is removed in an HF-solution. The front side doping is conducted similarly, by depositing a SiN_x protection layer on the rear side, applying a $POCl_3$ diffusion step and afterwards removing the nitride layer with HF. After a FGA step the samples are laser cut into $25 \times 25\,\mathrm{mm}^2$ large pieces. Then an Indium Tin Oxide (ITO) layer is deposited by sputtering on the rear and front side of the pieces through a mask with $21 \times 21\,\mathrm{mm}^2$ large openings. Metalization is done by evaporating a $20 \times 20\,\mathrm{mm}^2$ large Al pad on the rear side and an Al finger grid on the front side.

Figure 4.14 shows suns-$V_{\mathrm{oc,impl}}$ measurements of one of the solar cells after doping of the poly-Si and the FGA step (black circles). The measured curve exhibits an $V_{\mathrm{oc,impl}}$ value of 710 mV and an implied pseudo fill factor (pFF_{impl}) of 84.2 %. After laser-cutting (red squares) the recombination in low-level injection (LLI) increases, but stays rather constant in high injection levels, resulting in an unchanged $V_{\mathrm{oc,impl}}$ value of 710 mV but a

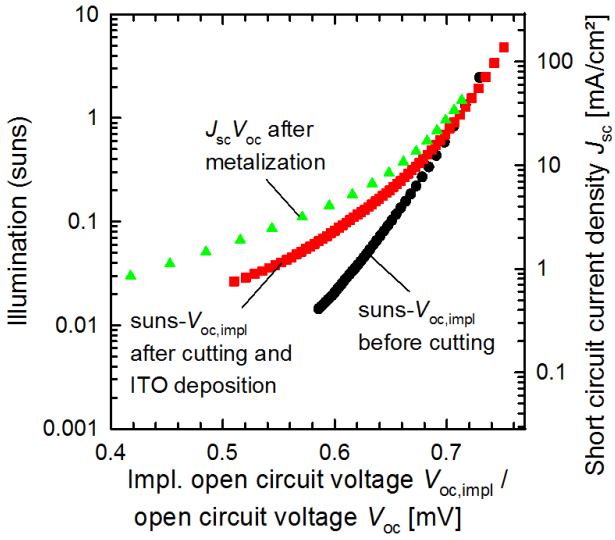

Figure 4.14.: Suns-$V_{\mathrm{oc,impl}}$ and $J_{\mathrm{sc}}V_{\mathrm{oc}}$ curves of a solar cell after different process steps. The $J_{\mathrm{sc}}V_{\mathrm{oc}}$ curve is been measured with a shadow mask.

Area [$\Omega\,\mathrm{cm}^2$]	V_{oc} [mV]	V_{oc} [mV] (full area illumination	pFF [%]	FF [%]	$R_{\mathrm{s,FF}}$ [$\Omega\,\mathrm{cm}^2$]	J_{sc} [$\mathrm{mA/cm}^2$]	η [%]
4.25	705	714	73.1	71.2	0.6	28.8	14.5

Table 4.2.: IV parameters of the best full poly-Si contacted solar cell.

reduced pFF_{impl} value of 77.6 %. The increased recombination in LLI can be explained by recombination in the *pn*-junction at the laser-cut wafer edges. This phenomenon has been investigated in detail by Kessler *et al.* [119]. After metalization the light IV and $J_{\mathrm{sc}}V_{\mathrm{oc}}$ curves are measured, with a shadow mask with a $20.6 \times 20.6\,\mathrm{mm}^2$ large opening. The $J_{\mathrm{sc}}V_{\mathrm{oc}}$ curves in figure 4.14 show that the edge effects increase even further. The solar cell V_{oc} is measured to a value of 702 mV and the pFF to a value of 73.4 %. As the V_{oc} obtained by this measurement is reduced due to recombination effects in the not illuminated areas, additional measurements without the shadow mask are conducted. This measurement setup is a slightly better representation of a large area solar cell. The resulting value for the V_{oc} is 708 mV.

The IV parameters of the solar cell with the highest measured light conversion efficiency are shown in table 4.2. On this cell a V_{oc} of 714 mV is measured under full area illumination. When applied on solar cells with better light trapping properties, the V_{oc} is expected to increase even further, due to higher injection levels. As in the case of the cell described above, the pFF is limited by the strong recombination on the wafer edges, but the series resistance $R_{\mathrm{s,FF}}$ of the solar cell which is extracted from the difference between the pFF (73.1 %) and the FF (71.2 %) [120] is determined to a value of $0.6\,\Omega\,\mathrm{cm}^2$. The major contribution to the total series resistance of the cell can be attributed to the resistance in

the Al front side grid ($0.35\,\Omega\,\mathrm{cm}^2$) and the lateral resistance in the cell between the fingers ($0.22\,\Omega\,\mathrm{cm}^2$). Both series resistance contributions are determined with analytical models described in reference [121], for the effective sheet resistance between the fingers, the sheet resistances of the ITO layer, the poly-Si layer and the wafer at Δn_{MPP} are reciprocally summed.

The low J_{sc} value of $28.8\,\mathrm{mA/cm}^2$ is a result from the poor optics of the solar cell: No front side texture is applied and the poly-Si layer on the front side is more than 200 nm thick, leading to poor light trapping and high parasitic absorption. Thus the conversion efficiency η of these proof-of-principle solar cell is expectably low, with a value of 14.5 %. Nevertheless the intention of the experiment to demonstrate high open circuit voltages and low contact resistances on cell level is succeeded.

4.7. Structural investigations

Even though the experimental results in the last sections seem to support the pinhole model, the detection of pinholes in the oxide of a poly-Si contact with good passivation properties would be a further evidence and strongly increase the plausibility of the model. For this reason, structural investigations with the aim to provide evidence for the pinholes are conducted.

4.7.1. Transmission electron microscopy

Following the work of Wolstenholme *et al.* and others [39], [87], [88] (see section 2), TEM investigations of cross sections of differently processed poly-Si / *c*-Si test structures have been performed at the Laboratory for Nano and Quantum Engineering (LNQE) in Hanover. Figure 4.15 shows a cross-section high resolution TEM (HRTEM) image of a $n^+ \,/\, n \,/\, n^+$ test structure exhibiting a chemically grown oxide (a HNO_3 solution has been used) that has been annealed for 30 min at 1050 °C. This rather high thermal budget applied on a test structure with a rather thin thermal oxide leads to a comparably low surface passivation quality (see also section 4.1). The TEM investigations show that the interface oxide is broken up on various regions and that the oxide disruptions have widths of $\sim 50\,\mathrm{nm}$.

In the shown measurement the sample is tilted with respect to the electron beam such that electrons passing the wafer (or crystallites with the same orientation) are interfering destructively, while electrons passing regions with other crystalline orientation are not interfering destructively so that the wafer appears darker than the poly-Si. An interesting feature in the measurements is the local epitaxial realignment of the poly-Si at the broken up regions, indicated by a darkening of these regions in this measurement mode.

TEM investigations on test structures with the same oxide, but lower annealing temperatures and therefore lower J_0 values did not result in finding pinholes. The same applies

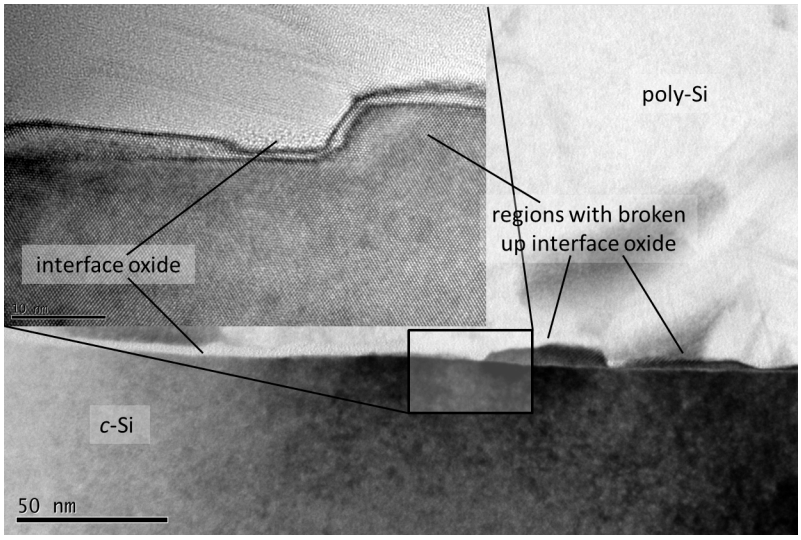

Figure 4.15.: Cross-section TEM image of a sample which received an extensive oxide break-up step, the inset shows a measurement of the marked area with a higher resolution.

for test structures with thermally grown oxides: On test structures with high thermal budget and high J_0 values, disruptions in the interface oxide can be found easily, while on samples with good J_0 values, the investigated oxide area shows no clear disruptions. This may be explainable by a too low areal density of the pinholes. According to the work of Peibst *et al.* [66] pinhole densities in the range of down to $10^7\,\mathrm{cm}^{-2}$ are well compatible with experimentally determined macroscopic properties of poly-Si junctions. In order to find a pinhole on a sample exhibiting such a low density, TEM investigations on a 100 nm thick slice would have to be performed on a 100 μm long section of the sample, which is not feasible.

Even though finding pinholes with TEM is challenging, interesting observations can be made. Figure 4.16 shows a cross-section HRTEM image of a $n^+ / n / n^+$ test structure exhibiting a 2.4 nm thick thermally grown oxide that has been annealed for 30 min at 1050 °C. In this figure a strong variation of the oxide thickness can be observed. Generally the oxide is thicker where grain boundaries of the poly-Si touch the oxide, but also in the other regions variations are visible. In this image a thickness of down to 1.8 nm is observed, but even lower local thicknesses could be present. A hybrid transport model with only local tunneling sites can be imagined. When taking into account that a thinner oxide is also a weaker barrier for the diffusion of dopants from the poly-Si into the *c*-Si wafer, locally stronger doped regions comparable to the semispheres of the original pinhole model would be the result. For the case of very thin oxide regions, where the transport is not limited by tunneling, for both charge carrier types, this hybrid model would, as well as the pinhole model, describe the carrier selectivity for both, *n*- and *p*-type poly-Si contacts.

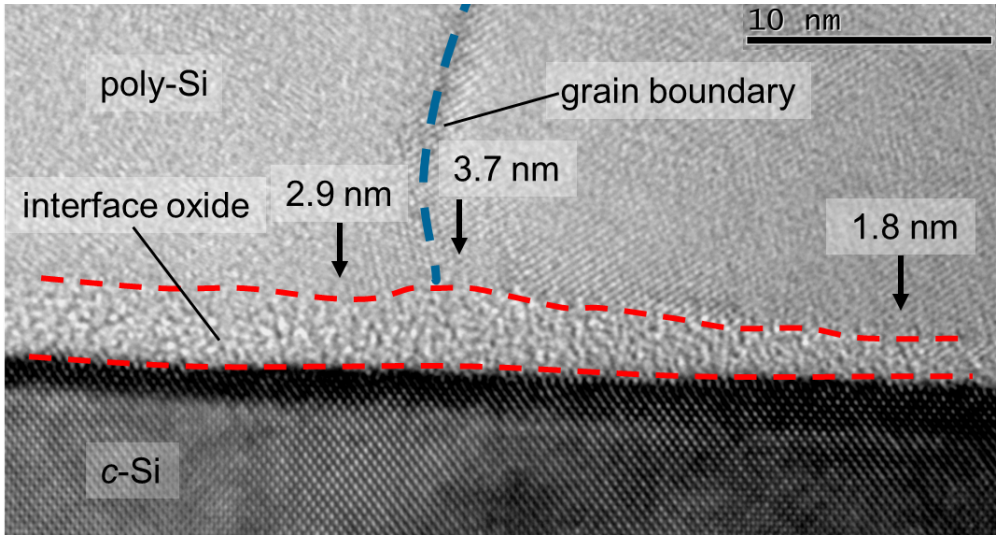

Figure 4.16.: Cross-section TEM image of a sample with a 2.4 nm thick thermally grown interface oxide after annealing.

Therefore, and because the pinhole model still seems to be more plausible, the hybrid model will not be taken into account in further discussions about the pinhole model, even though a very thin residual oxide layer could be present in the pinholes.

4.7.2. Conductive atomic force microscopy

As the TEM cross sectional investigations are limited in the observable oxide area, and the preparation of plan view samples was not successful, conductive atomic force microscopy (c-AFM) measurements are applied as an alternative method to investigate the nature of the current transport. During the measurements, a voltage is applied between the rear of the sample and a very fine conducting tip that scans the sample. The c-AFM measurements were conducted at the Laboratoire de Genie Electrique de Paris (LGEP).

Figure 4.17 shows a c-AFM measurement on a $p^+ / p / p^+$ test structure exhibiting a 2.4 nm thick thermally grown oxide that has been fabricated with the 2-step-approach (see section 4.1), including an annealing step for 90 min at 1050 °C and a BBr_3 diffusion. The relative contact resistance of the sample is below a value of 0.1, which corresponds to a good contact. In both, the topography image (figure 4.17 a)) and the conductance image (figure 4.17 b)), the poly-Si grain boundaries can be observed. The low measured resistance at the grain boundaries may be caused either by an enhanced conductance along the grain boundaries, compared to the grain volume, or by geometrical effects, as the AFM-tip has a higher contact area at steep edges, especially in trenches. Additionally some point like spots can be seen that also exhibit a low conductance.

In order to investigate the origin of these spots, SEM measurements of the sample have been conducted. Figure 4.18 indicates that the sample exhibits trenches at the grain

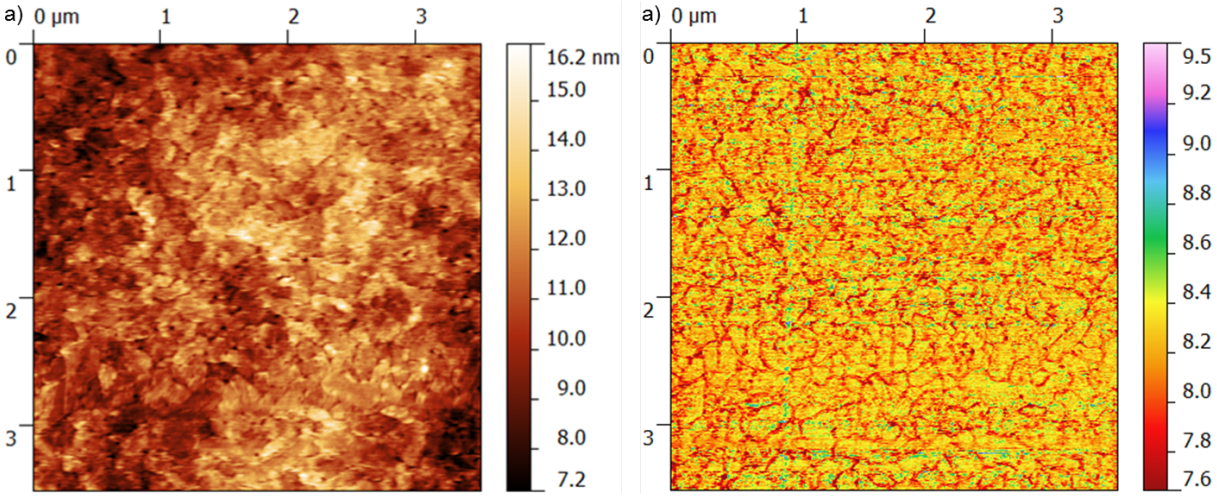

Figure 4.17.: Conductive AFM measurement of a $p^+ / p / p^+$ poly-Si test structure: a) the topography image and b) the conductance image. The color bar in b) gives the resistance in $10^x\,\Omega$, where x stands for the label at the color bar.

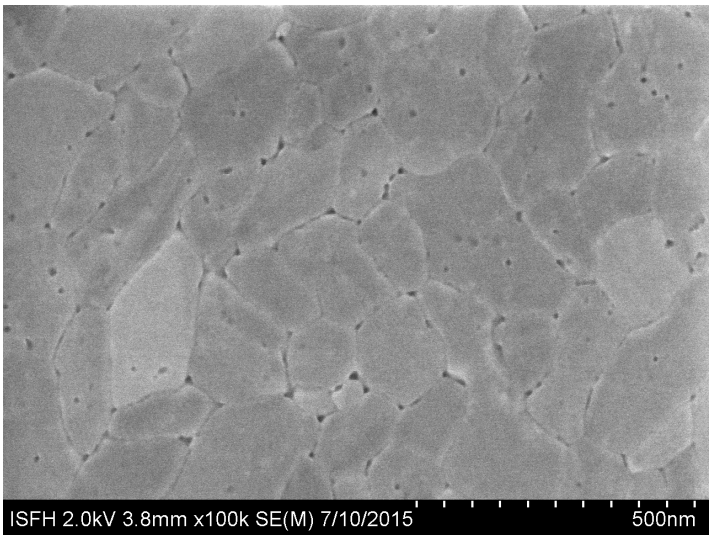

Figure 4.18.: SEM measurement the test structure shown in figure 4.17.

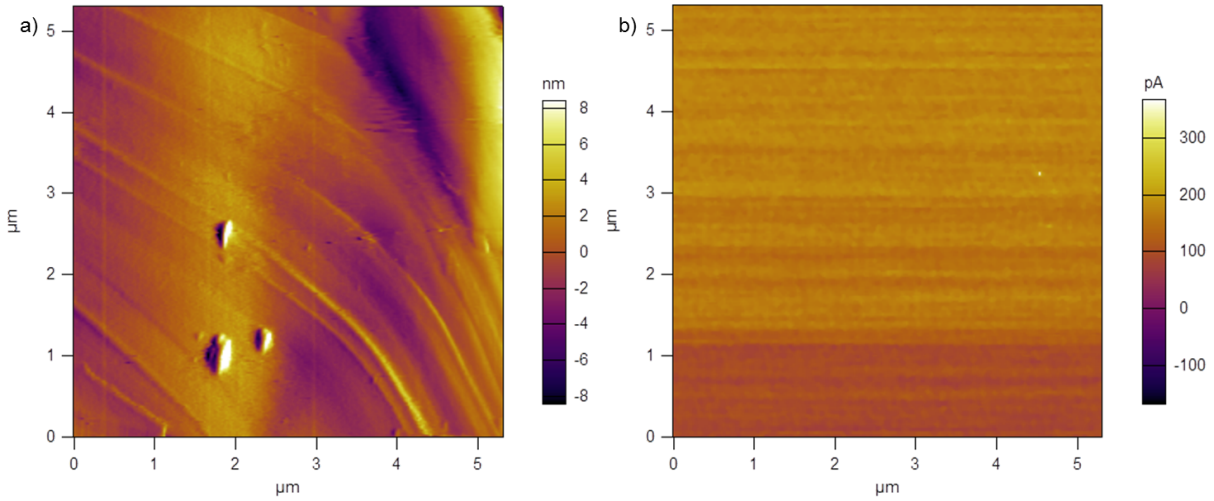

Figure 4.19.: Conductive AFM measurement of a $p^+ / p / p^+$ poly-Si test structure: a) the topography image and b) the current image.

boundaries and also numerous dimples at the surface. Most of the dimples are located at the grain boundaries, but some also in the middle of a grain. This observation makes it likely that the areas of high conductance in figure 4.17 a) are related to measurement artifacts caused by the surface topography.

The occurrence of trenches at poly-Si grain boundaries is a well known effect observed after oxidation of poly-Si films [122]. Even though, usually the poly-Si annealing steps in this work are conducted in nitrogen atmosphere, a residual oxygen partial pressure due to not perfectly sealed furnace openings, will always lead to a slight oxidation of the surfaces. By using an alternative furnace that has shown to exhibit a much lower residual oxygen partial pressure, the occurrence of the trenches can be averted.

In order to perform a second try with conductive AFM, a $p^+ / p / p^+$ test structure annealed in the alternative furnace is used. This sample has been fabricated with the 1-step-approach (see section 4.2) including the thermal growth of a 1.9 nm thick oxide, *i*-poly deposition, boron implantation and annealing for 60 min at 1050 °C. SEM investigations (not shown here) show a smooth surface without any trenches or dimples at the surface.

As the AFM group at LGEP has limited capacities, the new measurements have been conducted at the Australian National Fabrication Facility (ANFF) - Queensland Node. Figure 4.19 shows a corresponding measurement. The topography image (figure 4.19 a)) shows a relatively flat surface, without grooves and dimples. The same applies for the conductance image (figure 4.19 b)), where no features other than random noise can be seen.

These results point to the conclusion that either the current transport through the interface is homogeneous, or the contribution from the lateral transport in the poly-Si layer to the nearest pinhole is much smaller than the contributions from the current crowding

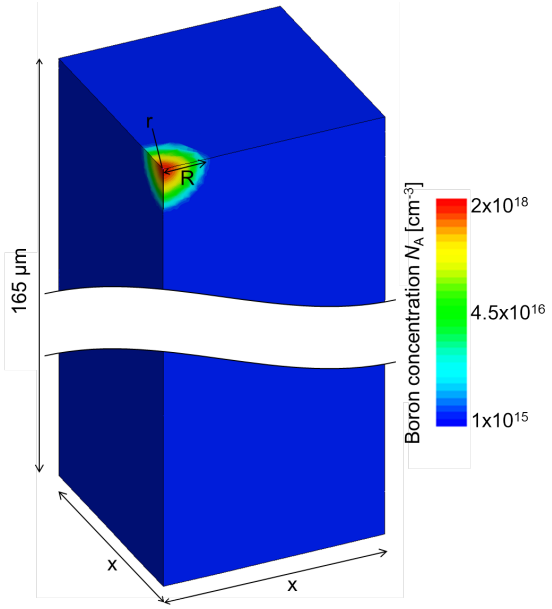

Figure 4.20.: Sketch of the unit cell used for the simulation of p^+ poly-Si contacts with spherically doped regions under the contacts.

under the AFM tip and from the transport through the wafer. The former contribution is at least responsible for the artifacts measured in figure 4.17.

4.8. Numerical simulation of pinhole contacts

In this section numerical device simulations are conducted in order to verify the plausibility of the pinhole model. One part of the simulational work is the verification of the analytically obtained results of Peibst *et al.* [66]. After that, scenarios with slightly more complicated device geometries that take some of the experimental observations into account are investigated.

The numerical 3D device simulations are conducted with SENTAURUS DEVICE [105]. The simulation is set up with a graphical user interface (GUI) programmed with the software MATLAB. The simulation domain consists of a square shaped (in the x- and y-plain) symmetry element of a test structure including a quarter of a pinhole and exhibiting a side length of half the distance between two pinholes and a height in the z-direction of 165 μm. The pinholes in the simulation are not circular, but square shaped. If not stated otherwise, the doping profiles under the pinholes are Gauss shaped in z-direction and at the borders of the pinholes also Gauss shaped in the x- and y-directions, resulting in a nearly radial doping distribution. Figure 4.20 shows a sketch of the simulation domain with a point contact on the front side. In order to obtain the saturation current density J_0 corresponding to the recombination at the poly-Si surface, symmetrical test structures with

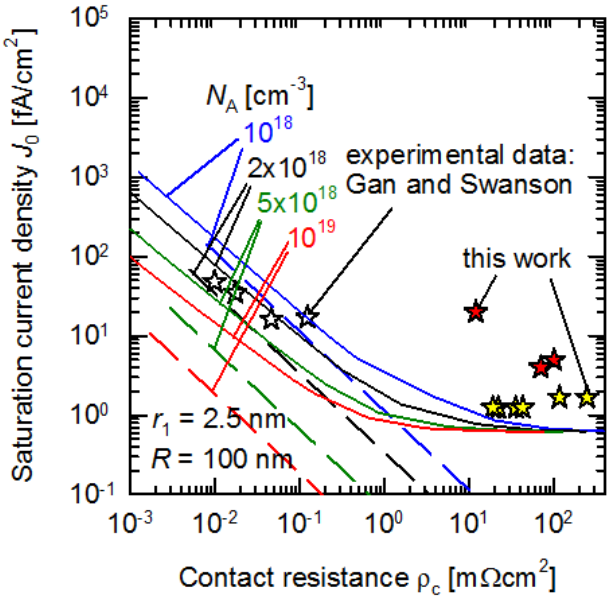

Figure 4.21.: Numerical simulations (lines) and analytical calculations (dashed lines) from ref [66] of J_0 and ρ_c values of p^+ poly-Si contacts with spherically doped regions under the contacts. Varied are in both cases the distance between neighboring pinhole contacts for varied peak doping concentrations. Also shown are experimental data from the work of Gan and Swanson [81] and from this work (although from this work n^+ poly-Si samples are used); the values of the red filled stars are taken from table 4.1 (IV-measurements on samples with different interface oxides), the values of the yellow filled stars are taken from figure 4.10 (TLM measurements on samples with different doping concentrations).

pinholes at both sides of the wafer are investigated. J_0 values are obtained by simulating a quasi steady state PCD measurement (see section 3.2.1) and by using the method of Kane and Swanson [96], similar to the experimental values. ρ_c is obtained by using a full area metalization with a negligible contact resistance between metal and semiconductor on the rear side of the simulation domain depicted in figure 4.20 and a local metal contact directly on the pinhole on the front side. In this simulation it is assumed that the major series resistance contribution of the poly-Si contact stems from the current crowding in the doped regions under the pinholes and not from the transport inside the poly-Si, therefore the contact resistance at the metal / pinhole interface is also set to a negligible value. In order to isolate the series resistance contribution of the poly-Si contact from the contribution of the transport through the wafer, additional simulations with full area metalized surfaces on both sides are conducted. The series resistance of the full area contacted sample is subtracted from the series resistance of the locally contacted sample. Thus, the resulting "lumped contact resistance" comprises not only the contribution from the current crowding around the pinhole, but for large distances between neighboring pinholes also the contribution from the lateral current flow in the wafer.

Figure 4.21 shows the simulation results obtained by varying the peak doping densities for different distances between the pinholes. Also shown for a comparison are analytically calculated values obtained by Peibst *et al.* [66]. In principle the analytically calculated dependencies are reproduced by the device simulations: higher doping densities are beneficial for the performance, as they result in much lower contact resistances. Nevertheless, the absolute values differ significantly. One difference is the different treatment of the contact resistance, in the work of Peibst *et al.*: Only the series resistance inside the doped regions has been calculated, while in the device simulations also the contribution from the distance between the pinholes is included. This contribution is independent of the peak doping density in the doped regions and therefore more pronounced for the structures with a lower contribution from the doped region, i.e. the structures with a higher peak doping concentration. A further difference is the J_0 offset of $\sim 0.6\,\mathrm{fA/cm^2}$. The reason for the offset is unclear. It is independent from the peak doping density, therefore Auger recombination in the doped regions can be excluded. No additional doped regions are included in the simulation and the surface recombination velocity at all surfaces, but the contact region, are set to zero. For simulated PCD measurements of a blank wafer without surface recombination and without doped regions at the surfaces, the offset is still measured. Therefore, it is likely a "measurement artifact" unrelated to the investigated contacts. The measurement artifact most probably originates from the inaccuracy in the determination of Δn. While for the simulations, as well as for "real" PCD measurements a mean value of Δn from the front till the rear is determined, for an accurate calculation of J_0 with equation 3.8 the value of Δn directly at the surface is important.

Despite the slightly differing results of the two methods, the experimental data of Gan and Swanson [81] and of this work can be well reproduced with both approaches. In section 4.3, doping concentrations well above $10^{18}\,\mathrm{cm^{-3}}$ are measured for both, phosphorus and boron doped poly-Si layers with low J_0 values. Therefore, peak doping densities of $2{\times}10^{18}\,\mathrm{cm^{-3}}$ or more, as required for a good matching with the experimental data of Gan and Swanson, are reasonable input parameters. The data points obtained in this work are met by the simulations, regardless of the peak doping concentration. Higher values of J_0 are always compatible with these simulations, as no surface recombination between the doped regions is applied.

Figure 4.22 shows additional simulations with a variation of a) the doping depth and b) the pinhole area. In agreement with the work of Peibst *et al.*, where the variation of the doping depth has no influence on the performance of the poly-Si contacts, here also only a minor effect is observed. For the smallest investigated doping depth of 100 nm slightly higher recombination can be observed, compared to the deeper doping profiles. A smaller contact radius hence, results in a reduction of the recombination for a fixed contact resistance, this observation is also in agreement with the work of Peibst *et al.*.

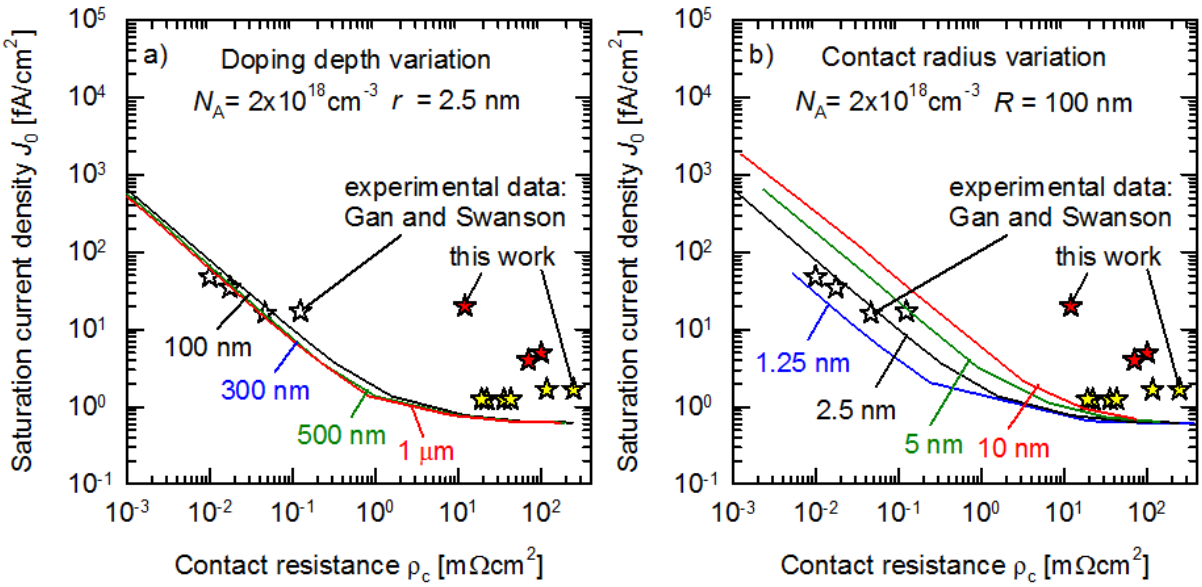

Figure 4.22.: Numerical simulations of J_0 and ρ_c values of p^+ poly-Si contacts with spherically doped regions under the contacts. Varied are the distance between neighboring pinhole contacts for a) varied contact radii and b) varied doping depths. Also shown are experimental data (see figure 4.21 for the details)

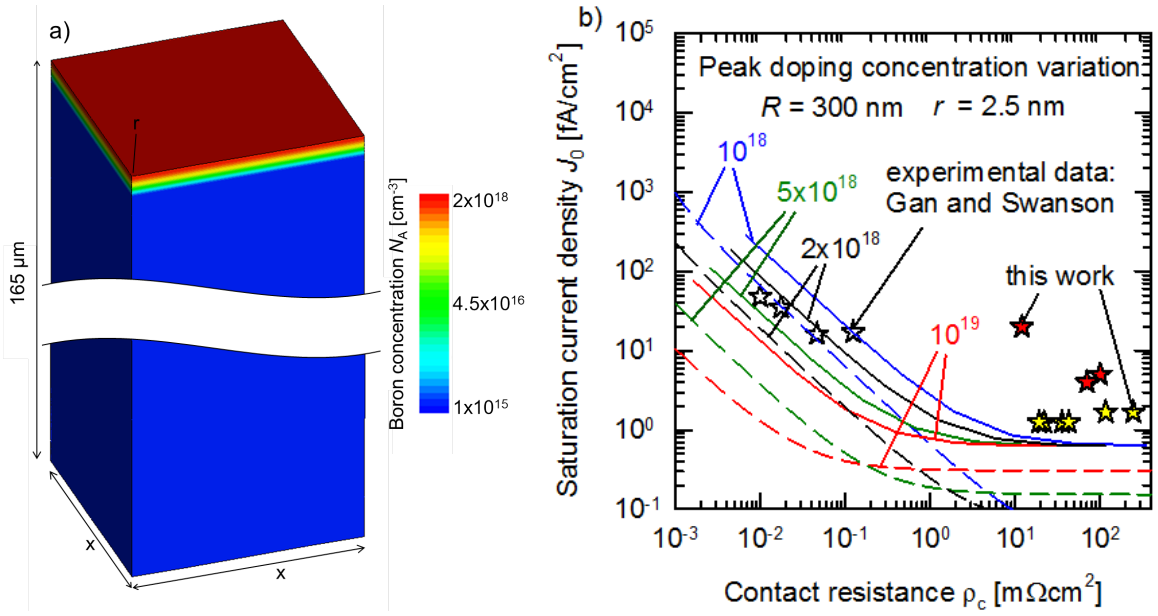

Figure 4.23.: a) sketch of the unit cell used for the simulation of p^+ poly-Si contacts with full area doped regions under the contacts. b) Numerical simulations (lines) and analytically calculated values (dashed lines, Fischer's model [123]) of J_0 and ρ_c values of p^+ poly-Si contacts with a homogeneously doped region at the wafer surface.

With the analytical approach of Peibst *et al.*, only pinholes with semi-spherically doped regions have been investigated. Experimental observations (see section 4.3) indicate that at least for boron doped poly-Si layers, a doped region is formed at the complete poly-Si / *c*-Si interface. In order to investigate this case with numerical simulations, Gauss shaped doping profiles are used on the whole area, not only under the pinholes. A sketch of the simulation area is shown in figure 4.23 a). Figure 4.23 b) shows the simulation results for a variation of the peak doping density. They are in principle similar to the results obtained with spherically doped regions, showing that the formation of doped regions exclusively under the pinholes is no necessary requirement for the explanation of the measured (J_0/ρ_c) pairs.

Also plotted are analytically calculated values obtained with the approach of Fischer [123] for the modeling of point contacted solar cells. In this approach, ρ_c is calculated with the formula

$$\rho_c = \frac{p^2\rho}{2\pi r}\arctan\left(\frac{2W}{r}\right) + \rho W\left(1 - e^{-\frac{W}{p}}\right), \tag{4.2}$$

where p is the distance between two contacts, ρ denotes the wafer resistivity, r the contact radius, and W the wafer thickness. The surface recombination velocity s_{eff} is calculated with

$$s_{\text{eff}} = \left(\frac{\rho_s - \rho W}{\rho D} + \frac{1}{f s_{\text{cont}}}\right)^{-1} + \frac{s_{pass}}{1-f}, \tag{4.3}$$

where D is the diffusivity, f the contact fraction, s_{cont} the recombination velocity at the contact, and s_{pass} the recombination velocity at the passivated surface. D is obtained with Einsteins relation

$$D = \frac{\mu k T}{q}. \tag{4.4}$$

Fischer then calculates the saturation current density J_0 with

$$J_0 = \frac{q n_0 D}{L} \cdot \frac{D\tanh(W/L) + s_{\text{eff}} L}{D + \tanh(W/L) s_{\text{eff}} L} \tag{4.5}$$

where L is the diffusion length and n_0 the minority charge carrier density at the surface. For the special case of highly doped regions and therefore high Auger recombination,

$$L = \sqrt{D\tau_{Auger}} \tag{4.6}$$

is used to calculate the diffusion length.

In order to adapt this model to the case of a poly-Si contacted wafer, with a highly doped region under the poly-Si layer, ρ is set to the peak concentration of the doping profile in the wafer and W is chosen to a value such that the sheet resistance of the layer equals the sheet resistance of the Gauss shaped doping profile. As in the simulations, the

surface recombination is set to zero, s_{pass} is also set to zero. s_{cont} is set to 10^7, similarly to the contact recombination in the simulation.

It can be seen in figure 4.23 that the numerically simulated values are again very comparable to the analytically determined values. Also the simulations of the full area doped regions match very well with the simulations of the semi spherically shaped doping profiles. For the analytically calculated values here also an offset in J_0 is observable. This is attributed to the Auger recombination included in the model. Due to the different definition of the doping profiles in the numerical and the analytical approach, the recombination implied by Auger recombination is higher in the analytical approach. The offset in the numerical approach is, as already explained an artifact of the simulations.

4.9. Summary

In sections 4.1-4.3 the parameters for the poly-Si contact fabrication are optimized towards low interface recombination and contact resistance between the poly-Si layers and the wafer. It is shown that the passivation quality of thicker, thermally grown interface oxides is more stable in high temperature processes, than the one of the thinner, chemically grown interface oxides, while the latter on the other hand require a lower thermal budget than the former in order to exhibit good contacts. The best pairs of low recombination and contact resistance are achieved with thermally grown oxides: $J_{0,\mathrm{poly}} = 0.66\,\mathrm{fA/cm^2}$ and $\rho_{\mathrm{int}} = 500\,\mathrm{m\Omega\,cm^2}$ and $1.0\,\mathrm{fA/cm^2}$ / $80\,\mathrm{m\Omega\,cm^2}$, both for n-type poly-Si contacts and $4.4\,\mathrm{fA/cm^2}$ without a contact resistance measurement and $5.0\,\mathrm{fA/cm^2}$ / $100\,\mathrm{m\Omega\,cm^2}$ for p-type poly-Si contacts. It is also shown that high doping densities in the poly-Si layers are beneficial for both, the passivation quality and the contact resistance. Too high doping densities nevertheless can result in a degradation of the passivation quality, so that optimal values have to be found.

The validity of the 4PP approach to estimate the contact resistance between poly-Si and c-Si introduced in the sections 3.2.7 and 3.2.8 is verified by measured contact resistances in sections 4.1 and 4.3.

In section 4.5 it is shown that the metalization of the poly-Si layers is possible without degrading the passivation quality. This is confirmed in section 4.6, where solar cells contacted on both sides with poly-Si contacts are fabricated. The cells exhibit open circuit voltages of 714 mV and series resistances of $0.6\,\Omega\mathrm{cm^2}$ (dominated by the transport in the cell and in the metal grid, not by the contact resistance), thus showing the transferability of the optimized layers to solar cells.

The structural investigations performed in section 4.7 are not successful in finding pinholes in the interface oxide of good passivating poly-Si contacts. Nevertheless, on "broken-up" poly-Si contacts, disruptions in the interface oxide can be found. Additionally,

thickness variations in the oxide are found that might be precursors for the pinhole formation.

The numerical simulations conducted in section 4.8 confirm the general plausibility of the pinhole model, for both, spherically doped regions under the contacts and full are doped regions, as implied by the doping profiles measured in section 4.3.

Pinhole model vs. tunneling model

The observed influence of the thermal budget on the passivation quality and contact resistance fits very well into the pinhole model, as the formation of pinholes (and therefore the reduction of the contact resistance) is likely thermally activated and too strong breaking up of the oxide will greatly reduce the passivation quality. The latter aspect is also shared by other researchers, observing a degradation of the passivation quality at high thermal budgets [54], [55]. The former aspect can also be explained within the tunneling model, as higher thermal budgets will increase the amount of dopants diffused through the oxide into the *c*-Si wafer and therefore increases the majority carrier density in front of the oxide and therefore the tunneling probability [80]. This is of course only true, if the poly-Si layer is doped before the high temperature process. In section 4.1 the thermal budget is applied before the doping process and nevertheless has a strong influence on the contact resistance. This observation is hardly explainable within the tunneling model.

A further inconsistency is the already in section 3.1.2 discussed observation of the symmetry of *p*- and *n*-type poly-Si contacts that are both capable of producing low surface recombination densities and contact resistances. Tunneling models in the literature usually assume different tunneling barriers for electrons and holes and thus no model, capable to explain the symmetrical behavior of *n*- and *p*-type poly-Si with one set of parameters has been published up to now.

At least the experimentally observed discrepancies of the tunneling model are of course only true for the interface oxides used in these experiments. It may be possible that, for the rather thick oxides used in this work pinholes are needed for the contact formation, whereas for thinner oxides, full area tunneling could be the dominant transport mechanism. Additionally, a hybrid model, as discussed in section 4.7.1, where the oxide exhibits locally differing thicknesses and tunneling takes place only at some thinner regions, may also be valid. For this model, if the transport (especially the transport of the minority charge carriers) is not limited by the tunneling probability, but by the transport in the wafer to the tunneling sites, it would be compatible with the calculations and simulations in section 4.8.

Chapter 5

Counterdoping

Counterdoping describes the concept of overcompensating the dopants of one polarity with dopants of the other polarity such that the polarity of the semiconductor is changed. This definition includes the formation of an n-type (p-type) emitter in a p-type (n-type) wafer, but in this work the term is only used for the overcompensation of a highly doped region with dopants of the other polarity. In solar cell technology counterdoping can be used for the formation of the p- and n-type regions on the rear side of BJBC solar cells. When using counterdoping, the introduction of only one polarity has to be masked, while the other polarity can be doped on full area. In contrast to a BJBC solar cell with both doping steps masked, a precise alignment between the two doping steps is not required.

In this chapter, ion implantation is the only method used for the incorporation of dopants into the wafers. Ion implantation offers a simple way for local doping by inserting a shadow mask in the ion-beam (see figure 5.1). This results in a very lean process flow compared to other masking techniques, like PECVD deposited layers structured with a laser or with photo lithography.

In section 5.1 the general feasibility of counterdoping is shown for the case of c-Si without poly-Si contacts. In contrast to ion implantation into poly-Si, where the implantation-induced crystal defects do not matter, high lifetime c-Si devices require a high temperature annealing step to cure such defects [124], [125]. For the special case of touching highly doped p- and n-type regions there is an additional risk to observe band to band tunneling (BBT) or trap assisted tunneling (TAT) [126]. Device simulations are conducted to investigate the influence of crystal damage, residual from ion implantation or (as for the case of poly-Si contacts) intrinsic in the poly-Si layer on the IV-characteristics of counterdoped devices.

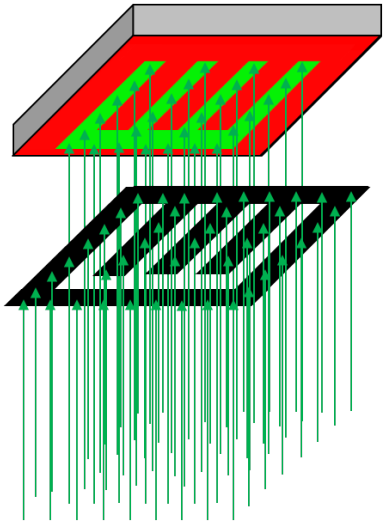

Figure 5.1.: Principle of masked ion-implantation: A shadow mask blocks part of the incoming ions so that a locally doped region is formed on the wafer (green area).

The simulation results are compared with measured IV-characteristics from test structures with patterned counterdoped regions. In section 5.2, counterdoping is applied on samples with poly-Si contacts. Again, counterdoping is first conducted on full area to show the principle feasibility and then patterned to reproduce the relevant case for BJBC solar cells. The understanding of the recombination mechanisms in the counterdoped poly-Si contacts is supported by device simulations.

5.1. Counterdoping in monocrystalline silicon

5.1.1. Doping profiles

In order to investigate the counterdoping process, test structures with full area counterdoping, i.e., first a boron implantation step and then a higher dose phosphorus implantation step, are fabricated. Here, doses of $1.5 \times 10^{15}\,\mathrm{cm}^{-2}$ for the boron implantation and $3 \times 10^{15}\,\mathrm{cm}^{-2}$ for the phosphorus implantation are chosen. In order to fully cover the boron profile already in the as implanted state, the as implanted ion distribution of both implant steps is determined with the software TRIM [127]. It is found that a boron implantation performed with an ion energy of 10 keV (mean ion range: 42 nm) can be fully covered with a phosphorus implantation performed with 35 keV (mean ion range: 51 nm). After an annealing step for 40 min at 1050 °C, serving the purpose of dopant activation and annealing of the implantation damage, SIMS measurements are performed. In order to contact an n-type wafer, the doping profile of the BSF species (phosphorus) has to overcompensate the profile of the emitter species (boron) over the whole doping depth.

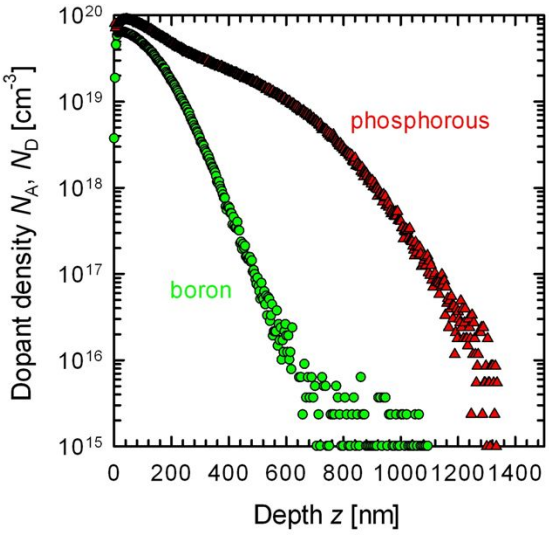

Figure 5.2.: SIMS profile of a sample which received a boron and a phosphorus implantation step and an annealing step.

Figure 5.2 shows the SIMS profile of the counterdoped test structure after the annealing step. The resulting sheet resistance, as determined by PCD measurements, is 46.5 Ω/□ and the saturation current density after SiO_x / SiN_x passivation is 220 fA/cm^2. The sheet resistances and saturation current densities of samples receiving only a full area boron or phosphorus implant are 110 Ω/□ and 27 fA/cm^2 and 23.9 Ω/□ and 190 fA/cm^2 after the same annealing step respectively.

The SIMS profile demonstrates that the chosen P implant parameters are suitable to ensure complete overcompensation of the emitter after a high temperature annealing step. Further, the resulting sheet resistances are suitable for the application in high efficiency BJBC solar cells [128], [129].

5.1.2. Diode test structures

The electrical properties of the *pn*-junction between a counterdoped local BSF area and the surrounding boron emitter are investigated with test structures featuring local counterdoped areas. Figure 5.3 shows the process flow for the test structure fabrication: A damage etched 1.5 Ωcm *p*-type 6 inch float zone silicon wafer is implanted full area with boron on the front and rear side. The front side receives an additional phosphorus implantation through a shadow mask with hexagonally arranged 400 μm wide circular openings with a distance of 1040 μm between the openings, creating localized diodes. After the annealing step, a passivation layer is deposited on the wafer. The layer is locally opened by laser ablation using a 532 nm laser with a pulse length of 10 ps. On the front side, laser contact openings are only applied at the counterdoped areas. Both sides are contacted with evaporated aluminum, followed by SiO_x evaporation and the HORIZON

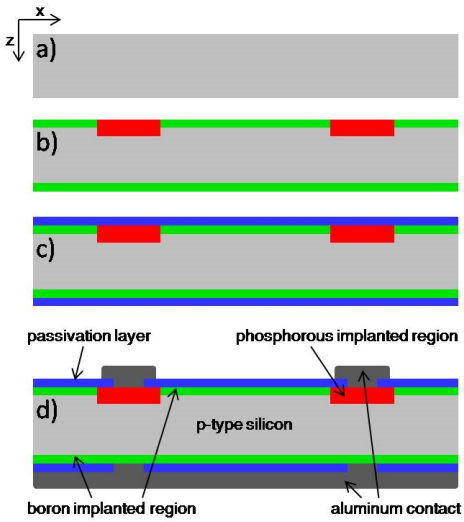

Figure 5.3.: Process flow for diode test structure processing: a) p-type FZ wafer, b) full area boron implantation on both sides and masked phosphorus implantation on one side c) co-annealing and passivation, d) contact opening and metalization

contact separation process [130]. The HORIZON process here consists of a local removal of the SiO_x protection layer with a laser and a subsequent etching of the metal at the laser scribed regions in a phosphoric acid based solution. In the protected, non laser scribed regions, the metal layer stays intact.

In this test structure, each phosphorus doped region poses a separate, small area diode, which is contacted from one side, while the boron doped region is contacted via the p-type base from the opposite side. Since the most important physical effects are occurring in the heavily implanted region at the n^+p^+-junction between the overcompensated n^+ BSF regions and the surrounding p^+ boron emitter, the test structures represent well the situation in an n-type BJBC solar cell.

5.1.3. Numerical simulations

For the investigation of possible implications of remaining implant damage and of the directly touching of n^+- and p^+-doped regions on the IV characteristics, two-dimensional numerical device simulations are performed using SENTAURUS device [105]. The simulation structure corresponds to the experimental test structure (figure 5.3). Gaussian profiles are used for the vertical dopant distributions of both phosphorus and boron doped regions and also for the lateral phosphorus distribution at the border of the phosphorus implanted regions (see figure 5.4). The p-type base has a resistivity of 1.5 Ωcm and a SRH-lifetime of 3 ms. The simulation domain has a thickness of 10 μm and a width of 20 μm.

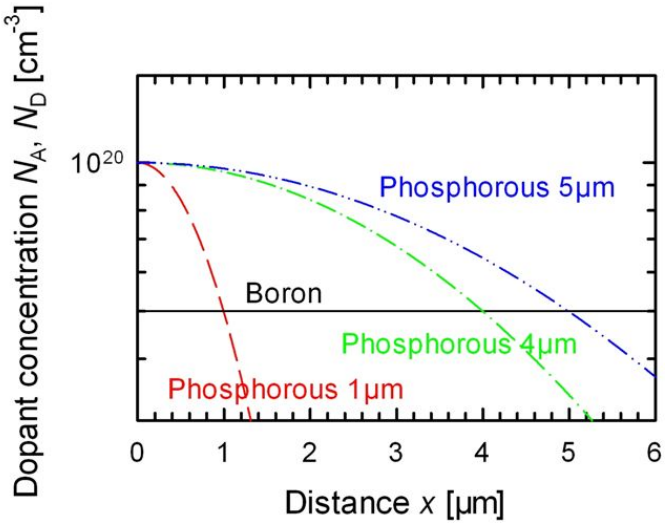

Figure 5.4.: Lateral dopant distribution at the edge of the phosphorus implanted region of the simulated diodes. The boron profile is laterally homogeneous, the phosphorus profile has a concentration of 10^{20} cm^{-3} in the counterdoped region and on the edges a Gauss-shaped grading with lateral depths of 1 μm, 4 μm and 5 μm respectively.

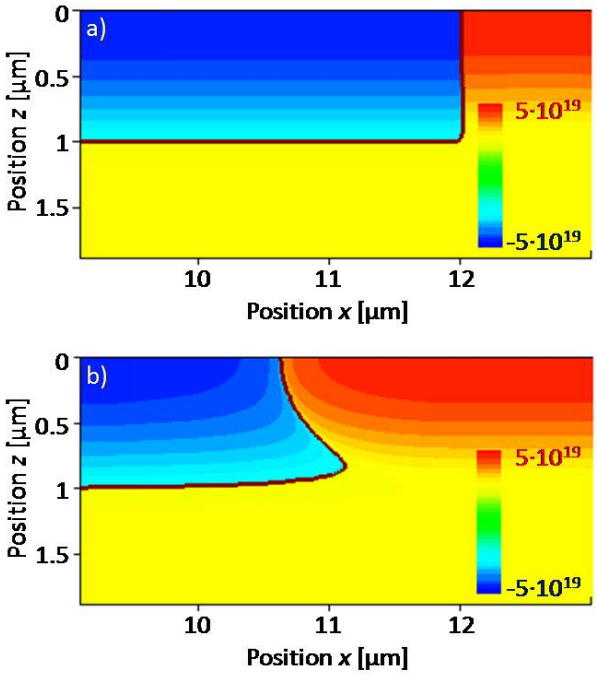

Figure 5.5.: Effective dopant concentration mappings of simulated diodes. The boron profile is laterally homogeneous with a peak concentration of 5×10^{19} cm^{-3} and a vertical depth of 1 μm. The phosphorus profile has a peak concentration of 10^{20} cm^{-3}, a vertical depth of 1 μm and a lateral depth of a) 0 μm (corresponding to an abrupt lateral pn-junction), and b) 5 μm.

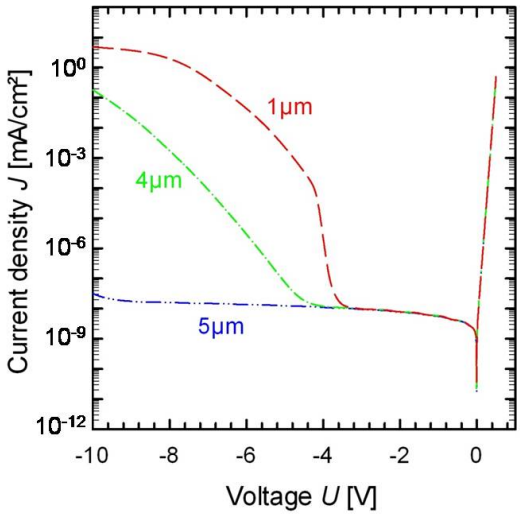

Figure 5.6.: IV characteristics of simulated diodes with a variation in the lateral dopant distribution. The boron profile is laterally homogeneous with a peak concentration of $5{\times}10^{19}\,\mathrm{cm}^{-3}$ and a vertical depth of $1\,\mu$m. The phosphorus profile has a peak concentration of $10^{20}\,\mathrm{cm}^{-3}$, a vertical depth of $3\,\mu$m and a lateral depth of $1\,\mu$m, $4\,\mu$m and $5\,\mu$m respectively (the case of $0\,\mu$m is not plotted, due to numerical inaccuracies at the singularity). The lifetime is kept a 3 ms.

The effective dopant concentration at the p^+n^+-junction between the counterdoped region and the boron doped region is shown in figure 5.5 for the case of a $0\,\mu$m and $5\,\mu$m deep lateral phosphorus profile. The influence of the lateral depth on the IV characteristic is shown in figure 5.6. For the case of a $1\,\mu$m deep lateral doping gradient, band to band tunneling sets in at -4 V in reverse direction. For laterally more graded doping profiles, the breakdown voltage is shifted to higher values. In forward direction, there is only negligible influence on the IV characteristic.

The influence of implantation damage, which might remain to some extend after annealing, is shown in figure 5.7 a). A heavily damaged implanted region is represented by a SRH-lifetime of 3 ns in the doped area, while a SRH-lifetime of 3 ms corresponds to a well annealed doped region. All curves refer to a phosphorus doping profile with a lateral depth of $1\,\mu$m. In the case of the reduced lifetime, the IV curve shows a strong increase of the current density in reverse as well as in forward direction. The application of the TAT model of Hurkx [131] has only a small effect on the IV curves of the simulated diodes.

These results can be interpreted as follows: For high SRH-lifetimes (low implant damage), band to band tunneling is dominating in reverse direction. In this scenario, the forward direction is not affected by trap-assisted tunneling. In the scenario of a large amount of remaining implant damage, the IV characteristic features multiple current transport mechanisms. In reverse direction, band to band tunneling occurs for reverse voltages

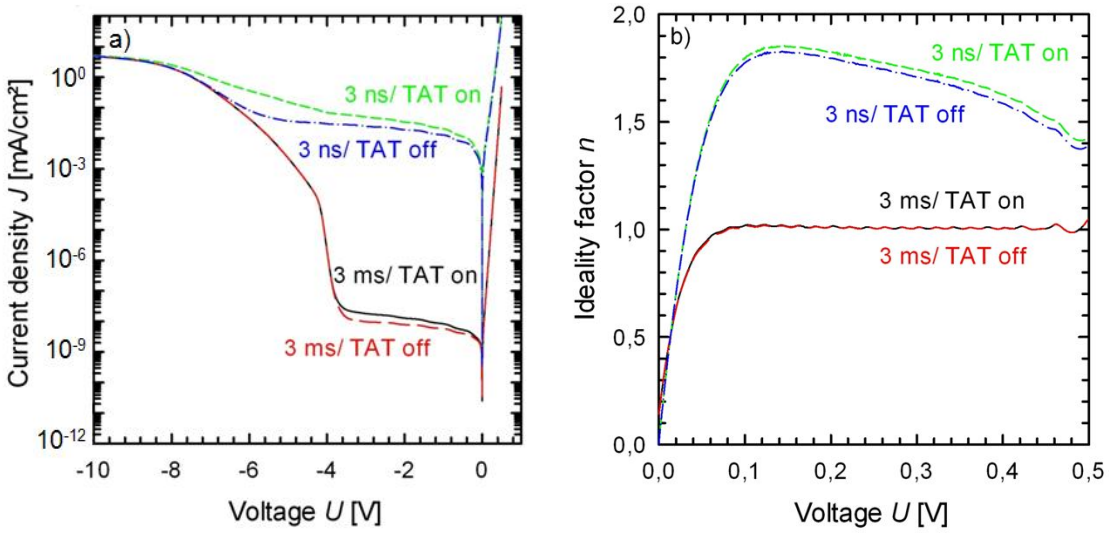

Figure 5.7.: a) *IV* characteristics and b) ideality factor of simulated diodes with a variation in the lifetime of the implanted region, black solid and red long dashed curve: 3 ms, green short dashed and blue dash-dotted curve: 3 ns. Simulations have been performed with and without the Hurkx TAT model [131] of SENTAURUS device, black solid and green short dashed curve and red long dashed and blue dash-dotted curve, respectively.

lower than -4 V. Additionally, trap assisted tunneling also contributes to some extend. Furthermore, the reverse current density is also increased by SRH generation in the space charge region. In forward direction, a low SRH-lifetime in the doped regions compromises the *IV* characteristic even for the case that trap-assisted tunneling is disregarded. The most plausible explanation are recombination processes in the space charge region, that typically lead to ideality factors of ~ 1.7 [132] (see figure 5.7 b). This is the dominating current transport mechanism in forward direction in this scenario, while trap-assisted tunneling plays a minor role. The high ideality factor would imply a very low fill factor in a solar cell device.

5.1.4. Electrical characterization

The dark *IV* characteristics of the single diodes are measured by applying a voltage between a contact at the counterdoped region on the front side and the rear side and measuring the current. A Süss PA 200 probe station and a Keithley 4200 analyzer equipped with Keithley 4200 PA pre-amplifiers are used. The *IV* characteristics are measured on numerous diodes on the 6 inch wafer, showing homogeneous results, which indicates a stable process. The characteristic of a typical diode is shown in figure 5.8 a). In reverse direction, the current density for small reverse voltages is very low, while it steeply increases for voltages higher than -8 V. This behavior is reminiscent to the simulated scenario for rather high SRH-lifetimes in the doped region (see figure 5.7), corresponding to an

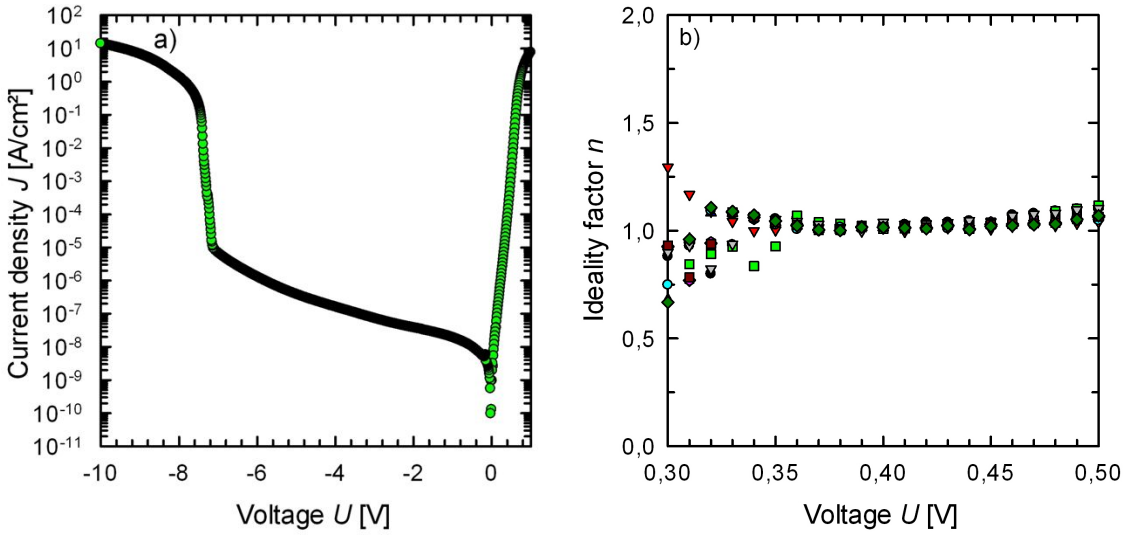

Figure 5.8.: a) Measured IV characteristics and b) ideality factor of diode test structures fabricated with counterdoping.

excellent annealing of the implant damage. No significant trap-assisted tunneling and SRH generation in the space charge region are observable in the devices, while band to band tunneling is possibly the root-cause for the breakdown at $-8\,\mathrm{V}$. Comparing the measured breakdown characteristic with the numerical simulations for different lateral phosphorus profile depths (see figure 5.6), it can be concluded that the touching doping profiles do not form an abrupt, but rather a considerably graded junction with a depth of some micrometers. This is possibly due to enhanced lateral inter-diffusion of the dopants during the annealing step, caused by the attractive Coulomb forces between the oppositely charged dopant species [133], or due to a divergence in the ion beam. The latter effect implies a smeared-out region at the boundaries of the phosphorus implanted regions. For a different experimental setup, micro 4PP measurements imply a lateral grading of $\sim 10\,\mu\mathrm{m}$.

In forward direction, in the voltage range between $0.35\,\mathrm{V}$ and $0.50\,\mathrm{V}$, the ideality factor of the measured diodes is close to 1 (see figure 5.8 b)). This observation indicates only weakly pronounced recombination processes in the space charge region, which is consistent to a very small amount of remaining implant damage.

Concluding, it can be stated that counterdoping with masked ion implantation in c-Si is possible and should not result in enhanced trap assisted tunneling or other detrimental effects, as long as the implantation damage is annealed appropriately. Thus, the fill factor of solar cells fabricated with counterdoping should be as high as the fill factor of BJBC solar cells fabricated with more complex processing steps.

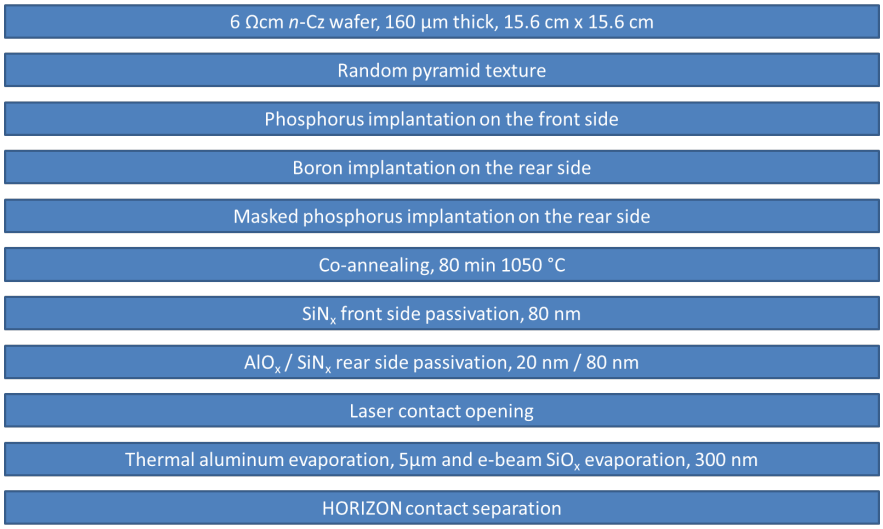

Figure 5.9.: Simplified process flow for the fabrication of ion implanted back junction back contacted solar cells with counterdoped BSFs.

5.1.5. Counterdoped BJBC solar cells

After the promising results obtained on the diode test structures, solar cells with ion implanted boron doped emitters and patterned ion implanted phosphorus BSFs are fabricated. The low complexity of this process is shown by the simplified process flow in figure 5.9 consisting of 10 steps. In this work, multiple solar cells with an active cell area of 20 mm x 20 mm are fabricated on a 156 mm x 156 mm wafer. Each wafer features 22 solar cells with a variation in the doping geometry and 3 fields for monitoring of the sheet resistance and the lifetime of the phosphorus, the boron and the counterdoped implantations, respectively.

In contrast to both side contacted solar cells, the emitter of BJBC solar cells can not be applied on the full area. In order to enable high short circuit densities, the average path length for the homogeneously generated minority charge carriers to the emitter has to be low. Therefore, for BJBC solar cells a high emitter fraction is beneficial. For the BJBC cells shown here, this is realized by implanting the emitter on the full area of each solar cell and applying counterdoped BSFs only at isolated circular areas. The BSF areas have diameters of 400 μm or 600 μm and are arranged in a square shaped pattern with a distance of 1200 μm or 1600 μm between them. This results in emitter fractions between 80 % and 94 %. Due to this special layout the BSF metal fingers overlap with regions of the emitter area. Despite the presence of a PECVD dielectric stack consisting of 20 nm AlO_x and 80 nm SiN_x between metal and emitter, this layout leads to the formation of shunts on numerous spots on the rear side of the wafer. While the density of the shunts can be reduced by the application of additional dielectric stack with varied thicknesses, for the best investigated combination (20 nm AlO_x, 80 nm SiN_x and 500 nm PECVD SiO_x)

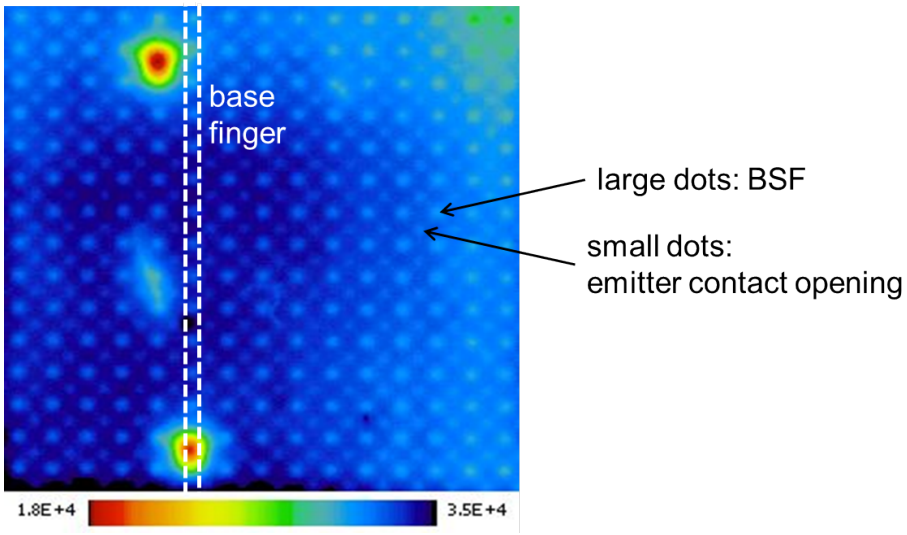

Figure 5.10.: PL image of a BJBC solar cell with circular BSF spots. Two shunts in the emitter region under the BSF metalization locally reduce the signal intensity. Also visible is a slight lifetime reduction at the highly doped BSF spots and at the emitter contact openings.

still more than one third of the cells on each wafer is shunted. Figure 5.10 shows the PL image of a solar cell exhibiting numerous shunts (red spots), also visible are the BSF spots, which are slightly darker than the surrounding full area emitter.

While, as expected, the solar cells with shunted regions show strongly degraded fill factors, also the fill factors of the cells without shunts are limited. The best solar cell with an efficiency of 21.1 % exhibits a fill factor of only 75.1 %, while the open circuit voltage has a value of 685 mV and the short circuit current density is 41.0 mA. The pseudo fill factor of this solar cell has a value of 82.4 % showing that neither shunts, nor a low volume lifetime or enhanced recombination in the space charge region (both with ideality factors larger $n = 1$) are responsible for the low fill factor. A difference between fill factor and pseudo fill factor can typically be attributed to the series resistance of the cell [120]. The value for R_s determined from the difference of the two fill factors is $1.5\,\Omega\,\mathrm{cm}^2$. TLM measurements on reference samples show contact resistances of $0.4\,\mathrm{m}\Omega\,\mathrm{cm}^2$ for the emitter contact and $0.8\,\mathrm{m}\Omega\,\mathrm{cm}^2$ for the BSF contact. Taking into account the contact fraction of $\sim 0.2\,\%$ for both, emitter and BSF, this should result in a series resistance contribution of $0.6\,\Omega\,\mathrm{cm}^2$. In this experiment the difference in the series resistance is presumably caused by an inappropriate laser contact opening process on the cells, as indicated by the light microscopy images shown in figure 5.11. Figure 5.11 a) shows a contact opening with the same parameters as on the solar cells, figure 5.11 b) shows a contact opening with a slightly higher laser puls energy. While with the lower energy, the SiO_x and SiN_x layers are removed, a residual grayish layer can be observed that is not present when applying the higher laser energy. This layer may possibly be attributed to the AlO_x layer. Further

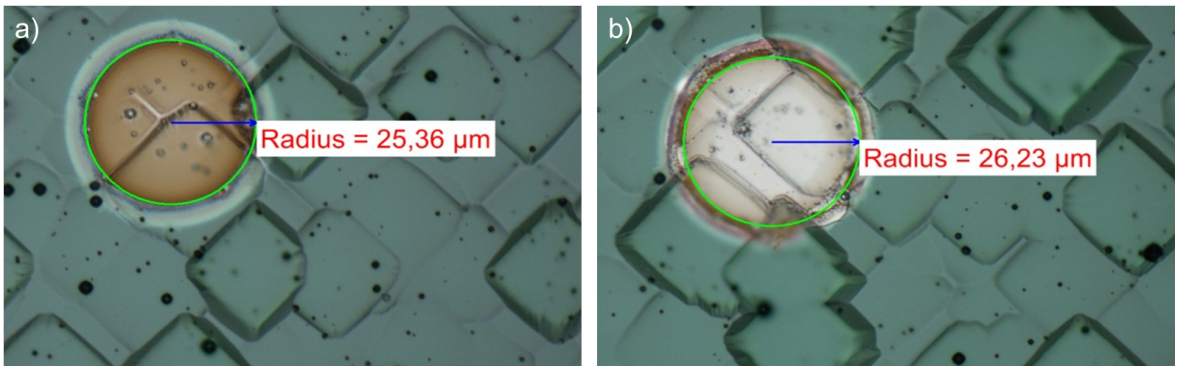

Figure 5.11.: Light microscope images of laser contact openings of an 20 nm AlO_x / 80 nm SiN_x / 500 nm SiO_x dielectric stack a) with an incomplete removal of the stack and b) with a complete removal of the stack.

investigations show that a 30s dip in diluted HF after the laser contact opening process with the lower pulse energy can also be used to remove the grayish layer and to improve the contact resistance.

Despite the high series resistance of the presented solar cells and the shunts on part of the cells, the results demonstrate the applicability of the counterdoping process for high efficiency *c*-Si BJBC solar cells. With some modifications this process has also been implemented on 156 mm x 156 mm large solar cells, resulting in conversion efficiencies of 22.1 %, with a V_{oc} of 676.2 mV, a J_{sc} of 41.6 mA/cm^2 and a FF of 78.5 % [128], [134].

5.2. Counterdoping in polycrystalline silicon

For the evaluation of counterdoping in poly-Si, ion-implanted test structures are fabricated with the process for poly-Si contacts without counterdoping that showed the best results (see section 4.3 and table A.4). In all counterdoping experiments, the phosphorus implantation dose is higher than the boron dose. The structuring of locally counterdoped regions is conducted with the same shadow masks as for the *c*-Si case.

5.2.1. Full area counterdoping

Figures 5.12 a) and b) show the $J_{0,poly}$ and ρ_{rel} values of the phosphorus implanted poly-Si test structures already presented in section 4.3 together with values of full area counterdoped test structures. The $J_{0,poly}$ values of the counterdoped test structures are comparable to the only phosphorus implanted samples, or in some cases even lower. However, the high values of ρ_{rel} for some counterdoped test structures show that for these samples no good contact is achieved. Figure 5.13 shows ECV measurements of the test structures. It can be seen that, due to the higher implanted phosphorus doses, the poly-Si layer is always effectively *n*-doped, but even for comparably low boron doses, the effective doping profile

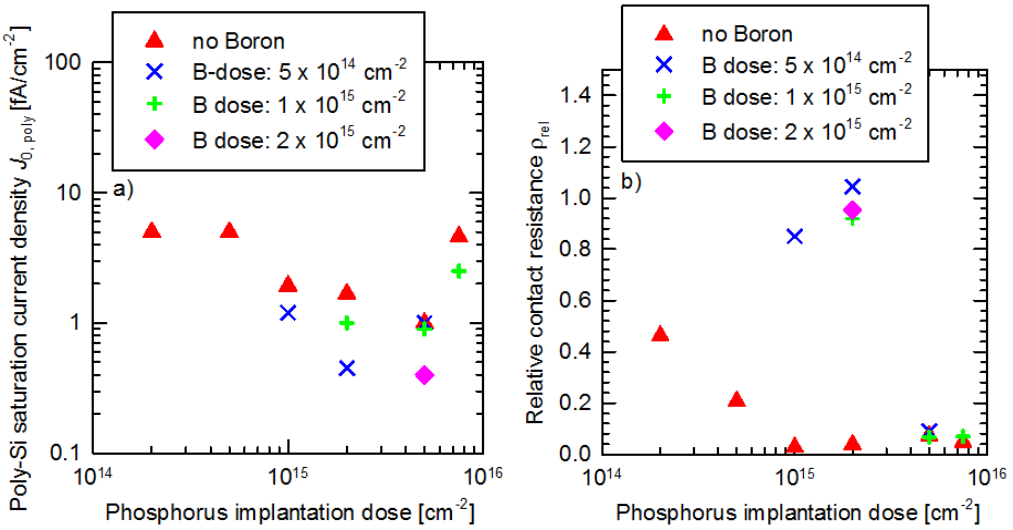

Figure 5.12.: a) $J_{0,\mathrm{poly}}$ values and b) ρ_{rel} values of counterdoped poly-Si test structures implanted with different doses of boron and phosphorus. Also shown are only phosphorus doped samples.

in the *c*-Si wafer of some test structures exhibits regions with an effective *p*-type doping near the surface. The reason for this behavior is the much larger (about two orders of magnitude) diffusion constant of boron compared to phosphorus in SiO_2 [135] (see also the doping profiles in section 4.3). For the test structures exhibiting *p*-type interlayers, the contact between the effectively *n*-doped poly-Si layer and the *n*-type wafer is blocked. This explains the high ρ_{rel} values of these samples. From the conducted experiments it can be followed that with a phosphorus dose of ~ 5 times the boron dose, counterdoping will be possible. The low values of ρ_{rel} for these samples show that strong phosphorus doping seems to hinder the boron diffusion to the SiO_2 layer and into the wafer. This is in accordance with the observations of Schrof *et al.* [136], who found a reduction of the boron diffusion in heavily phosphorus doped silicon. At P surface concentrations of $\sim 2 \times 10^{20}\,\mathrm{cm}^{-3}$ they observed a nearly complete blocking of a B diffusion from a borosilicate glass layer into the wafer.

Despite the comparable $J_{0,\mathrm{poly}}$ value of $1.0\,\mathrm{fA/cm^2}$ and therefore comparable surface recombination behavior of the best phosphorus implanted and the best full area counterdoped test structure (see figure 5.12), the comparison of the lifetime curves shows considerable differences (see figure 4.12 and figure 5.14).

The $V_{\mathrm{oc,impl}}$ value of 742 mV is the same as the one of the phosphorus doped test structure, but due to the $\tau_{\mathrm{SRH,bulk}}$ value of 9 ms (compared to 40 ms for the only phosphorus implanted sample) the dominating recombination mechanism at MPP_{impl} is the SRH recombination of the wafer in high level injection with an ideality factor of two, leading to a pFF_{impl} of only 84.7 % in contrast to the 87.3 % of the only phosphorus doped test structure.

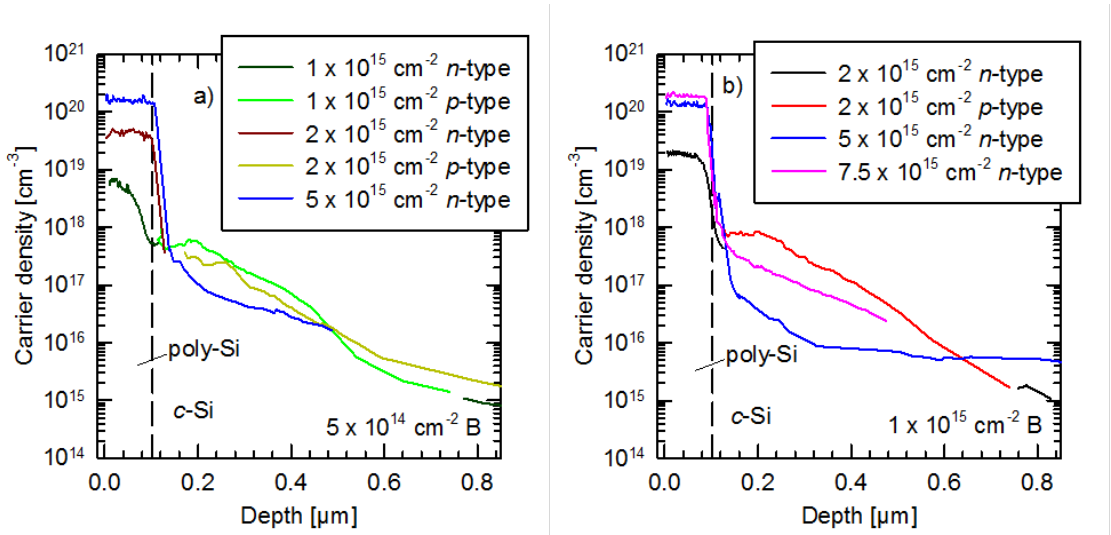

Figure 5.13.: ECV measurements of counterdoped test structures, with an implanted boron dose of a) $5 \times 10^{14}\,\mathrm{cm}^{-2}$ and b) $1 \times 10^{15}\,\mathrm{cm}^{-2}$ and phosphorus doses as specified in the legends. For some samples effectively p-doped regions are formed between the n^+ poly-Si and the n-type wafer.

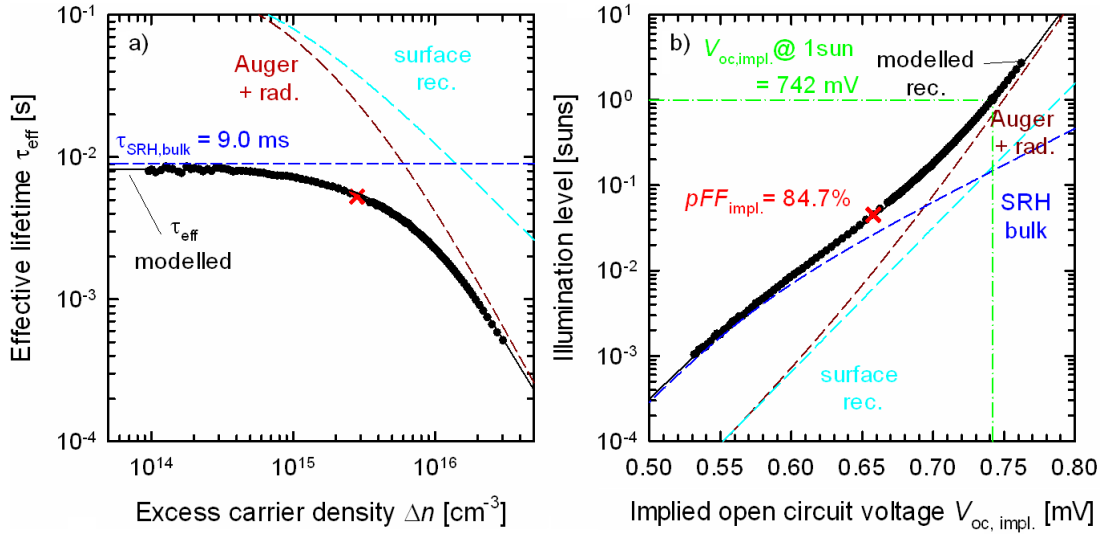

Figure 5.14.: a) τ_{eff}-Δn curve and b) suns-$V_{\mathrm{oc,impl}}$ curve of a poly-Si test structure, implanted with boron (dose: $1 \times 10^{15}\mathrm{cm}^{-2}$) and overcompensated implanted with phosphorus (dose: $5 \times 10^{15}\mathrm{cm}^{-2}$). The black circles are measured values, the lines modeled. The red cross marks the implied maximum power point (MPP_{impl}).

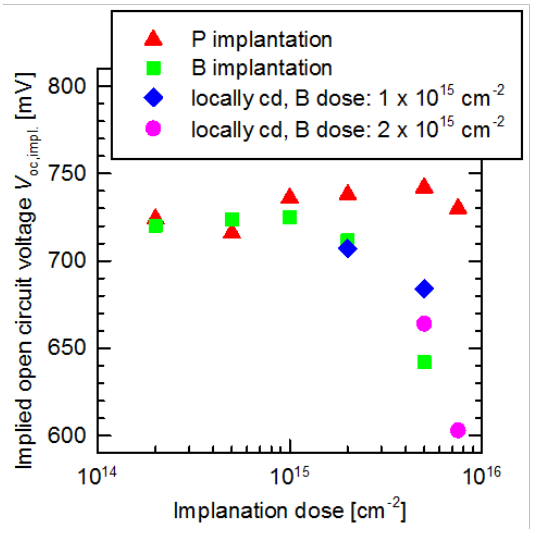

Figure 5.15.: $V_{\mathrm{oc,impl}}$ values of full area boron implanted and locally with phosphorus counterdoped implanted poly-Si test structures. Also shown are only phosphorus and only boron doped poly-Si test structures. For the locally counterdoped test structures the phosphorus dose is given by the X-axis value, while the boron dose is shown in the legend. As a result the boron doped test structures with the same boron doses are shown at different intercepts on the X-axis as the counterdoped test structures.

The reason for the lower bulk lifetime is as unclear as for the case of the boron doped test structure (see the discussion in section 4.4). Following the gettering hypothesis, this behavior would mean that the implantation of boron somehow reduces the gettering efficiency of phosphorus doped poly-Si layers. Further investigations would be needed to assess the plausibility of this hypothesis.

5.2.2. Patterned counterdoping

As the counterdoping of boron implanted poly-Si layers with phosphorus implantation is capable to produce low ρ_{rel} values and $J_{0,\mathrm{poly}}$ values comparable to only phosphorus implanted test structures, it seems to be a good idea to transfer this process to BJBC-like test structures. Therefore, locally counterdoped test structures are fabricated and analyzed. Unfortunately, the recombination characteristics of these samples differ strongly from the full area counterdoped test structures. As one consequence, the extraction of $J_{0,\mathrm{poly}}$ values with the method of Kane and Swanson [96] is not possible. Therefore, implied open circuit voltages are used in figure 5.15 for the comparison with other test structures. The $V_{\mathrm{oc,impl}}$ values of the locally counterdoped poly-Si test structures are strongly degraded compared to the full area implanted test structures doped. The $V_{\mathrm{oc,impl}}$ values of the full area counterdoped test structures (not shown here) are comparable to the only phosphorus implanted test structures.

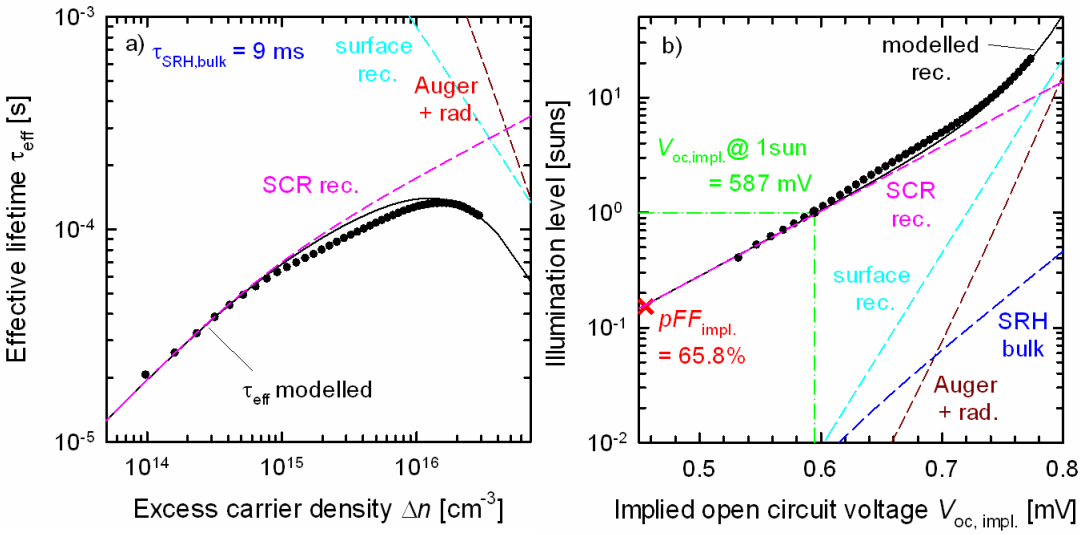

Figure 5.16.: a) τ_{eff}-Δn curve and b) suns-$V_{\mathrm{oc,impl}}$ curve of a full area boron-implanted (dose: $2\times10^{15}\,\mathrm{cm}^{-2}$) poly-Si test structure, locally overcompensated by ion implanted phosphorus (dose: $7.5\times10^{15}\,\mathrm{cm}^{-2}$). The black circles are measured values, the lines modeled. The red cross marks the implied maximum power point (MPP_{impl}).

For an understanding of the recombination mechanism responsible for the degradation of the locally counterdoped test structures, the injection dependent lifetimes and the suns-$V_{\mathrm{oc,impl}}$ curves of the counterdoped test structures showing the lowest and the highest $V_{\mathrm{oc,impl}}$ value are analyzed in the following and compared to a solar cell precursor fabricated with counterdoping in *c*-Si.

Figures 5.16 a) and b) show the injection dependent lifetime curve and the suns-$V_{\mathrm{oc,impl}}$ curve of a test structure exhibiting a full area boron-implantation with a dose of $2\times10^{15}\,\mathrm{cm}^{-2}$ which is locally overcompensated by an in-situ patterned phosphorus implantation with a dose of $7.5\times10^{15}\,\mathrm{cm}^{-2}$. As already indicated by the $V_{\mathrm{oc,impl}}$-values in figure 5.12, the resulting recombination characteristics are much worse than for the test structures exhibiting blanket implantations. The measured curves can only be fitted properly by adding an additional recombination mechanism with an ideality factor $n > 1$. According to the SRH statistics for a single trap level in the band gap, the ideality factor resulting from space charge region (SCR) recombination should be between one and two [132]. In real semiconductor devices several factors can lead to even higher ideality factors, e.g., coupled defects in a high defect region [137] or an resistively isolated region with high recombination [138]. Here, both cases could be present. When using a one-diode model with the ideality factor as fitting parameter for the modeling of the SCR recombination, the best fit is obtained with an ideality factor of $n = 3$. An advanced model is described in section 5.2.3, where the SCR recombination is investigated in more detail. Due to the non-ideal recombination behavior of this test structure, the extraction of the bulk

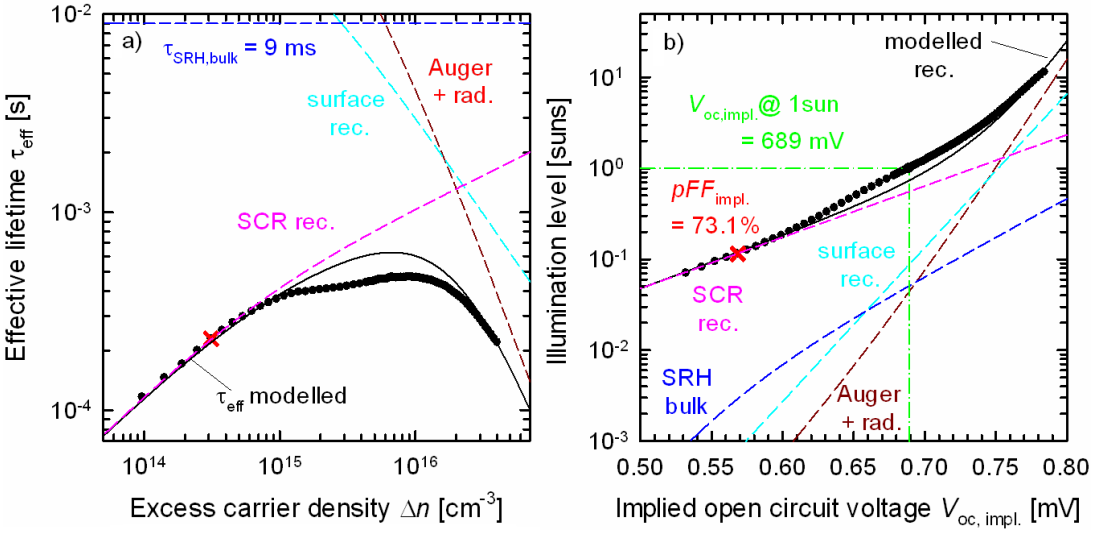

Figure 5.17.: a)τ_{eff}-Δn curve and b) suns-$V_{\mathrm{oc,impl}}$ curve of a full area boron-implanted (dose: $1 \times 10^{15}\,\mathrm{cm}^{-2}$) poly-Si test structure, locally overcompensated by ion implanted phosphorus (dose: $5 \times 10^{15}\,\mathrm{cm}^{-2}$). The implantation doses are lower than in the sample shown in figure 5.16. The black circles are measured values, the lines modeled. The red cross marks the implied maximum power point (MPP_{impl}).

lifetime in low level injection is not possible. Therefore the bulk lifetime of the full area counterdoped test structure (see figure 5.14) is used. The high and non-ideal recombination of the sample results in a $V_{\mathrm{oc,impl}}$ of 587 mV and a pFF_{impl} of 65.8 % (the latter value is extrapolated from the fitted curve). This recombination behavior is clearly not suited for solar cell approaches.

Applying the counterdoping process on a poly-Si test structure with lower boron and phosphorus doses (1×10^{15} cm^{-2} and 5×10^{15} cm^{-2}) results in strongly improved recombination characteristics compared to the previous test structure. Figure 5.17 shows the corresponding measurements. Again the test structure is limited by non-ideal ($n = 3$) recombination at MPP_{impl}, but the resulting pFF_{impl} of 73.1 % and the $V_{\mathrm{oc,impl}}$ of 689 mV are much higher than in the stronger doped test structure. Considering the case of a solar cell, the contributions from the surface recombination and the SCR recombination would be halved (as the test structures are symmetric), resulting in a pFF_{impl} of 74.9 % and a $V_{\mathrm{oc,impl}}$ of 714 mV. Reducing the implantation doses further could possibly result in an even lower SCR recombination contribution.

As a reference for the case with a rather high lifetime in the space charge region the recombination characteristics of a solar cell precursor with counterdoping via ion implantation in a *c*-Si wafer are measured. This wafer receives a comparable treatment as the test structures described in section 5.1: full area boron implantation (dose: $1.5 \times 10^{15}\,\mathrm{cm}^{-2}$), patterned phosphorus implantation (dose: $5 \times 10^{15}\,\mathrm{cm}^{-2}$) and a high temperature co-

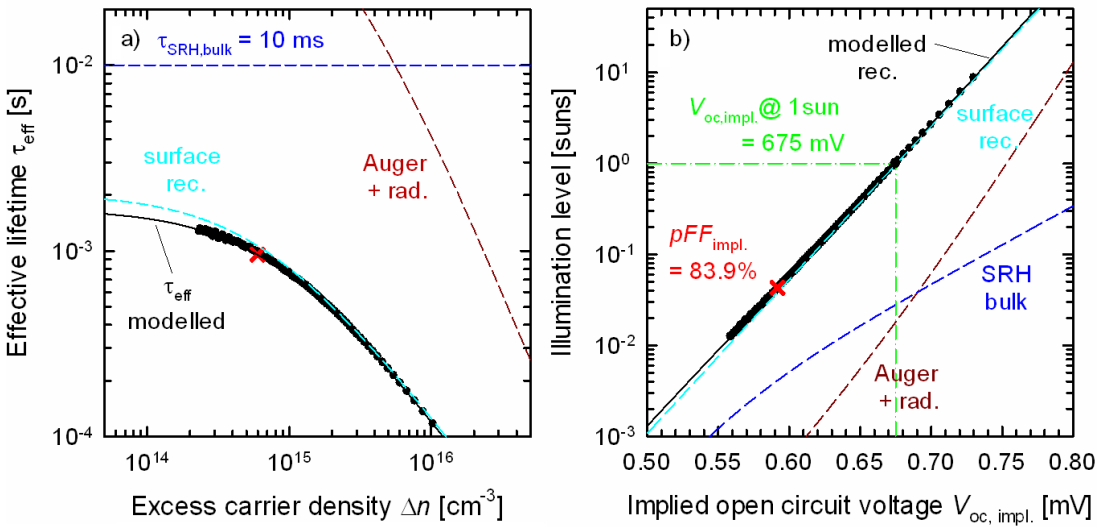

Figure 5.18.: a) τ_{eff}-Δn curve and b) suns-$V_{\mathrm{oc,impl}}$ curve of a full area boron-implanted *c*-Si cell precursor, locally overcompensated by ion implanted phosphorus. The measured curves are recalculated to account for the single sided doping (see text for the details). The black circles are measured values and the lines modeled. The red cross marks the implied maximum power point (MPP_{impl}).

annealing step (80 min, 1050 °C) for the reduction of the implantation damage. The same shadow mask and a comparable annealing process as for the diode test structure fabrication are used. As this wafer is a solar cell precursor, the doping is only conducted on the rear side. The front side exhibits no diffused front surface field and is passivated with an AlO_x/SiN_x-stack. For a better comparability with the symmetrically doped poly-Si test structures the measured curves in figure 5.18 are modified by doubling the surface recombination term in the modeled curves and recalculating the measured values accordingly. The recalculation of the data does assume the contribution from the front side to be negligibly small.

The τ_{eff}-Δn curve and the suns-$V_{\mathrm{oc,impl}}$ curve of this wafer show a very ideal recombination behavior, dominated by surface recombination with $n = 1$. No additional recombination mechanism accounting for recombination in the SCR has to be added. These observations support the assumption that the high recombination in the patterned counterdoped poly-Si test structures is caused by recombination in the lateral *pn*-junction in the highly defective poly-Si layer, while the lifetime in the *c*-Si *pn*-junction is obviously sufficiently high.

5.2.3. Modeling the SCR recombination in poly-Si

The experiments in the previous sections have shown that the excellently passivating poly-Si junctions stop being excellent, when two polarities of poly-Si touch. In this section an approach to model the recombination in the lateral diode in the poly-Si layer is presented

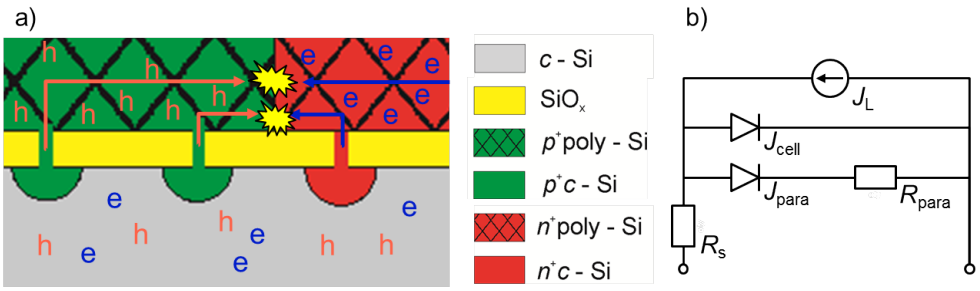

Figure 5.19.: a) Sketch of a *pn*-junction inside a poly-Si contact, featuring an oxide with pinholes and semi-spherically doped regions in the *c*-Si wafer under the pinholes. While almost only holes can penetrate the oxide under the *p*-type poly-Si region and only electrons can penetrate the oxide under *n*-type poly-Si region, the charge carriers can recombine in the touching region. The arrows indicate the current paths of the charge carriers. b) Equivalent circuit diagram accounting for the recombination in the poly-Si layer and the series resistance for this recombination path.

and the main parameters influencing the magnitude of this parasitic recombination are identified. Figure 5.19 a) shows a sketch of a lateral *pn*-junction in a poly-Si layer and the possible current paths of charge carriers generated in the touching *c*-Si layer. The scenario depicted in figure 5.19 a) can be modeled with an equivalent circuit (5.19 b)) consisting of the diode J_{cell} describing the recombination of a solar cell without touching regions in the poly-Si layer in combination with a parasitic diode J_{para} describing the recombination in the poly-Si layer. As the second diode is not in direct contact with the wafer a resistor R_{para} is connected in series to this diode. This resistor accounts for the contributions of the poly-Si / SiO_x / *c*-Si contact resistance and the sheet resistance of the poly-Si layer. R_{s} accounts for the series resistance of the solar cell and J_{L} for the photo generated charge carriers. For a PCD measurement, where the implied JV characteristics are determined from the inductively measured time dependent carrier density, no series resistance R_{s} is needed. The measured implied JV curve can then be described with

$$J_{\mathrm{meas}}(V) = J_{\mathrm{cell}}(V) + J_{\mathrm{para}}(V') \ , \tag{5.1}$$

where V' is determined from

$$V = V' + J_{\mathrm{para}}(V') \cdot R_{\mathrm{para}} \ . \tag{5.2}$$

In order to model the measurements on the locally counterdoped test structures shown in section 5.2.2 the recombination current density of the parasitic diodes has to be determined.

In thermal equilibrium, the recombination in the space charge region of an ideal, abrupt *pn*-junction in silicon with a much higher *n*-type than *p*-type doping, can be expressed as

$$J_{\mathrm{para}} = \frac{q\,W\,n_{\mathrm{i}}}{2\tau} e^{qV/2kT} \text{ [139]}, \tag{5.3}$$

where W is the width of the SCR, and is given by

$$W = \sqrt{\frac{2\epsilon kT}{q^2 N_{\mathrm{A}}} \ln\left(\frac{N_{\mathrm{A}} N_{\mathrm{D}}}{n_{\mathrm{i}}^2}\right)} \text{ [139]}, \tag{5.4}$$

with ϵ being the permittivity of Si. It can be seen that the main contributors to the recombination are the charge carrier lifetime and the doping density in the lower doped region.

As already pointed out in section 5.1, the as-implanted doping profile exhibits a rather large lateral grading of some micrometers. Additionally, the diffusion coefficient of phosphorus in poly-Si is more than a factor of 100 larger than in *c*-Si [140], which can result in an even larger lateral dopant grading. For the case of the ion implanted samples shown in section 5.2.2, where an annealing after implantation of 60 min at 1050 °C is used, this results in a lateral depth of $\sim 6\,\mu$m. In this approximation an infinite diffusion source and no lateral grading in the as-implanted profile are assumed and the lateral depth is the depth, where the dopant concentration reduces to a value of 1/5 of the peak dopant concentration, which is also the multiplier between the measured phosphorus and boron doping densities in the poly-Si layers of some typical counterdoped samples.

For this reason, 2D SENTAURUS device [105] simulations are conducted, where also arbitrarily shaped doping profiles can be simulated. In order to simulate not only the recombination directly in the space charge region, but also in the adjacent poly-Si regions, a rather large value of 50 μm is used for the height of the diode. For the doping densities in the *p*- and *n*-type regions, values from ECV measurements on full area implanted reference samples are used. At the *pn*-junction, a Gauss shaped doping profile with varied depth is used for the phosphorus dopant distribution, while the boron doping is assumed to be constant over the full depth. Figure 5.20 shows the dopant distribution and the recombination current density of a diode with a 10 μm deep gradient in the phosphorus profile and a charge carrier lifetime of 10^{-10}s. As can be seen, the total recombination current density is dominated by recombination in the SCR region and the recombination in the *n*- and *p*-type regions can be neglected. Figure 5.21 a) shows simulated IV-curves for varied SRH lifetimes in the simulation area. As expected from the case of abrupt junctions, the recombination current density increases steeply with decreasing lifetime. Depending on the fabrication method, values for the lifetime of CVD deposited poly-Si

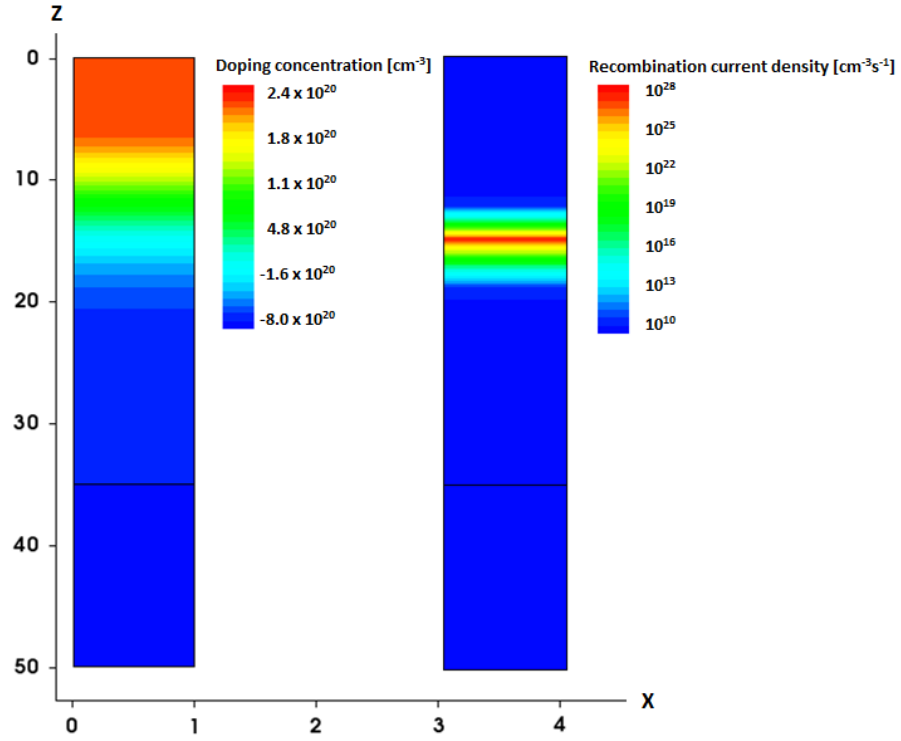

Figure 5.20.: Sketch of the unit cell used for the simulation of the lateral *pn*-junction in the poly-Si layer. In the unit cell on the left side the dopant distribution for a 10 μm deep phosphorus profile (after a 5 μm deep constant plateau) is shown. The unit cell on the right side shows the recombination current density for the same doping concentration and a lifetime of 10^{-10}s.

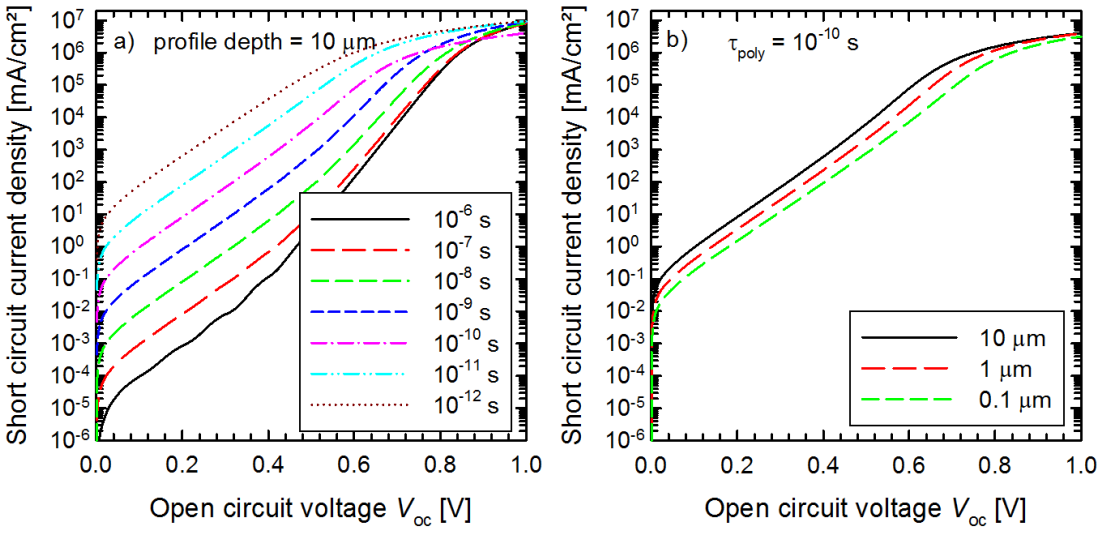

Figure 5.21.: Simulated IV-characteristics of diodes a) with varied SRH lifetime and b) with varied doping depth. The phosphorus peak concentration of all diodes is $3 \times 10^{20}\,\mathrm{cm}^{-3}$ and the boron concentration is $8 \times 10^{19}\,\mathrm{cm}^{-3}$.

layers, found in the literature are 2×10^{-11}s - 5×10^{-11}s [141], 2×10^{-12}s - 5×10^{-11}s [142], or 6×10^{-11}s [143].

Figure 5.21 b) shows the results from a variation in the doping depth. For an increasing depth, the current density increases. This behavior is reminiscent to the case of linearly graded junctions, where the SCR width is dependent from $(\ln(a)/a)^{1/3}$ [139], where a is the doping gradient. For steeper profiles, the SCR width and therefore the recombination current density will decrease.

The remaining quantity needed to implement these parasitic diodes into equation 5.1 is the series resistance R_{para}. This value is determined by additional 2D device simulations. Here, the unit cell consists of a 160 μm thick wafer with a resistivity of 6.5 Ω cm. For the length of the unit cell, 520 μm (half the distance between two BSF dots) is used. The BSF length is set to 88.4 μm, accounting for the BSF area fraction of $\sim$ 17 %. The layout of the poly-Si contacts is implemented analogously to the 4PP simulations shown in section 3.2.8: A thin region of low conductance is sandwiched between the wafer region and another thin region accounting for the poly-Si layer. For the region with low conductance a thickness of 20 nm is used to ensure stable running simulations. A constant doping profile in the poly-Si and oxide region is used, with a height and a diffusion into the wafer according to ECV measurements of the samples shown in section 4.3. The contact resistance between poly-Si and wafer is determined by the doping density and the charge carrier mobility in the sandwiched region. For the poly-Si layer an electron mobility of 10 cm^2/Vs and a hole mobility of 30 cm^2/Vs are used [144], [145]. R_{para} is determined by applying two contacts on either side of the lateral pn-junction and simulating a light-IV measurement. In order

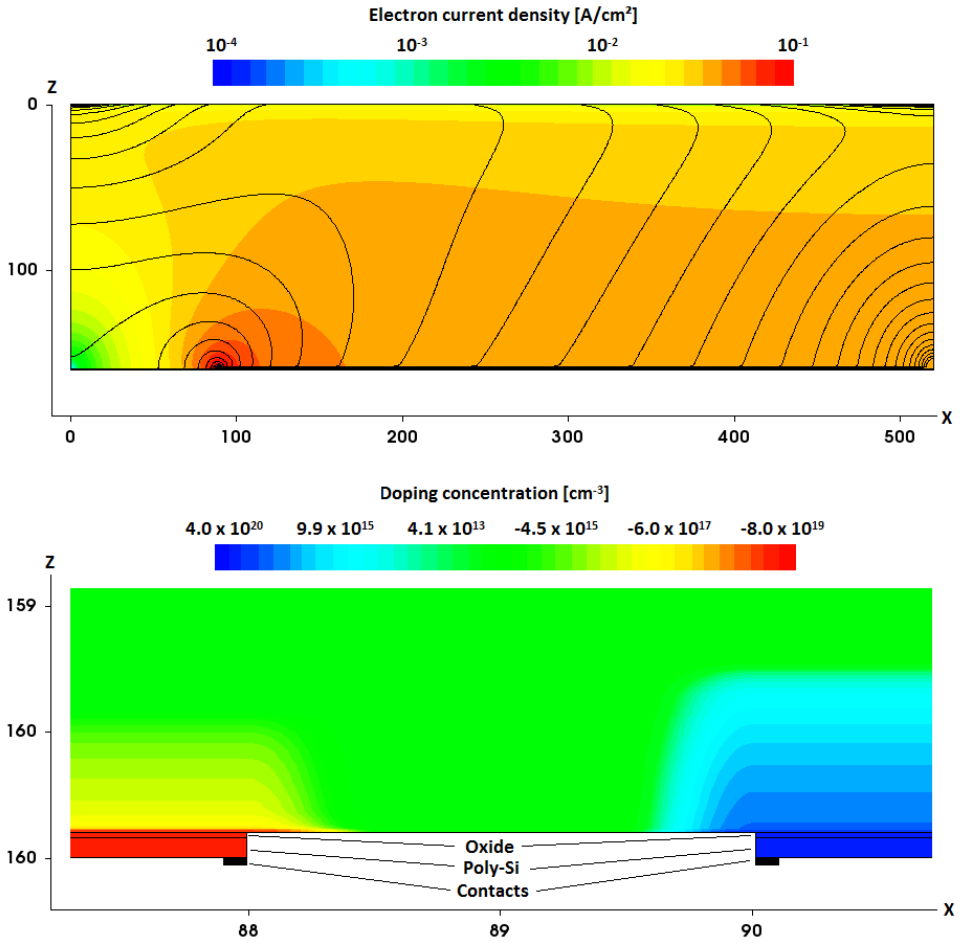

Figure 5.22.: Upper figure: Sketch of the unit cell used for the simulation of the series resistance of the parasitic diode in the poly-Si layer. The electron current density is color coded, the hole current density is shown by the contour lines. The lower figure shows a magnification of the region with the contacted areas. The doping concentration is color coded.

to omit a shunt between the neighboring contacts and to only measure the current path through the wafer, 2 μm of the poly-Si region between the contacts are removed. Both contacts are 100 nm large and thus as large as the poly-Si thickness. Figure 5.22 shows a sketch of the simulation area.

In order to model the measured characteristics of the locally counterdoped sample shown in figure 5.16 the characteristics of a diode with a doping profile depth of 10 μm is used for J_{para}. The lifetime of the diode and the series resistance used for R_{para} are varied to match the measured curve best. Using the area weighted $J_{0,\mathrm{poly}}$ values of the full area implanted boron doped and counterdoped samples and a bulk lifetime of 9 ms together with the Auger contribution for a 160 μm thick 6.5 Ω cm wafer for J_{cell}, equations 5.1 and 5.2 should represent the measurements of the locally counterdoped test structures. Figure 5.23 a) shows the measured and the modeled suns-$V_{\mathrm{oc,impl}}$ curves together with

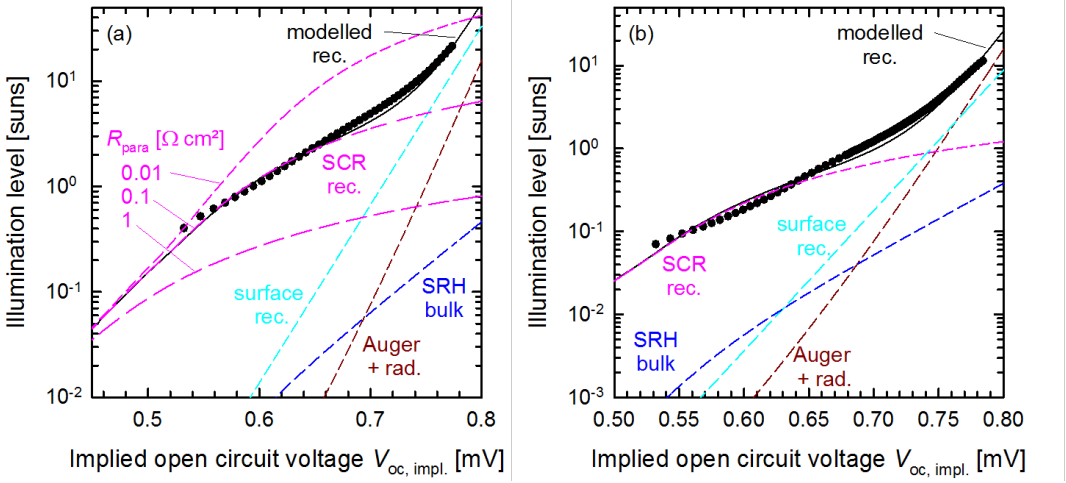

Figure 5.23.: suns-$V_{oc,impl}$ curves of full area boron-implanted (doses: a) $2 \times 10^{15}\,cm^{-2}$, b) $1 \times 10^{15}\,cm^{-2}$) poly-Si test structures, locally overcompensated by ion implanted phosphorus (doses: a) $7.5 \times 10^{15}\,cm^{-2}$, b) $5 \times 10^{15}\,cm^{-2}$). The black circles are measured values, the lines modeled.

the single contributions. The best agreement between modeled and measured curve is obtained with a lifetime of 10^{-8} s and $R_{para} = 100\,\Omega\,cm^2$. The contribution of J_{para} is shown for various values of R_{para}. $R_{para} = 100\,m\Omega\,cm^2$ corresponds to an interface contact resistance of $54\,m\Omega\,cm^2$. Applying the same procedure for the locally counterdoped sample with lower implantation doses (shown in figure 5.17) results in the modeled curve shown in figure 5.23 b), with a lifetime of 10^{-7} s in the poly-Si layer and an interface contact resistance of $490\,m\Omega\,cm^2$.

Despite the good matching of the modeled and the measured suns-$V_{oc,impl}$ curves, it is questionable, why different lifetimes in the poly-Si layer have to be used to get a good overlap between measurement and model. Also, in both cases, the used lifetimes are much higher than the lifetime values of poly-Si layers found in the literature ($< 10^{-10}$s [141]–[143]). One explanation for the generally higher lifetime in this work could be due to the very high annealing temperatures of 1000 °C applied after the poly-Si deposition, possibly leading to a growth of grains and therefore to a reduction of the grain boundary density. Also, Dutoit and Sollberger [142] have observed an increase in the lifetime of their poly-Si layers from 2×10^{-12} s to 5×10^{-11} s with increasing poly-Si resistivity from 5 mΩ cm to 500 mΩ cm. In this work, the resistivities of the boron doped poly-Si layers are 2.6 mΩ cm and 1.5 mΩ cm for implantation doses of $1 \times 10^{15}\,cm^{-2}$ and $2 \times 10^{15}\,cm^{-2}$, respectively. This dependency might also explain the difference in the lifetime between the two samples.

The values used for the interface contact resistance in the modeled curves are surprisingly similar to the expected values: For the sample with the lower implantation dose, a value

of 310 $\mathrm{m\Omega\,cm^2}$ is obtained with the 4PP method on a full area counterdoped sample. For the sample with the higher implantation dose the full area counterdoped reference sample got broken before completion, but the value of an only P-implanted sample with a dose of $7.5 \times 10^{15}\,\mathrm{cm^{-2}}$ is 70 $\mathrm{m\Omega\,cm^2}$ (see figure 4.10).

Summary and Discussion

The experiments shown in this section demonstrate that despite the excellent passivation quality of homogeneously doped poly-Si layers, the high defect density of the poly-Si complicates the implementation of adjacent *p*- and *n*-type regions in one poly-Si layer. Nevertheless, the magnitude of this recombination can considerably be reduced, by a reduction of the implantation doses. Modeling the recombination characteristics with an equivalent circuit model including a resistively coupled parasitic diode yields the conclusion that the main factor for the reduction is an increase in the lifetime of the poly-Si layers with decreasing doping density. In order to further decrease the parasitic recombination, the implantation doses could be reduced even further. Unfortunately figure 4.6 a) and 4.21 imply that a reduction of the doping density leads to a decrease of the carrier selectivity of the poly-Si layer and therefore to an increase of $J_{0,\mathrm{poly}}$. Also the interface contact resistance between the poly-Si and the wafer increases with decreasing implantation dose (see figure 4.6 b)), implying an increase in the series resistance of solar cells fabricated with this process.

As possible compromise the implementation of an undoped or lowly doped region between the highly doped *p*- and *n*-type poly-Si contacts is investigated in the following.

5.2.4. Patterned counterdoping with lowly doped *pn*-junction

With the aim to reduce the doping density at the *pn*-junction, but maintaining the good passivation quality of highly doped poly-Si on the larger part of the wafer a new set of test structures is fabricated. The processing is similar to the processing of the locally counterdoped samples presented in section 5.2.2, but instead of masking only the phosphorus implantation, both implantation steps are masked. The aligned masked implantation is conducted at Applied Materials Inc., Gloucester, MA, USA. Figure 5.24 shows a microscope image of a control wafer used to monitor the alignment accuracy. Both implantation areas are line shaped, with a width of 550 μm for the boron implantation and a width of 300 μm for the phosphorus implantation. For the implantation doses $1 \times 10^{15}\,\mathrm{cm^{-2}}$ of boron and $5 \times 10^{15}\,\mathrm{cm^{-2}}$ of phosphorus are used. The gap between the implanted areas has a width of 75 μm. The gap area is either kept undoped or is doped by a full area implantation with a dose of $5 \times 10^{13}\,\mathrm{cm^{-2}}$, $1 \times 10^{14}\,\mathrm{cm^{-2}}$ or $2 \times 10^{14}\,\mathrm{cm^{-2}}$ of phosphorus. Additionally, for the comparison with previous experiments, a test structure with full area boron implantation and masked phosphorus implantation is fabricated. As

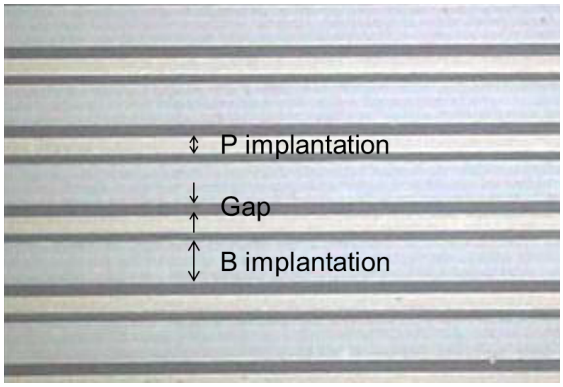

Figure 5.24.: Optical microscope image of a Si wafer implanted with BF_2 through two shadow masks. The thinner lines belong to the phosphorus implantation mask, the wider lines to the boron implantation mask. The implanted area is amorphized and therefore, the optical properties change in contrast to the undoped regions.

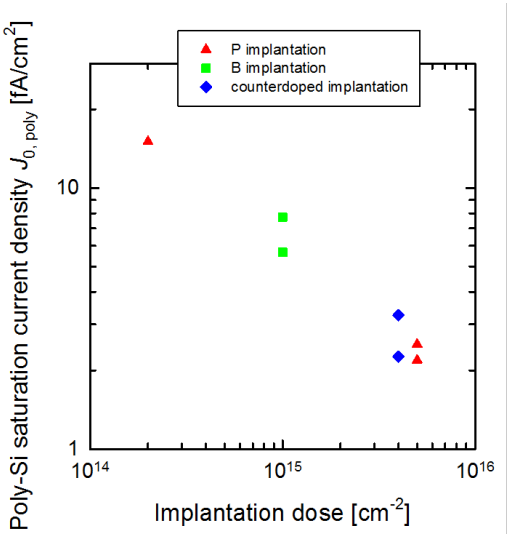

Figure 5.25.: $J_{0,\mathrm{poly}}$ values of full area implanted poly-Si test structures for different implantation doses. For the counterdoped samples the effective implantation dose is shown on the X-axis.

described in section 3.2.4, PCD measurements with a coil based inductive determination of the conductance are not suitable for samples with line shaped doping. Therefore, PCPLI is used to measure the recombination characteristics of these samples.

Figure 5.25 shows the $J_{0,\mathrm{poly}}$ values of full area implanted references. As expected from the dose dependence of $J_{0,\mathrm{poly}}$ shown in figure 4.6 a), $J_{0,\mathrm{poly}}$ increases rapidly with lower phosphorus implantation doses. For the two lowest doses of $5 \times 10^{13}\,\mathrm{cm}^{-2}$ and $1 \times 10^{14}\,\mathrm{cm}^{-2}$ no lifetime curve could be measured, which indicates an only negligible surface passivation quality.

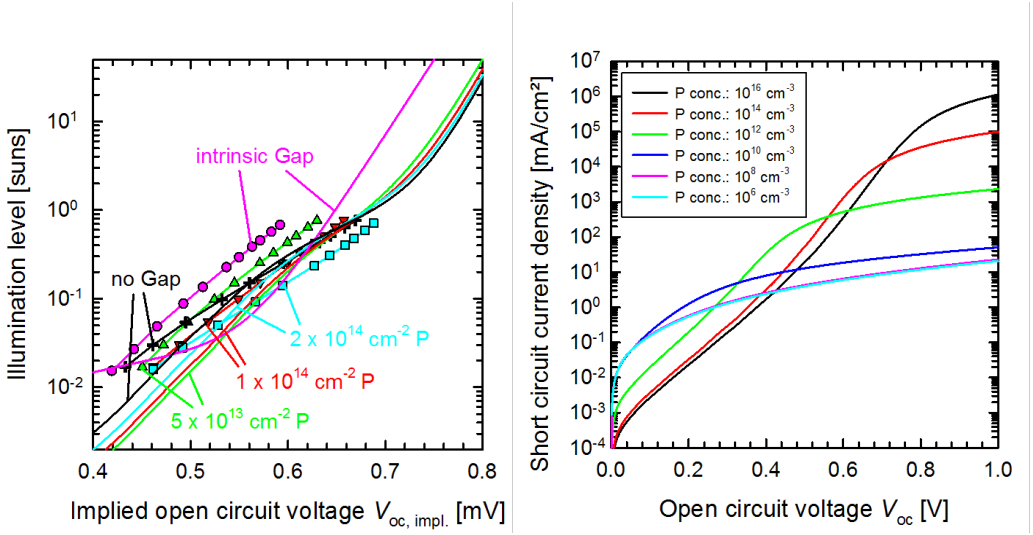

Figure 5.26.: a) suns-$V_{\mathrm{oc,impl}}$ curves of counterdoped test structures with a gap between the highly doped p- and n-type poly-Si regions. Curves with symbols represent measured values for different doping densities. The implantation doses used for doping of the gap region are given in the graph. Curves without symbols represent modeled curves. b) Simulated diodes with a variation in the doping density in the gap-region.

In figure 5.26 a) the measured suns-$V_{\mathrm{oc,impl}}$ curves of the patterned implanted samples are shown together with modeled curves. For the modeling, the lifetime and interface contact resistance values according to the values used for the modeling of the patterned counterdoped sample with the lower implantation doses ($1\times10^{15}\,\mathrm{cm}^{-2}$ of boron and $5\times10^{15}\,\mathrm{cm}^{-2}$ of phosphorus) are used: $\tau_{\mathrm{poly}} = 10^{-8}\,\mathrm{s}$ and $\rho_{\mathrm{int}} = 76\,\mathrm{m\Omega\,cm}^2$. The diodes are simulated with a $75\,\mu$m deep region between the boron and phosphorus doped region and $10\,\mu$m deep diffusion profiles for both, the boron and the phosphorus doped regions. The gap region is kept either undoped, or doped according to the implantation doses used in the experiment. For the $J_{0,\mathrm{poly}}$ values of the wafers, the area weighted mean values of the individual contributions are used. For the phosphorus implantation doses of $5\times10^{13}\,\mathrm{cm}^{-2}$ and $1\times10^{14}\,\mathrm{cm}^{-2}$, where $J_{0,\mathrm{poly}}$ could not be measured, a linear relationship in the double logarithmic plot shown in figure 5.25 is assumed to interpolate the $J_{0,\mathrm{poly}}$ values. The resulting values are $35\,\mathrm{fA/cm}^2$ and $23\,\mathrm{fA/cm}^2$, respectively. For the sample with an intrinsic gap a value of $1000\,\mathrm{fA/cm}^2$ is used. Even though these values might be far from being accurate, in the range accessible with the measurement setup, at least for samples with a doped gap region the $J_{0,\mathrm{poly}}$ value has only limited impact on the modeled curves.

A comparison between measurement and model shows that the differences between the differently doped gap regions is not described properly by the used model. While the simulations imply a decrease in the recombination current density for lower doping

densities in the gap region, the opposite is the case for the measured samples. In these simulations the lifetime of the doped region is kept constant. If assuming higher lifetimes for lower doping densities (as observed by [142] and as performed in the previous section), this would even enhance the difference between the model and the measurements.

Figure 5.26 b) shows simulated diodes with a variation of the doping density in the gap region. When the doping density is reduced to much lower values than in the experiment, both, the SCR width and the internal series resistance of the diodes increase. While the former results in an increased recombination current density, the latter limits the recombination for higher current densities. Therefore, for the simulated diodes with an undoped gap or a very low doping density in the gap region, the total recombination current density at values above 600 mV is not affected by the parasitic diode, but only by the $J_{0,\mathrm{poly}}$ value of the individual regions. In the experiments the contrary is observed, here the samples with an undoped gap show the highest recombination current densities.

A possible reason for the different behavior of the modeled curves and the measurements could be the neglecting of the charge carrier current entering the poly-Si layer directly through the oxide in the gap region, which is not regarded in the diode simulations, but could play a role for the 75 μm wide gaps (15 % of the total area). For lower implantation doses, the interface contact resistance of the minority charge carriers is expected to decrease (see figure 4.21), which would explain the higher recombination current densities observed for the samples with a lower doping density in the gap region.

The most important observation of this experiment is that, at least with the experimental approach used here, samples fabricated with an undoped or lowly doped gap at the lateral *pn*-junction do not perform better over the whole voltage range than samples with the much simpler counterdoping approach.

Outlook

Even though the addition of an intrinsic or lowly doped gap region at the lateral *pn*-junction does not improve the junction characteristics in the experiments shown in this work, Young *et al.* [146] demonstrated that it is possible to fabricate intrinsic poly-Si contacts that provide a high passivation quality with J_0 values below 20 fA/cm^2. Poly-Si layers with these properties would considerably improve the recombination characteristics of *pn*-junctions with an undoped gap. Further, the lateral series resistance could be enhanced by using thinner poly-Si layers. This would result in a reduction of the parasitic recombination, even for patterned counterdoped poly-Si layers with directly touching highly doped *p*- and *n*-type regions.

An alternative solution to reduce the parasitic recombination would be the selective removal of the poly-Si in the *pn*-junction region [48]. This solution would also imply

further process complexity, but e.g. an additional alignment step could be omitted, if this process would be performed after the metalization, e.g. together with the contact separation step. In simple BJBC solar cell layouts, the metal layer of one polarity will only cover doped regions of the same polarity. Therefore the contact separation between the metal fingers of different polarity will be at the same position as lateral *pn*-junction in the solar cell. By using appropriate etchants, it would be possible to not only remove the metal layer in this region, but also possible dielectric interlayers and the poly-Si layer. Of course this process sequence would also imply the need for an additional passivation step in the gap region after the poly-Si removal.

Chapter 6

Back junction back contacted solar cells with poly-Si BSF

Even though, the fabrication of BJBC solar cells with counterdoped poly-Si layers has not been successfully conducted in this work, the n-type poly-Si contacts developed in chapter 4 have been applied as BSF on a different type of BJBC solar cells.

In this section, n-type BJBC solar cells are fabricated from symmetric n^+ poly-Si / n c-Si / n^+ poly-Si test structures. Three test structures from the experiment shown in section 4.3, with implantation doses of $1 \times 10^{15}\,\mathrm{cm}^{-2}$, $2 \times 10^{15}\,\mathrm{cm}^{-2}$, and $5 \times 10^{15}\,\mathrm{cm}^{-2}$ are chosen. For the cell fabrication, the RISE process (see references [129], [147]) is chosen. The process sequence is shown in figure 6.1, starting with the symmetric test structures. On the rear side of the wafer a PECVD SiN_x layer is deposited and structured by laser ablation, leaving only the BSF regions protected by the SiN_x layer. Then a KOH solution is used to remove the poly-Si in the non-protected areas and additionally $7\,\mu$m of the c-Si, so that a step is formed at the BSF borders. The SiN_x layer stays on the BSF region and is used as diffusion barrier in a subsequent BBr_3 furnace diffusion resulting in a $60\,\Omega/\square$ emitter. This method implies a doping, not only in the trenches, but also at the edges so that the p^+ boron emitter touches the n^+ poly-Si BSF. The BSG and the SiN_x layer are removed with an HF dip. An ALD AlO_x and a PECVD SiN_x are deposited and serve as a passivation layer on the boron emitter and as a rear-side reflector on both the c-Si emitter and the poly-Si BSF. The dielectric stack is also used as a protection layer in a subsequent alkaline texturing step. The contact openings on the emitter and BSF regions are formed by local picosecond laser ablation of the dielectric layers. This step is especially challenging on the

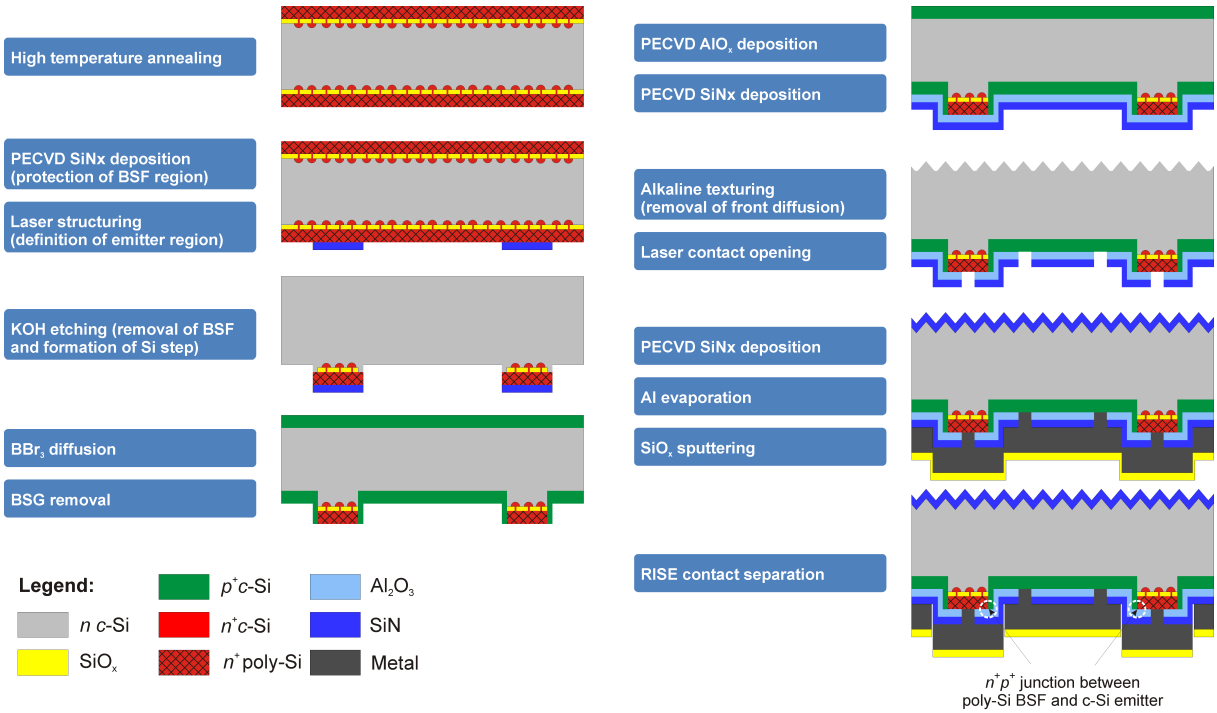

Figure 6.1.: Simplified process flow for the fabrication of n-type RISE BJBC solar cells with a poly-Si BSF.

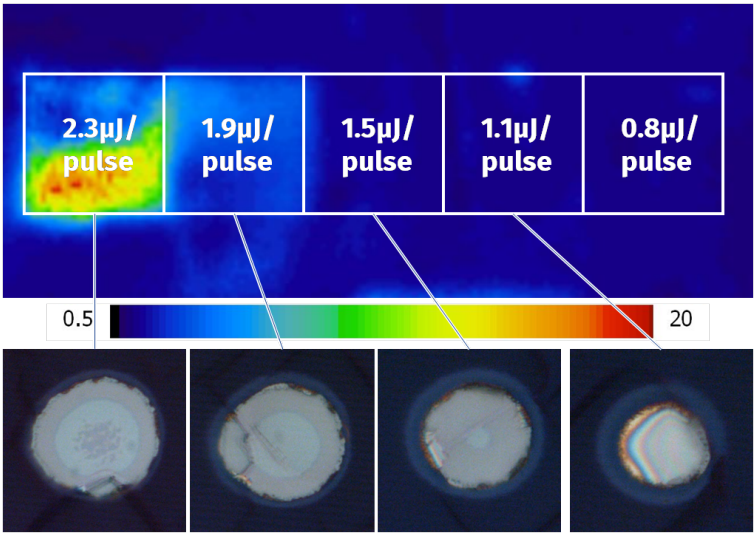

Figure 6.2.: Impact of full area laser ablation of a SiN_x layer on a n^+ poly-Si / n c-Si /n^+ poly-Si test structure. The color coding in the upper picture shows the ratio of the lifetime before and after laser ablation, measured by means of dyn. ILM. The lower picture shows optical microscope images of single laser contact openings.

rather thin poly-Si BSF regions, since damaging of the interfacial oxide has to be avoided. In figure 6.2 the lifetime ratio measured by means of dyn. ILM of a poly-Si test structure is shown before and after full area laser ablation of the dielectric stack. The laser pulse energy E_p is varied between 0.8 μJ and 2.3 μJ. It is found that for $E_\mathrm{p} > 1.9\,\mu$J the lifetime is reduced. In the lower part of figure 6.2 optical microscope images for $E_\mathrm{p} = 1.1$ - 2.3 μJ are shown. For $E_p = 0.8\,\mu$J no ablation of the dielectric layer is detected. For $E_p = 1.1\,\mu$J the ablated areas are very inhomogeneous in size and shape and thus not appropriate for the stable processing of solar cells. Therefore $E_p = 1.5\,\mu$J is chosen for the contact openings. After the contact opening process, a PECVD SiN_x passivation layer is deposited on the front side. The rear side is metalized by an evaporated Al layer, followed by the evaporation of a SiO_2 layer. The latter protects the Al during the RISE contact separation [148]: The wafers are subjected to hot phosphoric acid; at the steps between emitter and BSF, the SiO_2 protection layer does not cover the Al layer perfectly so that here the Al is etched and a contact separation between emitter and BSF metalization is formed. After a contact annealing step the cells can be measured.

On each 156 mm × 156 mm wafer 24 cells with an area of 2 cm × 2 cm are fabricated. Varied are the device geometry, i.e. the BSF index ranging from 450 μm to 1150 μm and the finger widths, resulting in emitter fractions from 66 % to 82 %. As reference, to the poly-BSF solar cells, also conventional n-type RISE cells are fabricated with $POCl_3$ and BBr_3 diffused junctions in c-Si. These reference cells also feature a full-area AlO_x / SiN_x passivation on both polarities on the rear side.

Measurement results Due to the good passivation quality of the n^+ poly-Si junctions compared to phosphorus diffused BSFs a strong improvement in the performance of the cells is expected. Besides the suppression of recombination at the BSF metal contacts, the poly-Si BSF does also imply lower recombination in the passivated regions since AlO_x does not provide a good passivation on n^+ doped c-Si regions [149]. Compared to the saturation current density of 1 fA/cm^2 for the poly-Si BSF, the conventional $POCl_3$-BSF exhibits saturation current densities of 202 fA/cm^2 when passivated with AlO_x. When exclusively considering the passivated BSF regions, a reduction in the J_{01} value of the total cell recombination current density between 30 fA/cm^2 and 67 fA/cm^2 is expected for the cells with BSF area fractions between 15 % and 33 %. This would correspond to an increase in the open circuit voltage between 7.5 mV and 14 mV.

However, this improvement is not observed in this experiment. Rather, the efficiency of 21.7 % for the best cell with poly-Si BSF is lower than the highest efficiency of 23.35 % measured on a reference cell with conventional BSF (see table 6.1). Even though the absolute J_sc values are not reliable for these measurements, a comparison between the samples measured with the same calibration is possible. While both cell types exhibit

	η [%]	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	pFF [%]	R_s(shift light $IV/J_{sc}V_{oc}$) [Ω cm^2]	J_{01} [fA/cm^2]	J_{02} [nA/cm^2]	R_{shunt} (fit $J_{sc}V_{oc}$) [kΩ cm^2]
best cell conventional BSF	23.35	677.5	42.74	80.7	82.23	0.37	146	6	317
best cell poly-Si BSF	21.7	673.6	42.1	77	78.8	0.4	112	33	8.5

Table 6.1.: Comparison of IV parameters of the best cell with poly-Si BSF and with conventional BSF, respectively. Both cells have a BSF index of 1150 μm and an emitter area fraction of 78 %. All data refer to in-house measurements on 3.96 cm^2 designated area. Due to the absence of appropriate reference cells for the calibration of the illumination density, the J_{sc} values are measured imperfectly and presumably too high (for both measurements).

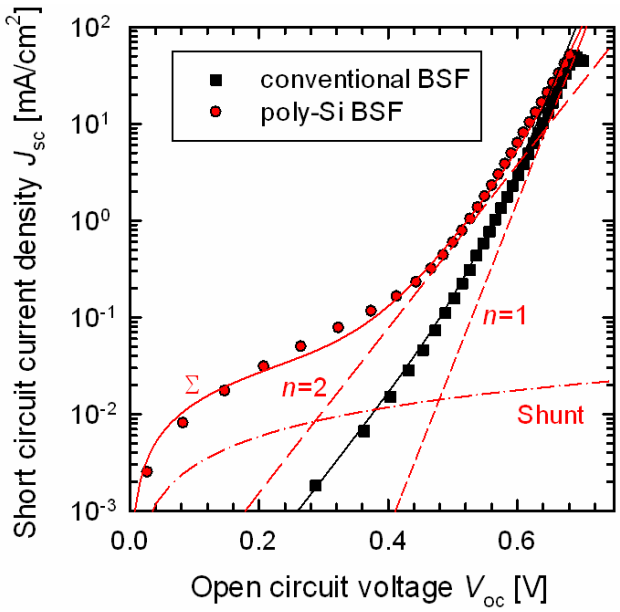

Figure 6.3.: J_{sc}-V_{oc} curves of the best cells with conventional BSF and poly-Si BSF and respective fits with a two-diodes-model. For the cell with poly-Si BSF, the single current contributions of the two-diodes-fit are shown (dashed red lines).

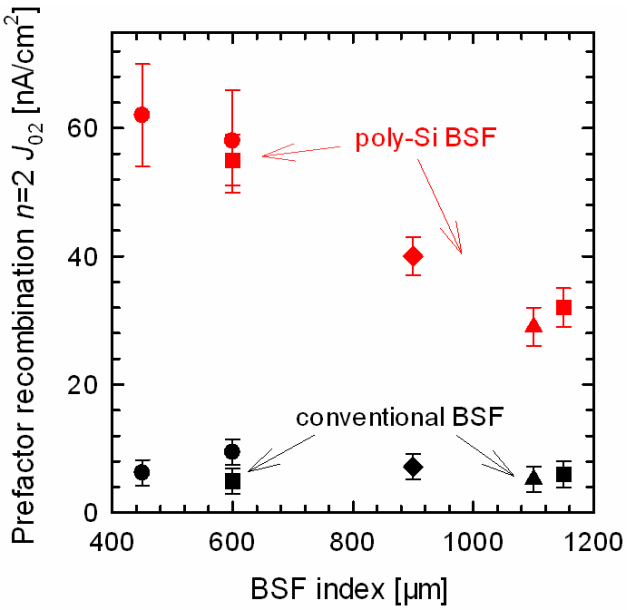

Figure 6.4.: J_{02} as a function of the BSF index (of the density of *pn*-junction lines) for cells with n^+ poly-Si BSF and cells with conventional *c*-Si BSF. Different symbols represent different emitter area fractions (circle 66 %, square 80 %, diamond 82 %, and triangle 85 %). All data refer to the best cells (in terms of efficiency) per group, respectively. On poly-Si BSF cells with slightly lower efficiency, even J_{02} values up to 150 nA/cm^2 are obtained.

comparable short circuit current densities and series resistance values, both, the open circuit voltage V_{oc} and the pseudo fill factor pFF of the n^+ poly-Si BSF cells are significantly lower than the values of the cells with conventional BSF. By fitting the $J_{sc} - V_{oc}$ curves of the solar cells with the two diodes model (see figure 6.3), the major reason for the worse cell performance of the poly-Si BSF cells can be attributed to a strongly increased J_{02} like recombination. It compromises both, V_{oc} and pFF significantly. When changing the J_{02} value of the fitted $J_{sc} - V_{oc}$ curve to 6 nA/cm^2 as in the case of the cell with conventional BSF, the V_{oc} value increases to 683 mV and the pFF value to 83.0 %.

Most likely the J_{02} like recombination can be attributed to the p^+n^+ junction meander between the n^+ poly-Si and the p^+ *c*-Si emitter, like in the experiments shown in section 5.2. This hypothesis is supported by the fact that the J_{02} values correlate well with the BSF index, i.e., the areal density of p^+n^+ junction lines between the emitter and BSF region (see figure 6.4). Different emitter (BSF) area fractions do not show an influence on J_{02}.

The formation of a lateral *pn*-junction in the poly-Si layer is in this process flow an artifact of the BBr_3 diffusion which results in a conformal doping at the edges of the trenches between emitter and BSF and also in the border region of the poly-Si BSF layer. By using directional doping methods, like ion implantation for the emitter formation, this effect can be circumvented. Resulting solar cells (fabricated in a project outside of this

work) reach much lower J_{02} values of $16\,\mathrm{nA/cm^2}$ and thus efficiencies of $22.0\,\%$ (Here the calibrated reference cells have been used for the illumination density calibration of the light source, resulting in more reliable J_{sc} values of $40.7\,\%$).

Chapter 7

Summary

In this thesis poly-Si layers for the application as carrier selective contacts for high efficiency *c*-Si solar cell applications have been developed and characterized. Additionally, counterdoping with ion implantation was investigated as an attractive process for the fabrication of back junction back contacted *c*-Si solar cells. Finally, the combination of these two technologies has been investigated.

The influence of the individual process steps of the poly-Si contact fabrication, such as the growth of the interfacial oxide, the thermal treatment and the doping process on the microscopic and macroscopic properties of the poly-Si contacts have been investigated. Based on these investigations a subsequent improvement of the junction quality was achieved, resulting in poly-Si contacts with a $J_{0,\mathrm{poly}}$ and ρ_{int} of $0.66\,\mathrm{fA/cm^2}$ / $\rho_{\mathrm{int}} = 500\,\mathrm{m\Omega\,cm^2}$ and $1.0\,\mathrm{fA/cm^2}$ / $80\,\mathrm{m\Omega\,cm^2}$ for *n*-type poly-Si contacts. For *p*-type poly-Si contacts $4.4\,\mathrm{fA/cm^2}$ without a contact resistance measurement and $5.0\,\mathrm{fA/cm^2}$ / $100\,\mathrm{m\Omega\,cm^2}$ have been obtained. These J_0 values are currently the lowest published values for poly-Si contacts.

In order to significantly reduce the time and effort for the fabrication of test structures to determine the contact resistance, a new method for the evaluation of the contact resistance on lifetime samples has been developed. For this method only sheet resistances obtained by inductively coupled measurements and sheet resistances obtained by four point probe measurement have to be performed. By comparing the results with 3D device simulations, also a quantitative statement of the contact resistance can be made. The contact resistances obtained with this method were in accordance with measurements obtained with contact resistance test structures.

Based on the analysis of the dependence of the passivation quality and the contact resistance on the process parameters, new indications on the nature of the main transport mechanism in poly-Si contacts have been found. The need for high temperature processes to obtain low contact resistances supports the assumption of the pinhole model, which assumes that the interface oxide has to break up to a certain amount to ensure a good contact between the poly-Si layer and the *c*-Si wafer. In the scope of the currently more accepted oxide tunneling model, this observation can hardly be explained. Further support for the pinhole model was given by 3D device simulations showing the comparability of experimentally obtained $J_{0,\mathrm{poly}}$ / ρ_{int} pairs with simulations of pinhole contacted wafers.

In order to simplify the fabrication process for BJBC solar cells, counterdoping with in-situ patterned ion implantation has been investigated. It has been shown that despite the touching highly doped *p*- and *n*-type regions no indications for trap assisted tunneling could be found after an annealing step. A comparison of the measured breakdown voltage with 2D device simulations indicated a laterally graded junction with a width of 4-5 μm. BJBC solar cells fabricated with this process reached efficiencies of 22.1 % on 156 mm × 156 mm large solar cells.

A process for the application of the counterdoping process on poly-Si contacts has been developed. The resulting $J_{0,\mathrm{poly}}$ and ρ_{int} values of 1.0 fA/cm^2 and 250 mΩ cm^2 for boron implanted layers, overcompensated with a full area phosphorus implantation, were comparable to the values of only phosphorus implanted poly-Si contacts.

Applying the process of patterned counterdoping on poly-Si junctions however, resulted in a detrimental degradation of the electrical characteristics. Investigations on the recombination characteristics of test structures have shown that this enhanced recombination is caused by the lateral *pn*-junction in the highly defective poly-Si layer. The magnitude of this parasitic recombination path was highly dependent on the doping density in the poly-Si layers. With the help of a simulation supported recombination model, it was tried to reduce the parasitic recombination by introducing specially designed diodes at the lateral *pn*-junction.

The parasitic recombination is considered to be the most important barrier for the application of the poly-Si contacts developed in this work in high efficiency BJBC solar cells. Therefore, further suggestions for the reduction were given.

By applying the poly-Si contacts as a back surface field in *n*-type BJBC solar cells, fabricated without counterdoping, efficiencies up to 21.7 % were reached. The open circuit voltage of the best cell was 673.6 mV and the corresponding series resistance had a value of 0.4 Ω cm^2. The successful application of poly-Si contacts on both polarities would enable to exploit the full V_{oc} potential of well above 710 mV.

Appendix A

Overview of the processed samples

Sample name	Oxid type	Oxide thickness [mn]	Annealing time [nm]	Annealing temperature [°C]	Doping source	τ_{eff} at Δn=10^{15}cm^{-3} [μs]	$V_{\text{oc,impl}}$ [mV]	$J_{0,\text{surf}}$ [fA/cm^2]	$R_{\text{sheet,poly}}$ [$\Omega/\square$]	ρ_{rel}
SH019d										
12	thermal	3.1	45	1050	$POCl_3$	1912	705	10	603	0.074
14	thermal	3.1	90	1050	$POCl_3$	924	682	37	2741.7	-0.0017
18	thermal	3.1	30	1050	$POCl_3$	1939	703	9	311.9	0.81
21	thermal	3.1	30	1050	$POCl_3$	2605	715	6	331.3	0.58
22	thermal	3.1	15	1050	$POCl_3$	4887	722	5	420.5	0.60
24	thermal	3.1	60	1050	$POCl_3$	2753	715	8	352.7	0.086
26	thermal	3.1	60	1050	$POCl_3$	1488	715	4	377.9	0.042
SH019e										
14	thermal	3.6	30	1050	$POCl_3$	1351	712	4	427.1	0.73
17	thermal	3.6	60	1050	$POCl_3$	2552	728	3	387	0.43
20	thermal	3.6	75	1050	$POCl_3$	4296	732	3	591.8	0.021
23	thermal	3.6	90	1050	$POCl_3$	6491	729	4	678.8	0.029

Table A.1.: List of the samples used in figures 4.2 and 4.3 in section 4.1, together with the varied process parameters and the measurement results; continuing in table A.2 on the next page.

Sample name	Oxid type	Oxide thickness [mn]	Annealing time [nm]	Annealing temperature [°C]	Doping source	τ_{eff} at Δn=10^{15}cm^{-3} [μs]	$V_{\text{oc,impl}}$ [mV]	$J_{0,\text{surf}}$ [fA/cm^2]	$R_{\text{sheet,poly}}$ [$\Omega/\square$]	ρ_{rel}
SH040										
17	thermal	3.6	30	1000	$POCl_3$	2173.2	705	17	221.8	0.98
18	thermal	3.6	30	1050	$POCl_3$	2546.5	716	6	216.4	1.03
19	thermal	3.6	30	1000	BBr_3	3084.2	701	19	145.3	1.06
20	thermal	3.6	30	1050	BBr_3	3100.3	706	15	140.2	1.00
21	thermal	3.1	30	900	$POCl_3$	5265.9	725	5	236.8	0.98
22	thermal	3.1	30	950	$POCl_3$	3040	710	13	240.6	0.97
23	thermal	3.1	30	1000	$POCl_3$	3799.5	718	8	229	0.94
24	thermal	3.1	30	1050	$POCl_3$	2469.2	719	5	217.4	0.96
25	thermal	3.1	30	1000	BBr_3	3598.1	703	17	138.4	1.02
26	thermal	3.1	30	1050	BBr_3	4181.6	710	13	135.2	0.98
27	thermal	2.4	30	900	$POCl_3$	4845.9	721	6	236.5	1.05
28	thermal	2.4	30	950	$POCl_3$	4404.5	721	7	245	0.96
29	*thermal*	*2.4*	*30*	*1000*	*$POCl_3$*	*broken*				
30	thermal	2.4	30	1050	$POCl_3$	5404.7	725	5	212.6	0.051
31	thermal	2.4	30	1000	$POCl_3$	4515.8	715	9	218.1	0.96
32	thermal	2.4	30	1050	BBr_3	3324.9	711	10	136	1.03
33	HCl	1.2	30	900	$POCl_3$	5571.2	720	7	230.4	0.063
34	HCl	1.2	30	950	$POCl_3$	3118	706	14	236.6	0.046
35	*HCl*	*1.2*	*30*	*1000*	*$POCl_3$*	*broken*				
36	HCl	1.2	30	1050	$POCl_3$	129.1	620	393	179.9	0.63
37	HNO3	1.2	30	900	$POCl_3$	1468.6	704	10	235.1	0.051
38	HNO3	1.2	30	950	$POCl_3$	2288.8	699	20	250.5	0.065
39	*HNO3*	*1.2*	*30*	*1000*	*$POCl_3$*	*broken*				
62	HNO3	1.2	30	1000	$POCl_3$	5595	721	5	243.9	0.062
41	HNO3	1.2	30	1050	$POCl_3$	109.6	615	508	188.9	0.90
42	HNO3	1.2	30	1000	BBr_3	305.3	644	177	117.8	0.90

Table A.2.: Continuation of table A.2 from previous page.

Sample name	Wafer material	Pre-implant-anneal	Implantation dose [mA/cm^2]	Post-implant anneal	τ_{eff} at Δn=10^{15}cm^{-3} [μs]	$V_{\text{oc,impl}}$ [mV]	$J_{0,\text{surf}}$ [fA/cm^2]	$R_{\text{sheet,poly}}$ [$\Omega/\square$]	ρ_{rel}
SH117									
1	n-Cz	30 min 1000°C	2.5e15 P	30 min 900°C	6160.6	739	1.01	299.7	0.065
2	n-Cz	30 min 1000°C	2.5e15 P	30 min 900°C	6647.4	738	1.65	300.2	0.071
3	n-Cz	30 min 1000°C	2.5e15 P	30 min 1000°C	19472.8	744	0.79	239.4	0.096
4	n-Cz	30 min 1000°C	2.5e15 P	30 min 1000°C	16038.1	741	1.36	247.4	0.085
5	n-Cz	-	2.5e15 P	30 min 1000°C	25320.0	744	0.66	202.0	0.11
6	n-Cz	-	2.5e15 P	30 min 1000°C	24539.0	741	0.97	206.6	0.10
7	n-Cz	30 min 1000°C	5e14 B	30 min 900°C	3439.0	719	7.05	607.9	
8	n-Cz	30 min 1000°C	5e14 B	30 min 900°C	2983.3	717	7.28	576.0	
9	n-Cz	30 min 1000°C	5e14 B	30 min 1000°C	4018.0	719	7.57	456.9	
10	n-Cz	30 min 1000°C	5e14 B	30 min 1000°C	4007.5	721	6.42	430.4	
11	n-Cz	-	5e14 B	30 min 1000°C	4303.7	721	6.77	400.5	
12	n-Cz	-	5e14 B	30 min 1000°C	4130.8	722	6.33	380.7	
13	p-FZ	30 min 1000°C	5e14 B	30 min 900°C	198.6	667	22.7	613.3	0.013
14	p-FZ	30 min 1000°C	5e14 B	30 min 900°C	908.9	714	6.08	590.6	0.0021
15	p-FZ	30 min 1000°C	5e14 B	30 min 1000°C	1407.8	714	4.99	424.1	0.00083
16	p-FZ	30 min 1000°C	5e14 B	30 min 1000°C	1458.8	719	6.04	405.9	0.00068
17	p-FZ	-	5e14 B	30 min 1000°C	1257.8	714	7.22	443.7	0.0028
18	p-FZ	-	5e14 B	30 min 1000°C	483.3	694	9.09	450.6	0.00027

Table A.3.: List of the samples used in figure 4.5 in section 4.2, together with the varied process parameters and the measurement results.

Sample name	Description material	Implantation dose [mA/cm^2]	Implantation dose [mA/cm^2]	τ_{eff} at Δn=10^{15}cm^{-3} [μs]	$V_{\text{oc,impl}}$ [mV]	$J_{0,\text{surf}}$ [fA/cm^2]	$R_{\text{sheet,poly}}$ [$\Omega/\square$]	ρ_{rel}
SH068								
6	Boron implantation	2e14 B		3635	720	7	854.2	
9	Boron implantation	5e14 B		4688	724	6	325.9	1.01
12	Boron implantation	1e15 B		5363	725	4.4	171.7	1.04
15	Boron implantation	2e15 B		4614	712	11	98.2	
18	Boron implantation	5e15 B		309.5	642	175	30.8	
21	Phosphorus implantation	2e14 P		2977	724	5	2232.4	0.46
24	Phosphorus implantation	5e14 P		2318	716	5	834.7	0.21
27	Phosphorus implantation	1e15 P		6218	736	1.9	405.8	0.027
30	Phosphorus implantation	2e15 P		8115	738	1.7	162.8	0.039
33	Phosphorus implantation	5e15 P		22167	742	1.0	76.58	0.073
38	Phosphorus implantation	7.5e15 P		8607	730	4.6	66.3	0.047
39	Counterdoping	5e14 B	1e15 P	1253	726	1.2	1596.9	0.85
40	Counterdoping	5e14 B	2e15 P	2881	741	0.45	399.8	1.04
41	Counterdoping	5e14 B	5e15 P	13436	745	1.0	98.7	0.091
42	Counterdoping	1e15 B	2e15 P	16651	732	1.0	925.5	0.92
43	Counterdoping	1e15 B	5e15 P	7152	742	0.90	138.4	0.067
44	Counterdoping	1e15 B	7.5e15 P	13702	739	2.5	94.6	0.070
45	Counterdoping	2e15 B	5e15 P	2412	739	0.40	223.0	0.95
46	*Counterdoping*	*2e15 B*	*7.5e15 P*	*broken*				
47	Masked counterdoping	1e15 B	2e15 P	998	707		198.3	
48	Masked counterdoping	1e15 B	5e15 P	366	684		216.4	
49	Masked counterdoping	2e15 B	5e15 P	271	664		118.8	
50	Masked counterdoping	2e15 B	7.5e15 P	69.9	603		119.9	

Table A.4.: List of the samples used in section 4.3 (samples 6-38) and in section 5.2 (samples 39-50), together with the varied process parameters and the measurement results.

Appendix B

Comparison between SIMS and ECV measurements

In section 4.3 secondary ion mass spectrometry (SIMS) measurement are shown together with ECV measurements. The SIMS measurements are conducted at the CiS Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH in Erfurt. The mass is determined by time of flight mass spectrometry and the depth by using the sputter rate determined on a *c*-Si reference sample and by assuming a homogeneous sputter rate in *c*-Si and poly-Si. For the measurements, O_2^+ ions with an energy of 15 keV have been used as primary ion for boron doped samples and Cs^+ ions with an energy of 10 keV for phosphorus doped samples. A comparison of the measurements is shown again in figure B.1 for one phosphorus and one

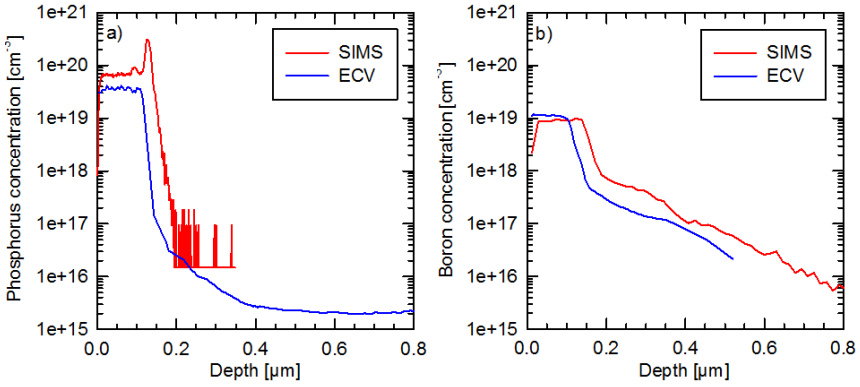

Figure B.1.: Comparison of SIMS and ECV measurements for poly-Si samples doped via ion-implantation (see section 4.3) implantation doses: a) $10^{15}\,\mathrm{cm}^{-2}$ P, b) $2 \times 10^{14}\,\mathrm{cm}^{-2}$ B.

boron doped sample. In general ECV measures the density of electrically active dopants, while SIMS measures the absolute density of atoms. Especially in the polycrystalline region it is plausible to assume that some of the dopant atoms are inactive because they are trapped at grain boundaries. Gosh *et al.* [150] estimate that at doping densities larger than $\sim 10^{12}\,\mathrm{cm}^{-2}/d$, where d is the grain size in the poly-Si layer, the trapping of dopants at grain boundaries becomes negligible. With a grain size of $\sim 100\,\mathrm{nm}$, as determined from SEM measurements, this would be the case for doping densities in the poly-Si regions of up to $10^{17}\,\mathrm{cm}^{-3}$ and therefore should not affect the ECV measurements. The difference in the measured signals can also be attributed to measurement uncertainties. For SIMS a uncertainty of 30 % has been given for the boron measurements. For the phosphorus measurements it is even higher, because the ^{31}P signal is overlayed by the signal of the ^{30}Si^{1}H molecule. Therefore the uncertainties of the SIMS measurements can very well explain the difference in the poly-Si region. Additional uncertainties from the ECV measurements are usually dominated by the measurement uncertainty during the determination of the etch area [151]. An error here will have a quadratic influence on the measured doping concentration (see equation 3.11). The low intensities in the first 10 nm at the surface and also the high signal at the poly-Si / *c*-Si interface for the SIMS measurement on the phosphorus doped sample, can be explained by SIMS artifacts that are typical at surfaces and interfaces. The difference in the depth profile may arise from the not very precise method for the depth determination used for the SIMS measurements, together with certain artifacts that complicate the SIMS measurement of steep doping gradients (knock on effects, influence from the border of the measurement area), or again from the uncertainty of the area determination for the ECV measurements.

Beside these effects, the SIMS profiles agree well with the measured ECV profiles. Nevertheless, for the special test structures with extremely steep dopant gradients, ECV seems to be less affected by measurement artifacts and the measurement uncertainty is assumed to be smaller than the one of SIMS. Therefore, only ECV is used for most of the samples in this work.

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List of abbreviations

4PP	four point probe
a-Si	amorphous silicon
a-Si:H	hydrogen rich amorphous silicon
AFM	atomic force microscopy
Al-BSF	Al doped back surface field
BBT	band to band tunneling
BJBC	back junction back contact
BJT	bipolar junction transistor
BSF	back surface field
c-AFM	conductive atomic force microscopy
c-Si	crystalline silicon
Cz	Czochralski grown silicon
dyn.-ILM	dynamic infrared lifetime imaging
ECV	electrochemical current voltage
FF	fill factor
FGA	forming gas anneal
FZ	float zone silicon
G	photogeneration
HET	heterojunction
HLI	high level injection
HRTEM	high resolution transmission electron microscopy
I	current
J	current density
J_0	saturation current density
J_{01}	saturation current density with ideality factor of 1

J_{02}	saturation current density with ideality factor of 2
$J_{0,\mathrm{poly}}$	saturation current density of the poly-Si layer
$J_{0,\mathrm{surf}}$	saturation current density of the surface region
J_{cell}	recombination current density of the solar cell
J_{gen}	light intensity
J_{meas}	measured recombination current density
J_{para}	parasitic recombination current density
J_{rec}	recombination current density
J_{sc}	short circuit current density
k	Boltzmans constant
L	diffusion length
LLI	low level injection
LPCVD	low pressure chemical vapor deposition
MPP	maximum power point
n	ideality factor
N_{dop}	doping density
n_{i}	intrinsic carrier density
p	pitch
PC-PLI	photoconductance-calibrated photoluminescence lifetime imaging
PCD	photoconductance decay
PECVD	plasma enhanced chemical vapor deposition
PERC	passivated emitter and rear cell
pFF	pseudo fill factor
pFF_{impl}	implied pseudo fill factor
PL	photoluminescence
poly-Si	polycrystalline silicon
PV	photovoltaic
r	radius
R_{4PP}	sheet resistance measured with the four point probe
R_{bulk}	sheet resistance of the wafer
R_{para}	parasitic resistance
R_{poly}	sheet resistance of the poly-Si layer
R_{total}	total sheet resistance of the test structure
RCA	cleaning sequence for silicon wafers
RIE	reactive ion etching
s_{cont}	surface recombination velocity at the contacts
s_{eff}	effective surface recombination velocity
s_{pass}	surface recombination velocity at the passivation layer

SCR	space charge region
SEM	scanning electron microscopy
SIMS	secondary ion mass spectrometry
SIPOS	semi-insulating polycrystalline silicon
SRH	Shockley Read Hall [recombination]
T	temperature
TAT	trap assisted tunneling
TEM	transmission electron microscopy
TLM	transfer length method
V	voltage
V_{oc}	open circuit voltage
$V_{\mathrm{oc,impl}}$	implied open circuit voltage
W	thickness of the wafer
Δn	excess carrier density
η	light conversion efficiency
η_{impl}	implied light conversion efficiency
μ_{n}	electron mobility
μ_{p}	hole mobility
ρ	resistivity
ρ_{c}	contact resistance
ρ_{int}	interface contact resistance
ρ_{rel}	relative contact resistance
σ	conductance
τ	charge carrier lifetime
τ_{Auger}	charge carrier lifetime implied by Auger and intrinsic recombination of the wafer
τ_{bulk}	charge carrier lifetime of the wafer
τ_{eff}	effective charge carrier lifetime
τ_{surf}	charge carrier lifetime implied by the surface recombination
$\tau_{\mathrm{SRH,bulk}}$	charge carrier lifetime implied by the Shockley Read Hall recombination of the wafer

List of publications

Refereed Journal Papers

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