Growth, structuring and interface manipulation of ultrathin oxide and silicate films on silicon single crystal surfaces

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M.Sc. Shariful Islam
geboren am 01. März 1982
in Comilla, Bangladesh

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Referent:	Prof. Dr. Herbert Pfnür
Koreferent:	Prof. Dr. Karl R. Hofmann
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Abstract

In search of an alternative gate oxide, the structural and electronic properties of mixed BaSr oxides/silicates and Barium silicate were investigated both spectroscopically and by electrical measurements in MOS-diode structures on Si(001). We studied the oxide and silicates elaborately both on structured and unstructured Si(001) surface after depositing both at room and at high temperature (650°C).

The dielectric-substrate interface plays a very important role on the growth condition and on the chemical, structural and kinetic properties of dielectric layers. Some very important properties like the sharpness of the interface, trap densities and band alignment also influenced by the cleanliness of substrate surface. We tried Piranha, HF, RCA-1 and RCA-2 in different ways to get clean silicon surface inside clean room which ensures better result of cleaning.

In order to specify the growth, stoichiometry, stability, band gap and band offset of these oxide and silicates we used X-ray Photoelectron Spectroscopy (XPS) and Electron Energy Loss Spectroscopy (EELS) respectively. Crystal structures were investigated by Spot Profile Analysis-Low Energy Electron Diffraction (SPA-LEED). To observe the crystalline growth, crystal orientation and thickness we used High Resolution Transmission Electron Microscopy (HRTEM) measurements. We performed electrical measurements (C-V and I-V) of the oxide and silicates as an alternate gate dielectric in a MOS diode to study the dielectric constant, hysteresis, capacitance equivalent thickness (CET), flat band voltage, leakage current and dielectric-substrate interface in detail.

Despite of all promising properties of Ba-Sr oxide as gate oxide in MOS diode, which discussed in this work and also in older work in our group, the limitations appear concerning thermal stability and hygroscopic. At high temperature, around 450°C, this oxide transformed into silicate. We investigated the crystalline silicates of both double metals $[(Ba_{0.8}Sr_{0.2})_2SiO_4]$ and single metal (Ba_2SiO_4). Barium silicate showed better results in comparison to Ba/Sr silicate, specially in case of leakage current. Barium silicate has high temperature stability upto desorption (~ 720°C), it has almost all the necessary properties as alternative gate dielectric, like, high dielectric constant ~ 20, very low hysteresis $< 0.5mV$, band offset $> 2eV$ and so on, discussed in this work. But the only limitation came from high interface trap densities (D_{it}) in comparison to Ba/Sr oxide.

Keywords

Gate dielectric, Dielectric constant, Stoichiometry, Leakage current, Hygroscopic, Crystalline, Flat band voltage, Hysteresis, Barium silicates (Ba_2SiO_4)

Zusammenfassung

In dieser Arbeit werden Barium-Silikate sowie gemischte BaSr-Oxide/Silikate hinsichtlich ihrer Eignung als alternative Gatoxide untersucht. Ihre strukturellen sowie elektronische Charakterisierung erfolgt durch spektroskopische sowie elektrische Messungen an entsprechenden MOS-Dioden auf Si(001). Oxid- und Silikatschichten werden sowohl bei Raum- als auch bei Hochtemperatur (650 °C) auf strukturierten und unstrukturierten Si(001) Oberflächen deponiert.

Für eine optimale Kontrolle der Wachstumsbedingungen und der chemischen, strukturellen und kinetischen Eigenschaften der dielektrischen Schichten, ist die Charakterisierung der Grenzfläche zum Substrat von besonderer Bedeutung. Da wichtige Eigenschaften der Grenzfläche, beispielsweise ihre räumliche Schärfe, die Störstellendichte sowie die Bandverbiegung von der Reinheit der Substratoberfläche abhängen, wurden verschiedene Verfahren (Piranha, HF, RCA-1, RCA-2) angewendet um möglichst optimale Reinigungsergebnisse zu erzielen.

Die Charakterisierung des Wachstums der Silikate und Oxide wird mit Hilfe von Röntgenphotoelektronenspektroskopie (XPS) sowie Elektronenenergieverlustspektroskopie (EELS) durchgeführt und so die Stöchiometrie, Bandlücke sowie Bandverbiegung bestimmt. Die Kristallstrukturen werden mit Hilfe niederenergetischer Elektronenbeugung (SPA-LEED) untersucht. Des Weiteren ermöglicht der Einsatz von hochauflösender Transmissionselektronenmikroskopie (HRTEM) die Beobachtung des Wachstums sowie die Bestimmung der Kristallorientierung und Schichtdicken. Die elektrische Charakterisierung der Silikat- und Oxidschichten erfolgt durch die Aufnahme von Kapazität-Spannungs- sowie Strom-Spannungs-Kennlinien. Hierdurch können Parameter der MOS-Dioden, wie beispielsweise die dielektrische Konstante, die Hysterese oder die gleichwertige Oxidschichtdicke (CET) bestimmt werden.

Trotz der vielversprechenden Eigenschaften, die BaSr-Oxide aufweisen, erschwert ihre limitierte thermische Stabilität sowie ihre Hygroskopie den Einsatz in MOS-Dioden. Bei hohen Temperaturen (etwa 450 °C) geht das Oxid in ein Silikat über. Daher werden die kristallinen Silikate $(Ba_{0.8}Sr_{0.2})_2SiO_4$ und Ba_2SiO_4 im Detail untersucht. Hierbei konnten signifikant bessere Ergebnisse mit den Barium-Silikaten erzielt werden. Neben geringen Leckströmen zeichnen sie sich unter anderem durch eine hohe Temperaturstabilität ($\sim$ 720 °C), eine hohe Dielektrizitätskonstante ($\sim$ 20) sowie geringe Hysteresen ($< 0.5\,\mathrm{mV}$) aus. Mit Ausnahme der relativ hohen Störstellendichten an der Si/Oxid-Grenzfläche im Vergleich zum Ba/Sr-Mischoxid besitzt das Bariumsilikat damit fast alle essentiellen Eigenschaften eines alternativen Gate-Dielektrikums.

Schlagwörter

Gatedielektrikum, Dielektrizitätskonstante, Stöchiometrie, Leckstrom, Hygroskopisch, Kristallin, Flachbandspannung, Hysterese, Barium-Silicate (Ba_2SiO_4)

Contents

1 Introduction

The further reduction of the minimum transistor dimensions in microelectronics which is based on silicon requires the solution of material problems apart from the further development of lithographic technique with high priority. In particular, it was essential to replace the SiO_2 that has been used over the years as a classical gate insulator by a material with substantially higher dielectric constant [1], [2]. The physics of the insulating thin film is related to many applications including microelectronics and this kind of investigation relates to a method of preparing highly insulating single crystal films in a molecular beam epitaxial growth chamber. For example, now a days a MOSFET with gate length below 50nm would need SiO_2 thickness less than 1nm to get necessary capacitance, at this thickness (1nm) SiO_2 has extremely high leakage current and leads to unacceptably high power dissipation [3], [4]. Therefore, in recent past world-wide (high k) gate-dielectric research of suitable alternative high ϵ_r was considerably intensified on middle to high value of dielectric materials to achieve the necessary gate capacities. With the help of larger insulator thicknesses the possibility of direct tunneling was suppressed.

Insulators with relative dielectric constants around 15 - 30, large band offsets >1eV, atomically sharp interface, low leakage currents, low insulator trap and interface trap densities are required for this kind of applications. In particular, the formation of SiO_2 at interface layers should be avoided, since it is a main source of reduction of the effective dielectric constant. Usually a single crystal substrate, Si(001) is provided to grow the desired thickness of thin dielectric films with an appropriate lattice match.

Whether the requirements of expected properties of high-k materials can be fulfilled is a matter of quite intriguing interface properties between the materials in direct contact. These are not only depend on the chemical stability of the components forming the interface, but also on activation barriers for chemical reactions, interface symmetries, lattice mismatch and starting conditions of growth.

Cleanliness of oxide-substrate interface plays a very important role on the growth condition of oxide and on the chemical, structural and thermodynamic properties of dielectric layers. Some very important properties like the sharpness of the interface, trap densities or band alignment also influenced by the cleanliness of the substrate surface.

Thin layers on silicon and other semiconductor surfaces have been extensively investigated in the past. Binary metal oxides were expected to be the most promising candidates, but ternary compounds such as titanates or aluminates are also interesting. The outcomes of the associated efforts are many and two of them are HfO_2 and ZrO_2 used by Intel as gate dielectrics with the help of metallic electrodes [5], [6] although it is far from ideal. High chemical reactivity and insufficient thermal stability are general problems. The materials which are used here are amorphous films, since it is believed that in this way it is possible to reduce the defect density at the interface to a bearable amount. The reduction of the effective equivalent oxide thickness is therefore inevitable (and/or the effective ϵ_r) [1] which is one of the several important parameters of the gate dielectrics. The currently

used materials as gate dielectrics are not yet ideal, although intensive optimization efforts regarding the electronic mobility [7] and other bulk and interface properties are lately under way. Therefore, also other compounds such as silicates are under investigation.

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2 Theoretical framework of spectroscopic characterization

In this chapter the theoretical foundations will be discussed, which are essential for the understanding of this work, measurement and evaluation methods.

The experiments took place in an ultrahigh vacuum (UHV) system at a base pressure of 1×10^{-10} mbar after bakeout. The system was equipped with different high resolution instruments like X-ray Photoelectron Spectroscopy (XPS), Spot Profile Analysis Low Energy Electron Diffraction (SPA-LEED), Ultraviolet Photoelectron Spectroscopy (UPS) and Electron Energy Loss Spectroscopy (EELS). Five separate metal crucibles were used with electron beam heater for evaporation of metals. A retractable Quartz Crystal Microbalance (QCM) was used to measure the mass flux at the position of the sample and to perform the oxidation experiment. For oxidation molecular oxygen (99.998% purity) was introduced by back filling the chamber avoiding any direct gas flow from the gas inlet to the sample. Pressure was measured using a well degassed extractor gauge. All these arrangements ensured the clean in-situ sample preparation and characterization of the sample in an atmosphere having contamination below the detection limit of our spectroscopic instruments.

2.1 X-ray Photoelectron Spectroscopy (XPS)

XPS is a very essential tool to characterize the chemical properties of the sample surfaces. Therefore, in our UHV system an XPS is installed. The XPS spectrum is the representation of binding energy and their corresponding intensities, means the total number of detected electrons of different elements present in the sample. It consists of an X-ray gun and a hemispherical energy analyzer . The x- ray gun can produce doublet X-ray radiation either with an MgK_α (1486.6 eV) or AlK_α (1253.6 eV) anode. The photons penetrate into the solid body and excite occupied electrons from their energy level, thus the excited electrons overcome their binding energy in the solid and eject out from the surface. As the binding energy of each electronic level is different, so the energy needed to release electron from various solid surface is also different. That's why intensity peaks of distinct elements usually appear at different positions in the XPS spectrum, which directly specify the elements present in the top most layers of the sample surface. Although the penetration depth of the photons goes far into the volume, the XPS is a surface sensitive analysis method, since the mean free path of the released electrons is very low ($<$1nm). Thus XPS essentially reflects the binding energy and chemical properties of the top 10 - 15ML. Core electrons ejected due to X-ray photons from the solid are accelerated and passed through a hemispherical energy analyzer, separated and detected by a channeltron successively. The number of electrons detected by the XPS analyzer is proportional to the sample cross section, exposed elements of sample by x-ray and sample orientation; each of the elements provides a characteristics peak in the output signal. The type or the shape of the characteristic XPS peaks is usually determined by the configuration of electrons, for example electrons ejected from different orbital configurations like 1s, 2s, 2p, 3s, etc. within the atoms of the sample [8].

Usually a preamplifier converts the channeltron current signal into a Transistor-transistor logic signal which is counted via an electronic counter. The energy separation is done by an electric field in the hemispherical analyzer, which allows only electrons of a given kinetic energy to enter the detector. It is possible to measure the atomic proportion of different elements in a particular sample from their peak ratio. In this case one has to divide the peak intensity by the "relative sensitivity factor" (RSF), and has to normalize with known densities of detected elements. The change of binding energy of a certain element with various composition in different sample can be identified from the XPS peak shift. It is possible to know the relative ratio of a known element in different sample with distinct binding energy. XPS is used in this work to investigate the band offsets at the interfaces of Ba-silicate and other oxides with the silicon substrate in combination with EELS [9].

The initial x-ray photon energy $E_{\hbar\nu}$, which is impinging on the sample surface, is usually transferred to an electron. To escape from the solid surface, an electron has to overcome the binding energy and the surface potential. Part of the incident energy is used to overcome the binding energy of the electron in the atom, E_{BE} and part of the energy to overcome the surface work function Φ_S. If no further energy is lost through scattering or other excitation processes, then rest of the energy will be used to give the electron a kinetic energy to move out of the surface. According to the principle of energy conservation the kinetic energy E_K of the electron after emerging from the solid surface satisfies the following energy conservation equation:

$$E_K = E_{\hbar\nu} - E_{BE} - \Phi_S \tag{2.1}$$

By applying a variable electrostatic field in front of the analyzer, scanning of different energies can be done. The kinetic energy is measured by the hemispherical energy analyzer with a constant pass energy and the count pulses are transferred to the computer simultaneously. By rearranging Eq. 2.1, it is possible to determine the binding energy directly from the known values of Φ_S, incident photon energy $E_{\hbar\nu}$ and from the measured value of kinetic energy E_K of the electron:

$$E_{BE} = E_{\hbar\nu} - E_K - \Phi_S \tag{2.2}$$

Once we get the binding energy, one can cross check the obtained binding energy and their corresponding material from different publications in a variety of chemical environments, which can be found on the internet as a collection [8]. Besides this one can get the idea of binding energy for a certain spectra from different database of surface spectroscopes in a tabular form, as [10]. Furthermore in XPS handbook one can find the chemical shifts of peaks in various chemical environments and bound with typical reactants such as C, O, or N depending on the kind of atoms under consideration.

2.1.1 Multiple splitting of core levels (shake up)

Final state configurations of an atom may change due to the removal of a core electron by the x-ray photon. Due to this reason we get individual spectrum with different binding energies in different lines. More precisely, due to electron spin orbit coupling of photoionized atom, multiple splitting can occur [11]. The spin can be oriented up or down, if the core electrons belong to an orbital with angular momentum quantum number $l > 0$ (i.e. except s-electrons) a doublet occurs due to the spin-orbit coupling between the spin and the orbital angular momentum. The total angular momentum results. It is a vector with quantum number $j = l \pm s$, depending on the parallel or anti-parallel position of electrons (for spin 1/2). For example the two non-degenerate states are $j_+ = l+1/2$ and $j_- = l-1/2$ and a doublet due to spin-orbit splitting is observed in the photoelectron spectrum. As an example, it leads to splitting of the p-orbital to $p_{1/2}$ and $p_{3/2}$ or the d-orbital to $d_{3/2}$ and $d_{5/2}$. The magnitude of this splitting depends crucially on the spin-orbit coupling constant ξ_{nl} which again depends on the expected value $\langle 1/r^3 \rangle$ of the respective orbital.

The energy difference $\triangle E_j$ between two split peaks can be several eV and grows for fixed n and l with the atomic number Z. The energy separation between the fixed n increases, due to the decrease of l values. The relative intensities of the split peaks are given by their degeneracy $(2j + 1)$. This leads, for example, between $d_{3/2}$ and $d_{5/2}$ to a ratio of 2:3. Usually, from a particular sub-shell in the photoemission spectrum that peak of the core level electron with the larger j is founded at lower binding energy. Clearly, for s core levels no spin-orbit splitting occurs in the photoemission.

2.1.2 Excitation process of core level photoelectrons

The one particle approximation can be used to describe the excitation process. Like shake up process, many body processes such as electron-electron, electron-phonon and electron-plasmon interactions lead to the generation of secondary electrons, which can be seen clearly in the photoelectron spectrum as a background signal. The interaction with electromagnetic radiation can be described by the Hamiltonian $\mathbf{H}$ and the perturbation $\mathbf{H}'$ which leads to dipole approximation. The Hamilton operator $\mathbf{H}_0$ of the unperturbed system has $\mathbf{p} = -i\hbar\bigtriangledown$ as momentum operator and $V(\vec{r})$ as crystal potential which has the following appearance:

$$\mathbf{H} = \frac{1}{2m_e}(\mathbf{p} + \frac{e}{c}\mathbf{A})^2 + e\Phi + V(\vec{r})$$

where

$$\mathbf{H}_0 = \frac{\mathbf{p}^2}{2m_e} + V(\vec{r}) \tag{2.3}$$

Here Φ is the work function. Transition to a disturbed system by electromagnetic radiation will be described with the transformation $\mathbf{p} \mapsto \mathbf{p} - e\vec{A}$ ($\vec{A}$: vector potential, e: electron charge). If the terms of order $\mathcal{O}$ $(\vec{A}^2)$ are neglected, the Hamilton operator Eq.

2.3 after the transformation looks like:

$$\begin{aligned}\mathbf{H} &= \mathbf{H}_0 + \mathbf{H}' \\ &= \frac{\mathbf{p}^2}{2m_e} + V(\vec{r}) - \frac{e}{2m_e}(\mathbf{p}\vec{A} + \vec{A}\mathbf{p}) + e\Phi\end{aligned}$$

Generally $\mathbf{p}\vec{A} = i\hbar\bigtriangledown\vec{A} = 0$ (Coulomb calibration). Although the vector field $\vec{A}$ may vary spatially on the surface, such effects are small, when the frequency of the photons is much larger than the plasmon frequency of the solid body [12]. This situation is prevalent in X-ray photoemission spectroscopy.

By considering source free space, adopting appropriate gauge transformations and neglecting higher orders of $\vec{A}$ (i.e., the term $\vec{A}\cdot\vec{A}$, which represents two photon processes) and with the Coulomb calibration, the perturbation operator $\mathbf{H}$ has the following form:

$$\mathbf{H} = -\frac{e}{2m_e}\vec{A}\cdot\mathbf{p} \tag{2.4}$$

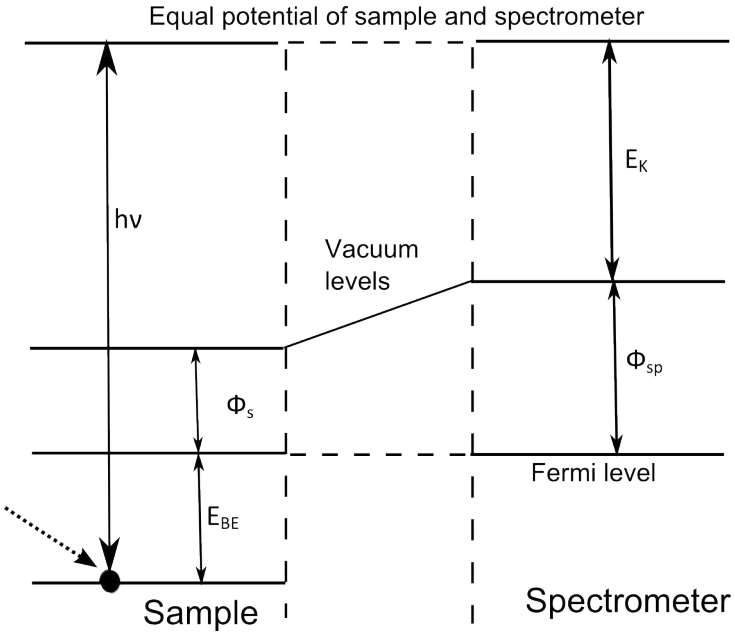


Figure 2.1 - Energy scheme for the photoemission process with contact potentials between a metallic sample and the analyzer.

An electromagnetic wave of the form $\vec{A}(\vec{r},t) = \vec{\epsilon}(\lambda)A_0\ e^{i(\vec{k}\vec{r}\pm\omega t)}$ is assumed in the case of incident X-rays ($\vec{\epsilon}(\lambda)$: Unit vector of the polarization direction). With the vector field $\vec{A}$, Eq. 2.4 changes in the general form,

$$\mathbf{H(t)} = \mathcal{H}e^{\pm i\omega t}, \qquad \mathcal{H} = -\frac{eA_0}{2m_e}\vec{\epsilon}(\lambda)e^{i\vec{k}\vec{r}}\mathbf{p} \tag{2.5}$$

where $\mathcal{H}$ corresponds to the time-independent component of the perturbation operator.

If the wavelength of the irradiated light is much greater than the atomic radius $\lambda = \frac{2\pi}{|\vec{k}|} \gg R = 10^{-10}m$, then the exponent of the plane wave in the entire area in which the electronic state wave function is very small $\vec{k}\vec{r} \leq |\vec{k}||\vec{r}| \leq \frac{2\pi R}{\lambda} \approx 2\pi 10^{-3}$ [13]. In this case, instead of the exponential function only the first term of the series expansion are used, the so-called *dipole approximation*:

$$e^{i\vec{k}\vec{r}} = 1 + i\vec{k}\vec{r} - (\vec{k}\vec{r})^2 + ...$$

With this approximation, the matrix element $\langle f|\mathcal{H}|i\rangle$ is apart from constant factors:

$$\langle f|\bigtriangledown|i\rangle = \frac{i}{\hbar}\langle f|\mathbf{p}|i\rangle \tag{2.6}$$

In X-ray photoemission spectroscopy, the assumptions made above are valid and the error under these circumstances is $\sim 2\%$ [14] at most.

Assuming a small perturbation $\mathcal{H}$, the time-dependent perturbation theory results in a first approximation, the *transition rate* $P_{i\to f}, f \neq i$ (transition probability per unit time) by *Fermi's golden rule* for the excitation from $|\Psi_i\rangle$ to $\langle\Psi_f|$ which stands for the initial and the final states with the corresponding energy levels E_i and E_f:

$$P_{i\to f} = \frac{2\pi}{\hbar}|\langle\Psi_f|\mathcal{H}|\Psi_i\rangle|^2\delta(E_f - E_i \pm E_{\hbar\omega}) \tag{2.7}$$

The δ-function in Eq. 2.7 obviously expresses a form of energy conservation law. Thus for example, induced absorption and emission of an atom is only possible when the irradiated light has exactly the frequency which corresponds to the energy difference of the final and the initial state. Therefore, ultraviolet light is required (UPS), for the excitation of the electrons in the valence bands. Due to the high binding energies of the inner shells, the excitation of those electrons can be done by X-rays (XPS). By taking into account the work function Φ (energetic distance between the Fermi level E_F and the vacuum level E_{Vac}) the δ-function in Eq. 2.7, can be written as follows:

$$E_{\hbar\omega} = E_f - E_i = E_{kin} + E_{BE} + \Phi \tag{2.8}$$

Here, E_{BE} is the binding energy relative to E_F and E_{kin} is the kinetic energy of the photoelectron outside of the solid. However, experimentally measured kinetic energy is not E_{kin}, rather the modified kinetic energy is E_{kin}. The reason here is that the kinetic energy is measured by a spectrometer, which has a work function Φ_{Spek}. So instead of Eq. 2.8 the kinetic energy is then

$$\begin{aligned} E_{\hbar\omega} &= E_f - E_i \\ &= E_{kin} + E_{BE} + \Phi_{Spek} \end{aligned} \tag{2.9}$$

which is described in [10, 15], at figure-2.1, it is also clearly visible.

2.1.3 Surface sensitivity and chemical bonds

X-rays which interact with matter weakly can penetrate deeply into a solid (1000 nm or more at $\hbar\omega \sim 1$ keV), again the excited electrons with energy in the range of 5-1500 eV can gradually lose their energy by inelastic scattering inside the material. In XPS experiments we are interested in those photoelectrons, which do not suffer from any energy losses. The probability of an electron to travel a certain distance z without losing any energy in the solid can be written as an exponential decay [16]:

$$P(z) \propto e^{-\frac{z}{\lambda_e}} \Longrightarrow < z >= \int zP(z)dz = \lambda_e$$

Electrons which experience energy losses and also able to escape from the surface into the vacuum, will contribute to the background signal, not to the main photoemission line. If we consider those electrons that are emitted perpendicular to the direction of the solid surface, then for a small element of thickness dz, at a distance z from the surface (surface plane, at z = 0) the measured intensity dI is:

$$dI \propto e^{-\frac{z}{\lambda_e}} dz$$

By integrating the above equation from 0 to t, the total intensity I underneath the surface of a thin film of thickness t can be expressed as:

$$I = I_0[1 - e^{-t/\lambda_e}]$$

It is often considered that the 95% of the photoemission intensity of the core level line comes from the depth of $3\lambda_e$ from the upper surface of the sample.

One of the key tasks in the study with XPS is the classification of chemical compounds. In the solid state different kinds of atoms are bound to each other. This causes a potential change to the inner core electrons of the atomic species, which changes their binding energies. In order to interpret the chemical shifts, often the charge potential model is used:

$$E_i = E_i^0 + kq_i + k\sum_{i \neq j} \frac{q_i}{r_{ij}} \qquad [28] \qquad (2.10)$$

Here E_i is the binding energy of a given core level of the atom i, E_i^0 is a reference energy, q_i is the charge of the atom i and the sum adds the potential of all the surrounding atoms j at the position of the atom i.

With the approximate assumption that atoms have a spherical shape and the distribution of valence charges on the surface is uniform, the classical potential q_i/r_v at all points inside the sphere is the same. Here r_v is the average valence orbital radius. A change in the valence charge by $\triangle\, q_i$ thus leads to a change in the potential in the sphere by $\triangle\, q_i/r_v$. This results in a change of binding energies of all core levels. For larger r_v the same change $\triangle\, q_i$ would lead to a slight reduction of the binding energy. If the abbreviation, V_i used

for the summation part of the equation 2.10, the shift of the binding energy of a given core level in two different environments can be written as follows:

$$E_i^{(1)} - E_i^{(2)} = k(q_i^{(1)} - q_i^{(2)}) + (V_i^{(1)} - V_i^{(2)}) \qquad [15] \qquad (2.11)$$

The first term makes it clear that the increase in binding energy is associated with the decrease in electron density of valence electrons of the atom i. Both equations 2.10 and 2.11 provide a simplified description of binding energy. The strongest simplification lies in neglecting the relaxation processes, such as the influences of the nuclear charge to the surrounding charges [15].

XPS spectrum can measure directly the chemical shifts. To see a shift of the entire peak, almost all the atoms of one type should bound together in the same way. If a certain fraction of atoms are embedded in a chemically different environment a splitting of the peak is seen. An example would be the Si2p-peak of the barium silicate film. As seen in Figure 2.2, this peak splits into two peaks. On one hand, the large peak at 99.2eV is attributed to pure silicon and the shoulder peak at 103.3eV indicates the bond of silicon with oxygen and barium to form Ba_2SiO_4.

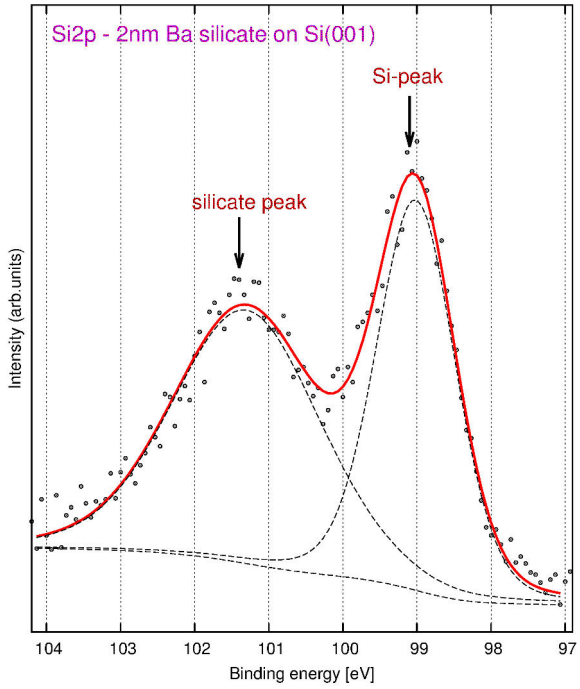


Figure 2.2 - Splitting of the Si2p peak due to the formation of silicate by annealing of BaO for 20min. up to 700°C.

The classification of such shifts is often not so easy. XPS databases can help here. But the rare bonds or the binding energies which are unknown, are difficult to find. In this case there is only one possibility to guess the shifts by knowledge of the on-surface materials and arrangements, but this can easily lead to misinterpretations. Theoretical calculations can further help to determine the expected energies of certain combinations.

2.1.4 Auger peaks

Instead of the photoelectrons, Auger electrons are also emitted due to relaxation of the energetic ions left after photoemission in the photoelectric process and appear in the XPS spectrum. The process of Auger electron emission occurs approximately 10^{-16} seconds after the x-ray photoelectric event. In Fig. 2.3 this process is illustrated schematically. An excited electron leaves an unoccupied level in a deep shell. When this state is occupied by an electron having higher energy, the energy difference between these two levels is transferred to an electron with lower binding energy without any further radiative emission. This electron is then ejected from the solid.

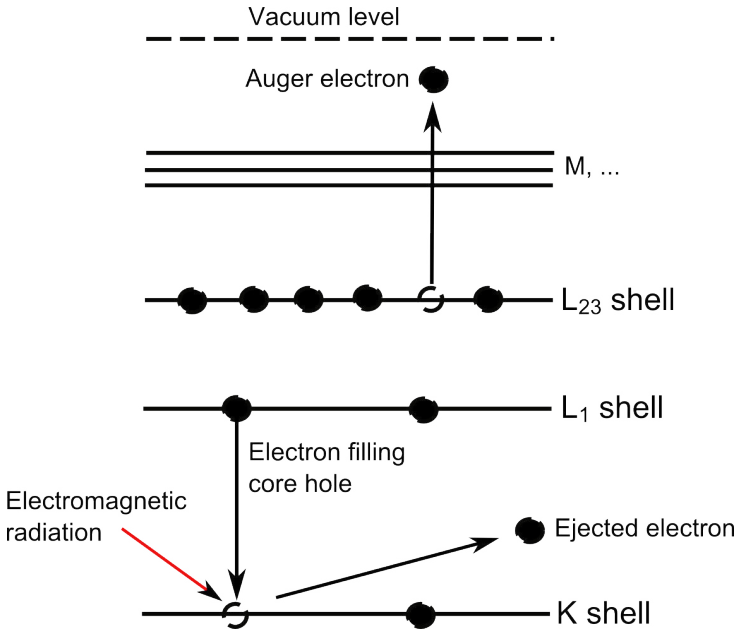


Figure 2.3 - Representation of the Auger process by a radiation less intra-atomic transition ([26]). First, an electron (here K shell) is ejected, another falls from a higher shell (here L_1) into this unoccupied state. Due to the energy released, an additional electron with lower binding energy is emitted from a higher shell (here $L_{2,3}$).

The name of the emitted electron results from the chemical names of the levels involved. In the example of Fig. 2.3 the levels of K, L_1 and $L_{2,3}$ are involved. It follows the name $KL_1L_{2,3}$ for the emitted Auger electron and its energy results from the difference of the binding energies. In this case, it initially receives the energy E_K - E_{L_1}. Beside that it also needs to overcome the energy $E^*_{L_{2,3}}$ in order to be released from the solid. The asterisk represents a slightly shifted energy in the presence of a hole in the state L_1. This gives a kinetic energy of $E_{KL_1L_{2,3}}$ for the Auger electron:

$$E_{KL_1L_{2,3}} = E_K - E_{L_1} - E^*_{L_{2,3}} - \Phi \qquad [15] \tag{2.12}$$

The energy $E^*_{L_{2,3}}$ is the energy after removal of the core electron from the atom, the equation is useful for many applications of Auger spectroscopy. A more general indication of the energy of an emitted Auger electron would be

$$E_{ABC} = E_A - E_B - E_C - E(BC:x) + R^{in}_x + R^{ex}_x \qquad [15] \tag{2.13}$$

where $E(BC:x)$ is the interaction energy between the holes in B and C in the atomic final state x, and R_x is the relaxation energy. Most of the Auger electrons do not have enough energy to appear in the spectrum. Important Auger peak series in the x-ray spectrum are the KLL, the LMM and the MNN series.

In contrast to the kinetic energy of photoelectrons Auger electrons are independent of the excitation energy of the X-ray photons. When changing the excitation energy from AlK_α to MgK_α the photoelectron peaks shift by $\Delta E_{h\nu} = E_{h\nu,Mg} - E_{h\nu,Al} = 233eV$ in the plot of intensity versus kinetic energy, whereas the Auger peaks do not shift and remain at their respective positions. If the spectrum is plotted against the binding energy, the behavior is exactly vice versa [15]. A huge number of electrons from the inelastic scattering processes, so-called secondary electrons also form the Augur peaks, which usually appear on a high background.

2.1.5 Other XPS peaks

X-ray emission spectrum represents not only the characteristic x-ray, but some minor x-ray peaks at higher photon energies. As a consequence, for each x-ray photoelectron k_α peak, there is a family of minor peaks at lower binding energies, which is having the intensity and spacing characteristics of x-ray anode material, known as x-ray satellite peak. In addition to $K\alpha_{1,2}$ line, Mg and Al targets produce weaker lines. They are formed by the less probable transitions. A list of major X-ray satellites with their shifts and the relative intensities of the $K\alpha$ β can be found in Table 2.1.

		$\alpha_{1,2}$	α_3	α_4	α_5	α_6	β
Mg	displacement, eV	0	8.4	10.2	17.5	20.0	48.5
	relative height	100	8.0	4.1	0.55	0.45	0.5
Al	displacement, eV	0	9.8	11.8	20.1	23.4	69.7
	relative height	100	6.4	3.2	0.4	0.3	0.55

Table 2.1 - X-ray satellite energies and intensities [8].

Sometimes x-radiation from a different element rather than the x-ray source anode material falls upon the sample,causing some small peaks corresponding to the most intense spectral peaks, but displaced by a characteristic energy interval known as x-ray ghost peaks, another group of satellite peaks. They arise for example in Mg X-ray sources and can come through the thin Al monochromatic window, the photons can be triggered by the secondary electrons from the source. This can cause the shift of ghost peaks by $233eV$ higher in kinetic energy compared to the $MgK\alpha_{1,2}$. Table 2.1 indicates where such peaks are most likely to occur. Since the presence of ghost lines are rare, they should not be considered in sample characterization until all other possibilities are excluded.

It is possible that in some photoelectric process an ion will be left in an excited state, a few electron volts above the ground state rather than in the ground state. Kinetic energy

of the photoelectron is reduced in this process, which corresponds to the energy difference between the ground state and the excited state. As a consequence a satellite peak forms at a few electron volts lower in kinetic energy than the original characteristic peak, which is known as shake-up line. The valence electrons arrange themselves differently, which leads to an excitation into a higher unfilled state ("shakeup"). The necessary energy is provided by the photo-electron and that leads to a peak at lower kinetic energy. The occurring intensities can be up to 100% of the main peak at a particular system. Shake-off process is similar to the shake-up, here also first valence electrons will be ionized completely. In this case an ion is left behind, which leaves a vacancy both in the core and in valence state. These lead to the shake-off peaks which, however, are hardly noticed because they have a larger energy shift than the shake-up peaks and usually disappear in a broad inelastic tail [15].

2.1.6 Quantitative analysis

Using XPS it is possible to determine the relative concentrations of various elements in the sample. To quantify the amount of elements from the XPS measurements, the peak area sensitivity factors and peak height sensitivity factors have been developed. To analyze the volume of a homogeneous sample, the number of photo electrons per second in a certain spectral peak is given by:

$$I = nf\sigma\theta y\lambda AT \qquad [Assumption : homogeneous\ \ sample(see\ \ 2.1.3)]$$

where n is the number of atoms of the element per cm^3 of sample, f is the x-ray flux in the $photons/cm^2.sec$, σ is the photoelectric cross section for the atomic orbital in cm^2, θ is an angular efficiency factor, y is the efficiency in the photoelectric process , λ is the mean free path of the photo electrons in the sample, A is the area of the sample and T is the detection efficiency for the electrons emitted from the sample [17]. From the above equation:

$$n = \frac{I}{f\sigma\theta y\lambda AT} \qquad [17] \tag{2.14a}$$

The denominator in equation 2.14a can be represented by the symbol S, known as the atomic sensitivity factor. Considering a main peak from each of two elements, one can write:

$$\frac{n_1}{n_2} = \frac{I_1/S_1}{I_2/S_2} \qquad [17] \tag{2.14b}$$

Initially we can fit each of the peaks of different species with a fitting program, the integral intensity of the peaks can be found from the fit data directly and hence the ratio of an element into different sample using the sensitivity factor. A generalized expression for determination of the atom fraction of any constituent in a sample, C_x, can be written

as an extension of the equation 2.14b:

$$C_x = \frac{n_x}{\sum_i n_i} = \frac{I_x/S_x}{\sum_i I_i/S_i} \qquad [17]$$

Only for the homogeneous distributions of atoms.

2.2 Electron Energy Loss Spectroscopy (EELS)

An analytical method of sample measurement is electron energy loss spectroscopy (EELS), which measures the change of kinetic energy of electrons after they have interacted and deflected back from the sample surface. That means a beam of electrons is transmitted through or reflected from a crystal surface, here the change in energy and the direction of electrons are measured. There are two different types of electrons elastic and inelastic, both types of electrons can be scattered back from the sample surface and the amount of energy loss can be measured via an electron spectrometer and interpreted in terms of what caused the energy loss [18]. The inelastically scattered electrons have a smaller energy than the elastic ones, because they have given some of their energy to excitation. Some examples of inelastic interactions are phonon excitations, plasmon excitations, inter and intra-band transitions, Cerenkov radiation and inner shell ionization.

During EELS measurement the sample is bombarded by the electrons of fixed energy which lies within a narrow range of kinetic energies. The interaction between the electron beam and the electrons in the sample is due to the Coulomb potential. If the primary energy of electron is lower than the work function of the surface, the interacting electrons will not have sufficient energy to be released from the solid surface. Thus, the possible excitations are similar to those in light-scattering spectroscopy or optical absorption. Since EELS is based on an inelastic scattering process, all relationships concerning conservation of energy and momentum are valid [14]. One can investigate the vibrational modes on the surfaces in vacuum and also can probe phonons in the entire Brillouin zone. The energy resolution of present-day spectrometers is as high as 1meV. Furthermore, by varying the electron energy, different scattering mechanisms can be employed, leading to different selection rules for the inelastic scattering [19].

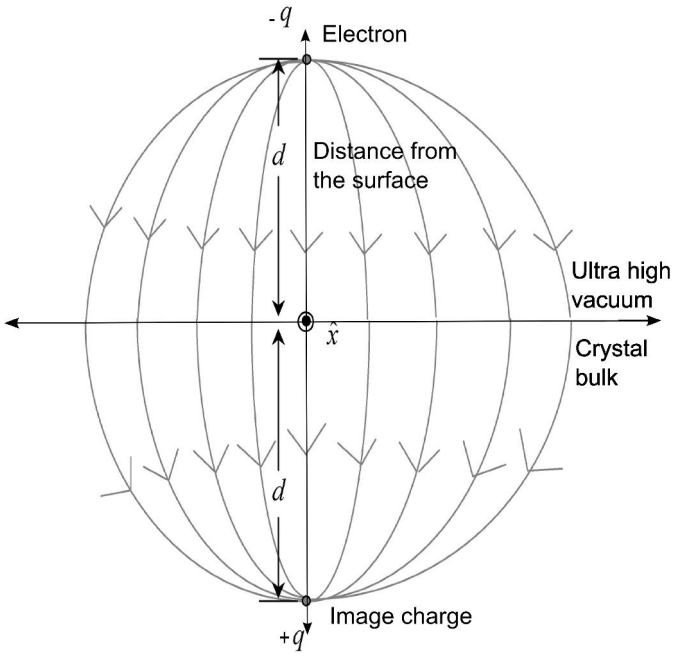


Figure 2.4 - Surface excitation by image charge effects during scattering of an electron [20]. The mirror charge inside the solid body moves as the incident electron.

Initial states are occupied as core-level, valence band or surface state and the final states are unoccupied as the conduction band or as a surface state. It is possible to occupy the unoccupied states and to determine the energy difference by EELS. The energy loss of primary electrons depends on the state they stimulate. The distance between the elastic peak and the loss peak directly gives the excitation energy of the state.

The processes of the scattering of electrons at the surface can best be described by the classical dielectric theory [50]. Far away from the surface, the field of an incoming and scattered electron can be considered as a point charge but near the surface the situation changes. Due to the polarization of the crystal, it produces an image charge of opposite sign. This applies strictly only for ideal flat metal surfaces. This description is valid and also a good approximation for the insulators and semiconductors with large ϵ_r. The resultant field strength is oriented perpendicular to the surface and has an extension, which approximately corresponds to the distance of the electron.

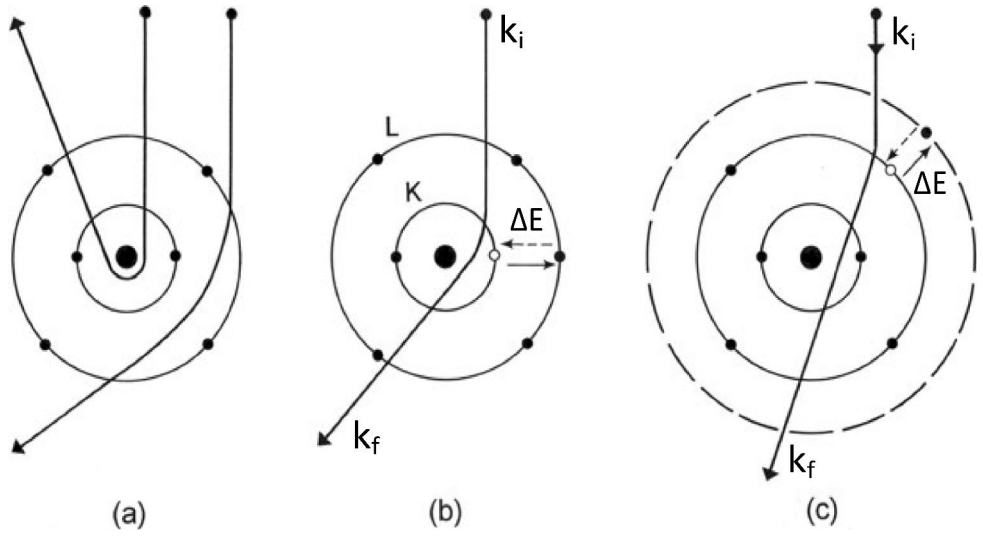


Figure 2.5 - A classical (particle) view of electron scattering by a single atom (carbon). (a) Elastic scattering is caused due to the Coulomb attraction of the nucleus. Inelastic scattering results from Coulomb repulsion by (b) inner-, or (c) outer-shell electrons, which are excited to a higher energy state. The reverse transitions (de-excitation) are shown by broken arrows and energy loss by **ΔE** [21].

Screening and general response to an electric field from outside: $\varepsilon(\omega, k_{\|}, k_{\perp})$. The dipole moments perpendicular to the surface can only be induced by this orientation in continuum limit i.e. $\lambda \gg a$. This leads to a small momentum transfer parallel to the surface $\Delta k_{\|} < 2\pi/d$. The inelastically scattered electron deviates a little at low energy and a minimum momentum change occurs for the direction change of diffracted electron. The characteristic scattering angle

$$\Theta_E = \frac{\Delta E}{2E_0} \qquad [20] \tag{2.15}$$

of the diffracted beam, where $\Delta E = \hbar\omega$ should be smaller than the primary energy E_0. There is a transfer of momentum $\hbar\Delta\mathbf{k} = \hbar(\mathbf{k_i} - \mathbf{k_f})$ and an energy loss ΔE, as shown in Fig.2.5. [20]

The dielectric function $\varepsilon(\omega, \mathbf{k}) = \varepsilon_1(\omega, \mathbf{k}) + i\varepsilon_2(\omega, \mathbf{k})$ is a function of $\mathbf{k}$ and q and characteristic of each solid. The dielectric theory of diffraction cross section is directly related to the dielectric response of the associated system. Within the bulk of a dielectric medium the amplitude of the field of an electron is screened by a factor of $1/\varepsilon$, the intensity by a factor $1/\varepsilon^2$. If the field moves through a medium then its damping will be proportional to ε_2 [22]. Thus for the energy loss one obtains

$$W_b(\mathbf{k}, \omega) \propto \frac{\varepsilon_2}{\mid \varepsilon \mid^2} = -Im\{\frac{1}{\varepsilon}\} = \frac{\varepsilon_2}{\varepsilon_1^2 + \varepsilon_2^2} \quad [22]$$

The energy loss by a moving electron on the surface having dipole interaction can be described by

$$W_b(\mathbf{k}, \omega) \sim \frac{\varepsilon_2}{\mid \varepsilon + 1 \mid^2} = -Im(\frac{1}{\varepsilon + 1}) = \frac{\varepsilon_2}{(\varepsilon_1 + 1)^2 + \varepsilon_2^2} \quad [22] \tag{2.16}$$

The function $-Im(\frac{1}{\varepsilon+1})$ is called surface loss function. It describes the fundamental structure of the loss spectra, since it has all the information about the dielectric behavior of the medium. [23]

2.3 Spot Profile Analysis - Low Energy Electron Diffraction (SPA-LEED)

Spot profile analysis low energy electron diffraction (SPA-LEED) is a very effective tool to observe and analyze the surface structures of crystalline sample. By measuring the intensity of diffracted beams one can determine the diffraction spot profiles of a sample using SPA-LEED technique. Electron diffraction spots are very sensitive to the morphology of the sample surface, hence by analyzing the diffracted spots it is possible to identify the sample surface condition. Using SPA-LEED it is possible to determine the surface roughness, surface steps or terrace sizes quantitatively [24]. The Spot Profile Analysis-LEED (SPA-LEED) was developed in the 70s and 80s by *M.Henzler* and was introduced at 1986 in [26] as an independent device.

The diffraction from surfaces may be described as sum of electron wave functions scattered from the initial wave vector $\mathbf{k}_i$ of the incoming electron to the final wave vector $\mathbf{k}_f$, by all the surface atoms at positions $\mathbf{r}(\mathbf{n})$

$$\Psi(\mathbf{K}, \mathbf{k}_i) = \sum_n f(\mathbf{n}, \mathbf{K}, \mathbf{k}_i) e^{i\mathbf{K}\mathbf{r}(\mathbf{n})} \tag{2.18}$$

where $\mathbf{K} = \mathbf{k}_i - \mathbf{k}_f$ is the scattering vector and $f(\mathbf{n}, \mathbf{K}, \mathbf{k}_i)$ is the structure factor which depends both on the initial electron wave vector $\mathbf{k}_i$ and final wave vector $\mathbf{k}_f$. The structure factor combines the electron wave coming from the surface atom at $\mathbf{r}(\mathbf{n})$ and all underlying atoms in the column perpendicular to the surface.

The LEED method is used to study the structure and morphology of surfaces. Electron energies of SPA-LEED can be between 5 to 500eV and the electron beam is focused on the detector but not on to the sample surface. This method uses the property that electrons are also having wave nature. According to *deBroglie* the wavelength of the electrons calculated in this case as $\lambda = h/p$, where $p = mv$ (h is Planck's constant, m is the electron mass, v is the velocity of the electron), later *Davisson* in [25] has proved the electron diffraction in matter. A more appropriate way of calculating the wavelength in Å is:

$$\lambda(\text{Å}) = \sqrt{150.4/E(eV)} \qquad [26] \tag{2.19}$$

Electrons can interfere like light or water waves due to this wave nature. By varying the emitted electron energy and also the incident angel, one can observe the entire reciprocal space of the sample surface using SPA-LEED. Here we see the convolution of differected electrons as an output image but not the interfere pattern. In classical LEED differected electrons interfere on a fluorescence screen and form a reciprocal image of the surface texture. A real space distance r corresponds to a distance proportional to 1/r in reciprocal space. In addition to the intensity of diffraction peaks, the profiles and the positions contain important information about the surface morphology.

The LEED spot of a rough surface is composed of a sharp central spike and a broadened

part depending on the scattering condition and the unit cell arrangement. The central spike includes all of the information on the layer distribution θ_h. θ_h is the coverage in the h^{th} layer. The normalized central spike intensity as a function of the total coverage θ is given by

$$G(S,\theta) = \sum_h \sum_l p_h p_{h-1} \cos 2\pi S l \tag{2.17}$$

P_h is the visible part of the layer h:

$$P_h = (\theta_{h+1} - \theta_h)$$

The phase S is the wavelength difference of electrons scattered from the neighboring terraces with one atomic step height d (K_z is the normal component of the scattering vector K):

$$S = \frac{dK_z}{2\pi}$$

This assumption valid for uniform material, where all atomic scattering factors are identical. Here long range phenomena considered but the multiple scattering phenomena is neglected.

Different SPA-LEED units

A SPA-LEED consists of four main parts: a fine focused electron gun, an entrance lens close to the sample, an electrostatic or magnetic deflection unit, and a small aperture in front of a single electron channeltron detector.

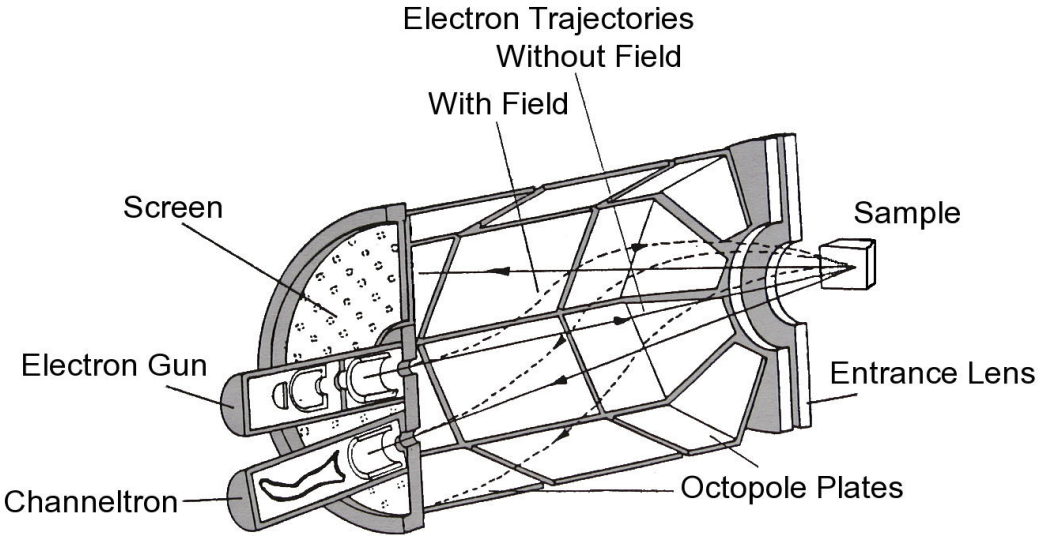


Figure 2.6 - The side view of a SPA-LEED with an electron gun, the channeltron detector, the conical octopole electrostatic deflection unit, the entrance lens and a sample in front of entrance lens [20].

In contrast to conventional LEED both the incidence and reflection angle of the electrons varied in SPA-LEED. This is done by the deflection voltage applied in x and y directions using the plates of the octopole via a resistor network. The octopole deflection unit of SPA-LEED consists of three rows of electrostatic deflection plates. Corresponding panels in the front and rear octopole have opposite polarity. This deflection plates bends the electron beam in an S-shaped fashion and change its incidence angle by keeping the position of incidence fixed on the sample surface. Since the detector is mounted right next to the electron gun, it means that the electrons undergo the same deflection path on the return trip. Diffraction image varies based on the incidence angle of the electrons.

2.3.1 Different surface configurations

An idealized interface should take the atomic arrangement of the volume. Energetically this is not always true. The atoms relax and reorganize over the base. If this is done in a periodic manner, this is called a superstructure. Their names result from the factors which describe, how many times the new periodicity has changed in the x-and y-direction relative to the earlier periodicity.

The form and nature of such a super-lattice structure is influenced by many effects. Defects play an important role. Point defects are known as zero dimensional defects that occur only at a single lattice point. A vacancy defect sometimes called a Schottky defect is usually a lattice site. When an ion moves into an interstitial site a vacancy is created, which often called a Frenkel defect. Linear defects are kind of dislocations around which some of the atoms of the crystal lattice are misaligned. There are two different kinds of dislocations, the edge dislocation and the screw dislocation.

In many cases, step edges on the surface can be domain boundaries. Adatoms and defects lead to disorder or even at higher concentrations to the destruction or rearrangement of the periodic superstructure. Facets are compared to the average surface inclined portions that result in additional diffraction effects. In the following the detection of certain surfaces arrangements and defects are discussed and some examples are shown.

2.3.2 Diffraction conditions and Ewald sphere formation

The diffraction phenomena with the diffraction spot intensity are mainly determined by the scattering cross section, i.e. the values of the structure factor, $f(\mathbf{n}, \mathbf{K}, \mathbf{k_i})$ as:

$$I(\mathbf{K}, \mathbf{k}_i) = \mid \Psi(\mathbf{K}, \mathbf{k}_i) \mid^2 \tag{2.20}$$

$$= \sum_{n,m} f(\mathbf{n}, \mathbf{K}, \mathbf{k}_i) f^*(\mathbf{m}, \mathbf{K}, \mathbf{k}_i) e^{i\mathbf{K}(\mathbf{r(n)}-\mathbf{r(m)})} \quad [26] \tag{2.21}$$

Where $\mathbf{K} = \mathbf{k}_i - \mathbf{k}_f$ is the diffraction vector and $f(\mathbf{n}, \mathbf{K}, \mathbf{k}_i)$ is the structure factor, through which the scattering behavior of the atoms are described.

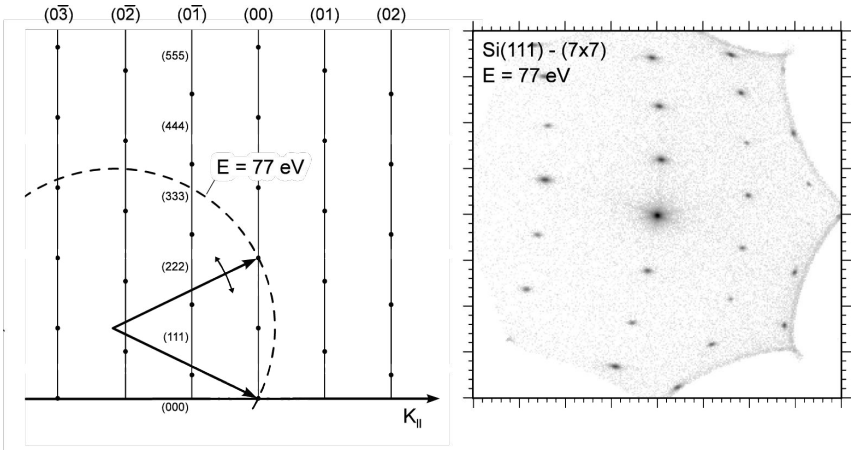


Figure 2.7 - Ewald construction at the reciprocal lattice rods [27]. Intersections of the Ewald sphere with the rods lead to LEED reflexes.

An extreme example is X-ray radiation with their low interaction and high penetration depth. This leads to well-defined 3D Bragg conditions which describe the periodicity of a single crystal. The selection rule for $\mathbf{K}_\perp$ leads to well-defined points in the reciprocal lattice representation with the dispersion in $\mathbf{K}_\perp$ direction. The other extreme example would be He atoms. They only encounter the surface and do not penetrate into the solid. So we are talking only about the first atomic layer and its structure factor. The lack of periodicity in the z-direction leads to a complete absence of selection rules for $\mathbf{K}_\perp$. This corresponds to surface lattice rods in the reciprocal lattice representation, as can be seen in Fig.2.7. The diffraction of electrons forms a situation similar to that of He atoms. They scatter elastically from the first few layers by electron-electron interaction. Influence of different periodicity perpendicular to the surface results in lattice rods, as almost any value of $\mathbf{K}_\perp$ is possible. In contrast to the He atoms, it is, however, major variations of the intensity along the grating rods and can go down to zero.

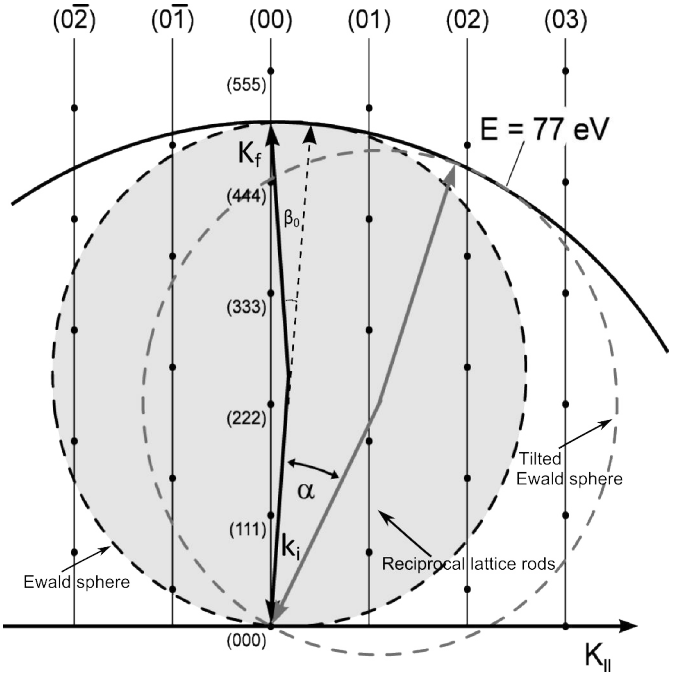


Figure 2.8 - Ewald construction by SPA-LEED: tilting of the Ewald sphere by angle change α between the incident beam and the sample and by fixed angle β_0 between the incident beam, $\mathbf{k}_i$ and the diffracted beam $\mathbf{k}_f$ [26]

Using these grid rods, the positions of the diffraction peaks can be derived with the so-called Ewald construction. For this purpose, a circle is drawn at the point (00) on the rod with the radius of the incident vector $\mathbf{k}_i$ in the reciprocal lattice representation. The incident vector is now the center of the circle in the corresponding angle of incidence of the electrons inserted from the surface to the circle in the image. In Fig.2.8 the electron beam falls vertically on the sample, which corresponds to the angle of most classical LEED apparatus. Constructive interference takes place at points where the circle intersects the bars, because the 2D Bragg condition is satisfied there. The diffraction vector $\mathbf{K}$ is now drawn from the tip of $\mathbf{k}_i$ to an intersection. The difference between the diffraction vector and the incident vector corresponds to the diffracted vector $\mathbf{k}_f$.

To perform electron diffraction, SPA-LEED needs three main components. First of all one needs a good source of electron, which can emit electrons of almost same energy at a time to perform a high-resolution electron diffraction where the signal to noise ratio is high. In the classical LEED there is a fixed luminescent screen. The entire screen is available to accommodate the differected electrons, which can be photographed or recorded by a video camera. In case of SPA-LEED, there is no screen. Here during scanning the angle of incidence Θ of the electrons changes, the incoming number of electrons measured by a channeltron which have a fixed angle β_0 to the incident beam and it is in a fixed location at the vicinity of the electron gun. If the angle Θ between $\mathbf{k}_i$ and the surface is changed by α, this results in tilting of the entire Ewald sphere by the angle α, as shown in Fig.2.8. Thus, the reciprocal space is scanned in one direction with appropriate Θ. A part of the reciprocal space can thus be scanned by changing the incident angle Θ and a fixed angle between the incident and emergent beam β_0. Due to the structure of the SPA-LEED the angle β_0 exactly corresponds to the angle between the electron gun and

channeltron(usually about 7°).

The used sample should be conductive, otherwise charging effect will appear, which might result in distorted image or no image case. Again the sample under investigation should have some long-range order, because amorphous samples are not suitable for SPA-LEED investigation. The mean free path, the energy difference (ΔE), change of angle ($\Delta\theta$), beam size of the electrons should be adjusted properly to travel from the source to the detector via the sample.

2.3.3 Diffraction from rough surfaces

The effects of regular surface defects in the LEED image will be discussed in this section, because the diffraction at a rough surface is not same as the diffraction at smooth or defect free surface, hence some deviations in structure factor values are expected. If the surface is not perfectly plane, but it consists of several terraces separated by steps, the diffracted electron waves of different phase will superimpose. Two electron waves refracted respectively from two planes separated by a distance d are superimposed at $K_{\parallel} = 0$, i.e. at (00) spot in the LEED image and a constructive interference will occur when the Bragg condition for electron energy

$$S = 2d\cos\vartheta\sqrt{E(eV)/150.4} \tag{2.22a}$$

or electron wavelength

$$S = 2d\cos\vartheta/\lambda_{electron} = n \tag{2.22b}$$

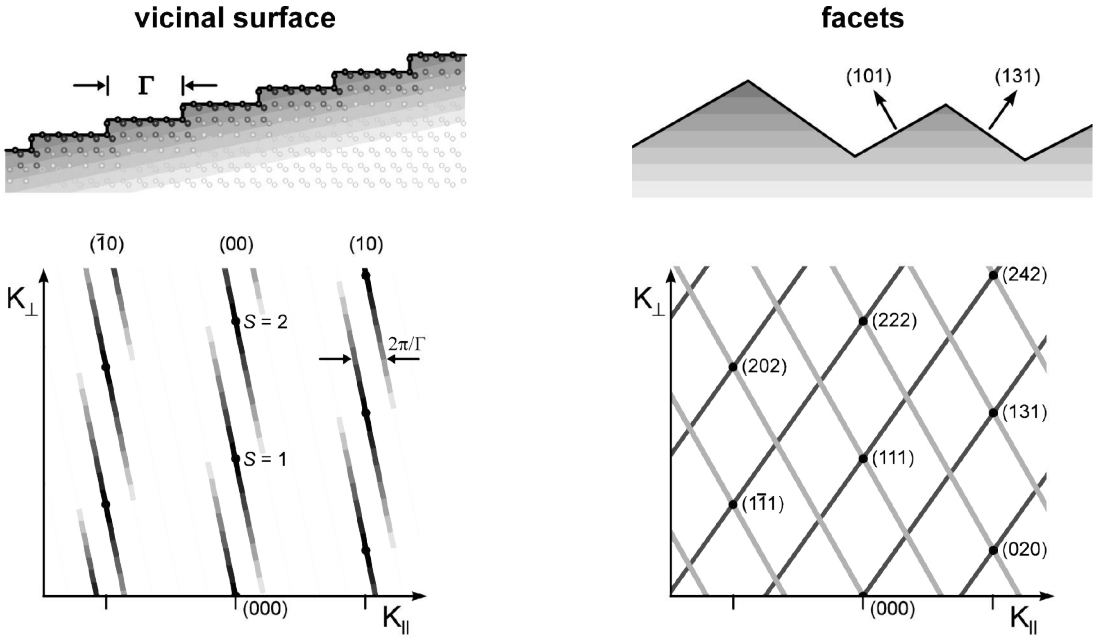
satisfies. In this case, $S = K_{\perp}d/2\pi$ is the dispersion phase, for constructive interference this should be a dimensionless integer (n) value. This is the so-called "in-phase" condition. For the "out-of-phase" condition, the electrons interfere destructively. This leads to the extinction of the (00)-spot and a diffuse background besides the sharp spot. The shape and the profile of such a spot is described by the lattice factor $G(\mathbf{K})$. It is composed of the intensity of the measured peaks I_{ij}, normalized by the integral intensity of the total spots including the diffuse background:

$$G(\mathbf{K}) = \frac{I_{ij}(\mathbf{K})}{\int d\mathbf{K}_{\parallel I_{ij}(\mathbf{K}_{\parallel})}} \qquad [26] \tag{2.23}$$

If the Bragg condition fulfills then G($\mathbf{K}$)=1, in the "out-of-phase" condition G($\mathbf{K}$)=0.

With the help of lattice factor it is possible to give a statement about the roughness of a surface. This grating factor is plotted against the energy of the incident electrons or against the scattering phase S, a so called $G(S)$ plot. In an ideal system, Gaussian like curves arise with maxima for $S = n$ and minima for $S = n + 1/2$ where 'n' is an integer number. The half width of the curve gives the so called RMS roughness vertical to the surface. Various factors make the curves for other systems not so ideal. For example, varying form factors or various types of disorder make the evaluation significantly more

complicated and difficult. Details on the evaluation of $G(S)$, roughness of difficult systems can be found in [33] and will not be further discussed here.



(a) Diffraction pattern from a vicinal surface with a regular step train. All LEED spots show a spot splitting due to the linear phase grid of steps. The spots move in accordance to the inclination of the vicinal surface.

(b) Diffraction pattern from a surface with low index facets. Each facet contributes with a complete set of diffraction rods to the pattern. All spots move with electron energy with respect to the macroscopic surface of the sample.

Figure 2.9 - Reciprocal Space Mapping on structures with different periodic defects.

The LEED image also identifies clearly regular steps on the surfaces. If, for example, a Si (001) is cut at a small angle off the [001] direction, this leads to a regular array of steps, which represent an additional periodic super-lattice having an average width Γ. The periodicity length is the terrace width Γ. This leads to the splitting of the spots to $\Delta k = 2\pi/Na_0 = 2\pi/\Gamma$ where N is an integer and a_0 is the lattice constant, as shown in fig.2.9a. Fig. 2.9b is an example of the energy dependent scans of facets present on the surface. From the width of the splitting of a spot in the LEED image, the average width of terraces can be calculated. Splitting of the spots called "reciprocal space mapping" depends on the applied energy, which are tilted Ewald rods and visible as

$$A(k) = \frac{\sin^2(\frac{N}{2}K_\perp a_0)}{\sin^2(\frac{1}{2}K_\perp a_0)} \qquad [26] \tag{2.24}$$

modulated in intensity. For $K_\perp = 2\pi/a_0$ these rods have their maximum, as can be seen from the equation 2.24. The tilting angle of the rods provide the information about the angle of the periodic superstructure to the actual structure. In case of a less inclined sample, the tilting angle can be read at the correct scale directly. In addition, the height of the steps can also be read by determining the scattering phase at the positions of the maxima. The scattering phase is given by $S = K_\perp d/2\pi$ and the maxima at $K_\perp = n.2\pi/a_0$. This yields $S = \frac{n.d}{a_0}$. Double steps would thus due to $d = 2a_0$ be fulfilled, as $S = 2.n$ would be twice as large.

Further opportunities of analysis and interpretation of LEED or SPA-LEED images will not be discussed here, in order not to exceed the scope of this work. Further details for interested readers are available in this reference [26].

3 Theoretical background of electrical characterization

We used current-voltage (I-V) and capacitance-voltage (C-V) measurements to characterize the electrical properties of our sample. To perform these measurements we applied a voltage between the gate and the substrate and measured the current flowing through the sample. During the measurement of the capacitance of our sample, we used a two element model, which is partially comparable to the MOS diode without any back contact resistance. Later the measured data was corrected using the three element model considering the back contact resistance value.

3.1 Capacitance-Voltage measurements (C-V)

Capacitance-Voltage measurement or CV measurement is a technique to characterize the electrical properties of semiconductor materials and devices and also the quality of the interfaces. In general, the CV measurements are done using two different methods, quasi static and high frequency. The measured data is used to plot a CV curve which graphically displays the capacitance per unit area of MOS diode as a function of bias voltage.

One can get the qualitative information of the insulator from the CV measurements, like mobile charge density, dielectric constant, fixed charges and defects at the bulk and interface. Quantitative information like interface trap density, the charge carrier densities at the interface can also be found from the CV measurements [35,36].

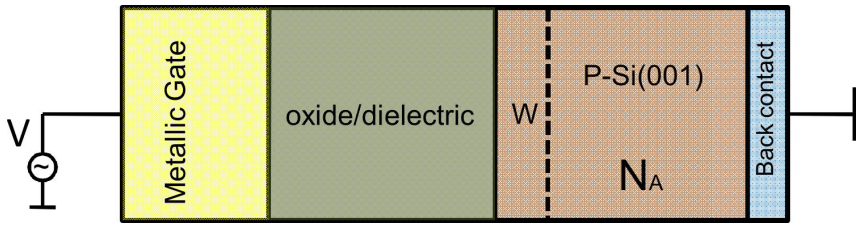


Figure 3.1 - Schematic of MOS diode with applied reverse bias voltage [30].

Let us consider a MOS diode as in Fig. 3.1 with top metallic gate and Oxide/dielectric. A space-charge region of width W formed after applying a reverse DC bias voltage, V, inside the p-type semiconductor with doping density N_A. The differential or the small signal capacitance can be defined by

$$C = \frac{dQ_m}{dV} = -\frac{dQ_s}{dV} \qquad [35] \qquad (3.1)$$

where Q_m and Q_s are the metal and semiconductor charges. The charge increment dQ_m need to be balanced by an equal semiconductor charge increment dQ_s, together with the bound interface charges Q_{it} to maintain the overall charge neutrality. The semiconductor

charge is given by

$$Q_s = qA \int_0^W (p - n + N_D^+ - N_A^-) dx \approx -qA \int_0^W N_A dx \tag{3.2}$$

where the approximation is obtained by considering the depletion approximation as $N_D = 0$ and $p \approx n \approx 0$ and all the acceptors are ionized. During the CV measurement, a small AC voltage signal is applied to the MOS diode, which changes the the amount of charge in the capacitor [35]. The applied voltage is thereby divided partly on the oxide and partly on the semiconductor, thus increasing the gate voltage V as the sum of the oxide voltage V_{ox}, the flat band voltage V_{FB} and the surface potential ϕ_s can be written as:

$$V_G = V_{ox} + V_{FB} + \phi_s \tag{3.3}$$

The flat band voltage V_{FB} comes from the work function difference between the gate metal and the semiconductor. Due to this potential difference, there will be band bending in the semiconductor near the interface without any external voltage. Only by applying the flat band voltage from the outside, the band bending can be canceled, and the flat band case be set. The flat band voltage does not contribute directly to the total capacitance, but simply shift the position of the CV curve on the voltage axis in the appropriate direction. The inverse of the total capacitance can be the sum of the inverse of individual capacitance and can be written as:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_s} \tag{3.4}$$

wherein the capacitance of the semiconductor C_s is the sum of Q_s, the change of the individual types of charges, divided by the surface potential in the semiconductor, comprised of:

$$C_s = -\frac{dQ_s}{d\phi_s} = -\frac{dQ_p + dQ_b + dQ_n + dQ_{it}}{d\phi_s} \qquad [35] \tag{3.5}$$

Here Q_n and Q_p are the charges of electrons or holes and the Q_b charge caused by the space-charge region in the semiconductor.

Oxide capacitance is the ratio of the sum of charges inside semiconductor Q_s and interface trap charges Q_{it} to the voltage drop across the oxide:

$$C_{ox} = -\frac{dQ_s + dQ_{it}}{dV_{ox}} \qquad [35] \tag{3.6}$$

The different charge states of the MOS diode, namely the accumulation, the depletion and the inversion charge and even the strength of small alternating voltage play separate role during the CV measurement.

For a highly doped p-substrate in accumulation, i.e. at negative gate voltage, Si is

highly conducting, so that one can assume a short circuit across the capacitor C_s. This makes the capacitance of the semiconductor $C_s = \infty$, because the charge in the case of short circuit can be changed arbitrarily in small variation of the potential. This is clear from equation-3.4 that the total capacitance in case of accumulation:

$$C = C_{ox} \tag{3.7}$$

For the same case at low positive voltages, i.e. in the region of depletion, the charges of the space charge zone $Q_b = -qN_AW$ [35], and also the fixed interface charges, Q_{it} dominate. So for the *total capacitance in depletion* can be written:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{it} + C_b} \tag{3.8}$$

For inversion, one must distinguish two cases. The applied frequency of the small AC signal here plays a decisive role during the measurement. In case of low frequencies, the behavior is like accumulation, dominated by the number of electrons Qn, that forms a short-circuit path. For *small frequencies in inversion* oxide capacitance refers to the total capacitance:

$$C = C_{ox} \tag{3.9}$$

For high frequencies it is rather more complicated. High frequencies mean, the frequencies which the inversion charges Q_n can not follow. In this case Q_b dominates and it is obtained for the total capacitance in inversion at high frequencies.

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_b} \tag{3.10}$$

where $C_b = \epsilon_{rs}\epsilon_0/W_{inv}$ with the space charge region width in inversion W_{inv} and dielectric constant of the semiconductor ϵ_{rs}. The typical CV measurements usually take place at sufficiently high frequencies. The measured capacitance in inversion is smaller than the capacitance in accumulation. This fact can easily seen by the comparison of the two equations (3.7) and (3.10), since the total capacitance in the case of inversion, C_b becomes smaller by the fraction of space charge zone. Rearranging equation-3.10 to C, and factoring out C_{ox} makes the situation clear again:

$$C = C_{ox}\frac{1}{1 + \frac{C_{ox}}{C_B}} \tag{3.11}$$

In the case of inversion the capacitance is therefore smaller by a factor of $(1 + \frac{C_{ox}}{C_B})$ than in accumulation.

3.1.1 Correction of C-V measurements using series resistance

A simplified model of the electronic measuring system is the "two element model", which is used in the CV measurement, but does not give the correct results. The measured

accumulation capacitance based on "two element model" is less than (Fig. 3.3) the actual capacitance of the capacitor. That means "two element model" is not sufficient to measure the actual capacitance. Therefore to obtain actual capacitance of the capacitor, the measured values were corrected by a "three element model", as in [42]. This model has been used successfully in the literature to describe the situation of the MOS diode properly with the thin insulating film and a low resistance of the substrate and the oxide layer [43, 44]. The result of the correction is usually higher and the capacitance remains constant in the region of accumulation, as expected for a real capacitor. The following explains how the correction is carried out and the base of their foundation is described below.

The "two element model", that was used during the measurement, is the equivalent circuit diagram for describing the MOS diode by a parallel circuit of a capacitance C_0 and a resistance R_0. Corresponding conductance G_m appears due to the leakage current through the oxide, as shown in Fig. 3.2(a).

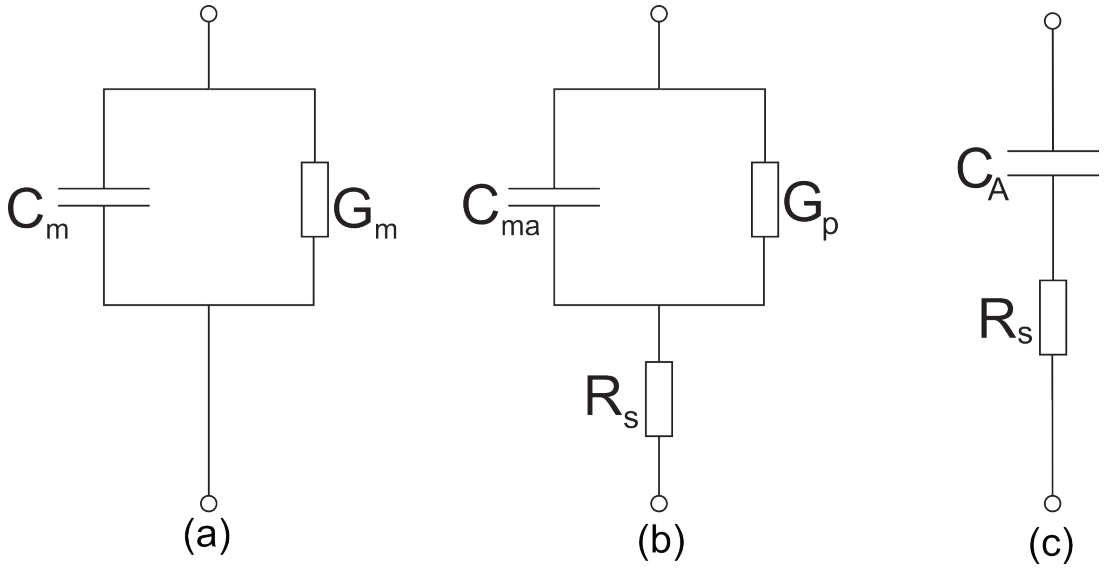


Figure 3.2 - Equivalent circuits of MOS-C (a) "two element model" with measured capacitance (C_m) and conductance (G_m) in parallel (b) "three element model" with series resistance (R_s), measured capacitance at accumulation (C_{ma}) and parallel conductance (G_p); (c) simplified version of (b) with accumulation capacitance (C_A) and serial resistance R_s [54].

The problem in this model is the measurements of the apparent frequency dependence of the resistance.The shape and height of the curve change at accumulation in this model as a function of the frequency [42]. To get rid of this non-physical dependence, a new equivalent circuit with three elements is used in which an additional resistor Rs is connected in series, in Fig. 3.2 (b). In case of very high applied AC frequency at strong accumulation, the parallel conduction (G_p) is negligible in comparison to accumulation capacitance, ($C_A >> G_p$) and can be easily ignored. Fig. 3.2 (c) shows the simplified version of "three element model" at accumulation.

To measure the R_s, the MOS capacitor is biased into strong accumulation, Fig.-3.2 (a). Considering the two element model, the measured impedance Z_m at strong accumulation in terms of the measured capacitance C_m and equivalent parallel conductance G_m becomes,

$$Z_m = G_m + \frac{1}{j\omega C_m} \tag{3.12}$$

Series resistance is the real part of the impedance $Z_m = \frac{1}{Y_m}$. Taking into account the back contact resistance of the wafer, R_s the two element model converts into three element model [Fig. 3.2(b)] and the impedance of the modified circuit would be:

$$Z_m = R_s + Z_p = R_s + \left[G_p + \frac{1}{(j\omega C_{ma})}\right] \tag{3.13}$$

Comparing the real and imaginary parts of the two and three element model, one can get the relation of back contact resistance R_s with the parallel conductance G_p and measured capacitance at accumulation C_{ma} at sufficiently high frequency ω as:

$$R_s = \frac{G_p}{G_p^2 + \omega^2 C_{ma}^2} \tag{3.14}$$

Corrected capacitance:

$$C_c = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{a^2 + \omega^2 C_m^2} \tag{3.15}$$

and

$$G_c = \frac{(G_m^2 + \omega^2 C_m^2)a}{a^2 + \omega^2 C_m^2} \tag{3.16}$$

Here, $a = G_m - (G_m^2 + \omega^2 C_m^2)R_s$, C_m and G_m are the capacitance and the equivalent parallel conductance measured across the terminals of the MOS capacitor.

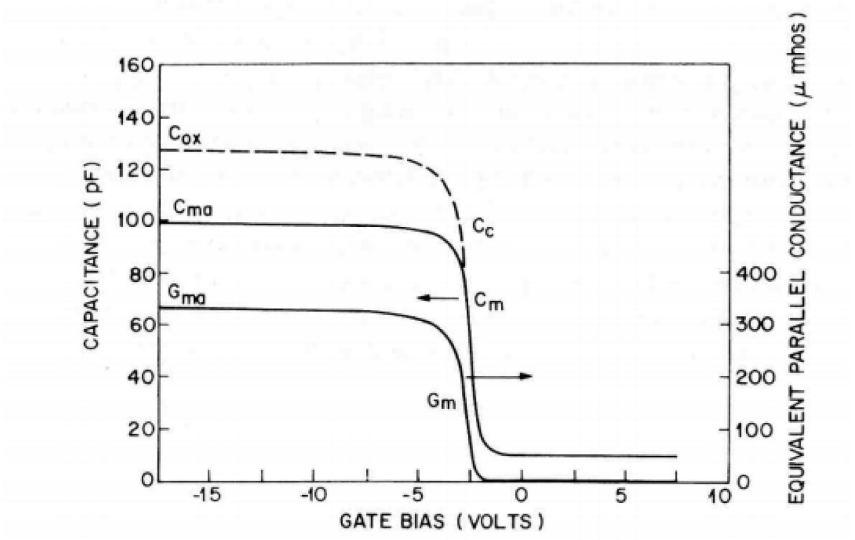


Figure 3.3 - Measured (C_{ma}) and corrected capacitance (C_c) according to three element model at 1 MHz including series back contact resistance (R_s). Equivalent parallel measured conductance (G_{ma}) also shown in right axis. [42].

In Fig. 3.3 we can see an example of the corrected CV curve using three element model. Measuring frequency dependent impedance at different points of the CV curve in accumulation, one can get the idea of frequency dispersion and hence the idea of the quality of sample. By proceeding in a similar manner to the real parts of the impedance, one can obtain also the actual values of the leakage current resistance.

3.1.2 Practical realization of the C-V measurements

In practice, our MOS diodes were investigated with high-frequency CV measurements, whose frequency typically falls in the range of 100Hz to 1MHz. With that one can stay in the sufficiently high frequency range, as described in section 3.1.1. The equivalent measuring arrangement is shown in Fig.3.4. Here, in the equivalent circuit C corresponds to the capacitance and G is the conductance of the MOS diode. The illustration is shown here in a parallel circuit of "two-element model". But the actual situation of a MOS diode with a thin gate oxide can not be explained properly for all voltage ranges by this equivalent circuit.

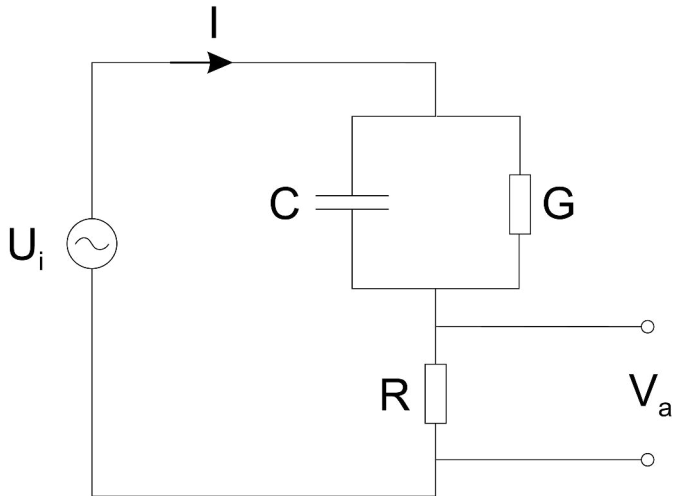


Figure 3.4 - Measuring setup of CV measurements by the "two element model" in a parallel circuit arrangement ([35]).

In the circuit it is shown that an AC voltage U_i is applied, which is slowly increased from $10mV$ to $30mV$. Each small step of the applied voltage corresponding to a measurement point in the C-V measuring curve.

The voltage V_a is measured, via the resistor R. In Fig. 3.4 a simple relationship exists between the voltages U_i and V_a

$$V_a = IR = \frac{R}{Z}U_i \qquad [35] \tag{3.17}$$

with the complex impedance Z, for the alternating current of the whole system. The impedance consists of a parallel combination of conductance G and capacitance C (by inverse addition of resistance) together with the resistance R in series:

$$Z = R + \frac{1}{G + i\omega C} \qquad [35] \tag{3.18}$$

We can get a slightly more complicated expression by substituting Z in Eq. (3.17), and modifying it a little as below

$$V_a = \frac{RG(1+RG) + (\omega RC)^2 + i\omega RC}{(1+RG)^2 + (\omega RC)^2} U_i \qquad [35] \tag{3.19}$$

Under the assumptions $RG \ll 1$ and $(\omega RC)^2 \ll RG$ we simplify the formula to the expression

$$V_a \approx (RG + i\omega RC) \cdot U_i \qquad [35] \tag{3.20}$$

In the real part one can find the conductance and in imaginary part the capacitance of the equivalent circuit. By measuring the output voltage V_a with a phase-sensitive detector, one can determine the conductance G and capacitance C, by knowing the value of resistance R and the frequency ω. The resistor R is to be chosen so that the above mentioned assumptions for the accuracy of Eq. (3.20) are valid.

3.1.3 Qualitative analysis of different defects from C-V measurements

From the shape of the CV curve, one can get several qualitative bits of information based on the quality of the insulating layer. Different types of defects yield their own distinctive characteristics in the CV curve. Typical features include the slope of the CV curve, the position of the flat-band voltage on the voltage axis, or a hysteresis appearing in the measurement between the forward and reverse bias at depletion region.

3.2 Current-Voltage measurements (I-V)

Current transport mechanisms

To explain the current conduction nature of high-k dielectric materials, many conduction mechanisms have been proposed, some of those mechanisms are as follows [57]:

1. *direct tunneling (DT),*
2. *Fowler-Nordheim(FN) tunneling,*
3. *Poole-Frenkel (PF) effect,*
4. *trap-assisted tunneling,*
5. *hopping of thermally excited electrons,*
6. *field ionization of trapped electrons,*
7. *shallow trap-assisted tunneling, and*
8. *space charge limited current (SCLC).*

For a thin film of good dielectric, the current conduction usually happens by PF and FN currents and in the case of ultra-thin (<3 nm) oxide by DT current. Trap-assisted conduction, hopping and space charge limited conduction take place in case of thin insulators with high trap density. Band offset (either conduction band or valence band) between the silicon substrate and the dielectric plays an important role in conduction mechanism such as FN, PF and DT. Due to the presence of some nano- or micro- crystallites in different modifications of high-k materials, the band offset of various sample will be different even for the same gate electrode. This means that the current conduction mechanism and recorded current levels in the high-k materials are affected by the film properties and the material parameters.

It seems that the conduction mechanisms mentioned above are not sufficient to describe the conduction through ionic (heteropolar) high-k dielectrics. Thus for the ionic high-k materials which are locally crystallized and possess high-trap density, the following conduction mechanisms are also important [58]:

1. *grain boundary conduction,*
2. *phonon-assisted tunneling, and*
3. *Poole-Frenkel with multi-phonon trap ionization.*

However, several factors play important role for the effective barrier height and the injection of carrier from the silicon substrate into the dielectric. According to Gauss's law, when an electric field is applied across a high-k stack, nearly all the voltage drops across the layer of small dielectric constant (i.e. SiO_2); the interface barrier is reduced for this reason. The value of effective barrier height depends on several parameters like dielectric-substrate interface, dielectric constant, and the thickness of dielectric layers [59].

Different trap-assisted conduction, Poole-Frenkel conduction, space-charge limited current and the local electric field distributions are affected by the trap density in the dielectric film. Compared to silicon dioxide, high-k metal oxides have higher trap levels, because of their ionic nature and smaller stability [60]. The primary source of oxide traps are the large number of oxygen vacancies(OV). Due to industrial processing temperature of high-k dielectric ($< 700°C$), it is possible to incorporate defects and incomplete oxidation, which leads to a higher amount of trap densities.

If the applied electric field across the high-k dielectric layer is lower than 8 MV/cm, the corresponding current conduction is trap-assisted current. That means the conduction happens due to the electrons tunneling into the shallow traps of the high-k insulator. In case of higher electric field, that means greater than 10 MV/cm, the conduction is mainly due to the Fowler-Nordheim(FN) tunneling and also depends on the preparation conditions of the dielectric layers. But if the applied field is within the range of moderate-field, both the FN current and direct tunneling mechanism of electrons can take-part to fill-up the traps, as a result a quasi-saturation region appears in the leakage current.

3.2.1 Determination of charge carrier densities at the interface

In order to analyze the leakage current mechanism and to get further insight into the details charge transport mechanism through the dielectric medium, it is essential to determine the density of trap states at the interface of semiconductor/insulator. The attribute of dangling bonds at the interface of semiconductor/insulator is known as interface traps or states. These interface traps control the quality of thin high-k dielectric films grown on top of the substrate. There are few famous methods of scanning the energy gap using simple C-V (capacitance-voltage) and I-V (current-voltage) measurements of MOS diode to determine the distribution of the interface states near the conduction and valence band edges. Three of the most famous methods are discussed below:

Terman method

One of the first methods for determining the interface trap density was the Terman method. It is a high-frequency capacitance method at room-temperature [53]. The high frequency capacitance technique used to determine surface state charge by comparing a high frequency C-V curve (0.1-1.0 MHz) with an ideal C-V curve. In this hf C-V measurement method, the applied frequency is sufficiently high to freeze the response (to charge and discharge) of interface traps which therefore, do not contribute to the capacitance. That means there is no frequency dependent response of interface trap charges but only applied bias voltage.

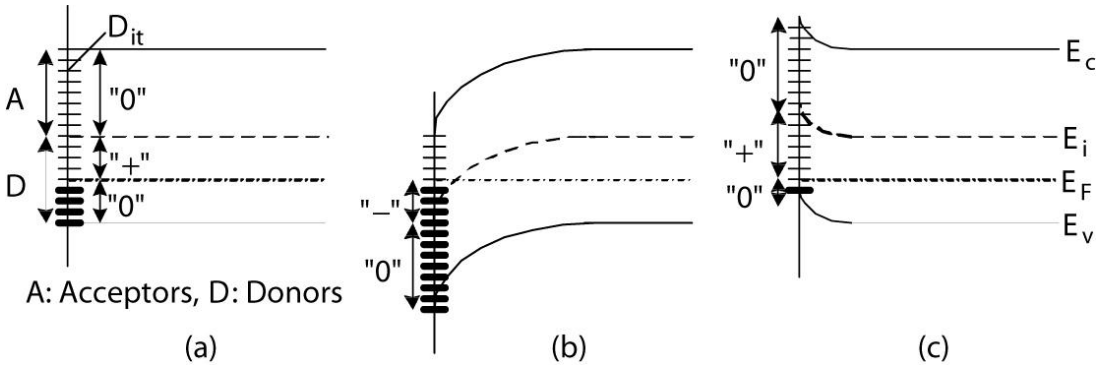


Figure 3.5 - Band diagram of semiconductor shows the effect of interface traps, (a) $V_G = 0$, (b) $V_G > 0$, (c) $V_G < 0$. Small horizontal heavy lines indicate the occupied interface states and rest are unoccupied.

The nature of interface traps at different bias condition shown in figure-3.5. Below E_i, states attribute like donor (D) and above E_i like acceptor (A), as shown in fig. 3.5(a). States within energy range $E_F < E < E_i$ are unoccupied donors and hence positive. Donor interface states below E_F are occupied by electrons, again above E_i are unoccupied acceptor states and hence both are neutral. If we apply positive gate voltage (fig. 3.5(b)) few acceptor states goes below E_F and show a net negative charge. In case of negative gate voltage (fig. 3.5(c)), there are more unoccupied donor states and show net positive charge. Here interface traps respond only to the slowly varying DC gate voltage and the result is the stretch out of the hf C-V curve along the gate voltage axis as the interface trap state occupancy varies with the gate bias voltage Fig. 3.6(a).

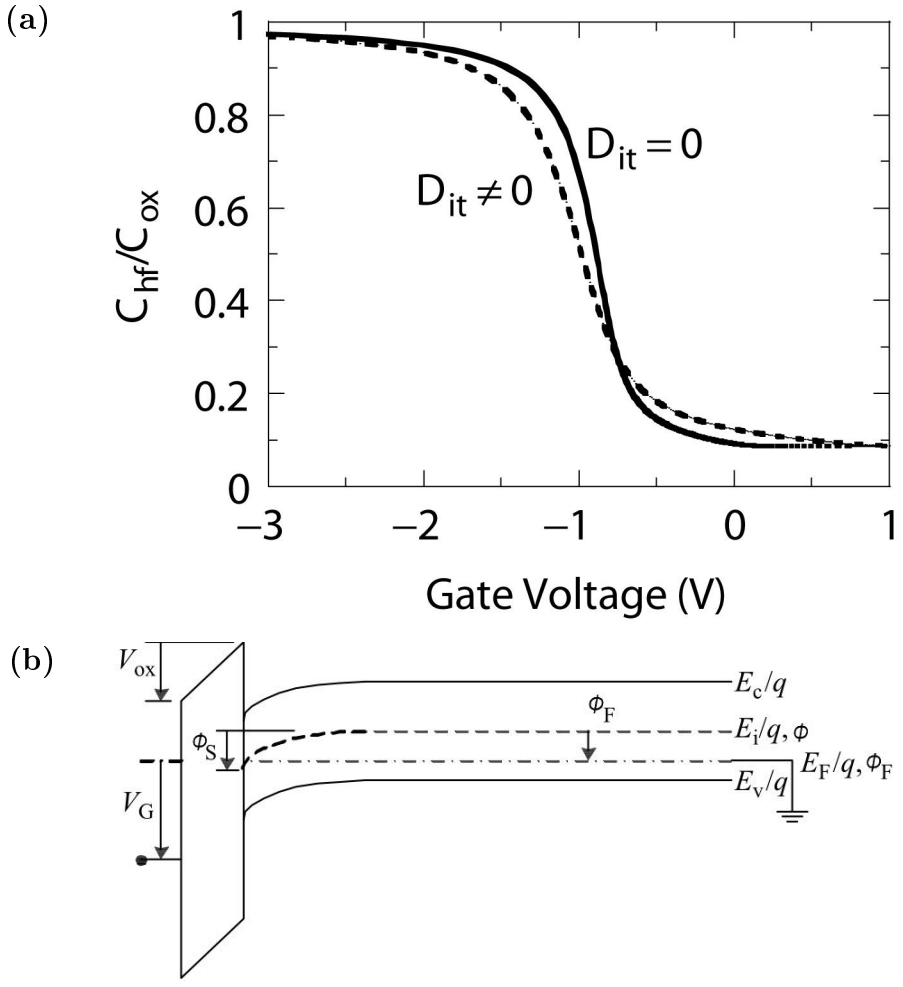


Figure 3.6 - (a) Theoretical high-frequency C-V curve of a MOS diode, with and without interface trap density (D_{it}), (b) Band diagram of a MOS diode [29].

The gate voltage drop partially across the oxide and partially across the semiconductor, hence the applied voltage splits inside the MOS diode as shown in figure- 3.6(b). In case of a MOS-C in depletion or inversion, applied gate voltage (V_G) induces additional semiconductor charges like space charge (Q_b), doping charge (Q_n), interface charge (Q_{it}), where $Q_G = -(Q_b + Q_n + Q_{it})$.

$$V_G = V_{FB} + \phi_s + V_{ox} = V_{FB} + \phi_s + Q_G/C_{ox} \qquad [35] \tag{3.21}$$

Where, V_{FB} is the flatband voltage, V_{ox} the oxide voltage, and ϕ_s the surface potential. For a given surface potential ϕ_s, variation in gate voltage creates a stretch-out in C-V curve (Fig. 3.6(a)), which produces a non parallel shift of C-V curve. But in case of peaked distributions of interface traps, C-V curves produce more abrupt distortions.

In this method at first one has to find the ϕ_s for a given C_{hf} from the the ideal C-V curve, then V_G has to be found from the experimental curve for the same C_{hf}. Repeating

the same process one has to draw a ϕ_s versus V_G curve. The relevant interface trap information can be extracted from this $\phi_s - V_G$ curve [54].

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{dV_G}{d\phi_s} - 1\right) - \frac{C_s}{q^2} = \frac{C_{ox}}{q^2}\frac{d\Delta V_G}{d\phi_s} \qquad [30] \tag{3.22}$$

Here $\Delta V_G = V_G - V_G(ideal)$ is the shift of voltage between the experimental and the ideal curve, and V_G is the experimental gate voltage.

Limitations of the Terman method

The Terman method works well for measuring interface trap densities of $10^{10}\ cm^{-2}eV^{-1}$ and above [55], but has been widely criticized for lower trap densities. For thinner oxides, the voltage shift associated with the interface traps also decreases. Simulations have shown that the interface state capacitance is small but not negligible, compared to the voltage stretch out of the thin dielectrics [56]. For thicker dielectrics, the interface state capacitance is same, but the voltage stretch out increases. Since both the interface trap capacitance and the voltage stretch out scale with D_{it}, and this method becomes questionable for thin oxides. Again one needs to know exactly the doping density of the substrate to compare the experimental curve with theoretical one. Any piled up dopant or diffusion can introduce an error. Surface potential fluctuations can cause fictitious interface trap peaks near the band edges. Sometimes if the applied frequency is not sufficiently enough, the assumption that the interface traps do not follow the ac probe frequency may not be satisfied for the surface potentials near flatband and towards accumulation.

Gray-Brown method

Another method of determining interface trap density is the Gray-Brown method. According to this method the high frequency capacitance is measured as a function of temperature [52]. By monitoring the temperature dependence of the flatband voltage of high frequency C-V curve in principle one can detect slow traps, as slow as 1s [59]. At lower temperatures the Fermi level shift towards the majority carrier band edge and the interface trap time constant τ_{it} also increases. At low temperatures it is difficult for the interface traps near the band edges to respond to typical ac probe frequencies whereas they can easily respond at room temperature. So this method could be used to determine the interface traps D_{it} near the majority carrier band edge [30] [41].

The typical hf CV curves are usually measured at room temperature and at liquid nitrogen temperature. The measured flat-band voltages at those two temperatures are used to calculate the interface trap density. Like the Gray-Brown method, the Terman method detects the occupancy rather than the AC response of traps and, therefore, it is not limited by the frequency of the AC signal. However, both methods face the same difficulty to obtain ideal high frequency C-V curves without significant D_{it} induced distortions. Like the Terman method the interface trap occupancy also changes here but not due to the

change of gate voltage rather the changes of temperature. From the analyzed interface trap occupancy the corresponding D_{it} can be extracted using the experimental data.

Conductance method

The conductance method was established for the first time by *Nicollian and Goetzberger* presented in a short paper in 1965 [39]. A detailed description of this method was published by the same authors in 1967 [40]. Unlike the Terman and the Gray-Brown method discussed above, in this method the interface state density is not determined from the CV curves, but from the conductance-voltage curve (G-V). As mentioned in the previous section, there are some limitations in the Terman method [38], but those are not coming into play here. The main difficulty in Terman method is the extraction of interface capacitance from the measured capacitance, which additionally consists of the capacitance of the oxide and depletion zone. In conductance method method determination of interface trap density is fully based on measured data and hence fully reliable and gives the exact value of D_{it}.

To measure the interface trap level density as a functions of gate bias and interface trap time constant dispersion, admittance must be measured as a function of both gate bias and frequency.

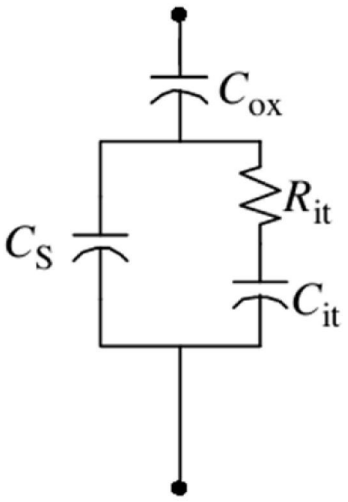


Figure 3.7 - Equivalent circuit of MOS diode with interface traps.

The conductance comes only from the charging and discharging of the interface states and that should allow a much more direct analysis.

$$\frac{\langle G_p \rangle}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} ln\left[1 + (\omega\tau_{it})^2\right] \tag{3.23}$$

The equivalent MOS diode including interface traps is seen in figure-3.7, here $\tau_{it} = R_{it}C_{it}$ = interface trap time constant. If the applied voltage to the circuit is equal to

flatband voltage, there will be no bias voltage driven conductance through the diode. At this particular case If we gradually increase only the frequency of applied AC signal from lower (100Hz) to higher (1MHz) value, we get frequency driven conductance. But at a certain frequency ($\omega \approx 2/\tau_{it}$) when the interface traps come into resonance with applied frequency we get the maximum conductance through the diode (fig. 3.8). This conduction or leakage current is only due to the interface traps and can be used to measure the density of interface traps.

Now we can write an approximate expression of interface trap density by substituting the value of ω in the above equation, in terms of maximum measured conductance as:

$$D_{it} \approx \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{max} \tag{3.24}$$

The measured admittance of MOS-C from figure- 3.2(a) is $(G_m + j\omega C_m)$, where C_m is the measured capacitance and the measured parallel equivalent conductance is G_m. By converting the admittance to impedance, subtracting the reactance of oxide capacitance from it, we convert the impedance again into admittance. Now using the real part of admittance and the above relation of $< G_p > /\omega$, we get:

$$\frac{\langle G_p \rangle}{\omega} = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \tag{3.25}$$

Here oxide capacitance (C_{ox}) is measured in strong accumulation of the capacitor, $\omega =$ angular frequency $= 2\pi f$, where f is the applied frequency.

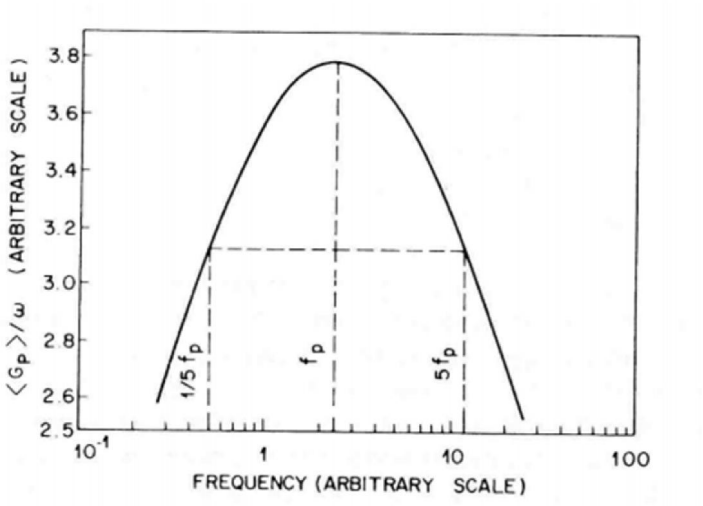


Figure 3.8 - $< G_p > /\omega$ versus log frequency curve, where f_p is the peak value of $< G_p > /\omega$ [29].

Figure 3.8 shows a typical $< G_p > /\omega$ versus log frequency curve from which maximum conductance is to be determined to calculate the interface trap density. If the admittance is measured as a function of frequency with gate bias as parameter, the maximum value of $< G_p > /\omega$ will be at a lower frequency, but if the admittance is measured as a function

of gate bias with frequency as parameter, we will find maximum at a gate bias closer to flatbands [54].

4 Experimental Setup

A part of our sample cleaning, different materials deposition on substrate and spectroscopic characterization of our unstructured sample were carried out in an UHV chamber all in-situ. Our UHV system was equipped with several spectroscopic facilities like X-ray Photoelectron Spectroscopy (XPS), Ultraviolet Photoelectron Spectroscopy (UPS), Spot Profile Analysis - Low Energy Electron Diffraction (SPA-LEED) and Electron Energy Loose Spectroscopy (EELS). The preparation of different oxides (*i.e.*BaO, SrO, $Ba_{0.7}Sr_{0.3}O$) and subsequent formation of silicates (*i.e.*Ba_2SiO_4, Sr_2SiO_4, and $(Ba_{0.8}Sr_{0.2})_2SiO_4$) were carried out in this UHV system. The system is a commercially available UHV chamber from the company *Leybold-Heraeus*, which has been updated over the years since it was purchased with several extensions. The UHV chamber consists essentially of three parts: the main chamber with a base pressure of 4×10^{-11} mbar, the main-load-lock ($\sim 5 \times 10^{-10}$ mbar) and the pre-load-lock ($\sim 1 \times 10^{-6}$ mbar). Through the two load-lock systems one can gradually transfer the sample from the pre-load-lock system to the main chamber without venting the vacuum. There are parking positions for samples in the main load-lock system, where one can park upto three samples and use them whenever necessary for measurement purpose. Which of course save the time of ventilation and pumping down the pressure in the chamber.

It is possible to investigate the different electrical, chemical and structural properties of the sample using various instruments in our UHV chamber. For example one can use photoelectric spectroscopy methods like XPS and UPS to characterize the chemical properties of the sample. To determine the structural properties, like crystallinity and lattice constant we use electron diffraction techniques like SPA-LEED, which is very surface sensitive due to low electron energy. To determine some electrical properties like band gap and band offset of an insulator film we used EELS, where loose energy spectroscopy of excited states can be measured by the detection of energy loose of incident electron after bombardment with the sample surface.

When the pressure of the chamber goes high for some reasons, it is essential to check the composition of the residual gas in the UHV system to get an idea about the possible reason of the elevated pressure, which was usually done by a mass spectrometer, also installed in our UHV chamber. If it is found that the detected gases are mostly from air or water, it is obvious that leak appears on the system. Helium gas was used along with the mass spectroscopy to find the position of the leak in the UHV system

4.1 Principle of an electron beam evaporator

To deposit the insulating layer on the substrate, the system was equipped with several evaporators, like Barium (Ba), Strontium (Sr), Aluminum (Al), Silicon (Si) and Gold (Au). Instead of silicon evaporator all other evaporators were manufactured in our Institute workshop. These are electron beam evaporators and the evaporating material is placed in a conductive crucible or enclosed the crucible by a conductive material, like

tungsten wire or thin Ta or Mo plate.

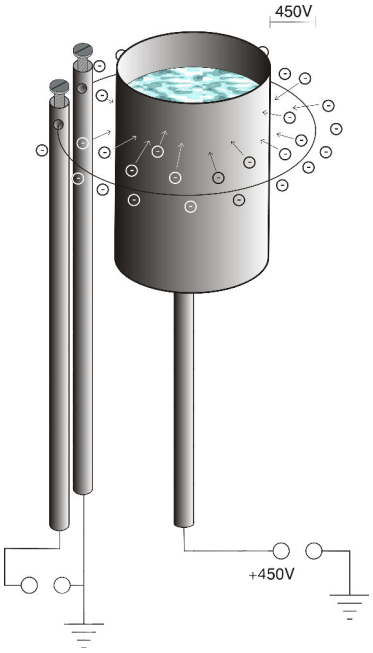


Figure 4.1 - Diagram shows how electrons discharge from a heated filament due to Edison Richardson effect. These are accelerated by the high voltage to the crucible and heat the crucible up.

A schematic diagram of an electron beam evaporator is shown in figure-4.1. There is a crucible attached with the center rod and a tungsten wire of diameter 0.075-0.125mm usually clamped around the crucible with two electrical contacts at a distance of about 4-5mm. Once we pass current through the wire ($\sim$ 2A/4V), it begins to glow. If we apply a positive voltage of 450-1000V between the filament and the crucible, the electrons are emitted from the filament due to the Edison Richardson effect [30]. These emerged electrons hit the crucible and their kinetic energy transforms into heat and warm the crucible up. In this way materials in the crucible were heated up and are eventually evaporated from the crucible on to the sample surface. There are many materials which sublimate directly from the crucible due to the very low pressure inside UHV. If evaporation by sublimation is sufficient the liquid phase of the material inside crucible does not exist, so it is possible to mount the evaporators for such materials in a horizontal position. The deposition rates depend very strongly on the heating power and the used material. Based on the vapor pressure one can have a rough guideline for the prediction of deposition rates, especially by comparing two materials. The higher the vapor pressure at the same temperature is, the higher the evaporation rate will be. Such tables and graphs for vapor pressures can be found for example in [20, 31].

4.2 Material handling of different evaporators

Ba and Sr are very hygroscopic metals in comparison to Al, Au or Si. If they are brought in contact with air, they react with the humidity of air and within a few second the surface of the metals converts into hydroxides. Within few minutes these materials completely disintegrate into white powder pieces of few mm in diameter. In direct contact with water,

the reaction is so violent that strong emission of relatively large amounts of gas in the form of bubbles is observed. The reaction that occurs here is as follows:

$$\begin{aligned} 2Ba(s) + O_2(g) &\rightarrow 2BaO(s) \\ 3Ba(s) + N_2(g) &\rightarrow Ba_3N_2(s) \\ Ba(s) + 2H_2O(g) &\rightarrow Ba(OH)_2(aq) + H_2(g) \end{aligned} \qquad [32]$$

Because of this reactivity of the pure Ba/Sr metal, repairing or refilling of the Ba/Sr evaporator is a matter of great effort. In both cases, the metals must be protected from the contact with water and also from the air of environment.

Therefore the crucibles were filled under constant flow of nitrogen gas in a *glove bag*, a kind of transparent plastic bag with large glove ports on the side. For this, at first the Ba or Sr was broken with small cutting pliers into about 1-3mm small chunks. These pieces were inserted directly into a Mo crucible of Ba evaporator with the aid of a ceramic rod and a hammer to compress the material.

A *glossy carbon* crucible was used to evaporate Sr. Glossy carbon is high purity carbon pressed under high pressure and temperature in the form of high purity carbon with the name of $SIGRADUR^{®}$ and offered by the company *HTW Hoch Temperatur Werkstoffe GmbH* [33]. It is high temperature resistant up to 3000°C and has a very low wettability for a large group of materials. The disadvantage of this material is its high brittleness, so unlike Ba, it is not possible to hammer the material directly into the crucible. One of the solutions is to form small pills of Sr of same diameter as the crucible, which can directly be inserted into the crucible. For this purpose, a cylindrical structure was prepared (made of V4A), with which it was possible to hammer Sr with a holding device and to form small pills or tablets of Sr. These are then put into the glassy carbon crucible with a pair of tweezers. During the entire time after filling, from mounting to installation in the UHV the contents of the crucible is protected by a layer of n-hexane on top, which has a particularly low proportion of water ($\leq 0.004\% H_2O$ [34]). The installed evaporator, has to be drizzled in short intervals with dried hexane to avoid the reaction with water in ambient air. Within a few minutes, the installation of the evaporator has to be completed in order to protect it from the further influence of moisture in air with the help of evacuation process.

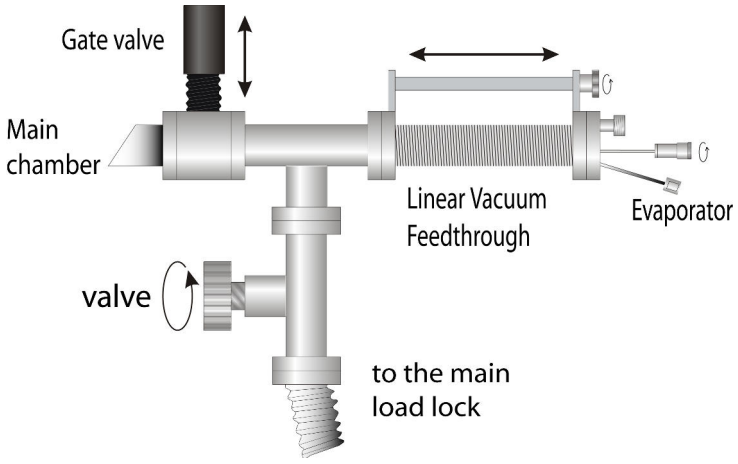


Figure 4.2 - Structure of the evaporator load lock. The evaporator can retire and separate from the main chamber with the help of gate valve, which helps venting and evacuation of the part without venting the main chamber.

The construction of a separable evaporator branch can be seen in Figure 4.2. One can access the main chamber through a sealed gate valve. It is connected to the main load lock via a further valve. After opening this valve, the evaporator can be vented via the load lock and also evacuated later. This construction allows to repair and re-fill the single evaporator without venting the main chamber.

4.3 Types of sample holders and their use

Depending on the application, two types of sample holders were used to hold the sample in the UHV. Drawings of the side and plan view of two types, respectively, are shown in Fig.4.3 and 4.4. In principle it is possible to connect up to six electrical contacts on the manipulator arm in both types of sample holder. Four of these contacts are carried out by the Mo jaws which are electrically isolated from each other but connected with the sample. Two further contacts, which can be installed on the backside of the holder, serve to measure temperature via thermocouples. For the sample holder in Fig.4.3 no thermal contacts are currently in use but this optional upgrade could be done if necessary.

Unstructured samples have been used to investigate different sample properties using XPS, EELS or SPA-LEED. Resistive heating is used to heat the unstructured samples by passing current through them (see Fig.4.3). The sample is mounted on two Ti contacts for the passage of current and clamped by means of high temperature sustainable molybdenum clamps and screws. Highly doped Si, so-called spacers are placed on the two contact surfaces above and below the sample for an ideal electrical contact. To avoid thermal gradients due to different contact resistance on the sample, it is important that the sample contact is uniform over the entire width of the support surface, during the installation of the sample.

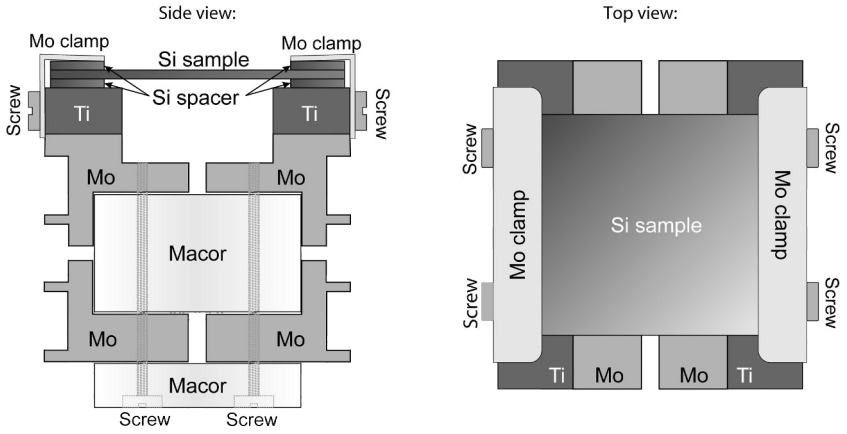


Figure 4.3 - Drawing of the sample holder used for resistive heating of the unstructured samples.

To prepare the structured samples another type of sample holder is used, which is not heated resistively but indirectly. For this sample holder, a boron nitride heater (BN heater) from the company *tectra* is used as shown in Fig.4.4.

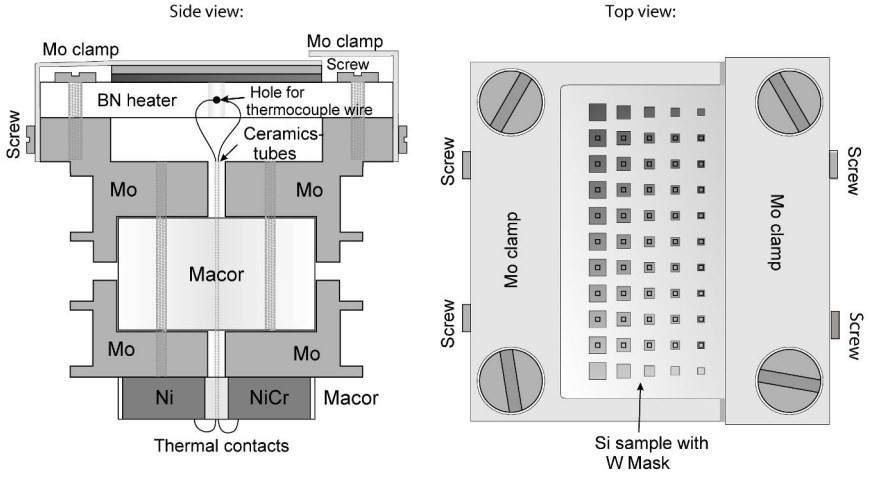


Figure 4.4 - Drawing of BN sample holder used for indirect heating of a structured sample with a W mask. Via Mo clamps, the sample is fixed with screws after sample and mask were aligned with each other under a stereo microscope.

The heater itself heated by resistive heating of the wires within the BN material. Electrical contacts are connected in each case via a mounting screw on both sides, instead of the upper sample holder jaws. The structured sample is mounted on this heater together with an electrically isolated W mask and molybdenum clamps, and heated indirectly on the hot plate. The clamps are chosen in such a size and shape so that areas of the BN

heater that are not covered by the sample, are covered by the clamps. Thereby unwanted evaporation on these areas is prevented. This is important, otherwise next time during indirect heating, the material what was evaporated on these unnecessary areas would evaporate again and contaminate the sample.

The temperature of the BN heater is measured by a Ni/NiCr thermocouple wire that is plugged into a hole (0.5mm in diameter and about 5mm deep) at one side of the BN heater. Via thermal contacts at their back of the holder it is connected with other two contacts on the manipulator, which with the help of thermocouple wires are routed out of the UHV system. It is ensured that no further contact voltage through different combination of materials on the way out of the chamber, can come to distort the measurement. The control of the temperature is achieved via a PID controller box *tectra HC3500*, desired temperature value passes manually via mechanical switches or by RS-232 cable from the PC. This then heats the BN sample holder via the power contacts until the desired temperature is reached. For proper heating of the sample the correct setting of the PID values in the control is a prerequisite to avoid overshoot or a too slow approach or drifting from the target value.

The reason for the use of BN-heater is the use of a mask system. For the preparation of detached MOS diodes a tungsten mask as shown in Figure 4.5 is used, which was put down on the patterned areas of the sample, during the evaporation of BaO, $Ba_{0.7}Sr_{0.3}O$ and of a subsequent Al/Au layer through the windows of the mask. In this way at the same time 45 detached MOS diodes can be prepared, which are physically and electrically separated from each other, after removal of the mask. The size of the overlapping areas on the SiO_2 varies by five different window sizes on the mask, thereby an estimation of the influence of overlapping area on the results of electrical measurements is possible and done, which is subtracted from the measured value after measurements. The unstructured regions of the sample in the windows of the rightmost column in Fig.4.5 allow to investigate the electrical influence of the overlapping region. Since there is no etched areas here, so the electrical properties of the thick SiO_2 layer without the influence of the thin active Ba_2SiO_4 diode can be determined.

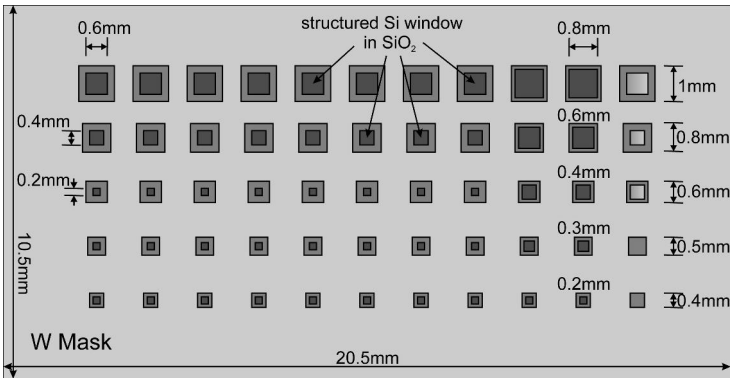


Figure 4.5 - Tungsten mask (light gray) for the preparation of discrete MOS structures. The side length of the window varies between 0.4 and 1mm . Underneath is the structured Si sample (dark gray) with the (0.2×0.2) to $(0.8 \times 0.8) mm^2$ large Si windows inside the SiO_2 (medium gray).

One of the main advantages of the BN heater is that it can be controlled by a computer program. With the help of the *Labview* program the temperature values are passed to the

temperature controller *tectra HC3500*. The simultaneous reading of the actual pressure can be automated with the running flash cycles of the program. Limits can be set for temperature and pressure, at which the flash cycle should start or be interrupted again. In addition, the program allows to set a minimum time between two flash cycles.

Furthermore, one can use this program to fix the temperature at a certain value and maintain it overnight for out-gassing the newly installed sample. To avoid accidents, here a maximum pressure is set which must not be exceeded. It may happen suddenly due to contact problems, that the measured temperature is smaller than the original temperature during the out-gassing of the sample. In this case, the electronics would try to heat up the sample more, in order to adjust the "right" temperature. This can lead to very poor pressure in the chamber and in the worst case due to the high temperature, the sample holder can melt together with the manipulator at the contact surface. At this point, the system will switch off the heating of the sample when the set maximum pressure is exceeded. Further heating in this case would have to be turned on manually again. At all stages it is always possible to do the whole process manually and control carefully each of the steps and hence to prepare the expected quality sample.

There are also disadvantages of the use of the BN heater compared with the other specimen holder. The samples cannot be heated as quickly as with the other sample holder with resistive heating. Although it is possible to heat the sample additionally up to 1200°C with this heater, the pressure of the chamber, even without a clamped sample, will rise too much (about $1 - 5 \times 10^{-7}$ mbar) so that the preparation of high quality sample is not possible. In practice, flash cycles were performed only up to 850°C for 1-2s. This problem is caused by the inertia of heating of the BN heater and the temperature controller, with the consequence that the high temperatures (800-1200°C) can not be reached as quickly as with the sample holder with direct resistive heating. The surroundings therefore heat up unnecessarily and cause a deterioration of the pressure in the UHV chamber.

Another disadvantage is the inability of direct control of the sample quality. Because of the mask and the structuring of the sample, our research methods XPS, LEED and EELS can not be used because they need an area of several mm^2, a large spatial area on the sample surface and therefore no specific examination can be done within the structures. For this reason, the recipes of preparation of the films are first tested on unstructured samples and verified with the corresponding methods to maintain the quality. Then these are implemented on the structured samples later.

4.4 C-V and I-V measurement probe station

The electrical properties of the MOS-diodes are investigated by measurements of current-voltage (I-V) and frequency dependent capacitance-voltage (C-V), conductance-voltage (G-V) [29] characteristics using AC impedance capacitance meters at room temperature. The measurement range of semiconductor C-V measurement for resistors is from $< 0.1\Omega$ to

$100M\Omega$ and capacitors from $< 10fF$ to $1\mu F$. The contamination in the dielectric ranging from roughly 5×10^9 ions to about 1×10^{13} ions per square centimeter and interface traps ranging from about $1 \times 10^{10} cm^{-2} eV^{-1}$ to about $1 \times 10^{13} cm^{-2} eV^{-1}$ charges is also possible to detect [49].

The AC impedance meter also known as an LCR meter (i.e. inductance [L], capacitance [C], resistance [R]), usually measures the complex impedance in combination with an auto balanced bridge maintaining AC virtual ground at the sense side of the capacitor. It is used to measure C-V and I-V characteristics. The meter has a frequency range from 100Hz to 10MHz.

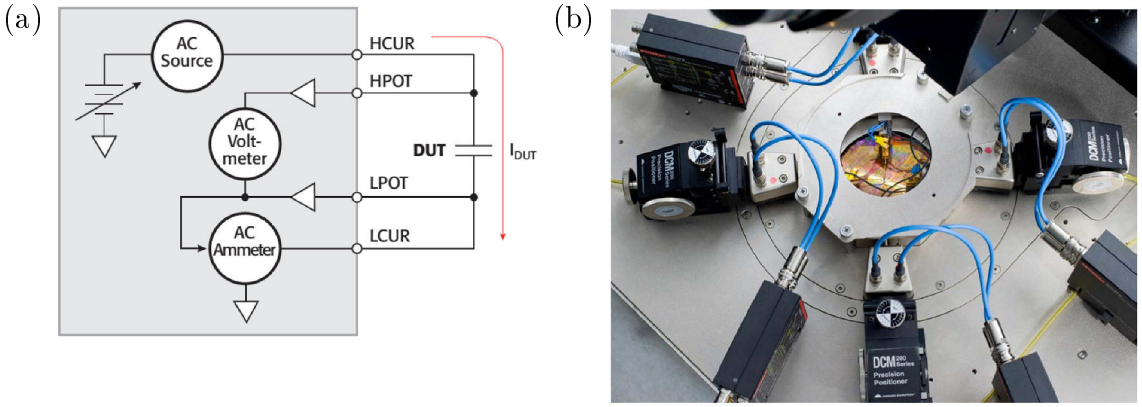


Figure 4.6 - (a) An AC impedance meter, (b) C-V & I-V probe station [49].

The operating circuit diagram of the probe station is shown in figure-4.6. It measures AC impedance by supplying an AC voltage out of the high current terminal (HCUR). The current through the device is measured by the low current terminal (LCUR), and the voltage across the device is measured by the high and low potential terminals (HPOT and LPOT). The voltage and current are measured in a phase-locked manner that precisely identifies the phase angle between them. By knowing the amplitude and phase angle, it is possible to calculate any desired AC impedance parameter.

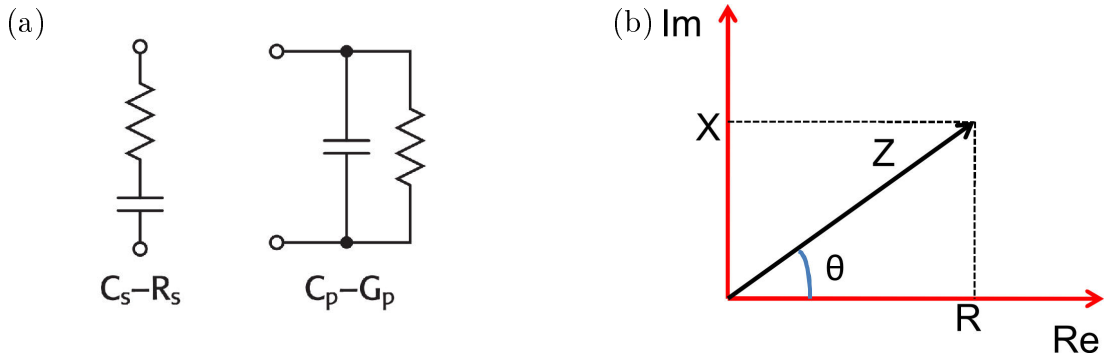


Figure 4.7 - Basic AC impedance parameters (a) Series and parallel impedance models, (b) Relationship between impedance (Z) and phase Angle (θ) [49].

There are two common AC impedance models [figure 4.7(a)], the parallel model and the series model. In the parallel model, results are expressed as the parallel capacitance (C_p) and the parallel conductance (G_p). In the series model, results are expressed as the series capacitance (C_s) and the series resistance (R_s). Measuring AC impedance parameters means measuring the amplitude of the impedance, which can be expressed as $|Z| = \sqrt{R^2 + X^2}$ and impedance, $Z = |Z|exp(j\theta)$. We also have to know the phase angle (θ) between the current and the voltage [figure 4.7(b)]. Hence we can represent the impedance Z as R plus jX, where R represents the real, or in-phase impedance vector, $R = |Z|cos\theta$ while jX represents the imaginary, or 90° out of phase impedance vector, $X = |Z|sin\theta$ which is also the capacitance vector. It is possible to convert the polar and rectangular forms mathematically into actual capacitance and resistance values.

The ratio of the real impedance to the imaginary impedance is called the dissipation factor (D) or the measure of energy loss-rate. It can be expressed as $D = G_p/\omega C_p$, where G_p and C_p are the parallel conductance and capacitance, respectively, and ω is the angular frequency. In both kinds of AC impedance model, the dissipation factor can always be easily calculated.

5 Unstructured and structured samples preparation

For a detailed investigation of the oxide layers with XPS, SPA-LEED and EELS, the oxide films are produced on unstructured samples. To achieve crystalline growth of Ba_2SiO_4 and $(Ba_{0.8}Sr_{0.2})_2SiO_4$, several steps are necessary, which are described briefly below. Detailed information about the growth of crystalline $Ba_{0.7}Sr_{0.3}O$ films are given in [36,37].

5.1 Cleaning of the unstructured Si(001) wafer

The cleaning of the substrate plays an important role on the quality of the oxide films. For a successful crystalline growth of silicate a well defined initial structure is necessary. The unstructured samples (size 10×15mm) are treated with wet chemicals prior to installation into UHV. First a pre-cleaning with petroleum benzene, acetone and Isopropanol took place in an ultrasonic bath about 10min for each solvent. To remove the metallic contamination from the silicon surface a RCA cleaning step is performed. For the removal of the oxide from the silicon surface, a HF dip for 50 second in 1% HF solution followed by rinsing with deionized water is performed. The hydrophobic behavior of the hydrogen-terminated Si surface is checked to assure the cleanliness of the silicon surface. The complete removal of water from the surface by skidding the sample indicates that the silicon oxide is completely removed and a hydrogen-termination has formed. After that, within 5-10min the sample is transferred into the UHV chamber. Within this time the hydrogen termination remains largely intact [35].

At the next step the sample is out-gassed for around 12 hours at about 550°C. Cooled compressed air is passed through the manipulator during the out-gassing in order to heating of the manipulator and an intolerable rise of pressure in the chamber.

After out-gassing we cooled the sample with liquid nitrogen for 1.5 hours. The temperature of the sample then reached about $-80°C$. This cooling is necessary for the subsequent flash cycle. While flashing, the sample is briefly heated at $1100°C$ for 1-2s. In this process, without the counter-cooling the surrounding would heat up too much and the pressure in the chamber would rise, hence the sample quality would suffer. The pressure during the flash process should never be higher than 5×10^{-9}mbar, to be on the safe side, it should not exceed even better if 1×10^{-9} mbar, in order to ensure a good quality of sample. For this reason, the sample is first "trained" by repeatedly heating between 800 - 850°C for $1 - 2$min without exceeding the pressure of 1×10^{-9} mbar. The actual flash cycle to $1100°C$ after the "training" is repeated $3 - 4$ times and the cleanliness and crystalline pattern of the sample is then checked using the XPS and SPA-LEED.

On a clean Si(001) sample only the $Si2p$ and $Si2s$ Peaks should be visible in the XPS. The $O1s$ and $O(KLL)$ auger peak of oxygen and the $C1s$ peak of the carbon may no longer be visible on an ideal sample surface. In particular, the complete removal of carbon from the surface is a major challenge because the C atoms except carbide can only be removed at very high temperatures around 1000°C from the surface. Because of the pressure in the

chamber, such temperatures can only be achieved for a very short time $(1-2s)$. Therefore residues of C are not excluded. If necessary, the flash cycle is repeated one more time. Due to this problem it is made sure that a large part of the C contamination is removed by wet chemical cleaning before installation of the sample. By checking the C and other contaminants of different Si sample using XPS we have found that the RCA cleaning helps to improve the sample quality by a factor of $2-3$ by removing metal contaminants.

On a clean Si(001) surface due to the dangling bonds a (2×1) superstructure is formed, in which adjacent atoms form double rows. This structure can be seen with the SPA-LEED. In LEED image streaky structures or frayed diffraction peaks, indicate a poorly prepared surface, on which for example facets have been formed.

5.2 Metal Oxide Semiconductor diode fabrication

Metal Oxide Semiconductor (MOS) diodes are produced in the UHV chamber on pre-patterned SiO_2/Si samples using a W mask. A sample having 50 electrically independent diodes is produced in the chamber following the manufacturing process and later electrical measurements can be performed individually. The structuring of the samples and the subsequent growth process is explained below.

5.2.1 Structuring of Si(001) samples

For the preparation of free-standing MOS diodes first a patterned thick SiO_2 layer (about $150-200$nm) is required on $Si(001)$, which can be processed in the UHV chamber subsequently. We structured these samples in the clean room of *Laboratorium für Nano und Quantenengineering (LNQE)* in cooperation with the *Institut für Materialien und Bauelemente der Elektronik (MBE)*. They serve as starting material for the production of MOS diodes. First, the wafer is subjected to a HF-dip (dipping the sample in 1.0% hydrofluoric acid for 50s under continuous stirring) and is then rinsed with DI water. Then it is transferred into a furnace for wet oxidation and is treated there at $700°C$ for 5hr with water vapor. In this process, a 200nm thick SiO_2 layer is formed on the silicon surface. To clean the surface and to remove the water, the wafer is transferred to another furnace at $150°C$ for 10min and treated with HMDS*(Hexamethyldisilazane)* solution and then purged with nitrogen gas.

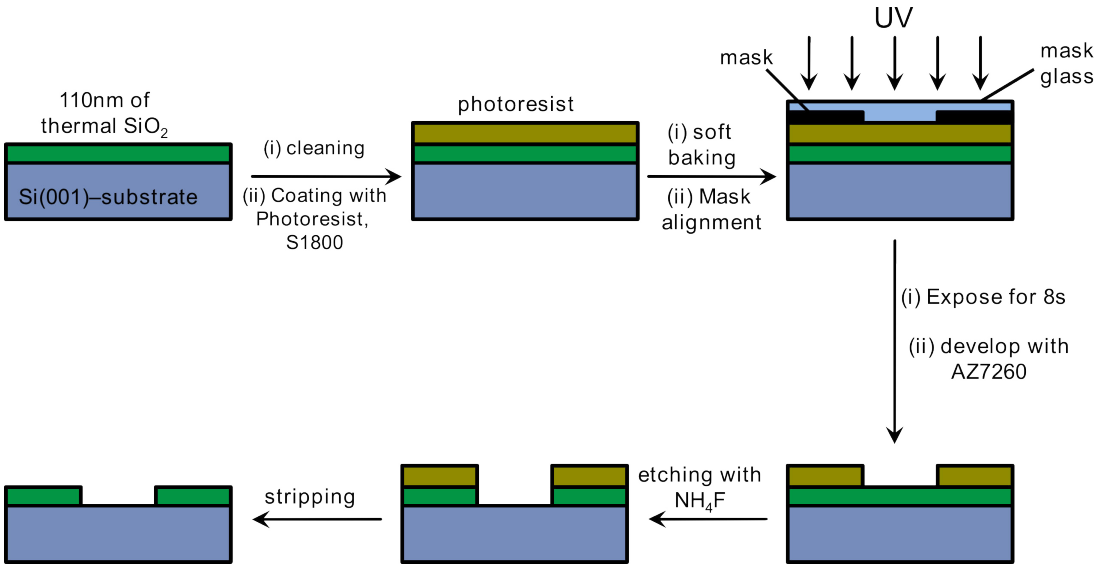


Figure 5.1 Steps of UV-Lithography on Si(001) wafer.

Then for structuring positive photo-resist (S1800) is spun onto the sample with a spinner (4000 U / min for 1 min), after that the wafer is heated for 1min on a hot plate at $110°C$. It follows the alignment of the lithography mask to the wafer and the photo-resist is exposed for 8s through this mask. Later with a developer (AZ7260), the exposed areas of the photo-resist are removed within 60s. The actual structure is then etched into the SiO_2 layer with ammonium fluoride all the way down to the unoxidized Si. Here, the tilt angle of the SiO_2 sidewalls is approximately 60° relative to the Si surface (Figure-5.2), which is verified by confocal microscopy and scanning electron microscopy (SEM). This angle is highly dependent on temperature, the concentration of the ammonium fluoride and etching time.

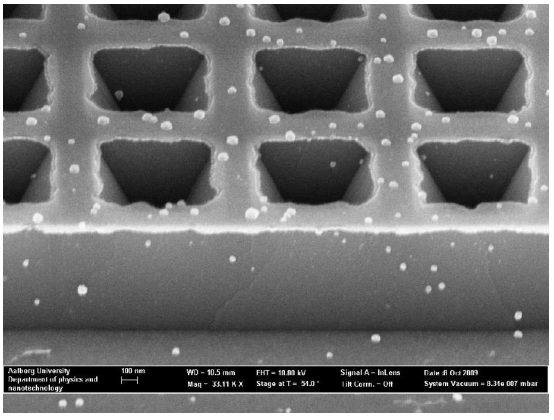


Figure 5.2 - Etched silicon dioxide (SiO_2) structure [44].

For electrical measurements, it is important that the back of the sample forms an ohmic contact with the stainless steel of the measuring apparatus. For this, the backside of the wafer is highly doped with an implanter. For n-Si Indium was used as back contact and

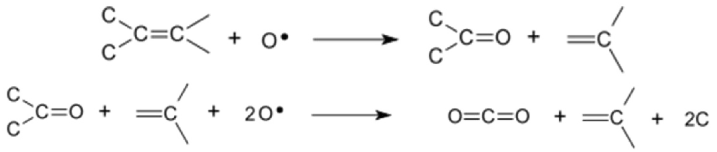
for p-Si, metal Tantalum (Ta) and Tantalum nitride (TaN) sputtered and back spattered subsequently with the help of argon gas for 5 hours at 40keV in an oven, during this process spattered atoms are reached at 1000°C. After this process the doping concentration at the back is $5 \times 10^{15} cm^{-3}$, according to machine manual. Both for n- and p-type Si samples, the ohmic behavior for the backside contact was confirmed by test measurements. Before implantation and the sputtering process, the front sides of the samples are covered by photo-resist to protect it from contamination. Then the samples are cut to an appropriate size of $15mm \times 10mm$.

5.2.2 Wet chemical cleaning of structured samples

To use the structured sample first we have to remove the photo-resist by a photo-resist remover (Microposit Remover 1165), which we applied to protect the structured area of silicon substrate. To clean photo-resist residue and other organic carbon contamination from the silicon wafer, we used piranha solution, which is a 4:1:4 mixture of 96% sulfuric acid (H_2SO_4) with 35% hydrogen peroxide(H_2O_2) and deionized (DI) water [45]. Piranha solution removes most of the organic matters. It will also make the surface highly hydrophilic (water compatible). The dissociated ions of piranha solution are shown as follows:

$$H_2SO_4 + H_2O_2 \rightarrow H_3O^+ + HSO_4^- + O$$

An example of the reaction mechanism of piranha solution with carbon residues:



The RCA/SC-1 cleaning step is performed to remove organic and ionic (metallic) contaminants with a 30% ammonium hydroxide, deionized water and 35% hydrogen peroxide ($NH_4OH : DI - H_2O : H_2O_2$) solution of ratio 5:1:1. In the process, it oxidizes the silicon and leaves a thin oxide on the surface of the wafer. So if there is any metal contamination within the top most layers of the wafer it will be oxidized and will come within the oxidized region and a subsequent HF dip will do the rest.

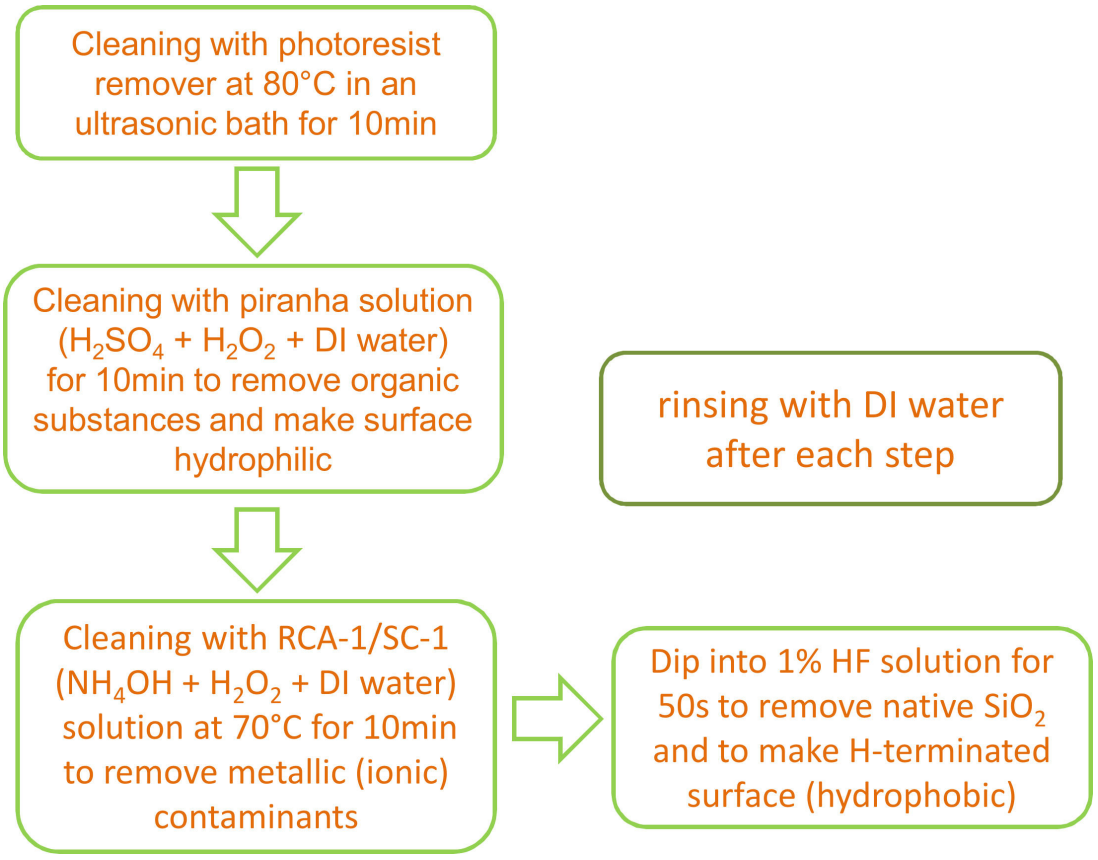


Figure 5.3 Cleaning steps of the structured Si(001) sample.

To remove silicon dioxide (SiO_2) from the surface of the wafer we dipped our wafer into 1% hydrofluoric (HF) acid solution for 50sec. The reaction mechanism of HF with SiO_2 is shown as follows:

$$SiO_2 + 4HF \rightarrow SiF_4(g) + 2H_2O$$
$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$$

Hydrofluoric acid attacks the silicon dioxide to form gaseous or water-soluble silicon fluorides [46] and leaves a hydrogen terminated hydrophobic silicon surface. Within few minutes after the HF dip we installed our sample into the UHV chamber. The sample is mounted inside the clean room on the BN heater (see Fig.4.4). In this way we have reduced the proportion of carbon residues to a minimum (just above the detection limit of XPS of about 1%) amount. A tungsten (W) mask with square openings of different sizes (see Figure 4.5) is adjusted onto the windows in the sample. For transport, the sample was put onto the manipulator, which in turn was mounted onto the pre-load lock system. Closing the gate valve, the sample could not get into contact with dust from outside the clean room. After mounting it with the UHV chamber it takes typically 15min to

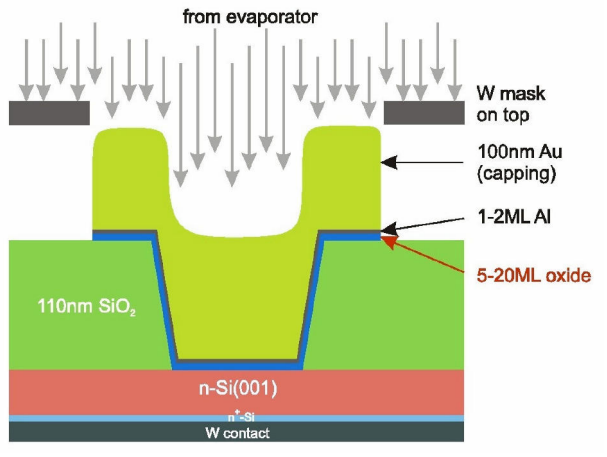
complete the evacuation. During this time, the hydrogen termination should mostly (80% - 90% coverage) sustain and only a very low coverage of substoichiometric SiO_{2-x} will form [35]

5.2.3 Further cleaning and film deposition in UHV

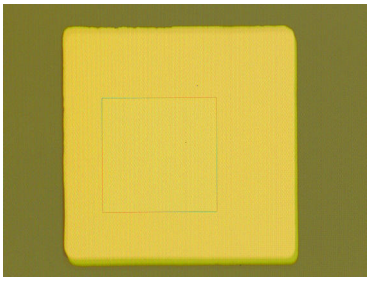
To remove the substoichiometric residual oxide and hydrogen-termination from the sample surface we need to flash the sample at high temperature. A major difference of the preparation of unstructured samples is in the thermal cleaning process. A chemical surface analysis (XPS) from unstructured samples with the same pretreatment shows that the temperature of 850°C is sufficient to remove the H termination, as well as existing SiO_{2-x} residues.

The BN sample holder in section-4.3, made this temperature treatment possible despite the W mask on the sample.

In the UHV chamber, the oxide layers are grown on the structured samples. The actual growth process of Ba/Sr oxides does not differ from the unstructured samples as described in chapter-6. Because of the tungsten mask, it is not possible here to check the quality of the layers with LEED, XPS or EELS. For this reason, unstructured samples as on the BN heater are produced with the same parameters and their chemical and structural properties have been checked. If one follows the same preparation steps in the structured samples, it can be assumed that the same high quality film is achieved. The finished MOS structure is shown in Fig.5.4 with n/p-Si substrate.



(a) Side view of the field



(b) Top view of the field

Figure 5.4 - (a) Finished MOS structure after deposition. The arrows from above indicate the evaporation direction through the W mask. The individual layers are not drawn to scale. Here only the stacking sequences of the final MOS diode are presented. (b) top view of the sample after preparation.

For the electrical measurements the sample has to be taken out from the UHV chamber.

In order to avoid chemical reaction with the water contents of the ambient air, the oxide film has to be protected with a metal layer. After the growth of oxide, a gold layer of 150-200nm thick is evaporated on the sample from an electron beam evaporator inside the main lock of UHV system. This layer also serves as a gate electrode for the MOS structure. Experience has shown that Au is not wetting the oxide and therefore the protective layer degrades easily. In order to improve the adhesion, a 1ML of Al is evaporated as an intermediate layer after the growth of oxide. The adhesion could be significantly improved by this growth step.

6 Growth of oxide and silicate on Si(001) substrate

The important steps of substrate structuring and the growth of silicates, like Ba_2SiO_4, $(Ba_{0.8}Sr_{0.2})_2SiO_4$ and oxides will be discussed in this chapter.

6.1 Optimization and deposition of dielectrics

Initially we worked with the oxide, formed from alkaline earth metals namely Strontium and Barium, deposited on Si(001). All experiments described here are carried out in UHV without exposing the samples to air except for the stability test of the sample. Pressure of the chamber is measured using a well degassed extractor gauge. Oxide layers are prepared either at room temperature or at higher temperature. The crystalline quality, stoichiometry and bandgap are checked on unstructured samples using SPA-LEED, XPS, and EELS, respectively. The deposition is done by e-beam evaporation. The deposition rate and the layer thickness is monitored by a quartz micro-balance (6MHz). By controlling the filament current and the emission current one can control the heating power and the ion flux out of the crucible. Usually it takes several minutes to achieve a constant emission setup of the evaporator electronics and the emission rate is controlled with the help of a quartz crystal micro-balance. Molecular oxygen of purity 99.998% is injected into the chamber for oxidation by back-filling it up to our desired pressure. Care is taken to avoid any direct gas flow from the gas inlet to the sample. To grow crystalline BaSrO we initially deposited a Sr mono-layer at the interface in order to prevent oxidation of Si. A careful adjustment of fluxes and the oxygen pressure is required too, as described in detail in [37].

The metals are evaporated from the electron beam evaporators (see chap.4.2). All of our evaporators except Au evaporator, are aligned to the center of the chamber, where the sample is positioned for the vapor deposition. The deposition rate of materials on the sample surface is measured with the help of a quartz crystal microbalance. The quartz micro-balance is cooled by water all the time to minimize drift during evaporation, which might influence the frequency rate of microbalance and hence our measured data. During deposition, quartz micro-balance is positioned just below the sample, so the rate of deposition measured by microbalance is not the same as on the sample surface (usually 15-20%). To solve this problem, initially we measured the deposition rate at sample position and later at balance position and calculated the geometrical factor, before starting the actual deposition. The actual deposition rate measured in real time at the sample is corrected from the rate of the quartz by using the geometric factor. Using a Labview program the rate is monitored. During the evaporation this program can display simultaneously the layer thickness in ML and nm and the rates over time graphically to observe the progress of deposition. With this program, the entire deposition process is monitored.

A thin metallic wetting layer is necessary to grow crystalline $Ba_{0.7}Sr_{0.3}O$ on Si(001). It is possible to use either Sr or Ba of thickness 1-1.2 ML as intermediate layer. Deposition of this layer is done at about 650°C. Further information of this intermediate layers and

about the possible outcomes are discussed in detail in [36, 37]. The film $Ba_{0.7}Sr_{0.3}O$ is grown at room temperature, after the deposition of the metallic interlayer. Adjusting the correct ratio of BaO (a_{BaO} = 5.54 Å) and SrO (a_{SrO} = 5.16 Å) is very important here. Because the lattice-matched growth reduces the interface stresses, so crystalline growth is favored. At a ratio of 70% BaO and 30% SrO the average lattice constant corresponds pretty much to that of the Si(001) surface ($a_{Si(001)}$ = 5.43 Å) as: $0.7 \cdot (5.54\ \text{Å}) + 0.3 \cdot (5.16\ \text{Å}) = 5.426$ Å.

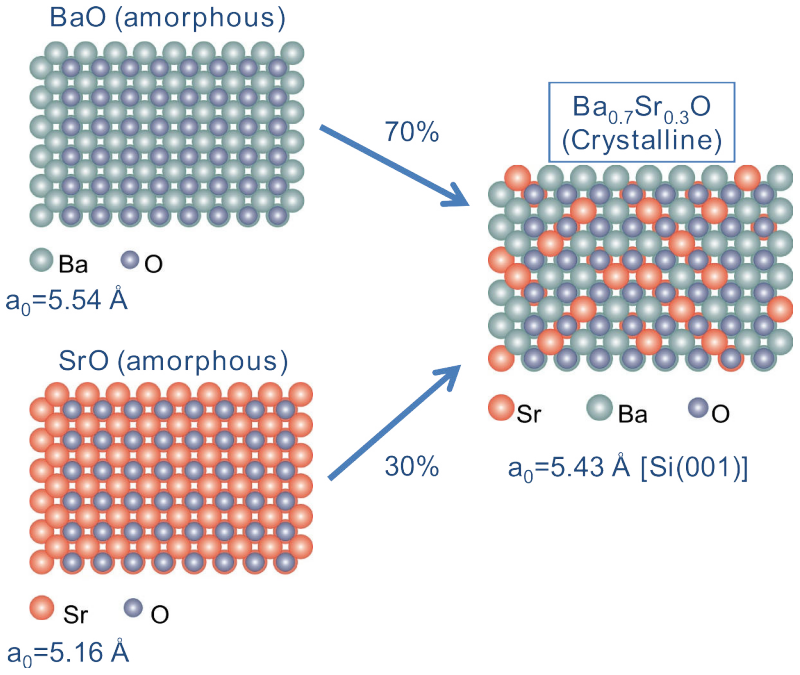


Figure 6.1 Crystalline barium-strontium mixed oxide ($Ba_{0.7}Sr_{0.3}O$) formed from amorphous barium oxide (BaO) and strontium oxide (SrO) [37].

The mass ratio of Ba and Sr can be calculated quite easily from the atomic ratio of 70%:30% by the atomic masses of the metals as: $(0.7 \times m_{mol,Ba})/(0.3 \times m_{mol,Sr}) = (0.7 \times 137.3g)/(0.3 \times 87.6g) = 3.66$. The ratio of the rates of two metals must therefore be 3.66. The quartz crystal microbalance measures the mass ratio of two evaporated materials. Just before starting the deposition process, we adjusted the ratio of Ba and Sr to make sure that we are growing the film of our desired stoichiometry. The flow of evaporation rates are regulated by adjusting the filament current manually to the desired ratio, by checking the evaporation rate separately from both of the evaporators on the microbalance. During this rate adjustment time the sample is protected from deposition by turning it to another direction. Before opening the shutter of the evaporators we turn on the oxygen flow with an oxygen(O_2) background pressure of 3×10^{-7}mbar and later metals are deposited simultaneously to grow $Ba_{0.7}Sr_{0.3}O$ film. The oxygen pressure is determined as an optimal pressure in [36], because at this pressure the film is grown with perfect match to Si. The oxygen is introduced through a fine precision valve into the main

chamber and can be set exactly in the pressure range up to $\pm 0.2 \times 10^{-7}$ mbar.

6.2 High temperature instability of BaSrO and silicate formation

In order to test the temperature stability of our MOS diode, we performed temperature dependent stability experiments both on thin and thick $Sr_{0.3}Ba_{0.7}O$ films using XPS, SPA-LEED and EELS measurements. We used both structured and unstructured Si(001) substrates in our experiments. We have grown a high-k oxide film at room temperature (RT) and observed LEED pattern, which confirmed crystalline growth of the oxide. In case of thin film we grew both 2ML and 3ML film on a Si(001) substrate. Afterwards we annealed the oxide at different higher temperatures for ten minutes and took XPS and EELS measurements at room temperature. We repeated these steps up to the temperature of desorption of the oxide films. While testing the thermal stability of crystalline BaSrO, we ended up in a new phase of amorphous silicate, which showed a certain stoichiometry both for thin and thick layers according to XPS measurements.

The heating intervals happened in steps of 20 or 50°C. Each of these temperature steps including the corresponding XPS, EELS and SPA-LEED measurements took approximately two hours. Because of the long duration of measurement we did not use all three methods on a single sample. Sometimes we performed XPS measurements along with EELS or sometimes XPS with SPA-LEED.

Here we compare the results of thermal stability obtained on an initially very thin ($2-3$ ML thick) $Sr_{0.3}Ba_{0.7}O$ layer with those of a 55 ML thick layer. This choice of thicknesses allows both to monitor modifications at the interface during thermal treatments, which is still visible in XPS of 3ML oxide. In order to study the properties of bulk oxide material, the 55 ML oxide layers are investigated, for the interface properties are not visible any more, with LEED and XPS. The major chemical changes appear at the Si 2p and O 1s peaks. From the analysis of the spectra we can see, with the increase of temperature the oxide ($E_B = 529.6$ eV) converts into silicate ($E_B = 531.6$ eV) and the corresponding chemical changes are identifiable clearly from the XPS spectra (figure-6.2).

Even after extended annealing up to $400°C$ the layers turn out to be stable, whereas at higher annealing temperatures a transformation sets in, which is obvious from the appearance of a new $O1s$ peak at 531.6 eV. This transformation is complete after annealing this layer at $580°C$. Further annealing steps up to $800°C$ showed that the layer remains unchanged up to annealing temperatures of $720°C$.

The XPS results for the as-grown samples and after those annealing steps, which shows clearly visible changes in the spectra, are shown for the O1s emission in figure-6.2 and for the Si2p emission in figure-6.3. The O1s peak from the 3ML oxide (see figure 6.2(a)) after growth at room temperature shows the well-known three peaks structure. The dominant peak at 529.6 eV binding energy is due to the bulk oxide, as seen by comparison with the thick oxide figure 6.2(b)). The other two peaks at binding energies of 531.2 and 532.9 eV are characteristic of interface formation with the Si surface, and have been attributed to

mixed Si-O-Sr(Ba) and Si-O bonds [37] respectively. Thus, SiO_2 formation is completely avoided under the chosen growth conditions, which becomes even more obvious as can be seen from Si2p spectra (see below) [38].

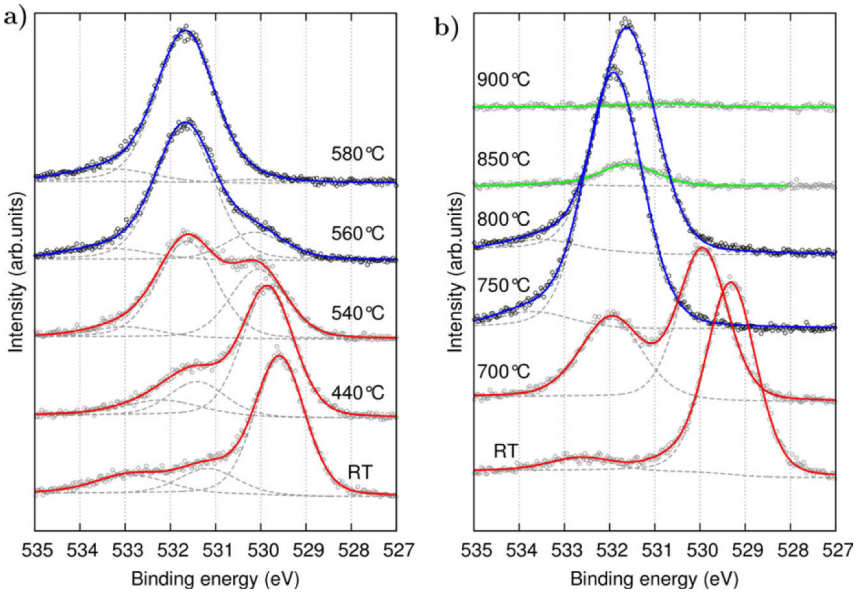


Figure 6.2- $O1s$ sample XPS spectra of an initially 3 ML thick $Sr_{0.3}Ba_{0.7}O$ film (a) and of an initially 55 ML thick $Sr_{0.3}Ba_{0.7}O$ film (b). Temperatures indicate annealing temperatures. Measurements are taken close to room temperature. The transformation from the oxide (E_B = 529.6 eV) to the silicate (E_B = 531.6 eV) is completed for 3 ML after annealing at 580°C, and for the thicker oxide at an annealing temperature of 750°C [38].

The same transformation is observed for the thick oxide films, but the transformation becomes visible only at higher annealing temperatures, see figure 6.2(b), and the new peak is shifted to 532.0 eV. The higher annealing temperature required here is due to a kinetic effect, which is obvious from the observations of Si2p emission (see below), since this transformation requires diffusion of Si from the Si bulk through the oxide layer in order to become visible with XPS. Therefore, this transformation is found to be completed only close to 750°C for the thick oxide layer. At higher annealing temperatures, desorption of the transformed layer becomes obvious even for the thick layers. For the thin layer, desorption is visible already between 720 and 740°C. The thick layer is completely removed after annealing at 900°C. The small differences in annealing temperature, where we see the same behavior, are most likely caused by the higher sensitivity of the thin layer. Since stability of thin and thick layers are very comparable, this can be taken as an indication for complete wetting also of the transformed layers.

More details of this transformation are seen from the Si 2p peak. After formation of the 3 ML thick oxide, the spectrum is dominated by the Si bulk peak at 99.9 eV, which appears together with a shoulder at 101.4 eV, characteristic for the bonds between Si and the oxide layer [37].

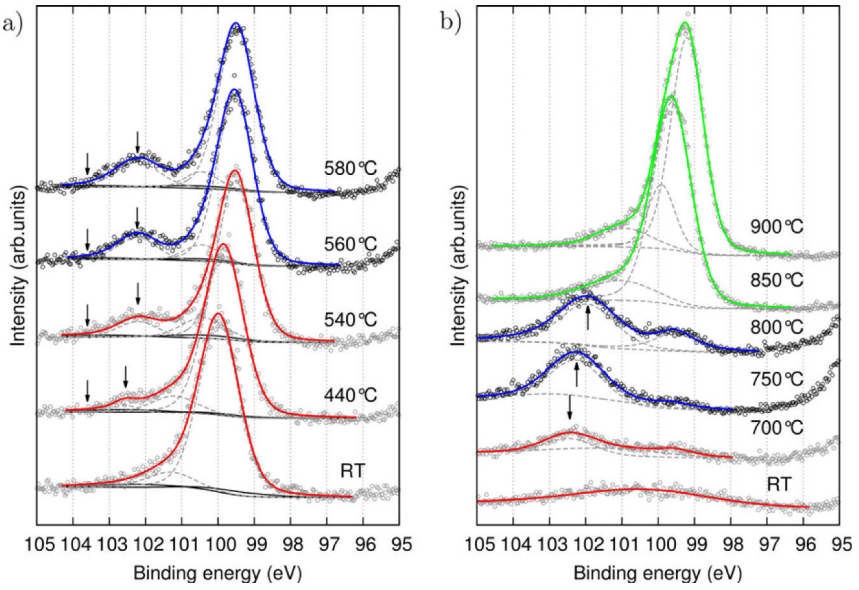


Figure 6.3- Si 2p sample spectra, similar to figure 6.2 for an initial oxide thickness of 3ML (a) and of 55ML after annealing to the temperatures indicated. The evolution of the silicate peak at 102.2 eV can be clearly seen. The shift of the initial bulk Si peak from 99.9 to 99.5 eV in (a) is attributed to band bending, whereas the further shift in (b) after desorption of most of the silicate at annealing temperatures between 850 and 900°C is indicative of the formation of Ba silicide [38].

As mentioned, no traces of a SiO_2 peak, expected at 103.3 eV [10], are visible. Its position is indicated by the left arrow in figure 6.3(a). Even after extended annealing up to desorption temperatures of the film, no intensity is ever detected at this binding energy; i.e, formation of SiO_2 can be excluded under all conditions from these mixed oxide layers.

Heating to 440°C for 5 min results in the appearance of a new peak, first at 102.6 eV, which shifts with growing intensity to 102.2 eV. This peak in photo-emission coincides very well with that found during oxidation of Sr on Si(001) at 500°C [39], which is ascribed to the formation of a silicate. Similar experiments with Ba evaporation in an oxygen atmosphere at these temperatures resulted in Ba_2SiO_4 formation [40]. Therefore, this XPS result shows, in agreement with those just mentioned, that at elevated temperatures around or above 500°C, silicate formation takes place. This process occurs by diffusion of Si atoms at the interface and its further propagation or diffusion into the oxide. That's why we can see a layer thickness dependence of the conversion, which we checked at the different conversion temperatures and also on various insulator film thicknesses. The shift of the silicate peak from 102.6 to 102.2 eV corresponds to the shift of the bulk Si peak from 99.9 to 99.5 eV, and may, therefore, be caused by band bending during the transformation.

6.2.1 Stoichiometry of newly formed silicate

We first determined the relative composition of thick silicate layers using the relative intensities, as shown in figure-6.4, at the completion of silicate transformation between 750° and 800°C together with our measured XPS photoemission intensities of Ba, Sr, O and Si for the thick $Sr_{0.3}Ba_{0.7}O$ layer and for the clean Si(100) surface, respectively, for which absolute densities of these elements are known. Here we have to assume a homogeneous concentration of silicate throughout the silicate layer. Within an error limit of 10% we obtained ratios (Ba+Sr):O of 0.5, (Ba+Sr):Si slightly below 2, and Ba:Sr = 4. These values are compatible with the stoichiometry of $(Ba_{0.8}Sr_{0.2})_2SiO_4$.

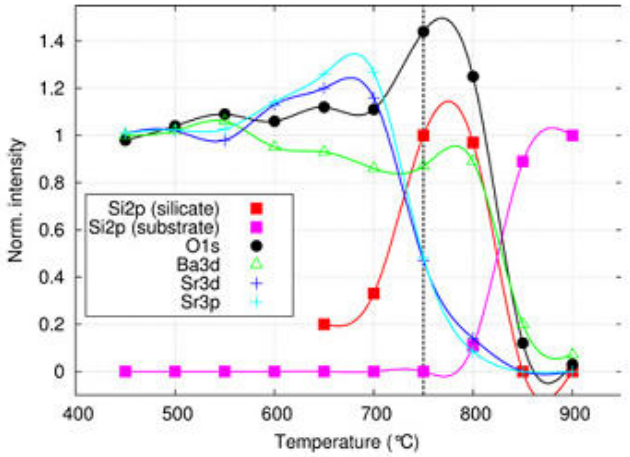


Figure 6.4 - Peak intensities as a function of annealing temperature for 55ML $Sr_{0.3}Ba_{0.7}O$. Peaks are normalized to the value at the lowest annealing temperature for Ba, Sr and O. In contrast, the Si peaks are set to unity at their highest intensities [38].

This stoichiometry is further corroborated by a comparison with crystallographic data [47, 48] for this compound. From these data, e.g., an absolute density of oxygen in the mixed BaSr silicate of $3.70 \times 10^{22} cm^3$ can be determined, which exactly corresponds to the observed 50% increase of O1s signal in XPS relative to the $Sr_{0.3}Ba_{0.7}O$ layer observed by us (see figure 6.4). Therefore, this measured increase of oxygen density is not an artifact, but means that the effective layer thickness must shrink accordingly during the transformation to silicate. The thermal treatment, on the other hand, leads to preferential desorption of Sr so that the original metal composition is changed and the Sr content is reduced. Further description about this silicate can be found at [38].

6.3 Formation and spectroscopic observation of Ba_2SiO_4

We investigated the barium silicate (Ba_2SiO_4) formation both on structured and unstructured samples. The substrate structuring, cleaning and deposition conditions are similar to $Sr_{0.3}Ba_{0.7}O$, as described above (section 5).

After wet chemical cleaning of unstructured sample, we installed it inside UHV and degassed the sample at the temperature of 550°C overnight (12 hr). After that we cooled the sample with liquid nitrogen for 1.5 hours and subsequently started the flashing process of the sample at about 1060°C to remove the hydrogen termination, native oxides and

carbon contaminants. Next we observed the sample surface with XPS to confirm that the carbon and oxide compounds are completely removed from the sample surface. To check the crystallinity we used SPA-LEED and have seen (2×1) reconstruction of Si(001) surface.

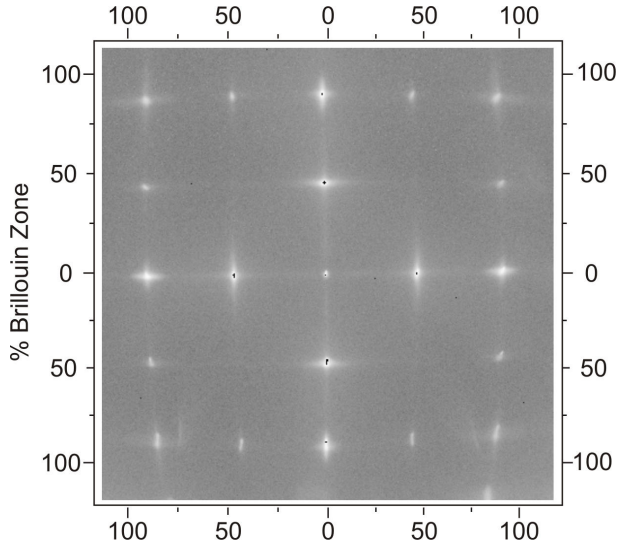


Figure 6.5 - SPA-LEED image of (2×1) reconstructed Si(001) surface.

At this stage, we rotated the sample manipulator and kept it away from the evaporators to protect the sample from any unexpected evaporation on it. We turned on the evaporation on quartz microbalance to determine a deposition rate of barium and to adjust the geometrical factor. Once finished, we rotated the sample to the position of evaporation, keeping the shutters of the evaporators closed. The actual layer deposition process can now begin.

After the deposition was done, we observed the sample by XPS, all the characteristic peaks were present and by SPA-LEED we observed no crystalline structure, means the grown oxide was amorphous. Afterwards we started heating the sample to temperatures between 650°-700°C for 45min and turned off the heating. Once the sample reached room temperature we investigated the sample surface with SPA-LEED again and saw a crystalline structure of Ba_2SiO_4 (see below for details). The formation mechanism of this silicate is similar to $(Ba_{0.8}Sr_{0.2})_2SiO_4$ as discussed above, here also silicon diffused from the substrate into the oxide and formed barium silicate. At this stage the process of sample preparation is completed and the quality of the sample is checked by XPS, EELS and SPA-LEED *in-situ*.

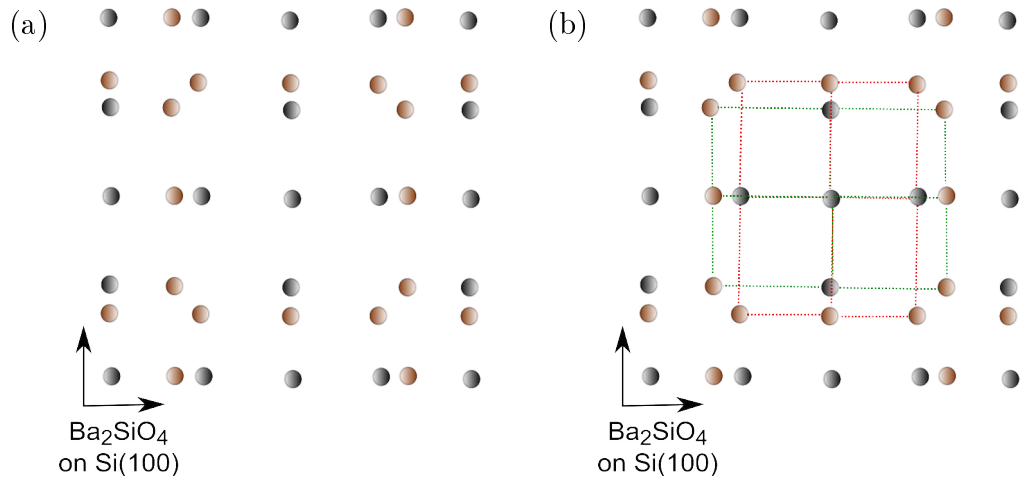


Figure 6.6 - (a) Schematic representation of interfacial atoms of barium silicate on reconstructed Si(001) surface. (b) two favorable domain orientations of barium silicate.

A well transformed Ba_2SiO_4 sample is crystalline on the silicon surface, as we have seen from SPA-LEED measurements. It forms an orthorhombic crystalline structure at the (2×1) reconstructed Si surface as shown in figure-6.6. In this figure the gray dots represent the diffraction spots from silicon atoms and orange dots are from Ba_2SiO_4. In second image we can see two possible domains of silicate on silicon surface, which are perpendicular to each other. By comparing the SPA-LEED image of Barium Silicate and reconstructed Si(001) surface, we determined the lattice constant of Ba_2SiO_4.

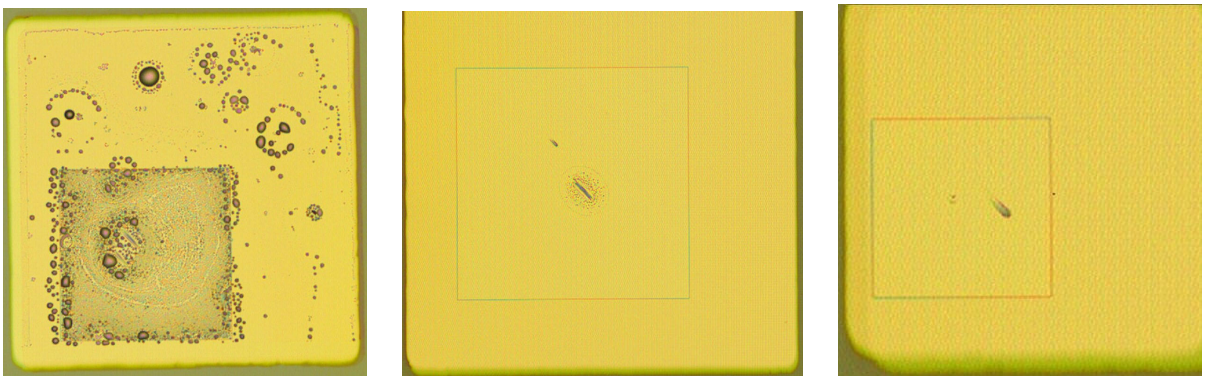
To observe the chemical composition of the newly transformed bulk silicate we took XPS measurements. We used XPS to observe the expected peak positions of barium, oxygen and silicon atoms in the overview spectrum. In case of thin layers ($< 20ML$), the Si peaks from the interface are also visible. Detailed description of this XPS spectrum are discussed in last chapter below. There should not be any other peaks like C1s, which would indicate the presence of dirt or impurity caused by insufficient good pressure in the chamber. Bad pressure can arise due to insufficient degassing of the evaporators or due to leak in the UHV chamber.

6.4 Protecting dielectrics from ambient atmosphere

After removal of the finished structured sample from the UHV, there have always been problems regarding the stability of the films. The $Ba_{0.7}Sr_{0.3}O$ films are more hygroscopic and highly reactive in contact with water compared to Ba_2SiO_4.

For protection, therefore, for protection the samples are covered with a Au layer before being taken out of the UHV. However, the protection of the films was not possible in many cases of $Ba_{0.7}Sr_{0.3}O$, or was only possible for a very short time (1min. to a few hours). Visually, the instability of the MOS diode is seen from the violent exothermic explosive reaction through the Au film, as it is clearly seen in Fig.6.7(a), which might be

due to the penetration of water through the Au layer and the subsequent reaction of the oxide to hydroxide.



(a) (b) (c)

Figure 6.7 - (a) Effect of dirt on substrate, (b) With thin gold layer and (c) with sufficiently thick gold layer.

One cause of instability is the poor adhesion of Au to oxide. Through the gap between dielectric and Au, water can reach to the oxide more easily. Due to low surface energy of oxides compared with Au, there would be weak binding between Au and the oxide. So the amount of 1ML Al is introduced at the interlayer, to improve the adhesion. The idea is that the Al on the oxide has a reducing effect, and thereby forms a bond. In addition, Au forms an alloy with Al, which connects the gate metal to oxide. In fact, a higher yield of stable MOS diodes could be achieved by the introduction this intermediate layer.

The lateral distribution of defects in Fig.6.7 (a) shows that although there are defects in the center area of the pads, the greatest concentration is found at the edge regions. One possible reason for the increased density of defects in the peripheral region, which has proven to be most likely, is a problem of contamination prior to installation of the sample into the UHV. During chemical cleaning by still not totally clean chemicals and beakers, impurities appear to remain on the surface, which accumulate in the edge regions. On the one hand, these impurities interfere with the growth of the oxide film, and on the other hand they make it difficult to get good adhesion and thus a closed film growth of the oxide/dielectric. The instability of the sample seems to be very random. Sometimes, most of the pads of the sample are stable and others are not, which is an indication that it is actually a matter of purity of the sample. Other effects, such as the inclination angle or the adhesion between Au/oxide, are of less or no importance.

In conclusion it can be stated that we have found the causes of the instability of the samples and those problems are mostly eliminated. The stability was significantly improved by various measures. The main improvement seems that we have taken special attention to a high cleanliness of chemicals and beakers in the cleaning steps prior to the installation of the sample in UHV, and the introduction of piranha and $RCA1$ cleaning

step (see section 5.2.2). XPS measurements on unstructured samples have shown that the carbon content was reduced almost to the limit of detection.

A properly clean sample with a thin gold layer on top, can be seen in fig. 6.7(b), the scratch is from the high voltage needle of current-voltage(I-V) measuring station and happened during electrical measurement. By close inspection one can see that the dielectric material starts to react with air through the scratch. This problem is solved by depositing a thick ($\sim$ 150nm) Au layer on top of the oxide fig. 6.7(c).

7 $Ba_{0.7}Sr_{0.3}O$ and Ba_2SiO_4 as alternate gate dielectric in MOS diodes

MOS test capacitors with high-k dielectrics can be fabricated on 4in. p-type Si(001) wafers. The wafer surface is covered with a thermally grown thick field oxide (SiO_2) of about 200nm, we have written the structure by optical lithography and have done subsequent wet chemical etching to obtain active windows with different areas. Ohmic back contact is produced by implantation of phosphorus, thermal annealing and sputtering of tantalum and tantalum nitrite.

The experiments took place in an ultrahigh vacuum (UHV) system as discussed in chapter-5 above. In this section the electrical measurements and obtained results are going to be discussed first.

We used electrical measurements (C-V and I-V) to know about the defects at bulk as well as at the dielectric-substrate interface. After appropriate corrections (3 element model and back contact resistance) of measured data (C-V and I-V), we have determined the different electrical properties like dielectric constant, interface trap densities (D_{it}), capacitance equivalent thickness (CET), etc.

7.1 Some properties of $Ba_{0.7}Sr_{0.3}O$

To use the ultra-thin, high-k oxide/dielectric in MOSFET technology, the electrical properties of these films are very important to know. First of all the theoretically expected value of high dielectric constant of this oxide/dielectric should be confirmed by CV measurements. In order to keep the power loss of such transistors at a lower level, high leakage currents through the dielectric should be avoided. To fulfill this requirement, the concentration of defect states at bulk dielectric and near the interfaces should be small enough to disfavor any kind of leakage tunneling current (i.e. hopping conduction) through the dielectric. Furthermore, the valence and conduction band in the region of the interface need to be adjusted so that the band offsets of the valence and conduction bands between the dielectric and substrate are larger than the technologically required minimum value of 1 eV [41]. If the band offsets are lower than 1eV, thermal excitation of the electrons or holes could directly occur from the semiconductor into the conduction or valence band of the dielectric and can cause high leakage current, in spite of the high quality of bulk oxide.

The electrical characterization of the ultra-thin $Ba_{0.7}Sr_{0.3}O$ and Ba_2SiO_4 films was performed in the MOS diode configuration of Si/dielectric/Au layer systems. The preparation of these films was already described in sections 5 and 6. The characterization is made essentially from the current-voltage (I-V) and capacitance-voltage (C-V) measurements. From these curves qualitative statements about the sample quality can be directly made. In this chapter the results and the further evaluations of the results are presented and discussed accordingly. Some results from this chapter have already been published in [38] and [42].

7.1.1 Quality of bulk dielectric

MOS diodes were fabricated here with $Ba_{0.7}Sr_{0.3}O$, thicknesses between 5nm and 16nm at room temperature without further annealing. To check the behavior of MOS diode and to know about the bulk defects of the oxide, we performed capacitance-voltage (C-V) measurements, by applying the negative gate voltage (V_G) up to constant accumulation and positive gate voltage up to the constant inversion of the MOS diode with a constant sweep rate of ± 0.2V/s. C-V curve shown in Fig. 7.1 was obtained by sweeping the voltage between inversion and accumulation regions at room temperature. A negative shift is visible both for C-V and G-V curves. The C-V hysteresis loop is measured counterclockwise. After obtaining the C-V measurement both for forward and reverse bias, we have measured the hysteresis of the diode at the middle of the C-V curve (figure-7.1).

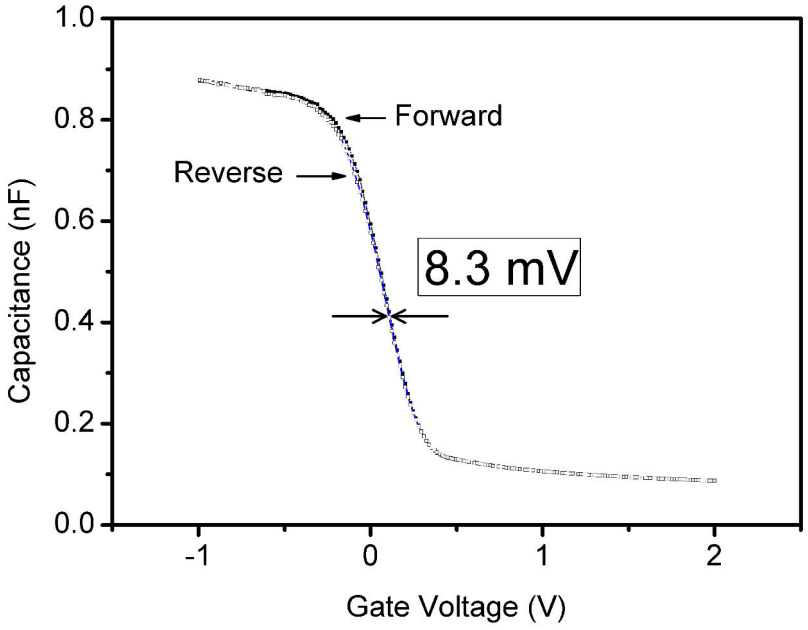


Figure 7.1- Hysteresis of 5nm $Ba_{0.7}Sr_{0.3}O$, from C-V measurement of $1.6 \times 10^{-3} cm^2$ MOS diode at 100kHz frequency.

The CV curves of MOS diode with 5nm BaSrO, show extremely small hysteresis, which in all cases is below 10mV, and sometimes barely detectable (fig.7.1). This demonstrates that the density of rechargeable traps (near interface) in the oxide is extremely low. This is a prerequisite for any high-k dielectric material for MOS diode application.

To get the quantitative value of leakage current through this diode we have done I-V measurements. The current density vs. voltage characteristics of MOS diode with 5nm BaSrO is shown in Fig. 7.2. The leakage currents is higher at negative gate voltages compared to positive gate voltage, which is the characteristics of MOS diode with p-type silicon substrate. At flat band voltage ($V_F = 0.094V$) if we apply negative bias voltage the MOS diode sets into forward bias condition and reaches at accumulation at around

$-0.64V$ gate voltage (fig. 7.1). Hence leakage current at negative bise is higher compared to positive bias voltage, which means that this is an effect of the Si substrate.

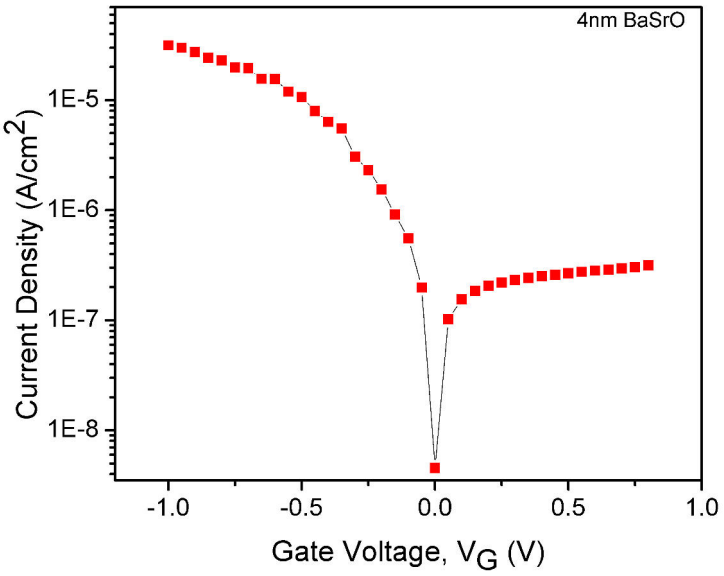


Figure 7.2 - Leakage current of 4nm BaSrO from the current-voltage (I-V) curve.

At positive bias the diode sets into reverse bias condition and reaches into inversion region. Due to that reason the leakage current is lower. Although there are considerable variations in the leakage current at the same oxide thickness, the lowest leakage current densities for the thinnest oxide (4nm) turned out to be 0.03 mA/cm^2 at $-1V$ above the flatband voltage in accumulation fig.7.2. The experimentally obtained leakage current values are by orders of magnitude lower than the leakage currents of SiO_2 and also in the range of leakage current densities of other high-k gate dielectric materials at corresponding CET values [65].

7.1.2 Capacitive equivalent thickness and dielectric constant of BaSrO

The Capacitance Equivalent Thickness (CET) is the thickness that a silicon dioxide film provides with the same capacitance as used high-k dielectric, which has higher physical thickness compared to SiO_2 in the MOS diode. It is possible to extract the dielectric constant value of dielectric film from the CET vs physical thickness plot of the dielectric film. We have used the following formula to calculate the CET from the measured value of capacitance.

$$CET = \frac{\epsilon_0 \cdot \epsilon_{SiO_2}}{C_{acc}}$$

Where ϵ_0 is the vacuum permittivity, ϵ_{SiO_2} is the dielectric constant of silicon dioxide and C_{acc} is the capacitance at accumulation.

We determined the active MOS diode capacitance in strong accumulation after correction for series resistance and parallel conductance with a frequency dependent 3-element

model and after subtraction of the gate metal/field oxide overlap capacitance for different window areas and several samples. The average values for each thickness are plotted as CET versus oxide thickness in Fig. 7.3 . Error bars are determined from the scatter of the data and correspond to the 3σ values of the average.

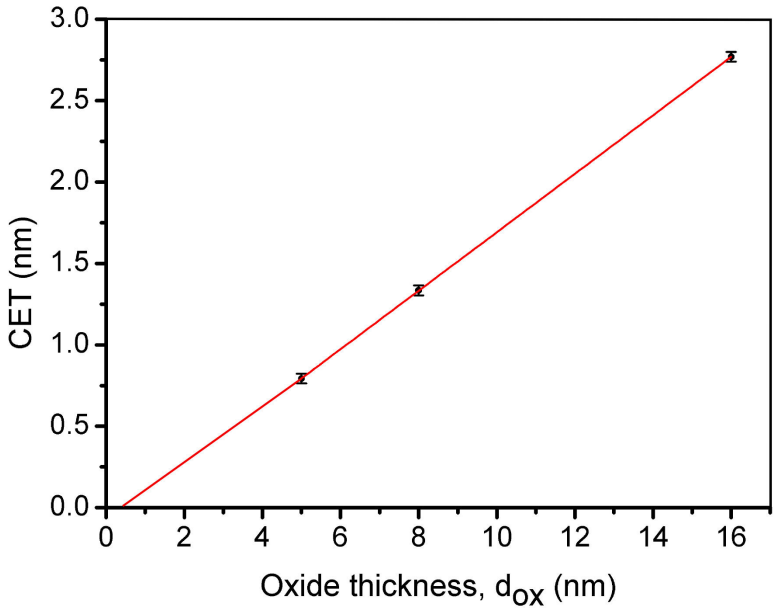


Figure 7.3 - Equivalent oxide thickness (CET) versus evaporated oxide thickness. From the slope of the straight line through the data $\epsilon = 21.8 \pm 0.2$ is deduced. The intersection of this line with the x-axis at 0.5 nm.

As seen, the data fall nicely on a straight line. The capacitance equivalent oxide thickness (CET) for the thinnest layer is about 0.75 nm (fig. 7.3) and fulfills well the critical limits of leakage currents for practical applications [43]. From the slope we determined the relative dielectric constant ϵ of the mixed crystalline oxide to be $\epsilon = 21.8 \pm 0.2$. Although within an expected range, this value is significantly lower than that obtained from linear interpolation of the bulk values ($\epsilon_{BaO} = 34$, $\epsilon_{SrO} = 14.5$) using the relative concentrations of Ba and Sr $(2:1)$ in the oxide. Since thinner layers than 5nm can easily be produced, it is obvious that CETs around 0.5nm are feasible.

Even more remarkable is the positive intercept of the straight line in this figure with the d_{ox}-axis at about +0.5nm oxide thickness. Within error bars, it is not possible to obtain a negative d_{ox} intercept, which would correspond to a positive CET-axis intercept expected for the finite semiconductor capacitance. Therefore, we tentatively explain this finding by the formation of an interface layer between silicon and oxide with a much higher dielectric constant than the bulk oxide. In fact, the intercept with the d_{ox}-axis at about +0.5nm yields the thickness of this interlayer for $\epsilon_{interlayer} \to \infty$, which is a lower boundary for its thickness at finite $\epsilon_{interlayer}$. This finding may be explained by the bonding configurations of metal and oxygen ions at the interface, in particular oxygen has to form bonds both to the Si and to the metal ions [61].

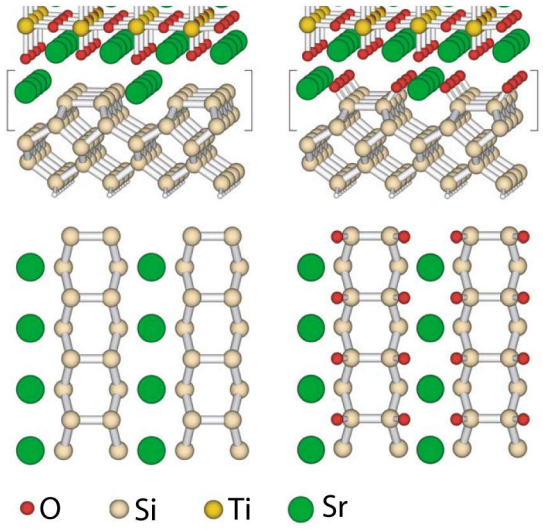


Figure 7.4- Oxide-substrate interface behavior [61].

A similar example of the above mentioned phenomenon can be seen at figure-7.4, where the strontium titanate deposited on top of silicon surface. The bulk oxide is homogenous and stable but at the interface the condition is different. At bulk an oxygen atom forms a stable bond with Ti atoms from the both sides but at the interface in one side it is connected with silicon atom and at the other side with strontium atom that makes an unstable interface, which can easily be influenced by the applied electric field. While applying electric field the electrons cloud at the interface will respond immediately and the resultant we are seeing at figure-7.3.

7.1.3 Temperature dependent leakage current of BaSrO film

Arrhenius plots of BaSrO MOS diode are seen in figure-7.5. Here the temperature dependent leakage current for the Au/Al/BaSrO/p-Si sample with 6nm thickness is plotted for $Ba_{0.7}Sr_{0.3}O$. In the 253-330 K temperature range the relationship between current density, J and inverse of temperature 1000/T is clearly linear. At higher temperature the thermally generated carriers increase and hence the leakage current. So lower voltage is sufficient to fill up all the trap levels at higher temperature. That's why we can see a converging tendency of all the lines at left side of figure-7.5 at high temperature. For forward bias, activation depends on applied voltage: as we are sampling different regions of the excitation spectrum but for reverse bias the applied electric field does not help to overcome activation barriers in the oxide (fig. 7.6).

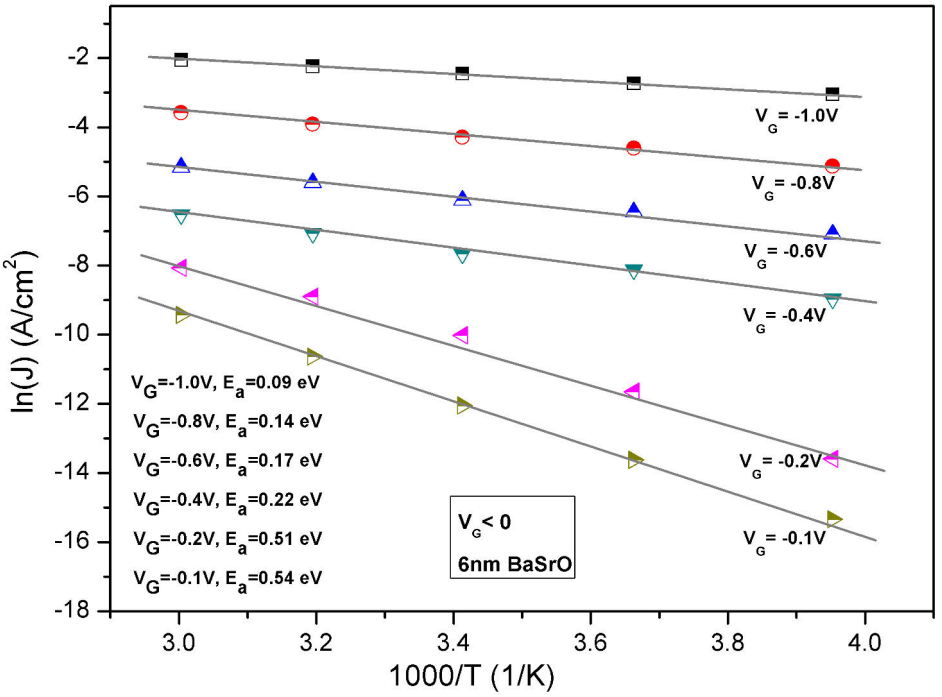


Figure 7.5- Temperature dependent leakage current in forward bias condition.

This kind of Arrhenius plot indicates a conduction mechanism controlled by Poole-Frenkel (PF) emission. The PF mechanism is bulk-limited and relies on the traps in the insulator. The PF is associated with the field-enhanced thermal excitation of charge carriers from traps. As is shown in the figure, the slopes of the lines do not vary appreciably with the applied voltage, indicating that the conduction takes place through an activated process having a single activation energy, E_a, which follows the relation

$$J = J_0 \cdot exp - (E_a/k_B T)$$

The activation energy values corresponding to each of the lines are shown in above plot. The activation energy values of the sample scatter between 0.09 and 0.54 eV, indicating that other different mechanisms of transmission take place as well, and so the combination of all of them are detected. The activation energy is obtained from the slope of the plot ln(J) vs. 1/T.

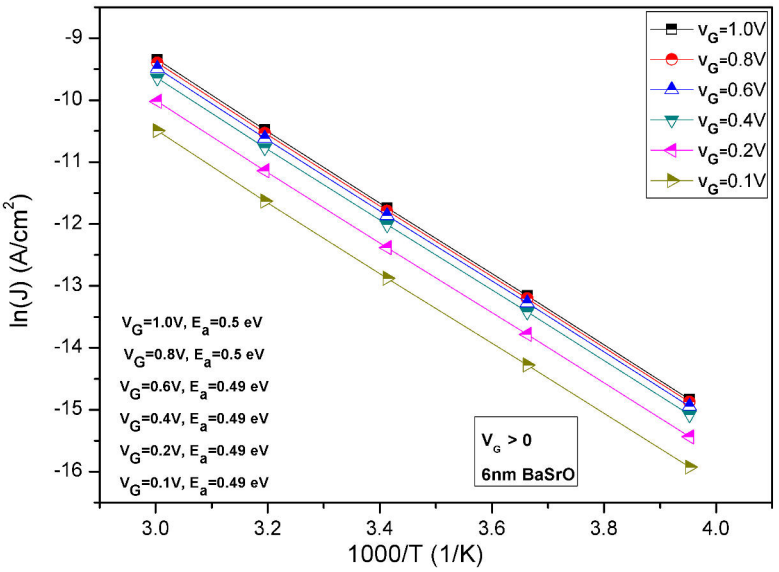


Figure 7.6- Temperature dependent leakage current in reverse bias condition.

In case of reverse bias condition, we only see scatter in temperature dependent leakage current plot. Here the situation has changed, thermally activated charges are accelerated once exited. Here in case of reverse bias the difference is that one cannot partially fill traps. Therefore, we get a unique answer from the experiment.

As discussed above, for electrical measurement purposes we need metallic back contact in our Si(001) substrate. Backside of the silicon wafer is spatter by tantalum and tantalum nitride respectively to make ohmic metallic back contact, figure 7.7(a). To confirm about the proper metalization of back contact of our silicon wafer we have measured the contact resistance first, the contact resistance is measured from I-V measurement.

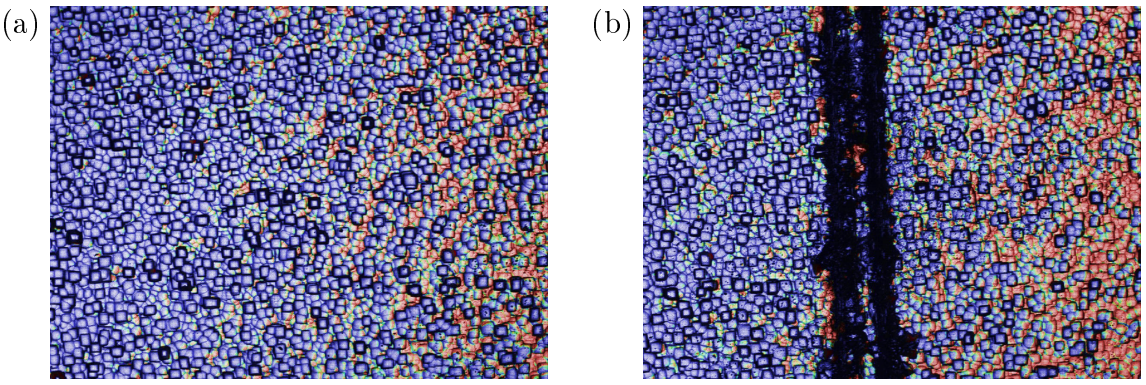


Figure 7.7- Metallic backside of silicon wafer (a) before scratching (b) after scratching.

After being satisfied about the contact resistance ($\sim 5-10 m\Omega \cdot cm$), we wanted to know the applied voltage range upto which the back contact shows metallic behavior. To do so

we made a scratch, shown in figure-7.7(b), at the back side of the wafer and removed the implanted metal completely. Next we placed two electrodes on two sides of the scratch and a voltage sweep has been applied. The current path from one electrode to the other has to cross the metal-silicon interface twice. We obtained the following IV-curve, shown in Fig-7.8.

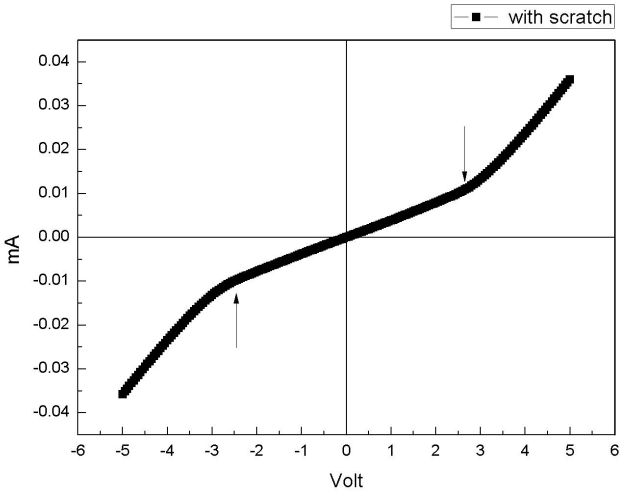


Figure 7.8 - Current-voltage (I-V) measurement at the back-side metal contact of silicon wafer to check the conduction properties of the back contact.

From this I-V plot we can see that the back metallic contact shows a straight line that means Ohmic behavior between the applied voltage range from +3V to −2.5V. But outside of this voltage range, the I-V curve shows Schottky behavior. Therefore, in order to ensure that there is no Schottky influence for back contact in our C-V and I-V measurements of MOS diode, we performed our electrical measurements within the Ohmic range of +3V to −2.5V.

Once we annealed our BaSrO on Si(001) substrate at temperatures around 650°C, the oxide transformed into barium-strontium silicate $[(Ba_{0.8}Sr_{0.2})_2SiO_4]$ as described in section-6.2. We have found that the silicate is crystalline but leakage currents are very high, as shown in figure-7.9.

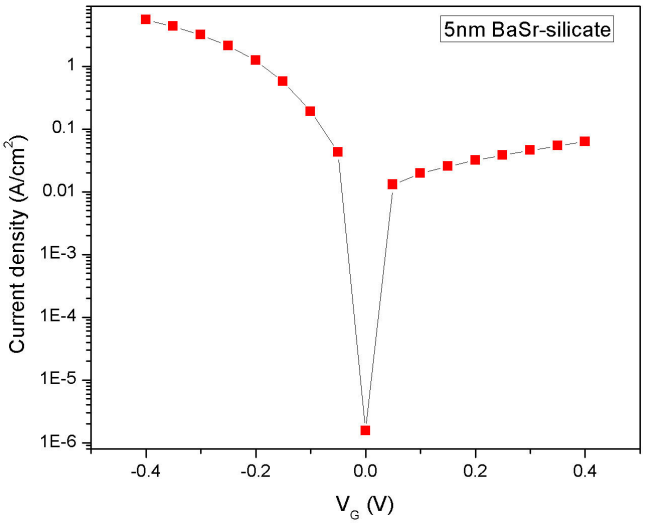


Figure 7.9- Leakage current of 5nm $(Ba_{0.8}Sr_{0.2})_2SiO_4$ from the Current-Voltage (I-V) curve.

To minimize the leakage current we have grown the silicate $[(Ba_{0.8}Sr_{0.2})_2SiO_4]$ at high temperature $(650°C)$ but no significant improvement regarding leakage current has been observed. To minimize the leakage current we decided to grow single metal silicate (Ba_2SiO_4) instead of double metal silicate $[(Ba_{0.8}Sr_{0.2})_2SiO_4]$.

At ambient atmosphere silicate absorbs crystal water [38] and the effect of that is seen in figure-7.10.

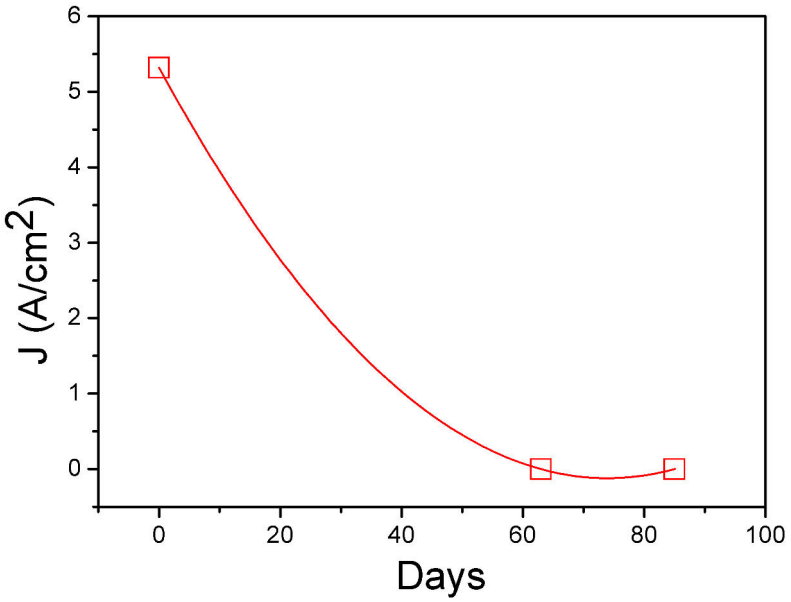


Figure 7.10- Change of leakage current through 6nm $(Ba_{0.8}Sr_{0.2})_2SiO_4$ with time from the Current-Voltage (I-V) measurements.

We observed the leakage current through a 6nm silicate sample stored in clean-room and in ambient atmosphere for 90 days. We can see the exponential decay of leakage current, which might be due to the absorption of crystal water. At the same time we measured the dielectric constant from C-V measurements. Concomitant with time the dielectric constant falls rapidly down to $\epsilon \approx 3.8$.

7.2 Growth and characterization of barium silicate

We have followed two different ways of barium silicate (Ba_2SiO_4) formation, similar to $(Ba_{0.8}Sr_{0.2})_2SiO_4$, first (I) Silicate formation by post annealing and second (II) Silicate formation during deposition.

(I) Silicate formation by post annealing: In this method we have deposited a certain known thickness of BaO at room temperature (RT) on top of Si(001) surface in UHV, which is amorphous oxide Figure-7.11(a). Later we heated the sample in-situ between $650° - 700°C$ for about 45 min Figure-7.11(b). During the time of heating, silicon from the substrate diffuses into the oxide and reacts with BaO and is transformed into Ba_2SiO_4 (figure-7.11(c)). Details of the diffusion mechanism and the similar kind of silicate formation can be found in [38].

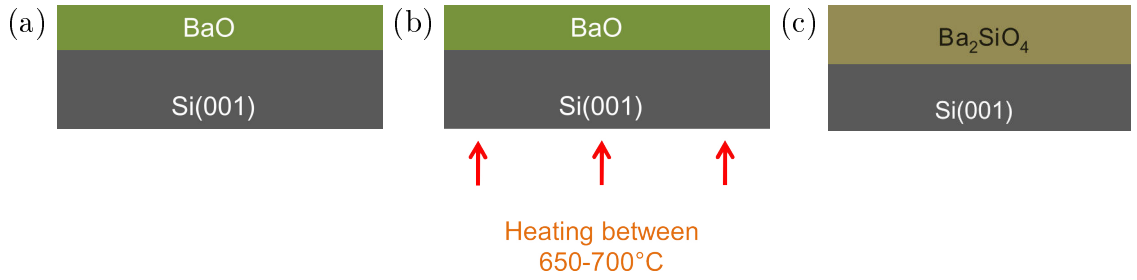


Figure 7.11- Silicate formation by post annealing (a) depositing a certain thickness of amorphous BaO at room temperature (b) heating the oxide between $650° - 700°C$ for 45 min (c) formation of Ba_2SiO_4

If the initial BaO thickness is less, like around 2nm, the transformed silicate is almost homogenous and fully crystalline, which we observed by XPS, SPA-LEED and TEM. But with the increase of oxide thickness the formed silicate become less homogenous and crystallinity is less observable. The reason is oxide thickness dependent self limiting diffusion of silicon through the oxide and the hence the partial formation of crystalline silicate and the presence of amorphous BaO at the top oxide surface.

(II) Silicate formation during deposition: Another method of silicate formation is depositing BaO at high temperature.

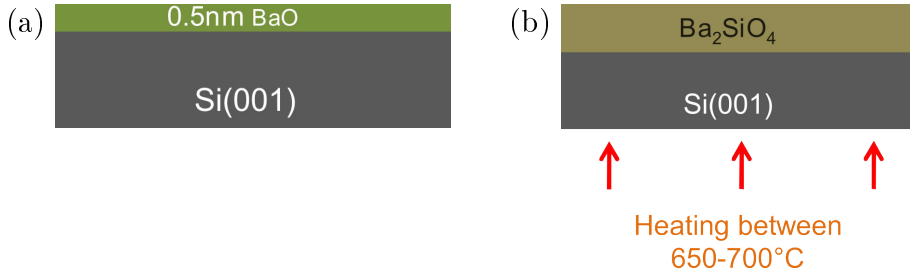


Figure 7.12 - Silicate formation during deposition (a) depositing 0.5nm of BaO at RT (b) formation of Ba_2SiO_4

In this method, at first we have deposited about 0.5nm of BaO [Fig.- 7.12(a)] at RT and then we turn on the heating at around 650°C and continue the deposition up to our desired thickness. After completing the deposition we keep heating the sample for another 45 min to ensure the maximum transformation of BaO in to Ba_2SiO_4. The advantage of heating the sample while depositing is, the silicon which is diffusing in to the oxide can get the necessary amount of metal barium and oxygen gas to transform into silicate. As a result the silicate film becomes more homogenous and more defect free. For the same amount of Ba deposited, the thickness of barium silicate is 25% higher than BaO. We checked the leakage current through both types of silicate and found that the first process has higher leakage current compared to the second one. The reason seems to be that the first process is forming more defects inside the silicate and also there might be micro cracks inside the silicate due to the way its formed. Comparing the two processes, we decide to follow the second one to form our desired silicate.

Secondary Ion Mass Spectrometry (SIMS) of Ba_2SiO_4

To observe the detailed stoichiometry of silicate, starting from the top of the layer up to the interface we have done secondary ion mass spectrometry (SIMS). It is a technique to analyze the material composition of thin films and solid surfaces by sputtering the surface of the sample with a focused ion (here O_2) beam and then collecting and analyzing the ejected secondary ions to get an idea about the depth profile of the sample. Usually SIMS is a qualitative technique to determine the mass/charge ratios of the sputtered ions by a mass spectrometer to find the elemental composition of the sample surface.

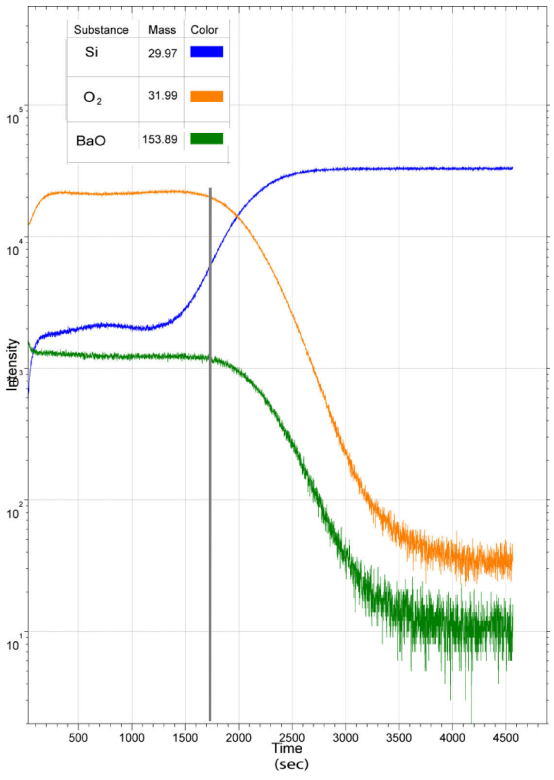


Figure 7.13 - Secondary Ion Mass Spectrometry (SIMS) of 12.5nm Barium-Silicate (Ba_2SiO_4)

The SIMS measurement of 12.5nm barium silicate is shown in figure-7.13 in intensity vs. time scale. Here three elements (i.e. Si, O, Ba) are represented in three different colors. It is more meaningful to consider the time axis as a silicate depth profile. Where the zero second represents the top surface of the silicate and around 1700 second (dark vertical line) is the interface of silicon and silicate layer. It took 28.3min to sputter 12.5nm silicate, means 0.44nm per min. One can see at this point both of the barium and oxygen intensities are sharply falling down and the intensity of silicon starts to increase very rapidly. During sputtering some silicate might went inside the substrate, due to that reason, low signals of Ba and O are visible just below the interface.

We can get an idea of silicon diffusion inside the oxide from these intensities. It is visible that the intensities of barium and oxygen remain constant from the interface up to near the top surface (200 sec) of the oxide, but the intensity of silicon is not as constant as that of other two, rather the intensity shows a gradient. It is also visible that in this 12.5nm silicate, silicon diffused more than three quarter (around 8nm or 500sec in above figure) of the oxide thickness and from the middle (850sec) of the silicate, silicon concentration is almost constant up to the interface, which indicates a homogenous growth of the silicate near the interface.

7.2.1 Spectroscopic (XPS) observation of barium silicate

To be sure about the chemical uniformity of silicate layer we measured and optimized the signal of O1s, B3d and Si2p using the XPS measurements. The obtained spectra of Ba_2SiO_4 layers are compared later on with those obtained earlier [38].

The sample spectra of Si2p, O1s, Ba3d and Ba4d signals are shown in Fig. 7.14 and Fig. 7.15. By comparing the spectrum of clean Si(001), the peak appearing at a binding energy of 101.6 eV is attributed to the formation of the silicate (fig. 7.14(a)). Due to the increase of silicate thickness the Si peak at 99.2 eV of the underlying Si sample is damped accordingly. The spectrum obtained with 3ML BaO shows not only the damped contribution of the Si substrate, it contains also a contribution of Si-O formation at the interface that has been analyzed in detail previously [37]. After transformation into silicate upon annealing at 650°C the same peaks are observed as those obtained for silicate formed at 650°C.

We also note that no silicon dioxide is formed. This is to be expected since even the reaction of BaO and SiO_2 is exothermic, as calculated from the respective enthalpies of formation [66]. Enthalpy of Me_2SiO_4 is between -210 to -220 KJ/mole.

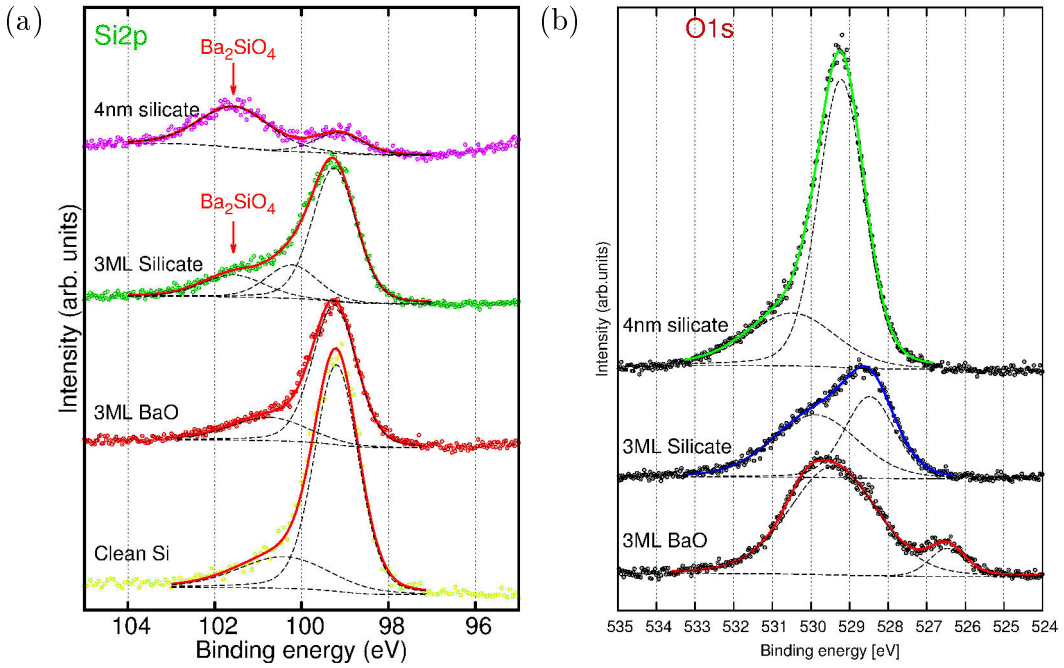


Figure 7.14 - (a) Si2p peaks, without oxide, with 3ML oxide and with thin (3ML) and thick (4nm) silicate on top of it (b) O1s peaks of pure BaO and from thin (3ML) and thick (4nm) barium silicate.

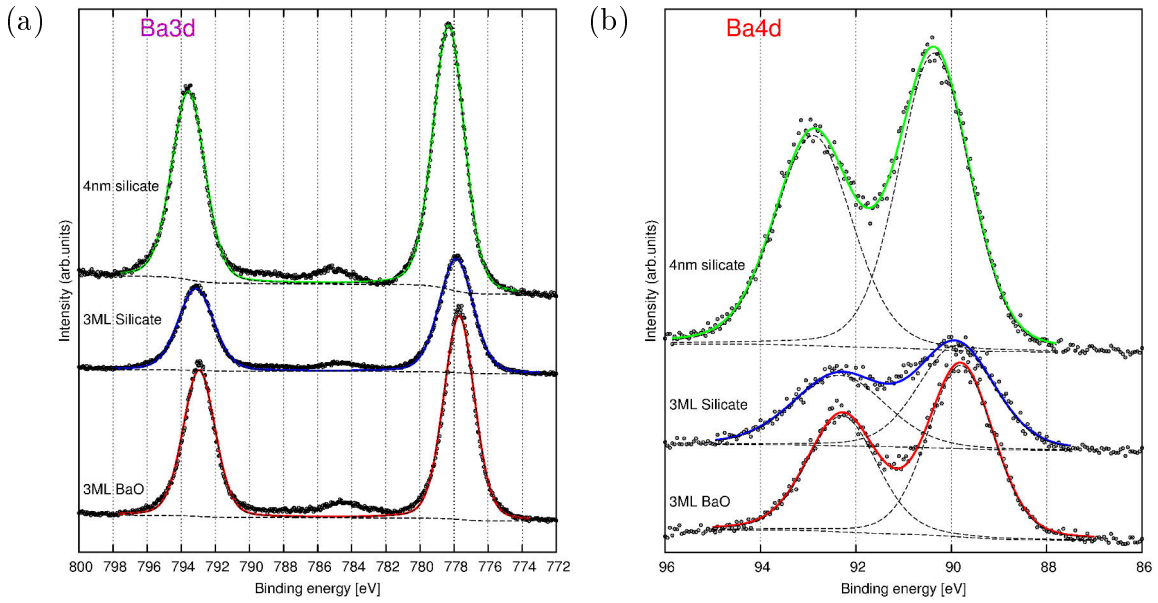


Figure 7.15 - (a) Ba3d peaks, with 3ML oxide and with thin (3ML) and thick (4nm) silicate on top of it (b) Ba4d peaks of pure BaO and from thin (3ML) and thick (4nm) barium silicate.

7.2.2 Structural (LEED) observation of barium silicate

The schematic diagram of diffracted image of barium silicate on top of Si(001) surface is shown in Section-6.3. The crystal orientation of silicate has an angle of 45° with that of Si(001) or Si(010) direction. SPA-LEED images of barium silicate are shown in Fig. 7.16. Here we have shown an example of 2.5nm thick Ba silicate film, together with unit cell marking on SPA-LEED image for better understanding. The film thickness is calibrated using TEM, see below. As seen here, two ordered rectangular crystalline domains can be discriminated, which are aligned along the [110] and [1$\bar{1}$0] directions of the Si(100) surface.

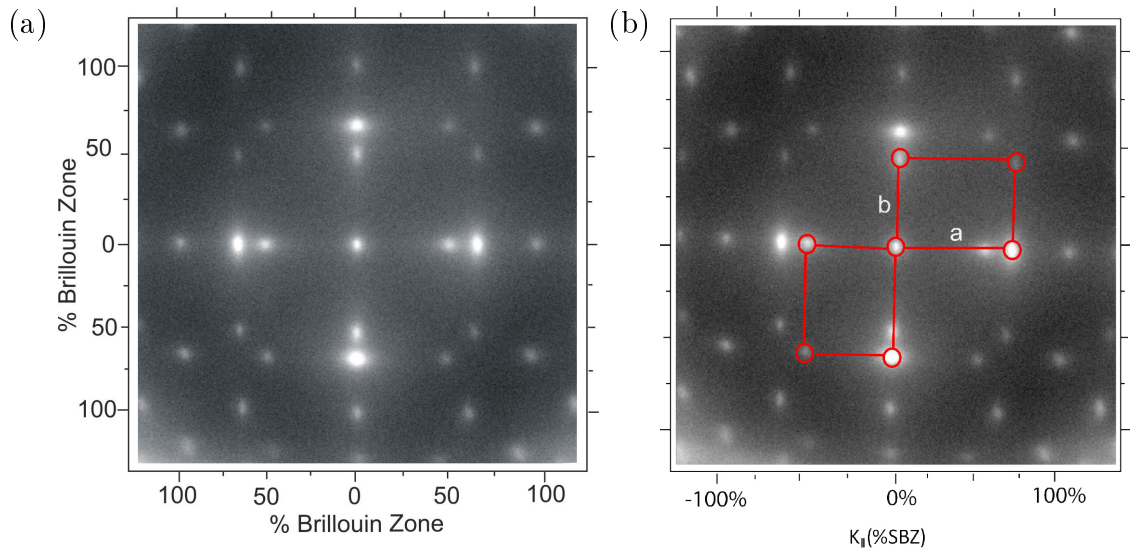


Figure 7.16- (a) SPA-LEED image of 2.5nm crystalline Ba_2SiO_4 at 70 eV, (b) inverse lattice constants of real lattice constants "a" and "b" of Ba_2SiO_4 unit cell are marked in diffracted SPA-LEED image

From the SPA-LEED measurements we can see the two axises (namely "a" and "b") of crystalline orthorhombic silicate but the largest axis of the orthorhombic Ba_2SiO_4 structure is normal to this projection, hence not visible here, which is visible from the Transmission Electron Microscope (TEM) image below. The shorter axis in reciprocal space coincides within error margins with the ×2 spots of the (2 × 1) reconstruction of the clean Si(001) surface, while the other one is one third longer. Precise evaluation and transformation to real space of these experimentally obtained diffraction spots [figure-7.16(b)] yields lattice constants of $|\overrightarrow{a}| = 5.77 \pm 0.03$Å and $|\overrightarrow{b}| = 7.61 \pm 0.03$Å, which are in close agreement with the values obtained from the literature [40], which states orthorhombic bulk lattice parameters of Ba_2SiO_4 are a = 5.81Å, b = 7.51Å and c = 10.21Å. From the lattice constants determined here it is obvious that the c-axis for the crystallites seen here is oriented normal to the surface, whereas there is epitaxial growth with 'a' and 'b' axis aligned along [110] and equivalent directions. we can also see that the length of 'b' axis of silicate is almost twice that of silicon lattice constant, $b \approx 2 \times 3.84$Å

($Si = 3.84$Å).

Crystalline growth and similar values of lattice parameters (a = 5.81Å, b = 7.51Å, c = 10.21Å) have also been obtained in a previous combined RHEED and x-ray diffraction study on Sr and Ba silicate films grown at comparable temperatures [40].

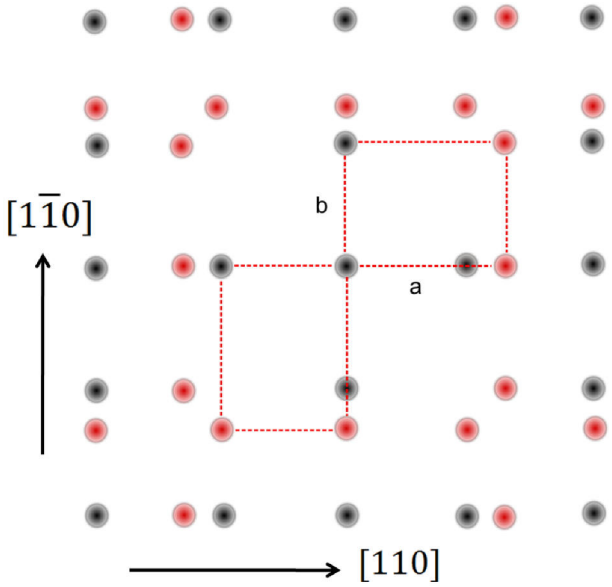


Figure 7.17 - Schematic diffracted image of barium silicate, which illustrates the spots of two domains of the Si p(2×1) (dark spots), coincide with those of the two rectangular unit cells of Ba_2SiO_4 domains and produce additional spots (red).

The schematic representation of SPA-LEED image at Fig.-7.16 shows at figure-7.17, for better understanding of the diffracted pattern of crystalline barium silicate. The two favorable growth direction of silicate unit cell are shown in the schematic. From two different thickness of thin film we have seen that the lattice constant 'a' agrees with the bulk lattice constant within error bars but lattice constant 'b' deviates in opposite directions. We cannot give a direct reason for this discrepancy, it might be due to slight differences in stoichiometry within the films. That such deviations from the exact stoichiometry occur is almost to be expected, since the Si species during silicate formation has to diffuse into and through the silicate films already present [38]. This process to be effective requires a finite gradient of Si concentration within the film, and thus a deviation from exact stoichiometry. This finding is in agreement with the observation of reduced crystalline quality with increasing film thickness (see below).

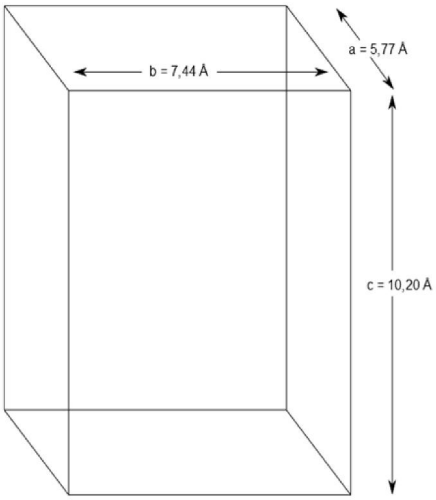


Figure 7.18- Orthorhombic unit cell of Ba_2SiO_4

The orthorhombic unit cell of Ba_2SiO_4 shown in figure-7.18 and the corresponding values of lattice constants $a = 5.77$Å, $b = 7.44$Å and $c = 10.20$Å according to the literature [40].

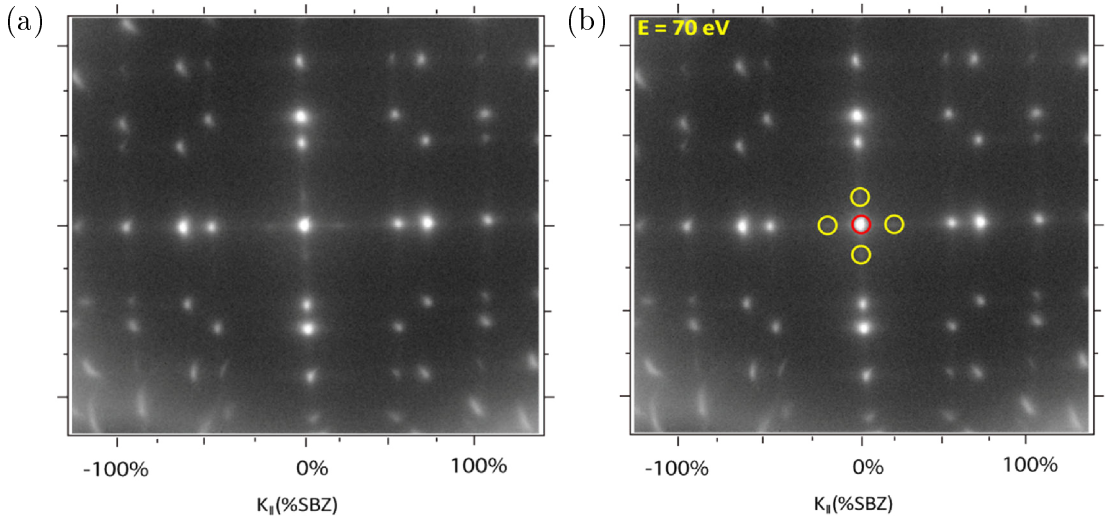


Figure 7.19- (a) SPA-LEED image of crystalline Ba_2SiO_4 structure at 70 eV, (b) Spots around center spot (0,0) marked with circles.

In SPA-LEED image we can see four additional spots (figure-7.19) around the center (0,0) spot. Which are not repeating anywhere in the diffracted image. To get further detailed information about these spots we have taken 1D SPA-LEED image along the red line of the 2D SPA-LEED image (figure-7.20(a)).

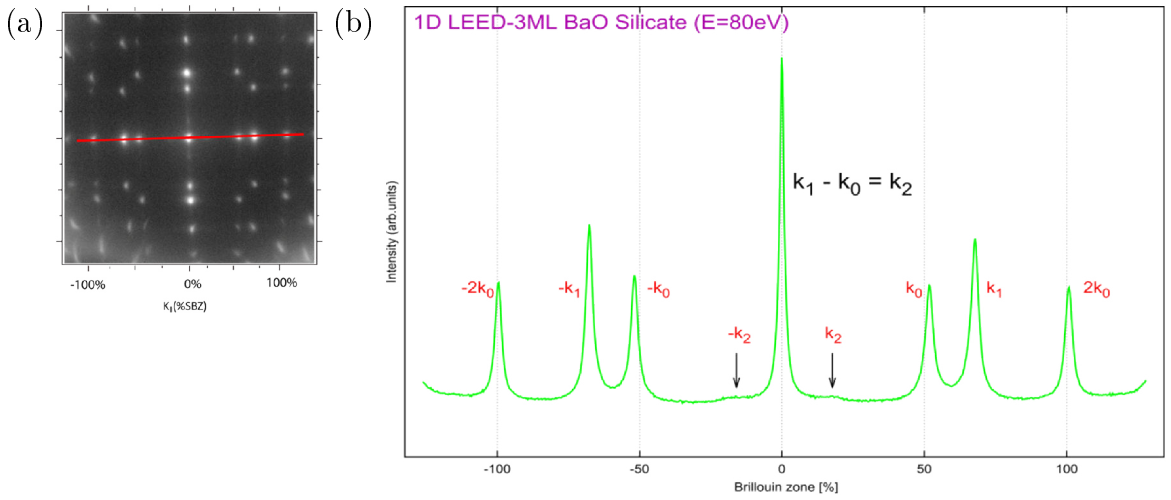


Figure 7.20- (a) Red line indicates the scan direction in 2D SPA-LEED image (b) 1D SPA-LEED image of silicate crystal surface

The 1D SPA-LEED image of 3ML Ba_2SiO_4 is shown in figure-7.20(b). The four spots around the center (0,0) spot are at position k_2, which is equal to the subtracting distance of k_1 and k_0, that is $k_2 = k_1 - k_0$ or $k_2 + k_0 = k_1$. But K_0 and k_1 belong to different crystallite orientation, which should not be able to interfere, so that this vector addition is fortuitous. From this relation it seems the spot at k_2 is not representing any real lattice point of silicate crystal, rather it appears due to the convolution of the structure. The real intensity of the spot k_2 is not very high or weak but due to logarithmic scale it is significantly visible in the diffracted image.

7.2.3 Silicate layer observation using TEM

In order to get more insight into the detail of the growth mechanism and the interface properties at the atomic scale, we performed cross sectional Transmission Electron Microscopy (TEM) investigations. The TEM results are discussed in this section. The Ba_2SiO_4 layer with a thickness of about 5nm is shown in figure-7.21. The silicate layer shown diagonally in the figure due to the technical reason.

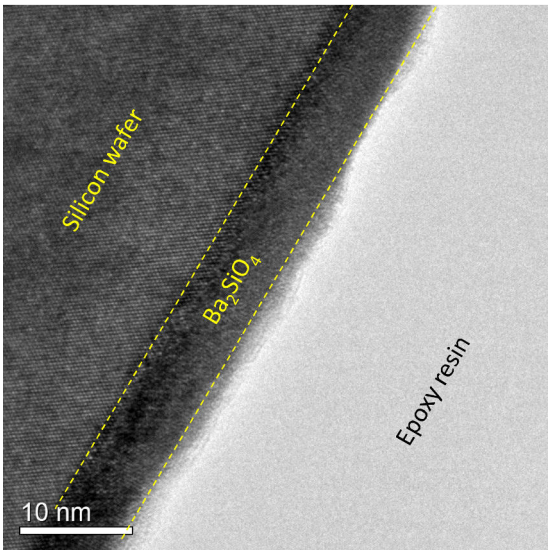


Figure 7.21 - HRTEM image of 5nm silicate.

The figures-7.22 below show the same sample area with bright-field and in the dark field contrast. The two dark-field images show the cross section of sample material. In these images the layer of Ba_2SiO_4 can be recognized by the bright contrast. From the overall observation these areas indicate cystallites with different orientations or in some cases the films can be polycrystalline. In addition, both dark-field images show different crystallites with high intensities which suggests that we are not dealing with epitaxial growth but the growth with preferred orientations. From these still somewhat qualitative images, we can identify a sharp interface between silicate and silicon. We can see uniformly thick silicate film on silicon substrate.

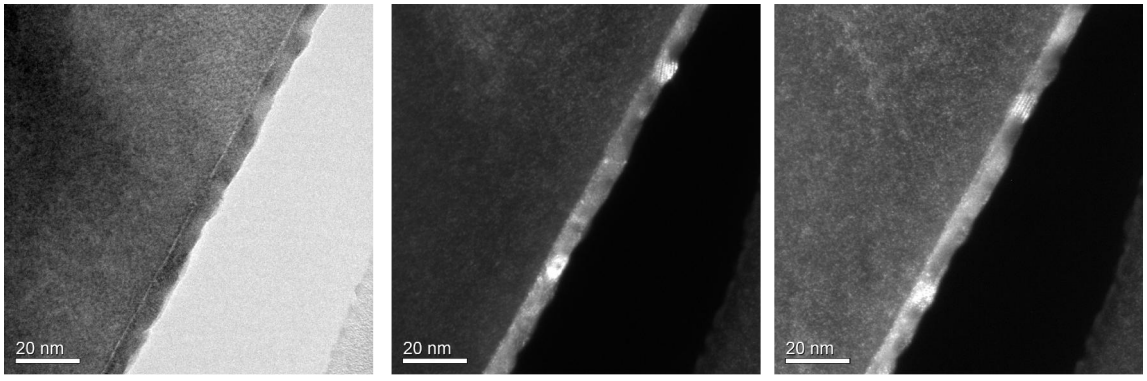


Figure 7.22 - Bright field and dark field TEM image of 5nm Ba_2SiO_4 from the same sample area. Areas with light contrast in the dark-field images show a polycrystalline character of Ba_2SiO_4 layer. Different crystallites of same orientation are visible with high intensities.

In TEM dark-field images, a certain orientation of crystal shows bright spot compared to others. During the electron microscopic observation of thick ($>$ 5nm) silicate layer, there are also areas that showed a significant higher amorphous content within the Ba_2SiO_4

layer. Bright field image here does not give more information about the crystalline silicate, but these are shown below with higher magnification in detail.

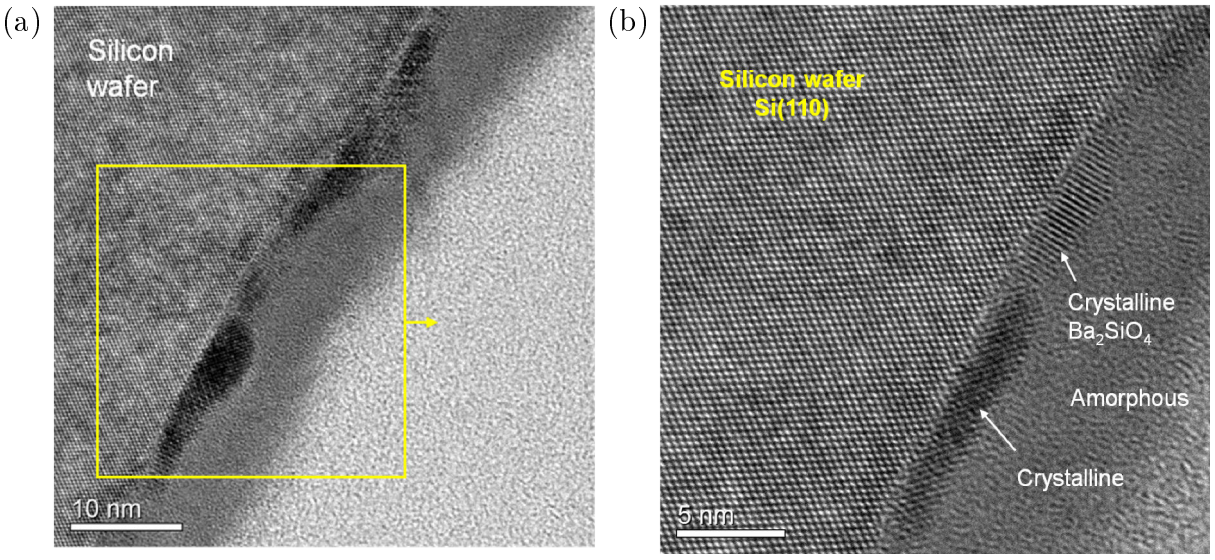


Figure 7.23 - (a) FE-TEM bright field image of 10nm barium silicate (b) HRTEM- image

The FE-TEM bright field image of Ba_2SiO_4 layer with a thickness of about 10nm is shown in figure-7.23(a). The selected sample area shown in the figure-7.23(a) is shown in higher magnification in figure-7.23(b). The average lateral extension of the crystallites is about 15nm.

The right figure shows the crystalline structures of the silicate layers. The layer shows crystalline structures all over the interface. The crystalline regions within the layer can be seen as dark spot, which can be identified by the partially visible lattice planes. Here one can see the Si(110) surface in the upper left part of the image and the growth of silicate at lower left side. Since the structure is centered rectangular, we always see some projection, and the one with the long narrow stripes corresponds to the (100) projection, which shows half of the lattice constant "a", similarly we see in other parts the (010) projection with lattice constant "b" [figure-7.16(b)]. In accordance with the LEED results shown above, the main crystallographic orientations of Ba silicate are along the [110] directions of Si, and crystallites with both types of orientations $[100]_{Ba_2SO_4} \parallel [110]_{Si(100)}$ and $[010]_{Ba_2SO_4} \parallel [110]_{Si(100)}$ (darker sections) can be identified.

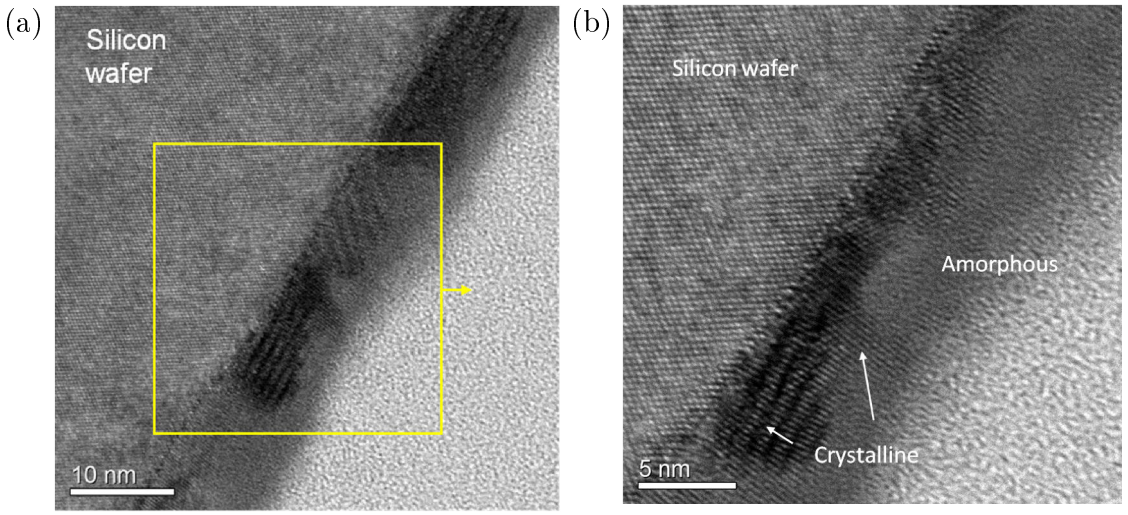


Figure 7.24 - (a) FE-TEM bright field image of 10nm barium silicate (b) HRTEM- image

We can see another TEM image of 10nm crystalline barium silicate (figure-7.24), where the enlarged view of FE-TEM image (a) is shown as HRTEM image at (b). At image (b) in some locations an intensity modulation normal to the interface with a period of 1.0 nm can be identified, which corresponds to lattice constant 'c' of the crystallites. The total thickness of the silicate is 10nm and we can see the maximum growth of crystalline silicate is almost 8nm thick. Although the thickness of crystal growth is not uniform but the growth is continuous all over the interface, which also support the evidence of close crystalline silicate growth at the interface from EDX measurements at figure- 7.28.

The figures below (fig. 7.25) show the Ba_2SiO_4 layer with a thickness of about 5nm at different magnifications. In this case the overall crystallinity of the film is improved considerably, since crystalline regions now extend up to the full layer thickness. Apart from extended crystallites with the same orientation and also a similar average size as described for the 10nm film, a minority species of much smaller nanocrystallites with other orientations are visible at figure-7.25(b), shown by the top and bottom arrows.

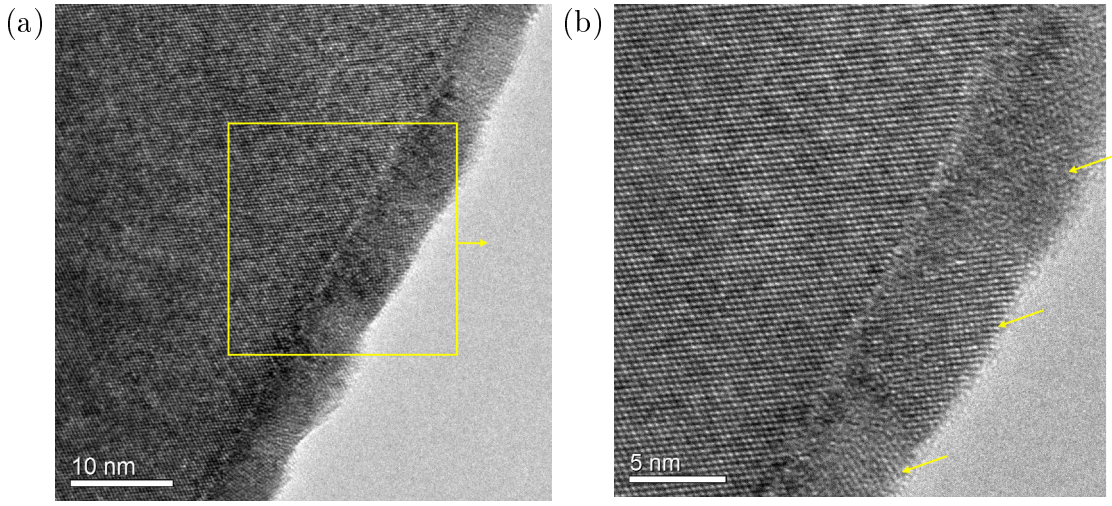


Figure 7.25 - (a) TEM bright field image of 5nm Barium Silicate (b) HRTEM- image, middle arrow shows the crystallites with same orientation, the top and bottom arrows show nanocrystallites with other orientations

From the HRTEM images, we do not see any clear evidence of a unidirectional epitaxial growth of silicate crystal on the silicon wafer. Rather we observe that the majority of crystallites clusters have the orientations also seen in LEED. Some of these clusters may even still be amorphous, since no signal above the diffuse background is detectable with SPA-LEED. From TEM it is not clear that the "crystallites with other orientations" are really crystalline. If they are amorphous or extremely small (around 1 nm), LEED would not see them. The relative amount of crystalline and amorphous silicate is dependent on the detailed growth conditions, which, however, are not varied systematically enough in this study to draw any quantitative conclusions.

Here silicate grows under reactive growth conditions. As silicon diffusion through the oxide is the most crucial step for the formation of Ba silicate, it is not surprising that the interface between silicon and silicate is quite rough, even on the atomic scale, as demonstrated in the enlarged figures-7.24 and 7.25 for 10nm and 5nm silicate films, respectively. But the silicon-silicate interface remains atomically sharp, as seen from these images. We can not see any evidence for formation of any kind of interface layer with a different composition or formation of a silicide at the interface. On the other hand, there is evidence for an enhanced concentration of structural defects at the interface in these images, which also may have consequences on the electrical properties (shown below). These structural interface defects are necessarily coupled with local compositional fluctuations on the atomic scale.

7.2.4 Studying elemental distributions in silicate using EDXS

The dark field STEM image shows the sample material in the cross section (Fig. 7.26). The layer of Ba_2SiO_4 is identifiable by the bright contrast. We performed EDXS mea-

surement on this sample and the outcomes are described below.

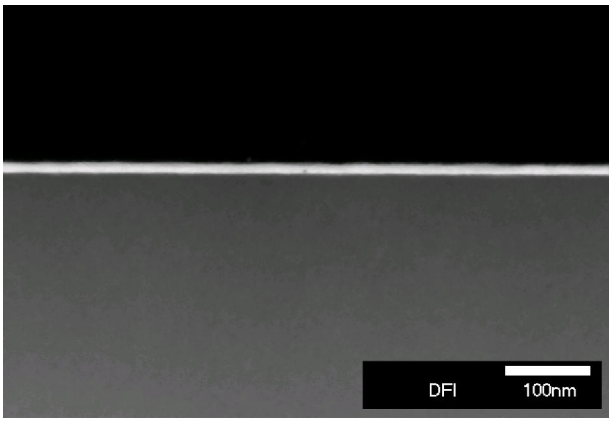


Figure 7.26 - Dark-field STEM image of 10nm Ba_2SiO_4 on Si(001), the area which was later analyzed by EDXS

According to the sample materials the elements carbon, oxygen, silicon and barium are detected in the Energy Dispersive X-ray Spectroscopy (EDXS) spectrum (fig. 7.27). Probably due to impurities the element chlorine is also found, which came from the sample preparation steps for TEM measurements.

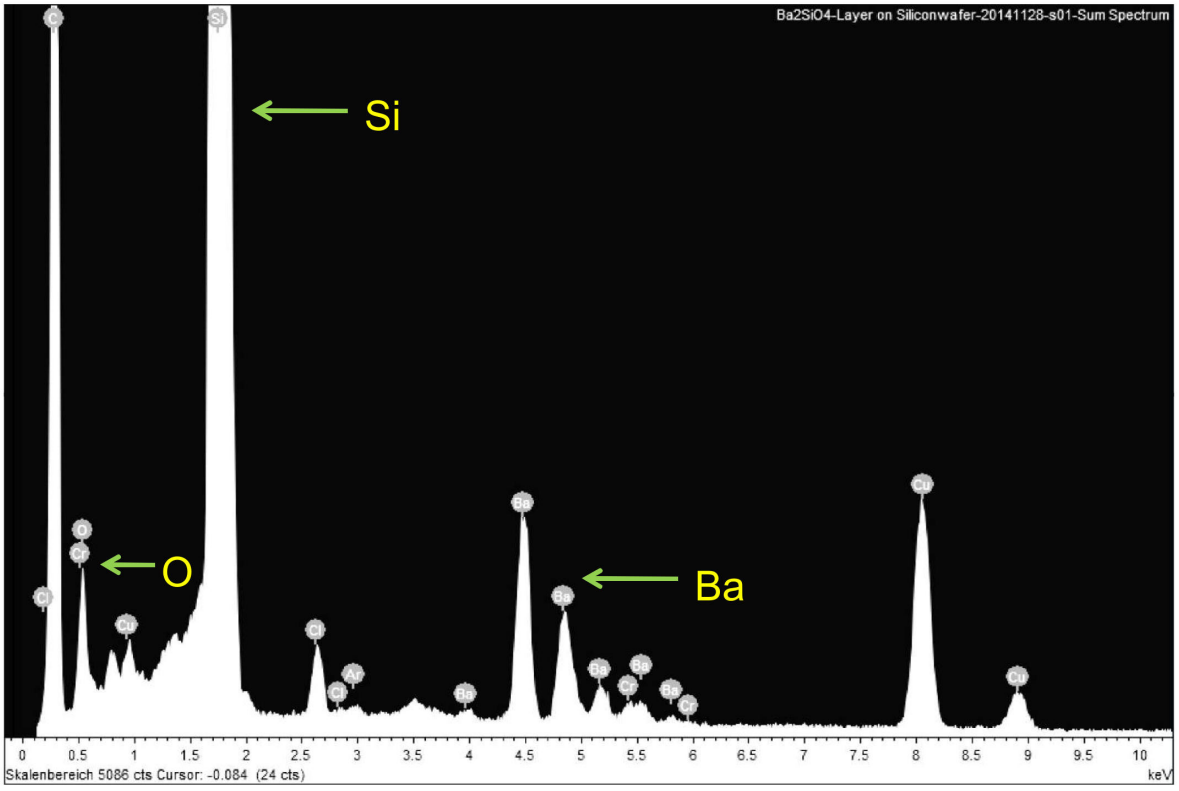


Figure 7.27- EDXS of 10nm Ba_2SiO_4 showing the different elements distribution in the sample segment shown at figure-7.25.

Due to an $Ar+$ ion sputtering process during sample preparation, the element argon is detected in the sample material at a low concentration. The Cu and Cr signals are from sample holder due to partial hit by measurement beam, but not from the sample under examination.

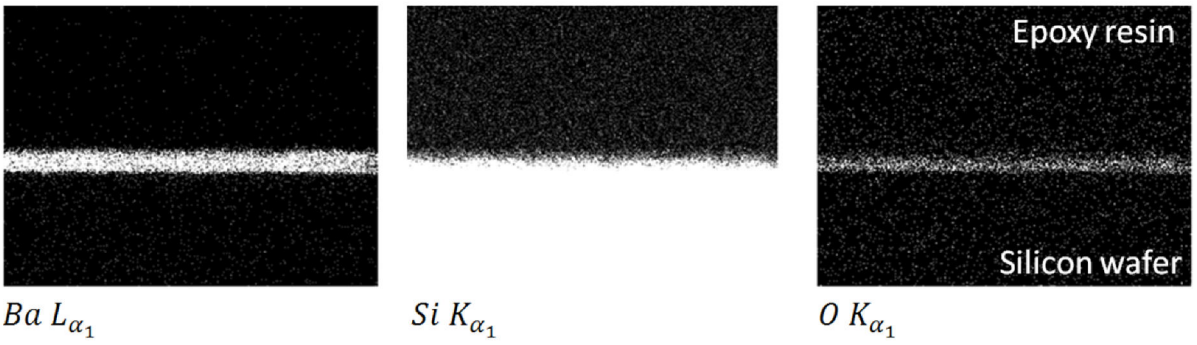


Figure 7.28 - EDXS of 10nm Ba_2SiO_4 showing the Ba, Si and O distribution in the sample within 170nm spatial range.

The EDX spectrum of barium (Ba), silicon (Si) and oxygen (O) are shown in figure-7.28. Here by fixing the detection energy at a certain small range, the concentration distribution image of that certain element in that scanned area is obtained. We start with an elemental analysis carried out with EDX analysis at the $K_{\alpha 1}$ edges of oxygen and Si, and the $L_{\alpha 1}$ edge of Ba, respectively, for a nominally 10nm thick silicate film. From the distributions of the elements, the homogeneous chemical composition of Ba_2SiO_4 layer can be seen. Here the epoxy resin is at top and silicon substrate is at the bottom of the image. Here detected elements are shown in bright or white color. In case of Silicon, it detects silicon both in silicate layer and also in substrate, so we can see bottom of the middle image is completely bright. Within the resolution of this method of about 2nm, we can directly observe the homogeneous concentrations of 'Ba' and oxygen within the layer, while the Si signal fades out at the edge to the epoxy layer, as expected from the arguments given above from TEM observations. As a consequence to this concentration gradient of Si, the 10nm thick film is only crystalline close to the Si-silicate interface, but lacks crystallinity in about half of the thickness, as seen in the Fig. 7.23.

7.2.5 Band offset of dielectric layers on Si(001) substrate

To get the band offset between silicate and silicon, we used x-ray photo-electron spectroscopy (XPS) on an unstructured sample. At first we determined the relative positions of valence band edges on bare Si, successively using on ultra-thin (2ML) and thick (>5 nm) silicate layers, which are deposited on top of Si-substrate. By following the method of Waldrop et al. figure 7.29 [64], we have deduced the valence band offset. This method is based on XPS measurements of the energy difference between arbitrary core lines and valence band edges of bulk materials of the silicate and of the silicon substrate. The energy difference between the same core lines for the silicon/silicate heterojunctions, as

schematically shown in Fig. 7.29. This method allows both the determination of band alignment and adsorbate induced band bending. From the experimentally determined band gap, the deduction of conduction band alignment is also possible (see below).

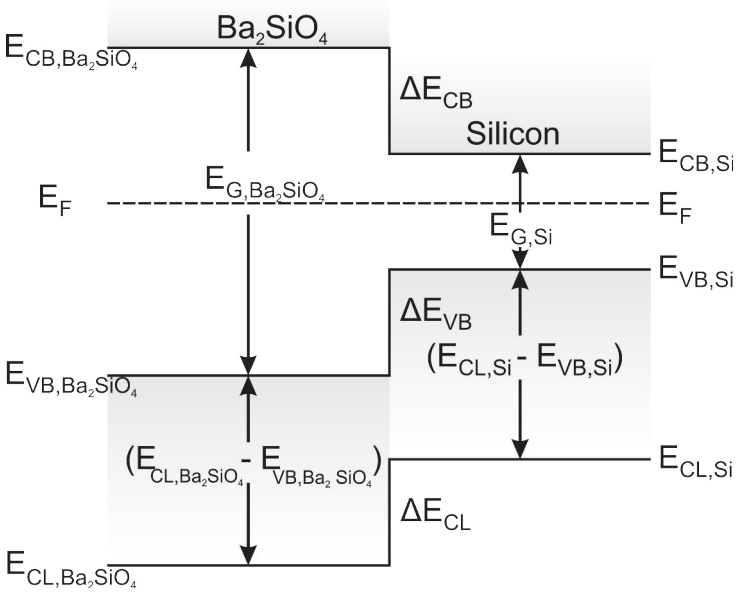


Figure 7.29 - Schematic energy band diagram of thin dielectric layer and silicon interface [64].

$$\Delta E_{VB} = (E_{CL,Si} - E_{VB,Si}) - (E_{CL,Ba_2SiO_4} - E_{VB,Ba_2SiO_4} - \Delta E_{CL})$$
$$\Delta E_{CB} = E_{G,Ba_2SiO_4} - \Delta E_{VB} - E_{G,Si} \qquad [64]$$

Here $E_{CL,Si}$ = Binding energy of the Si2p-Peak; $E_{VB,Si}$ = valence band edge of clean Si; E_{CL,Ba_2SiO_4} = binding energy of O1s-Peak from the 5nm Ba_2SiO_4; E_{VB,Ba_2SiO_4}= valence band edge of 5nm Ba_2SiO_4; ΔE_{CL} = energy difference between the O1s-Peak and the Si2p-Peak

We used the XPS spectra of pure p-Si(001) (2×1), for a thin (3 ML) Ba_2SiO_4 film on Si(001), where the Si2p is still visible in the spectrum, and for a thick Ba_2SiO_4 film ($\sim 10nm$), where the influence of the interface is negligible. In this way we measured the core level of silicon ($E_{CL,Si}$) and silicate (E_{CL,Ba_2SiO_4}). By fitting straight line in XP-spectra of valence band edge, we determined the valence band edge energy of silicon ($E_{VB,Si}$) and silicate (E_{VB,Ba_2SiO_4}); detail of fitting can be found in [37].

In order to determine the width of the bandgap, we performed electron energy loss spectroscopy (EELS) on unstructured samples using a standard electron gun as electron source, yielding an energy resolution of about 0.5eV. As seen from the typical EELS spectrum shown in Fig. 7.30, the silicate films have a clear band gap with a small excitation background of about 10^{-2} of the elastically scattered peak intensity. A gradual

increase is seen for loss energies above 4eV, which we ascribe to the excitation of Frenkel excitons. To measure the bandgap, we used both the Gaussian fit and the linear fit method [62]. It is visible from figure below that both of the methods are showing the same bandgap of 5.7eV. To estimate the bandgap energy according to the linear fit method, the intersection of a straight line drawn through the background level with a linear fit to the signal of bulk loss spectrum. Since the series of excitations cannot be resolved, only a single peak is used in the fit for the excitons, together with further Gaussian peaks for bulk silicate excitations. The steep increase close to 7eV loss energy indicated the dominance of bulk excitations at higher loss energies. An estimate for the bulk band gap of Ba silicate was obtained from the linear extrapolation of this steep increase back to zero loss intensity to be 5.7 ± 0.1eV. This value coincides with the first abrupt change of slope of the loss intensity, which can be taken as a further indication of the onset of bulk excitations.

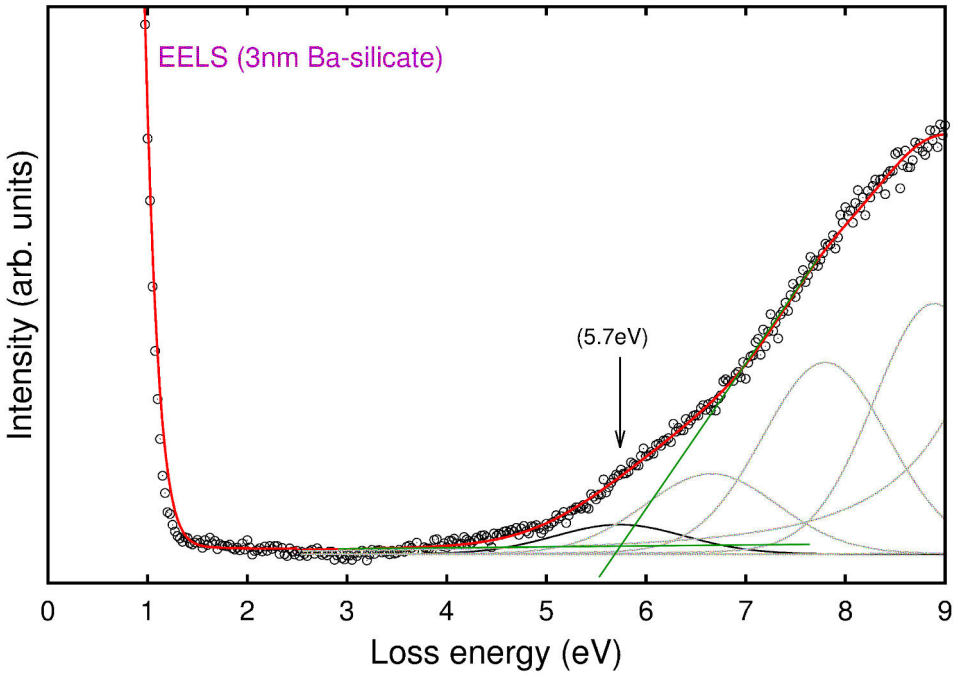


Figure 7.30 - Electron energy loss spectrum on a 6.25nm thin Ba silicate layer. The band-gap is determined by linear extrapolation of the loss intensity on the right side, not considering the excitonic loss (black curve). Measured band gap of Ba-silicate is 5.7eV with E = 100eV.

With this information, we then determined the band offsets and the band alignment of Ba silicate with respect to p-doped Si(100) by XPS using the methods of Waldrop et al. Core levels of Si2p, Ba3d, and O1s are used. Instead of bulk material for the silicate, we used the values for the 10nm thick film and compared it with the 3ML thick silicate film. More details of the data evaluation are described in ref [37]. The calculation of valance band and conduction band offset of barium silicate using Ba3d peak is shown below.

$$\Delta E_{VB} = (\Delta E_{Si} + \Delta E_{CL}) - \Delta E_{Ba_2SiO_4} = [(98.9 + 678.4) - 774.8] \pm 0.1eV = 2.5 \pm 0.1eV$$
$$\Delta E_{CB} = E_{G,Ba_2SiO_4} - \Delta E_{VB} - E_{G,Si} = (5.7 - 2.5 - 1.1) \pm 0.1eV = 2.1 \pm 0.1eV \quad [64]$$

Results of measured crystalline Ba_2SiO_4 and previously measured in our group, amorphous BaO layers [51] are shown in Fig. 7.31 and Fig. 7.32 respectively. All band offsets, within the accuracy of determination of ±0.1 eV, turned out to be close to or above 1 eV, on both p- or n-type substrates. Thus, the requirement for sufficiently low thermally excited leakage under typical electronic operating conditions is clearly fulfilled.

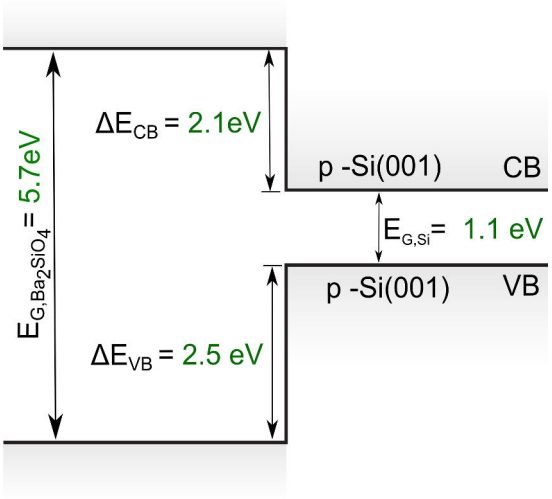


Figure 7.31 - Band offset of crystalline barium silicate and Si(001) from their band diagram

Again significant differences are found between crystalline silicate and amorphous oxide layers, which we ascribe again to the differences in interface preparation. Due to amorphous growth of BaO on Si(001) substrate and different band gap (4.2eV) in comparison to barium silicate results in a more asymmetric band alignment. While it may not be surprising that the high density of interface states for the amorphous oxides (i.e. BaO) determines the band alignment. It should be noted that this is also the case for the crystalline layers (i.e. Ba_2SiO_4). We worked with p-type silicon substrate, but previous studies shown that no differences in band alignment on n- and p-type substrates are detected [51], that means the relative positions of bands are pinned by the interface states both for crystalline and amorphous layers.

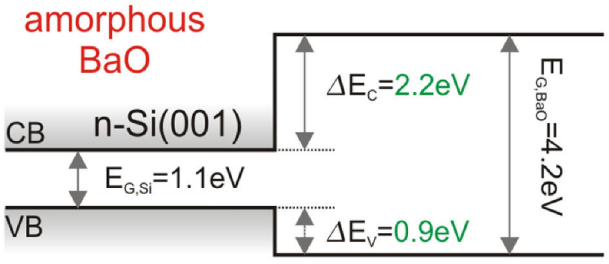


Figure 7.32 - Band offset of amorphous barium oxide and Si(001) from their band diagram

7.2.6 Stability of barium silicate at ambient air

We tested the stability of the silicate layers in air. While the BaO layers turned out to be extremely hygroscopic and to react to hydroxide within seconds when exposed to ambient conditions, the silicate is much more stable, as demonstrated by the spectral data shown in figure-7.33 for O 1s and Ba 4d.

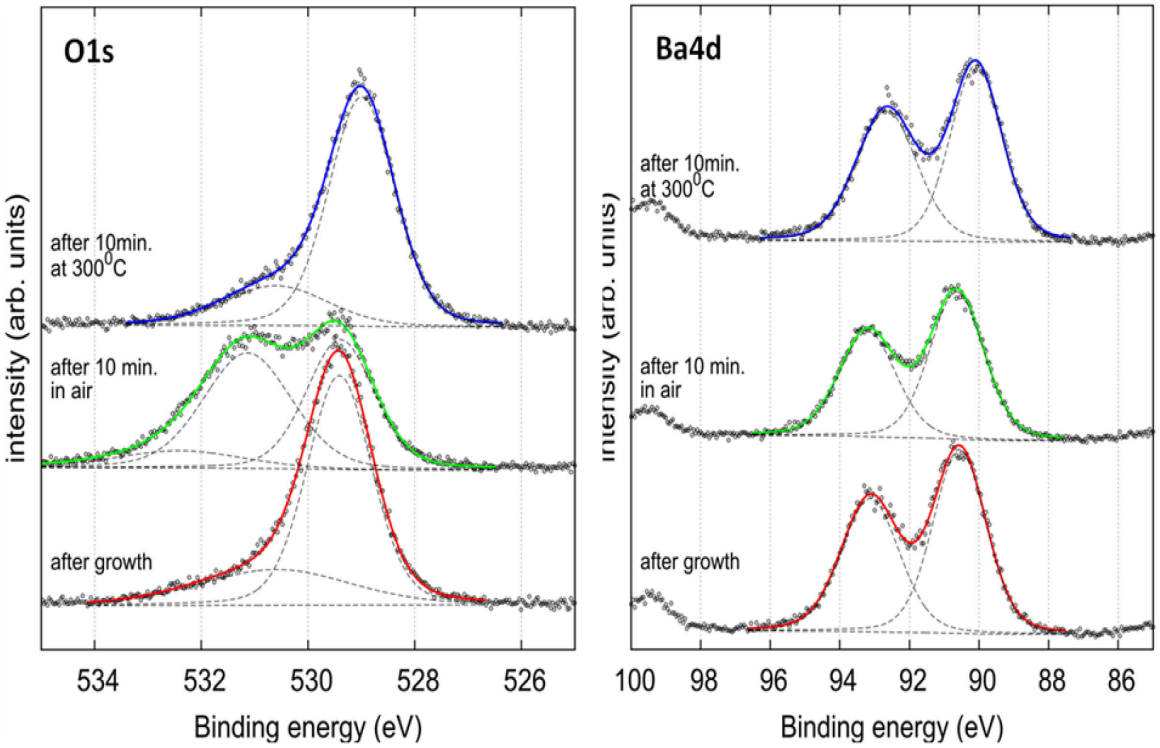


Figure 7.33 - Demonstration of crystal water uptake by silicate after exposure to air. From bottom to top, the XPS spectra are for a 5nm thick Ba_2SiO_4 film, after transformation to silicate, after exposure to ambient conditions for 10 min, and after heating in UHV to 300°C for 10 min.

The bottom spectra show the silicate after annealing of a 5nm thick oxide layer at 650°C for 45 min. Afterwards the sample is exposed to air for 10min and put back into vacuum. After this treatment, the XPS intensities of all XPS peaks are reduced and the shoulder of O 1s peak increased and broadened at higher binding energies. This finding, however, excludes the formation of hydroxy species, since they would increase the intensity of the peak at 529 eV binding energy [63], contrary to our observation. The shoulder to the O 1s peak is compatible with water adsorption, but may also contain contributions from carbon and oxygen containing species [63], since a clear C 1s signal can now be detected that was absent after growth and reaction of the silicate layers.

Also the Ba4d peak intensity gets reduced after exposing the sample in air which, however, is restored almost completely after annealing the layer to 300°C for several

minutes in vacuum. The latter treatment can, however, not completely remove the C1s signal but the intensity of O1s shoulder is reduced significantly i.e., the crystal water which is taken by silicate during exposure to air completely disappeared after annealing at temperature 300°C.

7.2.7 Dielectric constant of barium silicate

MOS diodes are fabricated completely in UHV for oxide thicknesses between 6.25nm and 13nm at a surface temperature of 650°C under a constant flux of Ba in oxygen background pressure with an Al interface layer and a Au capping layer, as mentioned above. These samples turned out to be stable in air (shown above) so that C-V and I-V measurements could be carried out ex-situ. From the measured C-V data we determined quantitatively the capacitance in strong accumulation using a frequency dependent 'three-element model'. The capacitance equivalent thickness (CET) is calculated from the capacitance value measured in the accumulation region, without considering any quantum mechanical effects. Here all the electrical measurements are taken on windows of the same size (area $= 4\times\ 10^{-4}$ cm^2). The gate metal/field oxide overlap capacitance was subtracted carefully for each case.

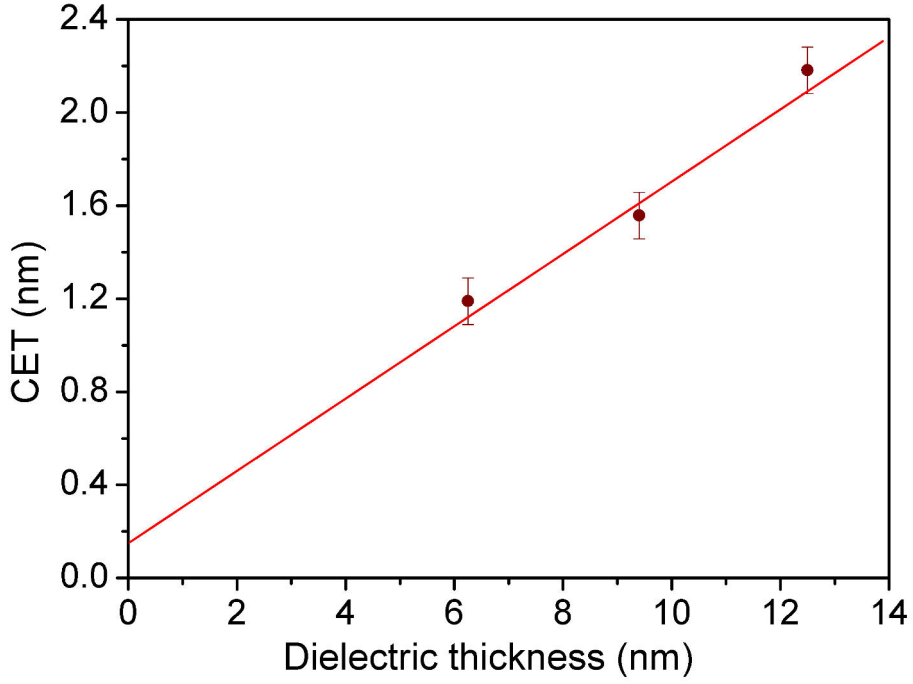


Figure 7.34 - CET variations as a function of the physical dielectric layer thickness for the Ba_2SiO_4 films. Here we plotted averages over nine diodes of different dielectric thicknesses.

Figure-7.34 shows the capacitance equivalent thickness (CET) of $Si/Ba_2SiO_4/Au$ structures at constant accumulation as a function of dielectric layer thickness. The error bars

are determined from the scatter of the values for various sample windows. Within these error limits the data fall on a straight line. The measured dielectric constant (k) value is $\epsilon = 24.6 \pm 0.2$ from the slope of the straight line fit in Figure-7.34. This value is within the high-k range. From the positive intercept on the ordinate we deduce that there is a contribution of capacitance of the silicon substrate with an equivalent thickness of 0.155nm. C-V characteristics recorded at 100 kHz indicate a systematic capacitance scaling with dielectric layer thickness, as illustrated in Figure-7.34. The lowest capacitance equivalent thickness achieved in the present study is ∼1.2nm for 6.25nm dielectric film. Since silicate layers with a thickness down to at least 3nm can be produced without problems, CETs of 0.5 or less are feasible with this material. Also expected is the negative intercept with the x-axis at -1.55nm due to the finite semiconductor capacitance not considered so far.

$$CET = \frac{\epsilon_0 \times \epsilon_{SiO_2}}{C_{acc}}$$

Where ϵ_0 = vacuum permittivity, C_{acc} = capacitance at accumulation and ϵ_{SiO_2} = relative permittivity of silicon dioxide.

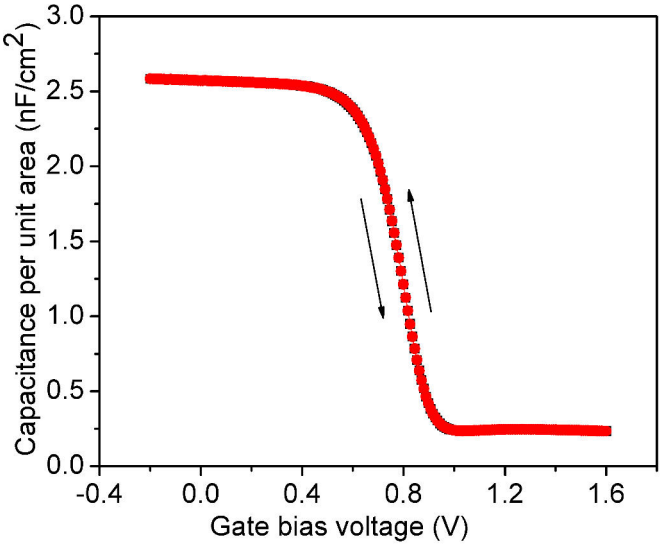


Figure 7.35 - Hysteresis < 0.5mV for 5nm Ba_2SiO_4

A typical C-V curve is shown in the Fig. 7.35. As seen there, hysteresis turned out to be below 1 mV at the middle of the curve, which on the scale shown in this figure is not visible. This demonstrates that the density of rechargeable traps near the interface is extremely low. On the other hand, the flat-band voltage is found close to 0.8V, an indication of the presence of polarization charges which sit either at the Si-silicate or the silicate-gold interface. As found by the XPS investigations shown in Fig. 7.14, however, the polarization at the Si-silicate interface is very small, so that the silicate-gold interface, and here in particular the Al interface layer, must be responsible. Although no systematic study of Al layer thickness has been carried out here, we want to mention that similar effects have been observed recently for mixed BaSr oxide layers [42] and from the theoretical work of $SiO_2 : HfO_2$ interface, where ionic charges in the oxide create image charges

in the metal at a polar interface and the amount of interface charges determine the shift in flatband voltage [67].

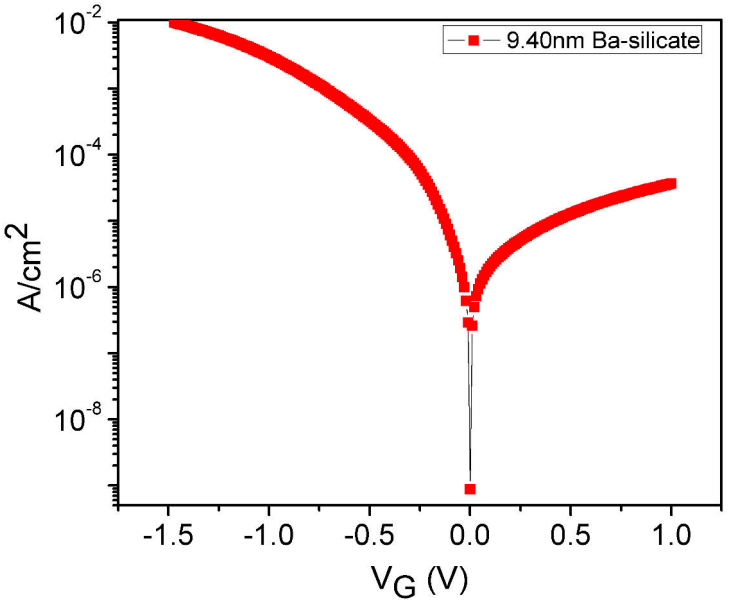


Figure 7.36 - Leakage current of 9.4nm Ba_2SiO_4 as a function of gate voltage (V_G). Zero has been set to the flatband voltage.

Figure- 7.36 shows the variation of leakage current with the applied gate voltage. For negative applied voltage the MOS diode is in forward bias condition, and hence the leakage current is higher in comparison to positive gate voltage.

An I-V curve for a 9.4nm thick film is shown in Fig. 7.36, yields a leakage current of 3 mA/cm^2 at 1V away from the flat-band voltage. The equivalent oxide thickness (CET) for this layer is 1.6nm (see above) and thus still fulfills the critical limits of leakage currents for practical applications [43].

7.2.8 Interface trap density (D_{it}) of silicate

Frequency dependent measurements are used to determine the density of interface traps D_{it}, near mid-gap using the conductance method [68]. Used substrates are p-type Si(001) wafers with a doping of $N_A = 3.5 \times 10^{15} cm^{-3}$ and measured active area of MOS diode is $4 \times 10^{-4} cm^2$. D_{it} values were derived from the peak values of conductance G_{it}/ω and the width in the frequency domain (see section-3.2.1, *conductance method*). An example is shown on the Fig. 7.37. From these curves and the known area of our windows, we have calculated the values for the interface trap density, D_{it} around $1 \times 10^{13} \pm 0.5 \times 10^{13}$ $eV^{-1}cm^{-2}$ at the position of Fermi level. Under flatband condition the Fermi level at the surface has the same distance from the valence band edge of the p-type semiconductor as in the interior (bulk). At room temperature, this energetic distance of the Fermi level from the mid-band gap is -0.32eV, determined by the bulk doping N_A.

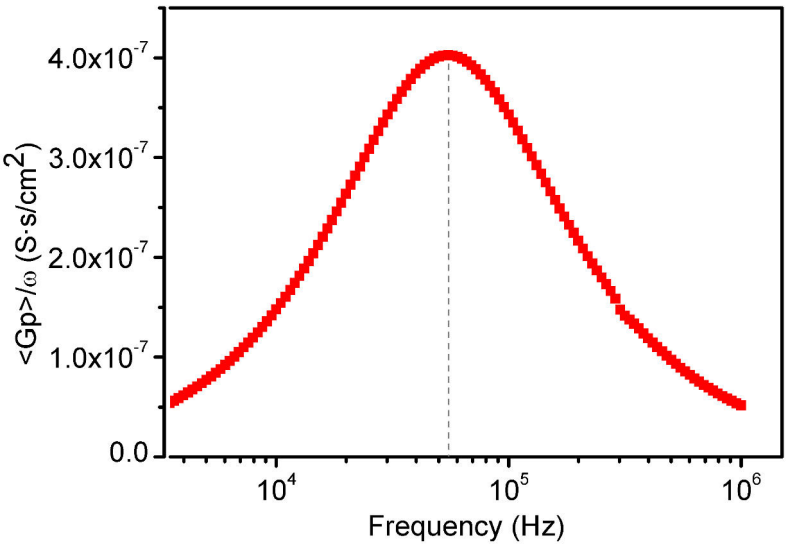


Figure 7.37 - Frequency dependent conductance curve

We used conductance vs. frequency curve (fig.-7.37) to determine the D_{it} using the equation-3.24. For example, the maximum value of conductance $[\left(\frac{G_p}{\omega}\right)_{max}]$ in figure-7.37 is $4.03 \times 10^{-7} S \cdot s/cm^2$, marked by the dotted line, substituting this value and the value of electron charge, $q = 1.6 \times 10^{-19} C$ in equation-3.24, we get interface trap density, $D_{it} \approx 6.3 \times 10^{12} eV^{-1} cm^{-2}$. Interface trap densities obtained in this way are plotted in figure-7.38. While these values scatter between samples, there is no clear tendency as a function of silicate thickness. The measured D_{it} values for silicate is too high in comparison to BaSrO [42].

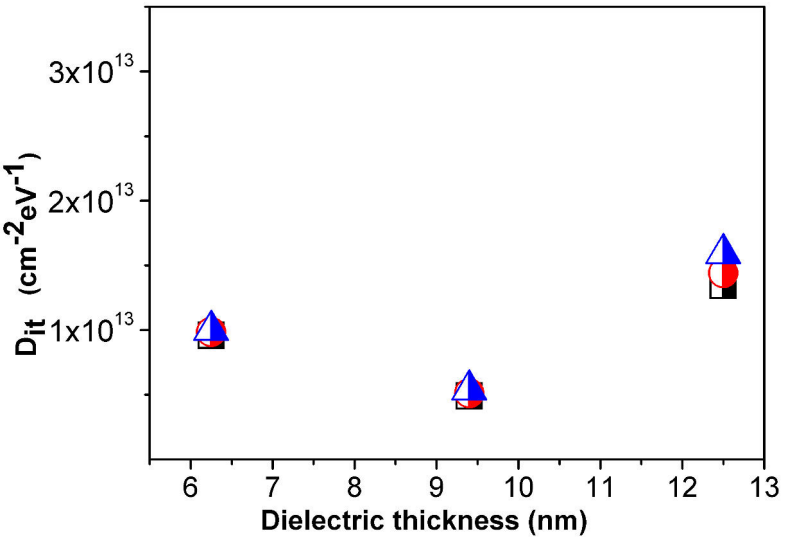


Figure 7.38 - Measured values of interface trap densities of Ba_2SiO_4 using conduction method

It may be too early to give a clear cut reason for these high values of D_{it} without further study, there are several possibilities. Two of them are, as already mentioned, the need for reactive formation of the Ba silicate and the diffusive transport of Si atoms into the silicate and to the silicate surface for further silicate formation. Especially the latter process causes a rough interface on the atomic scale between Si and the silicate, as seen in Figs. 7.24 and 7.25. Although crystallinity for the silicate layers in the vicinity of the interface is quite good, the roughness may cause local strain fields that are efficient in electron scattering. Variation of the growth mode may change this situation.

8 Summary and Perspectives

The results of this work show that Ba_2SiO_4 is a fascinating alternative gate dielectric, its outstanding properties are prerequisite for CMOS technology. The structural properties as well as most of the electrical properties are excellent. The crystalline Ba_2SiO_4 films on Si (001) have a high dielectric constant $\epsilon \approx 24.6 \pm 0.2$ with very low leakage current compared to SiO_2 films.

Capacitance-voltage measurements have shown that the defect density of movable, rechargeable impurities in the solid films is very low. As the transformation of silicate has been done at high temperature ($650°C$), the temperature stability of Ba_2SiO_4 is higher in comparison to $Ba_{0.7}Sr_{0.3}O$ as we have seen earlier in our group. The band gap of the silicate film is 5.7eV and the band offset of the film with silicon is $> 2eV$. The interface trap density D_{it} is high, which is around $1 \times 10^{13} \pm 0.5 \times 10^{13}\ eV^{-1}cm^{-2}$. Main reason of this high interface trap density is clear, which is the diffusion of Si atoms into the silicate, that makes the interface quite rough. Room temperature growth of silicate using barium and silicon evaporator simultaneously could solve this problem.

By considering all the properties of the silicate our hope that these films would be suitable for use in an industrial application.

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List of Figures

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Curriculum Vitae

Personal Information

Name	:	Shariful Islam
Genre	:	Male
Date of Birth	:	March 01, 1982
Place of Birth	:	Comilla, Bangladesh
Marital Status	:	Married
Address	:	Leibniz Universität Hannover Institut für Festkörperphysik Atomare und Molekulare Strukturen (ATMOS) Appelstr. 2, 30167 Hannover, Germany
E-Mail		shariful@fkp.uni-hannover.de
Tel		+49 172 463 8647

Education

10.2010 - 07.2015	PhD, Leibniz Universität Hannover, Germany Institut für Festkörperphysik Atomare und Molekulare Strukturen Thesis: Growth, structuring and interface manipulation of ultra-thin oxide and silicate films on silicon single crystal surfaces.
04.2006 - 07.2007	M.Sc, Jahangirnagar University, Dhaka, Bangladesh Department of Physics Thesis: Study of the soil moisture of Bangladesh by using station and NOAA satellite data.
06.2000 - 03.2006	B.Sc, Jahangirnagar University, Dhaka, Bangladesh Department of Physics