Design and analysis of field-powered transponders integrated in metallic objects

Von der Fakultät für Elektrotechnik und Informatik
der Gottfried Wilhelm Leibniz Universität Hannover
zur Erlangung des akademischen Grades

Doktor-Ingenieur
(abgekürzt: Dr.-Ing.)

genehmigte Dissertation

von
Dipl.-Ing. Eddy Brice Kaldjob
geboren am 22. Juni 1980 in Yaounde

2010

Referent: Prof. Dr.-Ing. Hermann Eul

Korreferent: Prof. Dr.-Ing. Ludger Overmeyer

Tag der Promotion: 25. Juni 2010

Kurzfassung

Schlagworte: passive Transponder, Gleichrichterentwurf, Integration im Metall.

In der vorliegenden Abhandlung werden der Entwurf und die Analyse in metallischen Gegenständen integrierter feldversorgter Transponder behandelt. Eine mathematische Gleichstromanalyse und Wechselstromanalyse von gleichrichtenden Spannungsvervielfachern mit Dioden wird für Cockcroft-Walton Gleichrichter, Dickson „charge pumps“ und Greinacher Gleichrichter im Zeitbereich durchgeführt, wobei die Anregung jeweils über eine ideale Wechselspannungsquelle erfolgt. Für die drei Schaltungstypen wird eine allgemeine Gleichung für die gleichgerichtete Ausgangsspannung entwickelt. Die Analyse berücksichtigt SPICE-Parameter der Diode, die Schaltungstopologie sowie den Lastwiderstand und ermöglicht somit ein tiefes Verständnis des Einflusses von jedem der oben genannten Parameter auf die Ausgangsspannung. Entwurfsregeln für die Maximierung der AC-zu-DC Konversion sind aus den hergeleiteten Formeln extrahiert. Die nichtlineare Diodenkapazität ist anhand eines Polynoms parametrisiert, was die Berechnung der Eingangsimpedanz der Schaltung ermöglicht. Die Analyse wird erweitert, indem die ideale Wechselspannungsquelle durch eine Antenne ersetzt wird. Zeitbereichs- und Frequenzbereichsanalysen werden für eine vollständige Systembeschreibung kombiniert, und verknüpfen die verfügbare Leistung an der Antenne, die Antennenimpedanz, die Dioden- und Schaltungseigenschaften sowie die gleichgerichtete Ausgansspannung miteinander.

Eine neuartige Implementierung von Backscatter-Modulation wird vorgestellt, wobei die logische Einheit den Betrag und Phase des Eingangsreflektionsfaktors des Gleichrichters verstimmt, indem sie dessen Lastwiderstand steuert. Die Realisierung von Amplituden- und Phasenmodulation wird anhand der Gleich- und Wechselstromanalysen untersucht, und Regeln für den Änderungsbereich des Gleichrichterlastwiderstandes werden formuliert. Empfindlichkeitsanalysen der Modulationsarten bezüglich Toleranzen der Antennenimpedanzen und Schwankung der erwarteten verfügbaren Leistung werden durchgeführt.

Das erarbeitete Konzept für die Integration in metallischen Gegenständen besteht darin, eine Bohrung innerhalb des Gegenstandes zu realisieren und sie als Einbauraum für die Transponderschaltung fungieren zu lassen. Ein adäquater Hohlleiter-zu-planar Übergang für die Feldkopplung zwischen Bohrung und Transponderschaltung wird entwickelt. Die Impedanzanalyse und Strahlungscharakteristiken der resultierenden Hohlleiterantenne sind für den Betrieb im 2,45 GHz ISM Band vorgestellt.

Erkenntnis aus dem Gleichrichterentwurf, der Modulationsimplementierung und der Integrationsmethode werden angewendet, um den beabsichtigten Transponder zu entwickeln. Die verwendeten Bauelemente sowie die auswählte Schaltungstopologie werden vorgestellt und diskutiert. Die Kommunikation findet im 5,8 GHz ISM Band statt, und die Bohrung wurde mit dielektrischen Polymeren gefüllt. Praktische Simulationsschritte für die Entwicklung der Schaltung und des passenden Hohlleiter-zu-planar Übergangs werden dargelegt. Das realisierte System wurde für Identifikation und ferne Temperaturmessung und -Übermittlung erfolgreich getestet.

Abstract

Keywords: passive transponders, rectifier design, integration in metal.

The design and the analysis of field-powered transponders integrated in metallic objects are treated in the present work. A mathematical time domain DC analysis of voltage multiplying rectifiers using diodes is done for Cockcroft-Walton rectifiers, Dickson charge pumps and Greinacher rectifiers, where the excitation is provided by an ideal AC voltage source. A general expression for the DC output voltage is developed for the three topologies. The analysis takes into account diode SPICE parameters, circuit topology and load resistance thus permiting a deep understanding of the effects of each of the above mentioned parameters on the rectified voltage. Design rules leading to the maximization of the AC-to-DC conversion and efficiency are extracted from the obtained formula. The non-linear diode capacitance is parameterized by means of a polynomial, allowing the calculation of the circuit input impedance. The analysis is enhanced by replacing the ideal AC source by an antenna. Time domain and frequency domain analysis are combined for a complete system description, giving the relation between the available power at the antenna, the antenna impedance, the diode and circuit properties, and the output DC voltage.

A novel implementation of the backscatter modulation is presented, where the logic unit controls the magnitude and the phase of the rectifier input reflection coefficient by controlling the load resistance of the rectifier. The realization of amplitude or phase modulation is analyzed by means of the combined AC and DC analyses and rules for the sweep range of the rectifier load resistance are presented. Furthermore, sensitivity analyses are done to predict the reliability of the performed modulations in case of tolerances of antenna impedance or variation of the expected available power.

The proposed approach for the integration of the transponder into metallic objects consists on the realization of a cylindrical cavity inside the object, and to use it as dwell place for the transponder circuit. An adequate waveguide-to-planar transition performing the field coupling between the cavity and the transponder circuit is developed. The impedance analysis and the radiation properties of the resulting waveguide antenna are presented for operation in the 2.45 GHz ISM band.

The knowledge on the rectifier design, the modulation implementation and the integration method are applied to develop the targeted transponder. The used electronic components as well as the choice of the circuit topology are presented and discussed. The communication has been operated in 5.8 GHz ISM band and the cavity has been filled with dielectric polymers. A practical simulation procedure for design of the circuit and the suitable waveguide-to-planar transition are shown. The realized system has been successfully tested for identification and remote temperature sensing and transmission.

Table of contents

List of abbreviations

Nature constants

$c = 299792458 \frac{\mathrm{m}}{\mathrm{s}}$	Speed of light
$e \approx 2.71828182$	Euler number
$k \approx 1.3806503 \cdot 10^{-23} \frac{\mathrm{J}}{\mathrm{K}}$	Boltzmann constant
$\pi \approx 3.14159265$	Pi

Formula symbols

a	length of the cross section
a_i	polynomial coefficient
a_F	path loss
b	width of the cross section
f	frequency
f_c	cut-off frequency
f_clock	microcontroller clock frequency
f_0	fundamental frequency
h	current-voltage characteristic
i	subscript
i_C	current through the diode capacitance
i_{Cc}	current through the circuit capacitance
i_D	total diode current
i_G	current through the diode conductance
i_R	current through the resistance R
l	length
m	integer
m_mod	modulation depth
n	ideality factor
q	elementary charge
r	link range

t	time
v_{Cc}	circuit capacitance voltage
v_{D}	total voltage across the diode
v_{oc}	open circuit output DC voltage
v_{R}	voltage across the load resistance R
v_{s}	AC source voltage in the Thevenin model
x , z	variables

B_{D}	diode susceptance
B_{V}	breakdown voltage
C	total diode capacitance
Cc	circuit capacitance
C_{dep}	depletion capacitance
C_{dif}	diffusion capacitance
C_{e}	end shunt capacitance
C_{i}	parasitic capacitance between inner conductors
C_{j}	effective depletion capacitance
C_{j0}	zero voltage depletion capacitance
C_{m}	resonant circuit capacitance with resonance at the harmonic $m \cdot f_0$
C_{max}	maximum bit rate
C_{o}	parasitic capacitance between inner and outer conductor
C_{p}	package capacitance
D	diameter
$\vec{E}_{\varphi}, \vec{E}_{\vartheta}$	electric field components in $\vec{e}_{\varphi}$ and $\vec{e}_{\vartheta}$ directions
E_{inc}	electric field of the incident electromagnetic wave
E_{ref}	electric field of the reflected electromagnetic wave
F_c	forward-bias depletion capacitance coefficient
G	non-linear diode conductance
G_{D}	diode conductance in frequency-domain
G_{R}	receiver antenna gain
G_{T}	transmitter antenna gain
I_m^*	conjugate complex current phasor of the order m
I_s	diode saturation current
K	number of resonant circuit
L	inductance
L_{m}	inductance of the resonant circuit with resonance at the harmonic $m \cdot f_0$
M	grading coefficient
N	number of diodes

N_P	number of digital output ports
P	power
P_a	available power
P_b	junction built-in potential
P_D	power loss in the diode
P_{max}	maximum power
$P_{min,int}$	minimum power at the interrogator
$P_{min,tag}$	minimum power at the tag
P_R	power loss in the resistance R
Q	total charge in the diode
R	load resistance
R_a	antenna resistance at the fundamental frequency
R_{ant}	antenna resistance
$R_{a,opt}$	optimal antenna resistance
$R_{\eta_{max}}$	load resistance with maximum efficiency
R_{fwd}	forward-link-limited range
R_{mod}	modulator resistance
R_{opt}	optimal rectifier load resistance
$R_{\mu C}$	microcontroller resistance
R_N	rectifier input resistance
$R_{N,opt}$	optimal rectifier input resistance
R_P	load resistance of the output port
$R_{P_{max}}$	resistance with maximum power
R_{rev}	reverse-link-limited range
R_s	diode path resistance
R_{them}	thermistor resistance
R_0	constant resistance
S	scattering matrix
S_m	measured scattering matrix
T	absolute temperature
T_0	signal period
T_b	power reflection coefficient
T_{cycle}	instruction cycle time
Tt	transit time
V'	DC voltage loss
V_0	AC source voltage amplitude
V_{AC}	AC voltage amplitude
V_{Cc}	DC voltage across a circuit capacitance

V_D	DC voltage across the diode
V_{DC}	DC voltage amplitude
V_{DD}	DC supply voltage of the microcontroller
V_j	junction built-in potential
V_m	conjugate complex voltage phasor of the order m
$V_{0,ref}$	reference magnitude of the AC source voltage
V_{osc}	demodulated ASK signal
V_P	output port potential
V_s	voltage amplitude of the AC source in the Thevenin model
V_T	thermal voltage
V_{th}	threshold voltage
X_a	antenna reactance
$X_{a,opt}$	optimal antenna reactance
X_N	rectifier input reactance
$X_{N,opt}$	optimal rectifier input reactance
Y_D	diode admittance
Z_a	antenna impedance at the fundamental frequency
Z_{ant}	antenna impedance
Z_{Cc}	impedance of the circuit capacitance
Z_d	differential impedance
Z_N	rectifier input impedance
Z_0, Z_{ref}	reference impedance

α, α'	tangent slope
α_h	horizontal 3 dB beam width
α_T	thermistor temperature coefficient
α_v	vertical 3 dB beam width
β, β'	y-intercept of the tangent
φ_0	phase of the electromagnetic wave
φ_Γ	phase of the reflection coefficient
γ	propagation constant
ε_r	dielectric constant
η	efficiency
η_{ov}	overall efficiency
λ	wavelength
λ_0	wavelength in vacuum
λ_{WG}	waveguide wavelength

μ_r	relative permeability
φ_Γ	reflection coefficient phase
Γ	reflection coefficient
ω_0	fundamental angular frequency

Acronyms

ABS	Acrylonitrile Butadiene Styrene
AC	Alternating Current
ADC	Analog-to-Digital Converter
ADS	Advanced Design System
ASK	Amplitude Shift Keying
BJT	Bipolar Junction Transistor
BPSK	Binary Phase Shift Keying
CAD	Computer Aided Design
DC	Direct Current
EIRP	Equivalent Isotropic Radiated Power
ERP	Equivalent Radiated Power
FET	Field Effect Transistor
FR4	Flame Retardant 4
FSL	Free-Space Loss
GaAs	Gallium Arsenide
GaAsP	Gallium Arsenide Phosphide
GaP	Gallium Phosphide
Ge	Germanium
GP	General Port
HB	Harmonic Balance
HFSS	High Frequency Structural Simulator
IEC	International Electrotechnical Commission
ISM	Industrial, Scientific, and Medical
ISO	International Standard Organization
LF	Low Frequency
LSSP	Large Signal S-Parameters
OOK	On-Off Keying
PC	Polycarbonate
PIN	Positive Intrinsic Negative
PMMA	Polymethylmethacrylate
PTFE	Polytetrafluoroethylene
RF	Radiofrequency
RFID	Radiofrequency Identification
Se	Selenium
Si	Silicon
SMD	Surface Mounted Device
SNR	Signal-to-Noise Ratio
SOD	Small-Outline Diode
SOIC	Small-Outline Integrated Circuit

TE	Transversal Electric
TM	Transversal Magnetic
TEM	Transversal Electromagnetic
Tr	Transponder
UHF	Ultra High Frequency
VNA	Vector Network Analyzer

Mathematical functions and symbols

$\| \|$	magnitude
Δ	difference
j	imaginary number
I_m	modified Bessel function of the first kind of the order m
log	logarithm to the base 10
log_2	logarithm to the base 2
$\Im$	imaginary part
$\Re$	real part
arctan	arctangent
cos	cosine
sin	sine
tan	tangent

1 INTRODUCTION

In the last decade, wireless applications and especially Radio Frequency Identification (RFID) or remote sensing became attractive in industrial areas since the non-use of cables makes the data transfer more comfortable and reduces the time-consuming hardware maintenance. The common use of RFID tags for items identification in production and trading phase illustrates the advantages of this data communication concept, where the tags are usually mounted on or near to the surface of the objects to be identified [6].

1.1 MOTIVATION

In the future, the wireless identification concept of items by means of radio frequencies will be extended to monitor the production and the conditions of a product from the first production step till the end of its lifecycle. For this purpose, it is proposed that one or many tags will be assigned to the row product at the beginning of the production [14]. Once the product is designed, the CAD data, the identification numbers of machine tools supposed to achieve the required machining processes as well as the order of the processes are stored into the tag. By each production phase, the tags will collect, process, and communicate information for identification, automatic routing in the production area, quality control, real time control of machining accuracy, machining priority grade in case of components collision at machine-tools, etc.

Before going on the market, CAD data and further confidential design and production information will be erased from the tag memories. On the market, the tag will communicate information for purpose of optimal storing condition and trading the product.
After the selling of the product, the client can write own specific information such as date and place of acquisition, of mounting, etc. By means of incorporated sensors, the tag will be able to store information about the occurring operation conditions during the whole item lifecycle, or a user can transmit or retrieve data, for instance during maintenance duties.
At the end of the product lifecycle, the product transmits data to an operator about dissembling constraints to be observed for security and/or environment safety. Then it can be properly recycled, whereby the information about operation conditions stored

during the lifecycle is wirelessly retrieved by an operator. It is analyzed by the product development team, and is correlated to the end state of the product.

Considering several identical items, some mechanical, electrical, thermal or other weaknesses of the actual components generation can be statistically obtained, permitting the design of a next and more resistant generation of components.
This conciliation of intelligent and genetic capabilities in a component has been labeled as *gentelligence* [15]. Contrary to common tasks achieved by RFID tags where a machine program is activated by a specific word sent by an interrogator, the gentelligent tags need enhanced and more flexible functionalities [48]: in addition to the identification number transmission, the self-calculation of routes through the factory, the recognition of machine-tools and wireless duty assignment during the machining preparation, the real-time monitoring of machining processes, the evaluation of machining process qualities, the storing of operating conditions, the processing of maintenance data, and finally, the measurement of operation time require incorporated memories, sensors and a microcontroller as core of the transponder circuit.

The environment in industrial areas like machines construction factories is well known as particularly harsh. Hence, it is proposed to integrate the tag electronic circuitry inside the components to avoid mechanic damages. Another reason for the electronic work pieces identification and for the integration is the plagiary protection: own authentication and encryption methods, specific communication protocols for data interchange, and hiding the electronic circuitry under the components surface should minimize significantly risks of work piece counterfeiting and falsification of manufacturer name and country of origin [32].

However, a major challenge arises when the product to be identified is metallic because of the reflecting metallic surfaces which do not permit the easy propagation of electromagnetic waves from the surrounding environment to the inner of the object where the electronic communication system is to place. The expected low available power requires substantial knowledge on rectifier design techniques to maximize the energy conversion to supply the transponder and consequently to enhance the communication range. This makes the integration of wireless microwave communication modules inside the component be a challenging task.

1.2 STATE OF THE ART

Diverse mathematical analyses of voltage multiplying circuits are proposed in the literature. Most of them describe the diodes in rectifiers as short circuit [10] or as ideal DC voltage source [7]. It should be clear that many research works based their investigation on simulated or measured curves of specific circuits [66, 67], and interpolate or extrapolate the results to estimate the behavior of new configurations. Such empirical or semi-empirical data may be sufficient for a rough understanding of rectification processes and for the prediction of the rectified voltage range, but they do not offer possibilities for the improvement of the AC-to-DC conversion, since whether the diode parameters nor the circuit topology are accurately or analytically considered.

However, some works take into account diode SPICE parameters [2, 12, 63], but they neglect important parameters like the breakdown voltage and the ideality factor. Furthermore, only one rectifier topology, the Dickson charge pump is largely discussed, disabling helpful comparisons with other rectifier topologies.

Almost all reported transponders are realized as integrated circuits [49]. They use backscatter modulators which are mostly located at the interface between the antenna and the rectifier and consist on more or less complex CMOS circuits [3, 11, 29, 56, 57]. Such implementations are not suitable for experimental designs using only discrete components, since the required place would be too large for the integration in small objects. At last, field-powered transponders operating in frequency ranges higher than the 2.45 GHz ISM band are not state-of-the-art at this day, especially because the ISO/IEC 18000-5 standard, which defines air interface for RFID operating in the 5.8 GHz ISM band, has been withdrawn due to the lack of global interest [17, 33].

For identification or monitoring, objects are usually tagged with one or more transponders placed on the object surface. In case of metallic objects, UHF transponders are applied on a thick substrate mounted on the object surface to avoid critical tag detuning [5]. In [5], it is also proposed to realize an indentation that acts as dwell place for the transponder. The first and the second solution do not offer mechanical safety for the circuit. In the third solution, the tag detuning is so high, that the data transmission is achievable only for very short communication ranges. Furthermore, the evenness of the object surface gets lost in the second and third solution.

1.3 FRAME AND STRUCTURE OF THE WORK

This work presents a systematic and accurate design methodology and analysis of voltage multiplying circuits using diodes. Furthermore, a novel implementation of backscatter modulation and a novel approach for the integration of transponders into metallic objects are treated. The work is subdivided in five main parts.

In the first part, that is Chapter 2, the focus is set on an accurate formulation of the rectified output voltage. An enhanced mathematical DC analysis based on time-domain equations is done for three rectifier topologies: the Cockcroft-Walton rectifier, the Dickson charge pump and the Greinacher rectifier. The diodes are described by means of the saturation current, the ideality factor, the path resistance and the breakdown voltage. The consideration of all these parameters makes the analysis results more accurate than those proposed in the literature. The diode or circuit properties leading to the maximization of the rectified voltage, of the output power and of the AC-to-DC conversion efficiency are extracted from the mathematical analysis.

In Chapter 3, further diode SPICE parameters, namely the zero bias capacitance, the forward-bias depletion capacitance coefficient, the junction built-in potential and the grading coefficient are taken into account to describe the diode capacitance. Therewith the input impedance of the above circuits is analyzed by means of time-domain and frequency-domain equations. The developed system of equations gives a novel and

accurate description of the rectifier performances, as well as the understanding of the effect of each diode or circuit parameter on the entire system behavior. Criteria to maximize the achieved rectified voltage or the conversion efficiency are extracted from the analysis of two particular circuits and are generalized.

Chapter 4 treats the analysis and the realization of a novel backscatter concept using discrete components. The antenna impedance is considered to be time constant, while the circuit input impedance is varied electronically. The conditions for the realization of digital amplitude and phase modulation by tuning the rectifier load resistance are investigated using the results from the previous chapters.

A method for the integration of passive transponders into metallic objects, and particularly the design and the characterization of a suitable antenna, is the object of Chapter 5. A novel waveguide-to-planar transition is introduced. The impedance control and the radiation properties of the resulting waveguide antenna are presented.

The practical design and realization of a 5.8 GHz ISM band transponder integrated in a gear box cover are the topics of Chapter 6. The choice of electronic devices and the selected circuit topology are discussed. The simulation steps using the software ADS and HFSS are detailed, and realized transponders performing identification and sensing tasks are presented.

A conclusion closes this work.

2 DC ANALYSIS

As introduced in Section 1.3, an enhanced analysis of rectifiers is set as the first stage of the transponder design. Rectification is the conversion of alternating current (AC) to direct current (DC). This technique is widely used to supply DC power to electrical systems. Because rectifiers usually include devices that allow current to flow in only one direction, most of them use diodes as asymmetric devices.

2.1 BASICS ON VOLTAGE RECTIFIERS

One distinguishes half-wave rectifiers and full-wave rectifiers. In a half-wave rectifier, only half the wave of the input voltage v_0 is used to generate the rectified output voltage v_{out}. The simplest half-wave rectifier consists of one diode in series with the AC voltage source, as depicted in Figure 2.1 (a) [66].
A full-wave rectifier uses both half-waves of the AC input voltage to generate a rectified voltage at the circuit output. A common topology is the so-called bridge rectifier including four diodes, as shown in Figure 2.1 (b) [39].

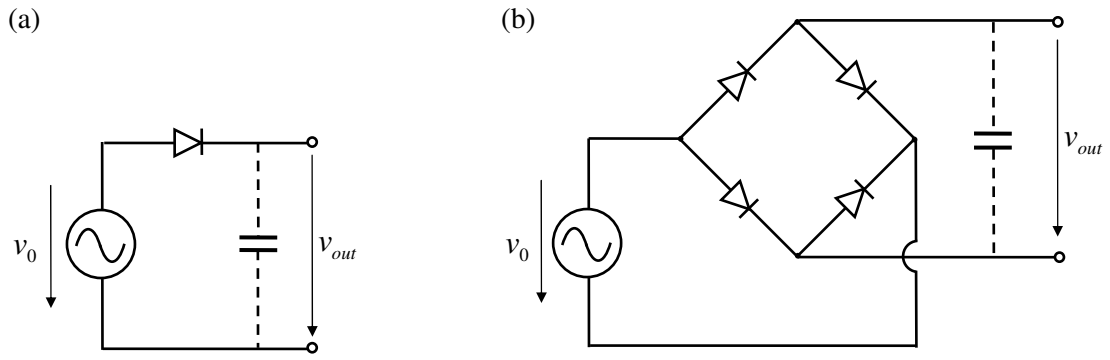


Figure 2.1: (a) Half-wave and (b) full-wave rectifiers.

The output voltage is a series of positive half-waves, as depicted in Figure 2.2. In the ideal case, each diode act as short-circuit in the forward bias and as open circuit in the

reverse bias. Then the maximum output voltage $V_{out,max}$ is equal to the source voltage amplitude V_0:

$$V_{out,max} = V_0 \,. \tag{2.1}$$

To convert the positive half-waves into a DC voltage, a smooth-capacitor is added in parallel to the circuit output. The larger its capacitance, the smoother the output voltage shape. If one assumes that the diodes are ideal, then in the case where the capacitance is so large that the rate of discharge at the output is much smaller than the period of the voltage source, then the output voltage is the same for both the half-wave rectifier and the full-wave rectifier, and is equal to the source voltage amplitude [10]:

$$V_{out} = V_0 \,. \tag{2.2}$$

Figure 2.2 shows the result of the transient simulation of a rectification process using a half-wave and a full-wave rectifier [57].

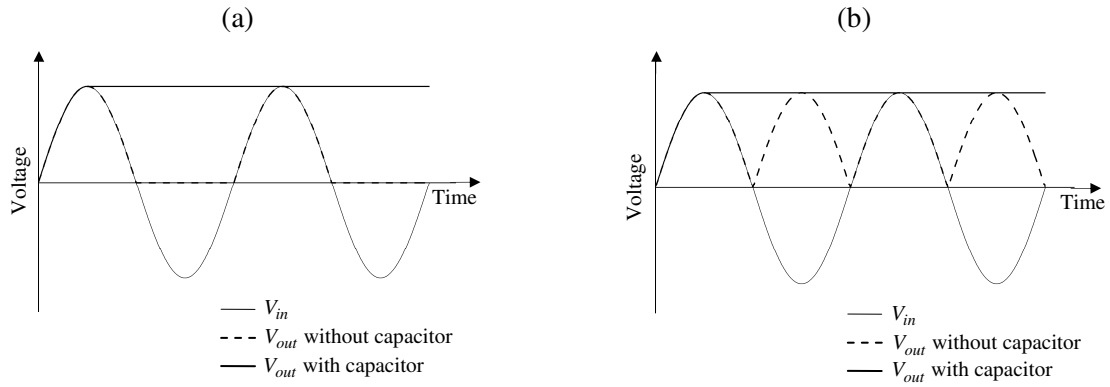


Figure 2.2: (a) Half-wave and (b) full-wave rectifier.

For non-ideal diodes, a voltage drop arises across the diodes. If V_D is the maximum voltage drop for each diode during the forward bias half-wave and assuming a large smooth-capacitance, then the output voltage is obtained as

$$V_{out} = V_0 - V_D \tag{2.3}$$

for the half-wave rectifier, and as

$$V_{out} = V_0 - 2V_D \tag{2.4}$$

for the full-wave rectifier [7]. The value of V_D depends mainly on the diode properties and the output load resistance.

2.2 VOLTAGE MULTIPLYING RECTIFIERS

Rectifiers are often configured as cascaded diode-capacitor stages to provide a DC output voltage that is higher than the AC source voltage amplitude. In a general manner, the higher the number of stages, the higher the open circuit DC output voltage. For ideal diodes and large smooth-capacitances, the number of diodes N determines the voltage multiplication factor, thus the following rough assumption is often accepted:

$$V_{out} = N \cdot V_0 . \tag{2.5}$$

A common voltage multiplying rectifier is the Cockcroft-Walton circuit, depicted in Figure 2.3 (a) and Figure 2.3 (b) for odd and even numbers of stages, respectively, where v_R represents the voltage at the output load resistor R [63].

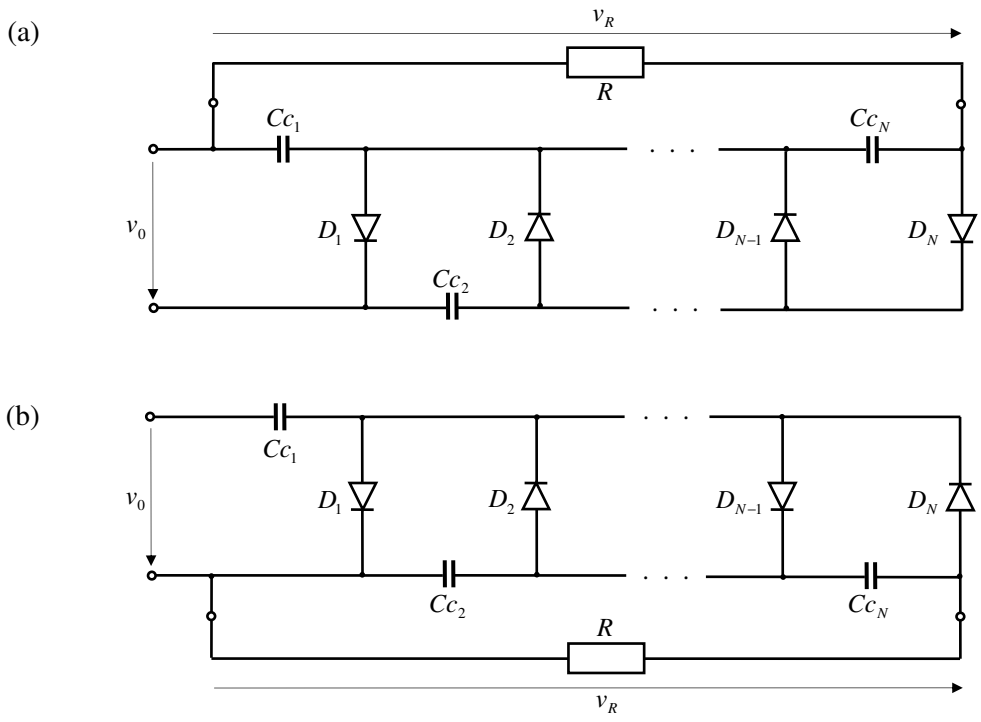


Figure 2.3: Cockcroft-Walton rectifier with (a) odd and (b) even numbers of stages.

The Dickson charge pump depicted in Figure 2.4 (a) is probably the most cited voltage multiplying rectifier in the literature [29, 56]. The main difference between the Cockcroft-Walton rectifier and the Dickson charge pump is that the latter requires an even number of diodes.

The full-wave Greinacher rectifier depicted in its modified form in Figure 2.4 (b) consists of two identical Dickson charge pumps and provides a differential output. Due to its configuration, the number N is always a multiple of four.

The choice of the rectifier topology will thus essentially decide on the required number of diodes. This might have considerable financial implications, especially in the case of mass production of discrete circuits, where the price of each device affects the cost of the whole system significantly.

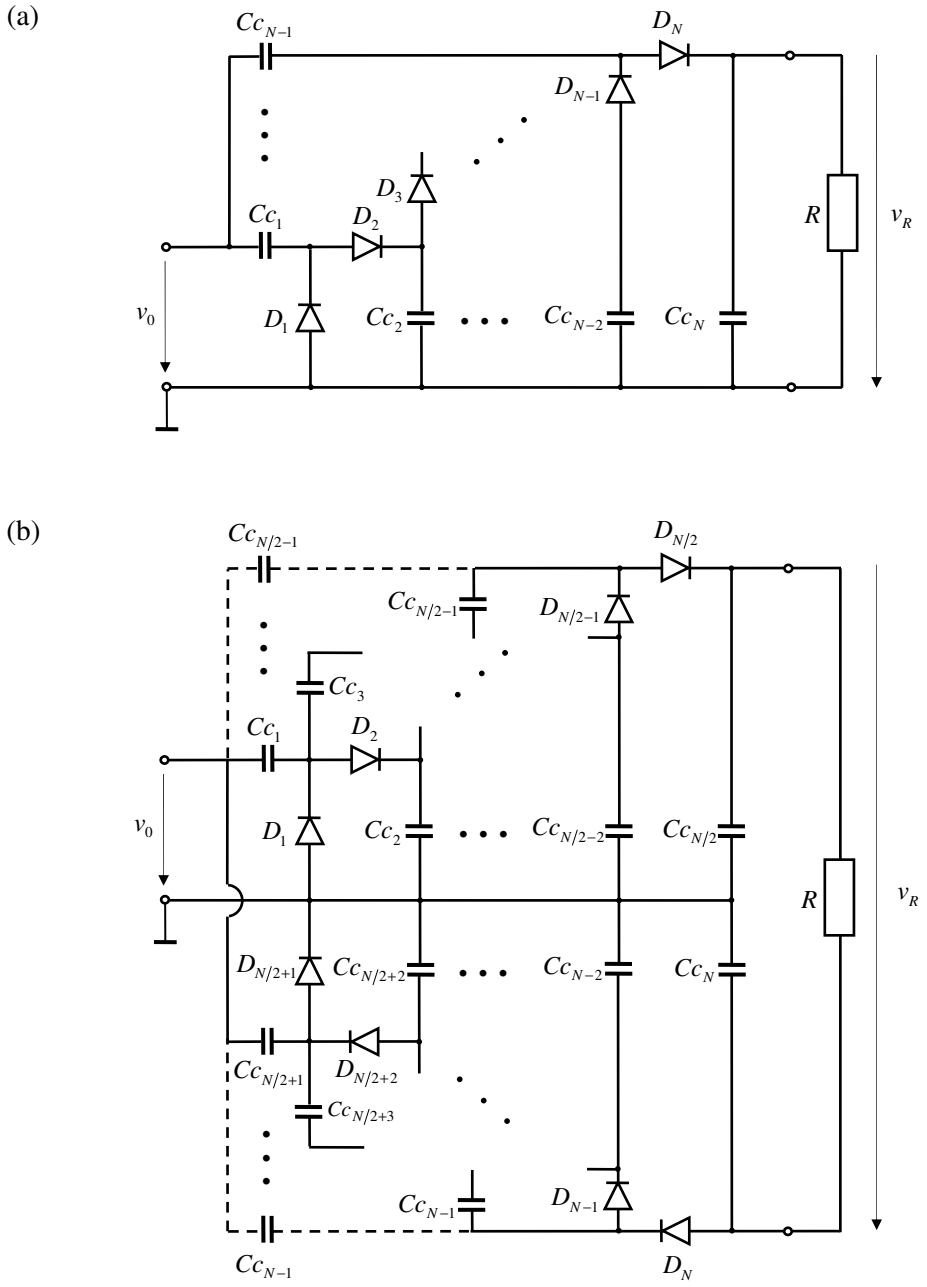


Figure 2.4: (a) Dickson charge pump; (b) Full-wave (modified) Greinacher rectifier.

For non-ideal diodes, the DC output voltage is usually given as

$$v_R = N \cdot V_0 - V', \tag{2.6}$$

where V' depends on N, V_0, R, as well as on the diodes properties [33]. For an efficient rectifier design, an analytic methodology taking into account the diodes properties should be used. As mentioned in Section 1.2, the diodes or transistors [36] working as rectifying devices are often modeled as constant voltage sources or short circuits for steady state analysis. Several works base their designs on heuristics or previous measurements. The use of such empirical design methods is due to the nonlinearity of the rectifying circuits, which requires numerical solving algorithms and does not allow mathematical solutions in comfortable and compact expressions. In the following sections of this chapter, an approach based on time-domain analysis of voltage multiplying rectifiers will be developed and the effects of diode and circuit parameters will be analyzed. Criteria to maximize the AC-to-DC conversion will then be deduced.

2.3 CIRCUIT ANALYSIS

To analyze the rectifier circuits, it is helpful to make some assumptions about the diodes properties. Each diode has been modeled as the parallel circuit of a non-linear conductance G and a capacitance C, as shown in Figure 2.5 [35].

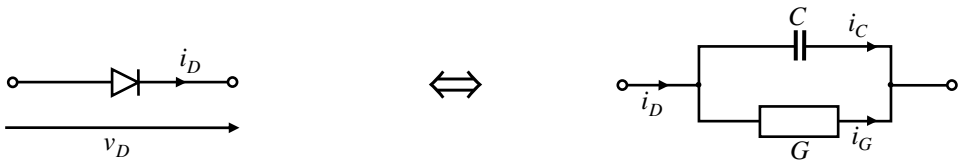


Figure 2.5: Simplified diode equivalent circuit.

The current-voltage characteristic of the diode conductance is given by the function h as [35, 43]

$$i_G = h(v_D) = I_s\left(e^{\frac{v_D}{nV_T}} - 1\right), \tag{2.7}$$

where i_G is the current through the conductance, I_s the diode saturation current, v_D the diode voltage, n the ideality factor or emission coefficient, and V_T the thermal voltage defined by the Einstein relation as

$$V_T = \frac{kT}{q}. \tag{2.8}$$

In (2.8), k is the Boltzmann constant, T the absolute temperature and q the elementary charge. Figure 2.6 displays a typical diode current-voltage characteristic according to (2.7).

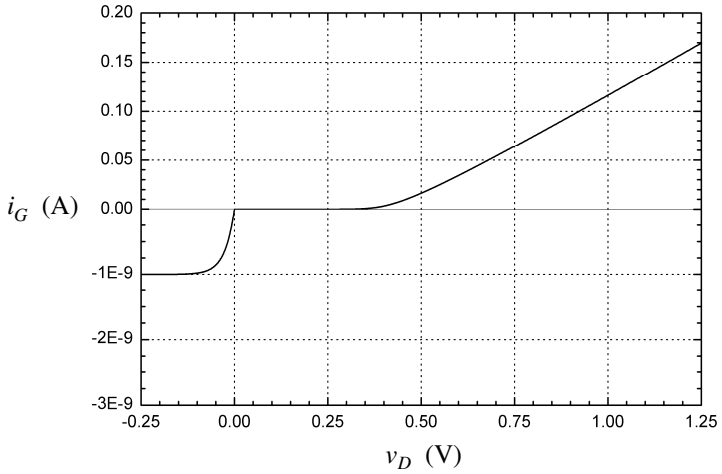


Figure 2.6: Typical diode current-voltage characteristic.

The diode capacitance C depicted in Figure 2.5 is the sum of the diffusion capacitance C_{dif} and the depletion zone capacitance C_{dep}. For discrete devices, the package capacitance C_p should also be taken into account to compute the value of C. Although both the diffusion and the depletion zone capacitances are non-linear [50], C is considered as voltage independent in this stage of the analysis. This assumption will allow a straightforward analysis permitting a basic understanding of the influence of the aforementioned diode parameters, without causing accuracy losses in the results.
Using the diode equivalent circuit depicted in Figure 2.5, the single-stage and two-stage diode rectifiers shown in Figure 2.7 (a) and Figure 2.7 (b), respectively, are analyzed. Each circuit feeds a load resistance R and is excited by an ideal AC voltage source which provides the voltage

$$v_0 = V_0 \cos(\omega_0 t), \tag{2.9}$$

where V_0 is the voltage amplitude, ω_0 is the excitation angular frequency, and t is the time. The single-stage circuit is usually expected to provide an output DC voltage almost equal to the AC source voltage amplitude V_0, while the two-stage circuit, also called voltage doubler, is expected to deliver almost twice this amplitude [52].

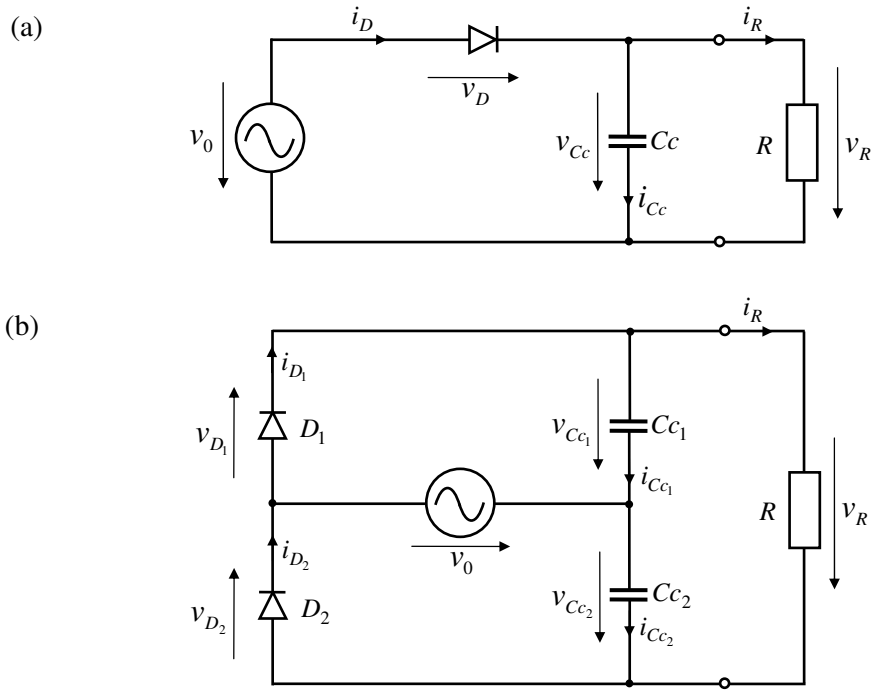


Figure 2.7: (a) Single-stage rectifier; (b) voltage doubler.

2.3.1 SINGLE-STAGE RECTIFIER

For Figure 2.7 (a), the Kirchhoff voltage and current laws are:

$$v_0 - v_D - v_R = 0\,, \tag{2.10}$$

$$i_D - i_{Cc} - i_R = 0\,. \tag{2.11}$$

By using (2.7) and (2.10), a developed form of (2.11) is obtained as:

$$I_s\left(e^{\frac{v_0 - v_R}{nV_T}} - 1\right) + C\frac{d\left(v_0 - v_R\right)}{dt} - Cc\frac{dv_R}{dt} - \frac{v_R}{R} = 0\,. \tag{2.12}$$

If one assumes that the rectified voltage v_R is time-invariant, then (2.12) can be written as

$$\begin{aligned} &I_s e^{\frac{-v_R}{nV_T}}\left[I_0\left(\frac{V_0}{nV_T}\right) - e^{\frac{v_R}{nV_T}} + 2\sum_{m=1}^{\infty} I_m\left(\frac{V_0}{nV_T}\right)cos\left(m\omega_0 t\right)\right]\,, \\ &-\omega_0 C V_0\, sin\left(\omega_0 t\right) - \frac{v_R}{R} = 0 \end{aligned} \tag{2.13}$$

where I_0 and I_m are the modified Bessel functions of the first kind and of order 0 and m,

respectively [39]. Considering only the time-invariant terms, (2.13) leads to the transcendent equation

$$\left(1+\frac{v_R}{RI_s}\right)e^{\frac{v_R}{nV_T}}-I_0\left(\frac{V_0}{nV_T}\right)=0\,, \tag{2.14}$$

which permits the calculation of the rectified DC output voltage v_R. Equation (2.14) can be graphically or numerically solved. The rectifier depicted in Figure 2.4 (a) has been analyzed with the simulation software ADS from Agilent Technologies. The AC source voltage frequency f_0 has been set to 1 MHz and the capacitance Cc to 50 nF. Figure 2.8 (a), Figure 2.8 (b) and Figure 2.8 (c) show that the simulation results agree very well with the developed equation and thus attest the correctness of (2.14).

Contrary to the common assumption expressed in (2.5), the achieved DC output voltage is definitely lower than the voltage source amplitude. Furthermore, it is shown that the diode parameters n and I_s, as well as the load resistance R affect the DC output voltage v_R, where the ideality factor n, which is a floating number between 1 and 2 [55], has a significant impact. On the other hand, the higher the value of I_s or R, the higher the voltage v_R.

The value of the capacitance Cc seems irrelevant due the assumption of a time constant v_R. This assumption is valid only if the charge and discharge of the capacitor occur slowly, which can be expressed by [63]

$$\omega_0 Cc >> \frac{1}{R}\,. \tag{2.15}$$

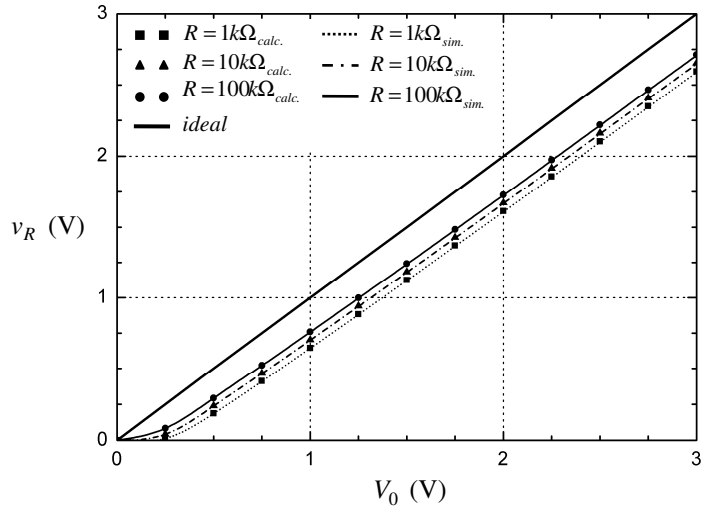
The diode capacitance C also does not seem to affect v_R. Its influence has been analyzed by means of simulations. Assuming that (2.15) holds, it has been observed that as long as the condition

$$\frac{C}{Cc} << 1 \tag{2.16}$$

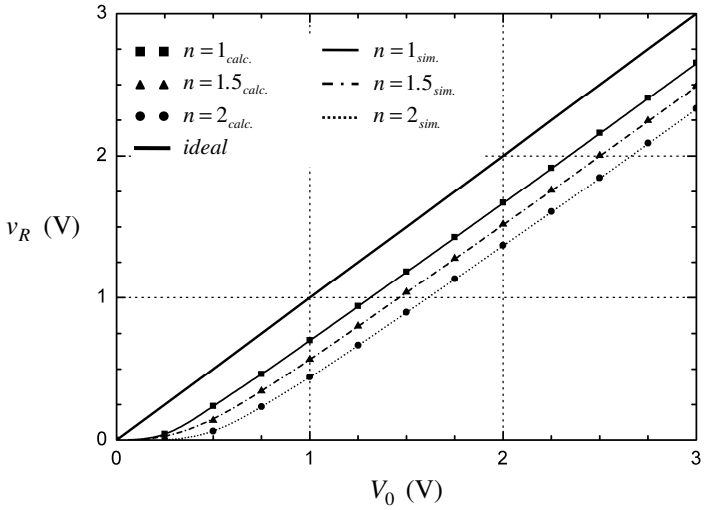
is met, the ripple of the voltage v_R is negligible. When the condition (2.16) is not met, the constant component of v_R, noted $v_{R,f=0Hz}$, is lower than the value given by (2.14) [7]. At the same time, the amplitude of the spectral component of v_R at the fundamental frequency, noted $\hat{v}_{R,f=f_0}$, increases, and thus the ripple of v_R increases. From Figure 2.9, a rough design rule to keep the ripple negligible can be extracted as

$$Cc \geq 100C\,. \tag{2.17}$$

(a)



(b)



(c)

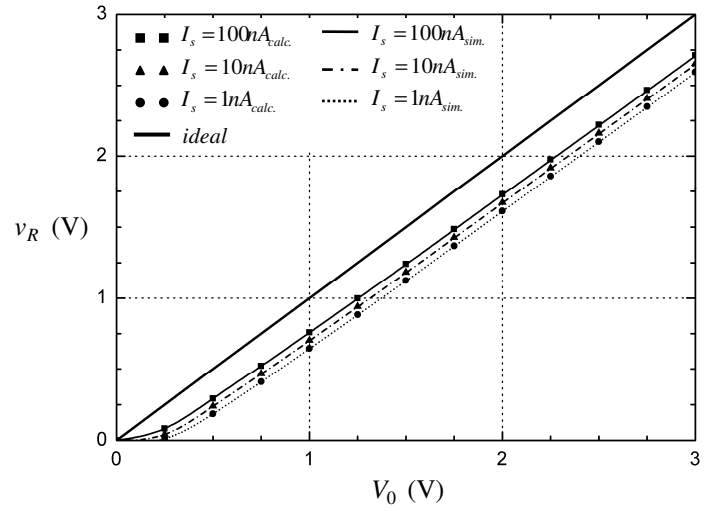


Figure 2.8: AC-to-DC conversion function for single-stage rectifier for different values of (a) R, (b) n and (c) I_s. The ideal conversion function $v_R = V_0$ is depicted for comparison.

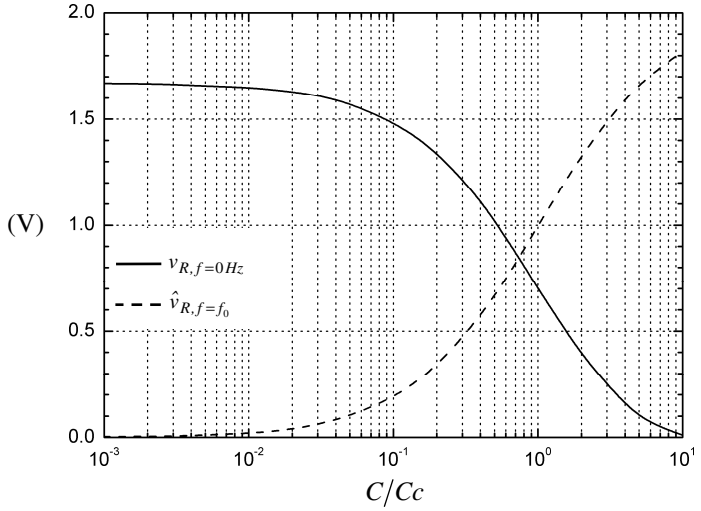


Figure 2.9: Simulated effects of the depletion zone capacitance for $V_0 = 2$ V, $R = 10$ kΩ, $I_s = 10$ nA, $n = 1$ and $f_0 = 1$ MHz.

2.3.2 DIODE PATH RESISTANCE

For a more accurate description of the real DC behavior of the circuit, the diode equivalent circuit of Figure 2.5 has been enhanced by adding the diode path resistance R_s (see Figure 2.10). In this case, (2.7) can be written as [8]

$$i_G = h(v_D) = I_s\left(e^{\frac{v_D - R_s i_G}{nV_T}} - 1\right). \tag{2.18}$$

The resistance R_s should reduce v_R since a part of the AC source voltage v_0 will drop on it. A mathematical expression for the resulting DC output voltage is not possible here due to the complexity of the problem and the fact that only numerical methods may be used to resolve (2.18). However, for low values of R_s, the equations developed above - especially (2.14) - are expected to remain valid. Figure 2.11 shows the simulated effect of R_s on the DC output voltage v_R. As expected, a slight drop of the achieved DC voltage appears for low values of R_s.

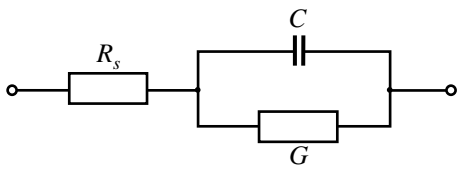


Figure 2.10: Enhanced diode equivalent circuit including the path resistance R_s.

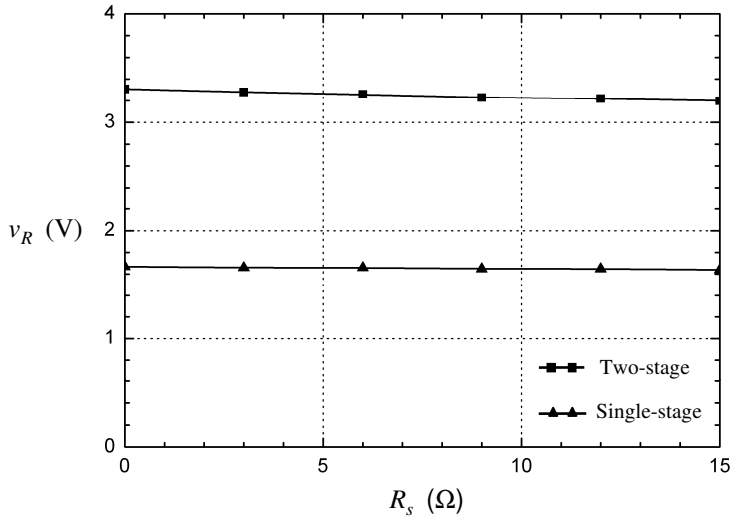


Figure 2.11: Simulated effects of the path resistance on the DC output voltage for $V_0 = 2$ V, $R = 10$ kΩ, $I_s = 10$ nA, $n = 1$, $C = 1$ pF, $Cc = 50$ nF and $f_0 = 1$ MHz.

2.3.3 VOLTAGE DOUBLER

The same procedure described in Subsection 2.3.1 is used to analyze the output of the voltage doubler depicted in Figure 2.7 (b). The Kirchhoff voltage and current laws are:

$$i_{D_1} - i_{Cc_1} - i_R = 0\,, \tag{2.19}$$

$$-i_{D_2} + i_{Cc_2} + i_R = 0\,, \tag{2.20}$$

$$v_0 - v_{Cc_1} - v_{D_1} = 0\,, \tag{2.21}$$

$$v_0 + v_{Cc_2} + v_{D_2} = 0\,. \tag{2.22}$$

If the rectified voltage v_R is assumed to be time-constant, then the symmetry of the circuit leads to

$$v_{Cc_1} \approx v_{Cc_2} \approx \frac{v_R}{2}\,. \tag{2.23}$$

Hence, putting (2.23) in (2.21) and (2.22), and using (2.7), the current laws (2.19) and (2.20) can be written respectively as follows:

$$C\frac{dv_0}{dt}+I_s\left(e^{\frac{v_0-\frac{v_R}{2}}{nV_T}}-1\right)-(C+Cc)\frac{dv_{Cc_1}}{dt}-\frac{v_R}{R}=0\,, \tag{2.24}$$

$$C\frac{dv_0}{dt}-I_s\left(e^{\frac{-v_0-\frac{v_R}{2}}{nV_T}}-1\right)+(C+Cc)\frac{dv_{Cc_2}}{dt}+\frac{v_R}{R}=0\,. \tag{2.25}$$

Developing the difference of (2.24) and (2.25) and setting

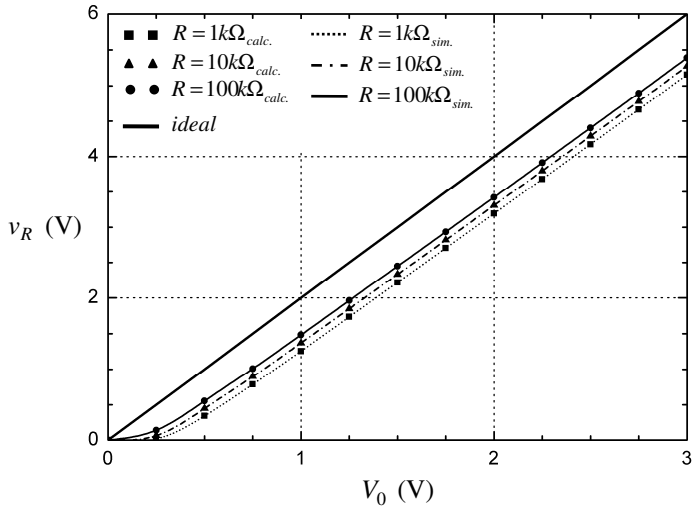
$$\frac{dv_{Cc_1}}{dt}+\frac{dv_{Cc_2}}{dt}=\frac{dv_R}{dt}\approx 0\,, \tag{2.26}$$

which means that the rectified voltage is almost time-invariant, and considering only time-invariant terms and using the same development as in (2.13), one obtains the transcendent equation for v_R as

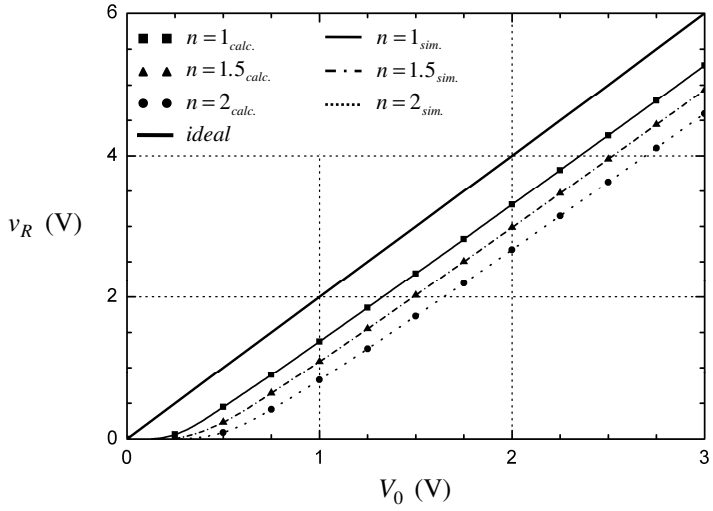
$$e^{\frac{v_R}{2nV_T}}\left(\frac{v_R}{RI_s}+1\right)-I_0\left(\frac{V_0}{nV_T}\right)=0\,. \tag{2.27}$$

The resulting AC-to-DC conversion function is depicted in Figure 2.12, where the good superposition of calculated and simulated results proves the correctness of the developed analytical expressions.
Even here, the achieved DC voltage is definitely lower than twice the AC source voltage amplitude, as assumed in (2.5). The influence of n, I_s, R, R_s and C on the achieved DC voltage is similar than in the case of a single-diode rectifier.

(a)



(b)



(c)

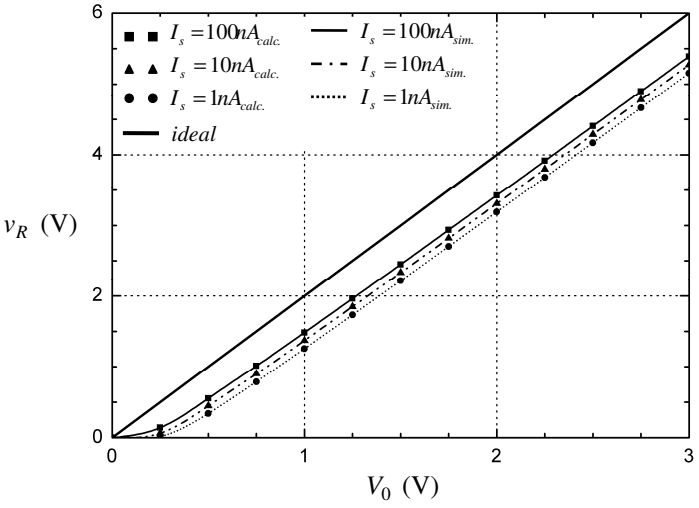


Figure 2.12 AC-to-DC conversion function for voltage doublers for different values of (a) R, (b) n and (c) I_s. The ideal conversion function $v_R = 2V_0$ is depicted for comparison.

2.4 DC ANALYSIS OF N-STAGE VOLTAGE MULTIPLYING RECTIFIERS

The complexity of the analytical determination of the AC-to-DC conversion function using the Kirchhoff laws rises with the number of diodes. A general equation of the conversion function is sought for a rectifier consisting of N diodes and capacitors. Looking at the DC output voltage equation for the single-stage rectifier and the voltage doubler given in (2.14) and (2.27), respectively, one sees that the only difference appears in the denominator of the exponential function argument: it is nV_T for the single-stage rectifier, and $2nV_T$ for the voltage doubler. Therefore, assuming identical diodes and capacitors ($Cc = Cc_1 = Cc_2 = \cdots = Cc_N$), the equation for the DC output voltage for a voltage multiplying rectifier consisting of N diode-capacitor stages (or simply N diode stages) is expected to be

$$e^{\frac{v_R}{NnV_T}}\left(\frac{v_R}{RI_s}+1\right)-I_0\left(\frac{V_0}{nV_T}\right)=0\,, \tag{2.28}$$

where N appears in the denominator of the exponential function argument. Both the Cockcroft-Walton rectifier and the Dickson charge pump will be analyzed in order to prove the proposed formula.

2.4.1 COCKCROFT-WALTON RECTIFIER

The current i_R flowing through the load resistance R and assumed to have only a DC component, flows entirely through the diode D_N, since the capacitor Cc_N (see Figure 2.3 (a)) acts as DC block, as depicted in Figure 2.13.

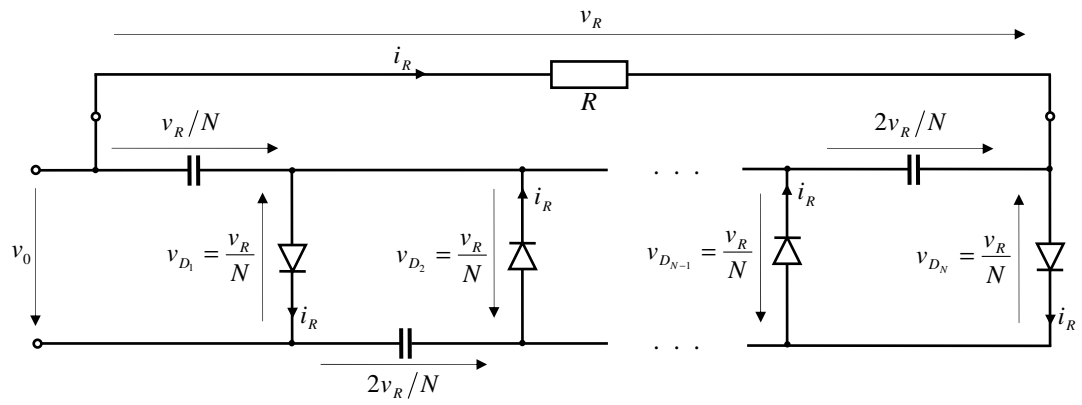


Figure 2.13: DC analysis of a Cockcroft-Walton rectifier.

Consequently, i_R is the DC current through D_{N-1}, D_{N-2}, …, and at last through D_1:

$$i_R = I_{D_N} = I_{D_{N-1}} = \cdots = I_{D_1} = \frac{v_R}{R}. \tag{2.29}$$

On the other hand, considering only the DC voltages at the diodes, then:

$$v_R = \sum_{i=1}^{N} V_{D_i}, \tag{2.30}$$

where V_{D_i} is the DC component of the voltage v_{D_i} at the diode D_i. Furthermore, since all diodes are assumed to be identical, then:

$$V_{D_1} = V_{D_2} = \cdots = V_{D_N} = \frac{v_R}{N}. \tag{2.31}$$

Considering (2.29), (2.30), and (2.31), the diodes can be viewed as the equivalent series circuit of N identical DC voltage sources feeding the load resistance R as depicted in Figure 2.14. Here, each diode provides the DC voltage v_R/N. It is important to note that all diodes are reverse-biased.

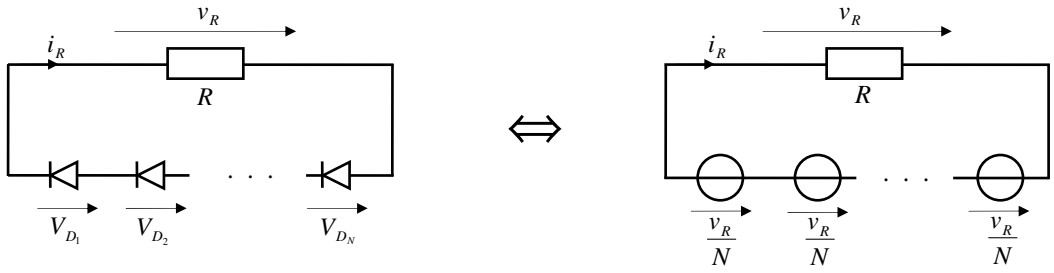


Figure 2.14: Equivalent DC circuit of a Cockcroft-Walton rectifier.

The Kirchhoff voltage law at the rectifier input is

$$v_0 - v_{Cc_1} - v_{D_1} = 0. \tag{2.32}$$

The source voltage v_0 is sinusoidal and thus has no DC component. Since for a large capacitance Cc, v_{Cc_1} is almost time-invariant, then one can write (2.32) using (2.31) as:

$$v_{Cc_1} = V_{D_1} = \frac{v_R}{N}. \tag{2.33}$$

Furthermore, the total current i_{D_1} through the diode D_1 is the sum of its AC and DC

components, and can be expressed using (2.7), (2.32) and (2.33) as

$$i_{D_1} = C\frac{d}{dt}\left(v_0 - \frac{v_R}{N}\right) + h\left(v_0 - \frac{v_R}{N}\right). \tag{2.34}$$

Developing (2.34) similarly to (2.13) and setting the resulting DC current component equal to I_{D_1} obtained in (2.29), one obtains the expression proposed in (2.28). The validity of (2.28) for Cockcroft-Walton rectifiers with an even number of stages can be proved using the same method. It should be noted that the AC-to-DC conversion function does not include the frequency of the AC source voltage.

2.4.2 DICKSON CHARGE PUMP

The analysis of the Dickson charge pump depicted in Figure 2.4 (a) is done hereunder with the help of Figure 2.15.

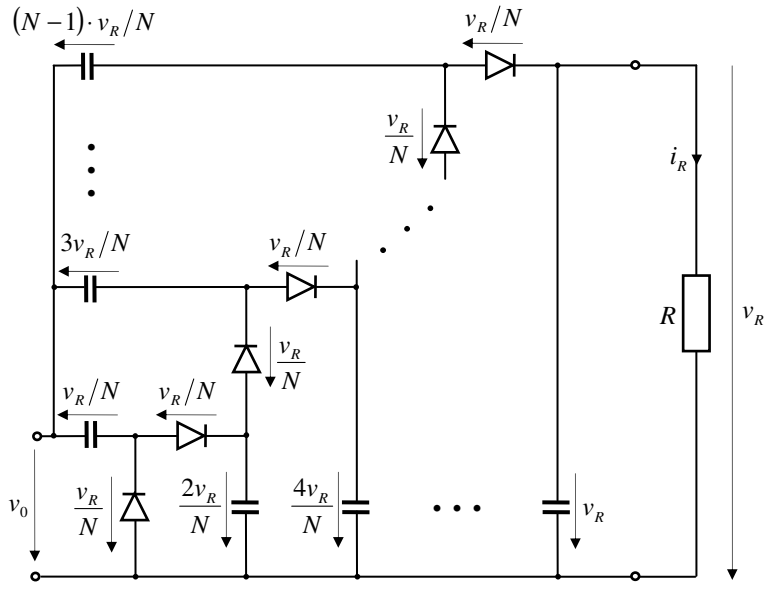


Figure 2.15: DC Analysis of the Dickson charge pump.

A DC voltage is assumed at the load resistance. The resistance current $i_R = v_R/R$ is the DC current flowing through each diode, since the circuit capacitors act as DC blocks. Furthermore, all diodes are assumed identical, hence they can be considered as a series circuit of identical DC voltage sources. The diode DC model depicted in Figure 2.14 can then also be used in this case. To determine the rectified voltage v_R, the Kirchhoff voltage law can be applied to the loop consisting of the AC voltage source, the circuit capacitor Cc_1 and the diode D_1, similarly to (2.32). As it was previously done, the voltage at the capacitance Cc_1 can be assumed to be time-constant for large values of

Cc. Hence, the relation given by (2.33) is valid. Therewith the differential equation (2.34) describes the current through the diode D_1 and leads to the voltage v_R expressed in (2.28). Equation (2.28) is an enhanced formulation of the expression proposed in [12], where the SPICE parameter n is not considered. Dickson charge pumps including up to six diodes have been simulated. The good agreement between the calculated and simulated v_R shown in Figure 2.16 validates the developed formula.

For the Greinacher rectifier or its modified form, the determination of the DC output voltage can be done in the same manner, leading to (2.28). Hence, Cockcroft-Walton rectifiers, Dickson charge pumps and Greinacher rectifiers achieve the same AC-to-DC conversion function if they use the same number and type of diodes.

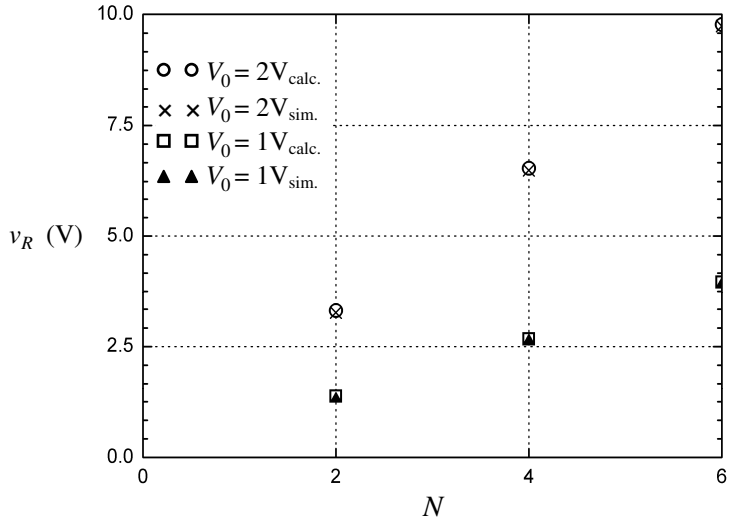


Figure 2.16: Achieved DC voltage of Dickson charge pumps, where $R = 10\,\text{k}\Omega$, $R_s = 0\,\Omega$, $I_s = 10\,\text{nA}$, $n = 1$, $C = 1\,\text{pF}$, $Cc = 50\,\text{nF}$ and $f_0 = 1\,\text{MHz}$.

2.4.3 CIRCUIT CAPACITORS

The voltages across the circuit capacitors depend on the rectifier topology and are examined in this subsection.
For Cockroft-Walton rectifiers, one can conclude using Figure 2.13, that

$$v_{Cc_i} = \begin{cases} \dfrac{v_R}{N} & \text{for } i = 1 \\ \dfrac{2v_R}{N} & \text{for } 1 < i \le N \end{cases}. \tag{2.35}$$

Hence, except for the capacitance Cc_1, all capacitances have the same DC voltage. This might be an advantage because it simplifies the design (by integrated circuits) or the choice (by discrete circuits) of the capacitors: the circuit capacitors have already been

assumed identical from the point of view of their capacitance. Now, they can be assumed identical from the point of view of their electric strength. Therefore the same design, technology, or type can be used for all capacitances.
For Dickson charge pumps, one deduces from Figure 2.15 that

$$v_{Cc_i} = i\frac{v_R}{N}. \tag{2.36}$$

The higher the subscript i, the higher the voltage across the corresponding capacitor Cc_i. This makes designing these voltage multiplying rectifiers challenging for high input voltage amplitude or for a high number of diodes, because the capacitors, which typically use the same type or the same technology, must be able to keep a constant behavior over a large voltage dynamic. Figure 2.17 illustrates (2.35) and (2.36).

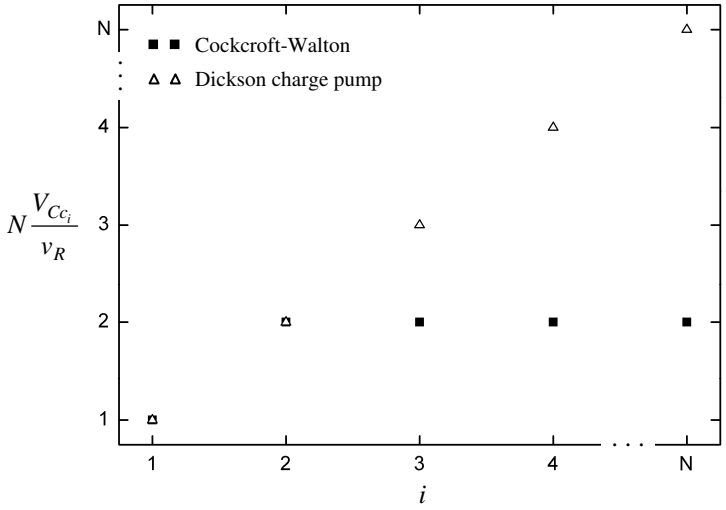


Figure 2.17: DC voltage at the circuit capacitors.

2.5 DIODE TECHNOLOGY

The choice of the diode type and thus the diode technology is critical when designing rectifiers. In Figure 2.8 and Figure 2.12, the effects of two diode SPICE parameters on the rectified voltage have been observed. The physical and technological reasons for this behavior will be presented. Furthermore, diodes are suitable for proper voltage rectification if additional factors are taken into account. In the following subsections, device technologies will be discussed and favorable requirements will be extracted.

2.5.1 COMPARISON BETWEEN SCHOTTKY DIODES AND P-N JUNCTIONS

Although the choice of diode type for device applications is usually dictated by purely

technological considerations, it sometimes happens that both of them are technologically realizable, and in such cases, the choice is made based on their electrical properties. Here, a brief comparison of Schottky diodes and p-n junctions is presented for two major factors: the transient response and the saturation current density.

2.5.1.1 TRANSIENT BEHAVIOR

In p-n junctions, minority carriers injected across the junction in forward bias must be removed before the current can reach a new steady-state value after the bias is reversed. This process controls the high-frequency limit of operation of system components such as rectifiers and mixers.
The transient response of a Schottky diode is determined by its equivalent circuit, which consists of the depletion capacitance C_{dep} in parallel with a conductance arising from the current transport mechanisms occurring at the metal-semiconductor or Schottky barrier. This parallel combination is in series with a path resistance R_s. In all practical cases, the pulse or high-frequency response of a Schottky diode is determined by the time constant R_sC, where C is the total differential capacitance of the Schottky diode, including both the depletion and the diffusion capacitances. However, for Schottky diodes, the diffusion capacitance is negligible and thus C is almost equal to C_{dep}. The resulting low values for C lead to time constants in the order of picoseconds for typical silicon mixer diodes [44]. These time constants are short enough for microwave applications. In most circuit simulation software, the diode SPICE parameter Tt called transit time, takes this effect into account.

2.5.1.2 SATURATION CURRENT SENSITIES

The effect of the saturation currents for rectifiers has been mathematically analyzed and observed in Figure 2.8 and Figure 2.12. It can be shown that for the same barrier height, the saturation current density of a Schottky diode exceeds that of a silicon p-n junction by a factor of 10^3 or more. For gallium arsenide diodes, this factor is smaller but still of the order of 10^2. In practice, the barrier height of a Schottky diode is likely to be appreciably less than that of a p-n junction made from the same semiconductor. This fact, taken in conjunction with the preceding argument, indicates that the saturation current density of a Schottky diode is likely to exceed that of a p-n junction made from the same semiconductor by a factor of 10^7 or more [44]. In other words, for the same saturation current density, the forward voltage drop across a p-n junction will exceed that across a Schottky diode by at least 0.4 V. In the simulation results presented in Figure 2.18, the effect of the saturation current on the diode voltage is well illustrated.
For the sake of completeness, it should be mentioned that the saturation current density depends strongly on the semiconductor used. Hence, the saturation current density of germanium diodes will exceed that of silicon diodes by several orders of magnitude, due to the lower band gap of germanium [51]. Consequently, the forward voltage drop across the germanium diodes is lower than that of silicon diodes by about 0.3 V. In Subsection 2.5.3, Table 2.2 presents typical diode forward voltages for different semiconductors.

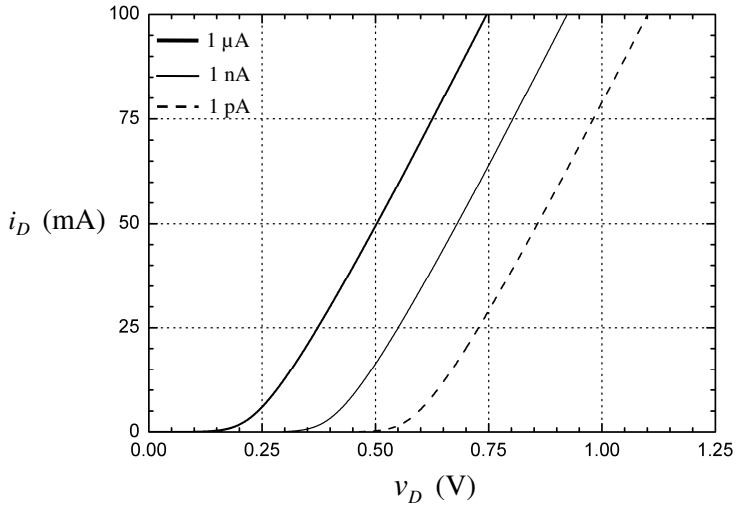


Figure 2.18: Effect of the saturation current on the diode current-voltage characteristic.

2.5.2 IDEALITY FACTOR

The effect of the ideality factor n has also been observed in Figure 2.8 and Figure 2.12: the closer n is to 1, the higher the rectified voltage. This behavior is comparable to the effect of the saturation current since the value of n shifts the curves. Expressed in a practical way: for the same saturation current, the diode forward voltage for $n = 2$ will exceed that for $n = 1$ by at least 0.35 V. In Figure 2.19, the plot of the diode current-voltage characteristic for two values of n illustrates it.

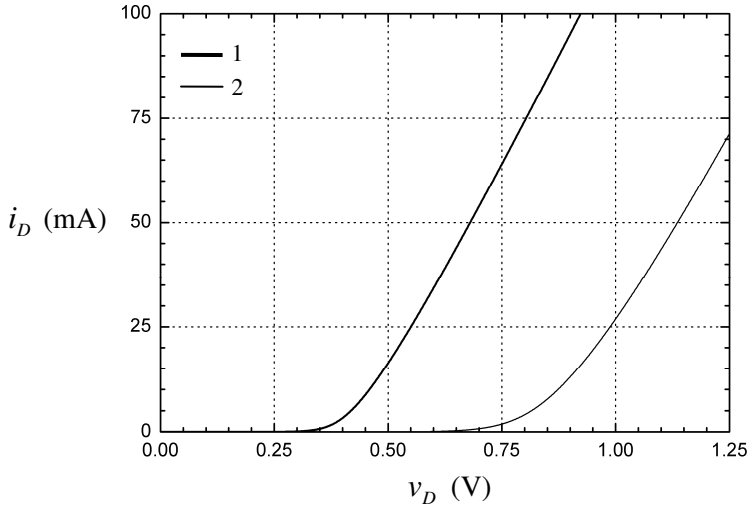


Figure 2.19: Effect of n on the diode current-voltage characteristic.

The value of n depends strongly on the diode technology process. In case of p-n junctions, n is close to unity if the p-type and n-type doping are in the same order of

magnitude. Conversely, n is close to 2 if one side of the p-n junction is doped much higher than the other. Otherwise, n is between 1 and 2.
For Schottky diodes, the ideality factor depends on the barrier height [51] and usually falls between 1 and 1.25 [58]. In most practical cases however, n is close to unity [55].
The conclusion of these discussions is that, for high-frequency applications where low-voltage or high-current rectification capabilities are required, Schottky diodes are far superior to p-n junctions.

2.5.3 CHOICE OF DIODE

In datasheets, commercial discrete diodes are characterized among others by their forward current-voltage characteristic or by their threshold voltage V_{th}, which is obtained as the intersection of the x-axis with the tangent of the current-voltage curve. To recapitulate Subsection 2.5.1 and Subsection 2.5.2, one can say that it is possible to maximize the AC-to-DC conversion by using diodes with the lowest possible forward or threshold voltage, as Figure 2.20 shows.

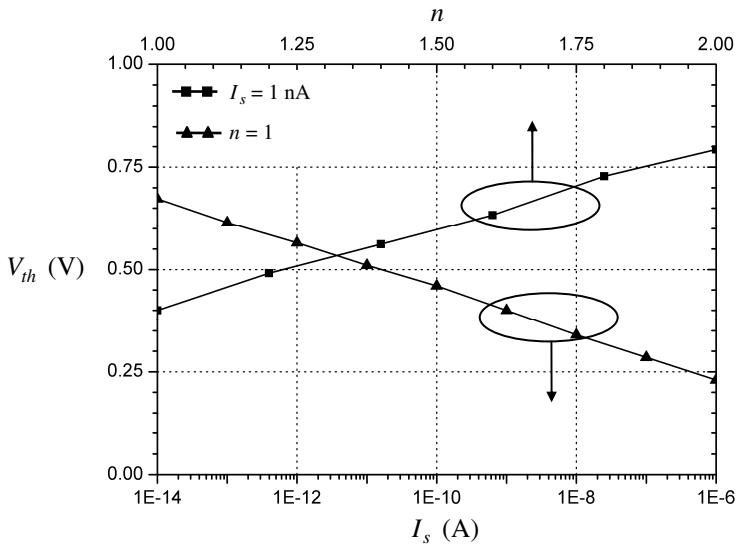


Figure 2.20: Diode threshold voltage as function of I_s (for n = 1) and of n (for I_s = 1 nA). The diode path resistance is 4.5 Ω.

Table 2.1 presents a brief comparative overview of some commercial Surface Mounting Devices (SMD) silicon Schottky and PIN diodes from the manufacturer Infineon Technologies [20].

Diode type	Device name	I_s (A)	n	Tt (s)
Schottky barrier	BAS40-04W	$5.1 \cdot 10^{-9}$	1.07	$25 \cdot 10^{-12}$
	BAT165	$50.2 \cdot 10^{-9}$	1.03	$10 \cdot 10^{-12}$
	BAT60A	$109.4 \cdot 10^{-6}$	1.09	$10 \cdot 10^{-12}$
	BAT62-02W	$250 \cdot 10^{-9}$	1.04	$25 \cdot 10^{-12}$
PIN junction	BA592	$3.9 \cdot 10^{-15}$	1.04	$140 \cdot 10^{-6}$
	BA595	$33.7 \cdot 10^{-12}$	1.22	$2.1 \cdot 10^{-6}$
	BAR64-03W	$3.7 \cdot 10^{-12}$	1.04	$2.5 \cdot 10^{-6}$
	BA597	$16.2 \cdot 10^{-12}$	1.02	$1.6 \cdot 10^{-6}$

Table 2.1: Comparison of the emission coefficient, saturation current and transit time between typical commercial Schottky barrier and PIN junction diodes.

Table 2.1 shows that high saturation current and short transit time are typical for Schottky diodes, and that low ideality factor is not characteristic of a diode type.
The aforementioned influence of the semiconductor on the saturation current density, and thus on the diode forward and threshold voltage, is illustrated in Table 2.2 [51].

Semiconductor	Threshold voltage
Germanium (Ge)	0.2 ··· 0.4 V
Silicon (Si)	0.5 ··· 0.7 V
Selenium (Se)	0.6 V
Gallium arsenide (GaAs)	1.3 ··· 1.5 V
Gallium arsenide phosphide (GaAsP)	1.6 ··· 2.2 V
Gallium phosphide (GaP)	2.2 ··· 2.4 V

Table 2.2: Typical diode threshold voltage for different semiconductors.

2.6 BREAKDOWN VOLTAGE

In the previous sections of this chapter, the circuit analyses have been done under the implicit assumptions that the diodes can be infinitely reverse-biased, and the resulting diode current is nearly equal to the saturation current I_s, according to (2.7). However, real diodes are characterized by a breakdown voltage, generally noted B_V. It gives the voltage in the reverse-biasing, where the collision ionization turns into an avalanche breakthrough [64]. As depicted in Figure 2.21, near this point, a slight voltage growth in the reverse-biasing can only be caused by a very high reverse current, which differs significantly from I_s, contrary to the implicit assumptions mentioned above.

Most diodes burn out when they are driven to this point, while so-called Zener diodes are conceived to operate near to this point. Assuming that the rectifier diodes are driven to this point without burning out, the mathematical analysis of the achieved rectified output voltage can be done after modeling the diode characteristic h by means of a step function around the voltage $-B_V$, as depicted in Figure 2.21.

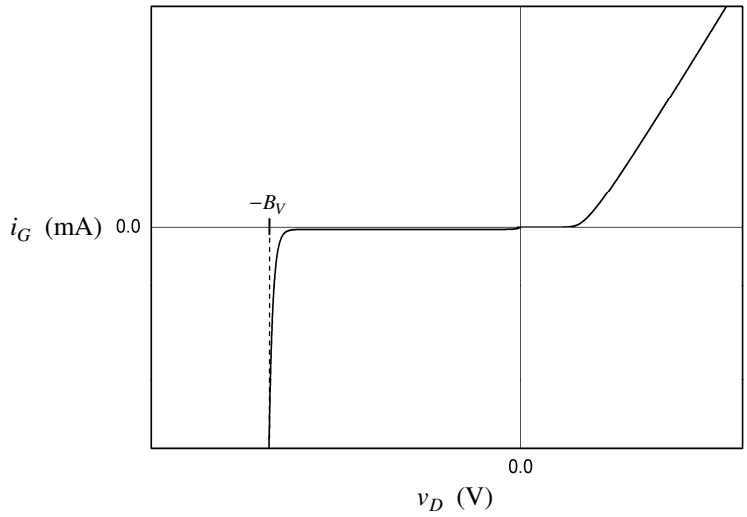


Figure 2.21: Diode current-voltage characteristic with respect of B_V .

2.6.1 ANALYTICAL DESCRIPTION

To determine the effect of B_V on the AC-to-DC conversion function, it is necessary to first analyze the typical voltage time function of a diode included in a voltage multiplying rectifier. As already shown in Figure 2.13 and Figure 2.15, all diodes are identically reverse-biased with the DC offset voltage v_R/N. The AC voltage v_0 is added to it (see Section 3.2), hence the voltage v_D across each diode has a time function similar to the curve shown in Figure 2.22, where T_0 is the period of the AC source voltage v_0.

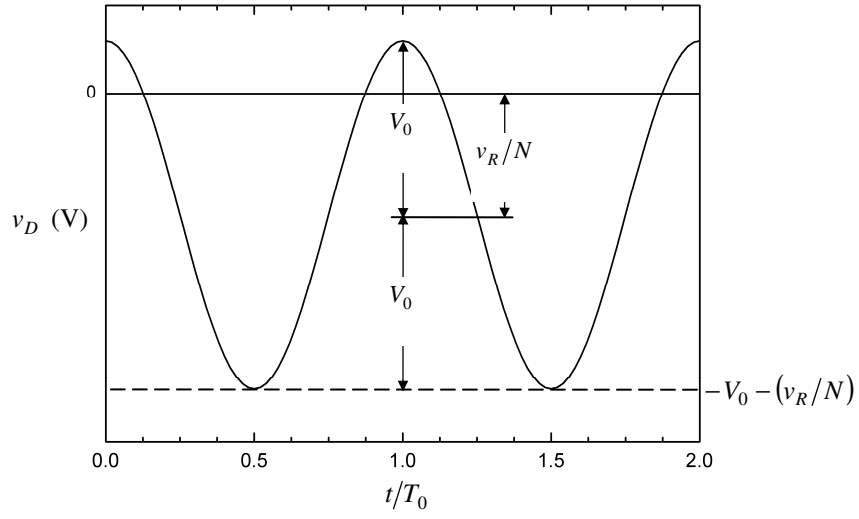


Figure 2.22: Typical diode voltage.

To keep the diodes safe, $-B_V$ should be lower than or equal to the lowest voltage in Figure 2.22. Then one can write:

$$-B_V \leq -V_0 - \frac{v_R}{N}. \tag{2.37}$$

In the extreme case where the breakdown voltage is reached, the highest possible DC voltage $v_{R,max}$ at the load resistance R is achieved and can be calculated by combining (2.37) and (2.28) in the system of equations:

$$\begin{cases} v_{R,max} = N \cdot \left(B_V - V_{0,max}\right) \\ e^{\frac{v_{R,max}}{NnV_T}}\left(\frac{v_{R,max}}{RI_s}+1\right) - I_0\left(\frac{V_{0,max}}{nV_T}\right) = 0 \end{cases}, \tag{2.38}$$

where $V_{0,max}$ is the lowest AC source voltage amplitude that causes the maximum DC output voltage $v_{R,max}$.

In the case of a voltage doubler, the calculated and simulated AC-to-DC conversion functions are plotted for diodes with different values of B_V in Figure 2.23. For $V_0 \geq V_{0,max}$, the DC output voltage remains equal to $v_{R,max}$. Hence, B_V describes the saturation of the conversion function. Furthermore, it can be seen that the error resulting from the assumption of a diode voltage-current step function around the voltage $-B_V$ made in Figure 2.21 is negligible. In a general manner, it is deduced that the lower B_V, the less the maximum achievable rectifier output voltage [38].

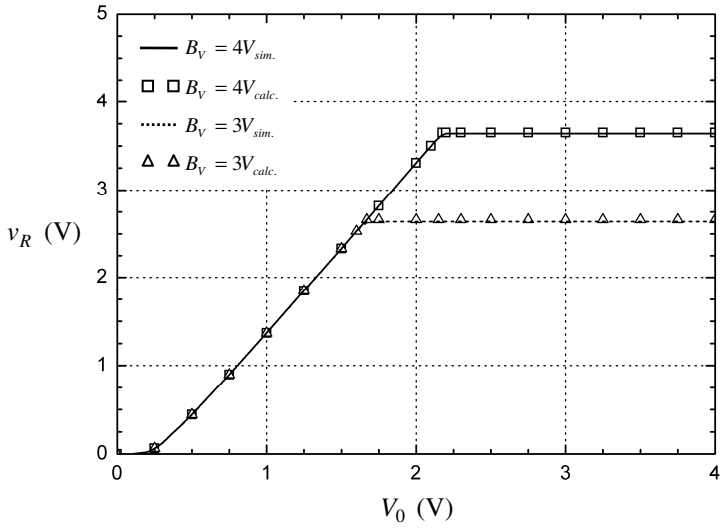


Figure 2.23: Effect of B_V on the conversion function with R = 10 kΩ, R_s = 0 Ω, I_s = 10 nA, n = 1, C = 1 pF, Cc = 50 nF and f_0 = 1 MHz.

2.6.2 THEORETICAL LIMIT

The theoretical upper limit of the achievable rectified voltage $v_{R,id,max}$ can be calculated, using the ideal AC-to-DC conversion function expressed in (2.5), and taking into account the inequality (2.37). Therewith (2.38) becomes

$$\begin{cases} v_{R,id,max} = N\left(B_V - V_0\right) \\ v_{R,id,max} = NV_0 \end{cases}. \tag{2.39}$$

The solution of (2.39) is

$$v_{R,id,max} = \frac{1}{2} N \cdot B_V \,. \tag{2.40}$$

Therewith a rough but quick and practical estimation of the maximum expectable rectified voltage is given. Equation (2.40) also gives an additional design rule for the number and the type of diodes to use. Furthermore, (2.40) gives the analytic and correct formulation of the empirical estimation made in [38] expressed as follows: with a single-diode rectifier, the maximum achievable DC output voltage is the breakdown voltage divided by 2.2. However, this estimation neglects the other diode parameters and the load resistance, which can decrease the expected DC voltage significantly.

2.7 LINEARIZATION

The transcendent equation (2.28) is not comfortable, since a mathematic or graphic solver is needed to determine v_R. However, looking at the curves depicted in Figure 2.8, Figure 2.12 and Figure 2.16, one sees that they seem linear for high values of V_0. The possibility of linearizing (2.28) will now be investigated, so as to simplify the analysis of the rectifier.

2.7.1 GENERAL APPROXIMATION

Assuming a linear behavior for large AC source voltage amplitudes in the aforementioned figures means that the conversion functions can be approximated by a straight line equation

$$v_R = \alpha \cdot V_0 + \beta \tag{2.41}$$

for $V_0 \to \infty$, where the parameters α and β can be determined analytically.

2.7.1.1 GRADIENT

The straight line slope α represents the tangent of the conversion function and can be obtained by differentiating (2.28) against V_0 as:

$$\frac{d}{dV_0}\left[e^{\frac{v_R}{NnV_T}}\left(\frac{v_R}{RI_s}+1\right)-I_0\left(\frac{V_0}{nV_T}\right)\right]=0\,. \tag{2.42}$$

The tangent is to be calculated for points far from the coordinate system origin, that is for $V_0 \to \infty$.
Knowing that for a real number z, one has [1]

$$\lim_{z\to\infty} I_0(z)=\frac{e^z}{\sqrt{2\pi z}}\,, \tag{2.43}$$

then, it results:

$$\lim_{V_0\to\infty} I_0\left(\frac{V_0}{nV_T}\right)=e^{\left(\frac{V_0}{nV_T}\right)}\left[2\pi\left(\frac{V_0}{nV_T}\right)\right]^{-\frac{1}{2}}. \tag{2.44}$$

Therewith for $V_0 \to \infty$, the second summand in (2.42) is

$$\begin{aligned}\frac{d}{dV_0}\left[I_0\left(\frac{V_0}{nV_T}\right)\right] &\approx \frac{d}{dV_0}\left(e^{\frac{V_0}{nV_T}}\left[2\pi\left(\frac{V_0}{nV_T}\right)\right]^{-\frac{1}{2}}\right).\\ &\approx \frac{1}{nV_T} I_0\left(\frac{V_0}{nV_T}\right)\end{aligned} \tag{2.45}$$

Furthermore, knowing that $v_R \to \infty$ when $V_0 \to \infty$, one has obviously

$$1+\frac{v_R}{RI_s}\approx\frac{v_R}{RI_s}\,. \tag{2.46}$$

Therewith (2.42) can be developed as follows:

$$\begin{aligned}&\frac{d}{dV_0}\left[e^{\frac{v_R}{NnV_T}}\left(\frac{v_R}{RI_s}\right)-I_0\left(\frac{V_0}{nV_T}\right)\right]=0 \Leftrightarrow\\ &\frac{1}{NnV_T}\frac{dv_R}{dV_0}\left(\frac{v_R}{RI_s}\right)e^{\frac{v_R}{NnV_T}}+\frac{1}{RI_s}\frac{dv_R}{dV_0}e^{\frac{v_R}{NnV_T}}-\frac{1}{nV_T}I_0\left(\frac{V_0}{nV_T}\right)=0\end{aligned}\,. \tag{2.47}$$

Furthermore, using (2.28) and (2.46), one has:

$$\frac{1}{RI_s} \approx \frac{e^{\frac{-v_R}{NnV_T}}}{v_R} I_0\left(\frac{V_0}{nV_T}\right). \tag{2.48}$$

Inserting (2.48) in (2.47) leads to

$$\frac{1}{NnV_T}\frac{dv_R}{dV_0} I_0\left(\frac{V_0}{nV_T}\right) + \frac{1}{v_R}\frac{dv_R}{dV_0} I_0\left(\frac{V_0}{nV_T}\right) - \frac{1}{nV_T} I_0\left(\frac{V_0}{nV_T}\right) = 0, \tag{2.49}$$

and at last to

$$\left(\frac{1}{NnV_T} + \frac{1}{v_R}\right)\frac{dv_R}{dV_0} - \frac{1}{nV_T} = 0. \tag{2.50}$$

Setting $\alpha = dv_R/dV_0$ and $1/v_R = 0$, the tangent is obtained as

$$\alpha = \frac{dv_R}{dV_0} = N. \tag{2.51}$$

Hence (2.41) can be written as:

$$v_R = N \cdot V_0 + \beta. \tag{2.52}$$

Equation describes an infinity of parallel straight lines.

2.7.1.2 Y-INTERCEPT

The parameter β is the y-intercept of the straight line and thus is expected to depend on the diode parameters n and I_s as well as on the load resistance R, as one can deduce from Figure 2.8. β can be determined by setting (2.52) in (2.28):

$$e^{\frac{NV_0+\beta}{NnV_T}}\left(\frac{NV_0+\beta}{RI_s}+1\right) - I_0\left(\frac{V_0}{nV_T}\right) = 0. \tag{2.53}$$

Assuming that β has a finite value and setting $V_0 \to \infty$, (2.53) is

$$e^{\frac{V_0}{nV_T}} e^{\frac{\beta}{NnV_T}}\left(\frac{NV_0}{RI_s}\right) - e^{\frac{V_0}{nV_T}}\left[2\pi\left(\frac{V_0}{nV_T}\right)\right]^{-\frac{1}{2}} = 0. \tag{2.54}$$

Thus β is then given as

$$\beta = NnV_T \, ln\left(\frac{RI_s}{N} \sqrt{\frac{nV_T}{2\pi V_0^3}} \right). \tag{2.55}$$

It proceeds from (2.55), that

$$\lim_{V_0 \to \infty} \beta = -\infty . \tag{2.56}$$

This is in contradiction to the assumed finite value for β. Therefore one can say that in general, the AC-to-DC conversion function cannot be asymptotically approximated with straight line equations.

2.7.2 RESTRICTED APPROXIMATION

It has been shown that a general asymptotic approximation is not possible. Nonetheless, one observes that in restricted intervals, the AC-to-DC conversion function may be accurately approximated by straight lines as

$$v_R = \alpha' \cdot V_0 + \beta' , \tag{2.57}$$

where α' and β' are obviously the gradient and the y-intercept, respectively. From (2.51), one sets

$$\alpha' = N . \tag{2.58}$$

Hence, using (2.57) and (2.58), the value of β' can be calculated for a reference source voltage amplitude $V_{0,ref}$ taken arbitrary in the restricted interval. β' is then assumed to be constant in the interval around $V_{0,ref}$:

$$\beta' = v_{R,ref} - N \cdot V_{0,ref} , \tag{2.59}$$

where $v_{R,ref}$ is the DC voltage corresponding to the reference source voltage amplitude $V_{0,ref}$ and is calculated using (2.28). Therefore, β' depends on n, I_s, R and N, as expected. Then the AC-to-DC conversion function (2.28) can be approximated as

$$v_R = N \cdot V_0 + \left(v_{R,ref} - N \cdot V_{0,ref} \right). \tag{2.60}$$

Figure 2.24 shows the plots of the conversion functions for a voltage doubler for different settings of the reference source voltage amplitude $V_{0,ref}$: 1 V, 10 V, and 100 V. The original function (2.28) is also plotted on Figure 2.24, and is compared against the three other conversion functions. In Figure 2.24 (a), the difference for low values of V_0

results from the different β' of the conversion functions. The absolute error between the original and the linear functions depicted in Figure 2.24 (b) shows that the approximations are the most accurate around $V_0 = V_{0,ref}$.

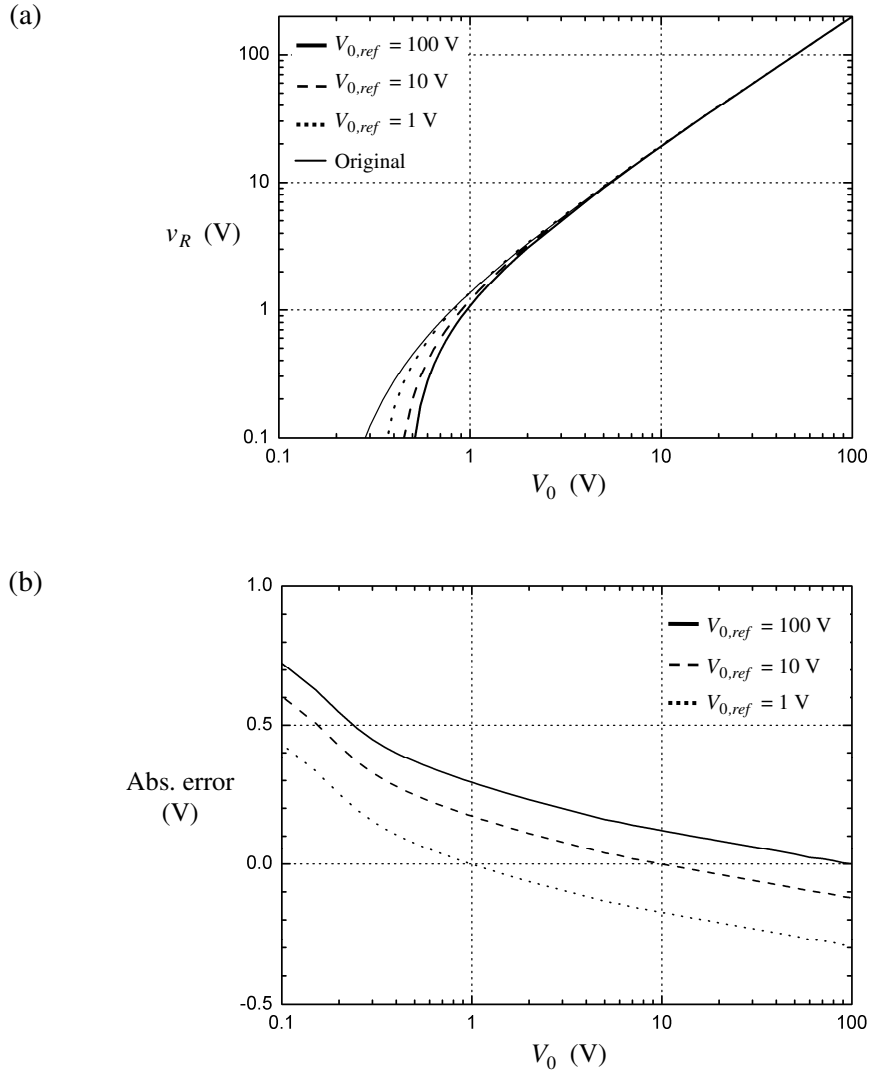


Figure 2.24: (a) Linear approximation of the conversion function; (b) difference between the original and the linear functions with $R_s = 0\ \Omega$, $R = 10\ \text{k}\Omega$, $n = 1$, $I_s = 10\ \text{nA}$, $C = 1\ \text{pF}$, $Cc = 50\ \text{nF}$ and $f = 1\ \text{MHz}$.

Furthermore, Figure 2.24 (b) shows that the absolute value of the absolute error grows slowly but continuously for high values of V_0. Nevertheless, the relative error decreases rapidly for $V_0 \to \infty$.

2.8 OPEN-CIRCUIT PERFORMANCES

The investigation of the rectified voltage by open rectifier output has no practical relevance for the system analysis. Nonetheless, it yields interesting results, which are presented in this section.
For this purpose, the breakdown voltage is set to infinity and thus, its limiting effect on the rectified voltage is not considered. The open-circuit DC voltage v_{oc} of N stage voltage multiplying rectifiers is analytically investigated after setting $R \to \infty$. Therewith one obtains from (2.28):

$$v_{oc} = \lim_{R\to\infty}(v_R) = NnV_T \, ln\left[I_0\left(\frac{V_0}{nV_T} \right) \right]. \tag{2.61}$$

Thus, the open-circuit DC voltage depends on the number of diode stages, the temperature, and the diode emission coefficient, but not on the diode saturation current I_s. The relation between v_{oc} and V_0 is shown in Figure 2.25 for $N = 1$ and $N = 2$, and in each case for $n = 1$ and $n = 2$. Even under these assumptions, the ideal conversion function described by (2.5) is not reached.

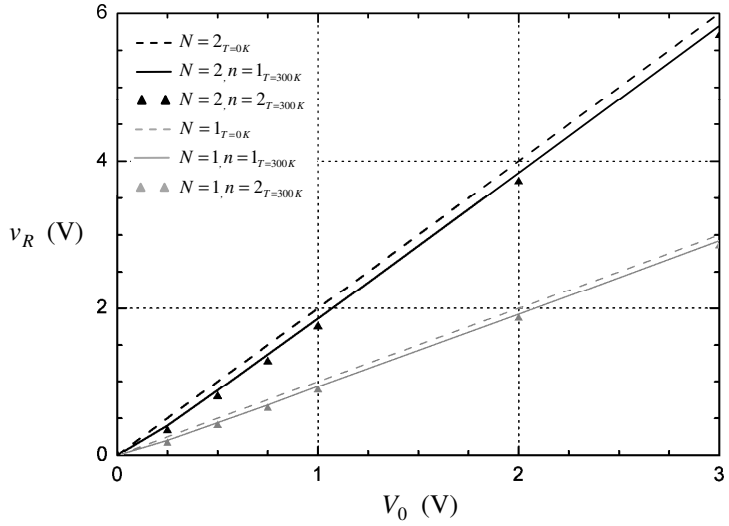


Figure 2.25: Open-circuit DC voltage v_R with $R_s = 0\ \Omega$, $C = 1$ pF, $Cc = 50$ nF and $f = 1$ MHz.

At last, the value of the open-circuit DC voltage at the temperature $T = 0$ K has been analytically investigated. According to (2.8), this means: $V_T = 0$ V. Similarly to the previous section, one can then write [1]:

$$\lim_{V_T \to 0V} I_0\left(\frac{V_0}{nV_T}\right) = e^{\frac{V_0}{nV_T}}\left[2\pi\left(\frac{V_0}{nV_T}\right)\right]^{-\frac{1}{2}}. \tag{2.62}$$

Inserting (2.62) in (2.61) leads to

$$\begin{aligned} v_{oc,T=0K} &= \lim_{V_T \to 0} NnV_T \, ln\left(e^{\frac{V_0}{nV_T}}\left[2\pi\left(\frac{V_0}{nV_T}\right)\right]^{-\frac{1}{2}}\right), \\ &= N \cdot V_0 \end{aligned} \tag{2.63}$$

which corresponds to (2.5). In this case, the rectified voltage does not depend on the diode parameters. Figure 2.25 shows the resulting conversion function of (2.61) and (2.63). The result from (2.63) is theoretical, since modified diode models hold at cryogenic temperature [68]. The DC voltage v_{oc} cannot be measured, since the circuit analyzer used for measurement has a finite internal resistance, which will behave as load resistance for the rectifier.

2.9 POWER AND EFFICIENCY ANALYSIS

In this section,the performances of the rectifier are analyzed by studying the power losses and power efficiency of the circuit. The circuit simply consists of the AC voltage source, diodes, capacitors, and the load resistor. The capacitors are assumed to be ideal, thus they do not consume electric power. Therefore the total power delivered by the AC voltage source is distributed in the diodes and the load resistor.

2.9.1 POWER ANALYSIS

It has already been discussed in previous subsections and especially in Subsection 2.6.1 that the rectifier diodes do not simply behave as short- or open circuits, contrary to common assumptions. Therefore, looking from the load resistance into the rectifier output, the rectifier circuit presents certainly a finite internal resistance, whose value is then expected to be dependent on the diode current-voltage characteristic. It is noted $R_{P_{\max}}$ since it is equal to the load resistance leading to the maximum output power $P_{\max}$. The analytical expression of $R_{P_{\max}}$ is investigated.

For this purpose, a time-invariant output voltage v_R is assumed. Therewith the power consumption P_R of the load resistance can be expressed as

$$P_R = \frac{v_R^2}{R}. \tag{2.64}$$

To obtain the value of $R_{P_{\max}}$ leading to the maximum output power $P_{\max}$, the differentiation against R of the output power expressed in (2.64) is set equal to zero:

$$\frac{dP_R}{dR} = 0 . \tag{2.65}$$

Inserting (2.64) in (2.65), one obtains

$$2R\frac{dv_R}{dR} - v_R = 0 . \tag{2.66}$$

The term $\frac{dv_R}{dR}$ in (2.66) can be obtained by differentiating (2.28) against R as

$$\frac{d}{dR}\left[e^{\frac{v_R}{NnV_T}}\left(\frac{v_R}{RI_s} + 1 \right) - I_0\left(\frac{V_0}{nV_T} \right) \right] = 0 . \tag{2.67}$$

The left side of (2.67) is set equal to zero because the left side of (2.28) is also equal to zero. The second summand in the square brackets of (2.67) is not dependent on R and thus is equal to zero after differentiation. Therewith the development of (2.67) leads to

$$\frac{dv_R}{dR} = \frac{NnV_T v_R}{R\left(NnV_T + RI_s + v_R\right)} . \tag{2.68}$$

Inserting (2.68) in (2.66) leads to

$$v_R = NnV_T - RI_s . \tag{2.69}$$

Inserting (2.69) in (2.28) leads to the transcendent equation for $R_{P_{max}}$ as

$$\frac{NnV_T}{R_{P_{max}} I_s} e^{\left(1 - \frac{R_{P_{max}} I_s}{NnV_T}\right)} - I_0\left(\frac{V_0}{nV_T} \right) = 0 . \tag{2.70}$$

Equation (2.70) shows that $R_{P_{max}}$ depends on the AC source voltage amplitude and on the diode current-voltage characteristic, as expected. Furthermore, Figure 2.26 shows that $R_{P_{max}}$ decreases as V_0 increases. This result is due to the fact that the higher the AC source voltage amplitude, the higher the diode forward bias current and thus, the less the diode forward resistance. For the same reason, the ideality factor n affects $R_{P_{max}}$ drastically: for a given value of V_0, the value of $R_{P_{max}}$ for $n = 2$ exceeds that for $n = 1$ by several orders of magnitude. This result proceeds from the fact that a higher value of n leads to a lower diode forward bias current. It results a higher diode resistance and consequently a higher value of the rectifier internal resistance. Figure 2.26 shows also that the value of $R_{P_{max}}$ increases with the number of diodes N. This confirms the

proposed equivalent rectifier DC circuit depicted in Figure 2.14.

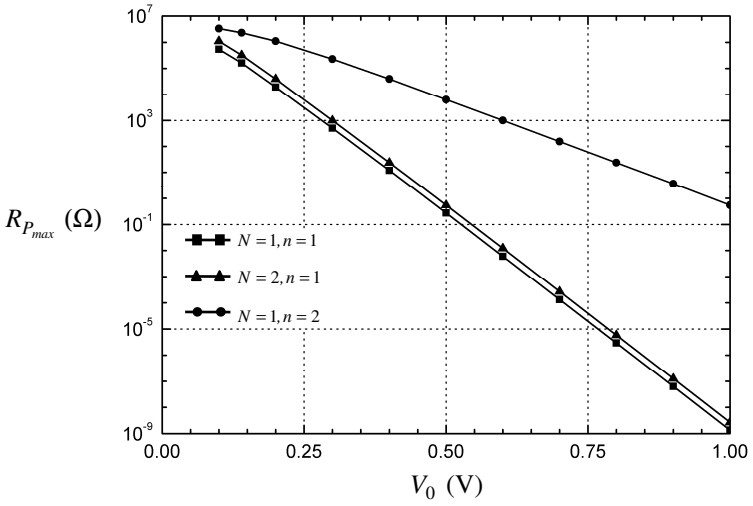


Figure 2.26: $R_{P_{max}}$ for different values of n and N with: $R_s = 0\ \Omega$, $I_s = 10$ nA, $Cc = 50$ nF, $C = 1$ pF and $f = 1$ MHz.

2.9.2 EFFICIENCY ANALYSIS

To analyze the efficiency analysis of the rectifier, the Cockcroft-Walton circuit depicted in Figure 2.13 is considered. All diodes are assumed to be identical and thus each one consumes the same electric power as the diode D_1.
The dissipated power in D_1, noted P_{D_1}, can be expressed as

$$P_{D_1} = \frac{1}{T_0}\int_0^{T_0}\left(v_{D_1}\cdot i_{D_1}\right)dt\,, \tag{2.71}$$

where v_{D_1} and i_{D_1} are the time function of the voltage and the current at the diode D_1, respectively. $T_0 = 1/f_0$ is the period of the AC source voltage. As shown in Figure 2.13, the DC current i_R and the DC voltage v_R/N across the diode D_1 are opposed. This means that D_1 acts as DC source, providing DC voltage and DC current. Thus, the power loss in D_1 is the difference between the total input power of D_1 and the power it delivers. Therefore, considering all harmonics, the power P_{D_1} can be expressed as

$$P_{D_1} = \sum_{m=1}^{\infty}\frac{1}{2}\Re\left\{V_m\cdot I_m^*\right\} - \frac{v_R}{N}i_R\,, \tag{2.72}$$

where V_m and I_m^* are the amplitude of the voltage and the conjugate complex current at the angular frequency $m\cdot\omega_0$, respectively. As it will be shown in Section 3.2, v_0 is the

only AC voltage across the diode D_1. Therewith (2.72) becomes

$$P_{D_1} = \frac{1}{2}\Re\{V_0 \cdot I_0^*\} - \frac{v_R}{N} i_R . \tag{2.73}$$

Developing (2.34) similarly to (2.13) leads to a current at the angular frequency ω_0 which is in phase with v_0. Inserting the amplitude of this current in (2.73) leads to

$$P_{D_1} = V_0 I_s e^{\frac{-v_R}{NnV_T}} I_1\left(\frac{V_0}{nV_T}\right) - \frac{v_R}{N} i_R , \tag{2.74}$$

where I_1 is the modified Bessel function of the first kind of order 1. Since all diodes have identical power consumption, the total dissipated power in the diodes is

$$\sum_{i=1}^{N} P_{D_i} = N \cdot P_{D_1} = NV_0 I_s e^{\frac{-v_R}{NnV_T}} I_1\left(\frac{V_0}{nV_T}\right) - v_R i_R . \tag{2.75}$$

Therewith the AC-to-DC conversion efficiency η of the rectifier which is defined as the quotient of the dissipated power in the load and the total power dissipated in the circuit can be expressed as:

$$\eta = \frac{P_R}{P_R + \sum_{i=1}^{N} P_{D_i}} . \tag{2.76}$$

The last summand $v_R i_R$ in (2.75) is obviously the dissipated power P_R in the load resistance R, as described in (2.64). Hence (2.76) can be expressed as

$$\eta = \frac{\frac{v_R^2}{R}}{NV_0 I_s e^{\frac{-v_R}{NnV_T}} I_1\left(\frac{V_0}{nV_T}\right)} . \tag{2.77}$$

The conversion efficiency is dependent on the AC source voltage amplitude, as Figure 2.27 (a) attests. Generally, for a given load resistance and a given AC source voltage amplitude, the conversion efficiency increases as the number of diodes decreases, since the diodes dissipate a part of the power delivered by the source. For high values of V_0, the total power dissipated in the diodes is negligible compared to the output power. Conversion efficiency close to unity is then reached.

The effect of the ideality factor n on the efficiency can be observed in Figure 2.27 (b). As expected from Figure 2.8, the higher the ideality factor n, the lower the conversion efficiency. Figure 2.27 (b) also shows that η reaches a maximum for a particular load

resistance. The value of this resistance, noted $R_{\eta_{max}}$, is analytically to be sought. For this purpose, equation (2.77) is used and the first derivative of η against R is set to zero:

$$\frac{d\eta}{dR} = 0 \Leftrightarrow \frac{d}{dR}\left[\frac{v_R^2}{NV_0RI_s e^{\frac{-v_R}{NnV_T}} I_1\left(\frac{V_0}{nV_T}\right)}\right] = 0\,. \tag{2.78}$$

Developing (2.78) leads to the differential equation

$$\left(2 + \frac{v_R}{NnV_T}\right) R\frac{dv_R}{dR} - v_R = 0\,. \tag{2.79}$$

Inserting (2.68) in (2.79) leads to $R_{\eta_{max}}$ as

$$R_{\eta_{max}} = \frac{NnV_T}{I_s}\,. \tag{2.80}$$

The resistance $R_{\eta_{max}}$ is proportional to the number of diodes and to the ideality factor, and is inversely proportional to the diode saturation current. It is notable that $R_{\eta_{max}}$ is not affected by the nonlinearity of the system, since it does not depend on V_0. To prove the correctness of (2.80), a single-stage rectifier is considered, and the diode saturation current is set to I_s = 10 nA. At room temperature, the thermal voltage is V_T = 25.6 mV. Inserting these values in (2.80), one obtains $R_{\eta_{max}}$ = 2.56 MΩ for $n = 1$ and $R_{\eta_{max}}$ = 5.12 MΩ for $n = 2$. Figure 2.27 (b) confirm these results and consequently the calculation method.

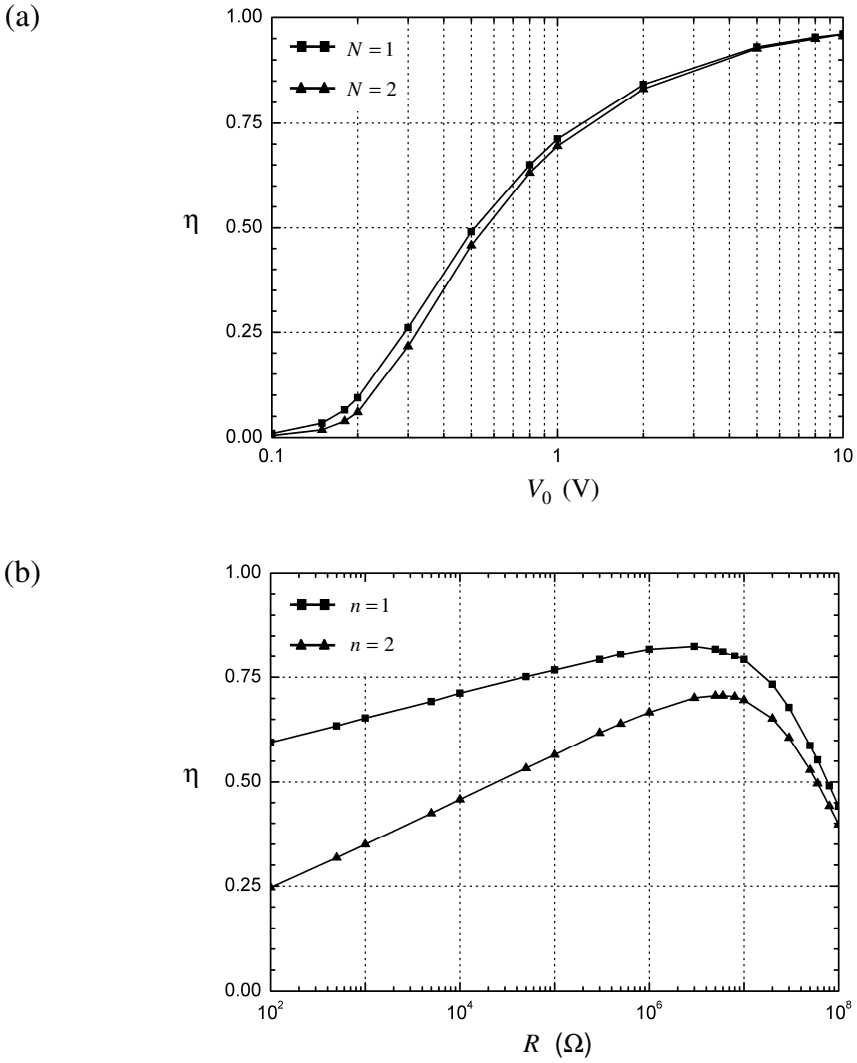


Figure 2.27: Influence of (a) the number of diode stages and (b) the diode emission coefficient on the efficiency.

2.10 CONCLUSION

In this chapter, a time-domain analysis of rectifiers including diodes has been presented. To take into account the diode parameters, a large signal diode model has been used. Based on the extracted formula for the DC output voltage of single-stage and two-stage diode rectifiers, a postulate for the DC output voltage of rectifiers including N diode stages has been enunciated and proved for two particular circuit topologies. The effects of diode parameters, load resistance and circuit capacitors on the rectified DC voltage have been investigated. Furthermore, the AC-to-DC conversion function has been piecewise approximated by straight functions with the tangent N, whereby the ordinate at the origin depends on the range of the AC source voltage amplitude as well as on the diode parameters and load resistance. The limit of the AC-to-DC conversion functions

has been investigated for open circuit and for absolute zero temperature. In the latter case, the DC output voltage is N times the AC voltage source amplitude. For given AC source voltage amplitude, the rectifier output power can be maximized by choosing carefully the load resistance. As well, the load resistance leading to the maximum conversion efficiency can be analytically determined for a given circuit topology and diode type.

3 HIGH FREQUENCY ANALYSIS

In this chapter, the AC analysis of voltage multiplying rectifiers and especially the investigation of the input impedance for the Cockcroft-Walton rectifier as well as the Dickson charge pump will be done. The first step to this goal is the building of a more accurate model for the non-linear diode capacitance than in Chapter 2. Therewith a basic AC analysis of the introduced rectifier topologies can be done for the basic case, where the excitation is achieved by an ideal AC voltage source. To consider the case of antenna supplied rectifiers, the analysis will then be extended for AC voltage sources with internal impedance. Finally, the effect of the breakdown voltage on the circuit performances will be examined and the conversion efficiency will be observed.

3.1 DIODE CAPACITANCE MODEL

As it will be shown in Figure 3.3, the voltage across each diode is the superposition of a DC and an AC voltage in rectifier circuits. Its expression is as follows:

$$v_D = V_{DC} + V_{AC}\cos(\omega_0 t), \tag{3.1}$$

where V_{DC} and V_{AC} are the amplitudes of the DC and AC voltage at the diode, respectively.
As shown in Figure 2.13 and in Figure 2.15, the diodes are reverse biased, so the DC voltage at each diode is negative. Hence, the diode voltage oscillates between $-V_{AC}+V_{DC}$ and $V_{AC}+V_{DC}$.
Furthermore, each diode has been modeled in Section 2.3 as parallel circuit of a non-linear conductance G and a capacitance C, whereby the capacitance C is the sum of the depletion zone capacitance C_{dep} and the diffusion capacitance C_{dif}. The package capacitance should be added to the both above cited in the case of discrete devices. However, in order to simplify matters, it will not be considered in the analysis. Therewith one has:

$$C = C_{dep} + C_{dif}\,. \tag{3.2}$$

Due to the advantages presented in Section 2.5, only Schottky diodes will be considered in the rest of the analyses. Thus, one sets $C_{dif} = 0$ and consequently $C = C_{dep}$, according to the discussion in Paragraph 2.5.1.1.

The depletion zone capacitance C_{dep} is usually described by means of the SPICE parameters C_{j0}, F_c, V_j and M, which are the zero bias capacitance, the forward-bias depletion capacitance coefficient, the junction built-in potential (also noted P_b), and the grading coefficient, respectively. The capacitance C can then be described by means of two functions that depend on the value of the voltage v_D [12].

For $v_D \le F_c \cdot V_j$:

$$C = C_{j0}\left(1 - \frac{v_D}{V_j}\right)^{-M} . \tag{3.3}$$

For $v_D > F_c \cdot V_j$:

$$C = \frac{C_{j0}}{(1-F_c)^M}\left[1 + \frac{M}{V_j(1-F_c)}\left(v_D - F_c \cdot V_j\right)\right]. \tag{3.4}$$

The nonlinearity of the depletion capacitance is however defined only by the parameters V_j and M, since for most of diodes, the parameter F_c has the value 0.5 [37]. Figure 3.1 shows the effects of V_j and M on the capacitance-voltage characteristic of C. It is obvious that the general assumption of an almost voltage independent depletion capacitance can cause more or less significant inaccuracies in the AC analysis of the circuit, depending on the value of V_j and M.

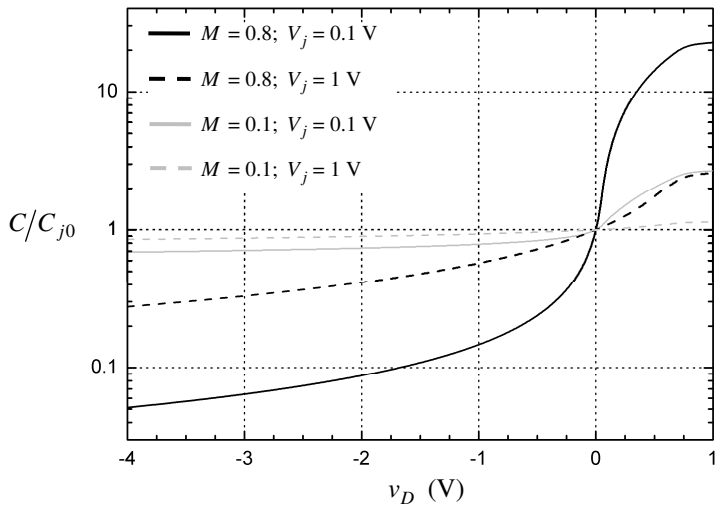


Figure 3.1: Influence of M and V_j on the voltage dependence of C

For convenient system analysis, the functions (3.3) and (3.4) are approximated by a polynomial:

$$C = C_{j0} \cdot \sum_{i=0} \left(a_i \cdot v_D^i \right), \tag{3.5}$$

where the polynomial coefficients a_i depend only on M and V_j according to the above discussion. In (3.5), the polynomial order may be infinite. However, it is a finite integer in practice. Setting the polynomial order to four and assuming a diode voltage oscillation between -4 V and 0.5 V, the values of the coefficients a_i are computed for different values of M and V_j, and are shown in Figure 3.2. One sees that in a general manner, the coefficients a_i become more significant for low values of V_j or high values of M. This behavior can be deduced from Figure 3.1, where the curve variations are more pronounced for $M = 0.8$ than for $M = 0.1$ on one hand, and more for $V_j = 0.1$ V than for $V_j = 0.8$ V on the other hand.

Once the coefficients a_i are obtained for a particular diode, the current i_C through the diode capacitance can be determined as

$$i_C = \frac{dQ}{dt} = \frac{d}{dt}\left(C \cdot v_D \right), \tag{3.6}$$

where Q is the total charge in the diode depletion zone. Inserting the polynomial approximation (3.5) in (3.6), it results:

$$\frac{d}{dt}\left(C \cdot v_D \right) = \frac{d}{dt}\left[C_{j0}\left(a_0 + a_1 \cdot v_D + a_2 \cdot v_D^2 + \cdots \right) \cdot v_D \right]. \tag{3.7}$$

After inserting (3.1) in (3.7) and considering only the terms at the fundamental frequency, one obtains

$$\left. \frac{d}{dt}\left(C \cdot v_D \right) \right|_{\omega_0} = -\omega_0 C_{j0} V_{AC} \, sin(\omega_0 t) \left[a_0 + 2a_1 V_{DC} + 3a_2 \left(V_{DC}^2 + \frac{1}{2} V_{AC}^2 \right) + \cdots \right] \cdot \tag{3.8}$$

Hence, the effective depletion capacitance C_j, which is the diode capacitance at the fundamental frequency, can be extracted as

$$C_j = C_{j0} \left[a_0 + 2a_1 V_{DC} + 3a_2 \left(V_{DC}^2 + \frac{1}{2} V_{AC}^2 \right) + \cdots \right]. \tag{3.9}$$

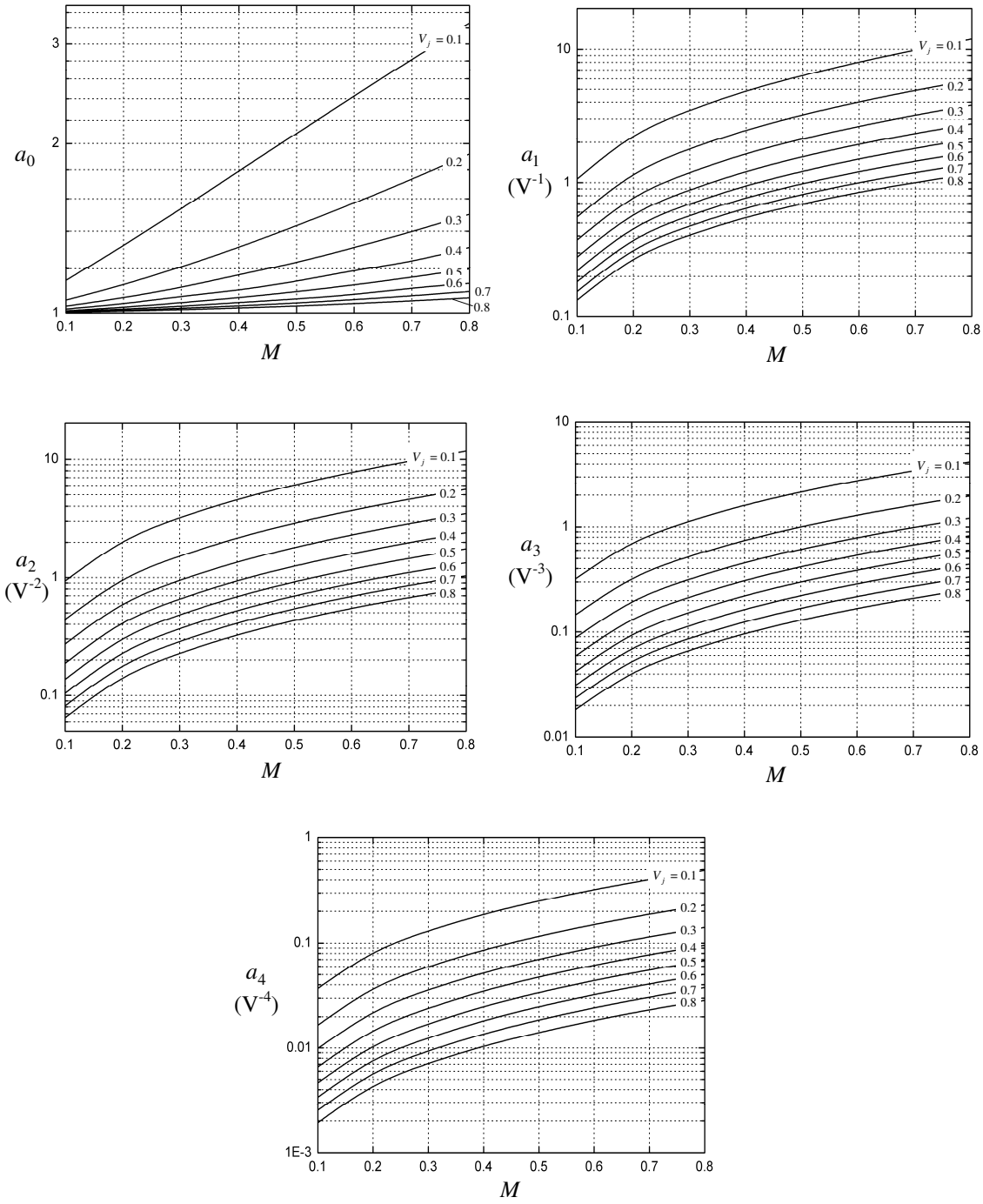


Figure 3.2: Polynomial coefficients as function of M and V_j . V_j is in V.

3.2 INPUT IMPEDANCE ANALYSIS

The determination of effective depletion capacitance C_j was an important step to the analytical description of the rectifier input impedance. In addition, the knowledge of the current and voltage repartition inside the circuit is required. The Cockcroft-Walton

rectifier will be first analyzed, and then the Dickson charge pump.

3.2.1 COCKCROFT-WALTON RECTIFIER

Without loss of the generality, a Cockcroft-Walton rectifier with an odd diode number is considered. Similarly to Figure 2.13, the circuit is excited by an ideal AC voltage source. The DC voltages from Figure 2.13 are reported in Figure 3.3 where the AC voltages are added.

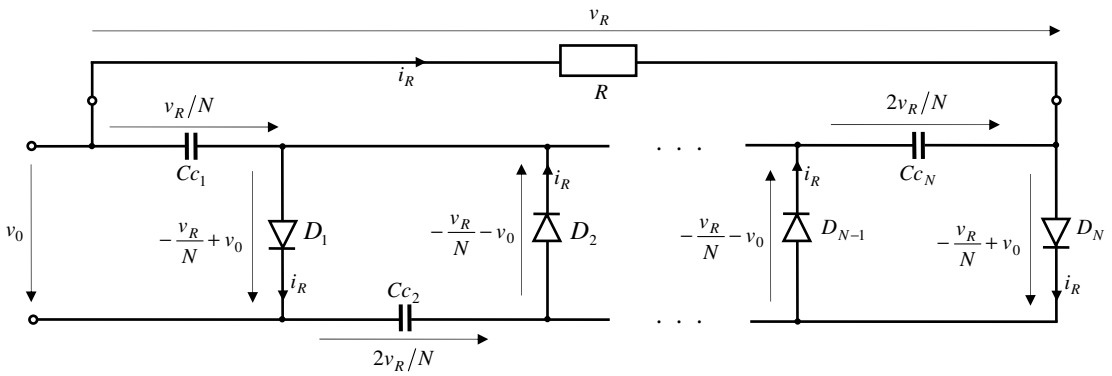


Figure 3.3: DC and AC analysis of a Cockcroft-Walton rectifier.

The source voltage v_0 is sinusoidal and thus, has no DC component. For large capacitance value Cc, v_{Cc_1} is almost time constant. Consequently, the AC voltage at the diode D_1 is v_0. Hence, the total voltage across the diode D_1 is

$$v_{D_1} = -\frac{v_R}{N} + v_0 . \tag{3.10}$$

The resulting current i_{D_1} through the diode D_1 can be expressed using (2.7), (3.6) and (3.10) as

$$i_{D_1} = h\left(-\frac{v_R}{N} + v_0\right) + \frac{d}{dt}\left[C \cdot \left(-\frac{v_R}{N} + v_0\right)\right]. \tag{3.11}$$

The first summand of (3.11) can be developed similarly to (2.13) as

$$h\left(-\frac{v_R}{N} + v_0\right) = I_s e^{\frac{-v_R}{NnV_T}}\left[I_0\left(\frac{V_0}{nV_T}\right) - e^{\frac{v_R}{NnV_T}} + 2\sum_{m=1}^{\infty} I_m\left(\frac{V_0}{nV_T}\right) cos(m\omega_0 t)\right], \tag{3.12}$$

where I_0 and I_m are the modified Bessel functions of the first kind of the order 0 and

m, respectively [39].
The second summand of (3.11) can be developed similarly to (3.8) under the consideration of (3.10).
Hence, the current i_{D_1} has components at the harmonics $m\omega_0$ with $m = 0, 1, \ldots, \infty$. The current i_{D_1,ω_0}, which is the spectral component of the diode current i_{D_1} at the fundamental frequency, that is for $m = 1$, is given as

$$i_{D_1,\omega_0} = \omega_0 C_j V_0 \cos\left(\omega_0 t + \frac{\pi}{2}\right) + 2I_s e^{\frac{-v_R}{NnV_T}} I_1\left(\frac{V_0}{nV_T}\right)\cos(\omega_0 t), \tag{3.13}$$

where I_1 is the modified Bessel function of the first kind and the order 1. Furthermore, the capacitance C_j is given by

$$C_j = C_{j0}\left[a_0 - 2a_1\left(\frac{v_R}{N}\right) + 3a_2\left(\left(\frac{v_R}{N}\right)^2 + \frac{V_0^2}{2}\right) - \cdots\right], \tag{3.14}$$

according to (3.9) and (3.10). The current i_{D_1,ω_0} has two components: the first one is $+\pi/2$ phase shifted to the excitation v_0, while the second is in phase with it. Therewith the admittance Y_{D_1} of the diode D_1 at the fundamental frequency is given by:

$$\begin{aligned} Y_{D_1} &= G_{D_1} + jB_{D_1} \\ &= \frac{2I_s}{V_0} e^{\frac{-v_R}{NnV_T}} I_1\left(\frac{V_0}{nV_T}\right) + j\omega_0 C_j \end{aligned}, \tag{3.15}$$

where G_{D_1} and B_{D_1} are the conductance and susceptance of the diode D_1, respectively. The Kirchhoff voltage law in each loop made of D_i, C_i and D_{i-1} shows that v_0 is the AC voltage across each diode. One deduces from Figure 3.3, that for diodes with odd subscript i, it results

$$i_{D_i} = \frac{d}{dt}\left[C \cdot \left(-\frac{v_R}{N} + v_0\right)\right] + h\left(-\frac{v_R}{N} + v_0\right), \tag{3.16}$$

and for diodes with even subscript i, it is

$$i_{D_i} = \frac{d}{dt}\left[C \cdot \left(-\frac{v_R}{N} - v_0\right)\right] + h\left(-\frac{v_R}{N} - v_0\right). \tag{3.17}$$

However, developing (3.16) and (3.17) similarly to (3.13) and taking into account the sense of the voltage arrows, leads to the same admittance Y_D for all diodes:

$$Y_D = Y_{D_1} = Y_{D_2} = \cdots = Y_{D_N}, \tag{3.18}$$

where $Y_D = G_D + jB_D$, with $G_D = G_{D_1}$ and $B_D = B_{D_1}$ Under the assumption that the current i_R has no AC component, the input impedance Z_N of a N stage Cockcroft-Walton rectifier can be calculated by means of the recursive expression

$$Z_N = Z_{Cc} + \frac{1}{Y_D + \dfrac{1}{Z_{N-1}}}, \tag{3.19}$$

where $Z_{Cc} = 1/j\omega_0 Cc$ and

$$Z_1 = Z_{Cc} + \frac{1}{Y_D}. \tag{3.20}$$

An enhanced diode model that takes into account the diode path resistance R_s and a lead inductance L, is shown in Figure 3.4 [8].

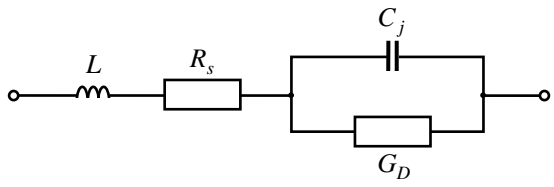


Figure 3.4: Equivalent circuit of the intrinsic Schottky diode.

For low values of R_s and $\omega_0 L$, the previous calculation of Y_D remains valid. Including this diode model in Figure 3.3 leads to Figure 3.5. Then (3.19) can be expressed as

$$Z_N = Z_{Cc} + \frac{1}{\dfrac{1}{Z_{N-1}} + \dfrac{1}{R_s + j\omega_0 L + \dfrac{1}{G_D + jB_D}}}, \tag{3.21}$$

where for $N = 1$, one has

$$Z_1 = Z_{Cc} + R_s + j\omega_0 L + \frac{1}{G_D + jB_D}. \tag{3.22}$$

Furthermore, the value of Cc has been set so large that the impedance of the circuit capacitors tends to zero at the fundamental frequency. Therefore, the rectifier input impedance Z_N can be approximated as

$$Z_N = \frac{1}{N}\left(R_s + j\omega_0 L + \frac{1}{G_D + jB_D} \right). \tag{3.23}$$

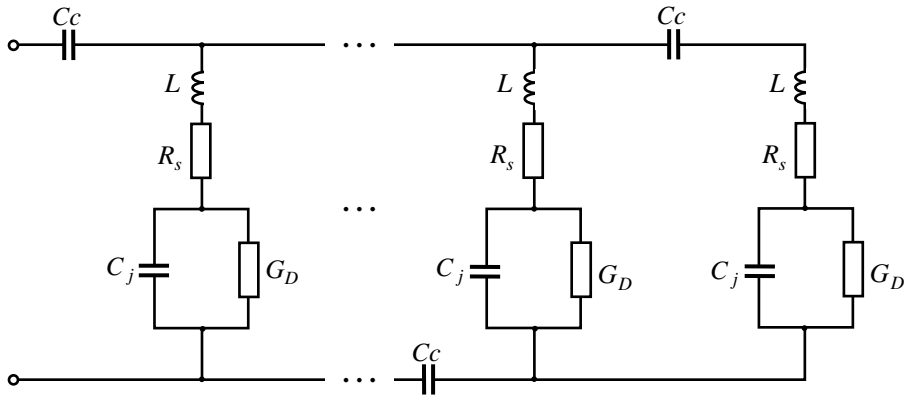


Figure 3.5: AC equivalent circuit of Cockcroft-Walton rectifiers at the fundamental frequency.

3.2.2 DICKSON CHARGE PUMP

The DC voltages shown in Figure 2.15 are reported in Figure 3.6. Since the circuit capacitor Cc_1 acts as short circuit at the fundamental frequency, the Kirchhoff voltage law at the rectifier input leads to $v_{D_1} = -v_0 - (v_R/N)$. Similarly, the voltages at the diodes are $v_{D_i} = -v_0 - (v_R/N)$ and $v_{D_i} = v_0 - (v_R/N)$ for odd and even diode subscript i, respectively, as depicted in Figure 3.6.

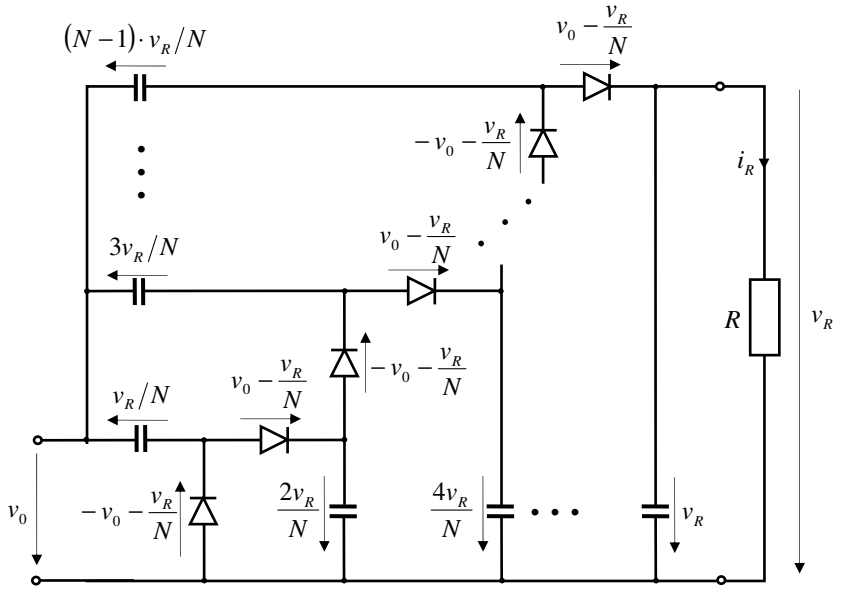


Figure 3.6: DC and AC analysis of the Dickson charge pump.

The diode currents can then be calculated by means of (3.16) and (3.17). They are identical to the voltages and currents in Cockcroft-Walton rectifiers, and thus, the resulting diode admittance can be calculated using (3.15). The load resistance R is considered as open circuit in order to determine the circuit input impedance: it is assumed that there is no AC current flow through R. Furthermore, all circuit capacitors are considered to be short circuits. Therewith the equivalent circuit at the fundamental frequency simply consists of a parallel circuit of the diodes D_1, D_2, ···, D_N, as shown in Figure 3.7.

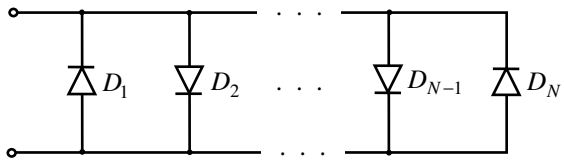


Figure 3.7: Equivalent circuit of the Dickson charge pump at the fundamental frequency.

Replacing each diode by its equivalent circuit according to Figure 3.4, the input impedance of the circuit is then given by (3.23). Hence, under the assumption that Z_{Cc} tends to zero at the AC source voltage frequency, Cockcroft-Walton rectifiers, Dickson charge pumps and consequently Greinacher rectifiers have the same input impedance for the same number and type of diodes.

3.2.3 VERIFICATION

To verify the correctness of (3.23), the input impedance of Cockcroft-Walton rectifiers including up to five stages is analyzed. The Schottky diode BAT15-03W from Infineon Technologies with following SPICE parameters is used [20]:

$I_s = 130$ nA

$n = 1.08$

$R_s = 4.5\ \Omega$

$C_{j0} = 0.26$ pF

$F_c = 0.5$

$V_j = 0.11$ V

$M = 0.047$.

The order of the approximation polynomial for the capacitance-voltage characteristic of C is set to four. The corresponding polynomial coefficients have been computed using the software Origin as follows:

$a_0 = 1.05808$

$a_1 = 0.44538\ \text{V}^{-1}$

$a_2 = 0.37332\ \text{V}^{-2}$

$a_3 = 0.12570\ \text{V}^{-3}$

$a_4 = 0.01435\ \text{V}^{-4}$.

The resulting polynomial is depicted in Figure 3.8 for a voltage ranging from -4 V to 1 V. The capacitance-voltage characteristic described by (3.2) and (3.3) is also depicted for comparison.

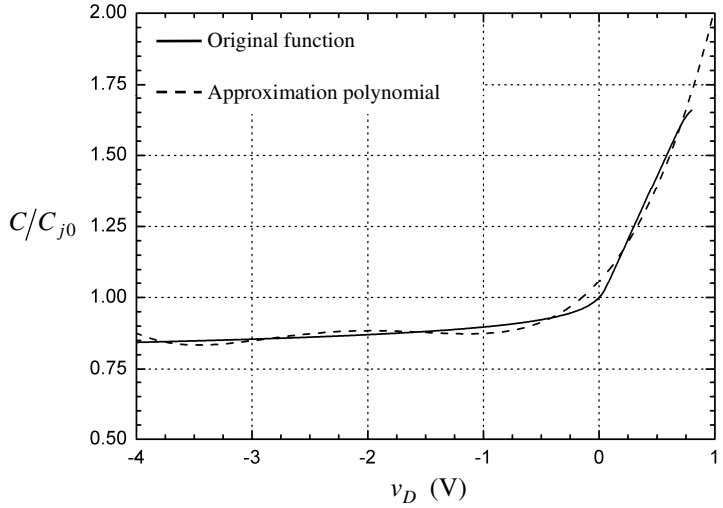


Figure 3.8: Approximation polynomial and original function of the capacitance-voltage characteristic for the Schottky diode BAT15-03W.

Knowing that the diode voltages are given by (3.10), the effective capacitance C_j is given accordingly to (3.9) as

$$C_j = C_{j0}\left[a_0 - 2a_1\left(\frac{v_R}{N}\right) + 3a_2\left(\left(\frac{v_R}{N}\right)^2 + \frac{V_0^2}{2}\right) - 4a_3\frac{v_R}{N}\left(\left(\frac{v_R}{N}\right)^2 + \frac{3}{2}V_0^2\right) + 5a_4\left(\left(\frac{v_R}{N}\right)^4 + 3\left(\frac{v_R}{N}\right)^2 V_0^2 + \frac{3}{8}V_0^4\right)\right] . \quad (3.24)$$

Furthermore, the AC source voltage amplitude and frequency are set to 1 V and 1 GHz, respectively. Likewise, the capacitance Cc and the load resistance are set to 1 nF and 10 kΩ, respectively. The simulated and the calculated input impedances are depicted in Figure 3.9. As expected from (3.23), the absolute value of the input resistance R_N and reactance X_N decreases as the number of diodes increases. The slight differences between the calculated and the simulated values are due to an error caused by approximating the diode capacitance-voltage characteristic. The resulting relative error is about 9% for the input resistance and less than 4% for the reactance. These discrepancies can be explained as follows: the value of v_R used in (3.15) is an approximated value, since R_s is not taken into account in (2.28). Since v_R is included in the argument of the exponential function, slight inaccuracies resulting from the

calculation of v_R can cause significant errors in the calculation of G_{D_1}, and consequently in the calculation of R_N and X_N.

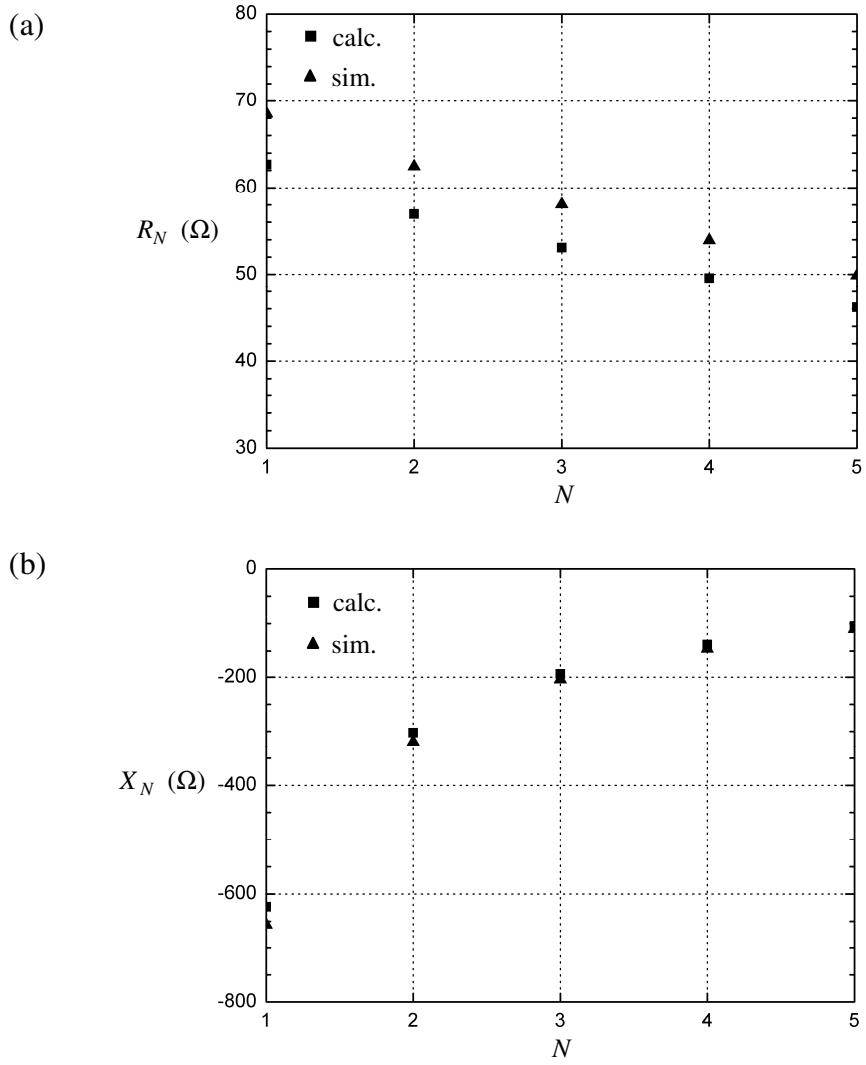


Figure 3.9: Calculated and simulated rectifier input (a) resistance and (b) reactance with respect of the number of diodes.

3.2.4 NONLINEARITY

The expressions in (3.14) and (3.15) show that the rectifier input impedance Z_N is non-linear. The influence of the AC source voltage amplitude V_0 is to be investigated. For this purpose, a voltage doubler including the aforementioned Schottky diodes BAT15-03W are analyzed. Figure 3.10 shows the analytically calculated and the simulated input resistance and reactance of the circuit. In a general manner, one can say that the higher the amplitude V_0, the higher the resistance R_N. At the same time, the absolute value of the reactance X_N increases slightly. The reasons for the discrepancies

between calculated and simulated values have already been discussed in Subsection 3.2.3.

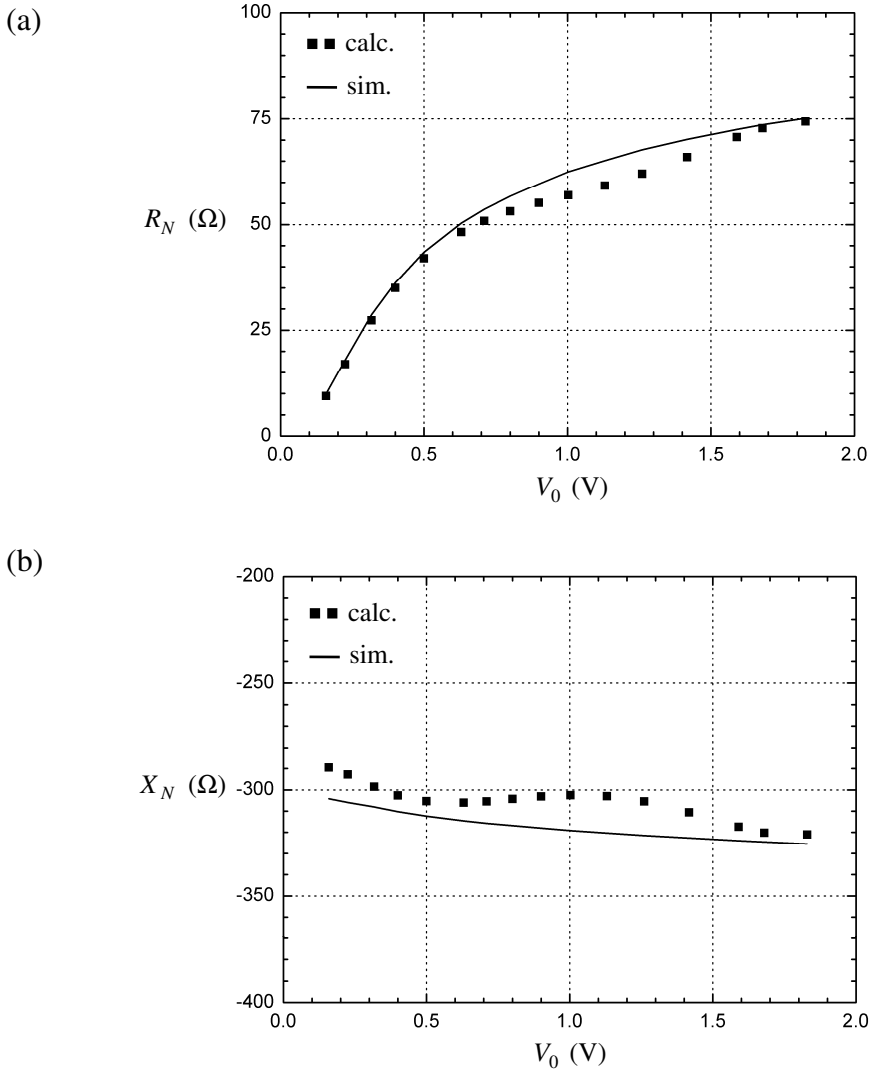


Figure 3.10: Input (a) resistance and (b) reactance as function of the AC source voltage amplitude.

It should be clearly stated that the rectifier input impedance described in (3.23) cannot be measured using common network analyzers. Actually, in the analysis made in Section 3.2, the circuit excitation is achieved by an ideal AC voltage source, which has a zero internal impedance. However, measurement ports of common network analyzers have non-zero internal impedance and thus, would cause at the rectifier input a spectral current amplitude distribution that differs from the above analysis. In this case, the developed equations are no longer valid. As such, it is not possible to have compact mathematical expressions for the achieved DC output voltage and the diode admittances. Therefore, the determination of the rectifier input impedance depends basically on the values of the internal impedance of the network analyzer measurement port at all harmonics $m \cdot f_0$, where $m = 0, 1, \ldots, \infty$.

3.3 ANTENNA SUPPLIED RECTIFIERS

Contrary to the previous analyses, the signal to rectify does not flow from a voltage source in field-supplied systems, but from one or several antennas. In this section, the feeding of rectifiers by one antenna is analyzed. Formulas to describe the rectifier output voltage as well as the input impedance will be sought under particular assumptions. The effects of the system nonlinearity and the influence of the breakdown on the rectifier performances will be presented. Finally, the system sensitivity will be analyzed and discussed.

3.3.1 ANTENNA REQUIREMENTS

In transponder systems, the tag antenna receives the electromagnetic waves sent by the interrogator and feeds the rectifier input.

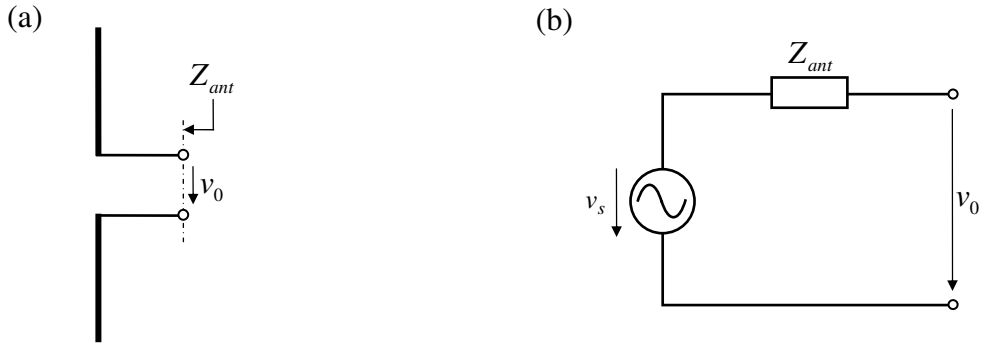


Figure 3.11: (a) Antenna and (b) its equivalent Thévenin model.

As depicted in Figure 3.11, the tag antenna is described by its equivalent Thévenin model consisting of an impedance Z_{ant} and an ideal AC voltage source with a voltage amplitude V_s [46]. The impedance Z_{ant} in Figure 3.11 (b) is the internal impedance of the antenna at the signal frequency f_0. Furthermore, the amplitude V_s of the AC voltage source is given by

$$V_s = \sqrt{8 R_{ant} P_a}\,, \tag{3.25}$$

where R_{ant} is the real part of Z_{ant} and P_a is the available signal power at the transponder antenna [18].
In Section 3.2, the rectifier input impedance at the fundamental frequency has been calculated under the assumption that the circuit is fed by an AC voltage source whose internal impedance is zero at all frequencies. Equations (3.7) and (3.12) show that when a monofrequent voltage is applied at the rectifier input, the delivered current has components at all harmonic frequencies $m \cdot f_0$, where $m = 0, 1, \ldots, \infty$. For illustration,

a single-stage rectifier supplied by a monofrequent voltage source is considered. The resulting infinitely wide comb structure of the source current magnitude spectrum shown in Figure 3.12 is a typical answer of non-linear systems excited by a monofrequent signal.

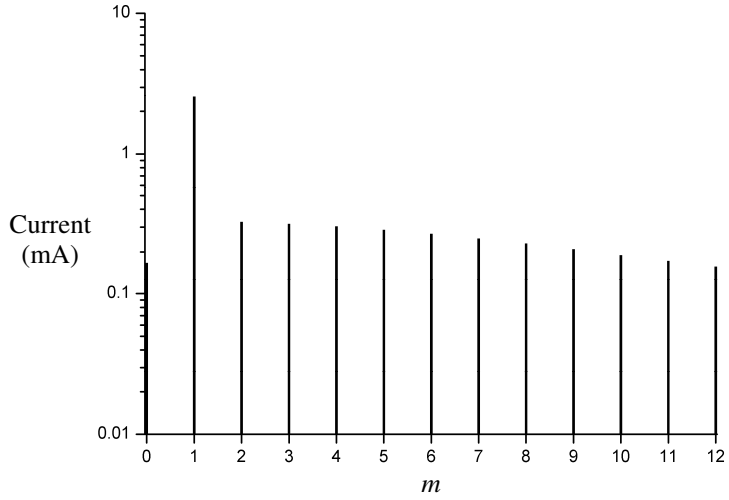


Figure 3.12: Voltage source current for $V_0 = 2$ V, $I_s = 10$ nA, $n = 1$, $f = 1$ GHz and $R = 10$ kΩ.

Therefore, if a rectifier is fed by an antenna, the antenna internal impedance will cause voltage components with an infinitely wide magnitude spectrum at the rectifier input, making further mathematical analysis with compact expressions no longer possible. Hence, to use the formalism developed in Chapter 2 and in Section 3.2, it is necessary that a monofrequent voltage drops at the rectifier input. To realize this condition, the antenna impedance should act as short-circuit at all harmonics except at the signal frequency. This is

$$Z_{ant} = \begin{cases} Z_a & \text{for } m = 1 \\ 0\Omega & \text{for } m \neq 1 \end{cases}, \tag{3.26}$$

where Z_a is the targeted antenna impedance at the signal frequency.

3.3.2 SOURCE CONFIGURATION

In a general manner, the condition (3.26) cannot be technically fulfilled by designing an antenna. Hence, it is necessary to achieve a further configuration after designing a transponder antenna with the internal impedance Z_a at the signal frequency. On one hand, the realization of an ideal configuration, where (3.26) is exactly fulfilled, will be investigated. On the other hand, alternative configurations permitting an approximation of (3.26) will be analyzed. Both solutions will then be discussed.

3.3.2.1 IDEAL CONFIGURATION

A method to fulfill (3.26) consists of connecting an antenna with the impedance Z_a at the signal frequency in parallel with an inductance L_0 and several serial resonant circuits consisting in each case of an inductance L_m and a capacitance C_m, as depicted in Figure 3.13.

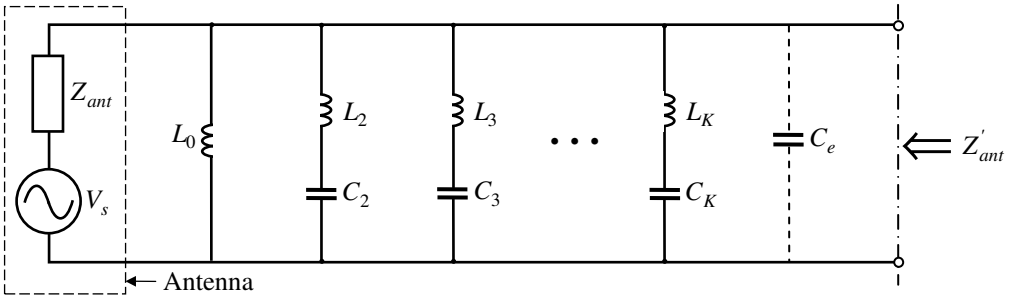


Figure 3.13: Ideal and first suboptimal source configuration.

The inductor L_0 acts as short circuit for $m = 0$. Each serial resonant circuit $L_m C_m$ acts as short circuit at the resonance frequency

$$m \cdot f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{L_m C_m}} \quad , \tag{3.27}$$

where $m \neq 1$. Theoretically, the number K of required serial resonant circuits should be infinite, since the spectrum of the source current is also infinitely wide. Furthermore, it should be ensured that each capacitance C_m is small enough to keep the corresponding resonant circuit high-impedance at the signal frequency given the fact that C_m and L_m are chosen to fulfill (3.27). Therewith the source impedance Z'_{ant} seen by the rectifier meets exactly the condition (3.26).

3.3.2.2 SUBOPTIMAL SOLUTIONS

The major disadvantage of the method described above is that the number K should be infinite. Therefore, the following practical but suboptimal solution is proposed: a finite number K of serial resonant circuits could be used so that $m = 0 \cdots K$, where $m \neq 1$. To short circuit the antenna at harmonics higher than Kf_0, a shunt capacitance C_e should be added in parallel to the resonant circuits, as shown in Figure 3.13. For this approach, K should be chosen high enough to ensure an almost monofrequent voltage at the rectifier input. At the same time, the capacitance C_e should be kept small to not affect the source impedance Z'_{ant} at the signal frequency significantly.

A second suboptimal method to nearly fulfill the condition (3.26) is to connect the antenna with the required impedance Z_a at the signal frequency in parallel with only

one parallel resonant circuit including an inductance L_1 and a large capacitance C_1 as shown in Figure 3.14.

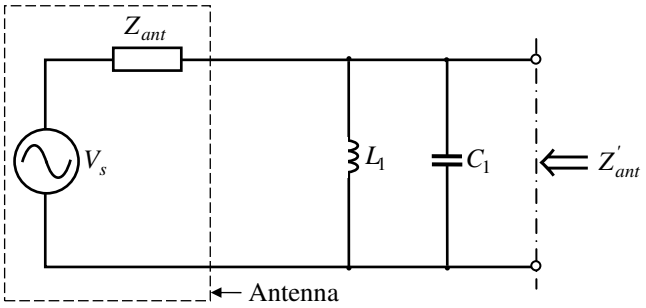


Figure 3.14: Second suboptimal source configuration.

The values of L_1 and C_1 are chosen so that the resonance frequency of the resonant circuit corresponds to the signal frequency f_0:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{L_1 C_1}}\,. \tag{3.28}$$

Similarly to the previous method, the inductance L_1 acts as short circuit for $m = 0$. At the signal frequency, that is for $m = 1$, the resonant circuit acts as open circuit, thus the rectifier input sees the source impedance Z_a. Furthermore, the shunt capacitance C_1 should be large enough to suppress voltage spectral components at higher harmonics, that is for $m \geq 2$. This method offers the advantage that only two devices are needed. However, the shape of the resonance curve of the resonant circuit should be very peaked to ensure very low value of $\left|Z'_{ant}\right|$ already at the harmonic $2f_0$. Additionally, it requires a high behavior reliability of the capacitance C_1 over a theoretically infinitely wide frequency range.

3.3.3 INPUT IMPEDANCE ANALYSIS

To maximize the rectified output voltage, it is necessary to achieve a power matching at the rectifier input, that is, at the antenna output. In the practice, this is done by measuring the input impedance of the rectifier input for diverse available powers. Then, an antenna with the corresponding conjugate complex impedance is connected to the rectifier input. However, the experimental determination of the rectifier input impedance is a well-known critical issue due to the following reasons: most transponders are integrated circuits. Hence, wafer probers are required to perform the measurements. Another difficulty is due to the nonlinearity of the circuit. This leads to the interdependence between the input impedance and the absorbed power. To solve this problem, the rectifier circuits are often characterized using measurement setups

including computer-controlled load pull tuners. Therewith the achieved rectified voltage can be measured and stored for each performed combination of measurement port impedance and incident power. Hence, for a particular incident power, the optimal antenna impedance is reached where the rectified voltage is the highest. This method is obviously time consuming and cost-expensive. Furthermore, the realized port impedances are mostly controlled only at the fundamental frequency. This restriction does not permit a realistic behavior prediction of the rectifier while fed by an antenna with unknown impedances at higher harmonic frequencies. In this subsection, the input impedance of the rectifier is analytically investigated under the assumption, that the condition (3.26) is fulfilled.

Based on the model depicted in Figure 3.11, the amplitude V_0 of the monofrequent voltage v_0 provided by the antenna at the rectifier input can be calculated using Figure 3.11 as

$$\begin{aligned} V_0 = V_s \left| \frac{Z_N}{Z_N + Z_a} \right| &= \sqrt{8 R_a P_a} \left| \frac{R_N + jX_N}{(R_N + R_a) + j(X_N + X_a)} \right| \\ &= \sqrt{8 R_a P_a \frac{R_N^2 + X_N^2}{(R_a + R_N)^2 + (X_a + X_N)^2}} \end{aligned}, \tag{3.29}$$

where $R_a = \Re\{Z_a\}$, $X_a = \Im\{Z_a\}$, $R_N = \Re\{Z_N\}$, and $X_N = \Im\{Z_N\}$. The power matching at the antenna-rectifier interface is expressed as:

$$Z_N = Z_a^* \Leftrightarrow (R_N = R_a \text{ and } X_N = -X_a), \tag{3.30}$$

where Z_a^* is the complex conjugate of the antenna impedance. Inserting (3.30) in (3.29) leads to the amplitude V_0 as

$$V_0 = \sqrt{2 R_a P_a} \sqrt{1 + \left(\frac{X_a}{R_a} \right)^2} . \tag{3.31}$$

Therefore, for a given available power P_a, the simultaneous calculation of the DC output voltage and the rectifier impedance by power matching can be done by solving the following system of equations including (3.31), (3.23), (3.15), (3.14) and (2.28) as

$$\begin{cases} V_0 - \sqrt{2R_N P_a}\sqrt{1+\left(\dfrac{X_N}{R_N}\right)^2} = 0 \\ R_N - \dfrac{1}{N}\left(R_s + \dfrac{G_D}{G_D^2 + B_D^2}\right) = 0 \\ X_N - \dfrac{1}{N}\left(\omega_0 L - \dfrac{B_D}{G_D^2 + B_D^2}\right) = 0 \\ G_D - \dfrac{2I_s}{V_0} e^{\frac{-v_R}{NnV_T}} I_1\left(\dfrac{V_0}{nV_T}\right) = 0 \\ B_D - \omega_0 C_{j0}\left[a_0 - 2a_1\left(\dfrac{v_R}{N}\right) + 3a_2\left(\left(\dfrac{v_R}{N}\right)^2 + \dfrac{V_0^2}{2}\right) - \cdots\right] = 0 \\ e^{\frac{v_R}{NnV_T}}\left(\dfrac{v_R}{RI_s} + 1\right) - I_0\left(\dfrac{V_0}{nV_T}\right) = 0 \end{cases} . \tag{3.32}$$

After solving (3.32) and using (3.30), the required antenna impedance for power matching can be directly deduced.
Cockcroft-Walton rectifiers including one, two, and three Schottky diodes BAT15-03W have been analyzed. Figure 3.15 depicts the DC output voltage as well as the input impedance as functions of the available power.
As expected from Figure 3.10 (a), Figure 3.15 shows that the impedance real part R_N grows significantly with the available power P_a, while the absolute value of the imaginary part increases moderately. The curves have been interrupted at the input power, where the corresponding rectified voltage is the highest, due to the limiting effect of the diode breakdown voltage. For this case, the suitable analysis is treated in Subsection 3.3.5.

Figure 3.15 (c) shows, that the less diode stages, the higher the DC output voltage. This is explained by power matching: the available power at the antenna is completely absorbed by the rectifier, whereby a part of the absorbed power is dissipated in the diodes and the remaining is provided to the load resistance. Hence, more diodes on the power path means more dissipated power in the diodes and thus, less power provided to the load resistor [7]. The latter fact results in a decrease of the rectified voltage. The influence of diode number N on the rectified voltage is more notable at low available power, since the relative differences between the rectified voltages are more significant than at higher available power, where the provided power in the load resistance is much higher than the dissipated power in the diodes. In the latter case, this results in the rectified voltages being almost identical. Therefore, low-power applications should use single-stage rectifiers to perform DC voltage supply in field-powered modules. However, the higher the diode number N, the lower the resistance R_N, and the absolute value of the reactance X_N. This could facilitate the realization of power matching to the antenna and thus, the voltage loss due to the high number of diodes could be compensated and even exceeded by an eventually better input power matching.

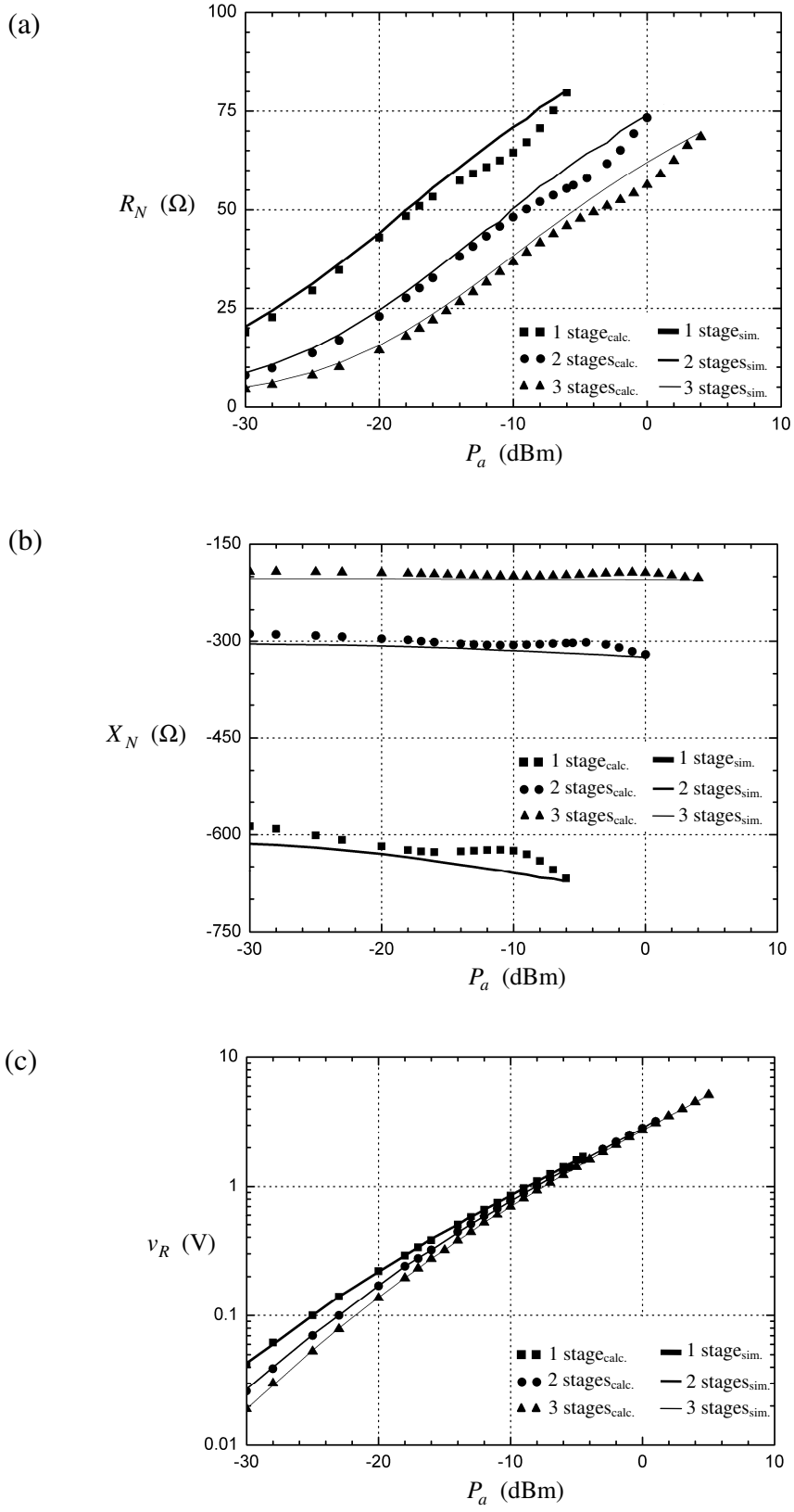


Figure 3.15: (a) Input resistance and (b) reactance; (c) output DC voltage.

Furthermore, in cases where the minimum required DC voltage cannot be achieved by a single-stage rectifier because of its breakdown voltage, a diode number N greater than unity is necessary, as already argued in Section 2.5. Thus, the choice of the diode number depends on the application to run and the targeted conversion efficiency. The optimal trade-off should be examined in each case.

3.3.4 INFLUENCE OF THE ANTENNA IMPEDANCE ON THE RECTIFIER PERFORMANCES

For any antenna impedance Z_a, the rectifier performances can be calculated by solving (3.32) after replacing its first equation by (3.29). The resulting system of equations provides more accurate values than the method proposed in [38].
To illustrate how both the rectifier input impedance and the DC output voltage are affected by the antenna impedance, a voltage doubler and a voltage tripler including the Schottky diode BAT15-03W have been analyzed, whereby the available power has been set to $P_a = 0$ dBm in each case. For each circuit, the antenna resistance R_a and reactance X_a have been tuned around the optimal values $R_{a,opt} = R_{N,opt}$ and $X_{a,opt} = -X_{N,opt}$, where $R_{N,opt}$ and $-X_{N,opt}$ are the rectifier input resistance and reactance by power matching obtained by solving (3.32) and depicted in Figure 3.15. In Figure 3.16, the resulting behavior of R_N, X_N and v_R can be observed. In the latter case, $v_{R,opt}$ is the DC output voltage by input power matching, calculated using (3.32) and shown in Figure 3.15 (c). It is notable that R_N is much more affected by the antenna reactance mismatch than by the antenna resistance mismatch, while X_N is generally almost non sensitive to the antenna impedance mismatch. It results that v_R is more dependent on the antenna reactance than on its resistance. Hence, the reactance should be accurately optimized to enhance the AC-to-DC conversion when designing the transponder antenna. Furthermore, one can conclude that the relative alterations of the rectifier performance due to input impedance mismatch have the same tendencies regardless of the diode number N.

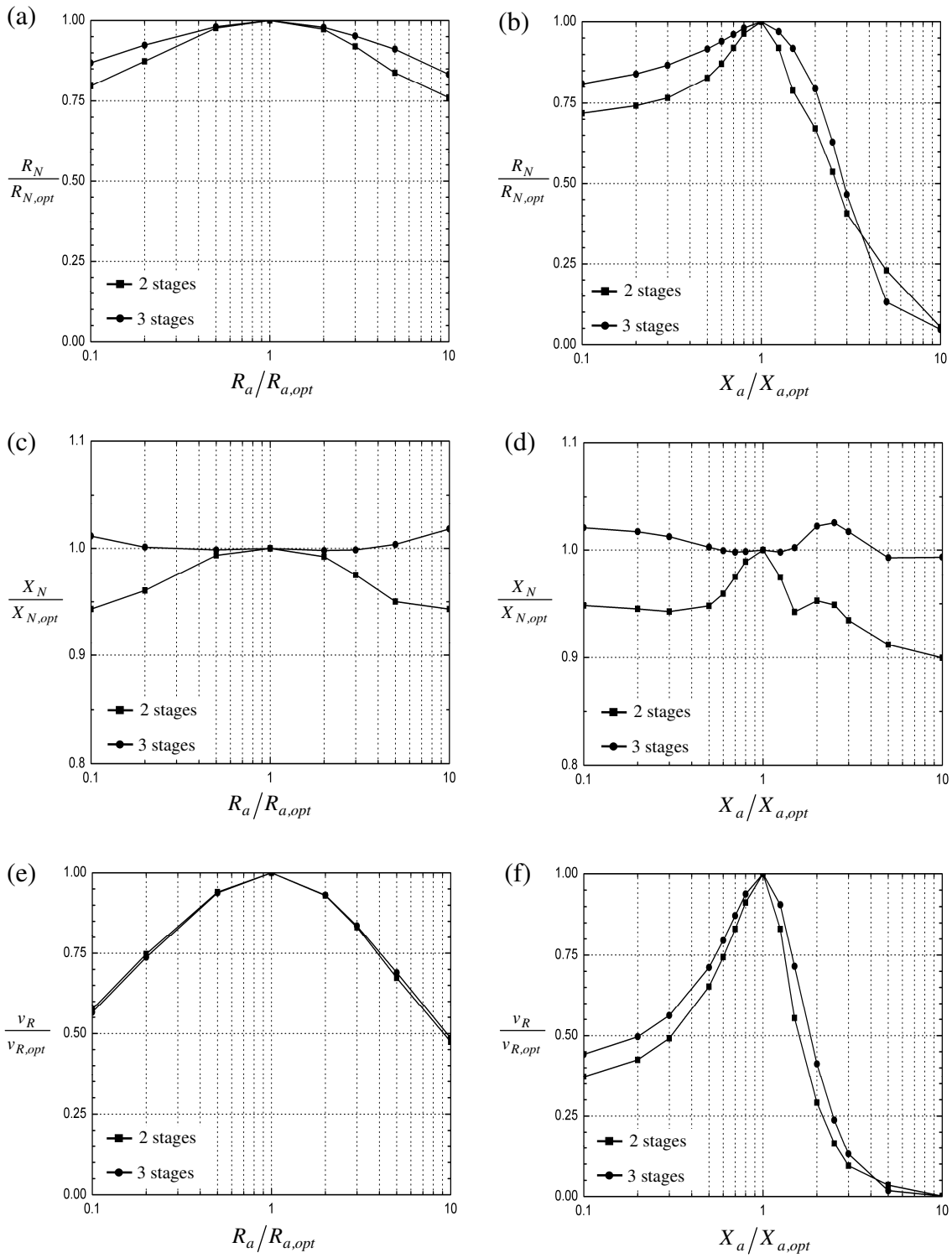


Figure 3.16: Alterations of the rectifier (a)-(b) relative input resistance, (c)-(d) relative input reactance and (e)-(f) relative DC output voltage due to power mismatch at the rectifier input.

3.3.5 BREAKDOWN VOLTAGE

In Figure 3.15, the curves have been interrupted at the input power, where the rectified voltage is maximum, that is for $v_R = v_{R,max}$, whereby $v_{R,max}$ is obtained from (2.38). Above this value, the rectifier behavior cannot be described using (3.32), therefore the analytical description of the rectifier input impedance Z_N is sought for this case, under the assumption that the diodes do not burn out and still behave according to the model proposed in Section 2.6.
When the voltage saturation due to the limiting effect of the breakdown voltage arises, the DC voltage across each diode is considered as power independent and equal to $v_{R,max}/N$. Thus, the sixth equation in (3.32) is no longer valid. Under the assumption of power matching at the rectifier input, the occurring input impedance can be determined by solving the system of equations:

$$\begin{cases} V_0 - \sqrt{2R_N P_a}\sqrt{1+\left(\dfrac{X_N}{R_N}\right)^2} = 0 \\ R_N - \dfrac{1}{N}\left(R_s + \dfrac{G_D}{G_D^2 + B_D^2}\right) = 0 \\ X_N - \dfrac{1}{N}\left(\omega L - \dfrac{B_D}{G_D^2 + B_D^2}\right) = 0 \\ G_D - \dfrac{2I_s}{V_0} e^{\frac{-v_{R,max}}{NnV_T}} I_1\left(\dfrac{V_0}{nV_T}\right) = 0 \\ B_D - \omega_0 C_{j0}\left[a_0 - 2a_1\left(\dfrac{v_{R,max}}{N}\right) + 3a_2\left(\left(\dfrac{v_{R,max}}{N}\right)^2 + \dfrac{V_0^2}{2}\right) - \cdots\right] = 0 \end{cases} . \qquad (3.33)$$

A single-stage rectifier including the Schottky diode BAT15-03W has been analyzed for verification. The diode breakdown voltage is $B_V = 4$ V. The maximum DC output voltage is calculated to $v_{R,max} = 1.86$ V for the load resistance $R = 10$ kΩ. The resulting input resistance and reactance are depicted in Figure 3.17 (a) and in Figure 3.17 (b), respectively. In Figure 3.15 (c), the maximum voltage $v_{R,max}$ is reached at the available power $P_a = -5$ dBm. Passed this value, the curve of the DC output is obviously horizontal as plotted in Figure 3.17 (c). This voltage self-stabilization mechanism may be advantageous in transponder circuits, where an additional voltage regulator is often located between the rectifier and the logic unit in order to keep the voltage in a specific range, or under a critical value [13, 67]. Here, the critical value is directly given by the breakdown voltage. In the voltage saturation zone, the curves shape of the input resistance and reactance change drastically. It is notable that in this case, the rectifier input becomes less capacitive as the available power is increased.

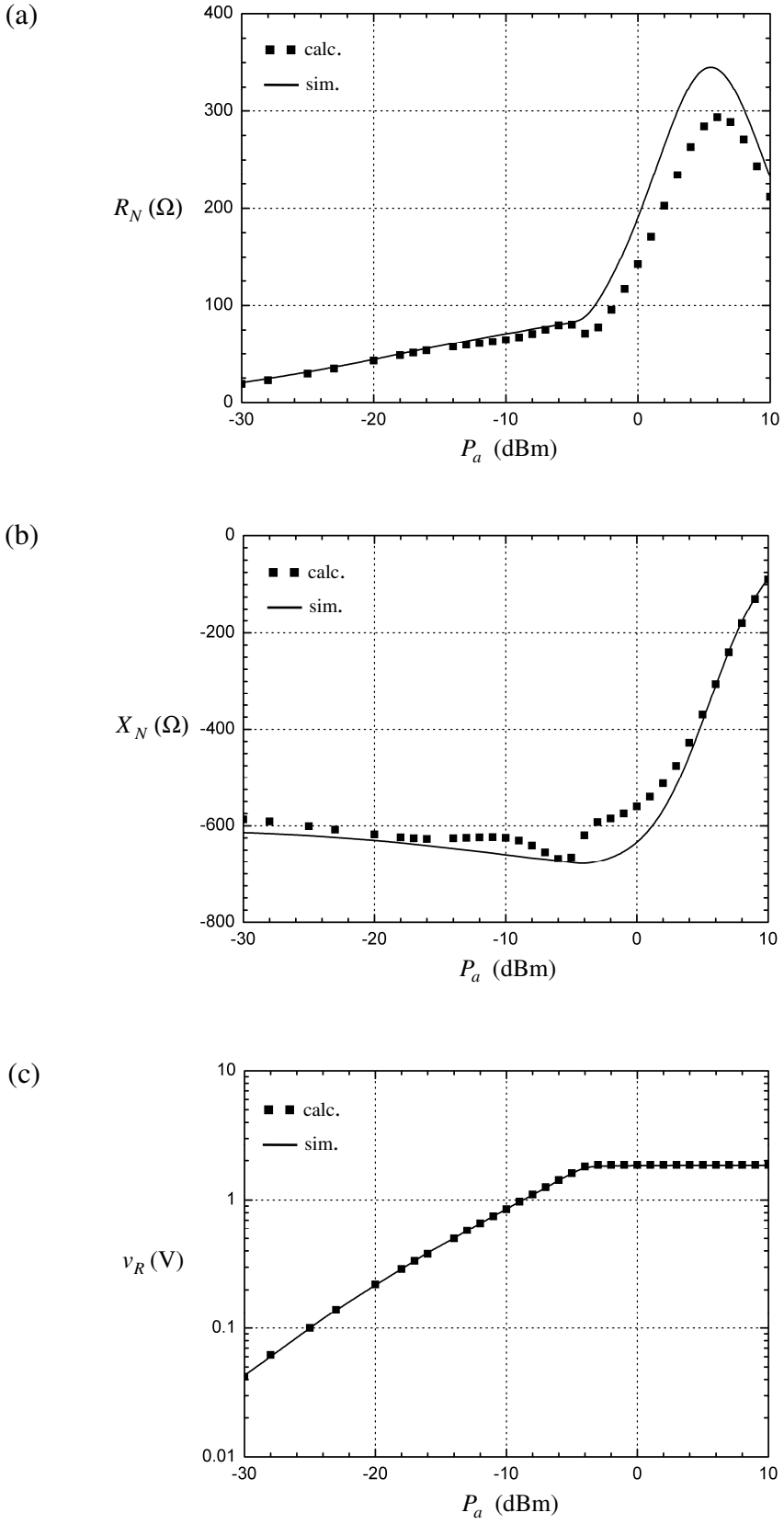


Figure 3.17: (a) Input resistance, (b) input reactance and (c) rectified voltage under consideration of the diode breakdown voltage.

3.3.6 OVERALL CONVERSION EFFICIENCY

Other than in (2.76), the overall conversion efficiency η_{ov} is defined as [29, 56]

$$\eta_{ov} = \frac{\text{output power}}{\text{incident power}}. \tag{3.34}$$

The incident power is the available power at the transponder antenna. Hence, (3.34) is

$$\eta_{ov} = \frac{P_R}{P_a} = \frac{v_R^2 / R}{P_a}. \tag{3.35}$$

Assuming input power matching for this analysis, the available power P_a is entirely absorbed by the rectifier circuit. Consequently, the available power P_a is the sum of the dissipated power in the diodes as well as in the load resistance. Thus, the overall conversion efficiency by input power matching corresponds to the efficiency defined in (2.76).
Using (3.35) and Figure 3.17 (c), the overall efficiency of the single-stage rectifier mentioned in Subsection 3.3.5 has been calculated and is plotted in Figure 3.18.

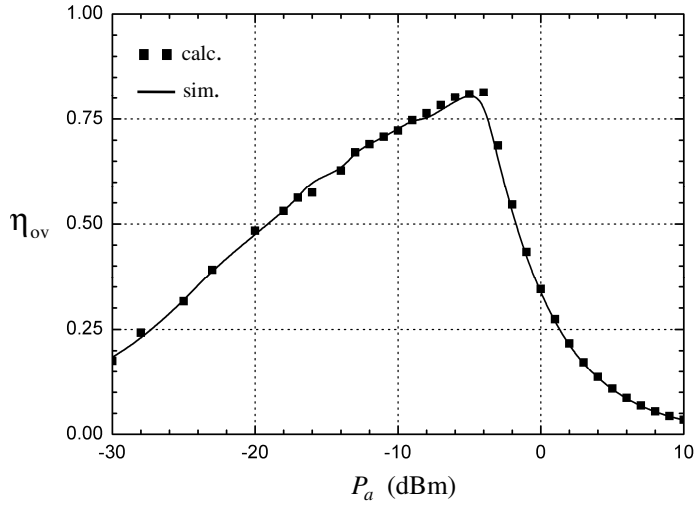


Figure 3.18: Overall conversion efficiency for B_V = 4 V.

Figure 2.27 (a) has shown that the higher the amplitude V_0, the higher the achieved efficiency. The same behavior is observed in Figure 3.18 before the maximum DC output voltage $v_{R,max}$ is reached, this is for $P_a \leq$ -4 dBm. Beyond this power, the output power P_R remains constant. Therefore, the overall conversion efficiency stops rising at this point, but decreases proportionally to the inverse of the available power. Based on

this fact, one can say in a general manner, that the higher the diode breakdown voltage, the higher the achievable overall conversion efficiency.
Furthermore, for $v_R \leq v_{R,max}$ and by input power matching, the efficiencies given by (3.34) and (2.76) are identical; however, contrary to the situation in Subsection 2.9.2, the voltage amplitude V_0 depends on the load resistance for antenna fed rectifiers. Thus, (2.68) and (2.79) are not valid here. Consequently, the load resistance $R_{\eta_{max}}$ leading to the maximum efficiency cannot be calculated using (2.80). Nonetheless, an approximate value of $R_{\eta_{max}}$ can be numerically obtained by solving (3.32) iteratively.

3.4 CONCLUSION

The capacitance-voltage characteristic of the diode capacitance can be accurately approximated using a high order polynomial. As such, the calculation of the input impedance of voltage multiplying rectifiers, excited by an ideal AC voltage source or by a particularly configured antenna, is analytically possible. For a given incident power, Cockcroft-Walton rectifiers, Dickson charge pumps and Greinacher rectifiers including identical diode type and number have identical input impedance. Input power mismatch due to disadvantageous antenna reactance decreases the DC output voltage more than disadvantageous antenna resistance. As well, the diode breakdown voltage is a major limiting factor to the achievable DC output voltage and to the rectifier overall conversion efficiency.

4 WAVE PROPAGATION AND MODULATION

In the present chapter, the signal flow between the interrogator and each transponder is analyzed, and a modulation method for the transponder is developed. Due to the relation between the antenna size and the signal frequency investigated in Section 5.2, only the UHF and the microwave range will be considered. Thus, the field coupling between the interrogator and each transponder takes place as wave propagation.
A typical transponder application with wave propagation is illustrated in Figure 4.1: an interrogator or reader sends an electromagnetic wave in the free space. The transponders located in the interrogator environment receive the signal and send information back to the interrogator [16, 17].

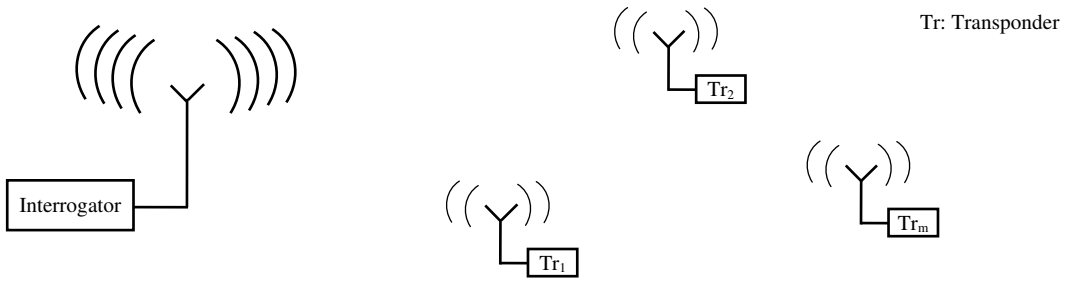


Figure 4.1: Interrogator-transponder links.

One distinguishes basically passive, semi-active and active transponders, which differ from each other in the art, how the logic unit is fed and how they send the information. As announced in the introduction of this work, the focus is set on passive or also called field-powered transponders.
Passive transponders include neither batteries nor any other kind of energy source. Thus, they are totally dependent on the interrogator, whose transmitted signal is partially converted by the rectifier of the transponder to supply its logic unit [17].

Consequently, if the transmitted interrogator signal does not provide sufficient power to run a local oscillator, passive transponders cannot generate electromagnetic waves to send information. Hence, instead of generating signals, passive transponders operating in UHF and microwave ranges reflect a part of the received electromagnetic wave, also called incident wave, by modulating it according to the bit stream to send [21]. This

method of data transmission is called “electromagnetic backscatter coupling”. Therefore, the basic block diagram of a passive microwave transponder consists of an antenna, a rectifier, a logic unit and a modulator, as shown in Figure 4.2 [65].

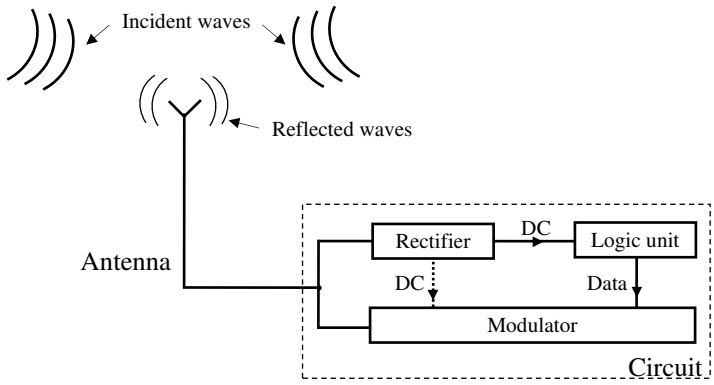


Figure 4.2: Transponder block diagram.

The antenna receives the transmitted electromagnetic waves and delivers an AC voltage at the rectifier input. The rectifier generates at its output a DC voltage to run the logic unit, which consists usually of a microcontroller or a state machine. Depending on the system design, the modulator can be fed by the rectifier as well. The logic unit activates the modulator depending on the actual bit to be sent. The modulator tunes the input impedance of the circuit and thus performs a controlled power mismatch at the antenna termination.
The basic principles of the electromagnetic backscatter coupling and methods to perform it using the rectifier topologies analyzed in the previous chapters are the addressed issues of the next sections.

4.1 LINK BUDGET

Based on Figure 4.1, the communication power flow including interrogator transmitted power, transponder received power, transponder reradiated power, and interrogator received power is illustrated in Figure 4.3 [17].

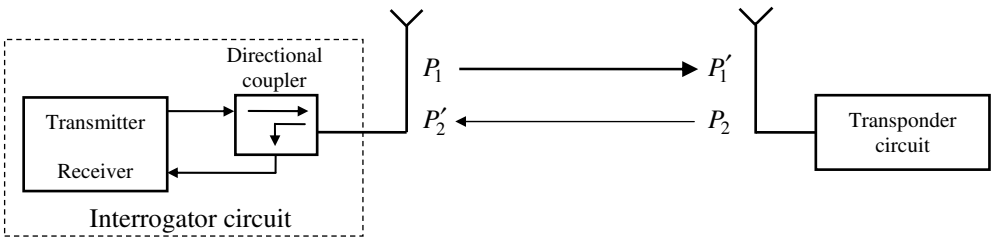


Figure 4.3: Power flow between interrogator and transponder.

4.1.1 INTERROGATOR TRANSMIT POWER

The interrogator consists mainly of a transmitter and a receiver path. For single-antenna systems, both paths are connected to the same antenna over a directional coupler, which separates the received from the transmitted signal. The radiated power P_1 is set by a combination of practicability and national or international regulations. Many RFID systems operate in a spectrum set aside for unlicensed use by the governmental body or international commissions that regulates radio operation in a given jurisdiction. Table 4.1 gives some values for UHF and microwave frequencies [17].

Frequency	Power
868 MHz (Europe: RFID)	2 W ERP
915 MHz (USA)	2 W ERP
2.45 GHz (Europe: RFID)	4 W EIRP
5.8 GHz (Europe)	5 W ERP
24 GHz ISM	0.1 W ERP

Table 4.1: Worldwide regulations in the UHF, 2.45 GHz, 5.8 GHz and 24 GHz bands.

The mention ERP (Equivalent Radiated Power) gives the product of a really radiated power P with the interrogator antenna gain G_T, whereby the interrogator antenna gain is related to the ideal radiating half-wave dipole. Hence, one has

$$ERP(\mathrm{W}) = \frac{G_T P(\mathrm{W})}{1.64}, \tag{4.1}$$

where G is related to the isotropic spherical radiator. When the power P is given in dBm, (4.1) is equivalent to

$$ERP(\mathrm{dBm}) = P(\mathrm{dBm}) + G_T(\mathrm{dBd}), \tag{4.2}$$

where

$$G_T(\mathrm{dBd}) = G_T(\mathrm{dBi}) - 2.16. \tag{4.3}$$

Furthermore, the term $EIRP$ is the Equivalent Isotropic Radiated Power and gives the product of a radiated power P with the interrogator antenna gain G_T, whereby interrogator antenna gain is related to the isotropic spherical radiator. Thus, $EIRP$ and ERP are related to each other through the equation:

$$ERP(\mathrm{dBm}) = EIRP(\mathrm{dBm}) - 2.16. \tag{4.4}$$

For linear scale, (4.4) is

$$ERP = \frac{EIRP}{1.64}. \tag{4.5}$$

Table 4.1 shows that the product of radiated power and transmit antenna gain is limited. Hence, the higher the antenna gain, the lower the maximum allowed radiated power.

4.1.2 PATH LOSS

A small proportion P_1' of the power radiated by the interrogator reaches the transponder antenna. The ratio of P_1' and P_1 is the free-space loss (FSL), also called path attenuation or path loss. FSL is usually referred to a_F. Its value depends on the distance r between the transponder and the interrogator antenna, the gain G_T and G_R of the transponder and interrogator antenna, respectively, and the frequency f of signal. Assuming optimal alignment of the interrogator and transponder antenna to each other, as well as isotropic lossless medium between them, the path loss a_F can be expressed by means of the Friis equation [17] as follows:

$$a_F = G_T G_R \left(\frac{\lambda}{4\pi r} \right)^2, \tag{4.6}$$

where λ is the wavelength of the electromagnetic signal. A common and convenient way to state the path loss is to express it in logarithmic scale as

$$a_F(\text{dB}) = -147.6 + 20log(r) + 20log(f) - 10log(G_T) - 10log(G_R), \tag{4.7}$$

where f and r have the unit Hz and m, respectively. Therewith by power matching at the transponder antenna, the transponder received power P_1' is

$$P_1' = P_1 G_T G_R \left(\frac{\lambda}{4\pi r} \right)^2. \tag{4.8}$$

4.1.2.1 IMPEDANCE MISMATCH

The received power predicted by the Friis transmission equation could, in practice, be further reduced by impedance mismatch between the antenna and the transponder chip. The impedance mismatch may be a consequence of the so-called tag detuning, which is due to the fact that antenna characteristics change when the transponder is placed on different objects or when other objects are present in the vicinity of the transponder. Furthermore, tag detuning degrades antenna gain and thus affects the communication range. Finally, as it will be discussed in Section 4.2, antenna impedance mismatch can be intentionally raised to transmit data [59].

4.1.2.2 ABSORPTION

Because most transponder systems are deployed indoors and there is not always a line-of-sight path between the transponder and the interrogator, the free-space assumption is usually not valid. The electromagnetic wave supplying transponders with power may be totally reflected by perfect metallic objects and partially reflected by dielectrics. Real-world lossy dielectrics between transponder and interrogator antennas will also absorb some of the radiated power. In practice, it results from these effects, that the effective path loss and thus the read range can be significantly less than predicted by (4.7).

4.1.2.3 MULTIPATH FADING

Even if there is a line-of-sight path between the interrogator antenna and the tag, small-scale fading effects can increase and decrease the read range. Multipath fading is caused by the interference between two or more versions of the transmitted interrogator signal, which arrive at the receiver at slightly different times. These multipath waves combine at the receiver to result in a signal that can vary widely in amplitude as well as in phase. Due to the constructive and destructive effects of multipath waves, a transponder moving past an interrogator antenna may pass through several fades in a small period of time. If the passive transponder passes through such a field null, it will lose power and eventually also its state [16].

4.1.2.4 POLARIZATION LOSSES

As well, the path loss and thus the read range is significantly reduced by polarization losses, because the orientation of transponders relative to the interrogator antenna is usually not known. Even if the interrogator radiates a circularly polarized wave, the transponder fails to be adequately powered when the axis of the transponder antenna is aligned with the propagation direction of the incident electromagnetic wave. Furthermore, emitting circularly polarized waves will introduce an additional loss of 3 dB, if the transponder antenna receives/radiates linear polarized waves. A promising approach to alleviate this orientation dependence is to use an interrogator and transponder antenna that both radiate circular polarized electromagnetic waves [16].

4.1.2.5 CHIP SENSITIVITY THRESHOLD

The chip sensitivity threshold is a critical range limitation. It is the minimum received RF power necessary to turn on the transponder chip. The lower it is, the longer the distance at which the transponder can be detected. Chip sensitivity is first defined by the RF front-end architecture and technological process. As described in (4.6) and (4.8), the antenna gain is another important limitation: communication range is at its highest in the direction of maximum directivity, which is fundamentally limited by the operation frequency and the size of the transponder antenna.
Using the Friis equation, and defining first the minimum power the transponder requires to operate as $P_{min,tag}$, the forward-link-limited range R_{fwd} is obtained as

$$R_{\text{fwd}} = \left(\frac{\lambda}{4\pi}\right)\sqrt{\frac{P_1 G_T G_R}{P_{min,tag}}} = \left(\frac{\lambda}{4\pi}\right)\sqrt{\frac{EIRP \cdot G_R}{P_{min,tag}}}\,. \tag{4.9}$$

R_{fwd} is the maximum distance from which the transponder receives just enough power to turn on and scatter back [16, 47].

4.1.3 REVERSE LINK BUDGET

Because of impedance mismatch, a portion of the incoming power P_1' is reflected and returned (reradiated) as power P_2 [31]. Assuming a power reflection coefficient T_b at the transponder antenna termination (T_b is also called backscatter transmission loss), the reflected power P_2 is given as

$$P_2 = P_1 T_b G_T G_R \left(\frac{\lambda}{4\pi r}\right)^2. \tag{4.10}$$

The reflected power P_2 is radiated into free space and thus is also subject to attenuation as described by (4.6). Hence, a small proportion of the power P_2 is picked up by the interrogator antenna as power P_2', which is given as

$$P_2' = P_1 T_b \left[G_T G_R \left(\frac{\lambda}{4\pi r}\right)^2 \right]^2. \tag{4.11}$$

Hence, the power received at the interrogator goes as the inverse fourth power of the distance and is proportional to the square of the antenna gains. The reflected signal therefore travels into the antenna connection of the interrogator in the backwards direction and can be decoupled using a directional coupler and transferred to the receiver input of an interrogator. The forward signal of the transmitter, which is stronger by powers of ten, is to a large degree suppressed by the directional coupler.
The interrogator sensitivity is another important parameter that defines the minimum level of the transponder signal the interrogator can detect and resolve. The sensitivity is usually defined with respect to a certain signal-to-noise ratio (SNR) or to an error probability at the receiver. Factors that can affect the interrogator sensitivity include among others receiver implementation details, communication protocol specifics, kind of modulation and interferences, including signals from other interrogators and transponders. As well, defining the minimum signal power for detection at the interrogator as $P_{\text{min,int}}$, one obtains the reverse-link-limited range R_{rev} as

$$R_{\text{rev}} = \left(\frac{\lambda}{4\pi}\right)\sqrt[4]{\frac{P_1 T_b G_T^2 G_R^2}{P_{min,int}}} = \left(\frac{\lambda}{4\pi}\right)\sqrt[4]{\frac{EIRP \cdot T_b G_T G_R^2}{P_{min,int}}}\,. \tag{4.12}$$

Hence, a bidirectional communication is possible only if the double condition

$$r \le R_{\text{fwd}} \quad \text{and} \quad r \le R_{\text{rev}} \tag{4.13}$$

is fulfilled. For the sake of completeness, it should be noted that on one side, a minimum power of the backscattered signal is required at the interrogator for a successful detection. On the other side, the interrogator demodulates the signal successfully only if a minimum modulation depth is ensured.

4.2 BACKSCATTER MODULATION

As already mentioned in Paragraph 4.1.2.1, impedance mismatch at the transponder antenna termination can be intentionally achieved to tune the reflection characteristics of the transponder antenna and by this way, to transmit data to the interrogator. This is called backscatter modulation, which is defined as a process where the transponder answers to an interrogator signal by modulating and reradiating the response signal at the same carrier frequency [33].

4.2.1 THEORETICAL BASICS

At the antenna-rectifier junction, the incident electromagnetic wave can be expressed by the phasor E_{inc} of its electric field as

$$E_{inc} = |E_0| \cdot e^{j\varphi_0}, \tag{4.14}$$

where φ_0 and $|E_0|$ are the phase and the magnitude of the electric field, respectively. At the antenna-rectifier junction, a reflection may take place if the antenna and the rectifier input are not power matched to each other. The phasor E_{ref} of the electric field of the reflected electromagnetic wave is given by

$$E_{ref} = \Gamma \cdot E_{inc} = |\Gamma| \cdot |E_0| \cdot e^{j(\varphi_\Gamma + \varphi_0)}, \tag{4.15}$$

where φ_Γ is the phase of input reflection coefficient Γ. Hence, the magnitude and phase of the electric field of the reflected electromagnetic wave depend on the magnitude and phase of the reflection coefficient Γ, respectively. For a complex antenna impedance Z_a, the circuit input reflection coefficient Γ is defined as

$$\Gamma = \frac{Z_N - Z_a^*}{Z_N + Z_a}, \tag{4.16}$$

where Z_N is the rectifier input impedance [31]. Using the resistance and reactance of

the antenna and circuit input, the reflection coefficient magnitude is given as

$$|\Gamma| = \sqrt{\frac{(R_N - R_a)^2 + (X_N + X_a)^2}{(R_N + R_a)^2 + (X_N + X_a)^2}}\,. \tag{4.17}$$

As well, the reflection coefficient phase φ_Γ is given by

$$\varphi_\Gamma = \arctan\left(\frac{X_N + X_a}{R_N - R_a}\right) - \arctan\left(\frac{X_N + X_a}{R_N + R_a}\right). \tag{4.18}$$

In the most cases, the impedance of the transponder antenna is defined by its geometry and substrate material and thus, is not electronically variable. Hence, the impedance mismatch leading to reflection characteristics alteration is usually done by detuning the circuit input impedance electronically. Methods to achieve amplitude and phase modulation are presented in the next subsections.

4.2.2 AMPLITUDE MODULATION

Without loss of generality, one assumes that the modulator can switch the circuit input impedance between two values $Z_{N,1} = R_{N,1} + jX_{N,1}$ and $Z_{N,2} = R_{N,2} + jX_{N,2}$. If the impedances $Z_{N,1}$ and $Z_{N,2}$ are chosen so that the magnitudes of the corresponding reflection coefficients are different, while the phases remain constant, that is [40]

$$|\Gamma_1| \neq |\Gamma_2| \quad \text{and} \quad \varphi_{\Gamma_1} = \varphi_{\Gamma_2}\,, \tag{4.19}$$

then a so-called "2-amplitude shift keying" (2-ASK) is realized.
A method to fulfill (4.19) is illustrated in Figure 4.4: first, one assumes $X_{N,1} = X_{N,2} = X_N$ with the condition that

$$X_N + X_a = 0\,. \tag{4.20}$$

Furthermore, one sets that $R_{N,1} = R_a + \Delta R_N$ and $R_{N,2} = R_a - \Delta R_N$, with the assumption

$$|\Delta R_N| \leq R_a\,, \tag{4.21}$$

since the input resistance of a passive circuit cannot be negative.

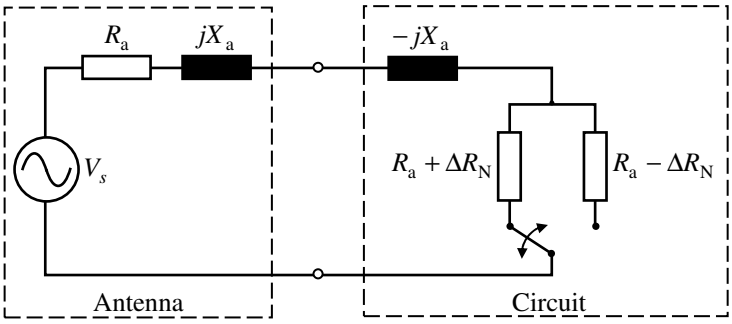


Figure 4.4: Switch of the circuit input resistance.

Using (4.17), the magnitude of the corresponding reflection coefficients results as

$$|\Gamma_1| = \left|\frac{\Delta R_N}{2R_a + \Delta R_N}\right| \quad \text{and} \quad |\Gamma_2| = \left|\frac{\Delta R_N}{2R_a - \Delta R_N}\right|. \tag{4.22}$$

As well, the respective phase can be calculated using (4.18) as

$$\varphi_{\Gamma_1} = \varphi_{\Gamma_2} = 0. \tag{4.23}$$

It is obvious that (4.22) and (4.23) fulfill the condition (4.19) if $|\Delta R_N| \neq 0$. This validates the proposed procedure.

Similarly to the analog amplitude modulation and according to (4.15), the modulation depth m_{mod} is defined as [17]

$$m_{\text{mod}} = \frac{\big||\Gamma_1| - |\Gamma_2|\big|}{|\Gamma_1| + |\Gamma_2|}. \tag{4.24}$$

To ensure data integrity during the transmission, it is necessary to increase the modulation depth and thus the difference $\Delta|\Gamma| = \big||\Gamma_1| - |\Gamma_2|\big|$ as much as possible. For this purpose, one assumes for the circuit input impedance the value $Z_N = R_N + jX_N$ and one sets: $R_N = R_a + \Delta R_N$. Equations (4.20) and (4.21) remain valid. Thus, it results for the corresponding phase: $\varphi_\Gamma = 0$.
The resulting reflection coefficient magnitude $|\Gamma|$ can be expressed using (4.17) as

$$|\Gamma| = \left|\frac{\dfrac{\Delta R_N}{R_a}}{2 + \dfrac{\Delta R_N}{R_a}}\right|. \tag{4.25}$$

Furthermore, the variable $\Delta R_N / R_a$ is swept between -1 and 1 according to (4.21). The resulting behavior of $|\Gamma|$ is depicted in Figure 4.5.

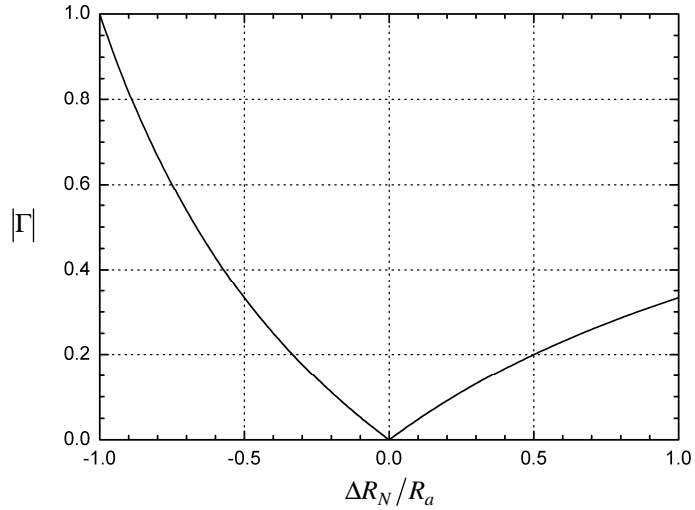


Figure 4.5: Reflection coefficient magnitude as function of $\Delta R_N / R_a$.

If the antenna impedance is optimized to match the circuit input at the first modulator state where $\Delta R_N / R_a = 0$, then the circuit input impedance is $R_a - jX_a$ and the reflection coefficient magnitude is consequently $|\Gamma| = 0$.

If the second state of the modulator sets the circuit input impedance so that $\Delta R_N / R_a \neq 0$, then a non-zero reflection coefficient will obviously take place, whereby the higher the parameter $|\Delta R_N / R_a|$, the higher the magnitude $|\Gamma|$. The maximum achievable magnitude difference between two modulator states is reached if in the second modulator state, the equation $\Delta R_N / R_a$ = -1 holds, bringing the circuit input impedance Z_N to $-jX_a$, where $|\Gamma| = 1$. In this particular case, as well as in all 2-ASK cases where in one modulator state, the reflection coefficient magnitude is zero, the highest possible modulation depth $m_{\text{mod}} = 1$ is achieved. The modulation is then called "on-off shift keying" (OOK).

For cases where the modulator switches the circuit input impedance between m different values, so that the resulting reflection coefficient magnitudes are all different from each other, a m-amplitude shift keying (m-ASK) is realized.

4.2.3 PHASE MODULATION

As well, it is assumed that the modulator switches the circuit input impedance between two different values $Z_{N,1}$ and $Z_{N,2}$. To realize a phase modulation, the following condition should be fulfilled:

$$|\Gamma_1| = |\Gamma_2| \quad \text{and} \quad \varphi_{\Gamma_1} \neq \varphi_{\Gamma_2} . \tag{4.26}$$

The requirement of equal reflection coefficient magnitudes is due to the fact that a phase modulated signal has a constant envelope [40].
A method to fulfill (4.26) is illustrated in Figure 4.6: the real part of the impedances $Z_{N,1}$ and $Z_{N,2}$ is set to the antenna resistance, that is $R_{N,1} = R_{N,2} = R_N$ with the additional condition

$$R_N - R_a \to 0 . \tag{4.27}$$

Furthermore, the imaginary parts are set as: $X_{N,1} = -X_a + \Delta X_N$ and $X_{N,2} = -X_a - \Delta X_N$, with the assumption: $\Delta X_N \neq 0$.

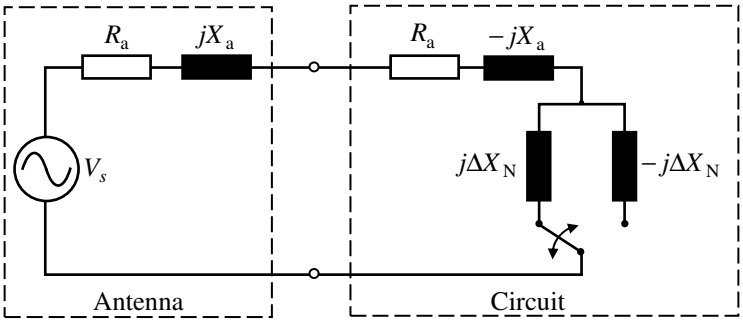


Figure 4.6: Switch of the circuit input reactance.

Therewith the reflection coefficient magnitude is the same for both modulator states:

$$|\Gamma_1| = |\Gamma_2| = \sqrt{\frac{(\Delta X_N)^2}{4R_N^2 + (\Delta X_N)^2}} . \tag{4.28}$$

The corresponding phases φ_{Γ_1} and φ_{Γ_2} are then:

$$\begin{aligned} \varphi_{\Gamma_1} &= \arctan\left(\frac{\Delta X_N}{R_N - R_a}\right) - \arctan\left(\frac{\Delta X_N}{2R_N}\right) \\ \varphi_{\Gamma_2} &= \arctan\left(\frac{-\Delta X_N}{R_N - R_a}\right) - \arctan\left(\frac{-\Delta X_N}{2R_N}\right) \end{aligned} . \tag{4.29}$$

The sum of the phases φ_{Γ_1} and φ_{Γ_2} is obviously zero and the assumption of a non-zero ΔX_N leads therefore to

$$\varphi_{\Gamma_1} \neq \varphi_{\Gamma_2} . \tag{4.30}$$

The expressions (4.28) and (4.30) fulfill the targeted condition in (4.26) and thus, confirm that a phase modulation is realizable by switching the circuit input impedance as proposed above.
To improve the robustness of digital phase modulations, the phase difference between the symbols should be as high as possible [40]. In the case of two impedance states, the highest possible phase difference is

$$\Delta\varphi_{\Gamma_{max}} = 180°. \tag{4.31}$$

To achieve the state difference defined in (4.31), equation (4.18) is first transformed into

$$\varphi_\Gamma = \arctan\left(\frac{\frac{\Delta X_N}{R_N}}{1-\frac{R_a}{R_N}}\right) - \arctan\left(\frac{\frac{\Delta X_N}{R_N}}{1+\frac{R_a}{R_N}}\right). \tag{4.32}$$

Considering (4.27), the reflection coefficient phase is given as

$$\begin{aligned} \varphi_\Gamma &= -90° - \arctan\left(\frac{1}{2}\frac{\Delta X_N}{R_N}\right) \quad \text{for} \quad \frac{\Delta X_N}{R_N} < 0 \\ \varphi_\Gamma &= +90° - \arctan\left(\frac{1}{2}\frac{\Delta X_N}{R_N}\right) \quad \text{for} \quad \frac{\Delta X_N}{R_N} > 0 \end{aligned}, \tag{4.33}$$

and is depicted in Figure 4.7.

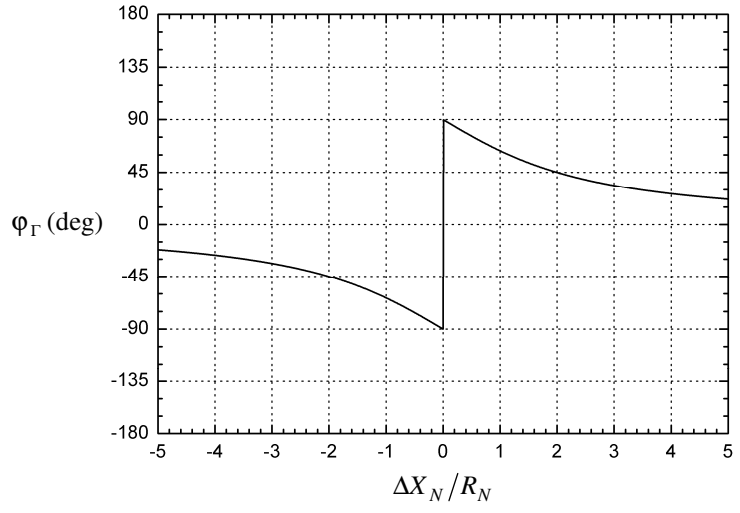


Figure 4.7: Reflection coefficient phase as function of $\Delta X_N / R_N$.

Hence, switching the circuit input impedance between two values $Z_{N,1}$ and $Z_{N,2}$ such

that $\Delta X_N / R_N \to -0$ and $\Delta X_N / R_N \to +0$, respectively, leads to a phase difference $\Delta\varphi_\Gamma = \varphi_{\Gamma_1} - \varphi_{\Gamma_2}$ of 180°, since the reflection coefficient phase is switched between -90° and +90°. Since it has been set above that $\Delta X_N \neq 0$, the required phase shift is fulfilled if and only if

$$R_N \to \infty . \tag{4.34}$$

That is, the circuit input resistance and consequently the real part of the antenna impedance should be as high as possible, enabling a binary phase shift keying (BPSK).

4.3 BACKSCATTER IMPLEMENTATION

As introduced in Subsection 4.2.1, passive transponders perform backscatter modulation by detuning the impedance at the antenna termination electronically. A circuit enabling this task is depicted in Figure 4.8.

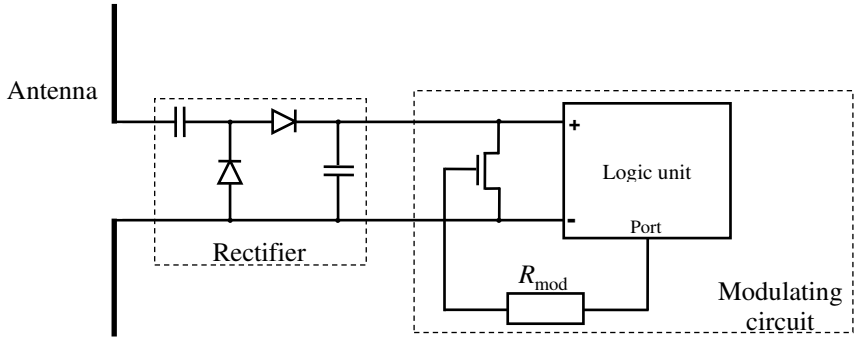


Figure 4.8: Block diagram of a passive transponder.

In Figure 4.8, a field-effect transistor (FET) is located between the rectifier and the logic unit. An output port of the logic unit is connected to the field effect transistor gate over a path, represented here by a resistance R_{mod}, controlling the drain-source resistance. On one hand, a bipolar junction transistor (BJT) may be used as well instead of a field effect transistor, providing certain advantages: the most commercial available discrete FETs require a minimum supply voltage and a gate voltage of several volts, which cannot always be ensured due to the low received power. But on the other hand, a FET can be powerless switched, while the bias network of a BJT cause inevitably power losses.

According to the bit sequence to be sent, the logic unit can change the load resistance at the rectifier output between two (or more) states and thus, in a certain manner the reflection coefficient. The analysis of this tuning effect is the object of the next subsections.

Under the assumptions made in Chapter 2, the rectifier output voltage and current are time constant values. Hence, only the effective shunt resistance at the rectifier output would influence the rectifier input impedance and thus, the input reflection coefficient. The system of equations (3.32) shows that the load resistance R has an impact on all system performances and thus, on the rectifier input resistance and reactance. However the complexity of (3.32) does not permit a compact analytical expression of the input reflection coefficient as function of the load resistance.

For analysis, a voltage doubler has been loaded with the resistance $R = R_{opt} = 5\ \text{k}\Omega$, and the antenna impedance has been set to match the rectifier input, whose resistance and reactance is $R_{N,opt}$ and $X_{N,opt}$, respectively. The load resistance R has been swept from 1 kΩ to 10 kΩ, and the resulting input resistance R_N and reactance X_N have been observed. Figure 4.9 (a) and Figure 4.9 (b) show the variation of $R_N / R_{N,opt}$ and $X_N / X_{N,opt}$ against R. In the almost total sweep range, the input resistance decreases as the load resistance increases. In contrast, the absolute value of the input reactance increases. In Figure 4.9 (c), the corresponding input reflection coefficient is plotted in a Smith chart, where the reference impedance Z_{ref} is the antenna impedance, that is: $Z_{ref} = R_{N,opt} - jX_{N,opt}$. It can be seen that the reflection coefficient magnitude and phase are affected by the load resistance.
Hence, unlike the assumptions made in Subsection 4.2.2 and Subsection 4.2.3 for the realization of amplitude and phase modulation, neither the resistance nor the reactance of the circuit input remains constant while the load resistance is varied. Nonetheless, the realization of amplitude or phase modulation is possible and can be discussed by means of Figure 4.10, where the magnitude and phase of the resulting input reflection coefficient have been depicted. The similarities between Figure 4.5 and Figure 4.10 (a) proceed from the fact that impedance match is achieved at one value in the sweep range.

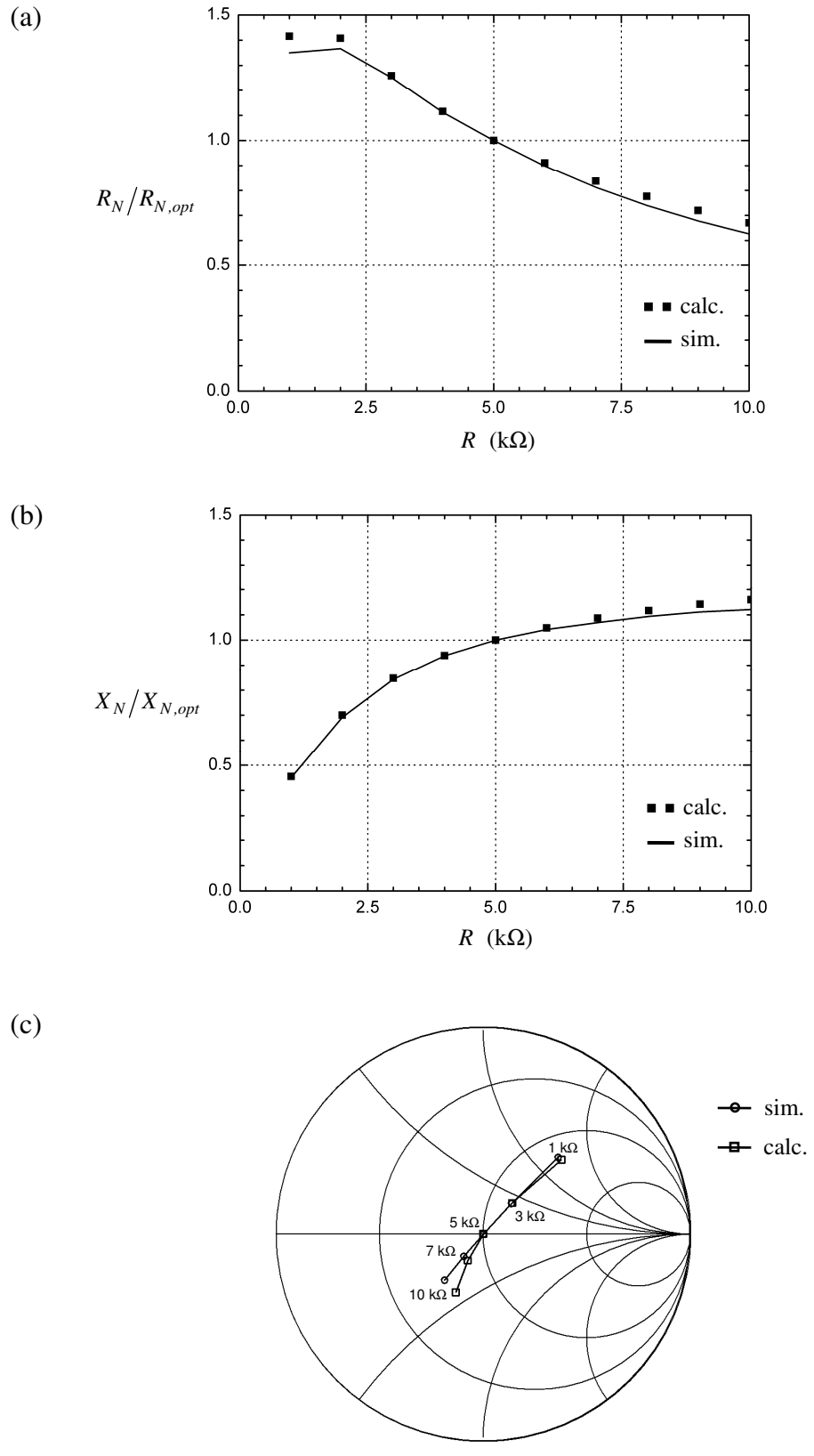


Figure 4.9: Relative variation of (a) the input resistance and (b) the reactance of a voltage doubler including the diode BAT15-03W; (c) Smith chart plot of Γ. f = 1 GHz; P_a = 0 dBm.

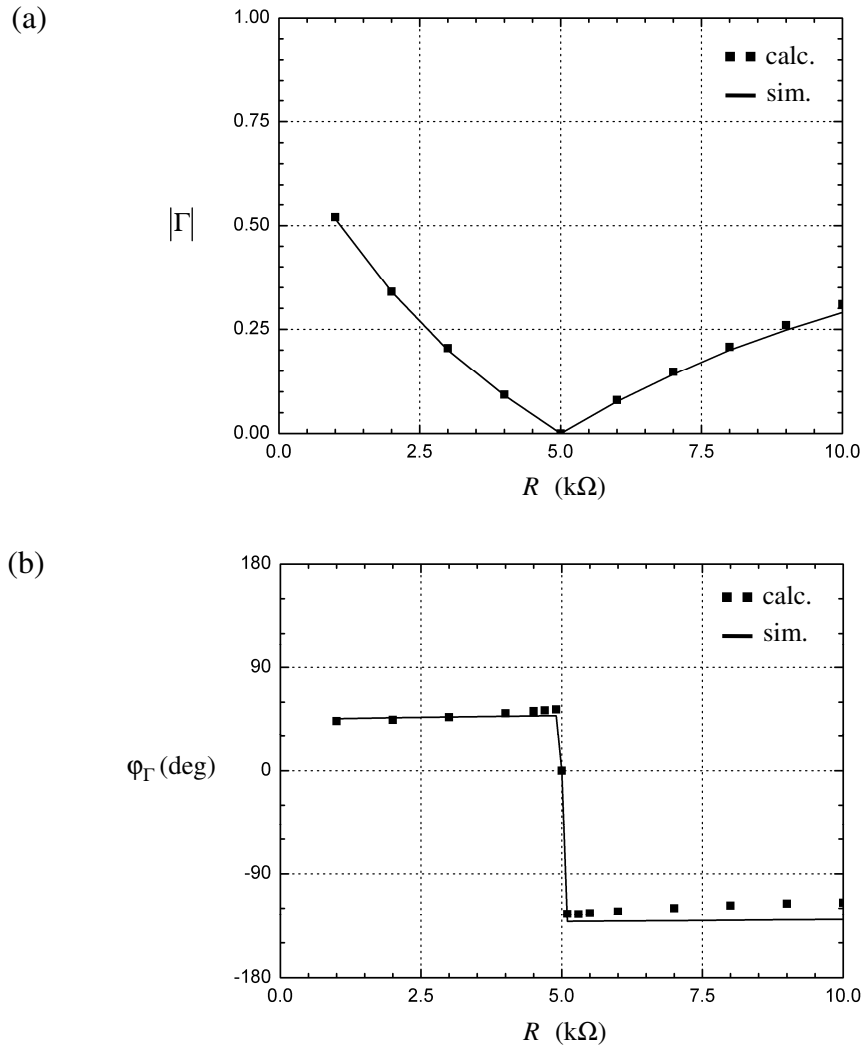


Figure 4.10: Influence of the load resistance on (a) the magnitude and (b) phase of the reflection coefficient.

4.3.1 AMPLITUDE MODULATION

As Figure 4.10 (a) shows, for $R \leq R_{opt}$, the magnitude of the input reflection coefficient decreases as the load resistance increases, while the phase remains almost constant. Similarly, for $R \geq R_{opt}$, the magnitude of the input reflection coefficient increases with the load resistance while the phase remains almost constant. One can say in a general manner that sweeping the load resistance either in the interval [0, R_{opt}] or in the interval [R_{opt}, ∞[will allow an ASK modulation, as argued in Subsection 4.2.2. The number of transmitted bits per symbol depends on the number of values the load resistance R takes inside the chosen interval, while the modulation depth depends on how close these values are to each other.
Without loss of generality, a 2-ASK modulation is now assumed: the load resistance R is switched between two values R_1 or R_2. Γ_1 and Γ_2 are the resulting input reflection

coefficients for $R = R_1$ and $R = R_2$, respectively. The OOK modulation is achieved if either R_1 or R_2 is equal to R_{opt}. Due to the technically limited sensibility of the interrogator receiver, a minimum modulation depth and consequently a minimum difference $\Delta|\Gamma|_{\min} = \big||\Gamma_1| - |\Gamma_2|\big|$ and thus, a minimum difference $|\Delta R|_{\min} = |R_1 - R_2|$ is required.

Looking carefully at Figure 4.10 (a), one sees that in the interval [R_{opt}, 10 kΩ], the curve is flatter than in the interval [1 kΩ, R_{opt}]. Hence, tuning of the load resistance in latter interval leads to higher modulation depth than in the interval [R_{opt}, 10 kΩ], permitting a higher SNR and thus, enhancing the maximum communication range between the interrogator and the transponder.

Furthermore, the logic unit requires a minimum supply voltage to operate. However, as shown in Figure 4.11, switching the load resistance from R_{opt} to a lower value decreases the instantaneous DC supply voltage, reducing the maximum power supply range of the transponder, as discussed in Paragraph 4.1.2.5. In the contrary, switching R to a higher value than R_{opt} will increase the supply voltage. Therefore, a trade-off is necessary by the choice of the load resistance sweep range.

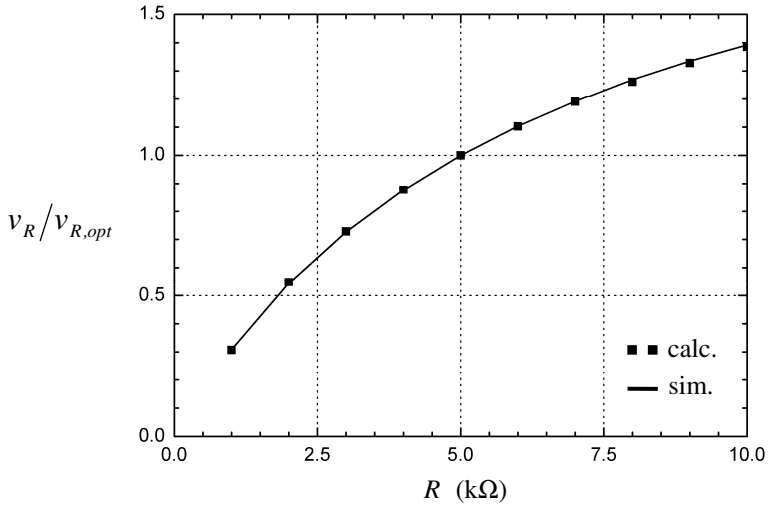


Figure 4.11: Relative variation of v_R, whereby $v_{R,opt}$ is the DC output voltage for $R = R_{opt}$.

4.3.2 PHASE MODULATION

In Figure 4.10 (b), the curve has a leap of almost ±180° when the load resistance R is switched from a value R_1 lower than R_{opt} to a value R_2 higher than that. Hence, according to Subsection 4.2.3, a BPSK is achievable in this case, if the magnitude of the corresponding input reflection coefficient is the same for $R = R_1$ and $R = R_2$. This method offers a larger sweep range than the procedure presented in Subsection 4.2.3, where a reflection coefficient phase shift of ±180° is only possible for an infinitesimal

sweep range around the point $R = R_{opt}$.

Choosing R_1 and R_2 as close as possible to R_{opt} provides the advantage, that the DC supply voltage remains almost constant by $v_{R,opt}$. However, the corresponding reflection coefficient magnitude and thus the power of the reflected signal would tend to zero, reducing drastically the communication range because of the aforementioned technically limited interrogator sensitivity. Hence, even here, a minimal difference $|\Delta R|_{\min}$ is required, so that $|R_1 - R_{\text{opt}}| \geq |\Delta R|_{\min}$ and $|R_{\text{opt}} - R_2| \geq |\Delta R|_{\min}$. Additionally, it should be ensured that for $R = R_1$, the DC supply voltage of the logic unit remains higher than the minimum required value.

4.4 SENSITIVITY ANALYSES

4.4.1 INFLUENCE OF THE AVAILABLE POWER

The argumentation and curves in Subsection 4.3.1 and Subsection 4.3.2 are valid for a transponder at a specific available power. In most applications however, transponders or interrogators are mobile, making the expected available power at the transponder antenna and consequently the rectifier performances dependent on the vicinity, the distance as well as the alignment of transponder and interrogator antennas to each other. Therefore, it is necessary to analyze the effects of power variations on the implemented ASK and BPSK modulations [46].

For this purpose, the voltage doubler from Section 4.3 is still considered: in the default configuration, the antenna impedance matches the circuit input for a load resistance $R = R_{opt} = 5\ \text{k}\Omega$ and for the nominal available power $P_a = 0$ dBm. For analyses, the available power P_a has been turned to -1 dBm, 0 dBm and 1 dBm while in each case, the load resistance has been swept from 1 kΩ to 10 kΩ. The resulting magnitude and phase of the input reflection coefficient are shown in Figure 4.12 (a) and Figure 4.12 (b), respectively.

It is notable that the resulting curves of $|\Gamma|$ and φ_Γ do not drift along the horizontal axis. The magnitude of Γ is affected slightly and does not have a zero for $P_a \neq 0$ dBm, disabling the realization of OOK modulation. Furthermore, the leap in the phase φ_Γ is rounded off, and depending on whether the available power is higher or lower than the nominal value 0 dBm, the phase φ_Γ decreases or increases while switching R from lower to higher values than R_{opt}. Hence, to achieve an 2-ASK modulation, either $R_1 < R_2 < R_{\text{opt}}$ or $R_{\text{opt}} < R_1 < R_2$ is required with the additional condition, that both R_1 and R_2 should be far enough from R_{opt} to provide quite identical phase of Γ. As well, a BPSK implementation with ± 180° phase shift is realizable if $R_1 < R_{\text{opt}} < R_2$ with the additional conditions that both values R_1 and R_2 are also chosen far enough from R_{opt}, and that the resulting reflection coefficient magnitudes are equal.

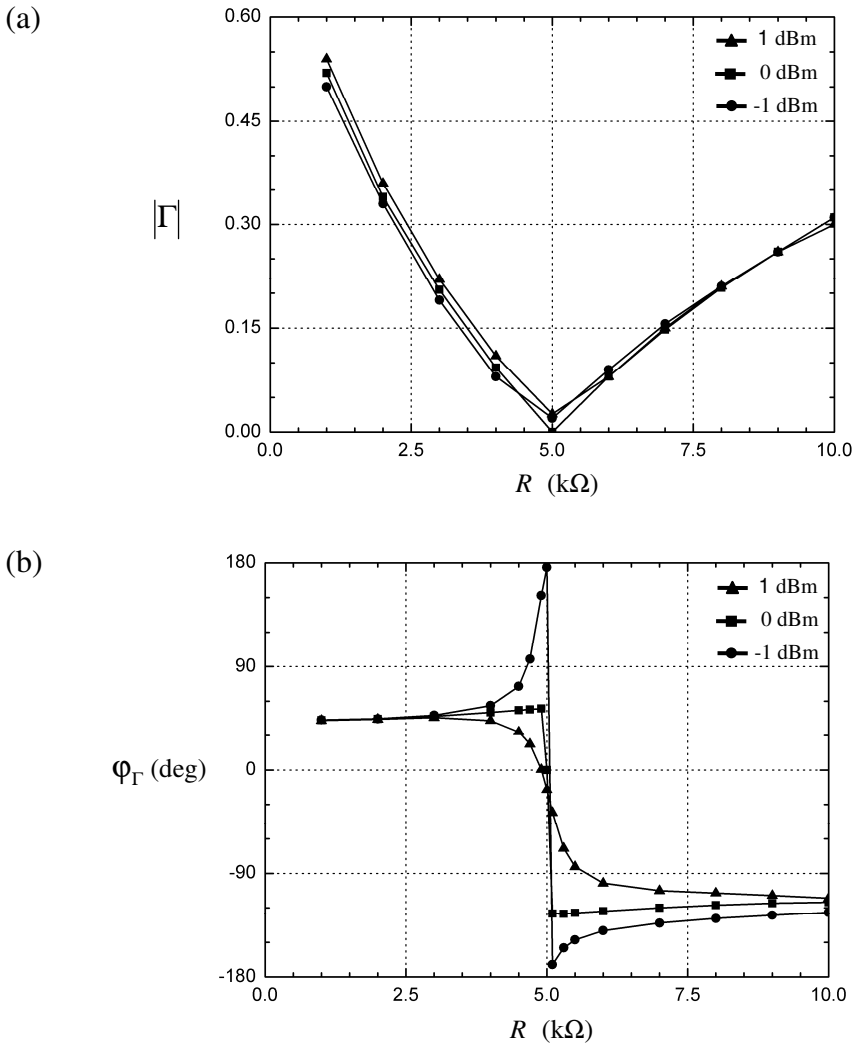


Figure 4.12: Influence of the available power on (a) the magnitude and (b) phase of the input reflection coefficient.

4.4.2 INFLUENCE OF THE ANTENNA IMPEDANCE

Fabrication methods and technological process tolerances affect the geometry and consequently the impedance of the transponder antenna, so that it may differ more or less from the targeted value. In Figure 3.16, it is shown that the antenna impedance affects the rectifier input impedance. Furthermore, as expressed in (4.16) and also discussed in Section 4.3, the reflection coefficient Γ and thus, the working of the implemented modulation processes depends on the antenna impedance. Therefore, the alteration of ASK and BPSK modulations due to tolerances of the antenna impedance should be analyzed.

For this purpose, the voltage doubler from Section 4.3 is still considered: in the default configuration, the antenna impedance $Z_a = R_a + jX_a$ matches the circuit input for the load impedance $R = R_{opt} = 5\,\text{k}\Omega$ and for the available power $P_a = 0\,\text{dBm}$. For analyses, the antenna resistance has been varied by ± 20% while the reactance has been

kept constant, and vice versa. In each case, the load resistance has been swept from 1 kΩ to 10 kΩ. The magnitude and phase of the resulting reflection coefficients are shown in Figure 4.13 (a) and Figure 4.13 (b), respectively.

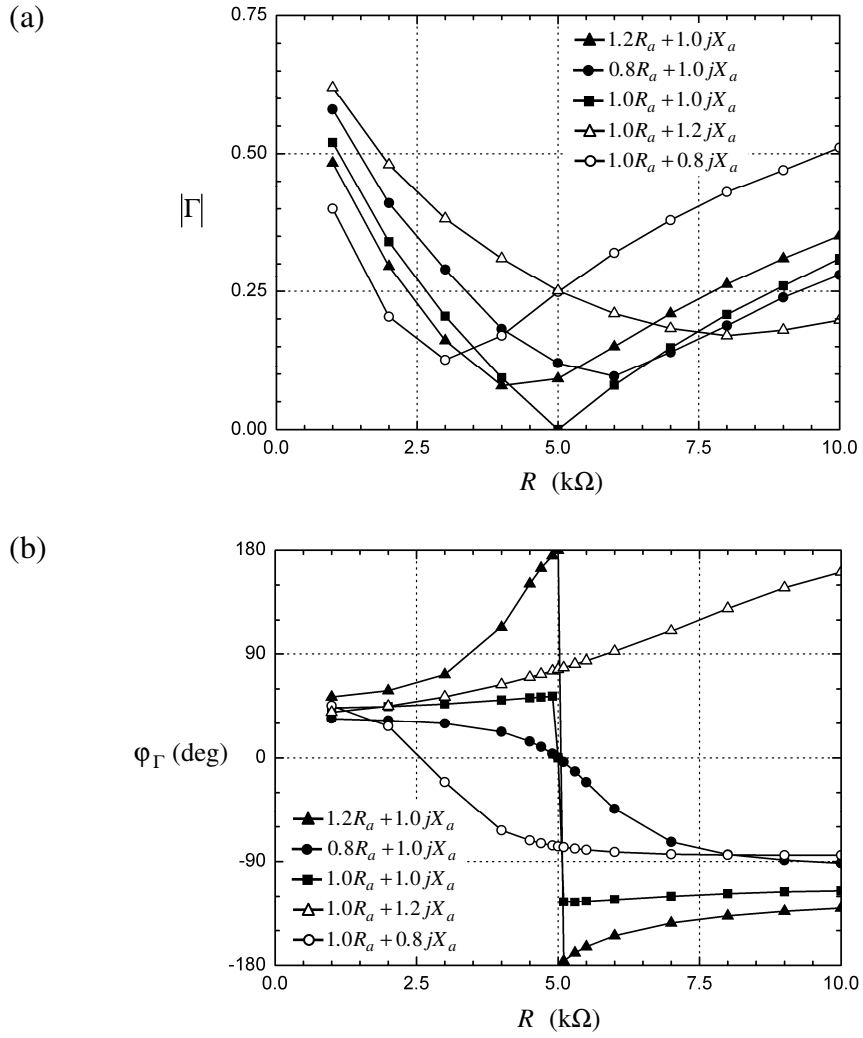


Figure 4.13: Influence of the available power on (a) the magnitude and (b) phase of the input reflection coefficient.

The tolerances of the antenna impedance eliminate the zero of $|\Gamma|$, disabling the implementation of an OOK. Furthermore, the curves of $|\Gamma|$ and φ_Γ are shifted along the horizontal axis: the minimum of $|\Gamma|$ is no longer reached for $R = R_{opt}$, but for a new value $R = R'_{opt}$. The resulting alteration of the amplitude modulation can be illustrated by means of two particular scenarios.

In the first one, it is assumed that the transponder is designed to perform a 2-ASK by switching the resistance R between 4.5 kΩ and 1.5 kΩ. This will switch the magnitude $|\Gamma|$ between 0.05 and 0.44 if the antenna impedance has the nominal value $R_a + jX_a$.

However, the magnitude $|\Gamma|$ will not be switched and will remain constant at the value 0.22 if the antenna impedance has the value $R_a + j0.8X_a$ instead of the nominal value.

In the second scenario, it is assumed that the transponder is designed to perform an 2-ASK by switching the resistance R between 5.5 kΩ and 8 kΩ. This will switch the magnitude $|\Gamma|$ between 0.05 and 0.21 if the antenna impedance has the nominal value $R_a + jX_a$. However, the magnitude $|\Gamma|$ will be switched between 0.23 and 0.17 if the antenna impedance has the value $R_a + j1.2X_a$ instead of the nominal value. Though an amplitude modulation is achieved, it would lead to the inversion of the sent bits after demodulation at the interrogator since a high power will be detected although a low magnitude $|\Gamma|$ was targeted, and vice versa. In such cases, the realization of an 2-ASK modulation requires the definition of new tuning intervals for the load resistance R.

Furthermore, the leap in the curve of φ_Γ is rounded off. Thus, switching the load resistance between two values R_1 and R_2, where $R_1 < R'_{opt} < R_2$ will shift the phase, and consequently it will permit the implementation of phase modulation, if additionally the corresponding reflection coefficient magnitudes are identical. However, a phase shift of ± 180° and consequently the realization of a BPSK modulation is not possible, even if both values R_1 and R_2 are chosen far from R'_{opt}.

4.5 CONCLUSION

In addition to the regulation constraints which limit the maximal radiated power, many other parameters related to the communication arrangement and system inherent specifications such as the vicinity of the interrogator and transponder antennas, their polarization, their distance and alignment to each other, impedance mismatch at the antennas, the minimum required SNR at the interrogator receiver, and the minimum required DC voltage at the transponder logic unit influence significantly the achievable range of the forward and reverse links.
Tuning the rectifier load resistance tunes the circuit input reflection coefficient, enabling amplitude or phase modulation of the backscattered signal. Especially the proposed realization method of the phase modulation provides new possibilities for transponder designers, since until now, few solutions have been presented in the literature [11]. The quality of the modulation processes is sensitive to variations of the available power and inaccuracies of the antenna impedance.

5 INTEGRATION IN METALLIC OBJECTS

Chapter 1 introduced the integration of passive transponders in metallic environments. The transponder block diagram depicted in Figure 4.8 includes mainly an antenna, a rectifier and a modulator. Chapter 2 and Chapter 3 presented the design of the transponder rectifier and its analysis. Chapter 4 examined the realization of backscatter modulator based on the controlled impedance mismatch between the rectifier input and the antenna. As last step of the transponder development, the design of antennas for the integration in metallic objects will be treated in this chapter.

For remote identification and sensing, tags are usually mounted on or near the object surface [5]. The use of this method to monitor metallic work pieces in factories or outdoor can lead to the following problem: mechanical chocks due to eventual rough handling of objects may destroy the transponder. An approach for solving this problem consists of integrating the transponder into the metallic objects. This perspective is particularly attractive since it offers the additional possibility to register and transmit object inherent physical data such as the internal temperature. However, a major difficulty arises because metallic surfaces reflect electromagnetic waves, which makes the integration of field-powered systems into metallic objects a challenging task [60].

5.1 TRANSMISSION LINES

The integration concept is depicted in Figure 5.1: a cavity is made from the object surface to the inside, wherein the transponder is placed. A transmission line connects the surface and the transponder. The transponder circuit requires a coupling structure that acts as antenna to receive and reflect the incoming waves. Coaxial cables, waveguides and fin-lines have been considered as possible transmission lines, as displayed in Figure 5.2.

Coaxial cables offer the advantage, that their outer diameter and thus the required cavity width are adjustable at will. If one assumes that the transponder circuit is realized on a substrate, then at one end of the cable, a coaxial-to-planar transition should be provided to contact the circuit. The disadvantage of this solution is that an antenna should be connected to the upper end of the cable to receive and transmit electromagnetic waves. This solution would drastically disturb the surface evenness of the object, making the

system fragile. This will work against the above mentioned robustness requirement. Even the antenna proposed in [53, 54] for UHF transponders is not suitable for mobile pieces since the junction between the radiating surface of the antenna and the feeding coaxial cable is mechanically fragile.

Waveguides provide the major advantages that they coincide with the cavity, since the work piece is metallic, and waveguides operate as good aperture radiators: an additional antenna at the object surface is not needed. The main inconvenient is that the minimum size of the cross section is function of the operating frequency. Furthermore, a waveguide-to-planar transition should be designed to connect the transponder circuit. Nonetheless, the required mechanical immunity of the circuit is achievable using waveguides as transmission lines.

For the sake of completeness, fin-lines should also be mentioned as possible transmission lines. They should be realized on a substrate and placed parallel to the cavity axis. On one hand, this solution offers the advantage that the transponder circuit could be directly mounted on the fin-line substrate. On the other hand, the minimum required size of the cross section width remains dependent on signal frequency. Furthermore, the fin-line width should progress slowly and gradually from the top of the cavity to the circuit in order to avoid wave reflection due to sudden geometrical size change. This requirement may lead to long fin-lines.

I have selected the waveguide as transmission line.

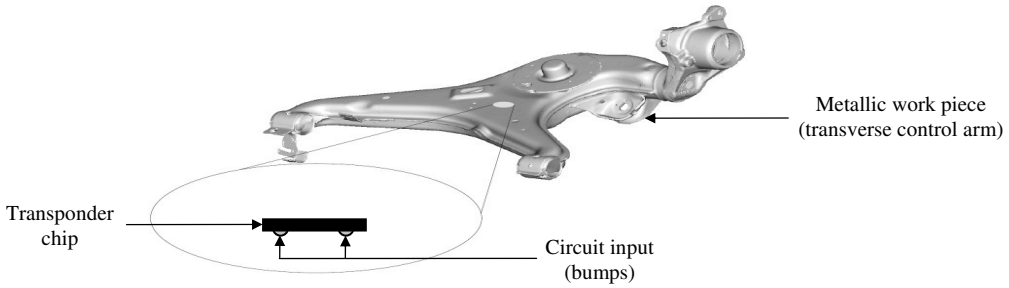


Figure 5.1: Vision of an integrated communication chip in a metallic object.

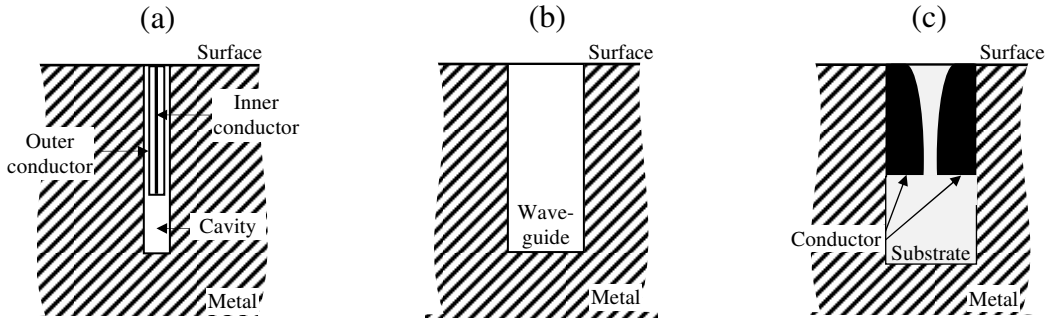


Figure 5.2: (a) Coaxial cable; (b) waveguide; (c) fin-line.

The next sections treat of the design of the waveguide. In addition, a concept for the realization of an adequate waveguide-to-planar transition, and finally the characterization of the resulting transponder antenna will be presented and discussed.

5.2 BASICS ON WAVEGUIDES FIELD THEORY

The cavity where the transponder will dwell can basically be realized as rectangular or circular waveguide, whereby the cross section of the rectangular waveguide is defined by the length a and the width b (with $a > b$), while the diameter D defines the cross section of the circular waveguide, as displayed is Figure 5.3.

Figure 5.3: Cross section geometry of (a) rectangular and (b) circular waveguide.

An electromagnetic wave can propagate in the cavity if and only if the frequency is higher than the cavity cut-off frequency f_c, which is defined as

$$f_c = \frac{c}{2a\sqrt{\varepsilon_r \mu_r}} \tag{5.1}$$

for rectangular waveguides. For circular waveguides, it is defined as

$$f_c = \frac{c \cdot t_{11}}{\pi D\sqrt{\varepsilon_r \mu_r}}, \tag{5.2}$$

where $t_{11} \approx 1.841$, c is the speed of light in vacuum, and ε_r and μ_r are the relative permittivity and permeability of the waveguide filler material, respectively [9, 34, 61]. In other words, a electromagnetic wave with the frequency f can propagate in a rectangular waveguide if and only if the length a is higher than the minimum value a_{min}, where

$$a_{min} = \frac{c}{2f\sqrt{\varepsilon_r \mu_r}}. \tag{5.3}$$

Similarly, the minimum required diameter D_{min} for circular waveguides is

$$D_{min} = \frac{c \cdot t_{11}}{\pi f\sqrt{\varepsilon_r \mu_r}}. \tag{5.4}$$

Hence, the lower the signal frequency f, the bigger the required waveguide cross section. However, (5.3) and (5.4) show that the minimum required cross section size can be reduced by choosing a filler material with a high relative permittivity or permeability. Figure 5.4 depicts a_{min} and D_{min} as a function of the frequency for different values of ε_r under the assumption: $\mu_r = 1$.

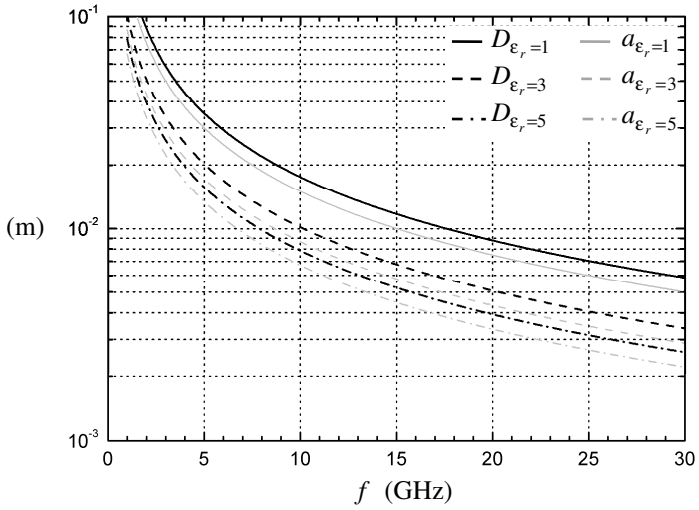


Figure 5.4: Minimum required length and diameter for with different relative permittivity.

The minimum length a_{min} and diameter D_{min} do not differ highly from each other, so the investigations will be focused on the circular waveguides because of their comfortable realization in metallic objects.

5.3 ONE SIDE SHORT-CIRCUITED WAVEGUIDE

The upper end of the cavity is open at the object surface, while the bottom is a metallic termination. Thus, the cavity can be considered as a one side short-circuited circular waveguide. The field distribution inside the cavity is investigated in the case where an incoming wave, whose frequency is higher than the cut-off frequency, falls on the

waveguide aperture. Here, one makes the additional restriction that the waveguide should be excited in its unambiguous frequency range. It means that only the transversal electric mode TE_{11} takes place. Hence, the frequency f should be higher than the TE_{11} cut-off frequency and lower than the cut-off frequency of the next higher mode, the transversal magnetic mode TM_{01}:

$$\frac{c \cdot t_{11}}{\pi D \sqrt{\varepsilon_r \mu_r}} \leq f < \frac{c \cdot s_{01}}{\pi D \sqrt{\varepsilon_r \mu_r}}, \tag{5.5}$$

where $s_{01} \approx 2.405$ [61].

The electric and magnetic field distribution in the one side short-circuited waveguide has been simulated in consideration of (5.5) using the 3D field simulation software HFSS 11 from Ansoft. Figure 5.5 depicts field plots in longitudinal and transversal cuts at a specific moment.

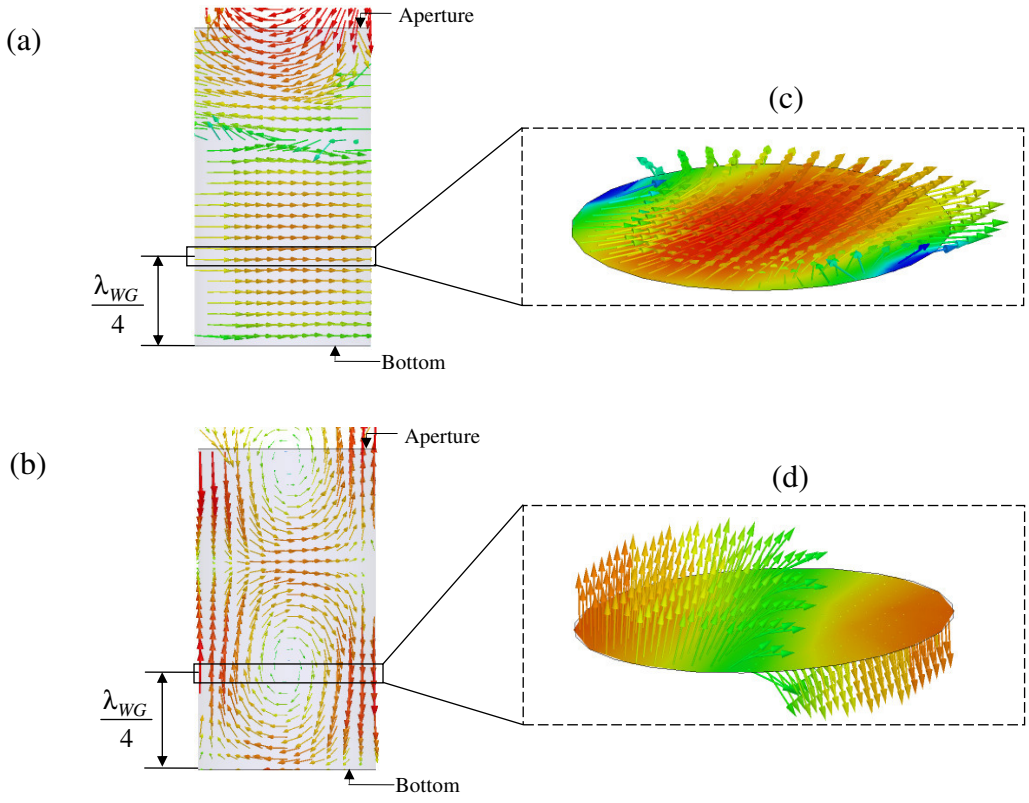


Figure 5.5: (a) Electric and (b) magnetic field in a longitudinal cut; (c) electric and (d) magnetic field in the transversal cut at the distance $\lambda_{WG}/4$ from the metallic bottom.

Figure 5.5 shows that the electric field is maximum in the middle of the cross section at a quarter waveguide wavelength distance from the metallic bottom. The waveguide wavelength can be calculated as follows [61]:

$$\lambda_{WG} = \frac{1}{\sqrt{\frac{\varepsilon_r \mu_r}{\lambda_0^2} - \left(\frac{t_{11}}{\pi D}\right)^2}}, \tag{5.6}$$

where λ_0 is the free-space wavelength, defined as

$$\lambda_0 = \frac{c}{f}. \tag{5.7}$$

Similarly, the magnetic field at the waveguide walls is maximum at the distance $\lambda_{WG}/4$ from the bottom.
Thus, the realization of a coupling structure to connect the transponder circuit to the waveguide seems to be possible by locating the planar coupling structure in the transversal plane at the distance $\lambda_{WG}/4$ from the bottom.

5.4 WAVEGUIDE ANTENNA

The transponder circuit requires a voltage and a current at its input to operate. It means that a transversal electromagnetic field distribution, also called TEM mode, should take place at its input, as depicted in Figure 5.6. Therefore, a waveguide-to-planar transition should be designed to convert the TE_{11} mode in the cavity to a TEM mode at the circuit input.

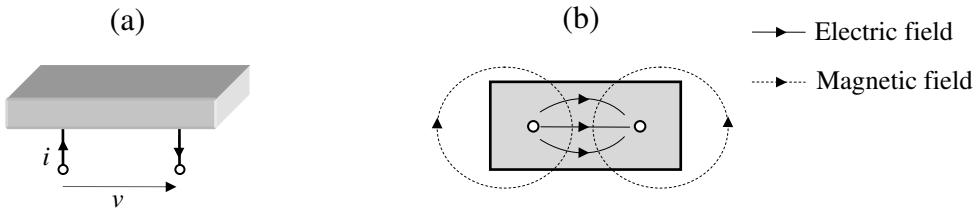


Figure 5.6: (a) Voltage and current, and (b) corresponding electric and magnetic field at the input of the transponder circuit.

5.4.1 WAVEGUIDE-TO-PLANAR TRANSITION

The planar structure depicted in Figure 5.7 has been developed. The transition consists of a single-layer circular substrate, whose diameter coincides with the waveguide diameter. The conductor layer is made of two arms, which are point symmetric about the centre of the circular substrate. The input pins of the transponder circuit should be connected to the transition contacts located in the middle of the structure, as shown in Figure 5.8.

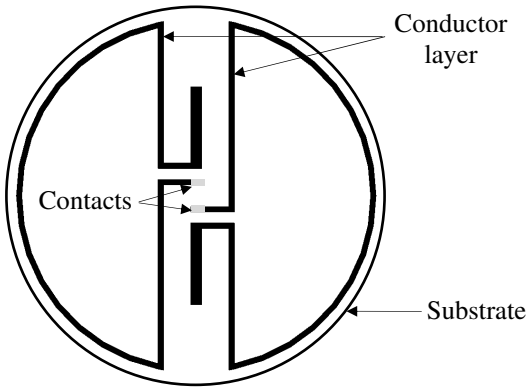


Figure 5.7: Waveguide-to-planar transition.

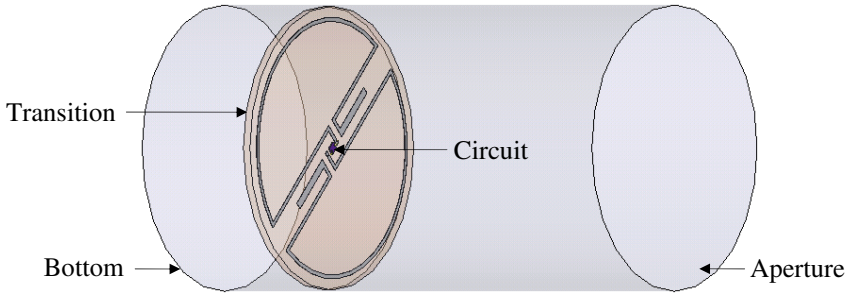


Figure 5.8: Planar transition as coupling structure between the transponder circuit and the waveguide.

5.4.2 IMPEDANCE MEASUREMENT

The waveguide in combination with the waveguide-to-planar transition works as antenna for the transponder circuit. Since the operability of the transponder depends highly on the antenna impedance, it is necessary to develop a method to measure the antenna impedance provided at the transition contacts.

The measurement setup used to determine the antenna input impedance includes a two-port vector network analyzer (VNA) and two coaxial cables, whose inner conductors have been extended to connect the contacts of the waveguide-to-planar transition, as depicted in Figure 5.9 [19]. It has been reported in [26] that the perturbation of the waveguide field distribution due to the presence of the coaxial cables is not significant. Consequently, the simulated and measured values of the antenna impedance are expected to correspond to each other.

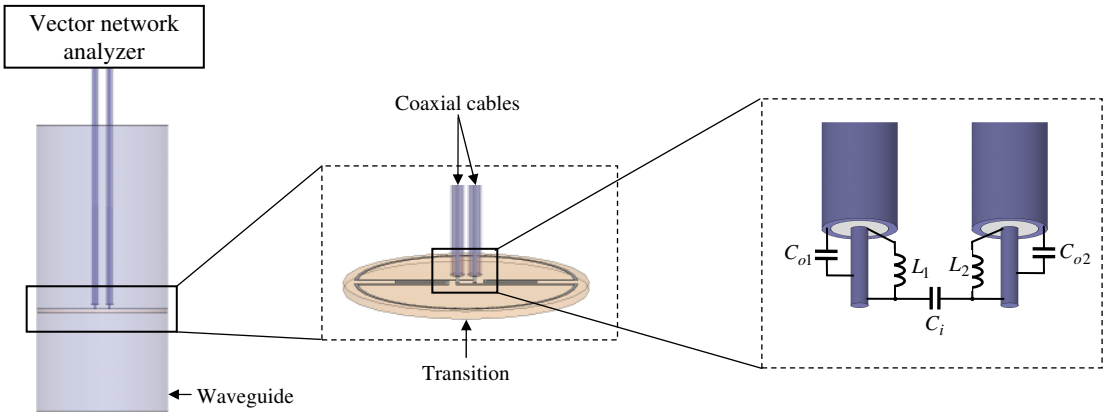


Figure 5.9: Parasitic effects by measuring the antenna impedance.

The junction between the coaxial cables and the waveguide-to-planar transition is not ideal due to the extension of the cables inner conductors. To take the resulting parasitic effects into account, an equivalent circuit has been developed, as shown in Figure 5.10.

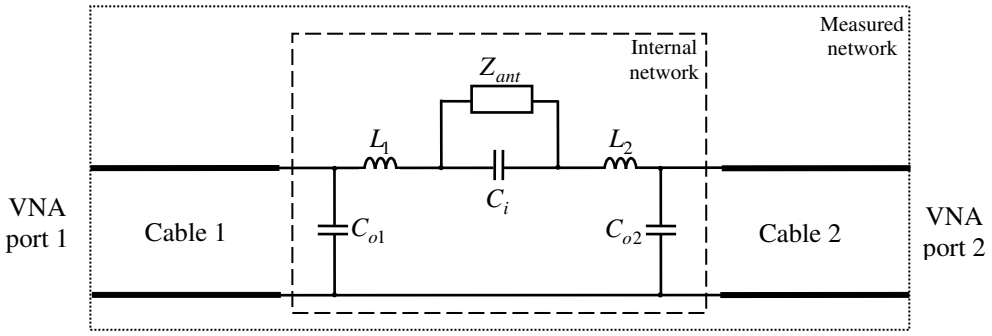


Figure 5.10: Equivalent block diagram of the measurement setup.

In this model, it is assumed that the main parasitic effects are the capacitance C_i between the inner conductor and outer conductor of each cable, the capacitances C_{o1} and C_{o2} between both inner conductors of both cables, and the inductances L_1 and L_2 resulting from the extension of each inner conductor. The antenna impedance Z_{ant} is connected in parallel with the parasitic capacitance C_i [4, 26]. To simplify matters, the measurement setup is assumed to be symmetric: $C_{o1} = C_{o2} = C_o$, $L_1 = L_2 = L$, and both coaxial cables have the same length l and propagation coefficient γ.
Due to the assumed identical coaxial cables, the S-matrix $[S]$ of the internal network is

$$[S] = [S_m] \cdot e^{2\gamma l} \Leftrightarrow \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} S_{m,11} & S_{m,12} \\ S_{m,21} & S_{m,22} \end{bmatrix} \cdot e^{2\gamma l}, \tag{5.8}$$

where $[S_m]$ is the measured S-matrix, as depicted in Figure 5.10. On one hand, the differential impedance Z_d of the internal network can be obtained from $[S]$ as

$$Z_d = 2Z_0 \frac{e^{-2\gamma l} + S_{m,11} - S_{m,12}}{e^{-2\gamma l} - S_{m,11} + S_{m,12}}, \tag{5.9}$$

where the reference impedance Z_0 is usually 50 Ω [23, 41]. On the other hand, the differential impedance Z_d can be deduced from Figure 5.10 as

$$Z_d = \frac{1}{j\omega_0 \frac{C_o}{2} + \frac{1}{2j\omega_0 L + \frac{1}{\frac{1}{Z_{ant}} + j\omega_0 C_i}}}. \tag{5.10}$$

Inserting (5.9) in (5.10) permits the calculation of the antenna impedance Z_{ant} as

$$Z_{ant} = \frac{N_{ant}}{D_{ant}}, \tag{5.11}$$

where the numerator N_{ant} is

$$N_{ant} = 2Z_0\left(e^{-2\gamma l} + S_{m,11} - S_{m,12}\right)\left(1 - \omega_0^2 LC_o\right) - 2j\omega_0 L\left(e^{-2\gamma l} - S_{m,11} + S_{m,12}\right), \tag{5.12}$$

and the denominator D_{ant} is

$$\begin{aligned} D_{ant} = &-j\omega_0 Z_0\left(e^{-2\gamma l} + S_{m,11} - S_{m,12}\right)\left(C_o + 2C_i\left(1 - \omega_0^2 LC_o\right)\right) \\ &+ \left(e^{-2\gamma l} - S_{m,11} + S_{m,12}\right)\left(1 - 2\omega_0^2 LC_i\right) \end{aligned}. \tag{5.13}$$

The semi-rigid cables EZ86 with the following data have been used:
Inner conductor diameter: 0.51 mm
Dielectric diameter: 1.68 mm
Outer conductor diameter: 2.20 mm
Dielectric constant: 2.08
The extension of the inner conductors has been limited at 2 mm. 3D field simulations have shown that $C_i \leq 0.01$ pF, and $C_o \approx 0.075$ pF.
Simulations give the following approximation for the parasitic inductance L:

$$L \approx \frac{1nH}{mm}\Delta l, \tag{5.14}$$

where Δl is the extension length of the inner conductor in millimeters [27].

5.4.3 THE 50 OHM WAVEGUIDE ANTENNA

A waveguide-to-planar transition has been designed to realize a cylindrical waveguide antenna with an impedance of 50 Ω in the 2.45 GHz ISM band. An air filled brass tube with a diameter of 85 mm and a length of 170 mm has been considered as the waveguide. The distance between the transition and the cavity bottom has been fixed to the quarter waveguide wavelength at 2.4 GHz, which is about 62 mm. This distance has been kept in the following way: a polystyrene piece with the length 62 mm has been placed between the waveguide bottom and the substrate, and another one has been inserted between the substrate and the waveguide aperture. Polystyrene has been chosen because it behaves almost as the air in the 2.45 GHz ISM band and thus, does not disturb the field distribution. The used substrate is a 1 mm thick FR4 sheet with a single 35 µm thick copper layer.
The geometrical parameters of the transition depicted in Figure 5.11 have been tuned using the simulation software HFSS to obtain the targeted antenna impedance of 50 Ω.

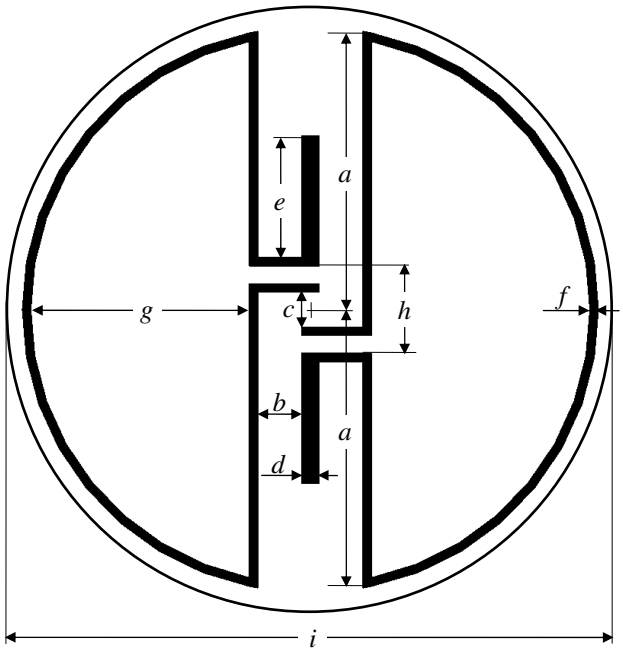


Figure 5.11: Geometry parameters of a waveguide-to-planar transition.

The resulting geometrical parameters are:
$a = 32.5\,\text{mm}$
$b = 3.9\,\text{mm}$
$c = 2\,\text{mm}$
$d = 3\,\text{mm}$
$e = 20.6\,\text{mm}$
$f = 1\,\text{mm}$
$g = 35.8\,\text{mm}$

$h = 8\,\text{mm}$
$i = 85\,\text{mm}$

Figure 5.12 depicts the simulated and measured impedance of the realized antenna.

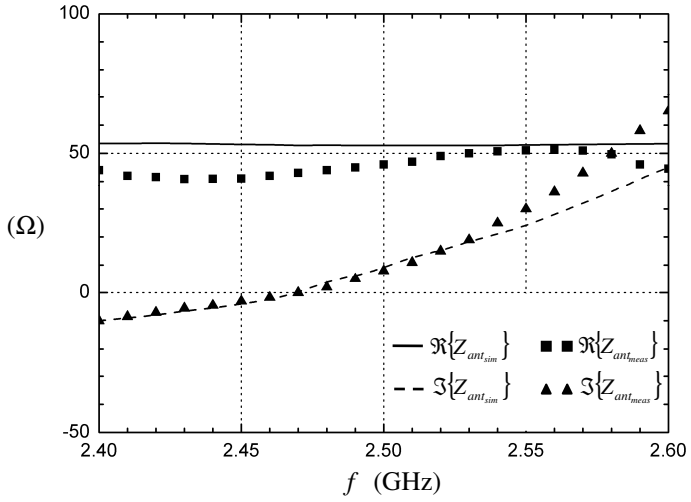


Figure 5.12: Simulated and measured impedance of the realized 50 Ω waveguide antenna.

The differences between the simulated and the measured curves may result from the inaccuracies in the technological fabrication process of the transition. Another source of discrepancies is that the relative permittivity of the used FR4 substrate may differ slightly from the value set in the simulation model. Nonetheless, the good agreement between the simulation and the measurement attests that waveguide antennas can be realized and excited as proposed above. Furthermore, it validates the developed impedance measurement procedure in the 2.45 GHz ISM band.

5.4.4 IMPEDANCE CONTROL

As discussed in Subsection 3.3.3, the antenna should provide the adequate impedance at the transition contacts to maximize the communication range between the interrogator and the transponder. Basically, the antenna impedance at the fundamental frequency can be transformed to the required value using a matching network consisting of discrete inductors and capacitors. Though this approach is always theoretically practicable, it presents the following inconvenient: not all inductance or capacitance values are provided by vendors. Furthermore, for cases where the signal frequency is very high, the waveguide cross section and thus the substrate area may be not large enough, disabling the use of additional discrete devices. To avoid this problem, an alternative method to tune the waveguide antenna impedance is required.

It has been observed that the waveguide antenna impedance can be influenced significantly by tuning some geometrical parameters of the waveguide-to-planar

transition depicted in Figure 5.11 [28]. In the case of the 2.45 GHz ISM band waveguide antenna presented in Subsection 5.4.3, the parameters a and b have been tuned, while the parameters c, d, … i have been set to the same values than in Subsection 5.4.3. Hence, for $b = 5.7$ mm, reducing a increases the antenna resistance and decreases its reactance, as shown in Figure 5.13 (a). As well, for $a = 35$ mm, reducing b decreases both the antenna resistance and reactance as shown in Figure 5.13 (b).

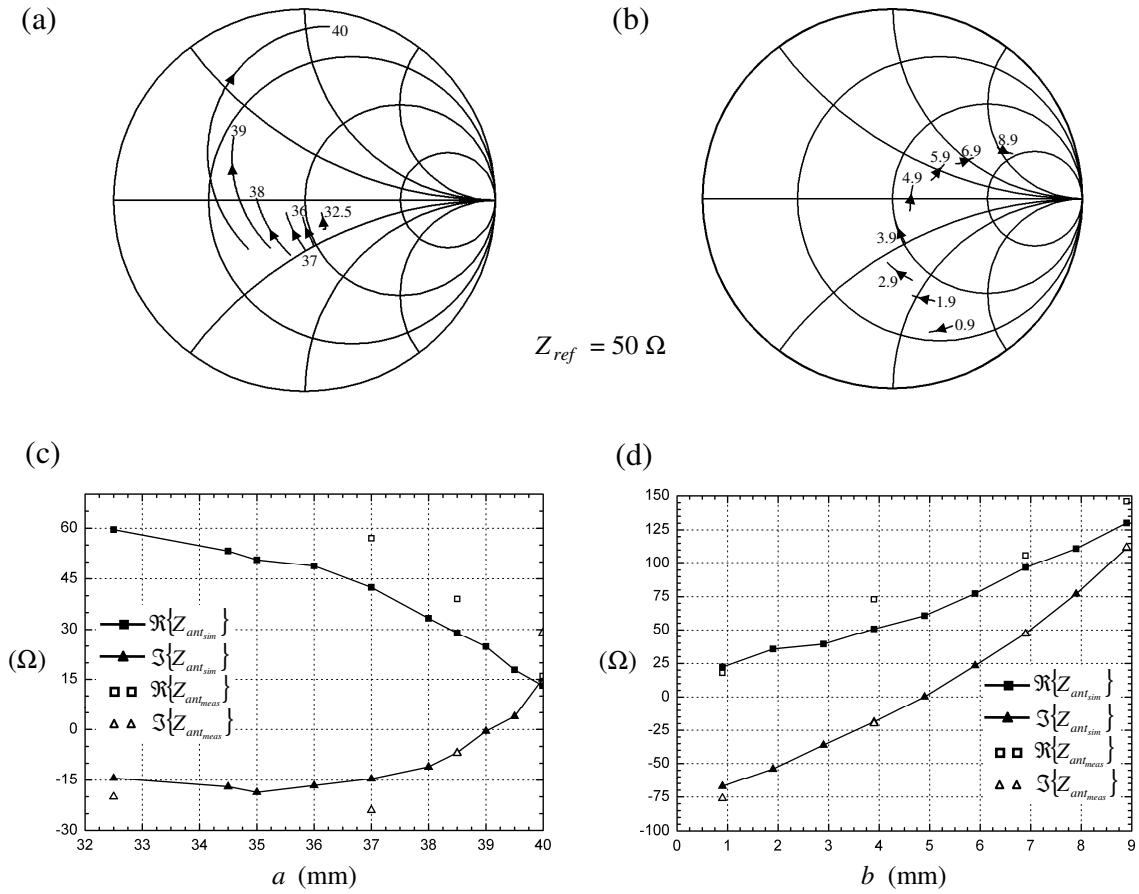


Figure 5.13: Smith chart plot of the antenna impedance in the 2.45 GHz ISM band by varying (a) the length a and (b) the length b. Resulting antenna impedance at the frequency 2.45 GHz by varying (c) the length a and (d) the length b.

Although the parameters a and b do not allow tuning either the antenna resistance or the antenna reactance independently, it is possible to realize a wide range of impedances by varying both of them.

For example, the resistance has been tuned from 60 Ω to 32 Ω at the frequency 2.45 GHz by setting $b = 5.7$ mm and varying the length a between 32.5 mm and 38 mm. The reactance remains hereby almost unchanged, as Figure 5.13 (c) shows.

On the other hand, the reactance can be tuned from -60 Ω to 110 Ω by setting a = 35 mm and varying b from 0.9 mm to 8.9 mm. The resistance varies hereby from 25 Ω to 130 Ω, as displayed in Figure 5.13 (d).
In cases where the targeted impedance cannot be realized using this method, the targeted antenna resistance or conductance can first be reached by tuning a and b as argued above, followed by connecting only one reactive component in series or in parallel between the transition contacts and the transponder circuit input.

5.5 RADIATION PROPERTIES

Additionally to a good impedance match at the transponder circuit input, the optimal alignment between the interrogator and transponder antenna should be sought to maximize the received power at the transponder. For this purpose, the radiation characteristics of the waveguide antenna should be analyzed.
The waveguide-to-planar transition has been designed to excite or couple the TE_{11} mode inside the cavity as long as the waveguide unambiguous frequency range is regarded. Each arm of the transition consists of a loop and a monopole. By exciting the transition at its contacts, it is expected that the radiated electromagnetic wave out of the cavity is linearly polarized according to the field distribution of the TE_{11} mode, whereby the electric field should be parallel to the transition monopoles.

5.5.1 MEASUREMENT SETUP

The waveguide antenna presented in Subsection 5.4.2 has been measured in an anechoic chamber to determine the far-field radiation pattern [28], as displayed in Figure 5.14.
The waveguide antenna is mounted on a turntable by means of a fixture. Coaxial cables have been connected to the transition according to Figure 5.9, whereby the cables have been inserted from the waveguide bottom through a small hole in order to disturb the field distribution as less as possible. The vector network analyzer feeds the antenna input through a balun to provide a differential excitation, since the transition is a balanced structure. The balun BIB-100G from Prodyn Technologies has been used. As coaxial cables, the 50 Ω semi-rigid cables EZ 34 with the following geometry data have been used:

Screen:	0.86 mm
Insulator:	0.66 mm (PTFE)
Centre conductor:	0.20 mm

Figure 5.15 depicts the entire measurement setup.

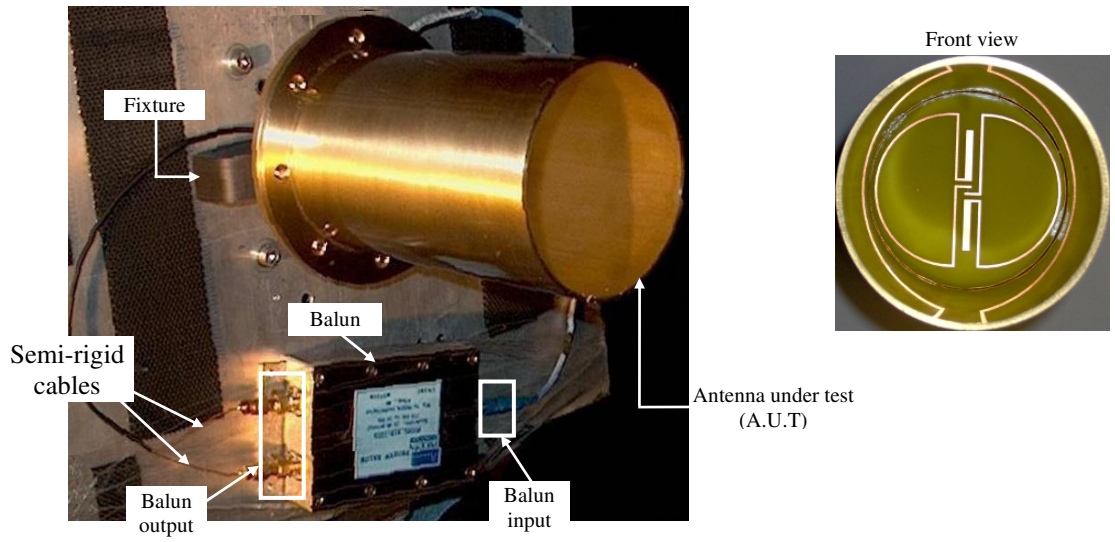


Figure 5.14: Waveguide antenna mounted on the turntable.

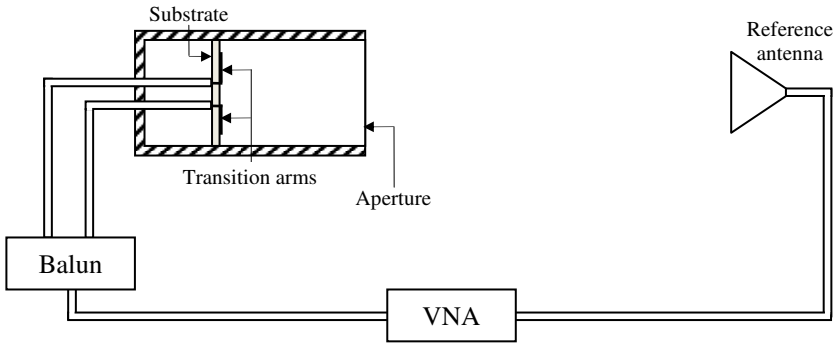


Figure 5.15: Schematic measurement setup.

5.5.2 MEASUREMENT RESULTS

The polar plot of the normalized magnitude of the electric field components $\vec{E}_\varphi$ and $\vec{E}_\vartheta$ in the $\varphi = 0°$ and $\varphi = 90°$-plane is depicted in Figure 5.16 (a) and Figure 5.16 (b), respectively. The orientation of the waveguide antenna and the used coordinate system are shown in Figure 5.17.

The magnitude of $\vec{E}_\vartheta$ and $\vec{E}_\varphi$ decreases as ϑ increases. This indicates that the antenna radiates with a unique lobe, and the main direction is the positive z-axis. The magnitude of $\vec{E}_\vartheta$ is significantly higher than that of $\vec{E}_\varphi$ in the z-axis. Hence, the radiated electromagnetic wave is linearly polarized and the polarization direction is parallel to the x-axis. Figure 5.18 displays the rectangular plot of the normalized magnitude of $\vec{E}_\vartheta$ and $\vec{E}_\varphi$ in the $\varphi = 0°$-plane. The axial-ratio is about 11 dB for $\vartheta = 0°$.

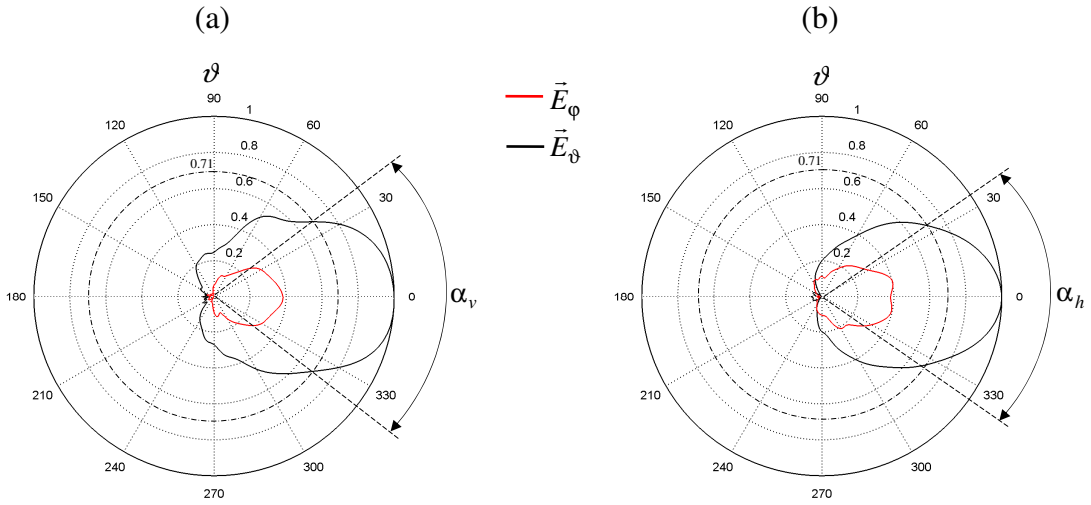


Figure 5.16: Polar plot of E_ϑ and E_φ in the (a) $\varphi = 0°$ and (b) $\varphi = 90°$ -plane.

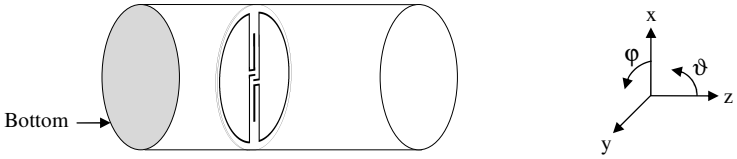


Figure 5.17: Coordinate system.

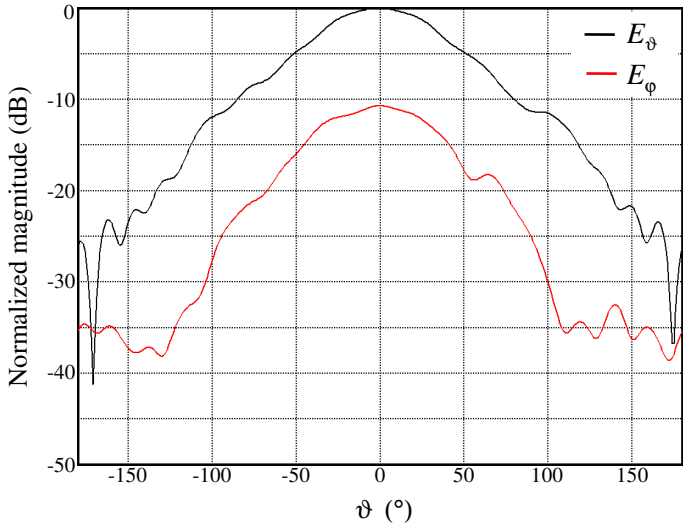


Figure 5.18: Polar plot of E_ϑ and E_φ in the $\varphi = 0°$ -plane.

The vertical and horizontal 3 dB beam widths α_v and α_h depicted in Figure 5.16 have been obtained by determining the angles where the normalized magnitude of $\vec{E}_\vartheta$ falls

below the value 0.707. Using the polar plots in Figure 5.16, it results: $\alpha_v \approx 72°$ and $\alpha_h \approx 66°$.

5.6 CONCLUSION

The developed waveguide-to-planar transition permits the use of the cavity as waveguide antenna for a wireless communication module integrated inside. The impedance of the antenna can be tuned in a wide range by varying the geometry parameters of the transition. This is a comfortable method to provide the adequate antenna impedance to the input of the transponder circuits, which will be integrated in metallic objects. The linear polarization and the relatively small beam width announce that the alignment between the interrogator and transponder antenna will be a critical factor for the communication range.

6 INTEGRATED 5.8 GHZ ISM BAND TRANSPONDERS

This chapter presents a practical realization of transponders integrated in a metallic work piece using design rules from the previous chapters. The systems should operate in the 5.8 GHz ISM band since it is license free. Lower ISM bands are not considered since the required diameter of the waveguide antenna will be too large, as discussed in Section 5.2. Designing a discrete rectifying circuit for the next higher ISM band, that is the 24 GHz ISM band requires special devices with almost unavailable SPICE parameters in the frequency range of interest. This would lead to highly inaccurate analyses.
The cavity is filled for further reduction of the minimum required diameter. The polymers polymethylmethacrylate (PMMA) also called acrylic, acrylonitrile butadiene styrene (ABS) and polycarbonate (PC) are selected as filler materials because of their availability and easy manageability. Their relative permittivity has been measured by means of a resonator method to 2.66, 2.71, and 2.84, respectively. The respective loss tangents are 0.0051, 0.0044, and 0.0047. These values have been obtained at the frequency 5.57 GHz. Assuming identical values for the 5.8 GHz ISM band, the waveguide diameter is set to 20 mm. Furthermore, the amplitude modulation is selected for data transmission.

6.1 DEVICES AND DESIGN METHODOLOGY

The transponder to design consists of a waveguide antenna, a rectifier and a logic unit, according to Figure 4.8. The circuit consists of discrete SMD components and is realized on the substrate of the waveguide-to-planar transition.

6.1.1 MICROCONTROLLER

The microcontroller PIC12F510 from Microchip is selected as logic unit. It requires a minimal DC supply voltage of 1.6 V to operate. Its internal clock frequency f_{clock} can be set whether to 4 MHz or 8 MHz by programming. An instruction cycle and thus the shortest output bit takes 1 µs for $f_{clock} = 4$ MHz, and it is 0.5 µs for $f_{clock} = 8$ MHz. Furthermore, the minimum required current is 117 µA and 171 µA and for

$f_{clock} = 4$ MHz and $f_{clock} = 8$ MHz, respectively. Hence, the highest input resistance $R_{\mu C}$ of the logic unit is 13.7 kΩ and 9.4 kΩ for $f_{clock} = 4$ MHz and $f_{clock} = 8$ MHz, respectively [42].
The PIC12F510 has five digital output ports and can feed external resistances for modulation tasks. Furthermore, it includes a three channel analog-to-digital converter (ADC), whose utility will be shown in Paragraph 6.2.4.3. The microcontroller die is encapsulated in an 8-lead small outline integrated circuit (SOIC) package as depicted in Figure 6.1 (a). Figure 6.1 (b) gives a simplified pin diagram of the PIC12F510. The DC supply voltage should be applied between the V_{DD} pin and the Gnd pin, which correspond to the positive and negative pole, respectively. The pins GP0, ···, GP5 can be set as digital input or output ports (GP3 excepted). The pins AN0, AN1 and AN2 are connected to the internal ADC and thus, can be set as analog input ports.

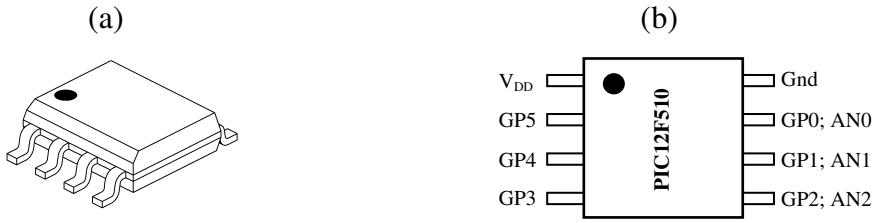


Figure 6.1: (a) 8-lead SOIC package; (b) simplified pin diagram of the PIC12F510.

6.1.2 DIODE

The Schottky diode BAT15-03W is selected for the voltage rectification because of its high saturation current $I_s = 130\,\text{nA}$, its short transit time $Tt = 25\,\text{ps}$, its low zero bias capacitance $C_{j0} = 0.26\,\text{pF}$, and its low ideality factor $n = 1.08$. The diode BAT15-03W has the breakdown voltage $B_V = 4\,\text{V}$. The other SPICE parameters, which are required for the circuit simulation, have been presented in Subsection 3.2.3. The diode die is encapsulated in a SOD 323 package, whose equivalent circuit model shown in Figure 6.2 should be included in the simulation schematic.

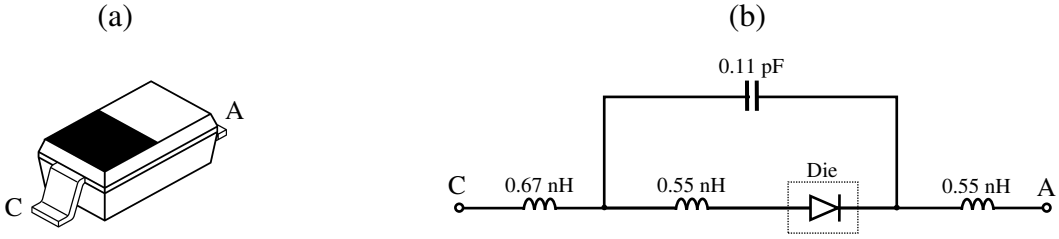


Figure 6.2: (a) SOD-323 SMD package; (b) equivalent circuit. A = anode and C = cathode.

6.1.3 DESIGN WITH ADS AND HFSS

6.1.3.1 CIRCUIT TOPOLOGY

The maximum achievable rectified voltage $v_{R,max}$ has been calculated regarding the highest resistance of the microcontroller using (2.38): a single-stage rectifier and a voltage doubler using the diode BAT15-03W would deliver at most 1.86 V and 3.70 V, respectively. Hence, as long as the available power is high enough, a single-stage rectifier would be theoretically sufficient to supply the microcontroller, which requires at least 1.6 V. However, the above estimation does not take into account the voltage drop over the diode path resistance. Furthermore, the resistance of the logic unit will be reduced during the modulation, decreasing the rectified voltage, as argued in Subsection 4.3.1. The resulting rectified voltage could then drop under the critical value of 1.6 V. Therefore, the rectifier is designed as voltage doubler to ensure sufficient supply voltage to the microcontroller for each modulator state.
It has been explained that the modulating circuit in Figure 4.8 modifies the resistive load of the rectifier. Thus, the transponder block diagram can be simplified as depicted in Figure 6.3.

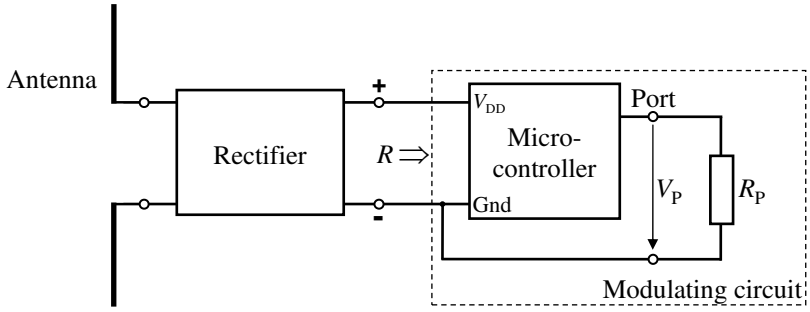


Figure 6.3: Transponder block diagram with modified modulating circuit.

The microcontroller controls the input resistance of the modulating circuit by driving or not the resistance R_P connected at one of its digital output port. This solution offers the advantage that no transistor is required, and that the modulation depth is a function of the resistance R_P.

6.1.3.2 DESIGN METHODOLOGY

The schematic of the simulated transponder circuit is shown in Figure 6.4. The circuit is analyzed by means of the simulation software ADS. The provided Harmonic Balance (HB) analysis controller treats the frequency conversion and thus, permits the calculation of the DC output voltage for a given available power at the antenna. The provided Large Signal S-Parameter (LSSP) analysis controller enables the calculation of the rectifier input impedance.
The diodes are modeled using the die SPICE parameters and the package model depicted in Figure 6.2 (b). The microcontroller is modeled by the resistance R. For the circuit capacitors, class GRM15 capacitors from Murata Manufacturing are chosen

because of their small size (1.0 mm × 0.5 mm) and their reliability in the frequency range of interest [45]. The metallic connections between the electric components are not modeled since their influences are expected to be negligible due to their small sizes compared to the wavelength. The antenna has been modeled using a port defined by the available power P_a and the internal impedance Z_a at the operation frequency. Figure 6.5 depicts the four steps design methodology of the rectifier.

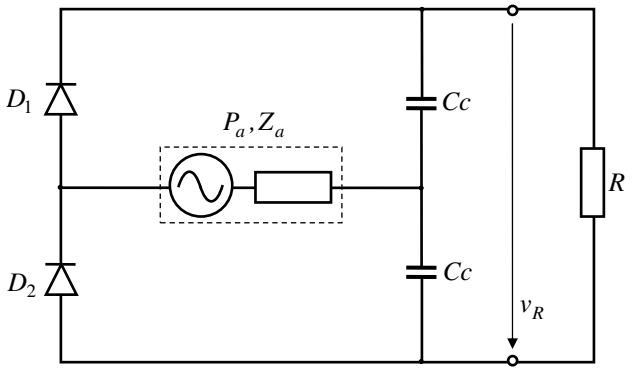


Figure 6.4: Schematic of the transponder circuit.

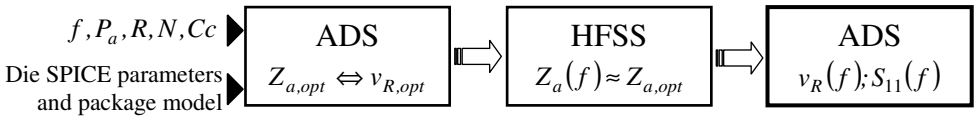


Figure 6.5: Simulation procedure.

1. The available power P_a is estimated as follows: the gain of the waveguide antenna is obtained from 3D field simulations with the software HFSS 11. Knowing the interrogator ERP or EIRP, the expectable available power P_a can be determined using (4.8) for a given distance and optimal alignment between the interrogator and transponder antennas, and under the assumption of power matching at each antenna.
2. The optimal port impedance $Z_{a,opt}$ providing the highest output DC voltage $v_{R,opt}$ is obtained from the HB and LSSP simulations in ADS. However, the software allows setting the port impedance only at the fundamental frequency. Thus, the port impedance at higher harmonics and at the frequency 0 Hz is not taken into account. This restriction could lead to discrepancies between measurements and simulation results.
3. The geometrical parameters of the waveguide-to-planar transition are tuned using HFSS to bring the waveguide antenna impedance Z_a as close as possible to the optimal value $Z_{a,opt}$. Generally, the realized impedance $Z_a(f)$ is frequency dependent in the frequency range of interest.
4. The port impedance in ADS is parameterized using an adequate function of the frequency f to coincide with the above simulated impedance $Z_a(f)$. The frequency response of the DC output voltage $v_R(f)$ can be computed therewith using the HB

analysis controller. Finally, the rectifier input impedance and consequently the resulting frequency dependent input reflection coefficient $\Gamma(f)$, which is defined as $S_{11}(f)$ in ADS, is computed by means of the LSSP analysis controller.

6.2 PRACTICAL IMPLEMENTATION

This section describes a practical simulation and realization of a transponder operating in the 5.8 GHz ISM band and integrated in a 20 mm wide and 49 mm deep cavity with metallic boundaries.

6.2.1 SIMULATION

The simulation steps are presented below:

1. The maximum interrogator ERP of 5 W is considered. The value of the waveguide antenna gain $G_R = 1.5$ dBi is obtained from simulations with HFSS. A communication range of $r = 25$ cm is arbitrarily assumed. Therewith the resulting available power is estimated to $P_a = 4$ dBm.

2. The microcontroller resistance and the circuit capacitors are set to $R = 8\,\text{k}\Omega$ and $Cc = 10$ pF, respectively. Simulations with ADS indicate that the optimal antenna impedance is $Z_{a,opt} = (3 + \text{j}5)\Omega$, leading to a rectified voltage of $v_{R,opt} = 2.7$ V.

3. To optimize the antenna impedance, the geometrical parameters of the waveguide-to-planar transition are tuned and set as follows: $a = 9.5$ mm, $b = 1.7$ mm, $c = 3.2$ mm, $d = 1$ mm, $e = 1.35$ mm, $f = 0.4$ mm, $g = 6.2$ mm, $h = 3.65$ mm and $i = 20$ mm. These parameters are depicted in Figure 5.11. The simulated impedance of the resulting waveguide antenna is displayed in Figure 6.6.

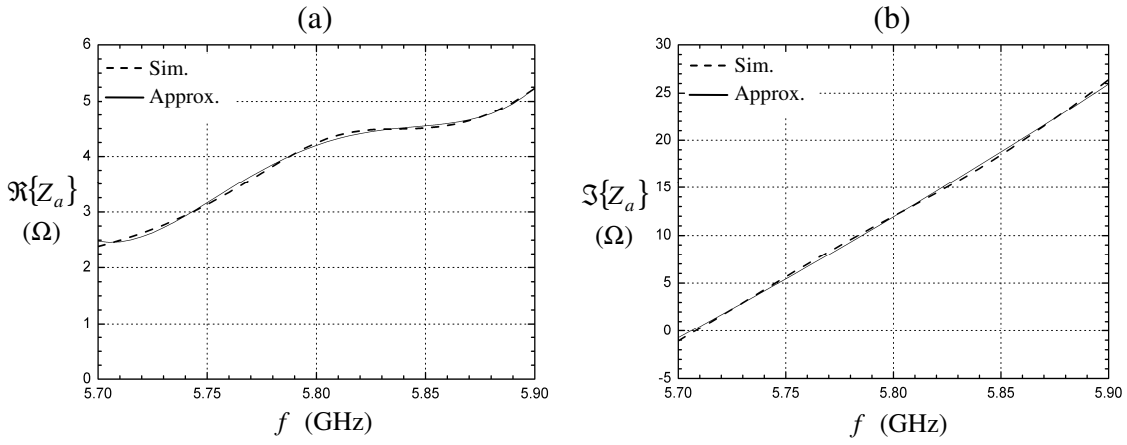


Figure 6.6: Simulated and approximated (a) resistance and (b) reactance of the antenna.

The optimal impedance is almost reached at the frequency 5.74 GHz. The antenna resistance and reactance are approximated by means of polynomials:

$$\Re\{Z_a\}(\Omega) = 2.481 - 0.725x + 6.601x^2 - 5.540x^3 + 1.383x^4, \tag{6.1}$$

$$\Im\{Z_a\}(\Omega) = -0.730 + 11.990x + 0.674x^2, \tag{6.2}$$

where the relation between the variable x and the frequency f is

$$x = 10^{-8} \cdot \left(f - 5.7 \cdot 10^9\right). \tag{6.3}$$

The frequency f in expressed in Hz in (6.3). The above polynomials are also displayed in Figure 6.6 for comparison.

4. The port impedance is parameterized using (6.1), (6.2) and (6.3), and the resulting output voltage is shown in Figure 6.7 for $R = 8\ \text{k}\Omega$ and $R = 5.5\ \text{k}\Omega$. In a wide frequency range, the expected DC voltage is higher than 1.6 V and thus, is sufficient to turn on the microcontroller.

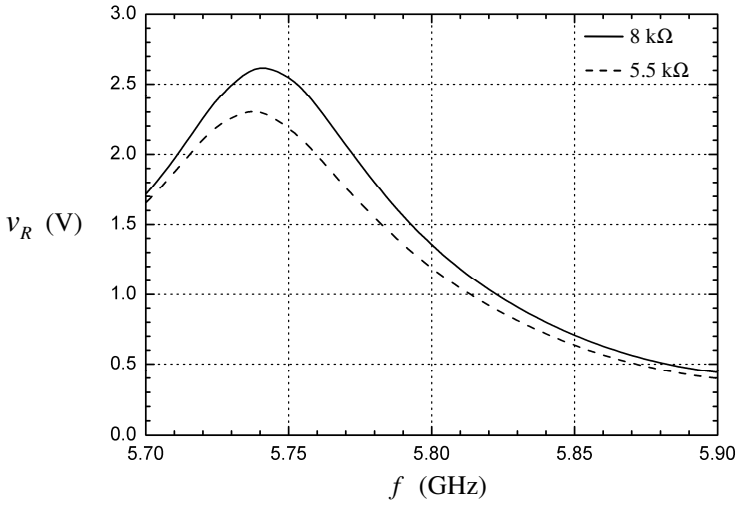


Figure 6.7: Simulated DC output voltage for two different rectifier load resistances.

The simulation of the ASK requires the knowledge of the expected changes of the modulating circuit input resistance R. Figure 6.8 shows measured values of R for different clock frequencies f_{clock} and for different driven port resistances R_{P}, whereby the mention $R_{\text{P}} = \infty$ means that the digital output port is open, or that its potential V_{P} is set to zero.

Assuming f = 5.74 GHz, f_{clock} = 8 MHz and R_P = 16 kΩ, the input resistance R will be switched between 8 kΩ and 5.5 kΩ, depending on whether the voltage V_P is set High or Low, according to Figure 6.7 and Figure 6.8. Figure 6.9 depicts the magnitude of the resulting reflection coefficient.

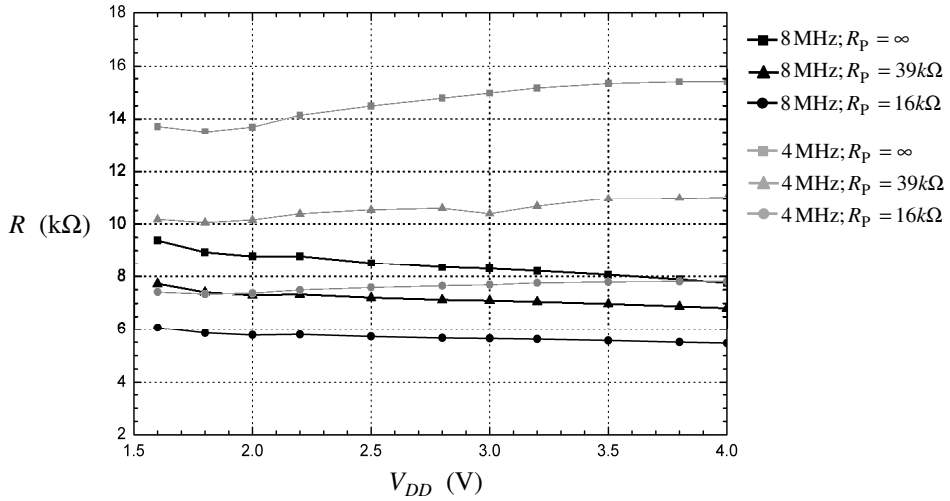


Figure 6.8: Resistance of the modulating circuit for different clock frequencies and port loads.

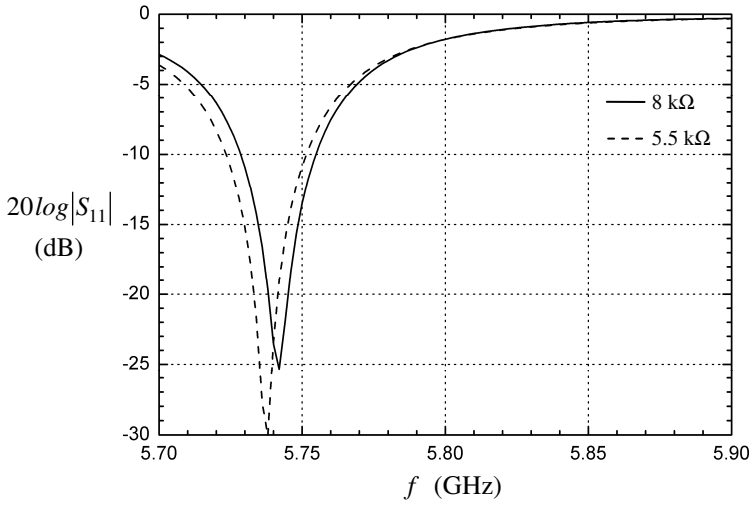


Figure 6.9: Magnitude of the input reflection coefficient for two different modulator states.

The above simulation results attest that the designed system can be sufficiently fed by the incident electromagnetic waves, and that the microcontroller can modulate the amplitude of the backscattered signal by controlling the potential at its digital output port.

6.2.2 CONSTRUCTION

The substrate of the waveguide-to-planar transition is Arlon AD450 with a thickness of 0.76 mm. The copper layer is 35 µm thick. The layout of the waveguide-to-planar transition and pictures of the assembled board are depicted in Figure 6.10.

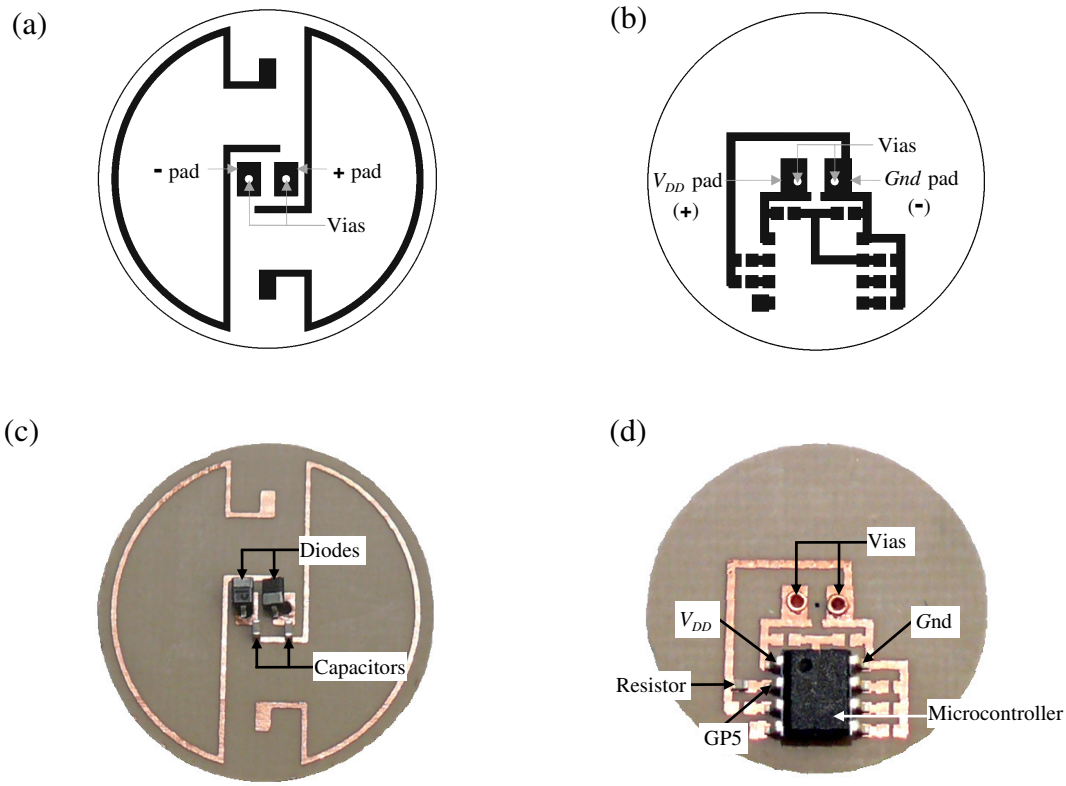


Figure 6.10: (a) Layout top side and (b) back side; pictures of the assembled board: (c) top and (d) back side.

The whole rectifier (diodes and the circuit capacitors) is mounted on the top side of the substrate, which also includes the transition arms. The rectangular pads in the middle of Figure 6.10 (a) are provided for connecting the diodes and the circuit capacitors. At the same time, they are the start points for the vias, which lead the DC voltage to the microcontroller mounted on the substrate back side [25].
The substrate has been structured by means of chemical etching. The cavity is 49 mm deep and is realized in a gear box cover made of cast aluminum. The board is embedded between two polymer pieces, as shown in Figure 6.11. Although the system has been simulated for the polymer ABS, the use of PC and PMMA was possible because their relative permittivities are in the same range.

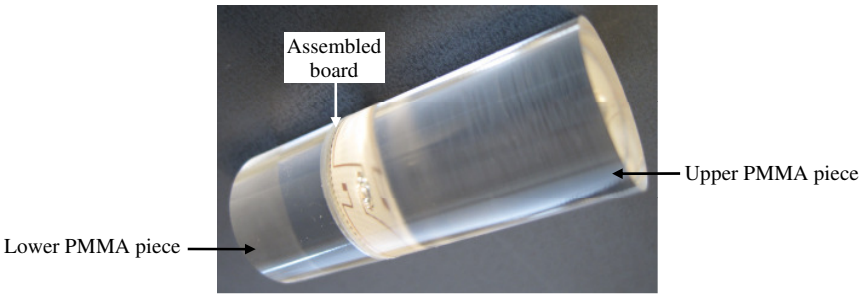


Figure 6.11: Transponder circuit board embedded between two polymer pieces.

The polymer pieces are structured to provide space for the circuit devices. The length of the lower piece is 18.5 mm and coincides to the quarter waveguide wavelength at the frequency 5.8 GHz. The upper piece is 29.7 mm long. Pictures of the transponder and the gear box cover are shown in Figure 6.12.

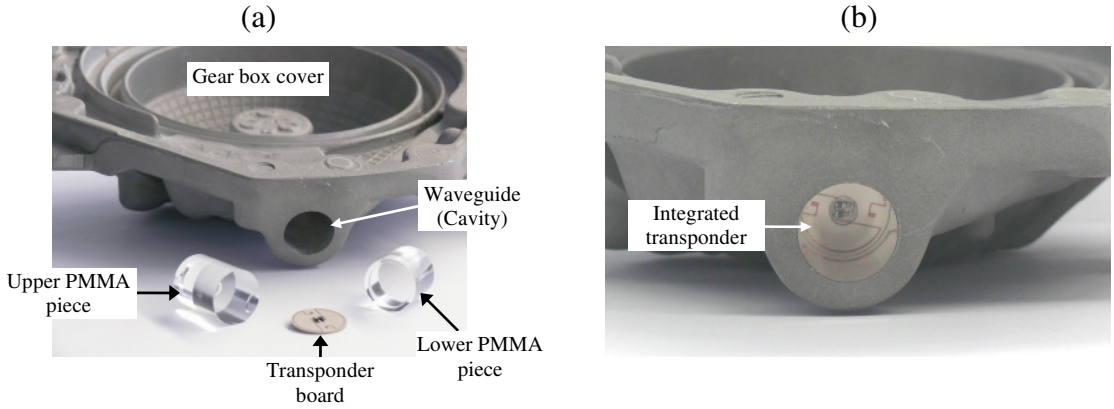


Figure 6.12: (a) Gear box cover with transponder components; (b) integrated transponder.

The method developed in Subsection 5.4.2 is inaccurate for frequencies above 3 GHz [19] and thus cannot be used to measure the antenna impedance. Even the measurement procedure presented in [22] is accurate below 4.5 GHz. It is assumed that the parasitic effects between the cables and the transition are more complex than in the model used in Subsection 5.4.2. Furthermore, simulations show that introducing coaxial cables through the polymer pieces affects drastically the antenna impedance. Nonetheless, the results presented in Subsection 5.4.3 allow the assumption that the realized 5.8 GHz ISM band waveguide antenna operates accordingly to the simulated model.

6.2.3 INTERROGATOR

The transmitter and receiver paths of the interrogator are realized as depicted in Figure 6.13. The used interrogator antenna is the planar antenna SPA-5600/40/14/0/V from Huber+Suhner. It provides a gain of about 13.5 dBi in the 5.8 GHz ISM band, and it radiates a linearly polarized wave. The signal generator MG3695B from Anritsu Technologies works as power source to deliver a continuous wave. The power amplifier MCU PA 602 from Kuhne Electronic permits to reach the maximum allowed ERP of 5 W. The receiver path is conceived as a common envelope detector: the directional coupler (circulator) separates the transmitted and the received waves and transmits the latter to the mixer. The mixer output signal is amplified and filtered. The resulting basis band signal is visualized by means of the digital oscilloscope TDS 3024B from Tektronix. The voltages V_{DD} and V_P are also monitored at the same oscilloscope during the data communication. For this purpose, three thin wires, which have been introduced from the back of the waveguide (similarly to Figure 5.15), contact the microcontroller pins V_{DD}, Gnd and GP5. The latter is connected to the port resistance R_P.

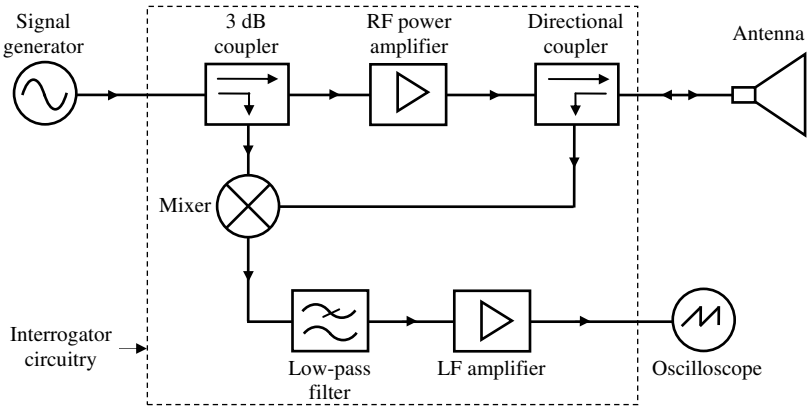


Figure 6.13: Interrogator block diagram.

Figure 6.14 shows the picture of the complete measuring station including the interrogator and a gear box cover with an integrated transponder.

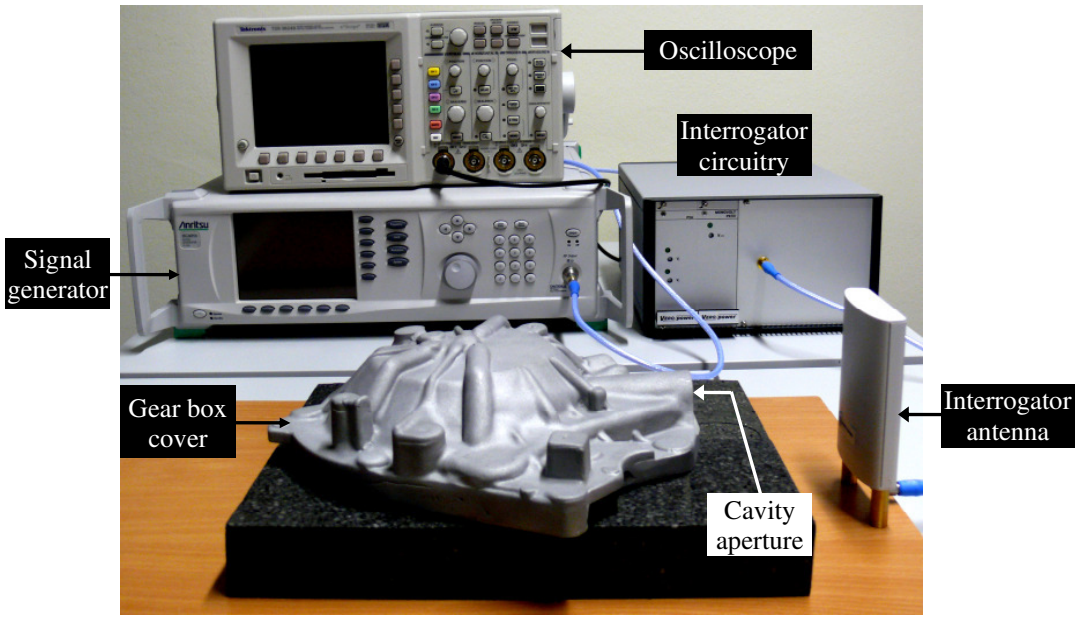


Figure 6.14: Measuring station.

6.2.4 RESULTS

The above realized transponder is used to achieve identification task and to perform temperature sensing and transmission. The implementation of these applications will be detailed in the following paragraphs.

6.2.4.1 IDENTIFICATION

The microcontroller has been programmed to transmit continuously an identification number by generating a specific sequence of rectangular pulses at the digital port GP5 loaded with the resistance $R_{P_5} = 15\ \text{k}\Omega$, as depicted in Figure 6.15 (a).

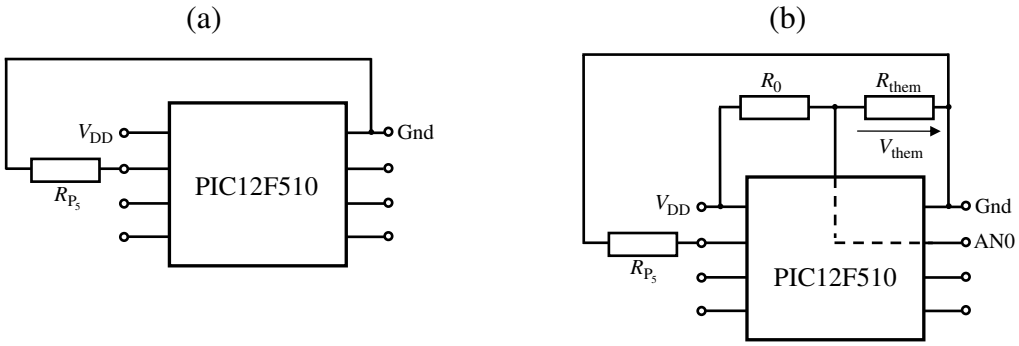


Figure 6.15: (a) Modulating circuit; (b) Modulating circuit with temperature sensing functionality.

The use of only port enables two modulator states and thus a 2-ASK. The pulse sequence at the port GP5 corresponds to the transmitted bit stream, whereby the maximum achievable bit rate $C_{\max}$ is determined by the length of the instruction cycle T_{cycle} as:

$$C_{\max} = \frac{1}{T_{\text{cycle}}}. \tag{6.4}$$

For experiments, the bit length has been set to 3 µs, leading to a bit rate of about 333.3 kb/s. Figure 6.16 depicts measurements of V_{DD}, V_P, and the normalized amplitude V_{osc} of the demodulated signal for an arbitrary time period.

Here, the distance between the interrogator antenna and the waveguide aperture is about 15 cm. The maximum achieved communication range was 22 cm. This limitation is defined by the minimum required voltage of the microcontroller and not by the interrogator receiver sensitivity, since latter can be enhanced at will by increasing the gain of the LF amplifier (see Figure 6.13).

The shape of the demodulated signal displayed in Figure 6.16 (b) coincides with the microcontroller output displayed in Figure 6.16 (a). This validates the proposed design procedure. Figure 6.16 (c) shows that the supply voltage decreases as the port resistance is driven. This fact has been predicted in Subsection 4.3.1.

The appearing noise in the demodulated signal is mainly due to the microcontroller: its supply current is not time constant for a given DC supply voltage, but contains regularly recurring peaks, causing a comb-shaped input resistance of the modulating circuit. This resistance has been measured during a modulation process and is depicted in Figure 6.17.

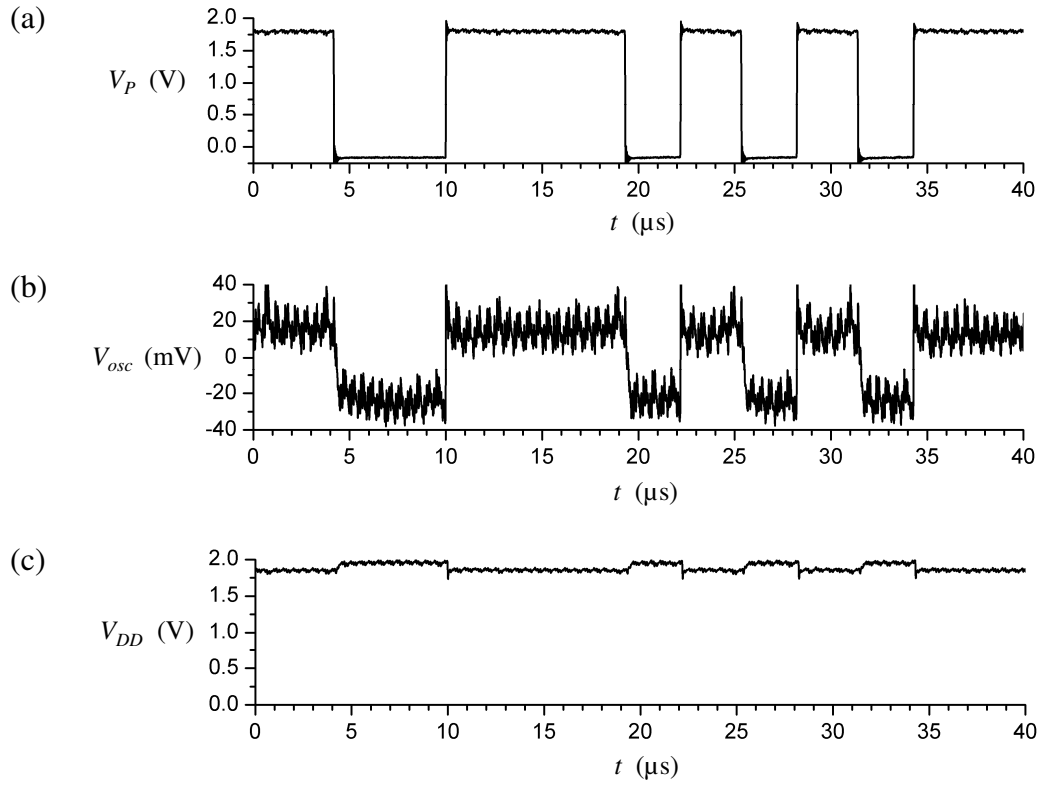


Figure 6.16: (a) Microcontroller output voltage; (b) normalized amplitude of the demodulated signal; (c) microcontroller supply voltage.

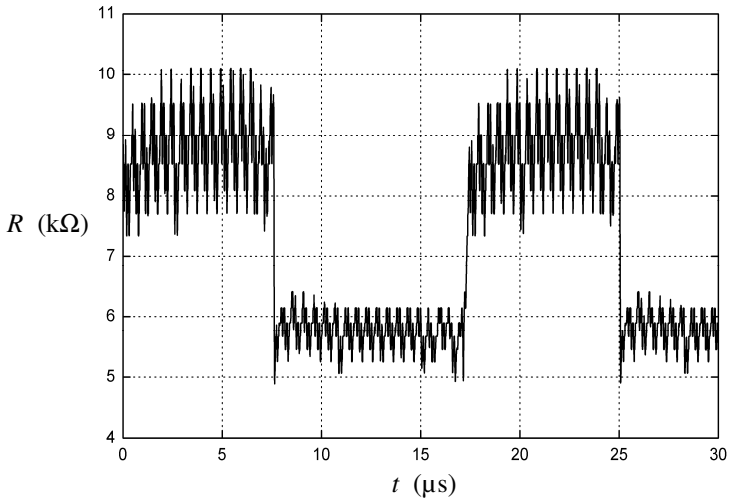


Figure 6.17: Resistance of modulating circuit during the modulation. f_{clock} = 8 MHz and R_{P} = 15 kΩ.

The use of more than one port to achieve the modulation enables the transmission of more than one bit per symbol. Hence, for a given number N_{P} of digital output ports used for the modulation, N_{P} bits can be transmitted per symbol. This would enable a

2^{N_P}-ASK if the resistances R_{P_1}, ···, $R_{P_{N_P}}$ loading the ports P_1, ···, P_{N_P}, respectively, are chosen such that the resulting modulating circuit resistance R is unique for each logic state combination at the output ports. In this case, the maximum achievable bit rate $C_{\max}$ is given as:

$$C_{\max} = \frac{N_P}{T_{\text{cycle}}}. \tag{6.5}$$

However, the effectively achieved data rate depends on the run application and on the implemented algorithm for the data preparation as well as for the ports control.

For experiments, the pins GP1 and GP4 are defined as digital output ports to transmit continuously an identification number by performing a 4-ASK. The resistances $R_{P_1} = 100\,\text{k}\Omega$ and $R_{P_4} = 15\,\text{k}\Omega$ are connected to GP1 and GP4, respectively. The microcontroller has been programmed to generate a particular digital state sequence at each port. Figure 6.18 depicts the demodulated signal.

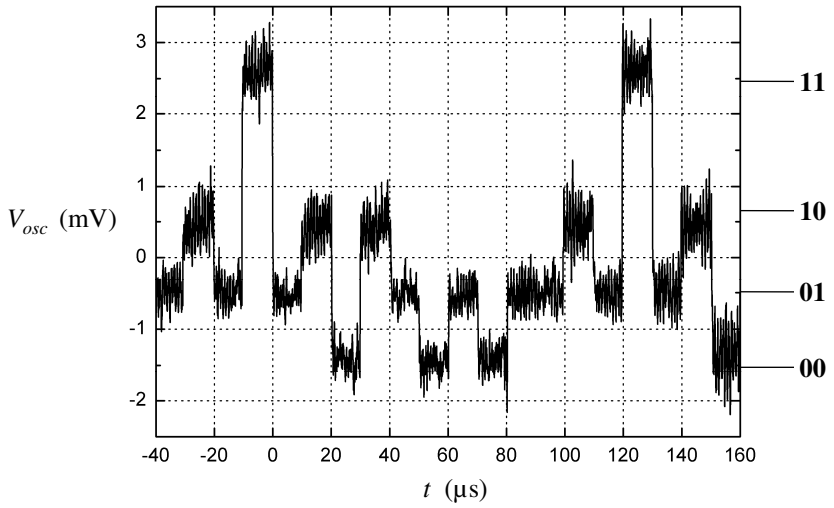


Figure 6.18: Demodulated 4-ASK signal. Each state is assigned to the corresponding 2-bit symbol.

Four levels can be easily distinguished in the shape of V_{osc}, attesting the possibility to realize a 4-ASK using the proposed method. Although the vertical distance between the different levels depend on the resistances R_{P_1} and R_{P_4}, they cannot be adjustable at will: one level is necessarily defined by the highest resistance of the modulating circuit. This takes place when all output port voltages are set to zero. The resistances R_{P_1} and R_{P_4} define the reflection coefficient magnitude when the ports GP1 and GP4 are set, respectively. However, the reflection coefficient magnitude when both ports are set is inevitably given by the value of the parallel circuit of R_{P_1} and R_{P_4}. This design

restriction can be avoided by generating N_P independent digital states using N_P ports. In this case, the maximum achievable bit rate is

$$C_{max} = \frac{\log_2(1+N_P)}{T_{cycle}}, \tag{6.6}$$

which is lower than the value given in (6.5).

6.2.4.2 REMOTE TEMPERATURE SENSING

The implementation of sensor functionalities into transponders is a growing trend [24, 30], since it permits the comfortable remote and wireless monitoring of the operating conditions of work pieces and installations, even in places difficult to access. Here, the temperature measurement inside the gear box cover is implemented using the internal 8-bit ADC of the transponder microcontroller.
For this purpose, a potential divider consisting on an almost temperature independent resistance R_0 and a thermistor R_{them} is mounted on the transponder board, as shown in Figure 6.15 (b). The potential divider is supplied by the rectifier and receives the same voltage than the microcontroller. The analog input port AN0 leads the voltage V_{them} across the thermistor to the ADC, which converts it in an 8-bit word. Then the CPU uses this 8-bit word as internal register to control the logic state and consequently potential at the digital output port GP5. The received word can be converted into a temperature value if R_0 and the temperature characteristics of R_{them} are known. Variations of the supply voltage do not affect the temperature measurement, since the ADC uses the microcontroller supply voltage as reference to perform the conversion.
The temperature measurement accuracy is mainly limited by the errors resulting from the analog-to-digital conversion.

6.3 CONCLUSION

The combined use of the circuit and field simulation software ADS and HFSS, respectively, permits the design of transponders integrated in metallic objects. The reduction of the cavity diameter can be enhanced by means of filler materials with higher dielectric constant, such as ceramic, whereby the corresponding loss tangent should be taken into account. The rectifier has been designed using rules and criteria extracted from Chapter 2 and Chapter 3. The ASK proposed in Chapter 4 has been successful implemented. The ADC of the microcontroller offers the possibility of remote temperature sensing. Using a microcontroller with lower power consumption and lower minimum operating DC voltage should permit to increase the communication range.
The simplicity of the circuit topology as well as the low number and complexity of the required electronic devices make the presented design method particularly attractive for discrete solutions.

7 CONCLUSION

The presented work consists mainly of three thematic focuses. The introduction addresses the problematic of the voltage rectification in field-powered communication systems, and the most used rectifier topologies using diodes are presented as analysis objects. The first goal of the analysis is the mathematical extraction of the rectifier AC-to-DC conversion function, and therewith, the formulation of design rules to maximize the rectified voltage. The second goal is the mathematical description of the rectifier input impedance in order to perform input power matching, and to derive criteria for the realization of backscatter modulation. The third and last main focus is the development of a method permitting the integration of communication modules into metallic objects.

The time-domain analysis of rectifiers using diodes and excited by an ideal AC voltage source led to a general AC-to-DC conversion function, which takes into account the number of diodes, the load resistance as well as the diode properties described by means of SPICE parameters. It results from the analyses, that the conversion function is the same for Cockcroft-Walton rectifiers, Dickson charge pumps, as well as for Greinacher rectifier, under the assumption that the circuit capacitances behave as short-circuits at the fundamental frequency. A low ideality factor and a high saturation current are the diode requirements to increase the rectified voltage. Therefore, Schottky diodes have been chosen: they provide high saturation currents and low transit times. This make them particular suitable for low-power rectification tasks in the microwave range. Furthermore, Schottky diodes have often a low breakdown voltage, and analyses showed that the maximum achievable DC voltage is drastically limited by this device parameter. It could finally be concluded that, the higher the load resistance the higher the rectified voltage.

The non-linear capacitance-voltage characteristic of the Schottky diode depletion capacitance can be accurately approximated using a high order polynomial, whose coefficients depend only on the junction built-in potential and the grading coefficient. As such, the calculation of the input impedance of rectifiers excited by an ideal AC voltage source is analytically possible, and investigations showed that Cockcroft-Walton rectifiers, Dickson charge pumps, and Greinacher rectifiers including identical diode type and number have the same input impedance. In field-powered systems, the excitation of the rectifier is performed by an antenna, whose equivalent circuit consists on an ideal AC voltage source in series with an impedance. Therefore,

the rectifier analysis has been correspondingly enhanced. To build on the previous findings, the antenna impedance should meet some conditions to suppress the effects of high harmonics currents. Under these assumptions, the complete system description including the available power, the antenna impedance, the rectifier input impedance, the number of diodes, the diode properties, the load resistance as well as the DC output voltage has been achieved by means of time-domain and frequency-domain analyses. An important result of this investigation is that the less the number of diodes, the higher the achievable DC output voltage. Sensitivity analyses show that the input power mismatch due to disadvantageous antenna reactance decreases the DC output voltage more than disadvantageous antenna resistance. As well, the diode breakdown voltage is a major limiting factor to the achievable overall conversion efficiency.

The proposed transponder circuit consists of an antenna, a rectifier, and a logic unit, which performs the modulation. The input impedance of the rectifier is given among others by the load resistance at the rectifier output. To perform a backscatter modulation, the reflection coefficient at the antenna has to be tuned according to the bit to be sent. Almost in all transponder designs, an electronic circuit is inserted between the antenna and the rectifier to tune the circuit input impedance seen by the antenna. In the new approach developed here, the load resistance of the rectifier is tuned by the microcontroller to influence the circuit input impedance and consequently the reflection coefficient. Depending on the optimal system configuration, that is by power match at the rectifier input, and depending on the sweep range of the load resistance, ASK or BPSK are achievable. By the ASK implementation, the larger the sweep range, the higher the magnitude variation of the reflection coefficient, and thus, the higher the modulation depth. However, power mismatch is a limiting factor for the ASK modulation depth, since a minimum power should be absorbed from the incoming electromagnetic wave to keep driving the logic unit. Sensitivity analyses showed that the sweep range for the load resistance as well as the achieved magnitude or phase of the reflection coefficient depend significantly on the available power and on the antenna impedance.

Novel investigations to integrate communication modules and especially passive transponders in metallic work pieces make use of cavities as dwell space. This ensures the protection of the electronic modules while keeping the evenness of the object surface. The cavities are realized as one side short-circuited waveguides and thus, they have good radiation properties, making the use of external antenna not necessary for field coupling. This advantage leads to the preference for the waveguide solution in comparison to coaxial cables or antipodal fin-lines as transmission lines between the object surface and the integrated communication module. The main disadvantage is the relation between the minimum required cavity diameter (or cross-section length in the case of rectangular waveguides) and the signal frequency, whereby the size reduction of the cavity cross section is achievable by using dielectric filler materials. The developed concept of novel waveguide-to-planar transitions offers comfortable solution for the targeted integration. The transition converts the field distribution in the cavity to a transversal electromagnetic field distribution at the transponder input. The resulting antenna impedance can be tuned in a wide range by varying the geometry parameters of the waveguide-to-planar transition. Hence, the optimal antenna impedance can be easily achieved without using additional reactive components. The realized waveguide

antenna radiates linearly polarized electromagnetic waves with a relatively small vertical and horizontal beam width.

The combined use of the circuit and field simulation software ADS and HFSS respectively, permits the development and integration of transponders in metallic work pieces. The polymers PMMA, ABS and PC have been used as dielectric filler materials to reduce the cavity diameter. In the selected 5.8 GHz ISM band, the cavity diameter and depth have been set to 20 mm and 49 mm, respectively. The microcontroller PIC12F510 has been chosen as core of the modulating circuit and requires a DC supply voltage of at least 1.6 V. The diode Schottky diode BAT15-03W has been selected as the best choice among the commercial available SMD diode for microwave rectification tasks, according to the design rules extracted from the general DC analysis of rectifiers. Its low breakdown voltage obliges the realization of a voltage doubler to ensure a sufficient DC supply voltage for the microcontroller. The ASK has been implemented according to the novel proposed method. On one hand, the achieved bit rate depends on the implemented software. On the second hand, the maximum achievable bit rate is strongly limited by the microcontroller clock frequency. The use of a microcontroller with low power consumption and low minimum operating DC voltage should increase the communication range. The provided ADC offers the possibility of wireless temperature sensing and transmission by means of a potential divider including a common thermistor.

The achieved analytical investigation of voltage multiplying rectifiers and the proposed development of a method to integrate communication modules into metallic objects permit the realization and optimization of field-powered transponders operating inside of work pieces, providing a solution to realize gentelligent components. The simplicity of the circuit topology as well as the low number and low complexity of the required devices make the presented design procedure attractive, especially for discrete transponder circuits.

8 REFERENCES

[1] Abramowitz M., Stegun I. A. (2002). *Handbook of mathematical functions with formulas, graphs, and mathematical tables* (10th edition). Norwich: Knovel.

[2] Agilent Technologies. (1999). *Designing the virtual battery.* Application note 1088.

[3] Amin N., Ng Wen Jye, Othman M. (2007). A BPSK backscatter modulator design for RFID passive tags. *Proceedings of the IEEE International workshop on radio-frequency integration technology*, Singapore, pp. 262-265.

[4] Balanis C. A. (2005). *Antenna theory* (3rd edition). New Jersey: John Wiley & Sons.

[5] Bernhard J. *et al*. (2007). RFID in metallic environment. *Proceedings of the 3rd European workshop on RFID systems and technologies*, Duisburg.

[6] Camp M., Eul H. (2006, July-December). Einsatz von RFID-Systemen zur kontaktlosen Identifikation von Objekten durch Funkübertragung. *Journal Telekommunikation Aktuell, Heft 07/12*.

[7] Chen C., Nejad M. B., L.-R. Zheng. (2006). Design and implementation of a high efficient power converter for self-powered UHF RFID applications. *Proceedings of the 1st International conference on industrial and information systems*, Peradeniya, pp. 393-395.

[8] Cojocari O. (2007). *Schottky technology for THz-electronics.* Shaker Verlag.

[9] Collin R. E. (1990). *Field theory of guided waves* (2nd edition). New York: IEEE Press.

[10] Curty J. P., Joehl N. (2005, December). A model for μ-power rectifier analysis and design. *IEEE Transactions on circuits and systems I, Vol. 52, No. 12*, pp. 2771-2779.

[11] De Vita G., Bellatalla F., Iannaccone G. (2006). Ultra-low power PSK backscatter modulator for UHF and microwave RFID transponders. *Microelectronics journal* (37), pp. 627-629.

[12] De Vita G., Iannacone G. (2005, September). Design criteria for the RF section of UHF and microwave passive RFID transponders. *IEEE Transactions on microwave theory and techniques, Vol. 53, No. 9*, pp. 2978-2990.

[13] De Vita G., Iannacone G. (2005). Ultra low power RF section of a passive microwave RFID transponder in 0.35 µm BICMOS. *Proceedings of the IEEE International symposium on circuits and systems 2005*, *Vol. 5*, Kobe, pp. 5075-5078.

[14] Denkena B., Battino A., Liedtke C. (2006). Optimization of process parameters with gentelligent components. *Proceedings of the XVII Workshop on supervising and diagnostics of machining systems*, Wroclaw, pp. 15-23.

[15] Denkena B., Hasenfuß K., Liedtke C. (2005, September). Gentelligente Bauteile – Genetik und Intelligenz in der Produktionstechnik. *ZWF – Zeitschrift für wirtschaftlichen Fabrikbetrieb, Vol. 100, No. 10*, pp. 569-572.

[16] Dobkin D. M. (2008). *The RF in RFID.* Amsterdam: Elsevier.

[17] Finkenzeller K. (2003). *RFID Handbook* (2nd edition). Chichester: John Wiley & Sons.

[18] Harrison R. G., Le Polozec X. (1994, May). Nonsquarelaw behavior of diode detectors analyzed by the Ritz-Galerkin method. *IEEE Transactions on microwave theory and techniques, Vol. 42, No. 5*, pp. 840-846.

[19] Herschmann R. *et al*. (2006). Ein Verfahren zur breitbandigen Impedanzmessung von RFID Transponderantennen. *Proceedings of the 2nd European workshop on RFID systems and technologies*, Erlangen.

[20] Infineon. (2007). *Datasheet.* http://www.infineon.com/cms/en/product/channel.html.

[21] Johnson J., Sainati R. (2007). Investigation of UHF RFID tag backscatter. *Proceedings of the 2007 IEEE Antennas and propagation society international symposium*, Honolulu, pp. 2753-2756.

[22] Kaldjob E. B., Geck B., Eul H. (2009). Impedance measurement of properly excited small balanced antennas. *IEEE Antennas and wireless propagation letters, Vol. 8*, pp. 193-195.

[23] Kaldjob E. B., Geck B., Eul H. (2008, December). Comments on "Measuring the impedance of balanced antennas by an S-parameter method". *IEEE Antennas and propagation magazine, Vol. 50, No. 6*, pp. 113-114.

[24] Kaldjob E. B., Geck B., Eul H. (2008). Field powered 5.8 GHz ISM band transponder for sensors integrated in metallic objects. *Proceedings of the 38th European microwave conference*, Amsterdam, pp. 1719-1722.

[25] Kaldjob E. B., Geck B., Eul H. (2008). Reduced size 5.8 GHz ISM band transponder integrated in metallic work pieces. *Proceedings of the 2008 International symposium on antennas and propagation*, Taipei.

[26] Kaldjob E. B. *et al*. (2007). A novel planar cylindrical waveguide-to-planar transition for transceivers at 2.45 GHz band. *Proceedings of the 37th European microwave conference*, Munich, pp. 87-90.

[27] Kaldjob E. B., Gamal El Din M., Geck B. (2007). A novel planar cylindrical waveguide-to-planar transition for transceivers at 2.45/5.8 GHz band. *Proceedings of the 2007 International symposium on antennas and propagation,* Niigata, pp. 1015-1018.

[28] Kaldjob E. B. *et al*. (2008). Impedance control and radiation properties of a 2.45 GHz ISM band wave guide antenna for embedded transponders in metallic objects. *Proceedings of the 2008 International symposium on antennas and propagation*, Taipei.

[29] Karthaus U., Fischer M. (2003, October). Fully integrated passive UHF RFID transponder IC with 16.7-µW minimum input power. *IEEE Journal of solid-state circuits, Vol. 38, No. 10*, pp. 1602-1608.

[30] Kitayoshi H., Sawaya K. (2005). Long range passive RFID-tag for sensor networks. *Proceedings of the IEEE 62nd Vehicular technology conference*, *Vol. 4*, pp. 2696-2700.

[31] Kurokawa K. (1965, March). Power waves and the scattering matrix. *IEEE Transactions on microwave theory and techniques, Vol. 13, No. 3*, pp. 194-202.

[32] Lange F. (2007, February). Der Bauplan im Innern-Plagiatschutz durch Werkstückkennzeichnung innerhalb des Bauteils. *phi-Produktionstechnik Hannover informiert*, Hanover, pp. 10-11.

[33] Lehpamer H. (2008). *RFID design principles.* Norwood: Artech House.

[34] Lewin L. (1975). *Theory of waveguides.* London: Butterworth & Co. Ltd.

[35] Liou J. J. (1994). *Advanced semiconductor device physics and modeling.* Norwood: Artech House.

[36] Ma C., Zhang C., Wang Z. (2007). A low-power AC/DC rectifier for passive UHF RFID transponders. *Proceedings of the 2007 International symposium on microwave, antenna, propagation and EMC technologies for wireless communications*, Hangzhou, pp. 309-314.

[37] Massobrio G., Antognetti P. (1993). *Semiconductor device modeling with Spice* (2nd edition). New York: McGraw-Hill.

[38] McSpadden J. O., Fan L., Chang K. (1998, December). Design and experiments of a high-conversion-efficiency 5.8-GHz rectenna. *IEEE Transactions on microwave theory and techniques, Vol. 46, No. 12*, pp. 2053-2060.

[39] Meinke H. H., Gundlach F. W. (1986). *Taschenbuch der Hochfrequenztechnik* (4th edition), Vol. G, Berlin / Heidelberg: Springer.

[40] Meinke H. H., Gundlach F. W. (1986). *Taschenbuch der Hochfrequenztechnik* (4th edition), Vol. O, Berlin / Heidelberg: Springer.

[41] Meys R., Janssens F. (1998, December). Measuring the impedance of balanced antennas by an S-parameter method. *IEEE Antennas and propagation magazine, Vol. 40, No. 6*, pp. 62-65.

[42] Microchip. *PIC12F510/16F506 Data Sheet.*

[43] Mishra U., Singh J. (2008). *Semiconductor device physics and design.* Dordrecht: Springer.

[44] Moss T. S. (1993). *Handbook on semiconductors* (Vol. 4). Amsterdam: Elsevier.

[45] Murata Manufacturing Co. [Online]. http://www.murata.com/products/

[46] Nikitin P. V., Rao K. (2006, December). Theory and measurement of backscattering from RFID tags. *IEEE Antennas and propagation magazine*, pp. 212-218.

[47] Nikitin P. V., Rao K. (2005, September). Power reflection coefficient analysis for complex impedances in RFID tag design. *IEEE Transactions on microwave theory and techniques, No. 9*, pp. 2721-2725.

[48] Nyhuis P., Fisser F., Schmidt M. (2008). Gentelligent factory structures and assembly control. *Proceedings of the 4th IPROMS Virtual international conference.*

[49] Panitantum N. *et al*. (2002). A CMOS RFID Transponder. *Proceedings of the International symposium on communications and information technologies,* Pattaya.

[50] Parker G. (1994). *Introductory semiconductor device physics.* Hertfordshire: Prentice Hall.

[51] Paul R. (1992). *Elektronische Bauelemente* (3rd edition). Stuttgart: Teubner.

[52] Pylarinos L., Rogers E. S. *Charge pumps: an overview.* University of Toronto.

[53] Ranasinghe D. C. *et al*. (2004). A small UHF label antenna for embedding in metallic objects. *Auto-ID Labs workshop.* Zurich.

[54] Ranasinghe D. C. *et al*. (2004). An embedded UHF RFID label antenna for tagging metallic objects. *Proceedings of the 2004 Intelligent sensors, sensor networks and information processing conference*, pp. 343-347.

[55] Schlachetzki A. (1990). *Halbleiter-Elektronik.* Stuttgart: Teubner.

[56] Seemann K., Weigel R. (2005, June). Ultra-low-power rectification in passive RFID tags at UHF frequencies. *Frequenz, journal of RF-engineering and telecommunications, Vol. 59, No. 5-6*, pp. 112-115.

[57] Sperling M. (2003). *RF to DC converter in SiGe process.* Carnegie Mellon University.

[58] Sze S. M. (2002). *Semiconductor devices, physics and technology* (2nd edition). New York: John Wiley & Sons.

[59] Turner C. (2003). Backscatter modulation of impedance modulated RFID tags.

[60] Um Y. *et al*. (2007). A novel antenna design for UHF RFID tag on metallic objects. *Proceedings of the 2007 Progress in electromagnetics research symposium*, Prague, pp. 158-161.

[61] Unger H.-G. (1981). *Elektromagnetische Theorie für die Hochfrequenztechnik* (Teil I). Heidelberg: Hüthig.

[62] Wang Z. *et al*. (2007). Issues in integrated circuit design for UHF RFID. *Proceedings of the IEEE International workshop on radio-frequency integration technology*, Singapore, pp. 322-328.

[63] Waidelich D. L., Shackelford C. L. (1944). Characteristics of Voltage-Multiplying Rectifiers. *Proceedings of the Institute of radio engineers*, *Vol. 32, Issue 8*, pp. 470-476.

[64] Yuan J. S., Liou J. J. (1998). *Semiconductor device physics and simulation.* New York: Plenum Press.

[65] Yuan T. *et al*. (2007). Passive RFID-Tag designed using discrete components. *Proceedings of the 2007 International symposium on antennas and propagation*, Niigata, pp. 616-619.

[66] Zhu Z., Jamali B., Cole P. (2004). *Brief comparison of different rectifier structures for HF and UHF RFID.* University of Adelaide, Auto-ID Lab.

[67] Zhu Z., Jamali B., Cole P. (2005). *An HF/UHF RFID analogue front-end design and analysis.* University of Adelaide, School of electrical and electronics engineering, Adelaide, Australia.

[68] Zirath H. *et al*. (1988, November). Temperature variable noise and electrical characteristics of Au-GaAs Schottky barrier millimeter-wave mixer diodes. *IEEE Transactions on microwave theory and techniques, Vol. 36*, pp. 1469-1475.

Lebenslauf

Persönliche Daten

Vor-, Nachname	Eddy Brice, Kaldjob
Geburtstag	22.06.1980
Geburtsort	Yaounde, Kamerun
Staatsangehörigkeit	kamerunisch
Familienstand	ledig
Eltern	Jean Victor, Kenla
	Angélique Hélène, Kenla geb. Ngo Njé

Schulbildung und Sprachkurse

1986 – 1990	Grundschule in Yaounde, Kamerun
1990 – 1995	Gymnasium: Lycée d'Élig-Essono in Yaounde, Kamerun
1995 – 1997	Gymnasium: Lycée de Nkol-Éton in Yaounde, Kamerun Abschluss Juli 1997: Abitur
1997	Deutschkurs am Goethe Institut in Yaounde, Kamerun
1998	Deutschkurs an der Technischen Universität Braunschweig 1. Abschluss März 1998: Zertifikat Deutsch als Fremdsprache 2. Abschluss Oktober 1998: Deutsche Sprachprüfung für den Hochschulzugang ausländischer Studienbewerber

Studium und Praktika

10.1998 – 08.2003	Studium der Elektrotechnik an der Technischen Universität Braunschweig Studienschwerpunkt: Informationstechnik Abschluss August 2003: Diplom
02.1999 – 03.1999	5 Wochen Grundpraktikum bei PPS in Salzgitter
08.1999	3 Wochen Grundpraktikum bei der PTB in Braunschweig
02.2001 – 04.2001	8 Wochen Fachpraktikum bei Siemens in Braunschweig
07.2001 – 08.2001	5 Wochen Fachpraktikum bei Deutsche Telekom in Braunschweig
07.2002 – 08.2002	5 Wochen Fachpraktikum bei Toshiba in Braunschweig

Beruflicher Werdegang

01.2004 – 06.2009	Wissenschaftlicher Mitarbeiter am Institut für Hochfrequenztechnik und Funksysteme der Leibniz Universität Hannover