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# Efficient modelling of IC conducted emission for power integrity analysis

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**Abstract.** In this paper two methodologies to reduce the complexity of IC conducted emission models for Power Integrity analysis in ICs are presented. The methodologies differ concerning the applicability in simulation tools, complexity and accuracy of the generated models. The first methodology uses a complex model and reduces its order to generate a model with a fewer number of elements. This methodology therefore involves a model order reduction approach. A second minimum complexity, module based modelling approach is introduced for rough estimations, as the order reduced model is still too complex for some applications. The two methodologies are applied to an IC conducted emission model of two digital modules of a 32 Bit microcontroller. The results of the three models are compared and discussed. Fields of application for the introduced modelling approaches are the estimation of the magnitude and time behaviour of the supply current as well as the determination of the number and position of the IC's supply pins.

## 1 Introduction

The ongoing development in the area of electronic circuit integration is accompanied by new, outstanding challenges in the field of low power design. This leads to more severe constraints in the field of power integrity, especially in regard to the ever decreasing supply voltages in modern electronic devices, circuits and systems. For a reduction of time-to-market by first-time right designs these low power and power integrity constraints need to be considered in an early stage of the design flow. To achieve this, the designer is reliant on modern, power-conscious EDA tools and accurate models that give insight to the power consumption and integrity behaviour at a high abstraction level of the design (Landman et al., 1994). For the estimation of the power integrity behaviour of integrated circuits (IC), IC Conducted Emission Models are created. Depending on the precision and simulation speed demands of the designer, different complexity levels for these models exist. Section 2 shows the necessity of reducing the complexity of certain IC conducted emission models and describes the structure of such models. The modelling methodologies of the two models with lower complexity, gained by reducing the size of the complex model, will be described in Sects. 3 and 4. In Sect. 5 simulation results of the three models are presented and compared. Section 6 gives a summary of the paper.

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## 2 IC conducted emission models

The three IC conducted emission models employed in this section describe the conducted emission behaviour of the supply system of an IC. The model with the highest level of complexity is generated with the so-called EXPO tool (Hesidenz and Steinecke, 2005).

It consists of several modules, each describing a specific functionality on the chip (e.g. digital, analogue, memory). Each module consists of up to hundreds of identical supply line models (SLM) forming a mesh (Fig. 1). The SLM therefore represents the basic element of the EXPO model. Each SLM contains a power distribution network (PDN) consisting of passive R, L, C elements, and an independent current source (Fig. 2) (Dhia et al., 2006).

While the PDN describes the parasitic electromagnetic effects of the on-chip power supply, the current source characterises the internal activity (IA), i.e. the simultaneous switching noise (SSN) of the transistors. The parameters of the passive elements of the PDN as well as the prescribed waveforms of the current sources vary from module to module, but are the same for all SLMs within one functional module. The parameters of the model are determined either during the IC design phase or by taking measurements on an existing chip.

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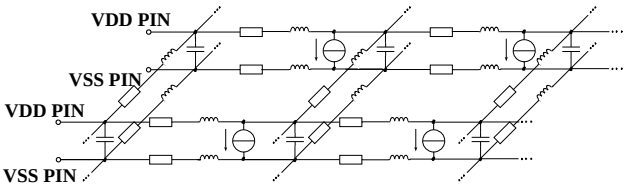


**Fig. 1.** Section of a functional module of the EXPO model consisting of a large number of SLMs.

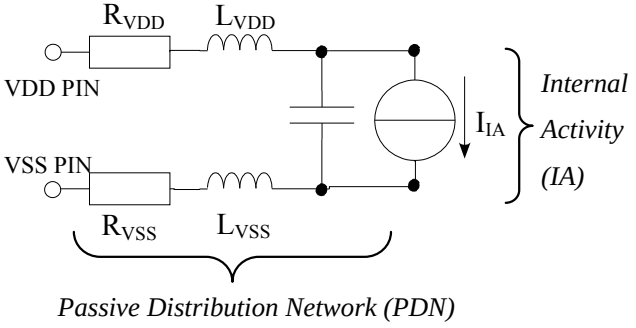


**Fig. 2.** Supply line model (SLM) consisting of PDN and IA.

Due to the relatively high complexity of the model gained with this approach, applicability in power integrity analysis tools is limited. IC conducted emission models with a smaller number of elements are required to lower the computational effort. Two methodologies to gain models adequate for the implementation in EDA tools by reducing the complexity of the EXPO model are presented here. While the computational effort is reduced and the ability to obtain information about the power integrity behaviour is preserved with these models, the accuracy is diminished to a certain degree compared to the complex model.

## 3 Modelling of an order reduced IC conducted emission model

The first modelling methodology involves a model order reduction (MOR) approach. The objective of the MOR modelling methodology is to reduce the size of the considered model and thereby its complexity while approximating the properties at the pins of the original network (Ludwig, 2008b). For MOR the electrical network of the IC conducted emission model has to be described with the help of the modified nodal analysis as a system of differential algebraic equations. Here the number of equations specifies the order of the system. To use MOR in IC conducted emission models efficiently, certain preparations have to be made in the network's description, as we have shown in Ludwig (2008a). The network description of the IC conducted emission model can now be reduced by the use of MOR algorithms. Order reduction of system descriptions of networks has to preserve their main properties. This is for example achieved by using moment matching, as we investigated in Radić-Weissenfeld (2009). Here we use the block Arnoldi algorithm, where every system matrix is directly reduced, resulting in a drastically reduced order of the system. It can be shown that the obtained transfer function of the considered network matches the original transfer function within the investigated frequency band. In a last step, the order reduced circuit equations have to be synthesised as an electrical network for simulations with power analysis tools. The network synthesis method we proposed in Ludwig (2008b) generates a network with a low number of nodes and is exported as a SPICE netlist. By reducing the complexity of the EXPO model by means of MOR, the EXPO model's SLM structure is not maintained in the final synthesis step, resulting in a model consisting of G, C components and controlled current sources (Fig. 3).

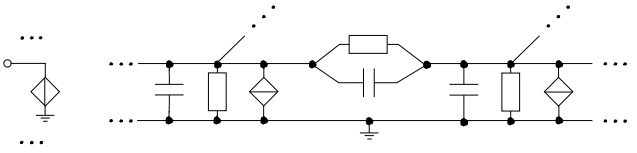

**Fig. 3.** MOR reduced IC conducted emission model.

## 4 Module-related IC conducted emission model

For a rough estimation of the power integrity behaviour where low simulation time takes priority over preciseness, the MOR modelling approach still leads to models that are too complex. For these applications a simplified IC conducted emission model with a very low number of elements is required. Such a model can be generated either by measurements or in a simulative approach and contains only one SLM for each functional module, i.e. the elements of the PDN and one current source (UTE 47A EMC Task Force, 2002) (Fig. 4). To meet the low complexity demands of the model, a curve fitting approach is used to obtain the R, L, C parameters of the PDN.

The fitting equation for an impedance $Z_{mn}$ defined as the voltage $V_m$ between the $V_{DD}$ and $V_{SS}$ Pins at module m divided by the input current $I_n$ at the $V_{DD}$ pin at module $n$ is

$$Z_{mn}(s) = \frac{V_m}{I_n} = a_{mn} + s \cdot b_{mn} + \frac{c_{mn}}{s} \tag{1}$$

where the coefficients $a_{mn}$, $b_{mn}$ and $c_{mn}$ are obtained from the simulation results of the of the EXPO model. The relation between the coefficients and the $R_{mn}$, $L_{mn}$, $C_{mn}$ parameters are as follows

$$\begin{aligned} R_{mn} &= a_{mn} \\ L_{mn} &= b_{mn} \\ C_{mn} &= c_{mn}^{-1} \end{aligned} \tag{2}$$

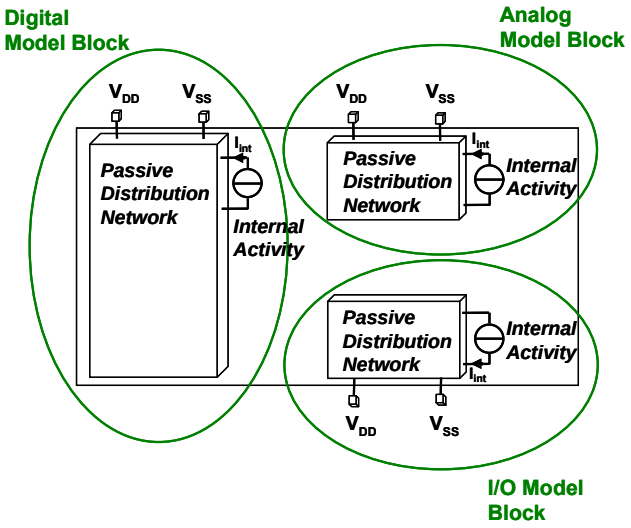


**Fig. 4.** Module-related model with one SLM (encircled) for each functional module.

For every module, $Z_{mn}$, m=n, is determined. The coefficients for $m \neq n$ are not considered, as coupling effects between modules are neglected for this low complexity approach.

For the determination of the internal activity of the SLMs, the external currents at the pins of the model are obtained through simulation. Following this, the external currents are converted into the frequency domain and multiplied with the transfer function of the previously determined PDN of the SLM, resulting in the internal current of the SLM of the model.

$$I_{\text{int}}(j\omega) = I_{\text{ext}}(j\omega) \cdot \left(1 - \omega^2 LC + j\omega RC\right) \tag{3}$$

## 5 Simulation results

For the analysis, the three proposed methodologies were applied to an IC conducted emission model describing two digital modules of a 32-Bit IC. The model consists of 12 SLMs with 120 elements and 51 nodes and is generated with the EXPO tool (Hesidenz and Steinecke, 2005). This model was reduced with the MOR approach to a model containing 64 elements and 14 nodes.

Since the netlist of the module-related model for rough power integrity estimation contains only 8 elements and 6 nodes, complexity is even further reduced with this approach compared to the MOR approach.

All three models were simulated in HSpice. Figure 5 shows the impedance curves $Z_{11}$ of one digital module for all three models. The $Z_{11}$ curve of the MOR model as well as the curve of the module-related model show very good matching with the curve of the model generated with the EXPO Tool.

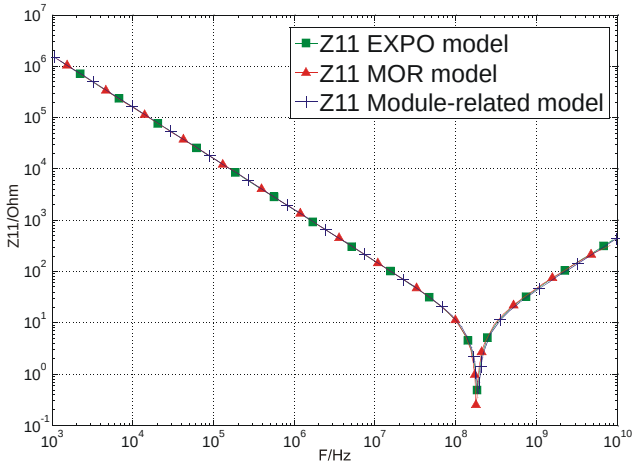


**Fig. 5.** Impedance curves $Z_{11}$ of the EXPO model, MOR model, and module-related model.

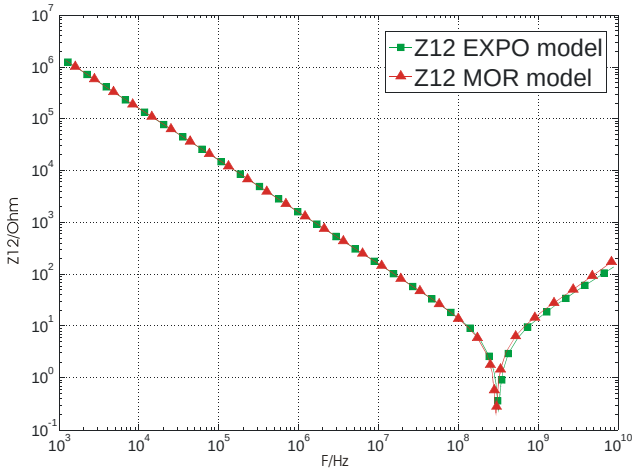


**Fig. 6.** Impedance curves $Z_{12}$ of the EXPO model and MOR model.

For the $Z_{12}$ parameter, describing the coupling between the two modules, Fig. 6 depicts good correlation between the EXPO model and the MOR model. A $Z_{12}$ curve is not provided for the module-related model, as coupling effects between modules can not be considered for this type of model.

Figure 7 shows the transient response of the supply voltage $V_{DD1,\text{ref}}$=1.5 V for the three models at the $V_{DD1}$-Pin of the first digital module.

Again, the MOR model as well as the module-related model show a very good matching with the EXPO model.

The main properties of the three models are summarised in Table 1. The simulation time is reduced significantly for the MOR and the module-related approach.

For the module-related model in this work, two digital modules of the complex EXPO model were reduced to one SLM for each module. Since the SLM possesses only two pins, the model is merely suitable for module-related

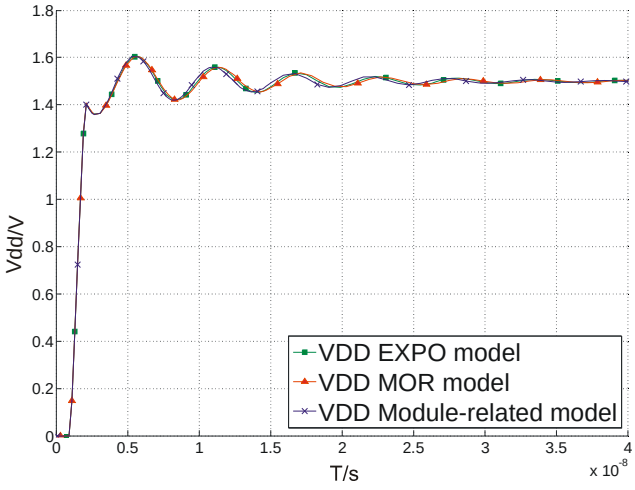


**Fig. 7.** Transient response of the EXPO model, MOR model, and module-related model.

**Table 1.** Complexity of the EXPO model, MOR model and module-related model.

| | EXPO | MOR | Module-related |
|---|---|---|---|
| | Model complexity | | |
| El. compon. | 110 | 64 | 8 |
| nodes | 51 | 14 | 6 |
| | HSpice simulation time | | |
| AC-Analysis | 100% | 42% | 19% |
| Transient | 100% | 74% | 13% |
| | Accuracy | | |
| | – Pin-related | – Pin-related | – Module-related |
| | – Crosstalk considered | – Crosstalk considered | – Crosstalk not considered |

estimation of conducted emission, whereas for the EXPO and the MOR model, having all IC pins modelled, pin-related estimation of emission is possible.

## 6 Conclusion

This paper proposes two methodologies to reduce the complexity of large IC conducted emission models. The first methodology uses MOR algorithms, while the second method uses a fitting algorithm to obtain the parameters of a minimum complexity module-related model from simulation results of the complex model.

While it is possible to make a point about the disturbances at the IC pins with both modelling approaches, only the MOR model provides conclusive information about pin-coupling effects. This information is lost for the module-related model.

The MOR and module-related model were compared with the EXPO model and close alignments were observed in the time and frequency domain. A significant speed-up in simulation time was achieved for the MOR model in comparison to the EXPO model, and even more so for the module-related model.

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