Evaluation of Metal-Organic Frameworks in Electronic Devices for Gas Sensing

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To my family Basilio Montañez, Rufina Huamán, Kevin, Geraldine, Nancy and Edith

Kurzfassung

Die Integration von nanoporösen Metall-organischen Gerüstverbindungen (engl. metal-organic frameworks, MOFs) in elektronischen Bauelementen wie z.B. Kondensatoren, Transistoren und Memristoren, ermöglicht durch Adsorption von Gastmolekülen eine Anwendung in der Sensorik. Dünne MOF-Schichten in einem Metall-Isolator-Halbleiter (engl. metal-insulator-semiconductor, MIS) als Kondensatorenstruktur erlauben auf Grund niedriger Spannungen konkrete Anwendungen. MIS-Kondensatoren bieten auch eine Analyse der Grenzflächendefekte wie z.B. Grenzflächenzuständen (interface traps) und Ladungen nahe der Grenzfläche (border traps). Elektronische Bauteile erfordern eine geringe Konzentration von Grenzflächendefekten, um so Schwellwertinstabilitäten zu verkleinern. Diese Arbeit liefert eine detaillierte Untersuchung von Ladungen und Defekten in MOF-basierten MIS-Kondensatoren durch Impedanzspektroskopie. Der MOF $Cu_3(BTC)_2$ wurde direkt auf einer Si- und auf einer SiO_2-Oberfläche durch Layer-by-layer-Methoden aufgebracht. Die Schichtdicke konnte durch die Variation der Sprüh- bzw. Tauchzyklen leicht eingestellt werden. Des Weiteren wurden $Si/SiO_2/Al$-MIS-Kondensatoren zum Vergleich untersucht. Das erfolgreiche Wachstum von ultra-dünnen $Cu_3(BTC)_2$-Schichten auf Si-Substraten wurde durch Experimente mit Röntgenbeugung (engl. X-ray diffraction, XRD) verifiziert. Die Funktion von MOFs in MIS-Kondensatoren wurde mit Kapazitäts-Spannungs (C-V) und Leitfähigkeits-Spannungs (G-V) Messungen bei verschiedenen Frequenzen und Temperaturen untersucht.

Die Ergebnisse belegen positive und negative feste Ladungen in den dielektrischen $Cu_3(BTC)_2$-Schichten, wie auch das Vorhandensein von Ladungen an/in der Grenzschicht, die eine Hysterese in den C-V-Messungen verursachen. Hinweise auf Grenzflächenzustände können durch einen Peak in der G-V-Messung beobachtet werden. Die Analyse der Daten beweist, dass MOF-Schichten - hergestellt ohne Ultraschall (US) - eine relativ geringe Dichte von Ladungen an der Grenzschicht ($\sim 10^{11} cm^{-2}$) und geringe Grenzflächenzustände ($\sim 10^{11} eV^{-1} cm^{-2}$) bei einer Ansprechzeit von wenigen µs besitzen. Temperaturabhängige Messungen zeigten eine Degradation der elektrischen Eigenschaften von MOFs. Durch zusätzliche US-Behandlungen während der Beschichtung verringerte sich die ohnehin geringe Dichte von Ladungen nahe der Grenzschicht deutlich, die der Grenzflächenzustände blieb unverändert. Außerdem sind die Schichten thermisch stabiler und erreichen bei Abkühlung nahezu ihren Anfangszustand. Die experimentellen Ergebnisse belegen, dass MOF-basierte Kondensatoren eine Grenzflächenqualität vergleichbar mit anorganischen Materialien besitzen und sie für Anwendungen in der Sensorik nutzbar sind.

Abstract

Integrating nano-porous metal-organic frameworks (MOFs) in electronic devices such as capacitors, transistor or memristor enables sensing applications for a wide variety of guest molecules. Particularly, the incorporation of thin MOF films in metal-insulator-semiconductor (MIS) capacitor structures allows real-life applications because of its low voltage operation. Additionally, MIS capacitors offer a thorough study of interfacial defects such as interface traps and border traps distributed within the device. In electronic devices, a low concentration of interfacial defects is required to avoid threshold-voltage instabilities. This fact guarantees good stability and performance of electrical devices. This research work provides detailed investigation about charges and defects in MOFs-based MIS capacitors by impedance spectroscopy. $Cu_3(BTC)_2$ was coated directly on silicon, and on thermally grown silicon dioxide surfaces in a layer-by-layer fashion. The layer thickness was easily handled by varying the number of spray cycles in the coating process. In addition, $Si/SiO_2/Al$ MIS capacitors were investigated for comparison reasons. The successful growth of ultra-thin $Cu_3(BTC)_2$ films on silicon substrates was verified via X-ray diffraction (XRD) experiments. The function of MOFs within MIS capacitors was investigated via capacitance-voltage (C-V) and conductance-voltage (G-V) characteristics measured at different frequencies and temperatures.

The results show evidence of positive and negative fixed charges in the $Cu_3(BTC)_2$ dielectric layer as well as of the presence of border traps which cause hysteresis in the C-V characteristics. Evidence of interface traps is directly observed by the peak on the conductance curve. Analysis of the data demonstrates that ultra-thin $Cu_3(BTC)_2$ films prepared without ultrasonication exhibit a relatively low density of border traps ($\sim 10^{11} cm^{-2}$), interface traps ($\sim 10^{11} eV^{-1} cm^{-2}$) and time response in the order of µs. Temperature-dependent measurements degrade the electrical quality of the MOFs. The addition of ultrasonication steps on the coating process decreases considerably the density of border traps. Additionally, the layers are more stable under heating experiments, and after cooling they almost recover the initial state. The experimental results show that MOF-based capacitors exhibit interface quality comparable to inorganic materials, making them suitable for sensing applications.

Keywords: interfacial defects, metal-insulator-semiconductor capacitor, $Cu_3(BTC)_2$ metal-organic framework

Schlagwörter: Grenzflächendefekte, Metall-Isolator-Halbleiter-Kondensator, $Cu_3(BTC)_2$ Metall-organische Gerüstverbindung

Contents

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Abbreviations

AFM	atomic force microscopy
APTES	aminopropyltriethoxysilane
BDC	1,4-benzenedicarboxylate acid
BET	Brunauer-Emmett-Teller
BTC	1,3,5 benzenetricarboxylate acid
CV	capacitance-voltage
ESR	electron spin resonance
FET	field-effect transistor
FG	forming gas annealing
GV	conductance-voltage
HFCV	high-frequency capacitance-voltage
OFET	organic field-effect transistors
FWHM	full width at half maximum
HID	hydrogen induced drift
HKUST-1	Hong Kong University of Science and Technology
IRMOF	isoreticular metal framework
LBL	layer-by-layer
LFCV	low-frequency capacitance-voltage
MIL	Materials of Institute Lavoisier
MIS	metal-insulator-semiconductor
MOF	metal-organic framework
NA	non-annealed sample
NDC	1,4-naphthalenedicarboxylate acid
RTP	rapid thermal annealing processing
SAM	self-assembly monolayer
SURMOF	surface-mounted metal-organic framework
TMA	trimesic acid
UiO	University of Oslo
XRD	X-ray diffraction
ZIF	zeolitic imidazolate framework

Notation

A	area of the metal contact, cm^2
C	capacitance, F/cm^2
C_A	accumulation capacitance, F/cm^2
C_c	corrected capacitance, F/cm^2
C_d	dielectric capacitance, F/cm^2
C_F	capacitance in forward direction, F/cm^2
C_{HF}	high-frequency capacitance, F/cm^2
C_{it}	interface trap capacitance, F/cm^2
C_{LF}	low-frequency capacitance, F/cm^2
C_m	measured capacitance, F/cm^2
C_{ma}	measured capacitance in accumulation, F/cm^2
C_R	capacitance in reverse direction, F/cm^2
C_s	semiconductor capacitance, F/cm^2
C_{tot}	total capacitance, F/cm^2
D_{it}	density of interface traps, $eV^{-1}cm^{-2}$
E	trivalent silicon centers located at the Si/SiO_2 interface
E'	center in SiO_2 associated with oxygen vacancies
E_c	energy of conduction band-edge, eV
E_g	energy band gap, eV
E_i	intrinsic level
E_v	energy of valence band-edge, eV
f	signal frequency, Hz
G	conductance, S/cm^2
G_c	corrected conductance, S/cm^2
G_{cp}	Equivalent parallel conductance, S/cm^2
G_m	measured conductance, S/cm^2
G_{ma}	measured conductance in accumulation, S/cm^2
k	Boltzmann's constant, 1.3805×10^{-23} J/K
L_D	extrinsic Debye length, m
N_A	acceptor concentration in silicon, cm^{-3}
N_{bt}	density of border traps, cm^{-2}
n_i	intrinsic carrier concentration in silicon, cm^{-3}
q	elementary charge, 1.6021×10^{-19} C
Q_{bt}	border-trapped charges, cm^{-2}
Q_{fix}	fixed charges, cm^{-2}
Q_{in}	charges in inversion layer, Ccm^{-2}
Q_{it}	Interface-trapped charges, cm^{-2}
Q_m	charges in the metal, Ccm^{-2}

Q_{mob}	mobile charges, cm^{-2}
$Q_{\mathrm{ox,eff}}$	effective oxide charges, cm^{-3}
Q_{ot}	oxide-trapped charges, cm^{-2}
Q_{s}	total charges in the semiconductor, Ccm^{-2}
Q_{sc}	space charge density
R_{s}	series resistance, Ω
V_{FB}	flat-band voltage, V
$V_{\mathrm{FB,\ exp}}$	experimental flat-band voltage, V
$V_{\mathrm{FB,\ theor}}$	theoretical flat-band voltage, V
V_{g}	gate voltage, V
w	angular frequency, s
W_{m}	surface depletion region, cm
Y_{it}	admittance of interface traps
Y_{ma}	admittance in accumulation
Z_{ma}	impedance in accumulation

ε	permittivity of vacuum, 8.8542×10^{-12} F/m
ε_{d}	permittivity of the dielectric material
ξ_s	electric field, V/cm
χ	electron affinity, V
χ'	effective electron affinity, V
Φ_{F}	Fermi potential, V
Φ_{m}	work function of the metal, eV
Φ'_{m}	effective work function of the metal, V
Φ_{s}	work function of the semiconductor, V
Φ_{t}	surface potential, V
τ_{it}	response of interface traps, s
ψ_{s}	band bending, V

1 Introduction

1.1 Metal-Organic Frameworks in Electronic Devices

Metal-organic frameworks are porous hybrid materials composed of metal nodes that are connected by organic linker molecules. They exhibit extraordinary properties such as porosity, large surface area, and tailorable chemistry that can be tuned by adapting the functionality of its components. Because of these properties, MOFs are suitable for a wide variety of applications including gas storage [1], separation [2], sensing [3], catalysis [4], and drug delivery [5]. In the last years, the integration of MOFs as an integral component of electronic devices has received extensive attention [6,7]. The microelectronic industry requires the production of homogeneous thin films directly on substrates with controllable thickness, composition, and microstructure [6]. In order to attach thin MOF films on substrates, the deposition protocol of the conventional solvothermal process was modified [8], and new deposition techniques were developed [9,10]. Hermes *et al.* used the solvothermal synthesis to growth $Zn_4O(BDC)_3$ with BDC=1,4-benzenedicarboxylate on Au(111) substrates functionalized by COOH-terminated self-assembly monolayer (SAM). $Zn_4O(BDC)_3$ was grown with a layer thickness of ~5 µm and crystallites sizes between 100 nm to 500 nm [8]. By controlled layer-by-layer (LBL) synthesis, resulting in surface-mounted MOFs also referred to as SURMOFs, the layer thickness was considerably reduced to the nanometer scale [11]. Later, the chemical vapor deposition approach has emerged as a promising solvent-free synthesis which consists of two steps: first, the metal oxide is deposited on the substrate and then the substrate is exposed to a vapor-solid reaction [10].

Although significant progress has been made on the growth of thin MOF films on substrates, only a few reports address the integration of MOFs in electronic devices. For example, it was shown that ZIF-8 with ZIF=zeolitic imidazolate framework exhibits good adhesion to the support, elastic modulus higher than 36 GPa and low dielectric constant of 2.33(±0.05) at 100 kHz, therefore, this MOF is a promising candidate to separated copper interconnects on microelectronic chips [12]. The assembly of semiconducting or insulating MOFs in organic field-effect transistors (OFET) also has been investigated. Wu *et al.* fabricated the first microporous field-effect transistor using Ni_3(2,3,6,7,10,11-hexaiminotriphenylene)$_2$ as the active channel material. The semiconducting MOF exhibits high hole mobility (~48.6 $cm^2V^{-1}s^{-1}$) owing to its full charge delocalization [13]. Gu *et al.* coated $Cu_3(BTC)_2$ with BTC=1,3,5 benzenetricarboxylate on silicon dioxide surfaces in order to improve the performance of the OFET by modifying the SiO_2 dielectric layer. Incorporation of $Cu_3(BTC)_2$ in SiO_2-based transistors improves the hole mobility and decrease the threshold voltage to values lower than 10 V [14]. The present research work reported the feasible integration of ultra-thin $Cu_3(BTC)_2$ films within MIS capacitor structures and demonstrated that the MOF layer exhibits an interface quality comparable to inorganic materials [15,16].

1.2 Metal-Insulator-Semiconductor Capacitors as Sensors

Sensors compatible with integrated circuits technology consist of MIS structures such as MIS capacitor or transistor. Gas sensitivity of these devices is measured as the change in the work function of the metal gate when a dipolar layer is formed at the metal/insulator interface [17,18]. Sensitivity of the devices under exposure to hydrogen gas consists of three steps: (1) dissociation of hydrogen molecules on the catalytic metal surface, (2) then hydrogen atoms diffuse toward the metal/insulator interface, and (3) the adsorbed hydrogen atoms are polarized giving rise a dipole layer that shifts the flat-band voltage (V_{FB}) of the devices [17]. Lundström *et al.* demonstrated the potential of $Si/SiO_2/Pd$ transistors as a leak detector and gas alarm sensor [19]. Sensing experiments were performed at 150 °C to speed up the time response of the device. They show that the sensor detects hydrogen in air and the sensitivity increases under nitrogen atmosphere and even more under argon atmosphere. Under oxygen or nitrogen atmospheres chemical reactions take place on the metal surface leading a reduction of available hydrogen atoms. In an inert atmosphere, only dissociation/association of hydrogen occurs, therefore, the sensitivity is higher.

Nylander *et al.* investigated the flat-band voltage shift of $Si/SiO_2/Pd$ capacitors upon exposure of hydrogen. They found that the V_{FB} shift occurs not only due to change in work function of the metal but also due to hydrogen-induced drift (HID). HID is only related to the silicon dioxide layer but takes place close to the SiO_2/Pd interface and it is associated with the presence of SiO^-Na^+ that acts as weak binding sites for protons via ion-dipole interaction [20]. HID effects were improved by the incorporation of thin oxidized layers such as alumina, tantalum pentoxide, and silicon nitride between the SiO_2 and Pd. Improvement of HID is associated with the structure that the metal adopts on the top of different insulating materials [21]. On the other hand, Dwivedi *et al.* found that after dissociation of hydrogen on the catalytic metal, some of them can tunnel the insulator layer and reach the SiO_2/Si interface [22]. At the interface, hydrogen atoms react with interface traps leading to the formation of hydrogen-induced interface traps, thus affecting seriously the electrical characteristics of the sensor [23]. The layer thickness of the insulator material also influences the sensitivity of the devices because interface trap density increases for thicker layers. Aval *et al.* found this dependence in $Si/SiO_2/Ni$ capacitors with an oxide layer thickness between 28 nm to 53 nm [24]. Increase in layer thickness leads to an increment of interface trap density from $4.4\times10^-$

^{10} Ccm^{-2} (28 nm) to 6.9×10^{-10} Ccm^{-2} (53 nm) thus the response speed and recovery time of the devices decreases. A response of 87.5 % was achieved for the thinnest oxide layer. In addition to SiO_2, many oxide layers have been investigated for hydrogen sensing application [25]. For instance, it was demonstrated that $Si/TiO_2/Pd$ sensors detect hydrogen at room temperature in ambient or hydrogen atmospheres. The sensitivity depends on the deposition method of the insulator material. TiO_2 prepared by electron beam evaporation shows higher sensitivity of 84 % in ambient air and 90 % in nitrogen atmosphere [26].

1.3 Motivation and Structure of the Thesis

MOFs are potential candidates for electronic applications because of its tunable chemistry, porosity, and high surface area. The first applications of MOFs in transistors were reported in 2017 by Wu *et al*. [13] and Gu *et al*. [14]. However, little is known about the interface quality of the devices which can lead to threshold voltage instabilities and thus the performance of the devices can be degraded. Therefore, the aim of this thesis is the integration of metal-organic frameworks within metal-insulator-semiconductor capacitors and the investigation of interfacial properties by impedance spectroscopy. Generally, a large number of MOFs with good sensing characteristics and insulating properties are available [27]. In particular, $Cu_3(BTC)_2$ also known as HKUST-1 (Hong Kong University of Science and Technology) [28], exhibits excellent chemical and physical properties such as porosity, large surface area, large optical bandgap of 3.6 eV [29] and stable crystalline structure under post-annealing treatments [30]. Besides, it was demonstrated that $Cu_3(BTC)_2$ can be grown on silicon dioxide surfaces with low surface roughness and high crystalline quality [29,31]. Nevertheless, $Cu_3(BTC)_2$ possess a low dielectric constant. The theoretical k value is equal to 1.7 while the experimental one after deposition is ~2.3 [30].

Conventional metal-oxide-semiconductors capacitors were fabricated using $Cu_3(BTC)_2$ MOF as insulating material. Thin $Cu_3(BTC)_2$ films were prepared in a layer-by-layer fashion directly on silicon wafers and on silicon dioxide surfaces. Interfacial properties and charge transport mechanisms of the devices were evaluated through capacitance and conductance characteristics measured at different voltages and frequencies. The major benefit in comparison to the already reported MOF-based-FET electronic devices, which require relatively high voltages, is that the MOF-MIS-device can be operated with less than 10 V. The low-voltage-operation and thus the low-energy-consumption could enable real-life applications.

This research work was developed in cooperation between the Laboratorium für Nano- und Quantenengineering (LNQE) of the Leibniz University (LUH) and the Institut für Materialien und Bauelemente der Elektronik (MBE). Deposition of ultra-thin $Cu_3(BTC)_2$ films were done at the Institut für Physikalische Chemie und Elektrochemie (LUH) and at the Institut für

Funktionelle Grenzflächen (IFG) in Karlsruhe. The thesis is divided into eight sections. Chapter 2 provides a theoretical background about the physics and work principles of metal-insulator-semiconductor capacitors with an emphasis on the different charges that can be present in the devices, and the growth of thin films of metal-organic frameworks on substrates. In chapter 3, the fabrication of the capacitors and analytical techniques will be described. Chapter 4 summarizes the different methods used for the determination of interfacial properties of MIS capacitors from impedance measurements such as the conductance method and the Hill-Coleman approximation. Chapter 5 discusses the effect of trimesic acid (TMA) and forming gas (FG) annealing on SiO_2-based MIS capacitors. After that, the results of $Cu_3(BTC)_2$-based MIS capacitor will be presented. First, the analysis of samples prepared by the spray-method (Chapter 6) and then the samples prepared by the layer-by-layer approach assisted by ultrasonication (Chapter 7). Finally, conclusion and outlook are presented in Chapter 8.

2 Basics

The metal-insulator-semiconductor capacitor is formed by a dielectric material deposited or grown on top of a semiconductor wafer and followed by a metal electrode that serves as a voltage source. The MIS capacitor is the basic building block for several integrated devices such as transistors [32–34]. Additionally, they offer detailed information about the electrical quality of the semiconductor/insulator interface. The reliability of MIS structures is affected by charges, also known as defects, generated during the manufacture of the device. Five types of charges can be found in an MIS device: mobile ionic charges (Q_{mob}), oxide-trapped charges (Q_{ot}), fixed charges (Q_{fix}), interface-trapped charges (Q_{it}), and border-trapped charges (Q_{bt}) [35,36]. These charges are distributed within the insulator layer and at the insulator/semiconductor interface. Particularly, Q_{it} and Q_{bt} are located in traps which have energy levels within the silicon bandgap [37]. High amount of charges and traps leads to voltage threshold instabilities degrading the performance of the capacitors. Therefore, understanding the nature of defects is of great importance in order to improve the performance of the devices. The following section comprises the basics of MIS structures with an emphasis on the effect of charges on capacitance-voltage characteristics of the Si-SiO_2-Al system.

Metal-organic frameworks, a new class of porous materials composed of metal clusters and organic linkers have been used in a wide variety of applications because of its extraordinary properties such as high surface area, porosity, and tunable functionality [38]. In the last years, several efforts were made to integrate MOFs into electronic devices [13,14]. For instance, many methods were developed in order to attach MOFs on various substrates [9,39]. The present section will present the potential of MOFs in microelectronics with special attention on the properties of $Cu_3(BTC)_2$ MOF and deposition techniques that deliver thin film MOFs.

2.1 Metal-Insulator-Semiconductor (MIS) Capacitor

Figure 2.1 depicts a cross-section illustration of a metal-insulator-semiconductor capacitor consisting of a semiconductor, an insulating material, and a metal gate. The MIS structure is the simplest device for the study of semiconductor surfaces because it has only two terminals: the gate electrode and the silicon substrate that has to be connected by an Ohmic contact [34]. The most important and widely studied system is composed of Si-SiO_2-Al. In this system, the insulator layer is formed by thermal oxidation process leading defects distributed within the insulator material and at the Si/SiO_2 interface. The density of defects depends on the oxidation conditions such as atmosphere, temperature, and cooling. Additionally, they depend strongly on the characteristics of the wafer such as orientation, resistance, and doping concentration.

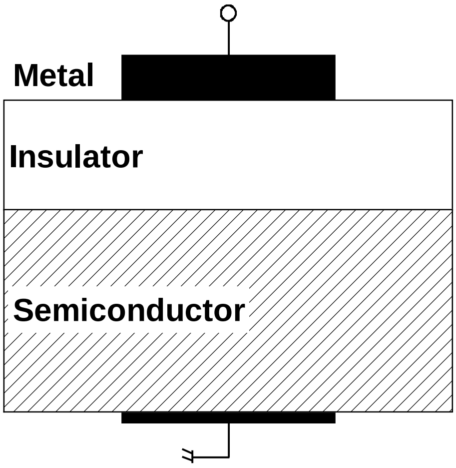


Figure 2.1 Cross-section illustration of a metal-insulator-semiconductor capacitor consisting of two electrodes (the metal gate and the silicon) separated by an insulator.

Defects near and at the Si/SiO_2 interface

Interfacial defects have been extensively investigated and characterized by their spin concentrations and spectroscopic g values obtained by electron spin resonance (ESR) [40–43]. Defects also termed as centers in the Si/SiO_2 system are classified into two groups: (1) *E* center or trivalent silicon center located at the Si/SiO_2 interface. They consist of silicon-bonded to three other silicon atoms $\cdot Si{\equiv}Si_3$ and (2) *E*' center or trivalent silicon center located in SiO_2 but close to the Si/SiO_2 interface. These defects consist of silicon-bonded to three oxygen atoms $\cdot Si{\equiv}O_3$ [40,42]. *E* centers were detected first by Nishi [44] on Si(111) substrates and they were classified as P_A(g=~2.000), P_B(g=~2.000 to ~2.010) and P_C

(g=~2.06 to ~2.07) paramagnetic centers. The centers were associated with the growth of SiO_2 layer in dry atmosphere and the heating/cooling process from room temperature to elevated process temperature and return. P_A and P_C centers were associated with trapped electrons in the oxide, while P_B center to trivalent Si centers in the broken Si-O network, respectively. Later Caplan and Pointdexter termed the *E* centers as P_b center and found a good correlation between the spin concentration of P_b centers and density of interface traps measured at the midgap position [40]. On the other hand, they associate the *E*' center to oxygen vacancies with unpaired silicon spin ($O_3{\equiv}Si\bullet$) and striped positively charges ($^+Si{\equiv}O_3$). On Si(100) substrates, 2 sub-groups of P_b center were found P_{b0} ($\bullet Si{\equiv}Si_3$) and P_{b1} ($\bullet Si{\equiv}SiO_2$) as is shown in Figure 2.2 [45].

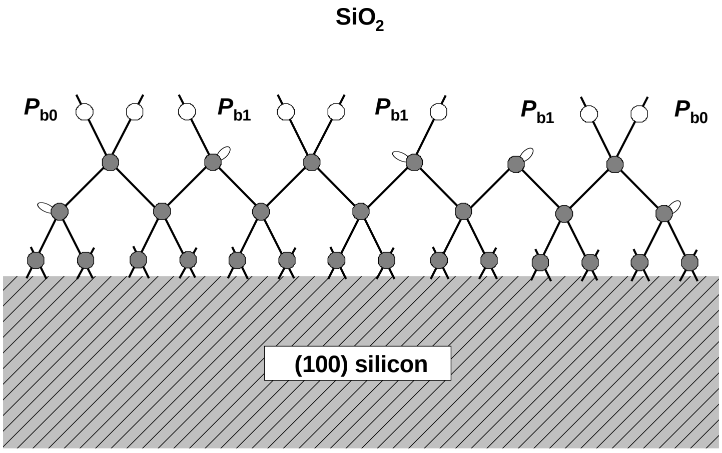


Figure 2.2 Structure and location of P_{b0} and P_{b1} centers generated in oxidized (100) silicon wafers based on electron spin resonance anisotropy. P_{b0} center is assigned to $\cdot Si{\equiv}Si_3$ back-bonded in the silicon surface while P_{b1} is associated with $\cdot Si{\equiv}SiO_2$ [45].

Defects at the Si/SiO_2 system capacitors can be quantified by several techniques such as impedance, deep-level transient spectroscopy, electron spin resonance, photocurrent-voltage, and others. The present research work will be focused on impedance spectroscopy which provides information of both, capacitance and conductance characteristics. Capacitance measures the change of charges in the capacitor produced due to the change of voltage. Conductance measures the energy loss due to change in occupancy of traps.

2.1.1 Ideal MIS Capacitor

The following part will address the ideal MIS capacitors, a perfect device without defects. The ideal MIS capacitor is a very simple system that facilitates the understanding of the structure and physics of the device. It is defined assuming the following suppositions [32,46,47]:

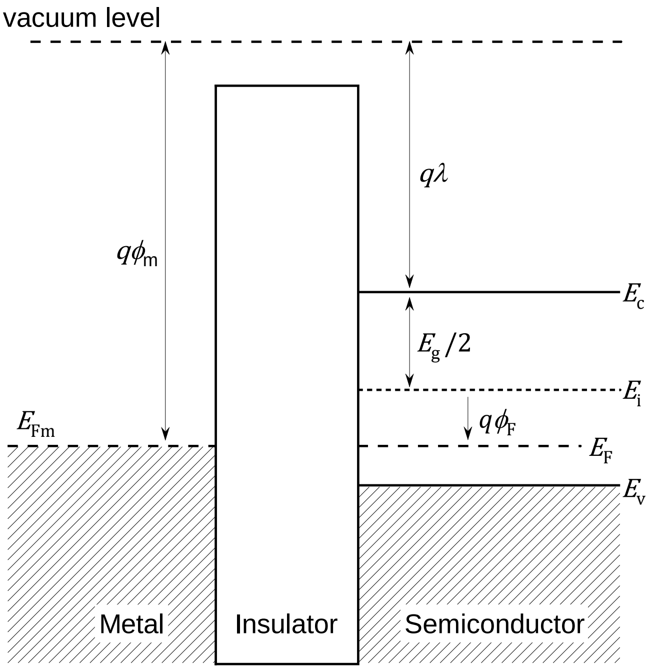


Figure 2.3 Energy-band diagram for an ideal MIS capacitor on p-type Si substrate. At zero voltage (V_g=0) the bands of the semiconductor are flat (flat-band condition) [46].

i) At thermal equilibrium conditions, the work function difference between the metal and the semiconductor is zero (Φ_{ms}=0 at V_g=0 V):

$$\Phi_{ms} = \Phi_m - \left(\chi + \frac{E_g}{2q} + \Phi_F\right) = 0 \qquad \text{for } p\text{-type Si} \tag{2.1}$$

where Φ_m and Φ_s, are the work function of the metal and the semiconductor, χ is the electron affinity, E_g is the energy bandgap, q is the elementary charge and Φ_F is the Fermi potential.

ii) There are no charges in the insulator layer as well as at the insulator/semiconductor interface (Q_{mob}=0, Q_{ot}=0, Q_{fix}=0, Q_{it}=0, Q_{bt}=0). The only charges that exist are located in the semiconductor (Q_s) in equal amount but with opposite sign that in the metal (Q_m), where $\pm Q_m = \mp Q_s$.

iii) The dielectric material is a perfect insulator (carrier transport under DC bias from the metal to the semiconductor is not allowed).

Energy-band diagram for the ideal MIS capacitor is shown in Figure 2.3. The insulator material has a large bandgap in comparison to the semiconductor, ~8.8 eV for SiO_2 and ~1.12 eV for silicon. Thus the flow of free carriers from the metal to the gate is prevented. Under no biasing conditions (V_g=0 V), the bands in the semiconductor are flat and the Fermi level of the semiconductor coincide with the Fermi level of the metal. This condition is known as the Flat-band condition. When voltage is applied through the metal gate, an electric field is established in the insulating layer and three situations can happen:

a) Accumulation

When the capacitor is biased with a negative voltage (V<0), the bands in the semiconductor bend upward (see Figure 2.4a). Note that bending occurs only at the semiconductor surface. Band-bending leads an exponential increase of majority carrier (holes) density near the SiO_2/Si interface that compensates the negative potential in the metal gate. The charge distribution of the semiconductor is equal to the metal, $\pm Q_m = \mp Q_s$.

b) Depletion

When the capacitor is biased with a small positive voltage (V>0), the bands in the semiconductor bend downward (see Figure 2.4b) and the majority carrier are depleted from the surface. In this case, the charge distribution of the semiconductor is known as space charge per unit area (Q_{sc}) and is proportional to the width of the surface depletion region (W_m) and the acceptor impurity (N_A), $Q_s = Q_{sc} = -qN_AW_m$.

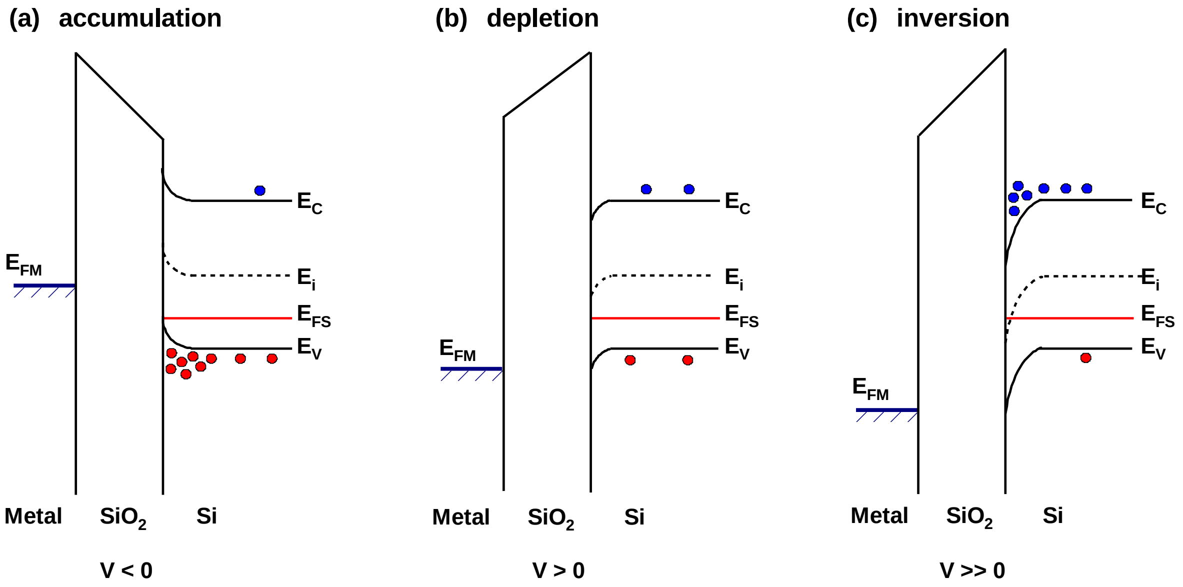


Figure 2.4 Energy-band diagram for an ideal *p*-Si/SiO_2/Al MIS capacitor under bias condition showing the accumulation (a), depletion (b) and inversion (c) cases. Upon bias condition, the bands in the semiconductors bend upward/downward and accumulation of holes/electrons occurs depending on the polarity of the applied voltage. Note that accumulation of carrier occurs only at the semiconductor surface [32].

c) Inversion

Once the negative voltage increases the bands in the semiconductor continue bending until the intrinsic level reach the Fermi level. This position is known as the midgap condition. When the capacitor is biased with a larger positive voltage (V>>0), the bands in the semiconductor bend downward even more that minority carrier is pushed out from the surface and the minority carrier (electrons) accumulates at the surface (see Figure 2.4c). In this case, the electron concentration is larger than the hole concentration, thus the surface behaves like an *n*-type Si semiconductor. This is known as the inversion region. The charge distribution of the semiconductor is the contribution of the space charge per unit area and the charge in the inversion layer $Q_s=Q_{in}+Q_{sc}$.

In the ideal case, the total charge in the semiconductor per unit area in the semiconductor is defined by the following equation [46]:

$$Q_s = -\epsilon_s \xi_s = \mp\sqrt{2}\,\frac{\varepsilon_s \Phi_t}{L_D}\,\mathrm{F}(\psi_s, N_A) \tag{2.2}$$

where Q_s is the total charge per unit area in the semiconductor, ε_s is the permittivity of the semiconductor, ξ_s is the electric field, Φ_t is surface potential, ψ_s is the band bending, and N_A acceptor concentration.

The differential capacitance of the semiconductor is proportional to the charge distribution and is defined by the following equation [46]:

$$C_s \equiv \frac{\partial Q_s}{\partial \psi_s} - \xi_s = \frac{\epsilon_s}{\sqrt{2}L_D}\,\frac{\left|1 - \mathrm{e}^{-\psi_s/\Phi_t} + \left(\frac{n_i}{N_A}\right)^2 (\mathrm{e}^{\psi_s/\Phi_t} - 1)\right|}{\mathrm{F}(\psi_s, N_A)} \tag{2.3}$$

where C_s is the differential capacitance, L_D is the extrinsic Debye length, and n_i is the intrinsic carrier concentration.

The total capacitance (C_{tot}) of the MIS system is a series combination of the dielectric capacitance (C_d) and the semiconductor capacitance (C_s) given by:

$$C_{tot} \equiv \frac{C_d C_s}{C_d + C_s} \quad , \quad C_d \equiv \frac{\varepsilon_d}{d} \tag{2.4}$$

where C_d and C_s are the dielectric and semiconductor capacitance, respectively. ε_d and d are the permittivity and thickness of the dielectric layer, respectively. In strong accumulation, the capacitance is equal to the dielectric capacitance, C_d.

High-frequency capacitance-voltage (HF-CV) curves measured from accumulation to inversion (acc-inv, solid curve) and back from inversion to accumulation (inv-acc, dashed curve) directions for an ideal *p*-Si/SiO$_2$/Al MIS capacitor are shown in Figure 2.5. The *C-V* curve exhibits the characteristic accumulation, depletion, and inversion regimes described above. When the DC sweep is high the inversion layer is not reached and then the deep depletion regime appears. At high frequencies (*f* >~100 kHz), minority carrier cannot follow the alternating current and, therefore, the capacitance in inversion does not increase. In the ideal case, the flat-band voltage (V_{FB}) is located at 0 V and the accumulation region is reached by applying a negative voltage to the metal gate. Furthermore, C-$V_{acc\text{-}inv}$ and C-$V_{inv\text{-}acc}$ curves are identical.

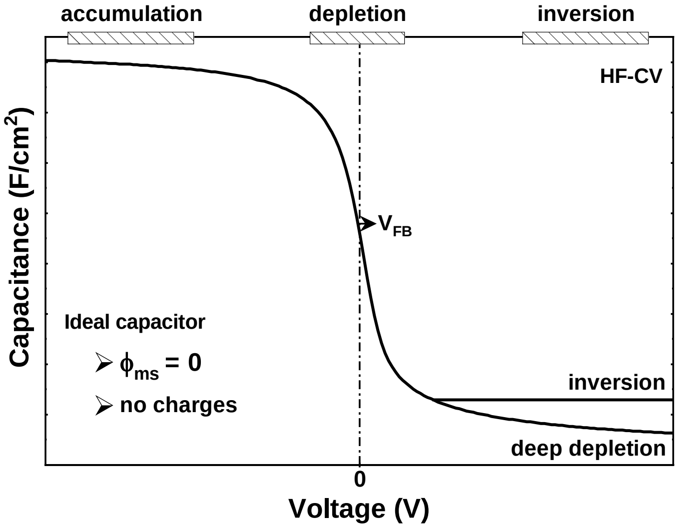


Figure 2.5 High-frequency capacitance-voltage curves for an ideal Si/SiO$_2$/Al MIS capacitor on *p*-type Si substrate. In the ideal case, the *C-V* curves in forward and reverse mode are equal and, therefore, no hysteresis is observed. In addition, the flat-band voltage is located at 0 V. The dashed areas represent the accumulation, depletion, and inversion regimes.

2.1.2 Real MIS Capacitor

The assumptions made for the ideal capacitor are invalid for the real case. In a real *p*-Si/SiO$_2$ system, the Φ_{ms} difference depends on the work function of the metal and the doping concentration of the substrate. The capacitor exhibits also charges and traps centers generated during the manufacture of the devices.

a) Effect of ϕ_{ms} in the C-V Curve

In the real case, the work function of the metal is different from that of the semiconductor, $\Phi_{ms} \neq 0$. Thus, in contrast to the ideal case ($V_{FB}=0$), the flat-band voltage is equal to the Φ_{ms} difference. V_{FB} due to Φ_{ms} difference is not influenced by charges, therefore, it will be considered as the theoretical flat-band, $V_{FB,theor}$. For a real MIS capacitor $V_{FB,theor}$ can be determined using the Equation (2.5). The effect of $\Delta\Phi_{ms}$ on capacitance measurements is shown in Figure 2.6. Note that $\Delta\Phi_{ms}$ produces only a parallel shift of the whole *C-V* curve toward the negative voltage axis.

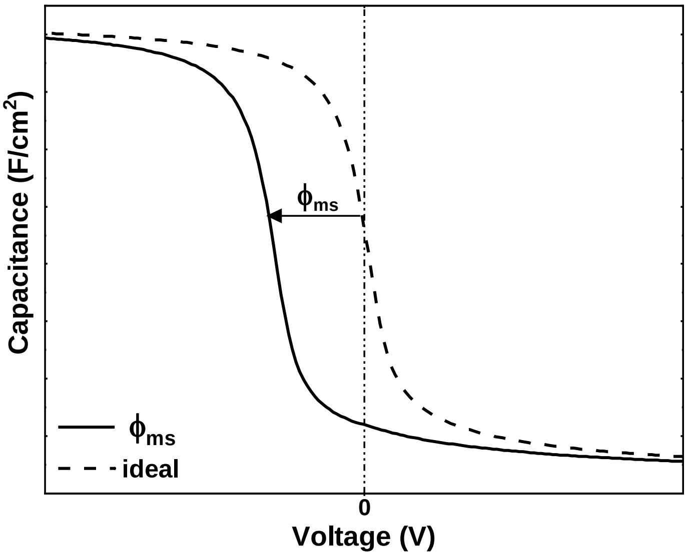


Figure 2.6 Capacitance-voltage curve for p-Si/SiO$_2$/Al MIS structure for the ideal case (black curve) and including the effect of work function difference between the metal and the semiconductor (red and purple curves). $\Delta\Phi_{ms}$ induces a parallel shift of the whole capacitance curve.

$$\Phi_{ms} = K - \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \ and \ K = \Phi'_m - \chi' - \frac{E_c - E_i}{q} \tag{2.5}$$

where N_A is the acceptor concentration, n_i is the intrinsic concentration, Φ'_m is the effective work function of the metal, χ' is the effective electron affinity, q is the elementary charge, and E_c and E_i are the conduction band edge and the intrinsic level. According to the doping concentration of the substrate, $V_{FB,theor}$ for p-Si/SiO$_2$/Al MIS capacitor can be varied from ~-0.89 V (N_A=1×10^{15}cm^{-3}) to ~-1.01 V (N_A=1×10^{17}cm^{-3}).

b) Effect of Oxide Charges in the C-V Curve

Real MIS capacitors contain charges distributed in the dielectric bulk and at the dielectric/semiconductor interface. In the p-Si/SiO$_2$/Al MIS system, the oxidation process leads to a non-stoichiometric SiO$_x$ layer as is shown in Figure 2.7. This layer is occupied by fixed charges and defects that can interact with the semiconductor. Therefore, these defects can respond to capacitance-voltage measurements. In 1979, Bruce Deal classified the charges in MIS capacitors in four groups: fixed charges (Q_{fix}), mobile ionic charges (Q_{mob}), interface-trapped charges (Q_{it}), and oxide trapped charges (Q_{ot}) [35]. Later, Fleetwood introduced the concept of border traps [36].

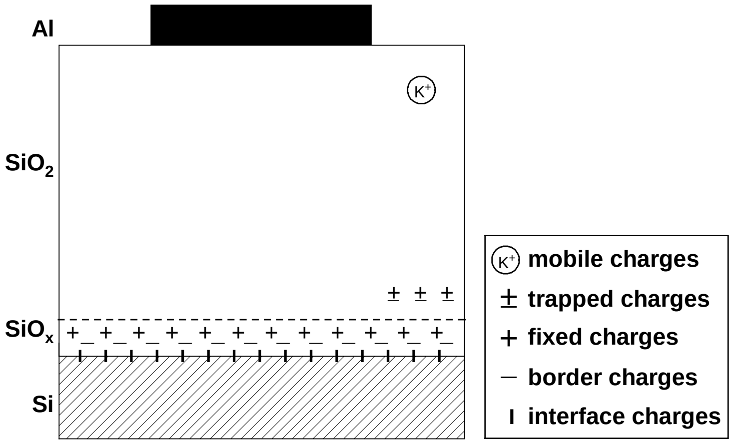


Figure 2.7 Charges and their location between the p-Si/SiO$_2$/Al structure according to the classification of Bruce Deal [35] and Fleetwood [36]. Charges located between the non-stoichiometric SiO$_x$ layer can be measured by capacitance-voltage. The oxidation process leads to a non-stoichiometric SiO$_x$ region occupied by charges that can be measured by impedance spectroscopy.

Mobile charges and oxide trapped charges are distributed within the bulk of the insulator. Q_{mob} are ionic impurities such as Li^+, Na^+, K^+, H^+. These charges are generated by contamination and became mobile at high temperature. Q_{ot} are positive (holes) or negative (electrons) charges generated by ionization radiation, avalanche injection, or similar process. The amount of Q_{ot} can be reduced by annealing treatments below 500 °C. Oxide trapped charges are not affecting *C-V* measurements, and mobile charge can be prevented by avoiding contamination during the manufacturing process of the device. Therefore, only the effect of fixed charges, interface charges, and border charges on the *C-V* characteristics will be analyzed.

a) Fixed Charges, Q_{fix}:

Fixed charges are distributed within the non-stoichiometric SiO$_x$ region. They are fixed in position and cannot interact with the semiconductor. Q_{fix} are created during the oxidation process and can be either positive or negative. In p-Si/SiO$_2$/Al MIS capacitor, Q_{fix} is positive [48,49] while for p-Si/Al$_3$O$_2$/Al is negative [50,51]. Similar to $\Delta\phi_{\mathrm{ms}}$, fixed charges induce a parallel shift of the whole *C-V* curve (see Figure 2.8). The density of fixed charges is determined in the following way: first, the theoretical flat-band voltage ($V_{\mathrm{FB,theor}}$) is subtracted from the measured capacitance ($V_{\mathrm{FB,exp}}$) curve and then Q_{fix} is calculated using Equation 2.6 [52]:

$$Q_{fix} = \frac{\Delta V}{q} C_d \; and \;\; \Delta V = V_{FB,theor} - V_{FB,exp} \tag{2.6}$$

where C_d is the dielectric capacitance and q is the elementary charge. $V_{FB,theor}$ and $V_{FB,exp}$ are the theoretical and experimental flat-band voltages values, respectively.

At the flat-band position, Equation (2.6) contains information of Q_{fix} alone only if the capacitor does not contain border and interface charges. When these charges are taken into account, Equation (2.6) gives information of effective oxide charges ($Q_{fix,eff}= Q_{fix} + Q_{bt} + Q_{it}$).

b) Interface Trapped Charges, Q_{it}:

Interface traps charges are located at the insulator/semiconductor interface (see Figure 2.7). There are three sources of Q_{it}: (1) oxidation-induced defects, (2) metal impurities, and (3) radiation or similar process that produces bond breaking. Interface trap charge density can be measured by charging interface traps levels. Interface traps levels are defects associated with trivalent silicon centers at the Si/SiO_2 interface distributed within the silicon bandgap and can interact with the silicon band edges by capture and emission of carriers with time response between 5 µs to 50 µs [53]. Interface traps are classified in two types: (1) acceptor-like interface traps, that are negatively charged after trapping electrons and neutral when empty and (2) donor-like interface traps are positively charged when donating electrons and neutral when filled [46]. Interface trapped charge stretches out the *C-V* curve along the depletion region and shifts the capacitance curve except at the midgap position (see Figure 2.8). Additionally, they contribute to the total differential capacitance.

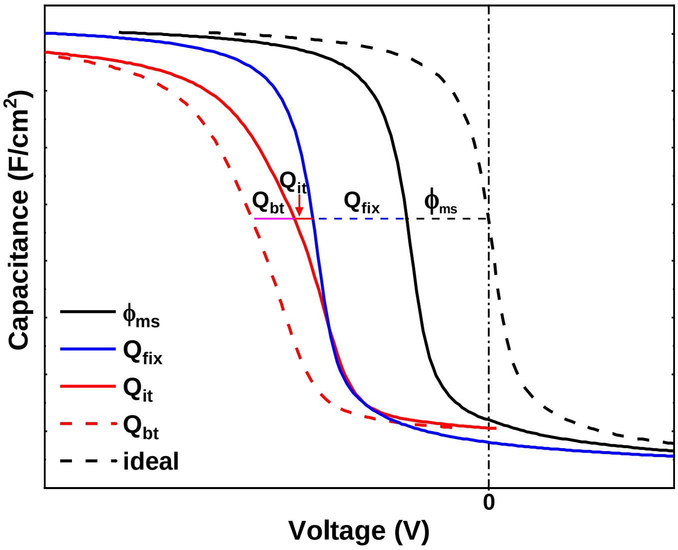


Figure 2.8 Capacitance voltage curve for a real *p*-Si/SiO$_2$/Al MIS capacitor showing the effect of ϕm and the different charges that can be present in the device. Fixed charges induce a parallel shift of the whole capacitance curve. In addition to a small parallel shift interface charges contributed to the accumulation capacitance. In contrast, border-trapped charges generate hysteresis in the *C*-*V* curve.

c) Border-Trapped Charges, Q_{bt}:

Border-trapped charges are located in the dielectric layer but close to the insulator/semiconductor interface (see Figure 2.7) and can be measured by charging border trap levels [54]. Similar to interface traps, border traps communicate with the underlying silicon substrate by exchanging charges predominantly via tunneling process [55] but with lower time response in comparison to interface traps (50 µs to 500 µs) [53]. The origin of border traps can be associated with *E*' centers within the insulator layer. Border traps yield the formation of hysteresis in the *C*-*V* curve and frequency dispersion in the accumulation region of the capacitance at low frequencies [54]. Figure 2.9 shows the three types of centers associated with border traps. Donor-like traps type (1) and (2) are positive trapped charges in the insulator layer which can exchange electron with the silicon. The location of traps type (2) are further than type (1), therefore, the charge exchange is lower for traps type (2). Type (3) is an amphoteric border trap center and similar to interface traps can exchange either electrons of holes with the semiconductor. These three types of traps contribute to the *C*-*V* hysteresis.

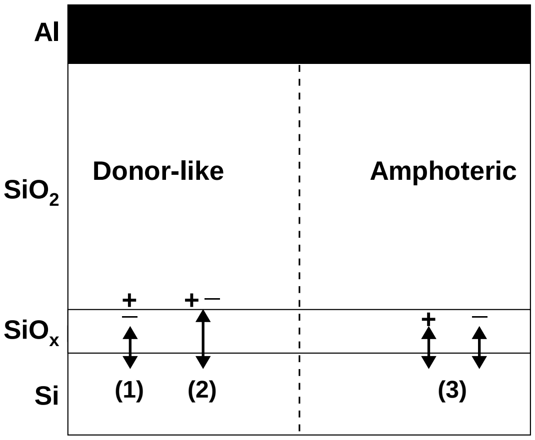


Figure 2.9 Schematic representation of border traps in MIS capacitors. Donor-like traps type (1) and (2) are associated with holes trapped near the interface while amphoteric traps (3) can exchange electrons or charge with the silicon band-edges. The dashed region in the insulator layer represents the non-stoichiometric SiO_2 [56].

In general, fixed charges are known as fixed states because they do not communicate with the semiconductor on the measurement time scale. In contrast, interface traps and border traps are switching states because they communicate electrically with the silicon band edges by capture and emission of carriers. Interface traps are associated with trivalent silicon center at the SiO_2/Si interface due to silicon dangling bonds while border traps are associated with trivalent silicon center in SiO_2 but close to the SiO_2/Si interface due to oxygen vacancies. Amount of fixed and switching states must be controlled since they significantly affect the long-term reliability of MIS-based electronic devices [56]. Defects in SiO_2-based MIS capacitors are reduced by post-annealing treatments under forming gas atmosphere. At high temperatures (~450 °C), hydrogen atoms diffuse easily through the oxide layer and saturate the dangling bonds [57].

2.2 Metal-Organic Frameworks (MOFs)

Metal-organic frameworks are highly ordered crystalline materials consisting of metal ions interconnected to organic linkers yielding a three-dimensional network with well-defined pores as is shown in Figure 2.10 [38,58,59].

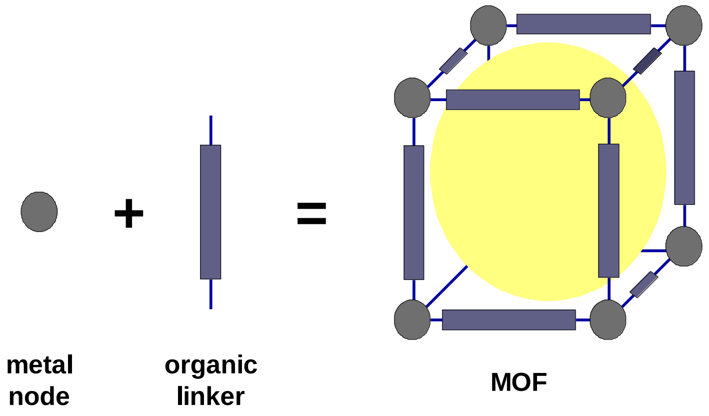


Figure 2.10 Schematic illustration of the construction of MOFs: the connection of the metal node with the organic linker leads a cubic structure [60]. The topology of MOFs is tuned by interconnecting different organic and inorganic components.

There are a large diversity of inorganic components such as Al^{+2}, Cu^{+2}, Fe^{+2}, Zn^{+2} Zr^{+2}, and lanthanides (Ln= La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, and Tm). The organic component typically consists of amines, carboxylates, nitrides, phosphates or sulfonates [61]. The topology and functionality of metal-organic frameworks can be tuned by connecting the inorganic component with different linkers resulting in a large number of MOFs with different geometries and properties suitable for many applications. Table 2.1 summarizes the structural features including metal unit and organic ligand of the different MOFs covered in this section.

Table 2.1 Acronym of metal-organic frameworks and their composition: metal unit + organic ligand. IRMOF: Isoreticular metal framework, MIL: Materials of Institute Lavoisier, ZIF: Zeolitic imidazolate frameworks, UiO: University of Oslo.

MOF acronym	Metal unit	Organic ligand
Co-NDC	Zinc	NDC=2,6-naphthalenedicarboxylic acid
$Cu_3(BTC)_2$	Cooper	BTC=1,3,5 benzenetricarboxylate acid
IRMOF-M2c	Zinc	naphtacene
NDC-Y-fcu MOF	Yttrium	NDC=1,4-naphthalenedicarboxylate acid
MIL-1	Iron	nicotinate molecules
MOF-5	Zinc	1,4-benzodicarboxylic acid
MOF-74	Magnesium	2,5-dihydroxyterephthalic acid
MOF-210	Zinc	2,6-naphthalenedicarboxylic acid
MOF-246	Zinc	DMF=N,N-dimethylformamide acid
UiO-66	Zirconium	1,4-benzodicarboxylic acid
ZIF-8	Zinc	2-methylimidazole

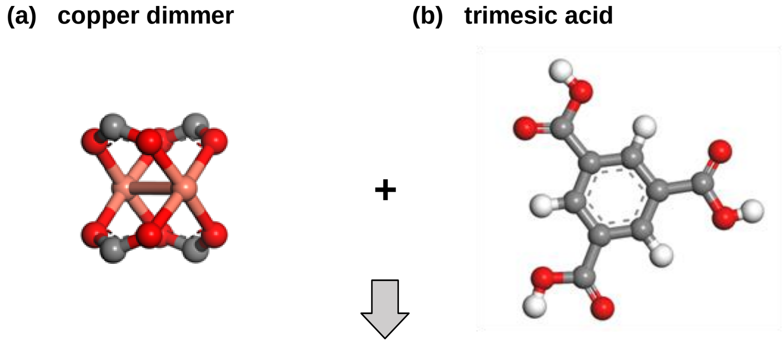
MOFs can host a wide variety of molecules on their inner surface because of its exceptional properties including ultra-high porosity and large surface area. In the case of MOF-210, the pore size and the Brunauer-Emmett-Teller (BET) surface area can be varied up to 48Å and 10.400 m^2g^{-1}, respectively [62]. They exhibit low (1.21 for IRMOF-M2c [63]) and high (14.17 for MOF-246 [64]) dielectric constant values. The optical bandgap can be varied up to 5.5 eV for ZIF-8 [65]. Metal-organic frameworks are affected by different types of defects such as point and extended defects [66]. Point defects are vacancies associated with missing linkers or unsaturated ion metals. On the other hand, extended defects are associated with imperfection in the crystal structure such as dislocations, and heterogeneity [67]. UiO-66 (Zr), MOF-74, and $Cu_3(BTC)_2$ exhibit unsaturated metal sites that serve as host centers for gases or molecules, however, they can degrade under high temperature and humidity conditions (40 °C, 90 % for $Cu_3(BTC)_2$) [68].

MOFs have lots of potential applications including gas storage, separation, catalysis and sensors [38]. In catalysis, UiO-type MOFs have been widely studied because of its chemical stability and defects resulting from the deficiency of linkers that act as active sites for acid-catalyzed reactions [4]. The amount of defects can be easily modulated during the synthesis process. In photovoltaic, Cu-BTC [69] and Co-NDC [70,71] have been investigated as a sensitizing layer in TiO_2 liquid junction solar cells. The conductivity and charge transfer reaction across the TiO_2/MOF/FTO interface were enhanced by iodine doping. Energy conversion efficiency values of 0.26 % and 1.12 % were attained for Cu-BTC [69] and Co-NDC [71] MOFs, respectively. In biomedicine, MOFs are attractive for the delivery of bioactive molecules such as nicotinic acid (vitamin B3). Particularly, the BioMIL-1 built up of non-toxic iron units via nicotinate molecules degrades within a few hours allowing the release of the biomolecule [5,72]. MOFs can sense different vapors, gases, and molecules [73]. For example, rare earths (RE) based MOFs were incorporated on interdigitated electrodes for sensing of ammonia (NH_3). Particularly, NDC-Y-fcu MOF with face-centered cubic lattice containing yttrium nodes and 1,4-naphthalenedicarboxylate (NDC) linker was prepared by the solvothermal method on SiO_2 surfaces functionalized by 11-mercaptoundecanoic acid. NDC-Y-fcu MOF exhibits excellent chemical stability with time and humidity conditions and can detect ammonia at concentrations down to ~1 ppm. Additionally, the MOF offers remarkable sensitivity toward NH_3 versus, CH_2, NO_2, and H_2 [74].

2.2.1 Properties of $Cu_3(BTC)_2$

$Cu_3(BTC)_2$ also known as HKUST-1 consist of Cu(II) dimers linked to 1,3,5 benzenetricarboxylate nodes. The framework was first prepared by Pech-Pickardt [62] and further investigations were performed by Chui *et al.* [28]. 1,3,5 benzenetricarboxylate is also known as trimesic acid (TMA), it comprises a benzene ring connected with three carboxylic groups (Figure 2.11b). The secondary building unit of $Cu_3(BTC)_2$ contains two copper ions (Figure 2.11a) bridged with four BTC units in a paddle wheel arrangement yielding a cubic structure with a lattice constant of 2.68 Å as is shown in Figure 2.11c. The crystal structure involves three pores with different diameters, 5 Å, 11 Å, and 13.5 Å [28].

$Cu_3(BTC)_2$ MOF exhibits the following properties: Brunauer-Emmett-Teller surface area of 1511 m^2g^{-1} [75], large optical bandgap of 3.6 eV [29], a low dielectric constant of 2.3 [30]. Additionally, partial positive charges exist on the copper atoms that are compensated by partial negative charges from the carboxylate units [28]. The unsaturated Cu^{+2} sites can act as absorption, sensing or storage of guest molecules.



(c) $Cu_3(BTC)_2$

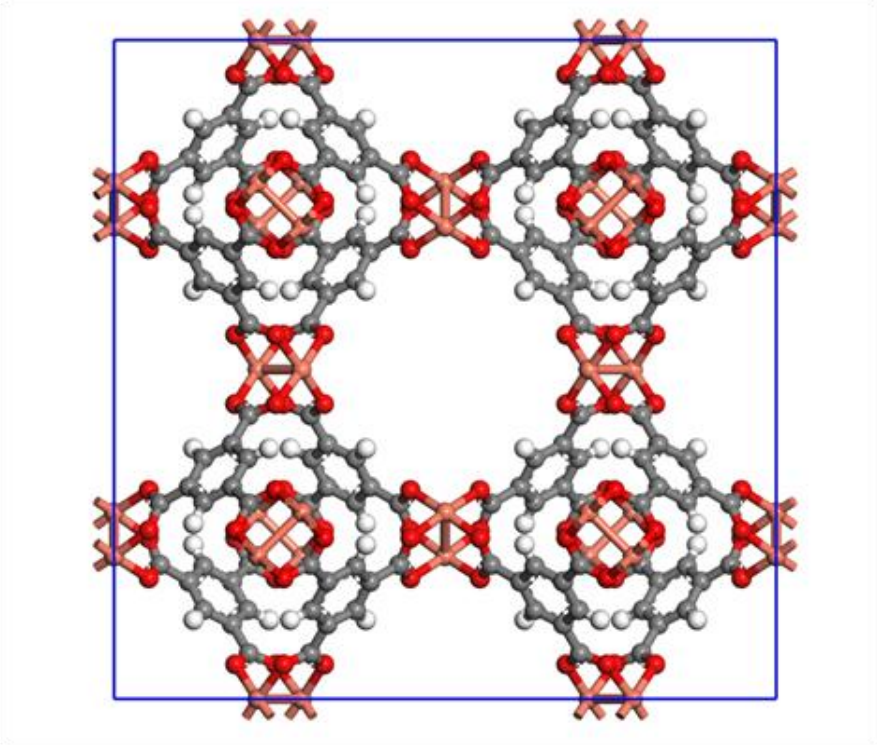


Figure 2.11 Schematic representation of $Cu_3(BTC)_2$ MOF which consist of copper ions (a) and benzene-1,3,5-tricarboxylate units (b) giving rise a cubic structure with a lattice constant of 2.68 Å (c). Cu(orange atoms), O(red atoms), C(gray atoms), and H(white atoms). Image constructed using BIOVIA Materials Studio [76].

2.2.2 Integration of MOFs in Electronic Devices

In the past years, extensive studies demonstrated the potential of metal-organic frameworks obtained as a powder in a wide variety of application [27,61]. Currently, the research is focused on the applications of MOFs in the electronics industry [13,14]. Integration of metal-organic framework into electronic devices requires the deposition of high quality and homogeneous MOFs on substrates with a layer thickness in the nanometer scales (d<100 nm) [6,7,77]. Several deposition methods were developed in order to achieve thin film MOFs on substrates including the solvothermal and the layer-by-layer methods.

a) Solvothermal Method

In this method, the solvents, metal salts and the organic linker are heated in a sealed vessel under pressure and at elevated temperatures. The crystalline structure can be modulated by temperature, pressure, and concentration of the metal and linker solutions. The crystallization process takes place between days or weeks. Additionally, the attachment of MOFs onto substrates supports require surface functionalization [78]. For instance, it was demonstrated that self-assembly monolayers, ultra-thin organic films with high structural quality, allow a direct binding of different materials onto a substrate [79]. One of the firsts deposition of MOFs on substrates was achieved by Hermes *et al.* [8]. They deposited MOF-5 on gold substrates by carboxylic acid-terminated SAM. The complete deposition process was performed in four days (72 hours for solution preparation and 24 hours for growth of the MOF). The solvothermal synthesis offers good control of the crystalline structure by using different functionalized SAMs. For instance, Biemmi *et al.* [80] demonstrated that the orientation of MOF crystals on gold substrates depend strongly on the molecular functionalization of the SAM. $Cu_3(BTC)_2$ grown on COOH-SAM is oriented along the (100) direction while the growth on OH-SAM is oriented along the (111) direction.

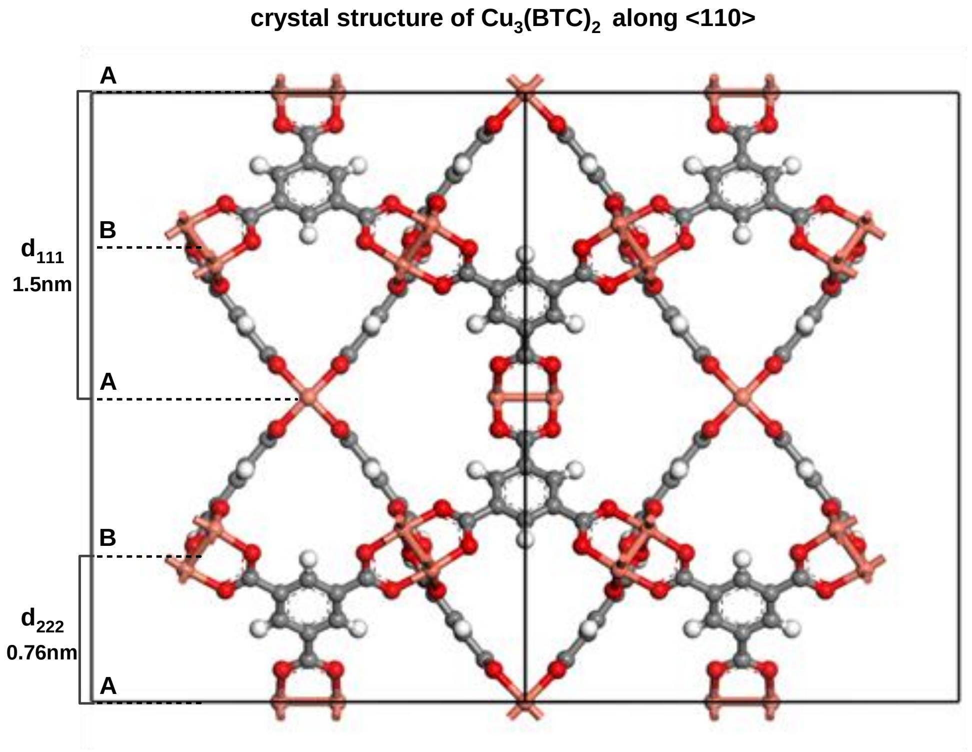


Figure 2.12 Crystal structure for $Cu_3(BTC)_2$ viewed along the <110> orientations showing the growth of the MOFs in step highs of 1.5 nm d_{111} and 0.76 nm d_{222}. Cu(orange atoms), O(red atoms), C(gray atoms), and H(white atoms). Image constructed using BIOVIA Materials Studio [76].

Figure 2.12 shows a cross-sectional analysis of the step-growth for $Cu_3(BTC)_2$ along the (110) direction. $Cu_3(BTC)_2$ can growth along the d_{222} or d_{111} crystal spacings with steps heights of 0.76 nm and 1.5 nm, respectively. The d_{222} step high consist of one layer of dimeric copper connected to four TMA units while the d_{111} is formed by two sublayers [81]. Surface termination at the layer of the octahedra A will leave one vacancy per Cu atom or one CO_2 group per trimesic moiety. Surface termination at the layer of the octahedra B leaves two vacancies per Cu atom or two CO_2 groups per trimesic moiety [81,82]. Atomic force microscopy (AFM) measurements reveal that $Cu_3(BTC)_2$ obtained by solvothermal method grows on steps highs of 1.5±0.1 nm in accordance with the 1.5 nm d_{111} crystal spacing. Additionally, steps highs of 0.8 nm, 2.2 nm, and 3 nm in accordance with the 0.76 nm d_{222} crystal spacing were found [81].

a) Layer-by-Layer (LBL) Growth

In the solvothermal method, the metal and linker precursors are mixed and sealed in a vessel for more than ~18 hours, after that the growth of MOFs takes place between days. In contrast, in the layer-by-layer growth, the metal and linker solutions are applied separately and in sequential order. In addition, pre-treatment of the precursors are not needed, therefore, the deposition process is reduced to hours. The layer-by-layer growth also known as step-by-step deposition was developed by Shekhah *et al.* [9] for the deposition of thin films of $Zn(CH_3CO_2)_2$ on COOH-terminated organic surfaces. The growth was made in a layer-by-layer fashion by repeated immersion of the substrate into a solution of Zn(II) acetate and then in the BTC solution. The MOF was characterized by infrared reflection adsorption spectroscopy which shows the characteristics bands of the carboxylic groups bonded to the Zn(II) ion. Besides, the MOF shows high stability under heating up to 100 °C. Nevertheless, no crystallographic information was obtained. Later $Cu_3(BTC)_2$ was grown on 200 nmAu/Si substrates functionalized by COOH-SAM. XRD and scanning electron microscopy measurements revealed the growth of homogeneous and highly oriented crystalline structures [11]. Deposition details are shown in Figure 2.13. First, the SAM functionalized substrate is immersed in a copper acetate solution for 30 seconds. Then the layer is rinsed with ethanol and dried in nitrogen atmosphere. After that, the substrate is immersed in the TMA solution for one hour and then rinsed in ethanol again.

The layer-by-layer method is based on the immersion of the substrates in the precursor solutions and the deposition time consist of hours and/or days. Later, the LBL approach was enhanced by including ultrasonic steps during the immersion of the substrate in ethanol. This optimization step leads MOFs with high crystalline quality and low defect density [31]. An alternative method based on the LBL process is the spray-coating technique. In this method, the solvents are sprayed onto the substrate. The spray process reduces the deposition time and delivers highly oriented crystalline MOFs. In the case of $Cu_3(BTC)_2$ coated on gold surfaces, the metal and linker solution are sprayed during 10 s and 20 s, respectively. Thus the deposition time consists of 30 minutes or hours according to the desired layer thickness [83].

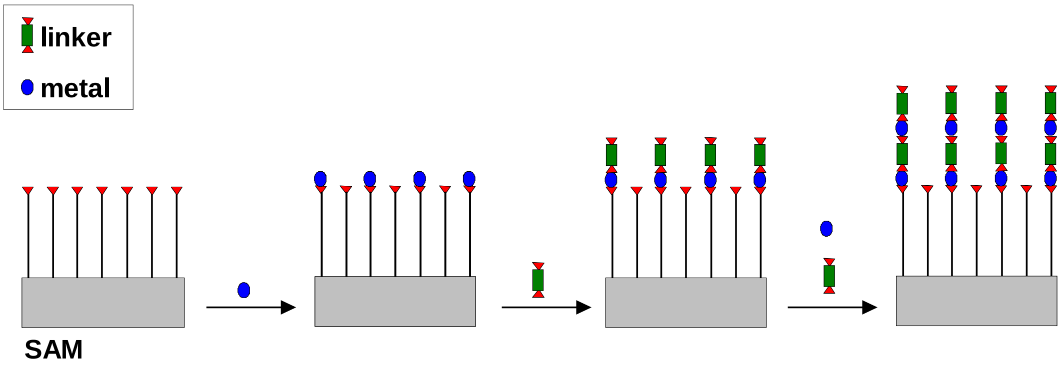


Figure 2.13 Schematic diagram of the layer-by-layer growth. $Cu_3(BTC)_2$ was coated on gold surfaces functionalized with COOH-SAM by repeated immersion of the substrate in copper acetate solution and then in trimesic solution [11].

In general, the layer-by-layer deposition of $Cu_3(BTC)_2$ on a functionalized OH-SAM substrate includes four steps [84]:

i) Nucleation: copper acetate $Cu_2(OAc)_4$ species are sprayed on the substrate and consequently react with the OH groups forming the initial surface precursor for the growth of the MOF.

ii) Ligand exchange: the addition of TMA acid on the substrate allows ligand exchange between the coordinated acetate and the TMA. Secondary building unit is formed by the copper dimmer bridged to four carboxylic groups.

iii) Structure formation: addition of $Cu_2(OAc)_4$ results in the formation of the first step high of 0.76 nm along with the d_{222} crystal spacing (see Figure 2.12).

3 Experimental Details

The following chapter describes the manufacturing of MIS capacitors using $Cu_3(BTC)_2$ MOF as dielectric material and the analytic techniques used for the characterization of the layers and the devices. MIS capacitors were fabricated in the clean room facilities of the Laboratorium für Nano- und Quantenengineering (LNQE) of the Leibniz University (LUH). Deposition of thin $Cu_3(BTC)_2$ films by the spray-coating method and XRD experiments were performed by Ina Strauß at the Institut für Physikalische Chemie und Elektrochemie (LUH). Deposition of MOF layers by the layer-by-layer approach assisted by ultrasonication and XRD experiments were performed by Kai Müller at the Institut für Funktionelle Grenzflächen (IFG) in Karlsruhe. Electrical characterization of the devices was performed at the Institut für Materialien und Bauelemente der Elektronik (MBE).

Attachment of MOFs on substrates was typically obtained through surface functionalization with artificial ultra-thin organic films [85,86]. Therefore in order to ensure the integration of the MOFs within MIS structures, the first set of $Cu_3(BTC)_2$ layers were grown on Si/SiO_2 surfaces functionalized with aminopropyltriethoxysilane (APTES). The growth of MOFs films directly on SiO_2 and Si surfaces was also feasible. Different capacitors were fabricated to demonstrate the reproducibility of the experiments. After manufacturing, inorganic-based MIS capacitors are subjected to post-annealing treatments to improve the quality of the devices by reconstruction of the silicon lattice and chemical passivation. However, $Cu_3(BTC)_2$-based MIS capacitors were not subjected to any post-deposition treatment because the properties of the MOFs degrade at temperatures higher than 200 °C [30]. The successful growth of MOFs on substrates and their functions within MIS capacitors were investigated by XRD experiments and impedance measurements, respectively.

SiO_2-based MIS capacitors were produced for the following purposes: (i) demonstrate the good quality of our oxide layers. This is attained by annealing the capacitor under forming gas atmosphere, (ii) investigation of the effect of trimesic acid (linker molecule of the MOF) on the electrical properties of the capacitor, and (iii) creating the possibility to compare the results.

3.1 Device Processing

MIS capacitors were fabricated on polished boron-doped *p*-type silicon (*p*-Si) and phosphor-doped *n*-type silicon (*n*-Si) wafers with (100)-orientation, 525 µm thickness, and 0.5-0.75 Ωcm resistivity. The quality of these wafers meets the requirements for the quality-oriented semiconductor industry. Three different techniques were used for the manufacture of the devices: (1) thermal oxidation for the growth of silicon dioxide, (2) electron beam evaporation for the deposition of the metal electrode, and (3) the layer-by-layer approach for the growth of the metal-organic framework $Cu_3(BTC)_2$.

3.1.1 Thermal Oxidation

Silicon dioxide layers were grown by thermal oxidation using a horizontal furnace from Centrotherm Europa 2000 Company. The furnace is maintained at a temperature of 700 °C under nitrogen atmosphere. Figure 3.1 shows the temperature-time profile inside the furnace used for the oxidation process of the silicon wafers.

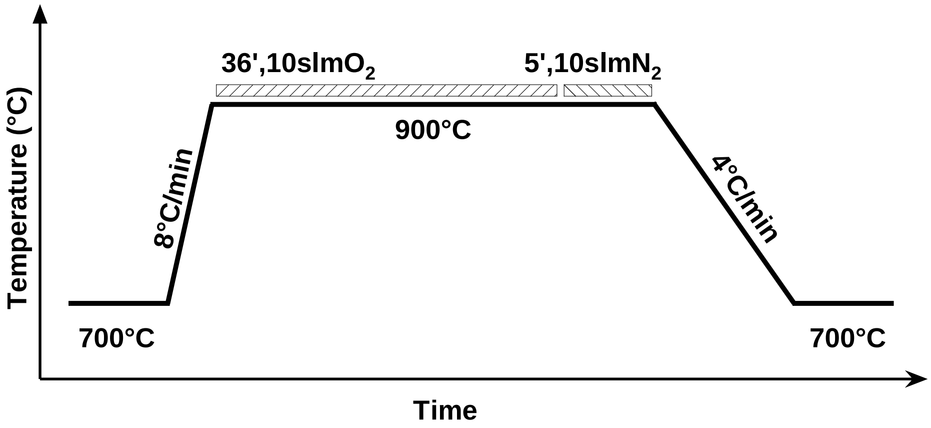


Figure 3.1 Temperature-time profile inside the horizontal furnace used from the growth of silicon dioxide layers. The figure shows the parameters used for the heating, oxidation, and cooling processes. The dashed regions indicate the starting point of the oxidation (light gray) and the cooling (dark gray) processes.

Prior deposition, the wafer was diluted in hydrofluoric acid (HF) solution to remove the native oxide and other contaminations. After that, the wafer was placed into the furnace and heated up to 900 °C in steps of 8 °C/min. The oxidation process occurs once pure oxygen is introduced inside the furnace. The layer thickness of the oxide is handled according to the oxidation time and temperature. For instance, 36 min at 900 °C renders a layer thickness of

~10 nm. Finally, nitrogen is introduced into the furnace and cooled down to 700 °C in steps of 4 °C/min. Silicon dioxide grows according to the reaction shown in Equation (3.1).

$$Si\ (solid) + O_2(gas) = SiO_2\ (solid) \tag{3.1}$$

3.1.2 Metallization

Aluminum electrodes were formed by electron-beam evaporation using a BALZERS BAK 610 system. The equipment consists of a crucible which contains the metal source and a holder substrate placed in the bottom and top of the evaporator system, respectively. In this deposition technique, an electron beam bombards the aluminum target which evaporates toward the substrate. Prior deposition, the base pressure inside the evaporator is in the order of 10^{-6} mbar and the electron beam is generated by heating a tungsten filament with a voltage of 10 kV and current of 200 mA.

3.1.2 Spray of Thin $Cu_3(BTC)_2$ Layers

Thin $Cu_3(BTC)_2$ layers were coated in a layer-by-layer fashion by the spray-coating process. In this method, the metal and linker solutions are applied separately and in sequential order. First, spray of 0.2 mM trimesic acid linker. Then the sample is sprayed with pure ethanol. After that, a spray of 1 mM ethanolic solution of copper (II) acetate. Then spray of ethanol again. This process corresponds to one spray-cycle. Different layer thickness can be achieved by increasing the number of spray cycles [16]. In the case of samples prepared by ultrasonication, the substrate was immersed in the linker and metal solutions using a dipping robot. Ultrasonic bath is switched on when the substrate is immersed in pure ethanol [39,85].

3.2 Fabrication of SiO_2-Based MIS Capacitors

Figure 3.2. Shows the manufacturing process for Si/SiO_2/Al MIS capacitor.

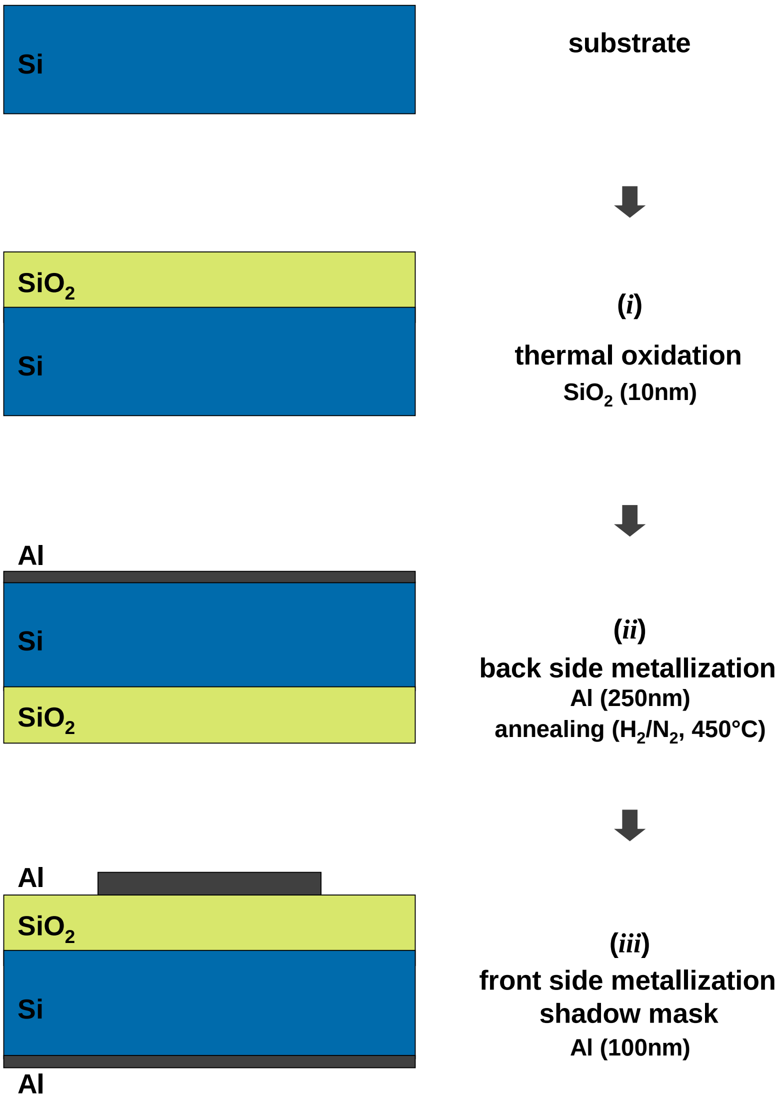


Figure 3.2 Fabrication process of Si/SiO_2/Al MIS capacitors through a shadow mask. First 10 nm SiO_2 was grown by thermal oxidation. After that, 250 nm Al was evaporated as the back electrode and subsequently, the wafer was annealing in forming gas atmosphere at 450 °C to obtain an Ohmic contact. Finally, 100 nm Al gate contacts were formed through a shadow mask.

(i) Growth of 10 nm SiO_2 by thermal oxidation:

First, native oxide and other contaminations were removed by immersing the silicon wafer in 1 % HF solution, and then it was rinsed in deionized water. After that, 10 nm SiO_2 was grown by thermal oxidation at a temperature of 900 °C in pure oxygen atmosphere for 36 minutes. The layer thickness of SiO_2 was confirmed by ellipsometry measurements.

(ii) Backside metallization of 250 nm Al:

The front side of the wafer was protected with photoresist, and then SiO_2 from the backside was removed by HF solution. Next, 250 nm Al was evaporated as the back electrode and then the photoresist was removed. Finally, the wafer was annealing in forming gas atmosphere at 450 °C to obtain an Ohmic contact and to passivate defects at the Si/SiO_2 interface.

(iii) Front side metallization through a shadow mask (100 nm Al):

Prior evaporation of aluminum, the wafer was cut in small pieces of 2 cm × 2 cm. Finally, 100 nm Al gate contact is formed through a shadow mask containing circular dots of areas between 0.0095 cm^2 to 0.0059 cm^2.

After device processing, the capacitors were subjected to different post-treatments: one set was annealed in forming gas atmosphere and the other was immersed in trimesic acid solution. Additionally, two capacitors were used as reference (non-annealed). Table 3.1 summarizes of the $Si/SiO_2/Al$ MIS capacitors used in this work.

Table 3.1 Summary of $Si/SiO_2/Al$ MIS capacitors fabricated on *p*-type and *n*-type silicon substrates. One set of capacitors were subjected to trimesic acid treatments at room temperature and another set was annealed under forming gas atmosphere inside a RTP furnace.

Capacitors	Substrate	Post-treatment
2	*p*-type Si *n*-type Si	Non-annealed (NA)
2	*p*-type Si *n*-type Si	Forming gas (FG)
2	*p*-type Si *n*-type Si	Trimesic acid (TMA)

Post-annealing treatment: rapid thermal annealing (RTA) processing

Forming gas annealing was performed inside an RTP furnace. The wafers were heated at 450 °C in H_2/N_2 atmosphere for three minutes. In this post-annealing treatment, the atmosphere contains hydrogen source that passivates silicon dangling bonds at the Si/SiO_2 interface and, therefore, the quality of the capacitor is improved.

Immersion of capacitors in trimesic acid

Effect of trimesic acid on the electrical properties of SiO_2-based MIS capacitors was investigated by immersing the capacitors in 0.2 mM ethanolic solution of trimesic acid at room temperature for one hour.

3.3 Fabrication of $Cu_3(BTC)_2$-Based MIS Capacitors

Thin $Cu_3(BTC)_2$ films were coated after step *ii* from the process described in Figure 3.2. Several capacitors were processing to demonstrate the reproducibility of the experiments. Figure 3.3 shows the structure of the capacitors fabricated using MOF layers coated by the spray-coating method. A summary of the substrate, functionalization process, and the number of spray cycles are given in Table 3.2.

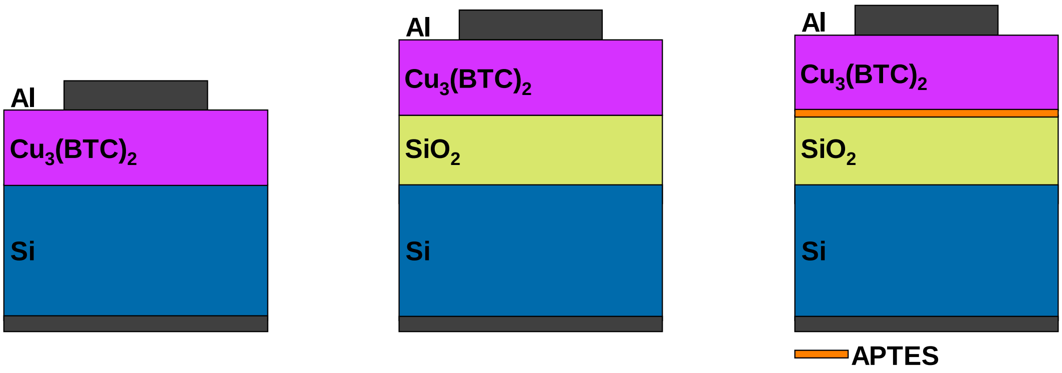


Figure 3.3 Device structure of MIS capacitors using $Cu_3(BTC)_2$ as the dielectric material. MOF layers were coated by the spray-coating method directly on silicon, on silicon dioxide alone and on silicon dioxide functionalized by APTES.

Table 3.2 Summary of $Cu_3(BTC)_2$–based MIS capacitors coated by the layer-by-layer approach with and without ultrasonication.

Spray-coating method			
Capacitor	Substrate	substrate treatment	Spray cycles
4	*p*-type Si	APTES	5, 10, 15, 20
4	*p*-type Si/SiO_2	-	5, 10, 15, 20
4	*p*-type Si/SiO_2	-	5, 10, 15, 20
4	*n*-type Si/SiO_2	-	5, 10, 15, 20
Layer-by-Layer approach assisted by ultrasonication			
2	*p*-type Si/SiO_2	oxygen plasma	15

3.4 Characterization Techniques

3.4.1 Structural and Morphological Characterization

X-ray diffraction (XRD) and Atomic force microscopy (AFM)

X-ray diffraction measurements of ultra-thin $Cu_3(BTC)_2$ films were performed on a Bruker D8 Advance X-ray diffractometer equipped with a $Cu_{K\alpha}$ (λ=0.154 nm) radiation source. The measurements were performed at the 2θ-range from 5 ° to 20 °. For more information see reference [16]. Surface topography of the MOF layers was investigated by atomic force microscopy in contact mode using an Autoprobe M5 device from Park Scientific Company.

3.4.2 Electrical Characterization

Impedance measurements

The electrical characterization was performed through impedance spectroscopy which offers information of capacitance-voltage and conductance-voltage curves separately using an Agilent 4294A impedance analyzer. The measurements were conducted with a small AC signal of 25 mV and by sweeping the DC gate voltage from accumulation to inversion (acc-inv) and then from inversion to accumulation (inv-acc). The DC gate voltage was varied between -6 V to +4 V according to the device structure. All the measurements were performed under constant environment ($T \approx 294$ K and approximately 30% relative humidity)

Capacitance and conductance curves were acquired as a function of gate voltage and frequency in order to apply the conductance method. Frequency-dependent measurements were carried out at room temperature in the frequency range from 3 kHz to 500 kHz. Heating experiments were performed to desorb guest molecules from the $Cu_3(BTC)_2$ pores, resulting in measurements of the electronic properties of the empty MOF. The samples were heated from 30 °C to 100 °C and then cooled down to room temperature in steps of 10 degrees Celsius. The frequency was fixed at 100 kHz for all heating experiments.

4 Methods for Characterizing Interface and Border Trap Density in MIS Devices

Several methods are available for characterizing defects and electrical parameters at the insulator/semiconductor interface. Among them, impedance spectroscopy composed of capacitance and conductance curves seems to be a powerful technique for the investigation of interface traps and border traps. Interface traps can exchange charges with the underlying silicon band edges by capture and emission processes, consequently, an energy loss occurs and it is manifested as a peak in the conductance-voltage curve. On the other hand, border traps interact with the silicon band edges by trapping/detrapping of charges via tunneling. Charging and discharging phenomena leads to hysteresis effects in the capacitance-voltage curve. This chapter describes the basic principles of the methods used to investigate the quality of insulating materials. Finally, the models will be applied to test the electronic properties of the metal-organic framework $Cu_3(BTC)_2$.

4.1 Series Resistance Correction

Capacitance and conductance measurements are strongly affected by different sources that produce energy loss in MIS capacitors. For instance, series resistance (R_s) can overlap important information about interfacial properties and doping profiles. Therefore, extraction of R_s from impedance measurements is necessary to perform an accurate analysis of the data. Correction of R_s was performed following the model proposed by Nicollian-Brews [87]. This method determines R_s from the equivalent circuit of an MIS capacitor biased in strong accumulation. Furthermore, the measured capacitance and conductance curves are corrected using the determined R_s.

In accumulation, the equivalent circuit for an MIS capacitor consists of the dielectric capacitance (C_d) connected in series with the parallel combination of the admittance of interface traps (Y_{it}) and the accumulation capacitance (C_A) as is shown in Figure 4.1a. In strong accumulation, admittance is shunted by the large value of C_A, thus the equivalent circuit is simplified to Figure 4.1 b. The circuit is further reduced to Figure 4.1c because of $C_A >> C_d$.

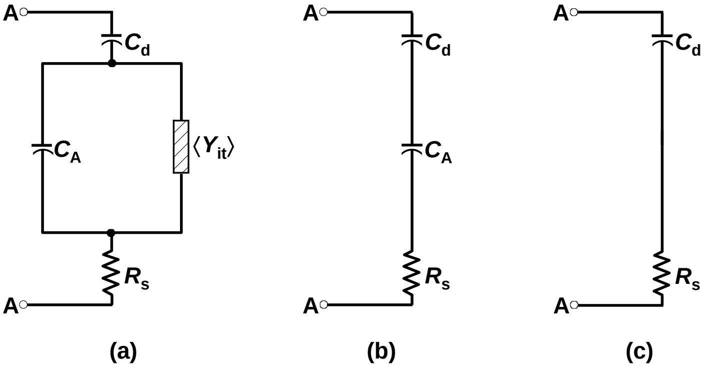


Figure 4.1 Equivalent circuit of an MIS capacitor in accumulation taking into account series resistance (a), simplified circuit of a (b), and simplified circuit of b (c) [87].

In Figure 4.1 c, the measured admittance in accumulation ($Y_{ma} = G_{ma} + j\omega C_{ma}$) across the terminal A-A is inverse proportional to the impedance ($Z_{ma} = 1/Y_{ma}$). Series resistance is determined from the real part of the impedance and is defined by:

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2} \tag{4.1}$$

where $\omega (= 2\pi f)$ is the angular frequency, C_{ma} and G_{ma} are the capacitance and conductance measured in strong accumulation, respectively.

Corrected capacitance (C_{c}) and corrected conductance (G_{c}) at any frequency of interested are given by the following equations:

$$\begin{aligned} C_c &= \frac{(G_m^2 + \omega^2 C_m^2) C_m}{a^2 + \omega^2 C_m^2} \\ G_c &= \frac{(G_m^2 + \omega^2 C_m^2) a}{a^2 + \omega^2 C_m^2} \end{aligned} \tag{4.2}$$

here a is a constant defined as $a = G_m - (G_m^2 + \omega^2 C_m^2) R_s$, C_{m} and G_{m} are the measured capacitance and conductance.

Figure 4.2 shows capacitance and conductance curves as a function of the gate bias measured at 500 kHz for p-Si/SiO$_2$/Cu$_3$(BTC)$_2$/Al MIS capacitor before (black curve) and after series resistance correction (dashed blue curve). A low series resistance of 10.8 Ω was obtained for the MOF based MIS capacitor. The small R_s value does not influence the capacitance curve. In contrast, the conductance is strongly sensitive to R_s in accumulation, depletion, and inversion regions. This fact, recommend the correction of the admittance curves before the evaluation of the interfacial properties of the devices.

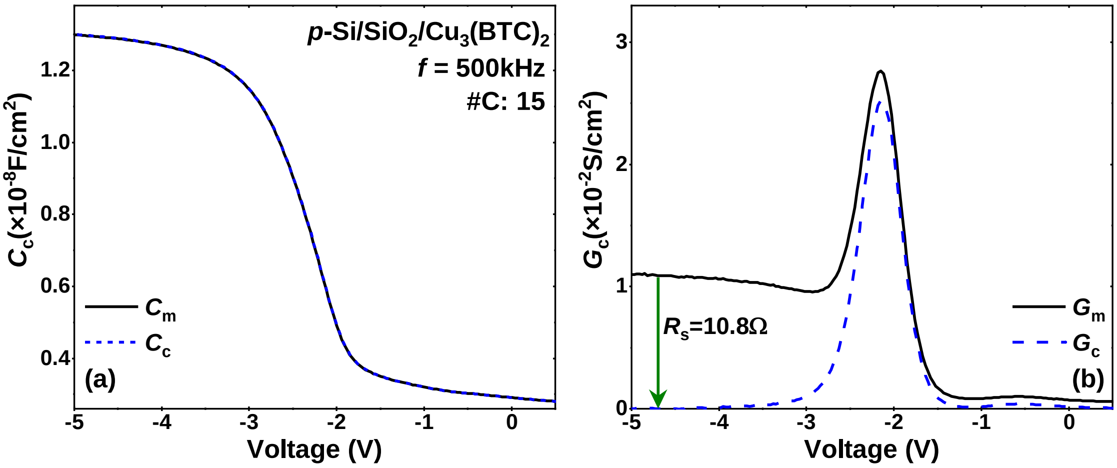


Figure 4.2 Measured capacitance C_m (a) and conductance G_m (b) curves as a function of gate voltage for p-Si/SiO$_2$/Cu$_3$(BTC)$_2$/Al MIS capacitor. The measurement was carried out form inversion to accumulation at a frequency of 500 kHz. The dashed blue curves have been corrected from series resistance, C_c and G_c.

4.2 Determination of the Dielectric Capacitance

Capacitance-voltage characteristics have been widely used to quantify interface trap densities at the SiO$_2$/Si interface. Besides, the layer thickness of the dielectric can be determined from the accumulation region of the capacitance curve. In accumulation, the capacitance consists of the series combination of the dielectric capacitance (C_d) and the semiconductor capacitance (C_s) and can be affected by interface traps too. Therefore, it is recommended to calculate C_d using an extrapolation model instead of manual calculation. The extrapolated algorithm used here was proposed by McNutt-Sah [88]. In this model, C_d is retrieved from the accumulation range of the capacitance curve, assuming that the concentration of the majority carrier is high and therefore the contributions of interface and near interface charges can be neglected.

$$\sqrt[2]{\left|\frac{dV}{dC}\right|} = \sqrt[2]{\frac{q}{2kTC_d}}(C_d - C) \tag{4.3}$$

where C_d is the dielectric thickness, q is the electric charge and kT is an energy scale factor.

The layer thickness of the dielectric material (electrically thickness, C_d) is calculated introducing the calculated C_d into the capacitance equation d=A$\varepsilon\varepsilon_d$ /C_d. It is important to perform capacitance measurements at high frequency since interface and border traps will not be fast enough to respond to the AC signal, thus dielectric thickness is extracted from the contribution of majority carrier only. Figure 4.3 shows the capacitance curves in strong accumulation measured at 500 kHz for p-Si/SiO$_2$/Cu$_3$(BTC)$_2$/Al MIS capacitor in the McNutt-Sah representation. The intercept with the y-axis represents the dielectric capacitance (C_d=6.61×10^{-07} F/cm^{-2}). The calculated electrically layer thickness was 10 nm.

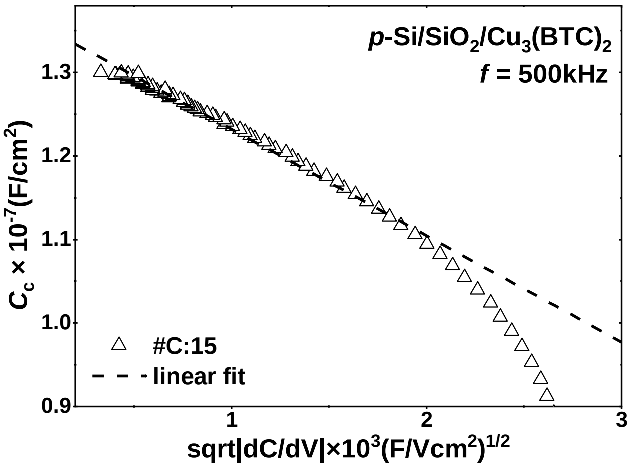


Figure 4.3 Capacitance curve in the McNutt-Sah representation model for p-Si/SiO$_2$/Cu$_3$(BTC)$_2$/Al MIS capacitor. The dielectric capacitance was determined from the linear extrapolation.

4.3 Determination of Interface Trap Density

Interface traps are defects located at the Si/SiO$_2$ interface and have energy levels distributed within the silicon bandgap. These defects change occupancy via capture/emission of carriers with the silicon band edges. Change in charge density (δQ_{it}) resulting from the capture of carriers stretched out the capacitance curve along the voltage axis and contributes an extra capacitance (C_{it}) to the total capacitance (C). In addition, change in occupancy causes an energy loss which is measured as an equivalent parallel conductance. In general, interface trap density can be quantitatively investigated from the capacitance and/or conductance components of the measured admittance. The capacitance-based methods compare the measured capacitance curve at high frequency (C_{HF}) or low frequency (C_{LF}) with the ideal ones [89,90].

At high frequencies, Terman assumes that there is no contribution of interface states to the total capacitance as they do not respond to the AC gate voltage [89]. In this method, a theoretical C-V curve ($C_{HF,theor}$) versus surfaces potential (ψ_s) is simulated and compared with the measured one ($C_{HF,m}$) versus V_g. Finally, ψ_s versus V_g can be calculated from the comparison between the $C_{HF,theor}$–ψ_s and the $C_{HF,m}$–V_g plots. In contrast, at low frequencies, capacitance immediately responds to the AC voltage, thus they will contribute to the total capacitance. The relation between ψ_s and V_g can be found using the Berglung integral [90]. Later, Castagne and Valpaille combine both methods to calculate interface trap information from high and low frequency C–V curves [91]. This approximation is very advantageous since the simulation of $C_s(\psi_s)$ is not needed.

4.3.1 Conductance Method

The conductance method developed by Nicollian-Brews is based on the analysis of the energy loss that occurs when interface traps change occupancy due to carrier transfer with the semiconductor band edges [87]. Interface trap occupancy can be perturbed by variation in gate voltage as is shown in Figure 4.4. Under any biasing condition (V=0), interface trap charges and additional contributions to the flat-band voltage will induce band-bending across the semiconductor interface (Figure 4.4a).

When a negative voltage is applied to the metal gate, the valence band edge moves closer to the Fermi level and the filled interface traps become empty by capture of holes (Figure 4.4b). On the contrary, a positive voltage moves the conduction band edge closer to the Fermi level. In this case, interface states emit holes to the conduction band and become filled (Figure 4.4c). Changes in occupancy of interface states occur in a small energy interval around the Fermi level (kT/q) and are measured by the equivalent parallel conductance using equation (4.4).

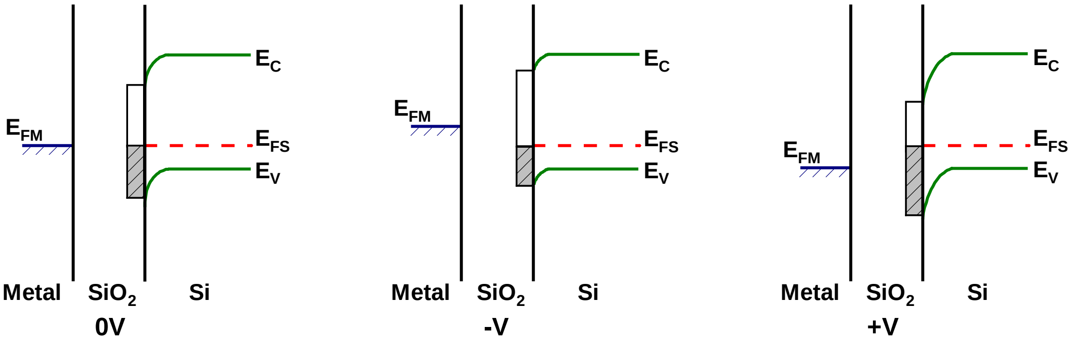


Figure 4.4 Energy band-diagram for a for *p*-Si/SiO$_2$/Al MIS capacitor under different applied voltages: zero voltage (a), negative gate voltage (b), and positive gate voltage (c). Interface traps below the Fermi level are empty and above are filled [87].

$$\frac{G_p}{\omega} = \frac{C_d^2 G_m}{G_m^2 + \omega^2 (C_d - C_m)^2} \tag{4.4}$$

where C_d is the dielectric capacitance, ω is the angular frequency and G_m and C_m are the measured capacitance and conductance.

The equivalent circuit for an MIS capacitor in depletion is shown in Figure 4.5. The circuit consists of the dielectric capacitance in series combination with the semiconductor capacitance. C_{it} and R_{it} are the capacitance and resistance contributions due to the capture and emission of carriers by interface traps. Figure 4.5b shows the equivalent parallel conductance (G_p) and the equivalent parallel capacitance (C_p) that can be retrieved with the conductance method. Single-energy level Interface trap density (D_{it}) is calculated from the conductance component using the following equation (4.5). Figure 4.5b shows the measured capacitance and conductance obtained by the impedance analyzer. The measured *C*–*V* and *G*–*V* curves are related to the parallel curve according to equation (4.4).

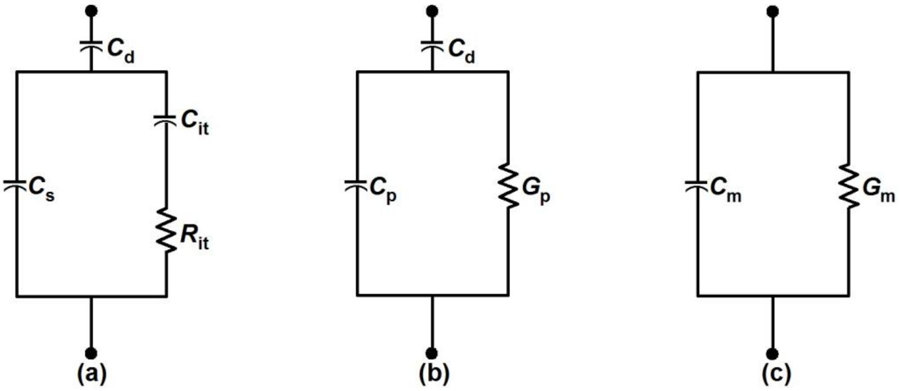


Figure 4.5 Equivalent circuit diagram of an MIS capacitor used to determine interface trap density. General circuit in depletion region (a), for the conductance method (b), and measured circuit (c) [52].

$$\frac{G_p}{\omega} = \frac{\omega\tau_{it}D_{it}}{1+(\tau_{it}\omega)^2} \tag{4.5}$$

where $\tau(= R_{it}C_{it})$ is the trap time constant and D_{it} is the interface trap density

Although the conductance method offers detailed information about interfacial properties, it requires admittance measurements as a function of the voltage and frequency increasing the complexity of the data. The data are evaluated in the following way: (1) first C–V and G–V measurements are performed at different frequencies; (2) the data are corrected from series resistances using the equation given in section 4.1; (3) G_{cp}/ω versus gate voltage is retrieved using equation (4.4) (see Figure 4.6a); (4) G_{cp}/ω versus angular frequency is calculated from the G_{cp}/ω–V curves and a Gauss fit is applied (see Figure 4.6b); (5) finally, the density of interface states is calculated from the peak of the G_{cp}/ω–V curve.

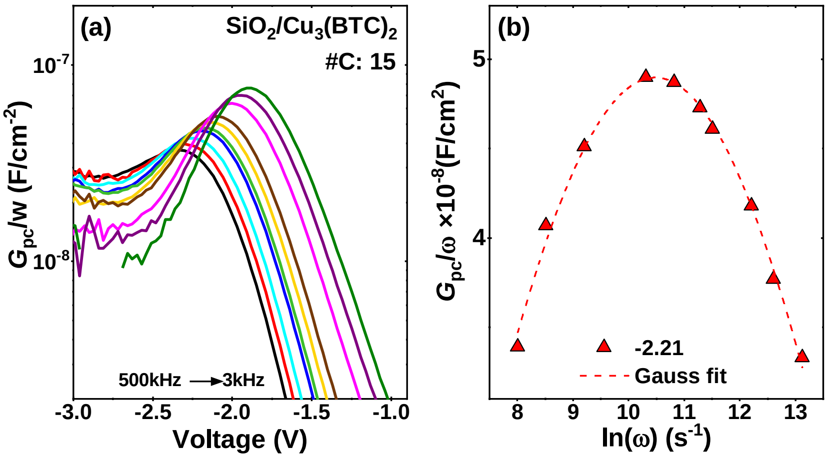


Figure 4.6 Equivalent parallel conductance versus gate voltage measured at different applied frequencies for *p*-Si/$SiO_2/Cu_3(BTC)_2$/Al MIS capacitor (a). Equivalent parallel conductance versus angular frequency at 2.21 V (b).

4.3.2 Hill-Coleman Method

The conductance method is considered the most accurate approximation to quantified interface traps because it employs only experimental data. Nevertheless, the evaluation of the data is tedious and time-consuming since a high amount of measurements are required. Hill-Coleman proposed a new evaluation procedure based in a single frequency measurement and allows determination of interface trap density from 7×10^{9}eV^{-1}cm^{-2} to 8×10^{11}eV^{-1}cm^{-2} [92].

The approximation technique requires a single impedance measure performed at high frequency as is shown in Figure 4.7. The density of interface traps is determined from the maximum value of the conductance curve and the corresponding capacitance value using the following equation:

$$D_{it,HC} = \frac{2}{eA}\frac{G_{m,max}/\omega}{\left(\frac{G_{m,max}}{\omega C_d}\right)^2 + \left(1 - \frac{C_m}{C_d}\right)^2} \tag{4.6}$$

where A is the area of the metal gate, *e* the electron charge, *ω* the angular frequency, $G_{m,max}$, C_m, and C_d are the measured conductance, capacitance, and dielectric capacitance, respectively.

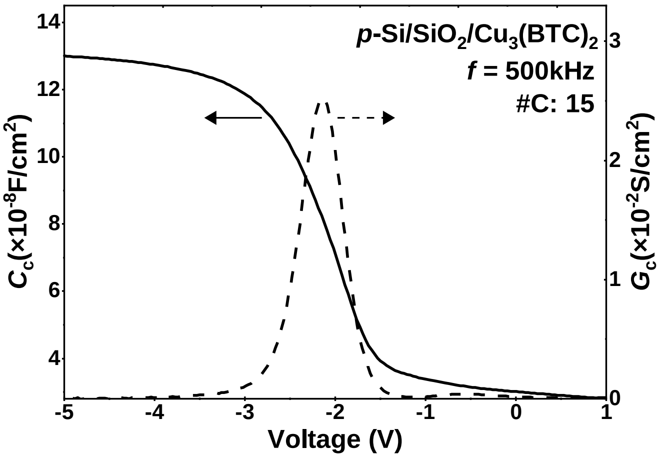


Figure 4.7 Corrected capacitance and corrected conductance as a function of gate voltage measured at 500 kHz for *p*-Si/SiO_2/$Cu_3(BTC)_2$/Al MIS capacitor.

Figure 4.7 shows the capacitance and conductance curve measured at 500 kHz for *p*-Si/SiO_2/$Cu_3(BTC)_2$/Al MIS capacitor. A density of interface traps of $4\times10^{11}eV^{-1}cm^{-2}$ was calculated using the Hill-Coleman approximation. Although the method offers a quick evaluation of D_{it}, the obtained value is very close to the obtained one using the conductance method, $5.36\times10^{11}eV^{-1}cm^{-2}$.

4.4 Determination of Border Trap Density

Border traps can be characterized from the hysteresis o the capacitance-voltage curve. Hysteresis occurs when border traps transfer charge with the silicon substrates or with the metal gate via tunneling during the voltage sweep. Density of border traps is retrieved from the difference between the forward and the backward measurements either at the flat-band or midgap positions using equation (4.7).

$$N_{bt} = \frac{\Delta V_{FR} C_d}{qA} \tag{4.7}$$

where C_d is the dielectric capacitance, ΔV_{FR} is the *C*–*V* hysteresis, *q* is the electronic charge, and A the area of the gate contact.

Alternatively, Fleetwood *et al.* [93] determined the total density of border traps by integrating the absolute difference between the forward and reverse *C*-*V* curve against gate voltage using the following equation (4.8).

$$N_{bt} = \frac{1}{qA}\int |C_F - C_R| dV \qquad (4.8)$$

where C_F and C_R are the forward and reverse capacitance.

Forward and reverse capacitance-voltage curves for *p*-Si/SiO$_2$/Cu$_3$(BTC)$_2$/Al MIS capacitor is shown in Figure 4.8. Density of border traps was determined from the hysteresis of the *C*-*V* curve using equation (4.8). Interface traps affect only the depletion of the conductance curve (Figure 4.7). In contrast, border traps influence not only the depletion region but also part of accumulation an inversion.

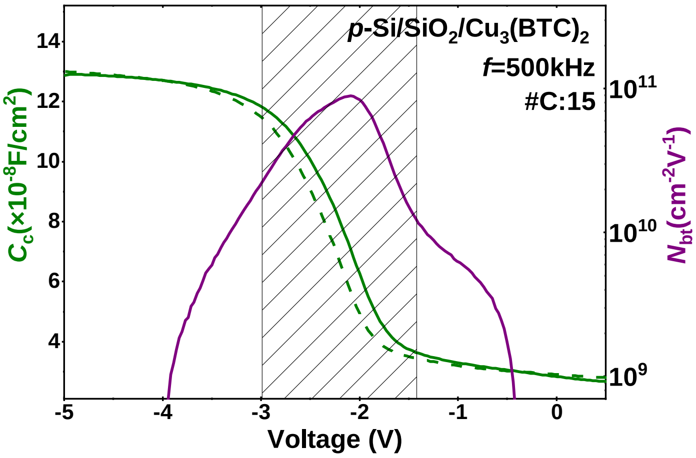


Figure 4.8 Forward (solid line) and reverse (dashed line) capacitance curves and total border trap density as a function of the applied gate voltage for *p*-Si/SiO$_2$/Cu$_3$(BTC)$_2$/Al MIS capacitor. The MOF layer was prepared with 15 spray cycles. The shadowed region represents the strongest contribution of border traps.

5 Effect of Trimesic Acid (TMA) in Si/SiO$_2$ MIS Capacitors

5.1 Introduction

This research work investigates the electrical properties of ultra-thin $Cu_3(BTC)_2$ metal-organic framework incorporated within MIS capacitors. The performance of MIS-based electronic devices depends on the quality of the dielectric/semiconductor interface. In MIS capacitors, good interface quality is achieved by passivating dangling bonds at the Si/SiO$_2$ interface through atomic hydrogen existing in the dielectric gate material or introduced during post-annealing treatments. The linker component (BTC=1,3,5 benzenetricarboxylate or TMA=trimesic acid) of $Cu_3(BTC)_2$ contains in its structure hydrogen atoms. Therefore, understanding the effect of trimesic acid on the electrical properties of Si/SiO$_2$/Al MIS capacitors is of great importance.

Adsorption of organic molecules on silicon substrates is an attractive research area of interest due to the possibility of modifying the substrate surface by molecular interaction between guest molecules and the silicon [94–97]. For instance, it was shown that benzene is chemisorbed non-dissociatively on silicon surfaces at 300 K and can saturate dangling bonds [98,99]. Electron energy loss spectroscopy demonstrates that on Si(111)(7×7) substrate benzene is π bonded to the surface [98] while on Si(100) the chemisorbed benzene is di-σ bonded to two adjacent Si-Si dimers [99]. Trimesic acid (also known as BTC) composed of a benzene ring with three carboxylic acid groups, can be also absorbed on Si(111)(7×7) at room temperature. Scanning tunneling microscopy and density of functional theory investigations reveal that, absorption of trimesic acid occurs in two different manner: (1) formation of three bonds between oxygen atoms of the carboxylic end groups and silicon atoms (non-dissociated case), and/or (2) dissociation of three OH bonds which leads free H atoms that can be covalently bonded with silicon atoms (dissociated case) [100]. It was further theoretically demonstrated that the electronic properties of silicon (111) surfaces can be tuned by the adsorption of isolated molecules or complete monolayer of TMA [95]. According to these findings, TMA can play an important role in the passivation of dangling bonds and electrical properties of Si-based MIS capacitors. In literature not much is known about this topic, therefore, the following chapter investigates the effect of TMA on SiO$_2$-based MIS capacitor structures.

$Si/SiO_2/Al$ MIS capacitors with 10 nm thick SiO_2 layers were fabricated on boron-doped and phosphor-doped silicon substrates with (100) orientation and series resistance between 0.5 Ωcm to 0.75 Ωcm. The investigated capacitors were divided into three groups. The first group was immersed under 0.2mM ethanolic solution of trimesic acid at room temperature during one hour. The second group was annealed in a rapid thermal processing furnace at a temperature of 450 °C during 3 minutes under forming gas (FG) atmosphere. The third group was not subjected to any treatment (non-annealed, NA) and was used as a reference.

The impact of TMA acid treatments and forming gas annealing on the electrical properties of the capacitors was evaluated by impedance measurements performed in forward and reverse mode at different frequencies. All the capacitance-voltage and conductance-voltage curves were corrected from series resistance using the Nicollian-Brews method [87]. Furthermore, border traps densities and interface traps densities were determined using the methods described in chapter 4. Evaluations of the $Si/SiO_2/Al$ MIS capacitors are beneficial to prove the capability of producing SiO_2 layers with good insulating properties and quality. On the other hand, in the next chapters thin $Cu_3(BTC)_2$ films will be stacked with SiO_2, therefore, the results obtained in this part will allow a good differentiation between the electrical properties of the $SiO_2/Cu_3(BTC)_2$ stack and the SiO_2 alone.

5.2 C-V and G-V Characteristics of Si/SiO_2 MIS Capacitors

5.2.1 Impact of TMA Treatments and Forming Gas Annealing

The effect of trimesic acid treatments and forming gas annealing on the capacitance-voltage characteristics of SiO_2-based MIS capacitors fabricated on *p*-type and *n*-type Si (100) substrates are shown in Figure 5.1. The measurements were performed in both forward (solid line) and reverse (dotted line) mode at a fixed frequency of 500 kHz and at room temperature.

Capacitance–voltage curve of *p*-$Si/SiO_2/Al$ MIS capacitor without any treatments (black curve) exhibits a high density of defects which is inferred from three notable characteristics in the *C*-*V* curve (see Figure 5.1a). First, flat-band voltage shift ($V_{FB,exp}$), there is a parallel shift of the whole *C*-*V* curve toward negative voltages indicating a large amount of fixed positive charges in the insulating material. Second, high density of interface traps which stretched-out the *C*-*V* curve in depletion. Finally, the *C*-*V* curve measured in forward and reverse bias mode exhibits a large hysteresis confirming the existing of border traps. In inorganic materials, the origin of border traps is attributed to defects in the insulating layer such as oxygen vacancies [101]. The orientation of hysteresis suggests that carriers are injected from the semiconductor into border traps [102,103].

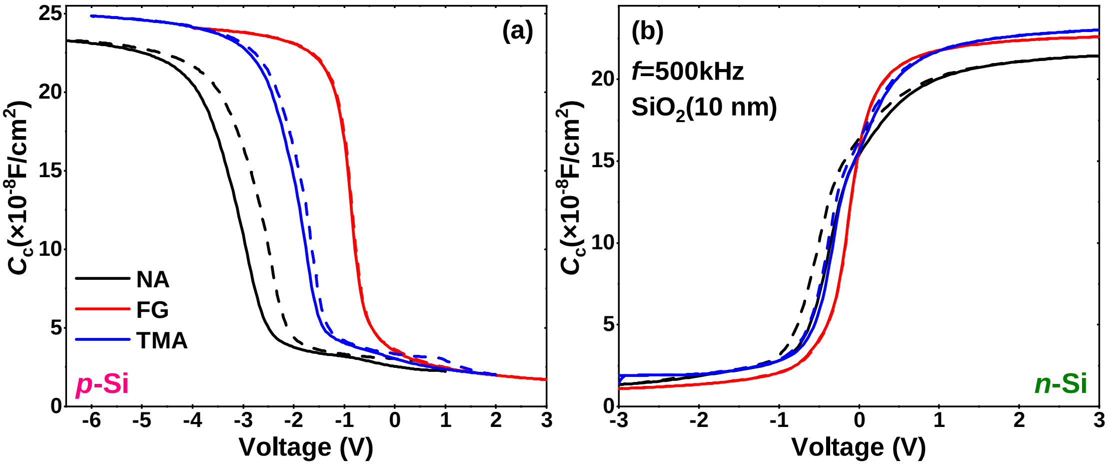


Figure 5.1 Impact of trimesic acid treatments (TMA, blue color) and forming gas annealing (FG, red color) on the capacitance-voltage characteristics of *p*-Si/SiO_2/Al MIS capacitors fabricated on *p*-type (a) and *n*-type (b) silicon (100) substrates. The capacitor without any treatment is referred as non-annealed (NA, black color).

Theoretical flat-band voltage ($V_{FB,theor}$) was calculated as the difference in work function between the semiconductor and the metal gate [52]. Doping concentration density values were retrieved from the measured *C-V* curve while the work function of aluminum and silicon were taken from reference [104]. $V_{FB,theor}$ values of -0.88 V and -0.28 V was found for *p*-type and *n*-type Si substrates, respectively. Experimental flat-band voltage ($V_{FB,exp}$) was determined using the method developed by Winter *el at.* [105]. In this method, first the second derivative of the capacitance is plotted as a function of the gate voltage. Then $V_{FB,exp}$ is extracted from the intersection of the d^2C_c/dV^2-V_g curve with the voltage axis. Further, effective oxide charge density ($Q_{ox,eff}$) in SiO_2 were determined from the flat-band voltage difference ($\Delta V = V_{FB,theor} - V_{FB,exp}$). In the case of *p*-type Si, $Q_{ox,eff}$ for non-annealed samples is found to be $+2.38\times10^{12}$ cm^{-3}. Immersion of the capacitor in TMA leads to a slight reduction of hysteresis, flat-band voltage and effective oxide charge density ($+1.24\times10^{12}$ cm^{-3}). Reduction of $Q_{ox,eff}$ could be connected with the reduction of fixed positive charges due to negative charges contributed by the TMA. The quality of the devices is further considerable improved by annealing in forming gas atmosphere. In this case, almost no hysteresis is observed, $V_{FB,exp}$(-0.89 V) was reduced close to the theoretical value, and a low $Q_{ox,eff}$ of $+3.2\times10^{09}$ cm^{-3} was calculated.

Figure 5.1b shows *C–V* curves for capacitors fabricated on *n*-type Si substrates. The devices exhibit smaller flat-band voltage shift and lesser hysteresis than those fabricated on *p*-type Si substrates, thus the effect of TMA acid and forming gas annealing is also less strong. The capacitor without any treatment exhibits a $Q_{ox,eff}$ of $+4.14\times10^{11}$ cm^{-3}. TMA treatments and annealing under forming gas atmosphere reduces $Q_{ox,eff}$ down to $+1.94\times10^{11}$ cm^{-3} and $+1.16\times10^{10}$ cm^{-3}, respectively.

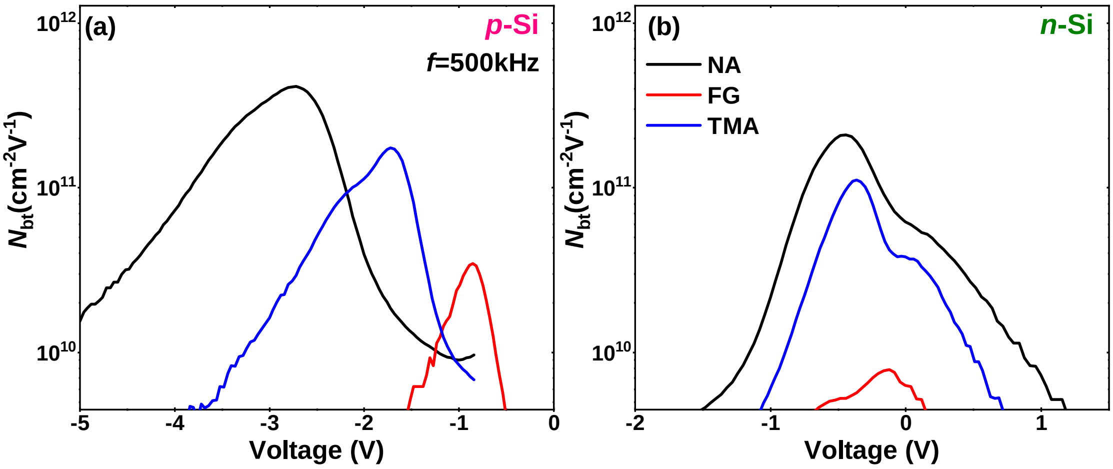


Figure 5.2 Effect of trimesic acid treatments (TMA, blue color) and forming gas annealing (FG, red color) on the border trap density of p-Si/SiO$_2$/Al MIS capacitors fabricated on p-type (a) and n-type (b) silicon substrates. $N_{bt,F}$ was retrieved using the model proposed by Fleetwood et al. [93].

Figure 5.2 shows the density of border traps determined from the C–V curves of Figure 5.1 using the approximation of Fleetwood *et al.* [93]. The response of border traps is strongly in depletion region and is manifested by a broad sharp peak which maximum value occurs around the flat-band voltage. Border traps can also respond in accumulation and inversion since time response of border traps (τ_{bt}~50 μs - 500 μs) is larger than interface traps (τ_{it}~5 μs - 50 μs) [53]. N_{bt} values for capacitors growth on p-type Si substrates decreases from 1.11×10^{12} cm^{-2} (non-annealed) to 2.99×10^{11} cm^{-2} (forming gas, Figure 5.1a). Capacitors grown on n-type Si substrates show even better results. The lowest $N_{bt,F}$ (7.8×10^{09} cm^{-2}) value was achieved for the sample annealed in forming gas atmosphere. Reduction in the density of border traps upon immersion of the capacitor in TMA can be attributed to the saturation of oxygen vacancies in the SiO$_2$ layer by hydrogen atoms dissociated from OH groups of the TMA.

Conductance–voltage characteristics measured at a fixed frequency of 500 kHz for SiO$_2$-based MIS capacitors fabricated on p-type and n-type silicon substrates are shown in Figure 5.3. The capacitors exhibit only one peak in depletion region indicating that only interface traps are able to follow the AC current. The non-annealed capacitors and the treated ones in

TMA acid show a sharp peak indicating a strong change in charge occupancy by capture and emission processes between interface traps and the silicon band edges.

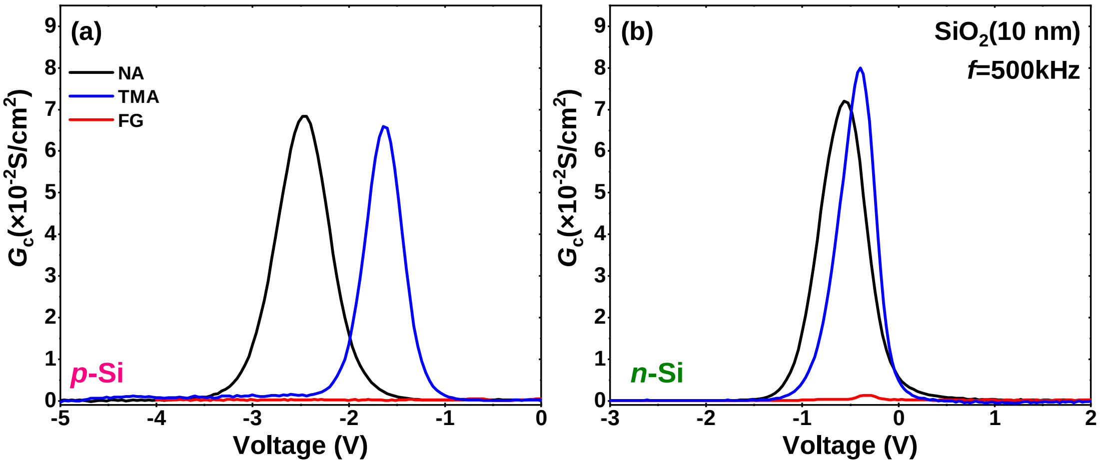


Figure 5.3 Impact of trimesic acid treatments (TMA, blue color) and forming gas annealing (FG, red color) on the conductance-voltage characteristics of *p*-Si/SiO$_2$/Al MIS capacitors fabricated on *p*-type (a) and *n*-type (b) silicon substrates.

The effect of TMA acid on the conductance curve is very little; it only produces a slight reduction of the full width at half maximum (FWHM). In contrast, annealing under forming gas passivates dangling bonds and thus change in charge occupancy is suppressed. Interface trap density retrieved using the Hill-Coleman method are 7.59×10^{11} eV^{-1}cm^{-2} (NA), 7.61×10^{11} eV^{-1}cm^{-2} (TMA), and 3.43×10^{09} eV^{-1}cm^{-2} (FG) for capacitors fabricated on *p*-type Si substrates while 8.06×10^{11} eV^{-1}cm^{-2} (NA), 7.99×10^{11} eV^{-1}cm^{-2} (TMA), 8.58×10^{09} eVcm^{-2} (FG) were obtained for *n*-type Si substrates. Capacitors fabricated on *p*-type Si substrates show lower interface trap density, meanwhile, border trap density is lower for *n*-type Si substrates.

The sources of defects in *p*-Si/SiO$_2$/Al MIS devices are trivalent silicon center (P_b center, also known as *E* center). Two P_b-centers were identified, P_{b0} associated with interface traps and P_{b1} centers associated with border traps. The P_{b0} center consists of silicon atoms with a single dangling bond (·Si≡Si$_3$) and the P_{b1} is a partially oxidized center (·Si≡Si$_2$O) [40–43]. The results suggest that trimesic acid passivates mainly border traps associate to oxidized centers in SiO$_2$ while forming gas annealing passivates effectively both interface and border traps.

5.2.2 Frequency Effects

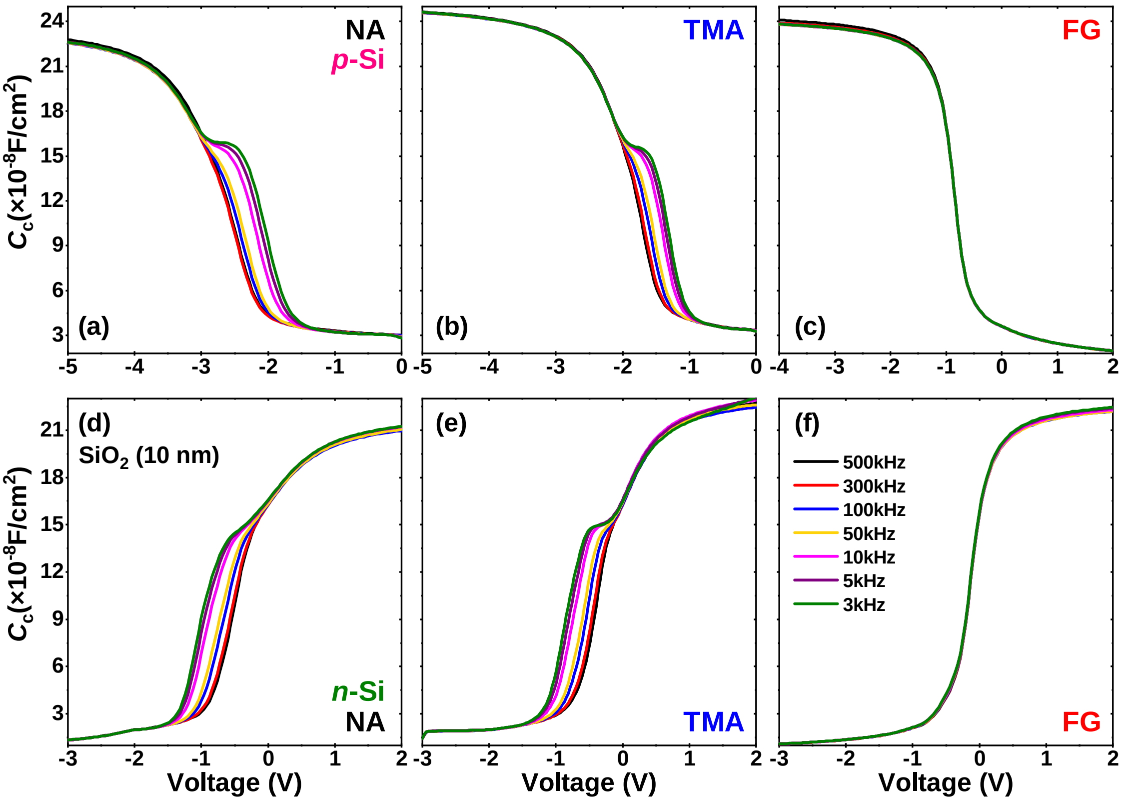


Figure 5.4 Capacitance-voltage characteristics for *p*-Si/SiO_2/Al MIS capacitors measured at frequencies from 3 kHz to 500 kHz. MIS capacitors without any post-treatment (a,d), subjected to TMA acid (b,e) and annealing in forming gas (c,f).

Frequency-dependent impedance measurements were performed to determine an accurate density of interface traps using the conductance method. Figure 5.4 shows capacitance-voltage characteristics measured in the frequency range from 3 kHz to 500 kHz for SiO_2-based MIS capacitors fabricated on *p*-type and *n*-type silicon substrates. Capacitance-voltage curves for the non-annealed capacitors and the immersed in TMA are very sensitive to the AC current at low frequency, especially in depletion region. At frequencies below 100 kHz, a hump appears and gradually increases as the frequency is decreased. Additionally, there is a slight decrease in the accumulation capacitance. Based on the above results, frequency dependence is attributed to the high densities of border traps and interface traps. The interfacial defects are passivated by forming gas annealing; therefore *C*-*V* curves are independent of the frequency (Figure 5.4c and f).

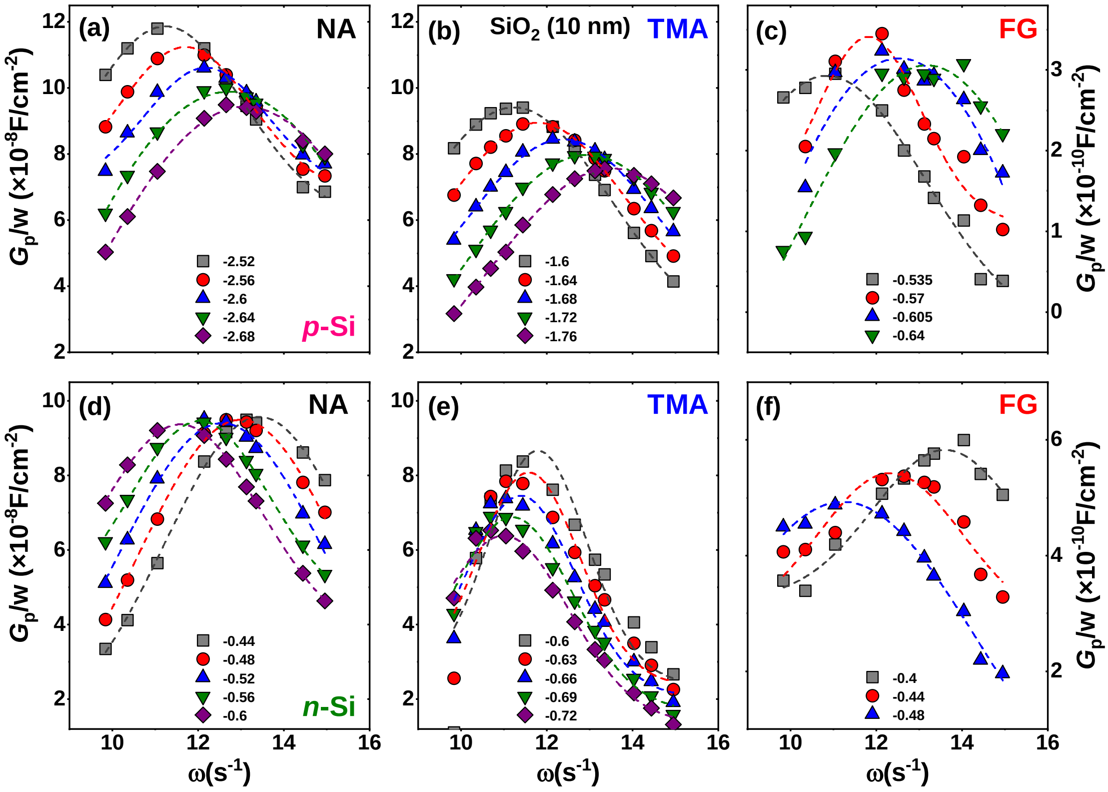


Figure 5.5 Equivalent parallel conductance as a function of angular frequency for *p*-Si/SiO$_2$/Al MIS capacitors without any post-treatment (a,d), subjected to TMA acid (b,e) and annealing in forming gas (c,f). The curves were fitted with a single Gaussian function (dotted lined) to determine the density of interface traps. The dots indicate the voltage at which the G_{pc}/ω-ω curve was extracted.

Equivalent parallel conductance curves (G_{cp}/ω) as a function of angular frequency for different gate voltages are depicted in Figure 5.5. The conductance curves show only one peak indicating that the major contribution to the energy loss is due to interface traps. Density of interface states is calculated from the maximum value of the G_{cp}/ω–V curves; this value was extracted by applying Gaussian fits to the conductance curve as is shown in Figure 5.5. High D_{it} values in the order of 10^{12} eV^{-1}cm^{-2} were found for the non-annealed capacitors and the immersed ones in TMA. In contrast, annealing treatments under forming gas atmosphere passivates effectively dangling bonds and thus D_{it} is reduced up to three orders of magnitude.

5.3 Summary

It was shown that non-annealed SiO$_2$-based MIS capacitors fabricated on *p*-type and *n*-type silicon substrates possess a high amount of fixed positive charges, and high density of interface and border traps that leads to threshold-voltage instabilities. Fixed charges shift the flat-band voltage to the negative voltage axis. Border traps act as trapping/detrapping sources leading to hysteresis in the *C–V* curves. Meanwhile, interface traps stretched-out the depletion regions of the capacitance and cause humps at low frequencies. Additionally, high density of interface traps broadens the peak of the conductance curve and increases its intensity. Furthermore, the high defect density induces frequency dispersion in the accumulation and depletion regions of the *C-V* curves. These electrical characteristics are slightly reduced by immersion of the capacitor in trimesic acid at room temperature. Those capacitors exhibit lower border trap density and therefore better interface quality in comparison to the non-annealed capacitors. Nevertheless, effective passivation of both interface and border traps can be obtained only by annealing the capacitor under forming gas atmosphere.

Two types of defects that dominated the electronic properties of the Si/SiO_2 interface were identified: stretched Si-Si bonds that lead distortion of the silicon lattice and silicon dangling bond centers with amphoteric ($\cdot Si \equiv Si_3$) or donor-like nature ($\cdot Si \equiv Si_2O$, $\cdot Si \equiv SiO_2$, $\cdot Si \equiv O_3$) [106]. Several methods were implemented to achieve MIS capacitors with low defect density. Some authors addressed the cleaning of the silicon surface by chemical treatments in order to remove impurities and native oxide before the deposition of the dielectric material. Among then HF-etching, piranha and the Radio Corporation of America (RCA) cleaning are the standard procedures [107,108]. Other authors focused on the chemical passivation and reconstruction of the silicon lattice by post-annealing treatments such as standard firing process or forming gas annealing [109–111]. Post-annealing treatments depend strongly on the temperature, annealing time, and atmosphere. Firing steps are performed inside a beltline furnace at ~850 °C during seconds. On the other hand, forming gas annealing is carried out inside an RTP furnace under vacuum, in H_2/N_2 atmosphere, at ~450 °C, and during ~3 minutes. It was shown that firing steps in SiO_2 alone leads only to the reconstruction of strained Si-O bonds and reduction of pin-hole density, but it hardly alters the density of interface traps because of the lack of hydrogen source [109]. In contrast, forming gas annealing offers good chemical passivation by saturation of dangling bonds through atomic hydrogen, therefore, interface trap density decreases [112,113].

Improvement of the quality of the capacitor immersed in trimesic acid at room temperature could be related to the adsorption of hydrogen atoms that dissociated from the carboxylates unit of TMA and then diffusion of atomic hydrogen toward the Si/SiO_2 interface [100]. Table 5.1 shows the electrical parameter determined from the capacitance and conductance curves for Si/SiO_2/Al MIS capacitors without any treatment, immersed in TMA, and annealed in forming gas. The results demonstrate good quality of the insulating SiO_2 layer but only under FG annealing.

Table 5.1 Effective oxide charges ($Q_{\mathrm{eff,ox}}$), border trap density ($N_{\mathrm{bt,F}}$), and interface trap density ($D_{\mathrm{it,HC}}$) for SiO_2 fabricated on *p*-type and *n*-type silicon substrates.

Capacitor	*p*-type Si			*n*-type Si		
	$Q_{\mathrm{eff,ox}}$ $\mathrm{cm^{-3}}$	$N_{\mathrm{bt,F}}$ $\mathrm{cm^{-2}}$	$D_{\mathrm{it,HC}}$ $\mathrm{eV^{-1}cm^{-2}}$	$Q_{\mathrm{eff,ox}}$ $\mathrm{cm^{-3}}$	$N_{\mathrm{bt,F}}$ $\mathrm{cm^{-2}}$	$D_{\mathrm{it,HC}}$ $\mathrm{eV^{-1}cm^{-2}}$
NA	2.38×10^{12}	1.11×10^{12}	1.66×10^{12}	4.14×10^{11}	0.93×10^{11}	1.48×10^{12}
TMA	1.24×10^{12}	2.99×10^{11}	1.32×10^{12}	1.94×10^{11}	0.40×10^{11}	1.16×10^{12}
FG	3.20×10^{09}	2.81×10^{10}	5.33×10^{09}	1.16×10^{10}	0.78×10^{09}	8.47×10^{09}

6 Ultra-Thin $Cu_3(BTC)_2$ Films Based MIS Capacitors: Spray-Coating Method

6.1 Introduction

Integration of metal-organic frameworks in electronic devices for sensing applications is an area of great interest because of its extraordinary properties, such as porosity and high surface area. The application of MOFs in metal-insulating-semiconductor structures is of particular importance since it offers information about interfacial defects including effective oxide charges and interfacial trap density. To our knowledge, we were the first to report about that topic [15,16]. Challenges to incorporating MOFs within capacitor structures are the growth of homogeneous thin MOF films on silicon substrates, with good insulating properties and layer thickness in the nanometer scale (<100 nm) [77]. The first attachment of MOFs on Si/SiO_2 substrates with layer thicknesses in the micrometer scale was achieved by the solvothermal method [39,85]. The layer thickness was considerably reduced to the nanometer scale by the spray-coating technique [2,11]. These methods require functionalization of the substrate with an artificial organic layer such as self-assembled monolayers or APTES to facilitate the nucleation of the MOF [85,86]. Here, it will be demonstrated the feasibility of integrating ultra-thin films of MOFs within MIS capacitor structures. MOF layers were successfully grown on silicon substrates and silicon dioxide surfaces with and without functionalization.

Ultra-thin $Cu_3(BTC)_2$ MOF films were prepared by the spray-coating method at the Institut für Physikalische Chemie und Elektrochemie (LUH) [2,11,16]. The layer thickness of the MOFs was easily handled by increasing the number of spray cycles: 5, 10, 15, and 20 spray cycles were used in the present investigation. One spray cycle consists of four steps: (1) spray of the metal solution, (2) spray of pure ethanol, (3) spray of the linker solution, and (4) spray of pure ethanol again. Thin $Cu_3(BTC)_2$ films were grown directly on silicon, on SiO_2 alone, and on SiO_2 functionalized with APTES [15]. The capacitors were fabricated on boron-doped and phosphor-doped silicon substrates with (100) orientation and series resistance between 0.5 Ωcm to 0.75 Ωcm. Insulating SiO_2 layers were grown by thermal oxidation with a layer thickness of 10 nm. Aluminum contacts with an area of 0.0061 cm^2 were used as the gate electrode for all the capacitors. The successful integration of $Cu_3(BTC)_2$ MOFs within MIS capacitor structures was corroborated by different analytic techniques. Crystalline structure and morphology of the $Cu_3(BTC)_2$ films were investigated by X-ray diffraction and atomic force microscopy, respectively. The electrical properties were studied by impedance measurements performed in a wide range of frequencies and at different temperatures. Electrical parameters of the capacitors were retrieved using the conductance method [87], and the approaches proposed by Winter *el at*. [105], Hill-Coleman [92], and Fleetwood *et al.* [93]. Part of the results of $Cu_3(BTC)_2$ grown directly on silicon is published in reference [16].

6.2 Structural and Morphological Properties of $Cu_3(BTC)_2$ on Si and SiO_2 Surfaces

X-ray diffraction experiments were performed to verify the crystalline structure and successful growth of $Cu_3(BTC)_2$ directly on silicon and silicon dioxide surfaces. Figure 6.1 shows the X-ray patterns for ultra-thin $Cu_3(BTC)_2$ films prepared with the following number of spray cycles: 5 cycles (black patterns), 10 cycles (red patterns), 15 cycles (blue patterns), and 20 cycles (green patterns). The diffraction patterns for all the investigated MOFs are in accordance with the calculated ones for powder [114].

According to the diffractograms, it can be demonstrated that the growth of thin $Cu_3(BTC)_2$ films is mainly oriented along the (222) diffraction plane. MOF layers growth with 5 spray cycles shows only a weak (222) peak. The crystalline structure of the layers is considerably improved upon the increment of the number of spray cycles during the coating process. This is demonstrated by the significant increase in the intensity of the peaks. MOFs coated on *p*-Si/SiO_2 and *n*-Si/SiO_2 substrates exhibit only the (222) diffraction plane. In contrast, in the case of $Cu_3(BTC)_2$ growth directly on silicon and functionalized by APTES, an increment of layer thickness favors the growth of grains along the (002), (022), (004), and (333) planes. Increase in peak intensity is related to an increase in layer thickness, d_{MOF}. For instance, 15 spray cycles results in a layer thickness of 9.1 nm $Cu_3(BTC)_2$ on SiO_2 and 20.5 nm for $Cu_3(BTC)_2$ on SiO_2 functionalized with APTES (see Figure 6.6).

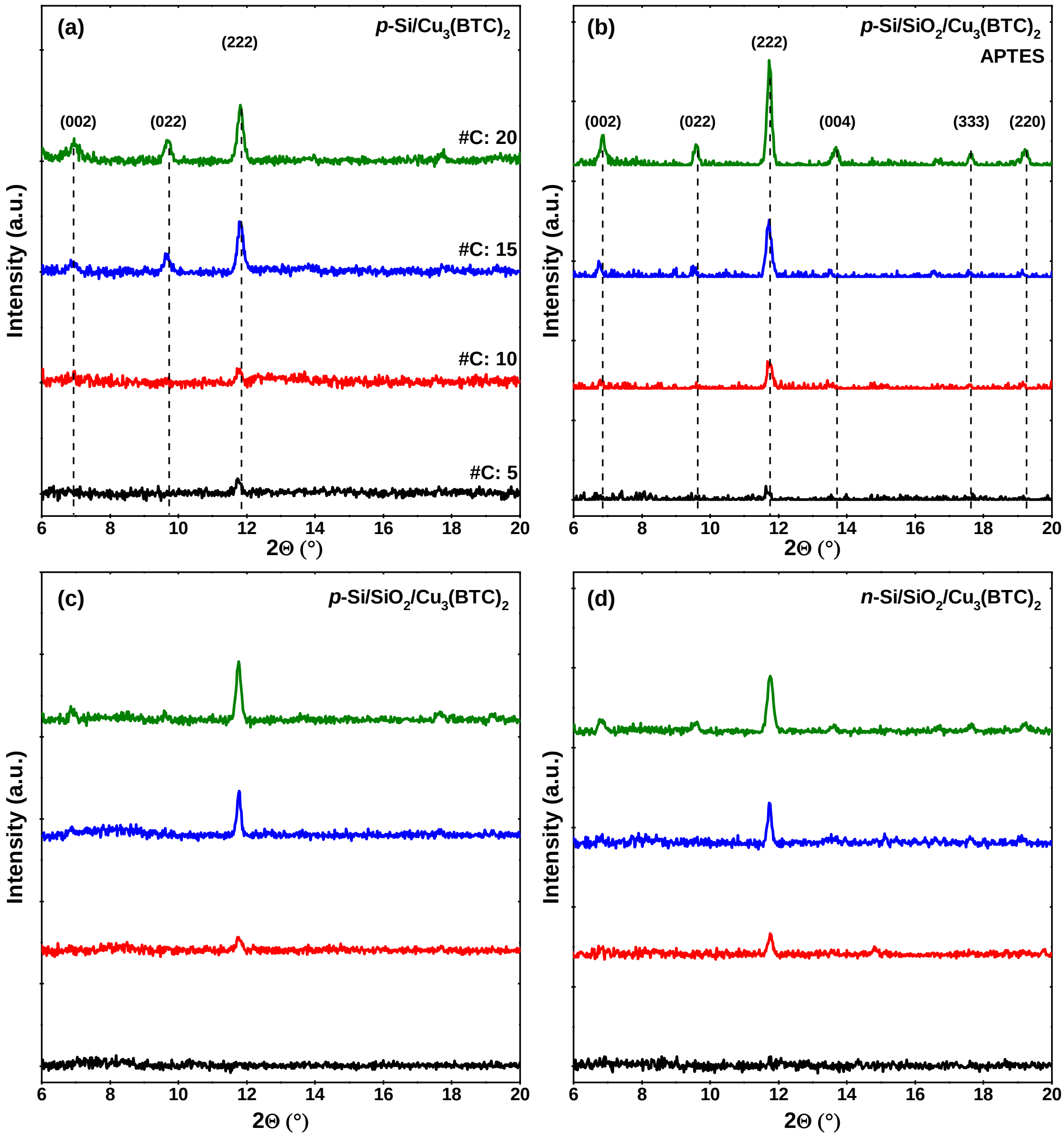


Figure 6.1 X-ray diffractograms for ultra-thin $Cu_3(BTC)_2$ films grown on different substrates: directly on *p*-type silicon (a), on *p*-Si/SiO_2 functionalized by APTES (b), on *p*-Si/SiO_2 (c), and on *n*-Si/SiO_2 (d). The following number of spray cycles was employed: 5 cycles (black patterns), 10 cycles (red patterns), 15 cycles (blue patterns), and 20 cycles (green patterns).

Atomic force microscopy image for $Cu_3(BTC)_2$ coated directly on silicon using 5 spray cycles is shown in Figure 6.2a. Average roughness (R_{ms}) of 3.41 nm was found for a scan area of 10 µm×10 µm. Small scan areas of 0.3 µm × 0.3 µm deliver smaller roughness values of 0.31 nm. Average roughness values for samples growth with 15 spray cycles are 13.30 nm and 6.11 nm in scan areas of 5 µm × 5 µm and 0.3 µm × 0.3 µm, respectively. The results show quite high R_{ms} values.

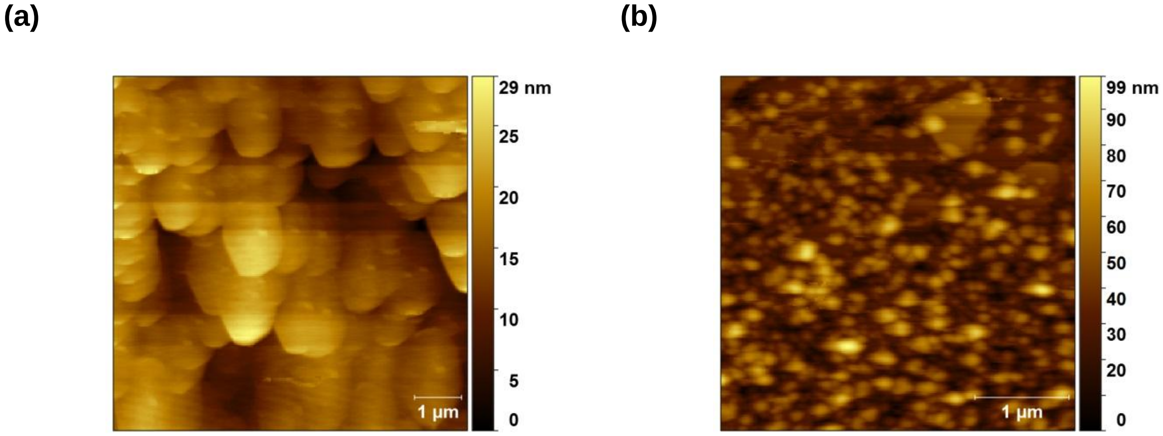


Figure 6.2 Topographical atomic force microscopy images for ultra-thin $Cu_3(BTC)_2$ films coated with 5 spray cycles directly on silicon (a) and 15 spray cycles on SiO_2 surfaces functionalized through APTES (b).

6.3. Impedance Characteristics of $Cu_3(BTC)_2$ on *p*-type Silicon

6.3.1 Effect of Layer Thickness

The following section presents the electrical properties of ultra-thin $Cu_3(BTC)_2$ films incorporated in different MIS capacitor structures using *p*-type silicon as a substrate. First, detailed information about the electrical characteristics for $Cu_3(BTC)_2$ growth directly on silicon will be presented. Afterwards properties of $Cu_3(BTC)_2$ growth on SiO_2 alone and SiO_2 functionalized by APTES will be summarized. The results will be compared with those for non-annealed *p*-Si/SiO_2/Al MIS capacitors since MOF-based capacitors were not subjected to post-annealing treatments. It is important to remark that SiO_2-based capacitors annealed in forming gas exhibits better properties, however, even inorganic dielectric materials can neither surpass nor archive such SiO_2/Si interface quality.

Electrical properties will be retrieved from impedance measurements in the following order: MOF layer thickness (electrically thickness, *d*), flat-band voltage, effective oxide charges, border trap density, and interface trap density. Every MIS capacitor has dimensions of 2 cm × 2 cm and contains gate electrodes in circular shape with an area of 0.0061 cm^2.

Impedance measurements were performed in different positions of every capacitor to evaluate the uniformity of the MOFs. Results are shown in Figure A-6.1. In depletion and inversion regions, there is a slight variation of the capacitance-voltage curves. The change in accumulation region is attributed to the difference in layer thickness. On the other hand, conductance curves exhibit only a slight difference in depletion region. The results demonstrate that the ultra-thin $Cu_3(BTC)_2$ films exhibit good uniformity even when AFM images deliver high R_{ms} values.

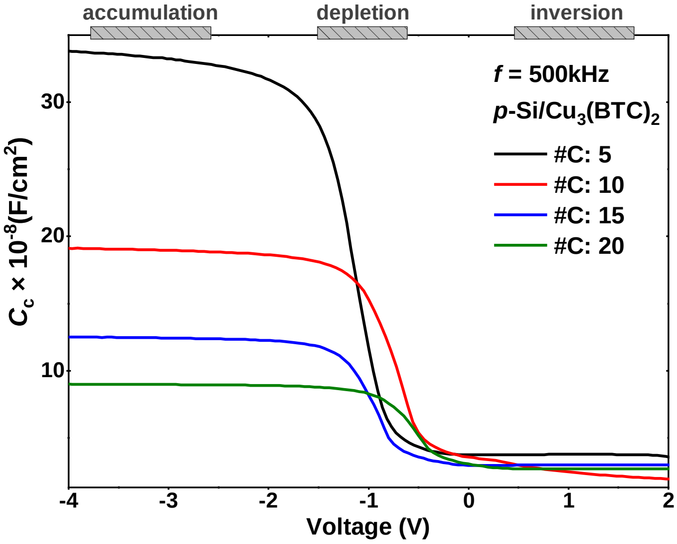


Figure 6.3 Capacitance-voltage characteristics for p-Si/$Cu_3(BTC)_2$/Al MIS capacitors measured in reverse mode at a fixed frequency of 500 kHz. The samples were synthesized by the spray-coating method using different numbers of spray cycles (#C). The dashed areas represent the accumulation, depletion, and inversion regimes.

Capacitance-voltage characteristics for ultra-thin $Cu_3(BTC)_2$ MOFs in reverse mode are shown in Figure 6.3. The C-V curves are measured at a fixed frequency of 500 kHz to avoid contributions of interface-trapped charges and border-trapped charges to the capacitance in the accumulation region. The MOFs were grown with the following number of spray cycles: 5 (black color), 10 (red color), 15 (blue color) and 20 (green color). The C-V curves exhibit the characteristics regimes of accumulation, depletion, and inversion typical for a functional capacitor. This verifies the successful integrations of $Cu_3(BTC)_2$ as a dielectric layer within MIS capacitors. Only in the case of the MOF prepared with 10 spray cycles deep depletion is observed.

Capacitance-voltage curve for an ideal capacitor without defects ($V_{FB}=\Phi_{ms}$, $D_{it}=0$, $N_{bt}=0$, $Q_{eff,ox}=0$) does not have hysteresis and the flat-band voltage is equal to the difference in work function between the metal and the semiconductor. Deviation of the capacitance curves in Figure 6.3 from the ideal one arises from different sources. (1) Fixed positive/negative charges; these charges shift the capacitance curve towards negative/positive voltages. The shift of the *C*-*V* curve could be associated with positive charges existing in the copper atoms of the framework or with negative charges existing in the BTC linker [115,116]. (2) Interface traps at the $Cu_3(BTC)_2$/Si, which produce a small stretch-out around the depletion region of the capacitance curve. (3) Border traps; which lead to the formation of hysteresis after the forward and reverse sweep (see Figure 6.7) [54,117].

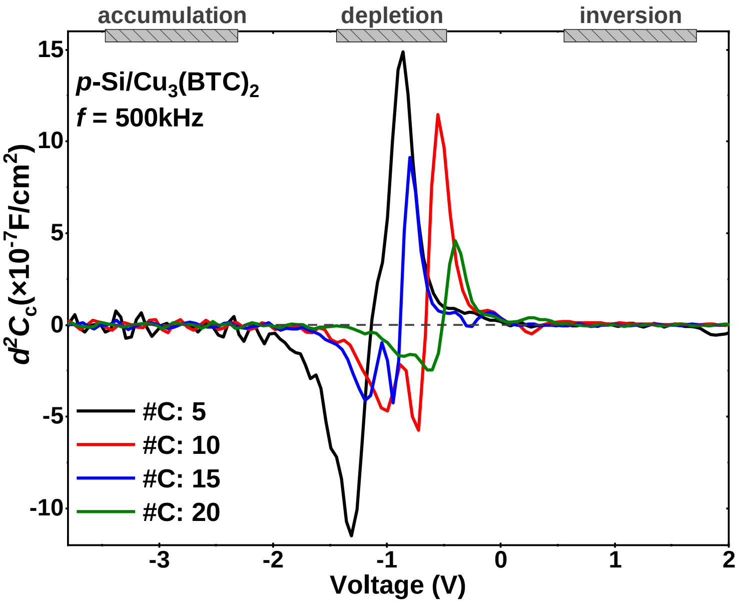


Figure 6.4 Second derivative of the corrected capacitance versus gate voltage for *p*-Si/$Cu_3(BTC)_2$/Al MIS capacitors measured in reverse mode at a fixed frequency of 500 kHz. The intersection of the curves with the voltage axis leads to the experimental flat-band voltage.

Experimental flat-band voltage, $V_{FB,exp}$, of the capacitors were retrieved using the method proposed by Winter *et al.* [105]. Figure 6.4 shows the second derivative of the capacitance curves versus gate voltage for $Cu_3(BTC)_2$ films grown with 5, 10, 15, and 20 spray cycles. The intersection of d^2C_c/dV^2 with the voltage axis gives flat-band voltage values of: $V_{FB,exp}$ =-1.13 V (5 cycles), -0.66 V (10 cycles), -0.88 V (15 cycles), and -0.51 V (20 cycles). In section 5, a work function difference of $V_{FB,theor}$ = ~0.88 V was determined for the *p*-Si-SiO_2-Al system. Effective oxide charges were calculated as the difference between the theoretical and experimental flat-band voltage values giving $Q_{ox,eff}$ of: $+5.4\times10^{11}$ cm^{-3} (5 cycles), -2.7×10^{11} cm^{-3} (10 cycles), -3.4×10^{09} cm^{-3} (15 cycles), and -2.1×10^{11} cm^{-3}

(20 cycles). Note that $Cu_3(BTC)_2$ MOF exhibits both types of charges positive and negative. For thin MOF films, positive charges are predominant.

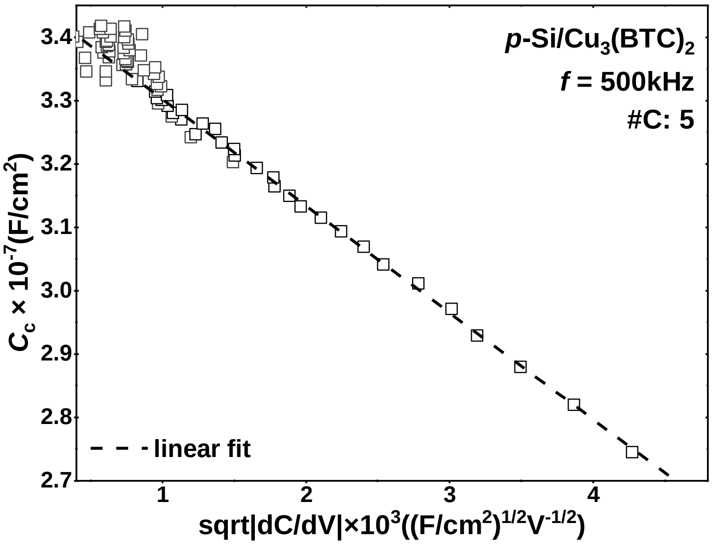


Figure 6.5 Capacitance curves in the McNutt-Sah representation model for *p*-Si/$Cu_3(BTC)_2$/Al MIS capacitor containing a MOF film coated with 5 spray cycles. The gray line represents a linear extrapolation to the capacitance curve.

Dielectric capacitance, C_d, was retrieved by the McNutt-Sah method [88]. In this approximation, C_d is determined from the accumulation region of the capacitance-voltage curve measured at high enough frequencies that the effect of interface traps and border traps are negligible ($f > 500$ kHz). Figure 6.5 depicts the capacitance curve for *p*-Si/$Cu_3(BTC)_2$/Al in the McNutt-Sah representation. The capacitor was measured at 500 kHz and contains a MOF film coated with 5 spray cycles. The capacitance shows a good linear behavior which is used for the determination of C_d. An extrapolation to the linear region leads to a dielectric capacitance of 3.5×10^{-7} F/cm^2. Assuming a dielectric constant of 2.3 [30], the calculated electrically extracted thickness, d_{MOF}, of the MOF was 5.9 nm. C_d and layer thickness for MOFs coated with 10, 15, and 20 are 1.9×10^{-7} F/cm^2 (10.5 nm), 1.3×10^{-7} F/cm^2 (15.0 nm), and 0.9×10^{-7} F/cm^2 (22.1 nm), respectively. d_{MOF} increases linearly with the number of spray cycles indicating that the spray-coating method offers good control of the layer thickness.

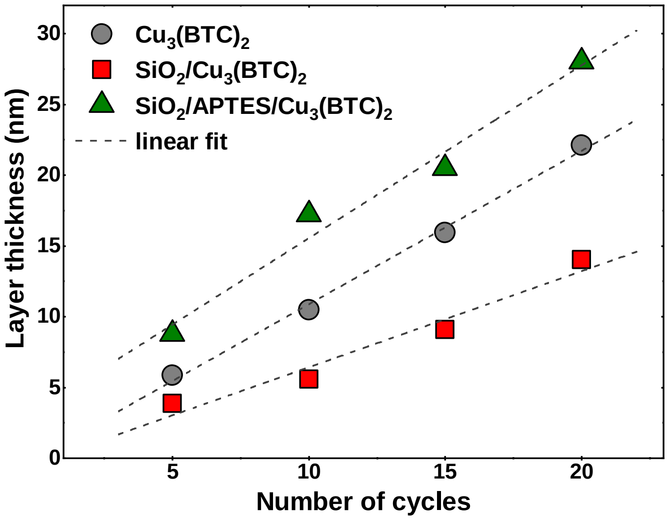


Figure 6.6 Layer thicknesses calculated from capacitance measurements using the McNutt-Sah method for ultra-thin $Cu_3(BTC)_2$ films growth directly on *p*-type silicon, *p*-Si/SiO_2 functionalized by APTES, and *p*-Si/SiO_2.

The crystal growth of $Cu_3(BTC)_2$ can occur along with the 1.5 nm d_{111} and/or 0.76 nm d_{222} crystal spacings. The step high of 1.5 nm d_{111} consists of two sub-layers of copper dimer connected to BTC linkers; this is the more stable crystal spacing because it leads lower free Cu sites and $-CO_2^-$ moieties than the d_{222} [81]. Atomic force microscopy measurements demonstrated that $Cu_3(BTC)_2$ layers prepared by the solvothermal method growth in steps of 1.5±0.1 nm associated with the 1.5 nm d_{111} crystal spacing and with steps highs of 0.8 nm, 2.2 nm and 3.0 nm associated with the 0.76 nm d_{222} crystal spacing [81,118]. In the case of ultra-thin $Cu_3(BTC)_2$ films ($d < 100$ nm) coated by the layer-by-layer method, a deposition of 1.143 nm per cycle was obtained [119]. A summary of the layer thickness versus the number of spray cycles for MOFs growth on silicon and silicon dioxide surfaces are shown in Figure 6.6. A linear extrapolation yields a deposition of approximately 1.1 nm per cycle (*p*-Si/$Cu_3(BTC)_2$/Al), 0.8 nm per cycle (*p*-Si/SiO_2/$Cu_3(BTC)_2$/Al), and 1.2 nm per cycle (*p*-Si/SiO_2/APTES/ $Cu_3(BTC)_2$/Al). The results are consistent with the values reported by Kim *et al.* [119] suggesting a slight reduction of the step growth around the d_{111} crystal spacing for ultra-thin $Cu_3(BTC)_2$ films.

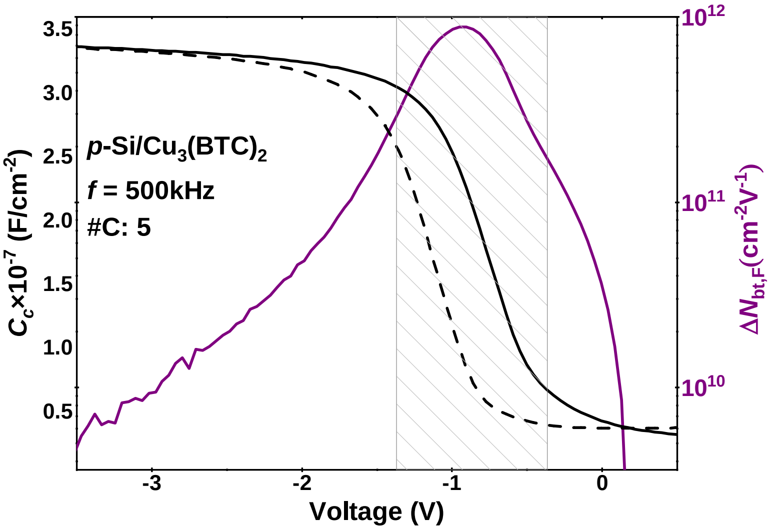


Figure 6.7 Total border trap density and capacitance-voltage curve measured at 500 kHz as a function of the applied gate voltage for p-Si/Cu$_3$(BTC)$_2$/Al MIS capacitor. The MOF layer was prepared with 5 spray cycles. The shadowed region represents the strongest contribution of border traps to the capacitance curve.

The effect of border traps in MOF-based MIS capacitors was evaluated from the hysteretic behavior of the *c*apacitance-voltage characteristic using the approximation of Fleetwood *et al.* [93]. Figure 6.7 shows *C*-*V* curves measured in forward (solid black line) and reverse (dashed black line) mode at 500 kHz and the extracted density of border traps (purple line) for p-Si/Cu$_3$(BTC)$_2$/Al capacitor containing a 5.9 nm thick Cu$_3$(BTC)$_2$.

The response of border traps is stronger in depletion region as is shown by the sharp broad peak with a maximum value around 2.12×10^{11} cm^{-2}. This value rapidly decreases and becomes negligible once the device reaches strong accumulation or inversion regimes. The strong contribution of $N_{bt,F}$ in depletion can be associated with the change of charge occupancy of donor-like or amphoteric border traps with the silicon band-edges due to the reduction of the majority carrier at the silicon surface. This effect is similar to that of interface states [87]. Nevertheless, border traps can respond in accumulation and inversion regions too, probably due to its large time response in comparison to interface traps.

Three mechanisms of charge transport in metal-organic frameworks were identified [6]. (1) through-bond conduction via the organic and inorganic components [120]. In this case, the covalent bonds of the framework serve as pathways for charge transport. (2) Through-bond conduction via guest molecules that can be infiltrated in the pores of the framework [121]. (3) Through-space conduction via charge delocalization. Here charge transfer occurs between adjacent linkers [122,123]. In Si/SiO_2/Al MIS capacitors, hysteresis occurs due to charge injection from the semiconductor into border traps located at the Si/SiO_2 interface (see Figure 5.1a). In contrast, the orientation of hysteresis in the *C*-*V* curve of $Cu_3(BTC)_2$ MOF (see Figure 6.7) indicates that injection of charges from the gate into border traps is the dominant process [124–126]. Thus, the activation of border traps in *p*-Si/$Cu_3(BTC)_2$/Al MIS capacitors can be explained in terms of through-bond tunneling and/or hopping transport. Where the hopping mechanism might occur through the BTC linkers or copper ions clusters [127,128].

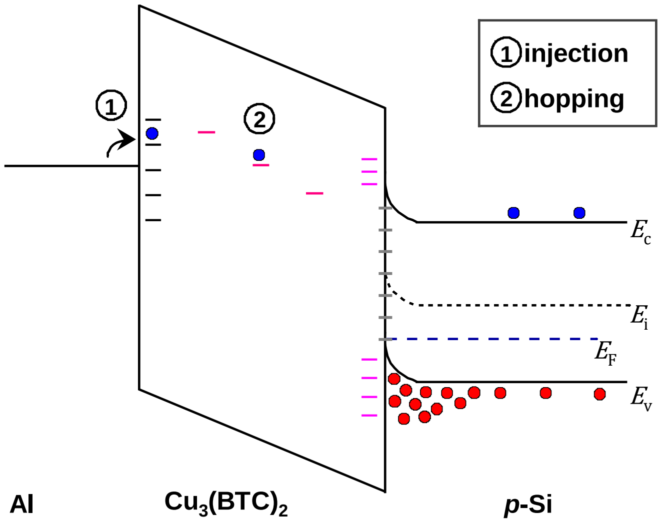


Figure 6.8 Schematic energy band diagram of the *p*-Si/$Cu_3(BTC)_2$/Al MIS capacitor under negative gate voltage (strong accumulation). The diagram shows the injection (1) and the hopping (2) processes that lead to the formation of hysteresis in the capacitance-voltage curves.

The schematic diagram of the band structure for *p*-Si/$Cu_3(BTC)_2$/Al MIS capacitor showing the charge transport mechanism in ultra-thin $Cu_3(BTC)_2$ film is depicted in Figure 6.8. First, the capacitor is biased under accumulation by applying a high negative voltage to the metal gate, this leads to the injection of charges into traps located near the Al/$Cu_3(BTC)_2$ interface (1). Afterward, electrons are transported via hopping through empty traps located between the bulk of the MOF until they reach the border traps located close to the MOF/Si interface and contributes either with positive or negative charges to the total effective oxide charges (2) [129,130]. In the case of the thinnest $Cu_3(BTC)_2$ sample (5 cycles, 5.9 nm), tunneling transport could be the most probable charge transport mechanism. In contrast, for thicker layers, the hopping process is the predominant one.

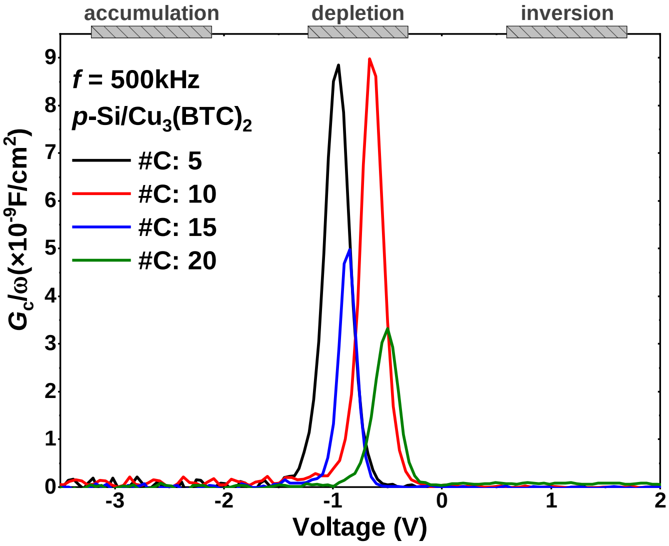


Figure 6.9 Conductance curve divided by angular frequency versus gate voltage after series resistance correction for p-Si/$Cu_3(BTC)_2$/Al MIS capacitors. The samples were coated with different numbers of spray cycles (#C). The measurements were carried out in reverse mode at a fixed frequency of 500 kHz. The dashed areas represent the accumulation, depletion, and inversion regions.

The effect of interface traps in MOF-based MIS capacitors is evaluated from the peak of the conductance curves that occurs due to the change in occupancy between interface traps and the silicon band-edges. Conductance characteristics divided by the angular frequency for ultra-thin $Cu_3(BTC)_2$ MOFs measured in reverse mode at 500 kHz are shown in Figure 6.9. MOFs were grown with 5 (black color), 10 (red color), 15 (blue color), and 20 (green color) spray cycles. It was demonstrated that border traps influence the accumulation, depletion, and inversion regions of the C-V curve (see Figure 6.7). In contrast, the response of interface traps occurs only in depletion region as is shown in Figure 6.9. In order to determine the density of interface traps, the G_c curves were divided by the angular frequency. Then $D_{it,HC}$ is determined from the maximum peak of the G_c/ω curve using the Hill-Coleman approximation. Low $D_{it,HC}$ values of 2.2×10^{11} $eV^{-1}cm^{-2}$(5 cycles), 3.5×10^{11} $eV^{-1}cm^{-2}$(10 cycles), 2.3×10^{11} $eV^{-1}cm^{-2}$(15 cycles), and 2.4×10^{11} $eV^{-1}cm^{-2}$(20 cycles) were obtained. The $D_{it,HC}$ values are slightly lower than SiO_2-based MIS capacitors and are comparable with other inorganic materials [131,132].

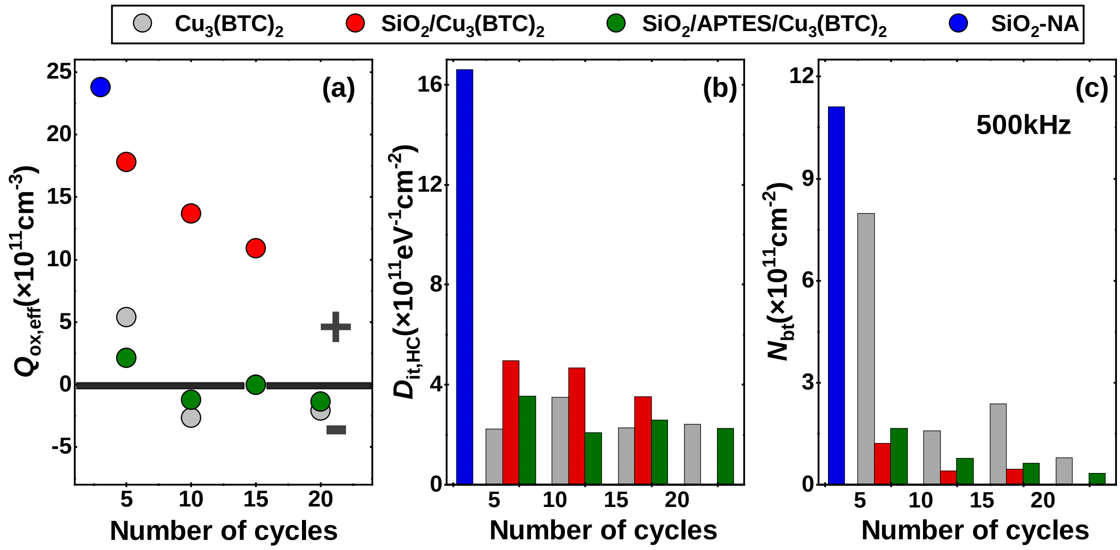


Figure 6.10 Effective oxide charge density $Q_{ox,eff}$ (a), density of interface traps $D_{it,HC}$ (c), and density of border traps $N_{bt,F}$ (c) determined from capacitance-voltage and conductance-voltage curves measured at 500 kHz. Thin $Cu_3(BTC)_2$ films were grown using 5, 10, 15, and 20 spray cycles directly on silicon, on SiO_2 alone, and on SiO_2 functionalized by APTES. Electrical parameters of non-anneal 10 nm thick SiO_2-capacitor is included for comparison reasons.

Figure 6.10 summarizes the effective oxide charges and defect trap density for all MOF-based MIS devices including the data for *p*-Si/SiO_2/Al (non-annealed capacitor). Density of border traps and interface traps were calculated using the Fleetwood and Hill-Coleman approximations, respectively. Effective oxide charge density in SiO_2-based capacitor is negative while in $Cu_3(BTC)_2$-based capacitors it can be either positive or negative. It seems that $Q_{ox,eff}$ is influenced by the layer thickness of the MOF and it becomes negative for thicker samples (d >5 nm). In the case of *p*-Si/$Cu_3(BTC)_2$/Al MIS capacitors, fixed charges might be the major contribution to $Q_{ox,eff}$ indicating that both fixed positive and negative charges can be formed due to the organic and inorganic components, respectively (see Figure 6.10a). The incorporation of $Cu_3(BTC)_2$ in SiO_2 compensates the positive $Q_{ox,eff}$ of the stack. Surface functionalization of the SiO_2 through APTES decreases further the positive $Q_{ox,eff}$.

$Cu_3(BTC)_2$-based MIS capacitors exhibit slightly lower interface trap density in comparison to SiO_2 alone while border trap density reduces up to one order of magnitude. In SiO_2-based MIS capacitors, defects at the Si/SiO_2 interface are reduced by post-annealing treatments. For instance, firing steps only reconstruct the distorted silicon lattice while forming gas annealing offers chemical passivation due to the diffusion of atomic hydrogen toward the Si/SiO_2 interface [109]. In $Cu_3(BTC)_2$-based capacitors chemical passivation might be related to the saturation of oxygen vacancies located in the MOF layer by hydrogen atoms coming from the carboxylate unit of the linker component.

On the other hand, in dielectric stacks containing Al_3O_2 or SiN_x as capping layer, firing can also saturate dangling bonds by atomic hydrogen released from the capping layer [133–136]. Hydrogen species are introduced during the deposition process of Al_3O_2 or SiN_x and the release of hydrogen and other species such as oxygen was demonstrated by effusion measurements [137]. The effect of firing process varies depending on the material. In SiO_2/SiN_x, a density of interface states up to $\sim 3\times10^{12}$ $eV^{-1}cm^{-2}$ was achieved [109]. Density of interface traps was further reduced for the SiO_2/Al_3O_2 stacking dielectric ($D_{it} < 10^{11}$ $eV^{-1}cm^{-2}$). The excellent passivation of the capping Al_3O_2 layer was attributed to the thermal stability of the stack and the effective transport of hydrogen within the SiO_2 toward the Si interface. Reduction of defect trap density in $Cu_3(BTC)_2$-based MIS capacitors can be explained in the following way: (1) dissociation of HO groups from the carboxylic groups of the TMA, then (2) hydrogen atoms are adsorbed at the Si/SiO_2 interface and passivate dangling bonds mainly located in the oxide layer rather than at the interface.

6.3.2 *Effect of Frequency*

Capacitance-voltage and conductance-voltage curves were measured over a wide frequency range to determine a more reliable density of interface traps using the conductance method. Additionally, this method offers information about interface trap response. Figure 6.11 compares the frequency dispersion of the capacitance-voltage characteristics for *p*-Si/$Cu_3(BTC)_2$/Al (a), *p*-Si/SiO_2/$Cu_3(BTC)_2$/Al (b), and *p*-Si/SiO_2/APTES/$Cu_3(BTC)_2$/Al (c) MIS capacitors measured in reverse mode at several frequencies varying between 5 kHz to 500 kHz. MOFs were coated with a different number of spray cycles but contain near similar layer thickness that allows comparison between them.

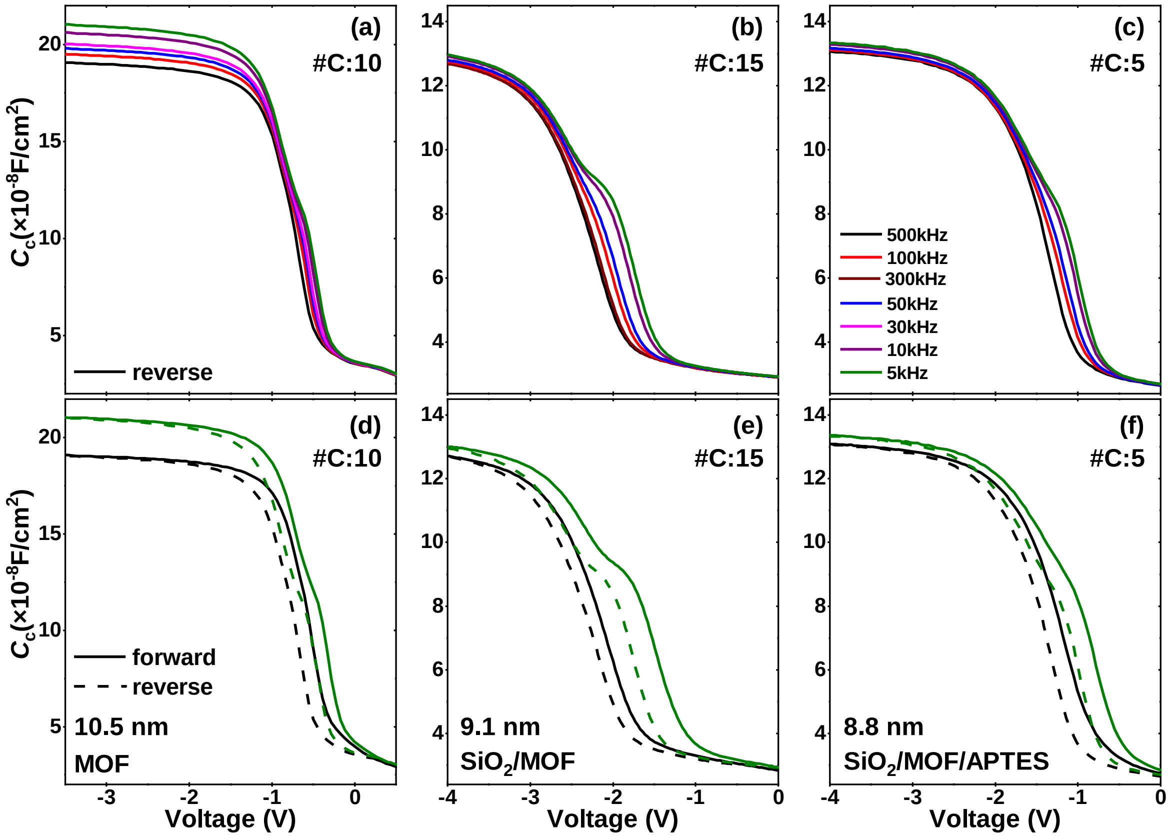


Figure 6.11 Capacitance-voltage characteristics for MOF based MIS capacitors measured at frequencies varying from 3 kHz to 500 kHz. Thin $Cu_3(BTC)_2$ films were grown directly on silicon (a)(d), on SiO_2 surfaces (b)(e), and on SiO_2 functionalized by APTES (c)(f). MOFs were grown with different number of spray-cycles, but possess similar layer thicknesses that allow comparison between them.

Layer thicknesses and border trap density were extracted from the capacitance-voltage curve measured at 500 kHz using the McNutt-Sah and Fleetwood methods, respectively. The retrieved d_{MOF} and $N_{\mathrm{bt,F}}$ are found to be 10.5 nm (1.56×10^{11} cm^{-2}), 9.1 nm (4.4×10^{10} cm^{-2}), and 8.8 nm (1.64×10^{11} cm^{-2}) for capacitors shown in (a), (b), and (c), respectively. The capacitors have nearly similar series resistance values between 0.07-0.08 Ωcm^{-2}. Density of interface traps remains almost constant in the range of: 3.5-3.6×10^{11} eV^{-1}cm^{-2}.

In chapter 5, it was shown that post-annealing treatments under forming gas atmosphere of SiO_2-based MIS capacitors reduce considerably the amount of interfacial defects. Therefore, capacitance-voltage curves do not depend on frequency. Quite opposite, non-annealed capacitors contain a high density of interfacial defects and thus capacitance curves in depletion regime strongly depend on the frequency. Capacitance-voltage curves of the capacitor containing only $Cu_3(BTC)_2$ display small variation in depletion but higher frequency dispersion in accumulation meanwhile hysteresis remains constant for all frequencies (see Figure 6.11d). Frequency dispersion in accumulation is improved for the $SiO_2/Cu_3(BTC)_2$ stack. However, border traps are unstable and induce an increase of hysteresis and humps upon decrease of frequency (see Figure 6.11e). Surface functionalization of SiO_2 with APTES stabilizes the hysteresis which becomes constant again at each frequency.

Dispersion in accumulation is associated with interfacial layer due to the formation of oxygen-related bonds (O-bonds) between the substrate and the dielectric material. For example, in the case of HfO_2 (~7.4 nm thick) grown on GaAs substrate, the formation of As-O and Ga-O bonds were revealed by X-ray photoelectron spectroscopic analysis [138,139]. These bonds introduce defect states in the band gap of the semiconductor and degrade the electrical properties of the capacitor. Formation of interfacial layer is usually improved by incorporating a thin dielectric layer (~1.6 nm thick) between the gate dielectric and the substrate [138]. On the other hand, dispersion in depletion is attributed to tunneling of carriers into interface traps and border traps [140–142]. Contribution of interfacial defects on the *C-V* characteristics of the MOF-based MIS devices is demonstrated by the presence of hysteresis in the capacitance curves and humps that appears in depletion region. The humps increase as soon as the frequency decreases because interfacial defects easily follow the AC signal at low frequencies. According to the experimental results, it seems to be that frequency dispersion in accumulation and depletion regions is affected by both interface traps and border traps. The major contribution to the dispersion in accumulation regime can be attributed to border traps and it is slightly reduced by the incorporation of SiO_2 layer.

Density of interface traps is determined from conductance curves measured as a function of voltage and frequency. First, the measured conductance, G_{m} (black line) was corrected from series resistance resulting in the corrected conductance, G_{c} (red line) as shown in Figure 6.12a for the case of $Cu_3(BTC)_2$ grown directly on a silicon wafer. It can be seen that series resistance influences accumulation and depletion regimes of the conductance curve, therefore, R_s was extracted from all impedance measurements to get reliable $D_{it,cond}$ values. After that, equivalent parallel conductance, G_{pc} (grey dots) was calculated by subtracting the reactance of the dielectric capacitance using the model proposed by Nicollian (see Figure 6.12a). The maximum peak value of G_c/ω-V (9.0×10^{-09} F/cm^2) is lower than G_{cp}/ω-V (3.2×10^{-08} F/cm^2) because C_d induces a short time constant. Therefore G_{pc}/ω-V will lead higher but accurate density of interface trap.

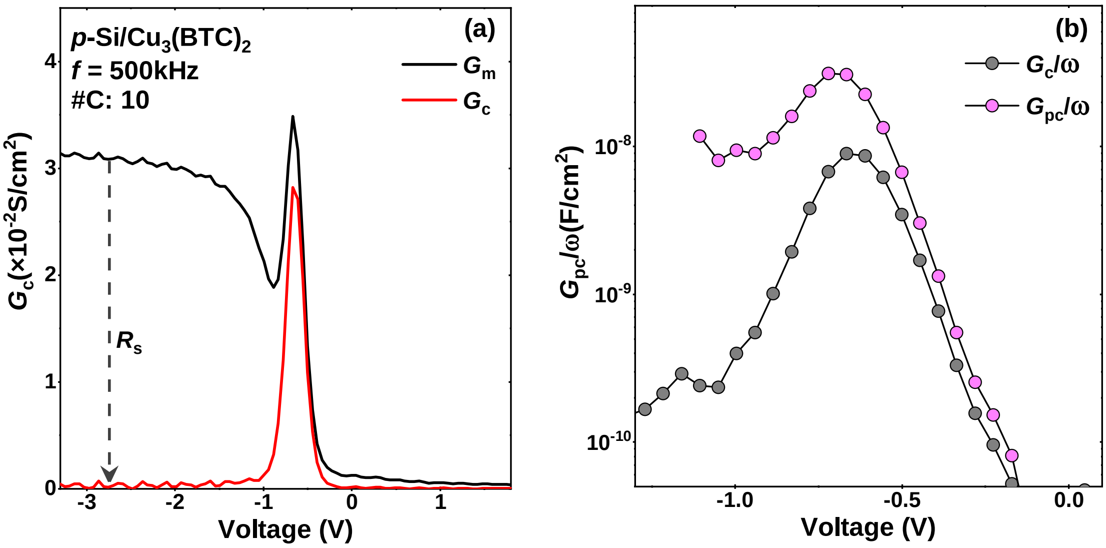


Figure 6.12 Measured (G_m) and corrected (G_c) conductance after series resistance subtraction (a). Corrected conductance (G_c/ω) and equivalent parallel conductance (G_{pc}/ω) as a function of angular frequency for *p*-Si/$Cu_3(BTC)_2$/Al MIS capacitor.

G_{pc}/ω-ω curves were constructed from the G_{pc}/ω-V curves at different voltages around depletion region. Figure 6.13 shows equivalent parallel conductance curves as a function of angular frequency for MIS capacitors containing $Cu_3(BTC)_2$ (a) and $SiO_2/Cu_3(BTC)_2$ (b) as dielectric layer. G_{pc}/ω-ω curves were retrieved at different gate voltage values and exhibit a single plateau shape indicating contribution only due to interface traps. The maximum peak value each curve were determined by fitting the experimental data with a single Gaussian distribution peak. Ultra-thin $Cu_3(BTC)_2$ films exhibit time response and density of interface traps varying between ~7.3 µs (~5.0×10^{11} eV^{-1}cm^{-2}) to ~4.3 µs (~5.6×10^{11} eV^{-1}cm^{-2}) extracted at -0.50 V and -0.67 V, respectively. In the case of $SiO_2/Cu_3(BTC)_2$ dielectric stack the following values were found: ~39 µs (~8.1×10^{11} eV^{-1}cm^{-2}) to ~12 µs (~6.8×10^{11} eV^{-1}cm^{-2}) extracted at -2.18 V and -2.30 V, respectively. $D_{it,cond}$ values are higher than $D_{it,HC}$ since the Hill-Coleman method uses the G_c/ω curve instead of G_{pc}/ω. Higher dispersion in depletion region of the $SiO_2/Cu_3(BTC)_2$ dielectric stack could be attributed to the large time response of interface traps in comparison to $Cu_3(BTC)_2$ alone (see Figure 6.11b).

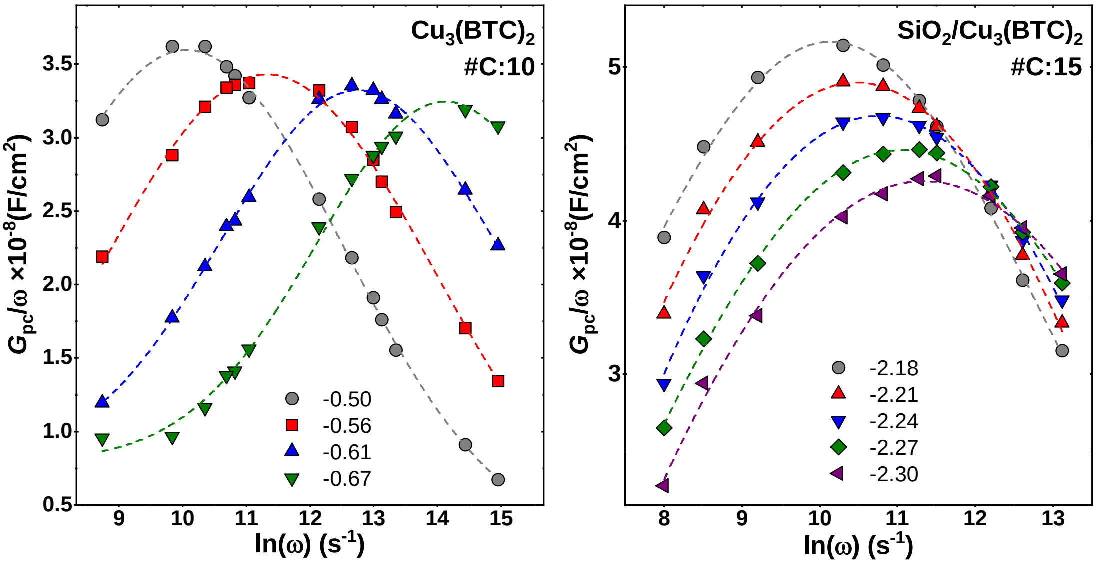


Figure 6.13 Equivalent parallel conductance as a function of angular frequency for MOFs based MIS capacitors. Thin $Cu_3(BTC)_2$ films were grown using 10 spray cycles directly on silicon (a) and on SiO_2 (b). Density of interface traps was determined by fitting the G_{pc}/ω-ω curve with a single Gaussian function (dotted lined). The dots indicate the voltage at which the G_{pc}/ω-ω curve was extracted.

6.3.3 Effect of Temperature

Heating experiments were performed in order to remove moisture from the pores of the MOFs which allows the extraction of the electrical properties of the empty MOF. The samples were heated during the measurements from room temperature to 100 °C and then cooled down to room temperature in steps of ten degrees Celsius. In every step, capacitance-voltage curves were retrieved in forward and reverse mode at a fixed frequency of 100 kHz. Figure 6.14 shows temperature-dependent capacitance-voltage curves for *p*-Si/SiO_2/APTES/$Cu_3(BTC)_2$/Al MIS capacitor containing a MOF layer coated with 15 spray cycles. Upon increment of temperature, the accumulation capacitance decreases in each temperature step. In depletion region, capacitance curve measured in forward mode remains nearly constant up to ~50 °C, after that, the *C*-*V* curve shifts towards the positive gate voltage axis (see Figure 6.14a). Additionally, the stretch-out around depletion increases indicating an increase of interface trap density.

In the case of measurements performed in reverse mode (see Figure 6.14b), capacitance-voltage curves shift toward negative voltage values and thus hysteresis becomes large as well as the flat-band voltage because of an increment of interface traps density and effective charge density, respectively. N_{bt} determined from the *C*-*V* hysteresis and $Q_{\mathrm{ox,eff}}$ values increase from $+2.4\times10^{11}$ cm^{-3} (6.4×10^{10} cm^{-2}, RT) to $+3.7\times10^{11}$ cm^{-3} (3.5×10^{11} cm^{-2}, 100 °C).

On the other hand, up to 40 °C, $D_{\mathrm{it,HC}}$ remains almost the same 2.9 - 3.2×10^{11} $\mathrm{eV}^{-1}\mathrm{cm}^{-2}$. For temperatures higher than 50 °C, another interfacial trap also contributes to the conductance curve, therefore, the extraction of $D_{\mathrm{it,HC}}$ was not viable. The response of the other interfacial trap is demonstrated by the shoulder that appears in depletion region of the conductance-voltage curve and becomes stronger for temperatures higher than 50 °C (see Figure A-6.2). This shoulder can be associated with the response of border traps which influence strongly the impedance measurements as is revealed by the broad hysteresis that occurs at 100 °C (see Figure 6.15). Contribution of border traps to the conductance curve was also reported for the case of inorganic materials [143–145]. Increase of $Q_{\mathrm{ox,eff}}$ could be related to an increase in positive fixed charges while border and interface traps are activated by temperature. Overall results demonstrate an increase in defect density, interface traps and border traps, upon an increment of temperature. This can be connected with the depassivation of dangling bonds near and at the Si/SiO_2 interface. Increase of positive charges could be related to the increase of copper-related vacancies that contribute with positive charges to the SiO_2/$Cu_3(BTC)_2$ stack.

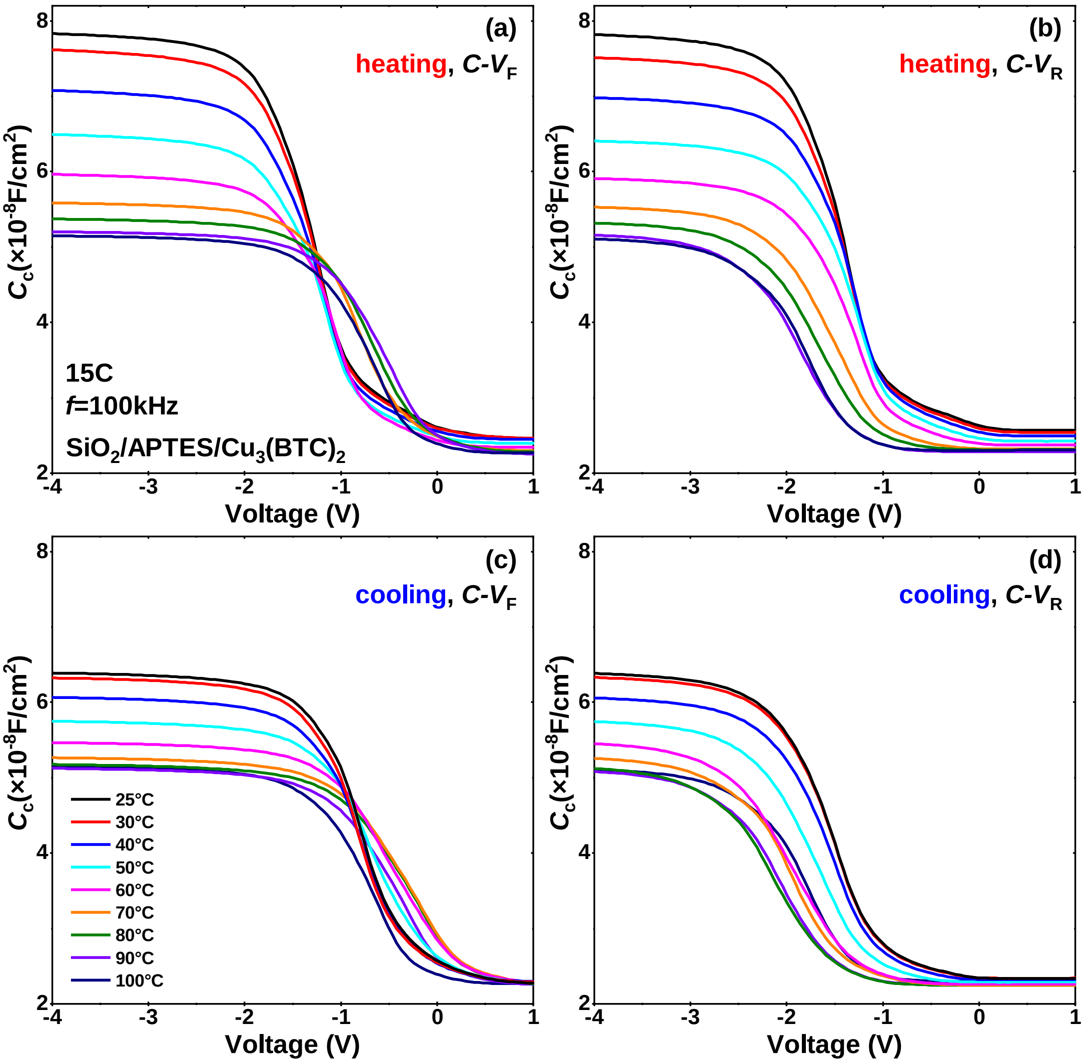


Figure 6.14 Capacitance-voltage curves measured at 100 kHz in forward (C-V_F) and reverse (C-V_R) mode upon heating (a)(b) and cooling (c)(d) experiments for p-Si/SiO$_2$/APTES/Cu$_3$(BTC)$_2$/Al MIS capacitor containing a MOF layer coated with 15 spray cycles.

Capacitance-voltage curves upon cooling experiments measured in reverse mode at 100 kHz for p-Si/SiO$_2$/APTES/Cu$_3$(BTC)$_2$/Al MIS capacitor are depicted in Figure 6.14c and d. The accumulation capacitance increases ones the temperature decreases. Note that the change of accumulation capacitance in each temperature step is slower than in the case of heating experiments. There is also a slightly recovering of the capacitance in depletion region. The improvement of defect density might be correlated with the adsorption of hydrogen atoms. It seems to be that adsorption of hydrogen atoms is favor at low temperature.

Figure 6.15 depicts capacitance-voltage curves for *p*-Si/SiO_2/APTES/$Cu_3(BTC)_2$/Al MIS capacitor measured in forward (solid line) and reverse (dotted line) mode. Before heating experiments, a small hysteresis in the *C-V* curve was observed (red color) and the capacitor exhibits density of interface traps and border traps of 2.8×10^{11} $eV^{-1}cm^{-2}$ and 6.4×10^{10} cm^{-2}, respectively. Heating the capacitor from room temperature to 100 °C and cooling down to room temperature again causes large hysteresis in the *C-V* curve, signifying an increment of border traps (3.1×10^{11} cm^{-2}). The results indicate degradation of the MOF layer under bias stress for temperatures higher than 100 °C.

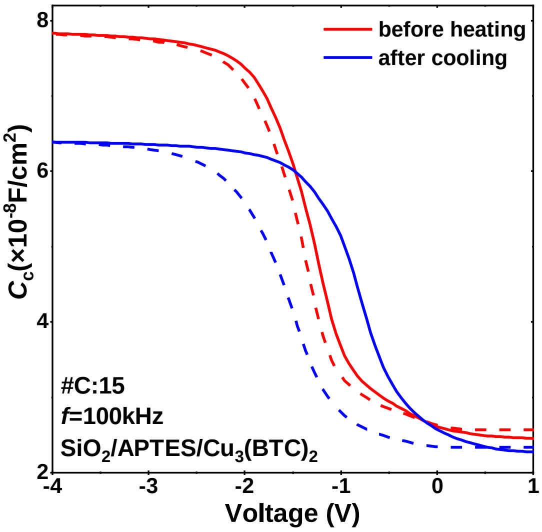


Figure 6.15 Forward (solid line) and reverse (dotted line) capacitance-voltage curves before heating and after cooling experiments for *p*-Si/SiO_2/APTES/$Cu_3(BTC)_2$/Al MIS capacitor containing a MOF layer coated with 15 spray cycles.

Figure 6.16 shows the accumulation capacitance (C_{acc}) as a function of temperature. C_{acc} was retrieved in strong accumulation regime at a gate voltage of -4.0 V. C_{acc} values decreases from 7.8×10^{-08} Fcm^{-2} to 5.1×10^{-08} Fcm^{-2} (red circles). This indicates the unloading of potential molecules from the pores of the $Cu_3(BTC)_2$ layer resulting in a decrease of the dielectric constant [30]. Upon cooling, the accumulation capacitance slightly increases up to 6.4×10^{-08} Fcm^{-2} due to the loading of guest molecules again. Note that upon heating/cooling experiments, $Cu_3(BTC)_2$ is very sensitive to humidity conditions. Nevertheless, only a recovering of 82 % of the accumulation capacitance was obtained. This indicates that electrical properties of $Cu_3(BTC)_2$ degrade after heating and thus after cooling experiments the initial state is not attained again.

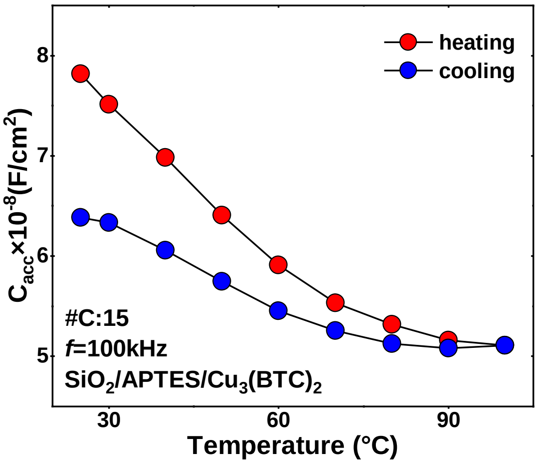


Figure 6.16 Accumulation capacitance as a function of temperature for p-Si/SiO$_2$/APTES/Cu$_3$(BTC)$_2$/Al MIS capacitor. $C_{c,acc}$ values were extracted at a gate voltage of -3.4 V from C-V curves measured at 100 kHz.

6.4. Impedance Characteristics of $Cu_3(BTC)_2$ on *n*-type Silicon

This section presents a brief description of the electrical properties for ultra-thin Cu$_3$(BTC)$_2$ films coated on *n*-type Si substrates. The procedure for the determination of electrical parameters is the same as in the case of MOFs grown on *p*-type Si substrates. First, the MOF layer thickness was determined using the McNutt-Sah method, by extrapolating the linear region of the capacitance-voltage curves. The following dielectric capacitance and layer thickness values were extracted: 2.1×10^{-7} F/cm^2 (3.7 nm), 5.6×10^{-7} F/cm^2 (5.6 nm), 1.5×10^{-7} F/cm^2 (7.8 nm), and 7.7×10^{-7} F/cm^2 (20.1 nm) for MOFs coated with 5, 10, 15, and 20 spray cycles, respectively. d_{MOF} values are comparable to samples fabricated on *p*-type Si substrates demonstrating that the growth of MOFs is slower on SiO$_2$ surfaces than on Si or on SiO$_2$ functionalized by APTES.

Figure 6.17 shows the capacitance-voltage and conductance-voltage curves measured in forward (solid curve) and reverse (dotted curve) mode at 500 kHz for MOF layers prepared with 5, 10, 15, and 20 spray cycles. In comparison to *p*-Si/SiO$_2$/Cu$_3$(BTC)$_2$/Al MIS capacitor, capacitance-voltage curves for MOFs grown on *n*-type Si exhibits low flat-band voltage values leading to low effective oxide charges of: $Q_{ox,eff}$ $=+2.5\times10^{11}$ cm^{-3} (5 cycles), -1.5×10^{10} cm^{-3} (10 cycles), $+8.3\times10^{09}$ cm^{-3} (15 cycles), and -1.1×10^{11} cm^{-3} (20 cycles). The orientation of hysteresis is also similar to MOF coated on *p*-type Si indicating that injection of charges from the gate metal is the predominant process. C-V curves exhibit small hysteresis indicating a low density of border traps which varies between 1.5×10^{10} cm^{-2}(20 cycles) to 9.1×10^{10} cm^{-2}(15 cycles). On the other hand, density of interface traps determined with the Hill-Coleman method varies from 3.8×10^{11} $eV^{-1}cm^{-2}$(20 cycles) to 6.7×10^{11} $eV^{-1}cm^{-2}$(5 cycles).

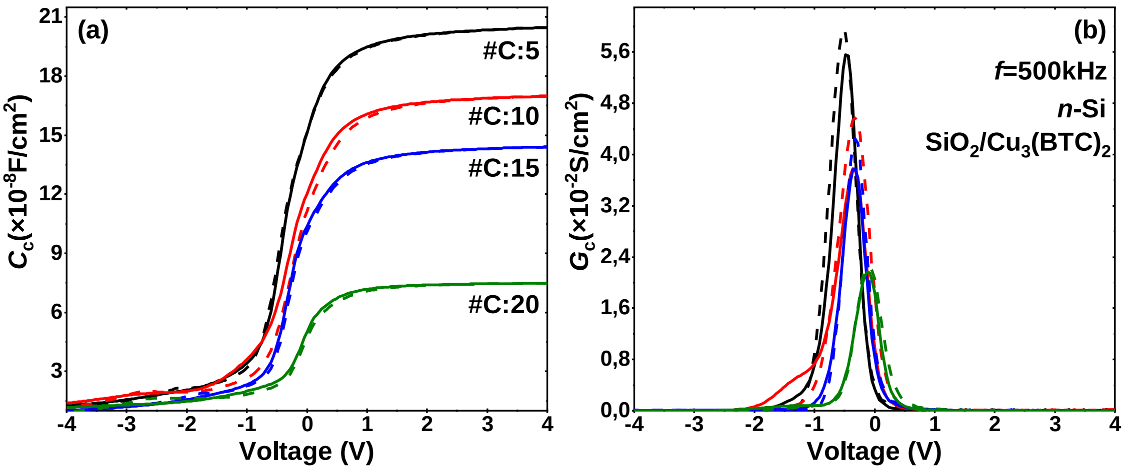


Figure 6.17 Capacitance-voltage (a) and conductance-voltage (b) curves for $Cu_3(BTC)_2$ MIS capacitors fabricated on *n*-type silicon substrate measured from forward (solid line) to reverse (dotted line) bias at a fixed frequency of 500 kHz. The samples were synthesized by the spray-coating method using different numbers of spray cycles (#C).

$SiO_2/Cu_3(BTC)_2$ dielectric stack on *n*-type Si presents lower flat-band voltage shift than on *p*-type Si, therefore, there is a considerable reduction of effective oxide charges. On the other hand, there is a slight decrease on border trap density, but an increase in interface trap density.

Frequency-dependent capacitance-voltage and conductance-voltage measurements are shown in Figure 6.18. In the case of the capacitance-voltage curve, frequency dispersion is low in accumulation, but high in depletion region. Additionally, the magnitude of hysteresis increases one frequency decreases, implying a strong dependence of border traps on the frequency. Similarly, for low frequency, the peak intensity of the conductance-voltage curve increases. This behavior is attributed to the ability of interface traps to follow easily the AC signal at low frequencies.

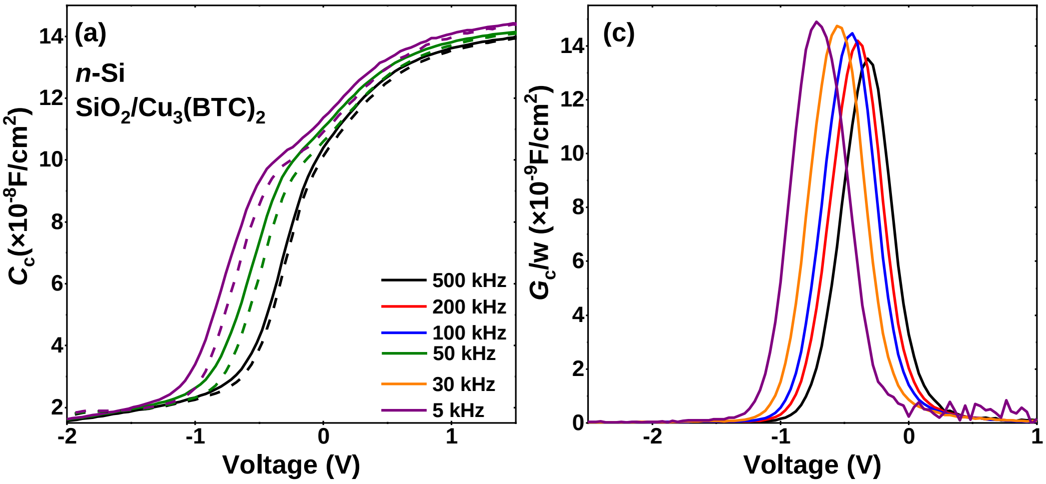


Figure 6.18 Multi-frequency capacitance-voltage (a) and conductance-voltage (b) curves for $Cu_3(BTC)_2$ fabricated on *n*-type silicon substrate.

Figure 6.19 (a) shows the equivalent parallel conductance versus angular frequency for *n*-Si/SiO_2/$Cu_3(BTC)_2$/Al MIS capacitor containing a MOF layer coated with 5 spray cycles. G_{cp}/ω- curves were constructed for a wide variety of gate voltage values around depletion region. The experimental data are very well fitted using a single Gaussian distribution (dotted line) and gives a density of interface traps around 1×10^{12} $eV^{-1}cm^{-2}$. The advantage of the conductance method over the Hill-Coleman method is that it offers a distribution of $D_{it,cond}$ within the bandgap of the silicon as is shown in Figure 6.19 (b). Precise distribution of the $D_{it,cond}$ around the Si bandgap can be obtained by determining the surface potential from quasi-static *C*-*V* measurements. Figure 6.19 (c) shows the time response of interface traps versus gate voltage. It can be seen that an increase in τ_{it} increases the $D_{it,cond}$ values.

Chapter 5 demonstrates that the interfacial properties of Si/SiO_2/Al MIS capacitor on *n*-type Si are better than on *p*-type Si. Therefore, an improvement of the interfacial properties of the SiO_2/$Cu_3(BTC)_2$ stack on *n*-type Si can be expected. Nevertheless, MOF-based MIS capacitors on *n*-type Si substrates exhibit only an improvement of effective oxide charge density, but border trap and interface trap densities remain in the same order. This result indicates that the type of substrate little influence N_{bt} and D_{it}.

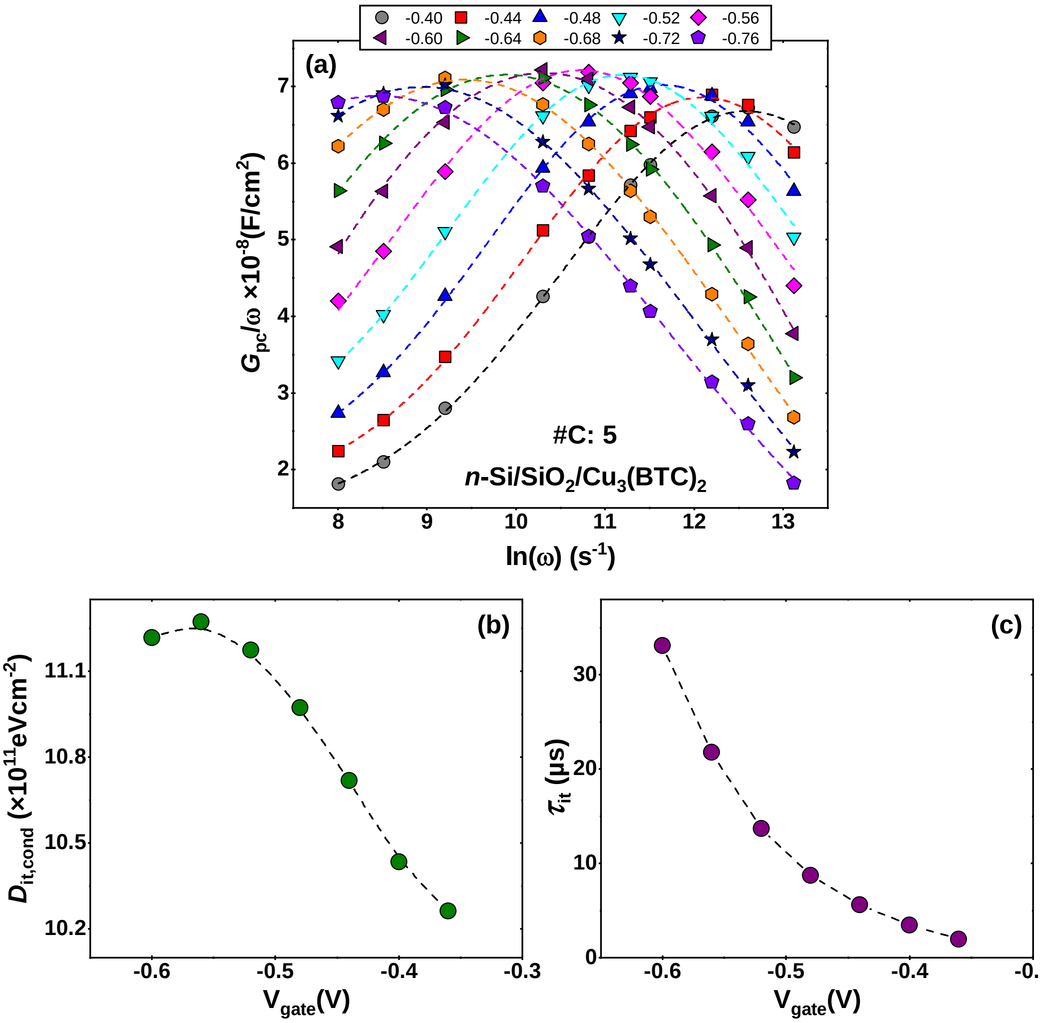


Figure 6.19 Equivalent parallel conductance versus angular frequency (a), density of interface traps (b), and interface trap response (c) calculated at different gate voltages near depletion region for $Cu_3(BTC)_2$ fabricated on *n*-type silicon substrate. Dots in (a) indicate the voltage at which the G_{pc}/ω-ω curve was extracted.

6.5 Summary

This section demonstrates the feasibility of integrating ultra-thin MOF films within MIS capacitor structures. Layer thickness varies from 3.9 nm up to 28.0 nm for MOF coated on SiO_2 surfaces and on SiO_2 functionalized with APTES, respectively. Depending on the layer thickness, fixed charges in ultra-thin $Cu_3(BTC)_2$ films can be negative or positive. Generally, MOF layers prepared with more than 10 spray cycles exhibits fixed negative charges. The capacitors also present a relatively low density of interface traps and border traps. According to the orientation of hysteresis in the capacitance curve, it can be concluded that charge transport mechanism in MOF-based capacitors consists of the combination of two processes. First, injection of carriers from the metal gate to border located near the Al/MOF interface and then transport of carriers within the MOF via through-bond hopping transport. The lowest (3.2×10^{10} cm^{-2}, #C:20) and the highest (8.0×10^{11} cm^{-2}, #C:5) density of border trap values were found for SiO_2/APTES/$Cu_3(BTC)_2$ stack and $Cu_3(BTC)_2$ alone, respectively. In the case of interface trap density, the lowest (2.1×10^{11} $eV^{-1}cm^{-2}$, #C:10) and the highest (5.0×10^{11} $eV^{-1}cm^{-2}$, #C:5) density of border trap values were found for SiO_2/APTES/$Cu_3(BTC)_2$ and SiO_2/$Cu_3(BTC)_2$ stacks, respectively. Interface traps and border traps cause frequency dispersion in the accumulation and depletion regimes of the capacitance curve which are comparable to the non-annealed SiO_2-based MIS capacitors. On the other hand, the SiO_2/$Cu_3(BTC)_2$ stack on *n*-type Si shows improved effective oxide charges than samples prepared on *p*-type Si, but there is no significant variation in density of interface trap and border trap.

Temperature-dependent measurements demonstrate the possibility of unloading/loading of moisture and potential molecules. Nevertheless, heating experiment causes degradation of the electrical properties of the device. This is demonstrated by the large hysteresis that appears in the *C*-*V* curve after cooling the capacitor from 100 °C down to room temperature. Therefore, it is not advisable to heat the capacitors at temperatures higher than ~80 °C.

7 Ultra-Thin $Cu_3(BTC)_2$ Films Based MIS Capacitors: Layer-by-Layer Approach Assisted by Ultrasonication

7.1 Introduction

In the last chapter, ultra-thin $Cu_3(BTC)_2$ MOF films coated by the spray-coating method with different layer thicknesses were incorporated into MIS capacitor structures using *p*-type and *n*-type silicon (100) as substrates. The capacitors demonstrated promising electrical properties even when the coating of the MOFs was performed by hand. An alternative procedure to improve further the electrical quality of the layer could be the layer-by-layer synthesis assisted by ultrasonication [11,83]. In this deposition method, the substrate is immersed in the metal and linker solution using a dipping robot. Furthermore, ultrasonication is switched on, when the substrate is immersed in pure ethanol. The coating process consists of the following steps: (1) immersion in the metal solution, (2) ultrasonic bath in ethanol, (3) immersion in the linker solution, and (4) ultrasonic bath in ethanol again. Thin film MOFs produced by this technique are called surface-mounted metal-organic frameworks (SURMOFs). The quality of the SURMOFs was evaluated by different analytical techniques that demonstrate the following improved characteristics: growth of highly oriented SURMOFs films [11], smooth and homogeneous surface that does not scatter visible light [30,146], transparent layers with slightly turquoise color and low defect density [31]. The following chapter is dedicated to investigate the influence of ultrasonic steps on the layer-by-layer synthesis of SURMOFs by electrical measurements.

Ultra-thin $Cu_3(BTC)_2$ MOF films were prepared at the Institut für Funktionelle Grenzflächen (IFG) in Karlsruhe and part of the results are published in reference [15]. The capacitors were fabricated on boron-doped *p*-type silicon (100) substrates. First, 10 nm thick SiO_2 was grown by thermal oxidation. Then the oxide surface was coated by $Cu_3(BTC)_2$ SURMOF using 15 dipping cycles. Finally, Al gate electrodes were evaporated through a shadow mask. Two *p*-Si/SiO_2/$Cu_3(BTC)_2$/Al MIS capacitors were fabricated to prove the reproducibility of the electrical properties. The successful growth of the SURMOFs on SiO_2 surfaces was characterized by XRD and AFM measurements. The electrical quality of the samples was evaluated through capacitance-voltage and conductance-voltage characteristics performed in a wide range of frequencies and temperatures. First, the measurements were carried out at room temperature and the frequency was varied from 500 kHz to 5 kHz. Temperature-dependent measurements were performed at a fixed frequency of 100 kHz. The capacitors were heated from 30 °C to 100 °C and then cooled down to room temperature. Analysis of the impedance data was performed using the methods described in chapter 4.

7.2 Structural and Morphological Properties of $Cu_3(BTC)_2$-Based MIS Capacitors

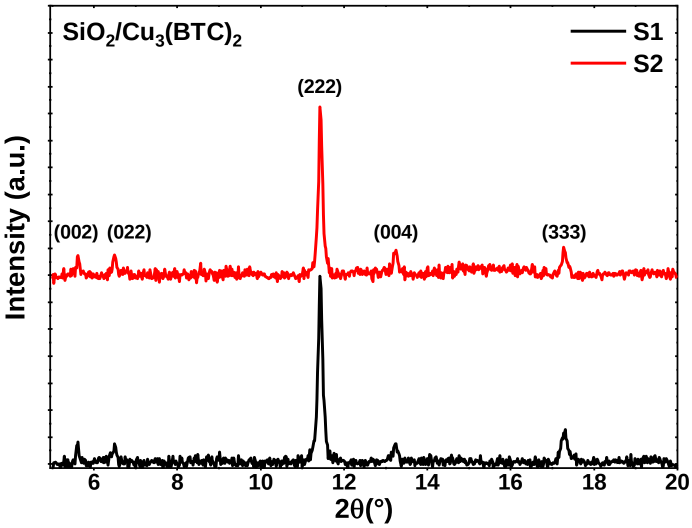


Figure 7.1 X-ray diffractograms of $Cu_3(BTC)_2$ coated on SiO_2 surfaces. The SURMOFs were prepared by the layer-by-layer process using 15 dipping cycles. The diffractograms show the crystalline structure, which is mainly oriented along the (222) diffraction plane.

X-ray patterns for two $Cu_3(BTC)_2$ SURMOFs, S1 and S2, growth with the same deposition parameters on 10 nm thick SiO_2 surfaces are depicted in Figure 7.1. The diffractograms exhibit characteristics diffractions peaks at around 2Θ= 5.62 °, 6.49 °, 11.44 °, 13.23 °, and 17.27 ° corresponding to orientations of (002), (022), (222), (004), and (333), respectively. The strongest intensity at the (222) Bragg peak indicates the growth of highly oriented SURMOFs at this diffraction plane. Both SURMOFs (S1 and S2) exhibits the same patterns indicating the reproducibility of the grown of thin $Cu_3(BTC)_2$ films on silicon substrates.

The incorporation of ultrasonic steps during the coating process of the SURMOF enhances the crystalline quality of the layers. This is demonstrated by X-ray patterns which show higher intensity peaks for SURMOFs prepared by ultrasonication in comparison to the samples prepared in chapter 6 (Figure 6.1c, 20 spray cycles).

Atomic force microscopy measurements for sample S2 are shown in Figure 7.2. The images exhibit a relatively smooth surface morphology with average roughness values of about 11.6 nm and 15.3 nm for scan areas of 1 µm × 1 µm and in 5 µm × 5 µm, respectively. In small scan areas, R_s values are smaller (6.13 nm for 0.4 µm × 0.4 µm). The obtained average roughness values are similar to the MOFs prepared without ultrasonication steps.

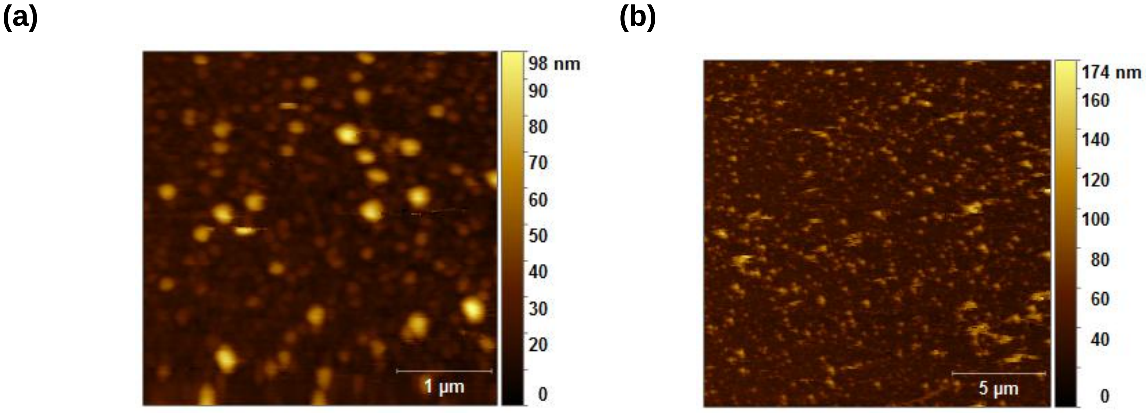


Figure 7.2 Topographical atomic force microscopy images for $Cu_3(BTC)_2$ SURMOF growth with 15 dipping cycles. The surface roughness exhibit standard deviations of 11.6 nm in an area of 1 µm × 1 µm and of 15.3 nm in an area of 5 µm × 5 µm.

7.3 Impedance Characteristics of $Cu_3(BTC)_2$-Based MIS Capacitors

Impedance measurements were performed in substrates containing dimensions of 2 cm × 2 cm. Circular Al gate contacts with areas of 0.0095 cm^2(A1), 0.0061 cm^2(A2), and 0.0059 cm^2(A3) were evaporated. In order to prove the reproducibly of the impedance experiments, two capacitors S1 and S2 were fabricated using $Cu_3(BTC)_2$ as a dielectric. The SURMOFs were coated with the same depositions condition. On the other hand, in order to assess the uniformity of the layers, several impedance measurements at a frequency of 100 kHz were performed in different areas and points of the capacitors. *C*-*V* curves for capacitor S1 exhibit a slight deviation in accumulation and inversion regions while the deviation of the *G*-*V* curves occurs only in depletion region (see Figure SI-7.1). Note that, the slight deviations of both curves ensure the homogeneity of the SURMOFs even when the roughness is relatively high.

Capacitance-voltage and conductance-voltage characteristics for $Cu_3(BTC)_2$ SURMOFs coated by the layer-by-layer process in 15 dipping cycles are shown in Figure 7.3 (a) and (b), respectively. The measurements were performed in forward (solid curve) and reverse (dotted curve) mode at 500 kHz by sweeping the gate voltage from -4 V to 1 V and back to -4 V. Layer thickness calculated from the capacitance curve in strong accumulation using the approximation of McNutt-Sah are 18 nm (S1) and 20 nm (S2).

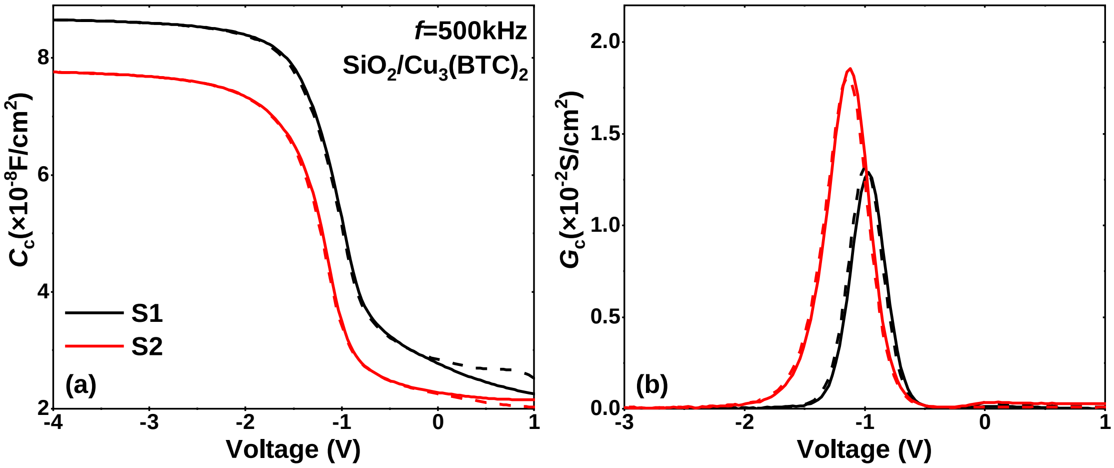


Figure 7.3 Capacitance-voltage (a) and conductance-voltage (b) characteristics measured at 500 kHz for *p*-$Si/SiO_2/Cu_3(BTC)_2/Al$ MIS capacitor. SURMOFs were prepared with 15 dipping cycles by the spray-coating method assisted by ultrasonication. Capacitors S1 and S2 were prepared using the same depositions process conditions to prove the reproducibly of the experiments.

Capacitance-voltage characteristics of the SURMOFs-based MIS capacitors in comparison to the ideal case ($V_{FB,the}$=0.88 V, D_{it}=0, N_{bt}=0, $Q_{eff,ox}$=0) exhibit two notable characteristics. First, there is a slightly parallel shift toward the negative voltage-axis indicating a low density of effective charges in the SiO_2/SURMOF stack. Indeed, low flat-band voltage values of -0.97 V (S1) and -1.15 V (S2) were determined. Effective oxide charge density determined from the difference of the experimental and theoretical flat-band voltage is found to be $+2.7\times10^{10}cm^3$ and $+7.3\times10^{10}cm^3$ for capacitors S1 and S2, respectively. The positive contribution of $Q_{eff,ox}$ could be assigned to fixed positive charges in the dielectric stack. In chapter 6, it was demonstrated that *p*-Si/SiO_2/$Cu_3(BTC)_2$/Al MIS capacitors exhibit large negative $Q_{eff,ox}$ values. In the case of SURMOFs-based capacitors coated by the LBL process assisted by ultrasonication, $Q_{eff,ox}$ reduces by two orders of magnitude.

Second, capacitance-voltage curves performed in forward and reverse mode reveal a very small hysteresis indicating a low density of border trap. Using the Fleetwood method, N_{bt} values at the flat-band voltage are found to be $9.5\times10^9cm^2$ (S1) and $9.0\times10^9cm^2$ (S2). These values are one order of magnitude lower than the values obtained for MOFs growth without ultrasonication. On the other hand, the density of interface traps determined from the conductance-voltage curve shown in Figure 7.3b using the Hill-Coleman method is $2.8\times10^{11}eV^{-1}cm^2$ for both capacitors. It can be seen that incorporation of ultrasonic steps during the coating process of the SURMOFs improves drastically the effective oxide charge density as well as border trap density. Nevertheless, the density of interface traps remains almost the same.

7.3.1 C-V and G-V Characteristics: Effect of Frequency

Figure 7.4 shows forward (solid line) and reverse (dotted line) capacitance-voltage characteristics measured at frequencies varying from 5 kHz to 500 kHz and at room temperature for capacitors S1 and S2. Both capacitors exhibit frequency dispersion in accumulation and depletion regimes. Frequency dispersion is attributed to a high density of border traps and interface traps. According to Figure 7.4, hysteresis in the *C-V* curves remains almost constant at all frequencies demonstrating that density of border traps is independent under variations of frequency. Besides the determined $N_{bt,F}$ values are lower in comparison to $D_{it,HC}$. Therefore, frequency dispersion in depletion will be attributed mainly to interface traps. On the other hand, the effect of interface traps is clearly observed by the broadening of the humps at low frequencies. The slightly lower frequency dispersion in accumulation region of capacitor S1 (0.02 Ω/cm^2) in comparison to capacitor S2 (0.27 Ω/cm^2) is attributed to the series resistance.

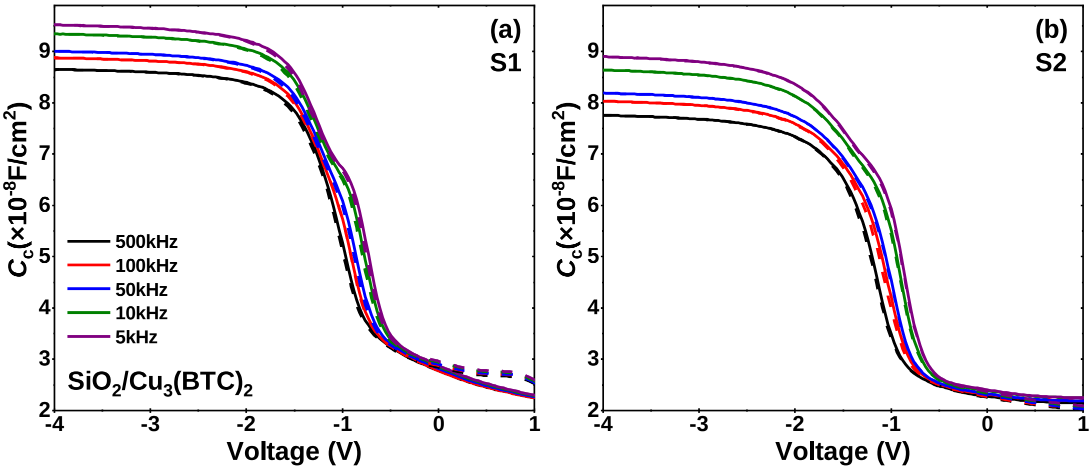


Figure 7.4 Capacitance-voltage curves measured in forward (solid line) and reverse (dotted line) mode at different frequencies for capacitors S1 (a) and S2 (b). Capacitor S2 exhibits higher frequency dispersion due to the higher series resistance (R_s=0.02 Ω/cm^2) in comparison to capacitor S1 (R_s=0.27 Ω/cm^2).

Equivalent parallel conductance as a function of frequency for capacitors S1 and S2 are shown in Figure 7.5 (a) and (b), respectively. G_{pc}/ω-ω curves were built by selecting different gates voltages around depletion region of G_{pc}/ω-V curves measured at different frequencies. It can be observed that the conductance curves are well fitted by a single Gaussian peak (dotted lines). Furthermore, low time responses of 4.81 µs (S1) and 5.43 µs (S2) were obtained, indicating that energy loss due to capture and emission of carriers is associated principally to interface traps rather than border traps. Density of interface traps retrieved at the G_{pc}/ω-ω peak around the flat-band voltage is found to be 5.7×10^{11}eV^{-1}cm^2 (S1) and 8.0×10^{11}eV^{-1}cm^2 (S2). Similar values were found for the samples prepared without ultrasonication.

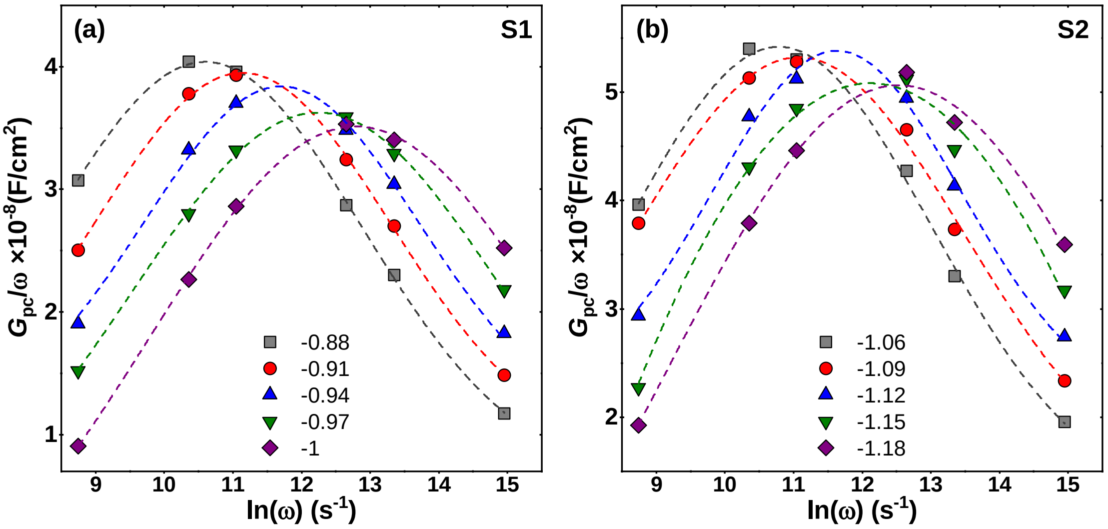


Figure 7.5 Equivalent parallel conductance versus angular frequency calculated at different gate voltages near depletion region for capacitor S1 (a) and S2 (b). The experimental points are very well fitted using Gaussian distributions (dotted line). Dots indicate the voltage at which the G_{pc}/ω-ω curve was extracted.

7.3.2 C-V and G-V Characteristics: Effect of Temperature

In order to gain further insight about the electronic properties of the empty MOF, the devices were heated from 30 °C to 100 °C in steps of 10 degrees and then cooled down to room temperature. Impedance measurements were performed by sweeping the gate voltage from -6 to 4 V and back to -6 V at a fixed frequency of 100 kHz. The heating experiments were performed in laboratory environment (T ≈ 294 K and approximately 30 % relative humidity). Capacitance-voltage and conductance-voltage curves measured in reverse mode for capacitor S1 are shown in Figure 7.6 (a) and (b), respectively. It can be observed that an increment of temperature during the measurements affects strongly the *C-V* characteristic. First, accumulation capacitance decreases as the temperature increase. Second, flat band voltage moves toward the negative voltage axis indicating an increment of fixed positive charges and interface charges. Positive fixed charges induce a parallel shift of the *C-V* curve while interface charges stretched-out the *C-V* curve along depletion region. $Q_{eff,ox}$ values increases from 8.3×10^{10}cm^3 (25 °C) up to 2.0×10^{11}cm^3 (100 °C).

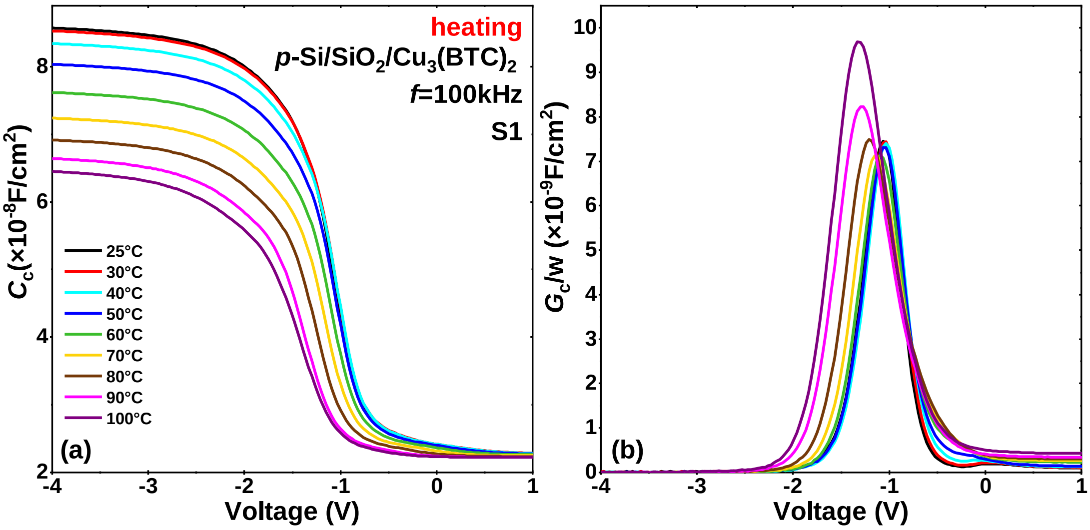


Figure 7.6 Capacitance-voltage (a) and conductance-voltage (b) characteristics for capacitor S1 measured at 100 kHz in reverse mode. The capacitor was heated from room temperature (RT) to 100 °C in steps of 10 degrees.

On the other hand, heating experiments also influence the conductance-voltage curve as is shown in Figure 7.6b. Upon increase of temperature up to 70 °C, the intensity of the conductance peaks increases slightly. At temperatures higher than 70 °C, the increment in intensity is strong. In addition, G_c/ω peak moves towards higher gate voltages values. Interface traps density retrieved using the Hill-Coleman method increases from 4.9×10^{11}eV^{-1}cm^2 (25 °C) up to 5.1×10^{11}eV^{-1}cm^2 (100 °C). In the case of MOF prepared without ultrasonication, at high temperatures, border traps contribute to the conductance (see Figure A-6.2). In contrast, in the case of SURMOFs coated by the LBL process assisted by ultrasonication, only interface traps contribute to the conductance curve.

Border trap density as a function of temperature was extracted from the hysteretic behavior of the capacitance-voltage curves shown in Figure 7.7. The measurements were performed in forward (black curve) and reverse (green curve) mode at a fixed frequency of 100 kHz. It should be noted that for temperatures below 60 °C, hysteresis in the capacitance-voltage curves remains small and density of border traps slightly increases from 1.6×10^{10} cm^2 (at 25 °C) to 1.9×10^{10} cm^2 (at 60 °C).

Temperatures above 60 °C induce a shift of the reverse capacitance curves to the negative side, broadening the hysteresis. Thus, N_{bt} considerably increases up to 1.5×10^{11} cm^2 at 100 °C. This effect could be attributed to the depassivation of defects leading an increase of border traps density. Cooling experiments result in a decrease of hysteresis, suggesting the reduction of the trapping process. The electrical quality of MOFs prepared without ultrasonication are degraded under heating experiments, and after cooling, they do not reach the initial state again. In contrast, after heating experiments, the SURMOFs prepared by the layer-by-layer process optimized by ultrasonication exhibit a slow recovering of the accumulation capacitance as well as hysteresis. In addition, the initial state of the capacitance-curve is almost obtained.

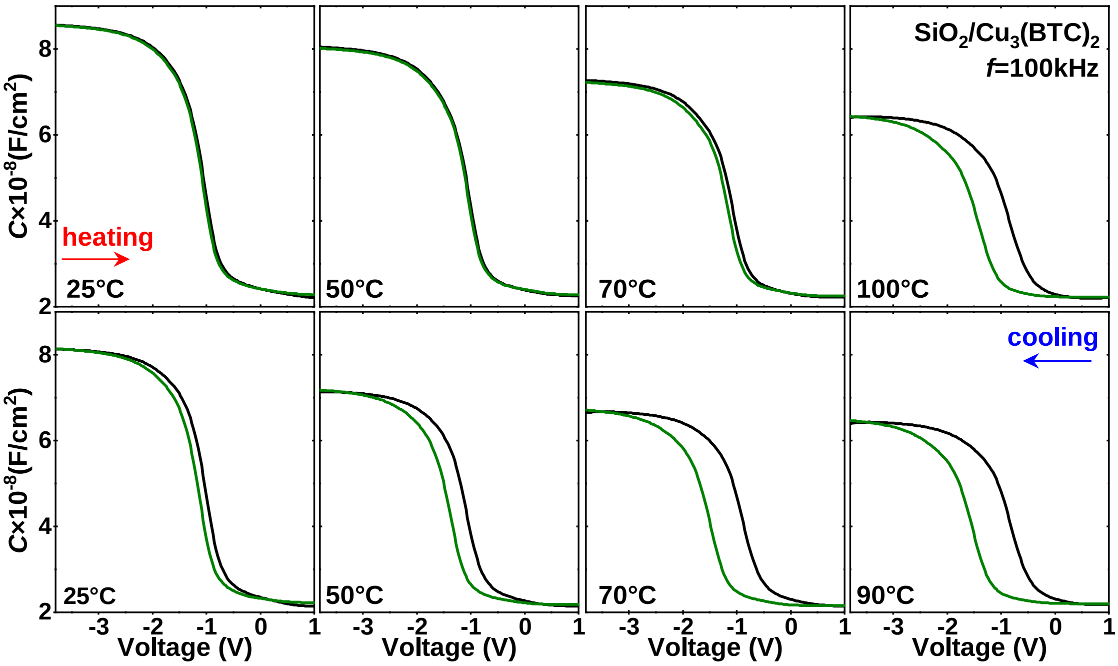


Figure 7.7 Forward (black) and reverse (green) capacitance characteristics for capacitor S1 measured at different temperatures. First, the capacitors were heated from room temperature (RT) to 100 °C in steps of 10 °C and then it was cooled down to RT.

Accumulation capacitance as a function of temperature for $Cu_3(BTC)_2$-based MIS capacitor is shown in Figure 7.8. $C_{c,acc}$ values were extracted from the C-V curves at a gate voltage of -3.4 V. The figure clearly shows that upon an increment of temperature the accumulation capacitance decreases. In the case of $Cu_3(BTC)_2$ SURMOFs, it was demonstrated that an increase in temperature causes a decrease in dielectric constant [30]. Therefore, decreases of $C_{c,acc}$ can be associated with the unloading of moisture and other related potential guest molecules into the pores of the $Cu_3(BTC)_2$ since the heating experiments were performed in laboratory environment. Decrease of temperature from 100 °C to room temperature results in an increase of accumulation capacitance signifying the loading of moisture again. Note that the unloading process is faster than the loading one. Accumulation capacitance recovers up to 94 % of the initial $C_{c,acc}$ value.

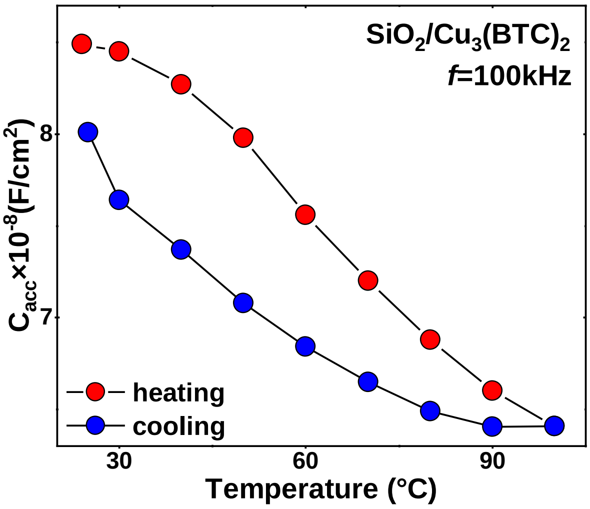


Figure 7.8 Accumulation capacitance as a function of temperature. $C_{c,acc}$ values were extracted at a gate voltage of -3.4 V from C-V curves measured at 100 kHz.

7.4 Summary

Thin films of $Cu_3(BTC)_2$ SURMOFs prepared with 15 dipping cycles by the layer-by-layer approach assisted by ultrasonication were incorporated into MIS capacitor structures. According to the results, it can be verified that the incorporation of ultrasonic steps in the coating process of the SURMOFs improves the electrical properties of the capacitor. This is demonstrated by the significant reduction of border trap density in comparison to the samples prepared without ultrasonication. Because of the small density of border traps, hysteresis is independent of frequency. This fact is confirmed by the small hysteresis in the C-V curve that almost does not change under frequency variations. In contrast, interface trap density depends strongly in frequency as is shown by the appearance of humps in the *C-V* at low frequencies.

On the other hand, temperature-dependent measurements demonstrate the good stability of the capacitor. Interfacial properties slightly change under heating experiments up to 60 °C. In addition, only interface traps contribute to the conductance curve. After cooling experiments, the capacitor almost recovers the initial state. However, the addition of ultrasonic steps during the deposition method of the SURMOFs does not improve interface trap density.

8 Conclusions

In this work, interfacial properties such as border trap density, interface trap density, effective oxide charges and time response of interface traps for ultra-thin films of $Cu_3(BTC)_2$ metal-organic framework have been intensively investigated by impedance spectroscopy and reported for the first time. $Cu_3(BTC)_2$ films with layer thicknesses between 5 nm to 30 nm were coated directly on silicon and silicon dioxide surfaces with and without functionalization in a layer-by-layer fashion. The growth of crystalline and uniform MOF layers allows its integration within MIS structures.

The quality and performance of MIS capacitors depend on the density of defects located near and at the insulator/semiconductor interface. In the Si-SiO_2-Al MIS system, defects are passivated by hydrogen atoms introduced during the deposition process of the dielectric layer or by post-annealing treatments under forming gas atmosphere. The linker component of the MOF, trimesic acid, contains hydrogen atoms in its structure, therefore, SiO_2-based MIS capacitors were fabricated to study the influence of trimesic acid. The capacitor was immersed in the trimesic acid solution for one hour at room temperature. MOFs-based MIS capacitors were not subjected to any post-deposition annealing because the properties of $Cu_3(BTC)_2$ degrade at high temperatures.

Trimesic Acid on SiO_2-Based MIS Capacitors

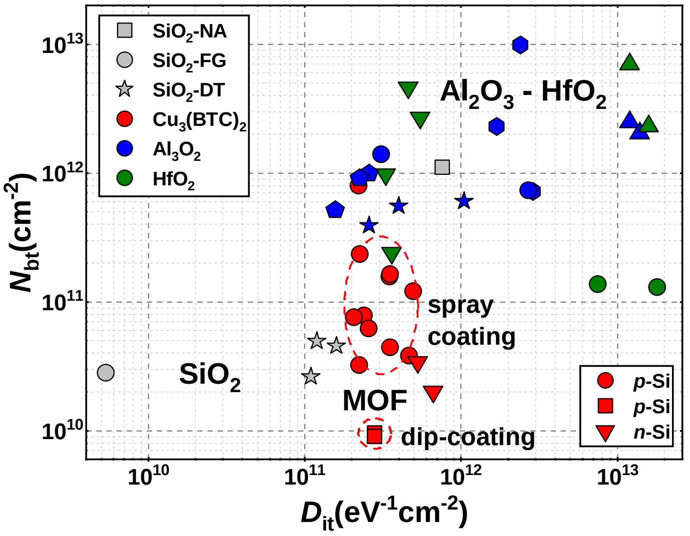
After immersion of the capacitors in trimesic acid solution, *C-V* curves shift to the right side of the voltage axis, indicating a reduction of fixed positive charges. It might be associated with partial negative charges existing in the carboxylates units of the TMA. Hysteresis in SiO_2-based MIS capacitors occurs due to charge injection from the silicon into border traps located at the Si/SiO_2 interface. The hysteresis of the capacitors immersed in TMA decreases indicating suppression of charge trapping process due to the strong reduction of border trap density from $1.11\times10^{12}cm^{-2}$ (NA) to $2.99\times10^{11}cm^{-2}$ (TMA). A slightly reduction of interface trap density from $1.66\times10^{12}eV^{-1}cm^{-2}$ (NA) to $1.32\times10^{12}eV^{-1}cm^{-2}$ (TMA) was also obtained. Reduction of defects could be related to the dissociation of hydrogen atoms existing in the trimesic acid that diffuse into the silicon dioxide layer toward the SiO_2/Si interface. Nevertheless, passivation by TMA is a temporary effect.

$Cu_3(BTC)_2$-Based MIS Capacitors

$Cu_3(BTC)_2$-based MIS capacitors exhibit both fixed charges, positive and negative. It depends on the MIS structure and the thickness of the MOF. Fixed positive charges are associated with unsaturated copper atoms while fixed negative charge to the linker component. The orientation of hysteresis in the bidirectional capacitance measurements suggests that charge carrier transport occurs in two sequential steps. First, injection of electrons from the gate into traps located close to the $Al/Cu_3(BTC)_2$ interface and then transport towards border traps located close to the $Cu_3(BTC)_2/Si$ interface via tunneling or/and hopping. The capacitors also exhibit frequency dispersion in the accumulation and depletion regimes of the capacitance curves attributed to interface and border traps.

Ultra-thin $Cu_3(BTC)_2$ films prepared by the spray-coating method exhibit a relatively low defect density ($\sim 10^{11} eV^{-1} cm^{-2}$ and $\sim 10^{11} cm^{-2}$). However, interfacial defects cause dispersion in the accumulation and depletion regimes of frequency-dependent capacitance-voltage measurements. Additionally, hysteresis in the C-V curve of p-$Si/SiO_2/Cu_3(BTC)_2/Al$ MIS capacitors becomes large ones the frequency is decreased. Surface functionalization of SiO_2 with APTES stabilizes the magnitude of hysteresis. Temperature-dependent measurements reveal the capability of the MOFs to load/unload moisture and potential guest molecules. This is demonstrated by the decrease/increase of the accumulation capacitance associated with the change in dielectric constant upon heating/annealing experiments. Furthermore, heating experiments favor the activation of border traps and, therefore, hysteresis in the C-V curve increases. Besides, they contribute to the conductance characteristics causing a shoulder in the depletion regime. Activation of interface traps is observed by the increase in stretch-out around depletion region of the capacitance curve. The activation of defects could be related to depassivation of dangling bonds, which leads to degradation of the electrical quality of the devices. The addition of ultrasonic steps on the coating process decreases considerably the density of border traps up to 8.89×10^9 cm^{-2}. Additionally, the layers are more stable under heating experiments and after cooling they almost recover the initial state. Nevertheless, ultrasonic steps do not improve interface traps.

Overall results of this study, demonstrate a relatively good interface quality of the MOF-based MIS capacitors as is shown in the figure below. $Cu_3(BTC)_2$ exhibits interfacial properties comparable to inorganic materials, although the MOFs-based MIS capacitors did not receive a final post-annealing treatment.



Density of border traps (N_{bt}) versus density of interface traps (D_{it}) for $Cu_3(BTC)_2$ in comparison to inorganic materials. $Cu_3(BTC)_2$ MOF (red color), SiO_2 (gray color, start [93]), Al_3O_2 (blue color, up triangle [147], pentagon [148], hexagon [149], star [150], circle [141]) and HfO_2 (green color, up triangle [147], down triangle [151], circle [152]). NA (non-annealed capacitor), FG (forming gas), and DT (different treatments).

The successful growth of ultrathin $Cu_3(BTC)_2$ films and their relatively low concentration of interfacial traps recommend the use of this MOF as a dielectric layer in capacitor-based sensors. Density of border traps could be most-likely further reduced by an innovative annealing procedure. Measurements of the electrical and sensing properties of the MOF under vacuum conditions are also of great importance. On the other hand, further experiments can be concentrated on the incorporation of high-temperature stable MOFs in capacitor structures to improve the quality of the devices by passivation of defects through post-annealing treatments under forming gas atmosphere. An interesting alternative could be ZIF-8 because it can be grown on substrates with layer thickness lower than 100 nm.

Appendix

Chapter 6: Ultra-Thin $Cu_3(BTC)_2$ Films Based MIS Capacitors: Spray-Coating Method

Figure A-6.1 shows capacitance-voltage and conductance-voltage curves measured in reverse mode at a fixed frequency of 100 kHz for *p*-Si/$Cu_3(BTC)_2$/Al MIS capacitors containing MOF layers coated with 10 and 15 spray cycles. The measurements were carried out in different positions of the capacitors with dimensions of 2 cm × 2 cm. There is a variation in the accumulation region of the capacitance curves indicating a change in MOF thickness. The change in thickness induces a small variation of the conductance curve. In general, the small variation of the *C*-*V* and the *G*-*V* curves demonstrate the relatively good homogeneity of the ultra-thin $Cu_3(BTC)_2$ films.

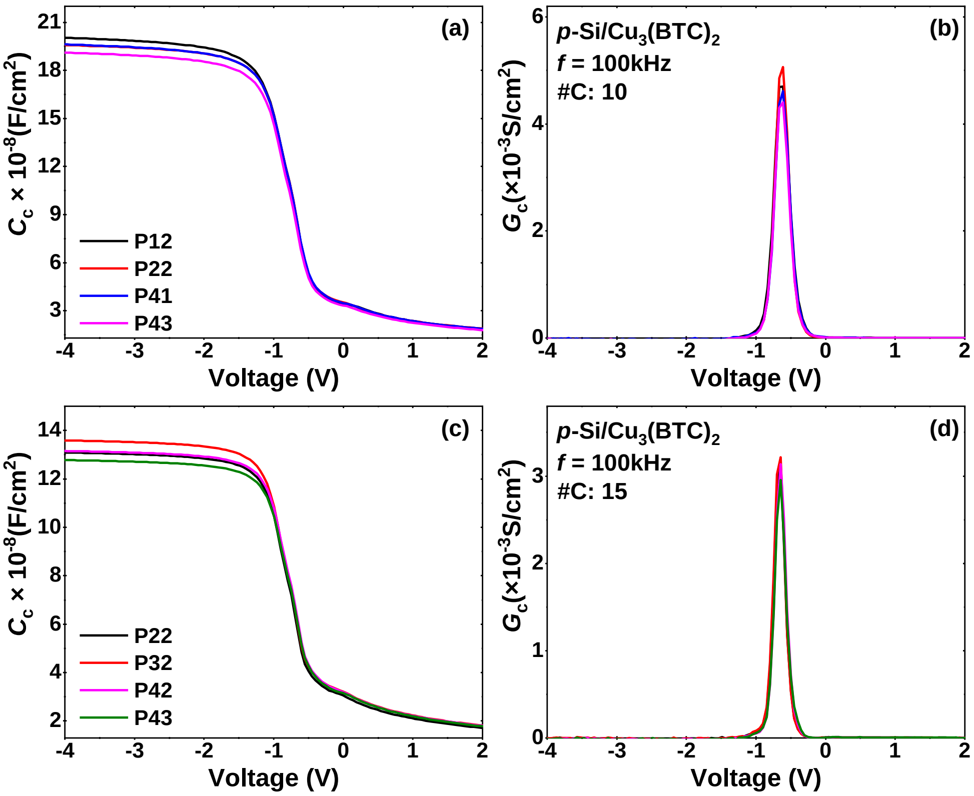


Figure A-6.1 Capacitance (a)(c) and conductance (b)(d) curves for *p*-Si/$Cu_3(BTC)_2$/Al MIS capacitor prepared with 10 and 15 spray cycles. The measurements were performed in different positions of the capacitor.

Figure A-6.2 shows the conductance-voltage curve for *p*-Si/SiO_2/APTES/$Cu_3(BTC)_2$/Al MIS capacitor containing a MOF layer coated with 15 spray cycles. The measurements were performed from room temperature to 100 °C. At room temperature, the conductance (black curve) exhibits only one peak indicating that only interface traps can response to the AC voltage. For temperatures higher than 50 °C, a shoulder appear in the conductance curve indicating that another interfacial traps defect but with low time response than interface traps are also able to follow the AC voltage. The shoulder increases for further temperatures.

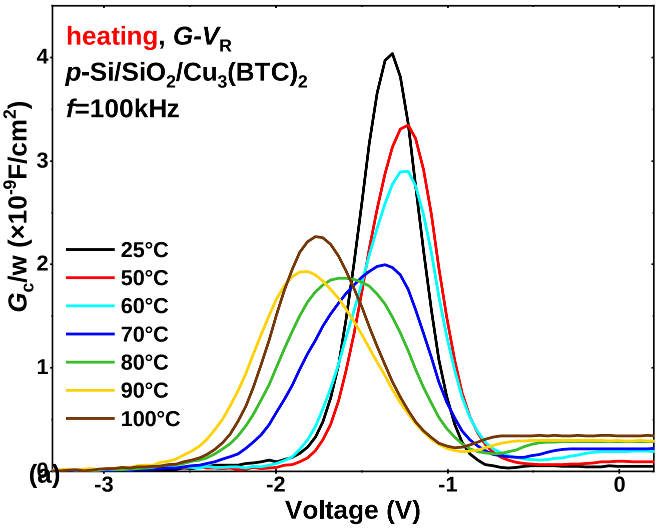


Figure A-6.2 Temperature-dependent conductance-voltage characteristics measured in reverse mode for *p*-Si/SiO_2/APTES/$Cu_3(BTC)_2$/Al MIS capacitor.

Chapter 7: Ultra-Thin $Cu_3(BTC)_2$ Films Based MIS Capacitors: Layer-by-Layer Approach Assisted by Ultrasonication

Figure A-7.1 shows the capacitance and conductance curves for *p*-Si/$Cu_3(BTC)_2$/Al MIS measured in different positions of the devices containing gate electrodes from different areas. Results demonstrate a good homogeneity of the ultra-thin SURMOF films.

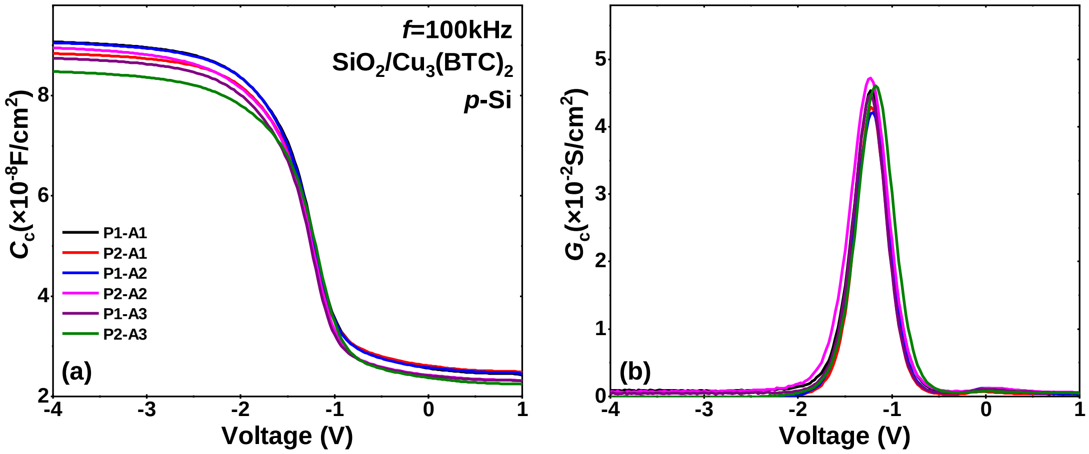


Figure A-7.1 Capacitance (a) and conductance (b) characteristics for *p*-Si/SiO_2/$Cu_3(BTC)_2$/Al MIS capacitor structure measured in different positions (P) of the devices and on gate electrodes containing different areas (A). A1(0.0095 cm2), A2(0.0061 cm^2), and A3(0.0059 cm^2).

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List of Figures

List of Tables

List of Publications

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