Quasi-Two-Level PWM Operation for Modular Multilevel Converters: Implementation, Analysis, and Application to Medium-Voltage Motor Drives

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Kurzfassung

Der Betrieb von modularen Mutlilevel-Umrichtern bei niedrigen Betriebsfrequenzen, notwendig für Anwendungen als Mittelspannungsantrieb, ist generell mit den bekannten Betriebsmodi herausfordernd. Besonders wenn das Bemessungsmoment während des Stillstands erforderlich und die Bemessungsfrequenz der Maschine niedrig sind, muss die installierte Modulkapazität sehr hoch sein. Eine mögliche Lösung für dieses Problem stellt der Quasi-Zwei-Level-PWM-Modus dar, welcher die Kapazität um mehr als eine Größenordnung reduziert. Obwohl er auf die Multilevel-Kurvenform verzichtet, bleiben alle anderen Vorteile eines konventionell betriebenen modularen Multilevel-Umrichters erhalten. Diese Vorteile beinhalten kleine Spannungsstufen (limitierend für die Probleme mit langen Maschinenkabeln und für Lagerströme), Modularität, Skalierbarkeit auf höhere Spannungen und eine unkomplizierte Möglichkeit Redundanz aufzubauen.

Diese Dissertation zeigt die Herleitung des Quasi-Zwei-Level-PWM-Modus und schlägt zwei geeignete Regelungsmethoden vor. Diese sind mittels eines skalierten Prototyps des modularen Multilevel-Umrichters validiert. Simulationen werden eingesetzt, um die Sensitivität der vorgeschlagenen Regelungen auf die Unsicherheiten der bekannten Umrichterparameter zu evaluieren. Zusätzlich werden besondere Effekte und Eigenschaften des Betriebsmodus untersucht. Diese sind z.B. Spannungsfehler, Reduzierung der Überspannungen bei langen Maschinenkabeln und eine Anwendung mit Flat-Top Modulation.

Neben den vorgestellten Regelungsmethoden wurde auch die Dimensionierung untersucht. Erst wurden die für den Betriebsmodus spezifischen Trade-offs der Umrichterparameter identifiziert. Die Evaluierung dieser Trade-offs hat gezeigt, dass der Quasi-Zwei-Level-PWM-Modus sich besonders gut für modulare Multilevel-Umrichter mit einer höheren Anzahl von Modulen pro Zweig eignet. Im nächsten Schritt wurden quasi-zwei-level-PWM-betriebene modulare Multilevel-Umrichter für mehrere Fälle von niederfrequenten Mittelspannungsantrieben dimensioniert. Für die Dimensionierung wurden das validierte Simulationsmodell und die in der Arbeit hergeleiteten analytischen Gleichungen angewendet. Zudem wurde das Modell zusätzlich genutzt, um eine dynamische Beschleunigung der Maschine zu simulieren. Die Simulationen bestätigen die Plausibilität der durchgeführten Dimensionierungen.

Die resultierenden Design-Indikatoren werden für die einzelnen Dimensionierungsfälle mit den Indikatoren des konventionell betriebenen modularen Multilevel-Umrichters, mit denen des Zweipunkt-Wechselrichters mit einer Serienschaltung von IGBTs und mit denen des modularen Multilevel-Matrix-Umrichters verglichen. Diese wurden für die gleichen Fälle dimensioniert. Der Vergleich mit dem konventionellen Betriebsmodus des modularen Multilevel-Umrichters und mit dem modularen Multilevel-Matrix-Umrichter zeigt Dimensionierungsvorteile des Quasi-Zwei-Level-PWM-Modus. Wie erwartet, wird die Verzerrung des Ausgangsstroms mit dem Quasi-Zwei-Level-PWM-Modus deutlich erhöht. Es ist jedoch zu erwarten, dass diese Verzerrung für die Anwendung in Mittelspannungsantrieben akzeptabel ist und kein zusätzlicher

Filteraufwand betrieben werden müsste. Zusammenfassend stellen quasi-zwei-level-PWM-betriebene modulare Multilevel-Umrichter eine vielversprechende Alternative für Anwendungen in niederfrequenten Mittelspannungsantrieben dar.

Schlagwörter:
modularer Multilevel-Umrichter, Quasi-Zwei-Level, reduzierte Kapazität

Abstract

The low-frequency operation of modular multilevel converters, required by variable-speed drives, is generally challenging within the established operation modes. Especially when rated torque beginning from zero speed is required and the rated machine speed is low, the installed module capacitance has to be very high. A possible solution to this problem is quasi-two-level PWM operation, which reduces the capacitance by more than an order of magnitude. Although the multilevel property of the modular multilevel converter has to be sacrificed, all other advantages, i.e. small voltage steps limiting the problems with long machine cables and bearing currents, modularity, scalability to higher voltage levels, and a straight-forward option to add redundancy, are retained from the conventionally operated modular multilevel converters.

This thesis presents a derivation of the quasi-two-level PWM operation mode and proposes two suitable control methods. These methods are validated using a downscaled prototype of a modular multilevel converter. Simulations are conducted to evaluate the sensitivity of the proposed control to uncertainities in the knowledge of the converter parameters. Furthermore, the specific effects and properties of the operation mode, such as output voltage errors, reduced overvoltages with long machine cables, and the operation with flat-top modulation, are analyzed.

In addition to the presented control methods, the design process is studied. First, the specific design trade-offs between the converter parameters are identified. The evaluation of trade-offs shows that quasi-two-level PWM operation is especially well-suited for modular multilevel converters with a high number of modules per branch. In the next step, the quasi-two-level PWM-operated modular multilevel converters are designed for several study cases of low-frequency medium-voltage drives. The design process utilizes the validated simulation model and derived analytic equations. Additionally, the validated model is also used to simulate a dynamic machine acceleration to confirm the plausibility of the designs.

The resulting design indicators of the conducted designs are compared to those of the conventional operation mode of the modular multilevel converter, to the two-level voltage-source inverter based on series-connected IGBTs, and to the modular multilevel matrix converter, which were designed for the same study cases. The comparison to standard operation modes of the modular multilevel converter and to the modular multilevel matrix converter shows design advantages for the quasi-two-level PWM operation of modular multilevel converters. As expected, the output current distortion is significantly increased with the quasi-two-level PWM operation. Nevertheless, the current distortion is likely to be acceptable for medium voltage drives without additional filter requirements. In conclusion, quasi-two-level PWM-operated modular multilevel converters are a favorable alternative for applications in low-speed medium-voltage drives.

Keywords:
modular multilevel converter, quasi two level, reduced capacitance

Contents

Abbreviations

ac	alternating current
dc	direct current
p.u.	per unit
ADC	analog-to-digital converter
AFE	active front-end
APOD	alternative phase opposition disposition
ASIC	application-specific integrated circuit
CHB	cascaded H-bridge
CPU	central processing unit
CRC	cyclic redundancy check
DSP	digital signal processor
EMI	electromagnetic interference
FFT	fast Fourier transformation
FPGA	field-programmable gate array
FSM	finite state machine
FTM	flat-top modulation
HF	high-frequency
HVDC	high-voltage direct current
HV-IGBT	high-voltage insulated-gate bipolar transistor
IGBT	insulated-gate bipolar transistor
IO	input-output
IPM	instantaneous power mode
LFM	low-frequency mode
MMC	modular multilevel converter
MMMC	modular multilevel matrix converter
MOSFET	metal-oxide-semiconductor field-effect transistor
P	proportional
PC	personal computer
PCB	printed circuit board

PD	phase disposition
PI	proportional-integral
POD	phase opposition disposition
PR	proportional-resonant
PMSM	permanent magnet synchronous machine
PWM	pulse-width modulation
RMS	root mean square
SoC	system on chip
SVM	space vector modulation
THD	total harmonic distortion
VSI	voltage source inverter

Symbol Conventions

a	variable
A	constant value, RMS value, or direct value
$\hat{a}$	peak value, or amplitude
$\bar{a}$	mean value
a^*	setpoint value
$\tilde{a}$	estimated value
$a_{\max}$	maximum value
$a_{\min}$	minimum value
$\lvert a \rvert$	absolute value
$\mathbf{A}$	matrix
$\mathbf{a}$	vector

Nomenclature

$\mathbf{A}$	system matrix
A	scaled chip area
a	chip-area scaling factor
a_1	chip-area scaling factor of the upper switch of a half-bridge module
a_2	chip-area scaling factor of the lower switch of a half-bridge module
A_{ref}	reference chip area
a_{tot}	total relative chip area of semiconductor switches in a converter
$\mathbf{B}$	input matrix
$\mathbf{B}'$	extended input matrix
c	triangle carrier function
C_{i}	dc-link capacitance
$C_{\mathrm{i}}^{\mathrm{ana}}$	analytically estimated dc-link capacitance
$C_{\mathrm{i}}^{\mathrm{sim}}$	dc-link capacitance estimated through simulations
C_{mod}	module capacitance
$\cos\varphi_{\mathrm{N}}$	rated power factor
$C_{\vartheta,\mathrm{ref},x}$	thermal capacitance of the x-th Foster-network section of the reference device
$C_{\vartheta,x}$	thermal capacitance of the x-th Foster-network section
$d_{i_{\mathrm{b}}}$	estimated branch current direction
$d_{i_{\mathrm{b}x}}$	estimated branch current direction of branch x
$\mathrm{d}i/\mathrm{d}t$	rate of current rise
$\mathrm{d}v/\mathrm{d}t$	rate of voltage rise
δ	duty cycle (defined as ratio between the setpoint output voltage and the half of input voltage), $\delta \in [-1, 1]$
δ_0	zero component of duty cycles
δ_{max}	maximum achievable duty cycle, selected during converter design
δ_x	duty cycle of phase x
$\mathbf{E}$	disturbance matrix
e_{b}	branch energy
$e_{\mathrm{b}x}$	branch energy of branch x
$E_{C\mathrm{i,tot}}$	total energy which can be stored in the dc-link capacitor
$E_{C\mathrm{mod,tot}}$	total energy which can be stored in module capacitors
$E_{\mathrm{D,rec,ref}}$	reverse recovery loss energy of reference diode
$E_{L,\mathrm{tot}}$	total energy which can be stored in branch inductors
$E_{\mathrm{T,off,ref}}$	turn-off loss energy of reference transistor

$E_{\mathrm{T,on,ref}}$	turn-on loss energy of reference transistor
ε_{r}	relative permittivity
η_{N}	efficiency at rated operating point
ΔE_{b}	branch energy variation
Δe_{b}	branch energy disturbance
$\Delta e_{\mathrm{b,max}}$	maximum branch energy variation
$\Delta e_{\mathrm{b}x}$	branch energy disturbance in branch x
$\Delta e_{\mathrm{mod,d,max}}$	worst-case module energy variation caused by delayed switching of the modules
f	frequency of the system connected to converter output
f_0	resonance frequency
f_{g}	grid frequency
f_{HF}	HF modulation frequency or frequency of the common-mode voltage HF component
$f_{\mathrm{HF,mod}}$	HF modulation frequency equally divided between the modules of a branch
f_{LP}	low-pass filter bandwidth frequency
f_{m}	modulation frequency
f_{PWM}	PWM frequency, $f_{\mathrm{PWM}} = 1/T_{\mathrm{PWM}}$
f_{s}	stator frequency
f_{sN}	rated stator frequency
$G_{\mathrm{P},e}$	proportional gain of the energy controller
$\Gamma_{\mathrm{machine}}$	reflection coefficient of the machine
Γ_{VSI}	reflection coefficient of the converter
H	energy storage constant
$H(s)$	transfer function
$H_{C\mathrm{i,tot}}$	energy storage constant for the energy stored in the dc-link capacitor
$H_{C\mathrm{mod,tot}}$	energy storage constant for the energy stored in module capacitors
$H_{L,\mathrm{tot}}$	energy storage constant for the energy stored in branch inductors
H_{tot}	energy storage constant representing the energy which can be stored in passive components of the converter
i_{b}	branch current
$I_{\mathrm{b,c,max}}$	maximum allowed compensating current, selected during converter design
$I_{\mathrm{b,c,rel}}$	maximum allowed compensating current relative to the designed maximum output current
$i_{\mathrm{b}x\mathrm{,c}}$	compensating current for branch x
$i_{\mathrm{b}x\mathrm{,c,HF}}$	additional compensating current component generated by HF-current injection in branch x
$I_{C\mathrm{i}}$	maximum RMS current of the dc-link capacitor
$i_{\mathrm{cir}x}$	circulating current number x
$I_{C,\mathrm{mod}}$	maximum RMS current of a module capacitor
$I_{\mathrm{c,thr}}$	threshold value of the compensating current used in the smart injection of HF current
$i_{C,x}$	current passing through the x-th capacitor

i_d	d component of the output currents in rotating reference frame
i_D	diode current
$i_{\mathrm{D}x}$	diode current of diode x
$i_{\mathrm{D}x,\mathrm{rec}}$	current sampled at diode x while the diode turns off
i_HF	HF current
i_i	input current
i_leg	leg current
$i_{\mathrm{leg}x}$	leg current of phase leg x
i_o	output current
$I_\mathrm{o,FH}$	RMS value of the fundamental harmonic of the output current
$i_\mathrm{o,T1}$	output current sampled at the first `TRANSITION STATE` within a PWM period
$i_\mathrm{o,T2}$	output current sampled at the second `TRANSITION STATE` within a PWM period
$i_{\mathrm{o}x}$	output current of phase x
i_q	q component of the output currents in rotating reference frame
I_sN	rated stator current
i_T	transistor current
$i_{\mathrm{T}x}$	transistor current of transistor x
$i_{\mathrm{T}x,\mathrm{off}}$	current sampled at transistor x while the transistor turns off
$i_{\mathrm{T}x,\mathrm{on}}$	current sampled at transistor x while the transistor turns on
$\Delta i_\mathrm{b,r,rel}$	worst-case peak-to-peak branch current ripple relative to the designed maximum output current
$\Delta i_\mathrm{b,r,max}$	worst-case peak-to-peak branch current ripple
J	rotational inertia
k	index for a discrete point in time
k_cr	design factor decreasing the achievable rated machine voltage to provide sufficient margin for the machine control
k_e	design factor increasing the installed module capacitance to provide sufficient margin for the branch energy control
l	cable length
L_b	branch inductance
l_crit	critical cable length
$l_\mathrm{crit,q2l}$	critical cable length for quasi-two-level waveforms
L_d	machine's inductance in d-axis
L_i	inner inductance of the input system
L_leg	leg inductance
L_o	output inductance
$L_\mathrm{o,eff}$	effective inductance affecting the output current
L_q	machine's inductance in q-axis
λ	ratio of the voltage drops over the leg inductor during the two different types of transition states
M	modulation index

$\mathbf{M}_{\mathrm{LF}}$	energy control matrix for low machine speeds
$\mathbf{M}_{\mathrm{N}}$	rated energy control matrix
μ_{r}	relative permeability
$n_{\mathrm{b}x}$	number of inserted modules in branch x
$n_{\mathrm{mod,tot}}$	total number of modules in a converter
n_{mpb}	number of modules per branch
n_{s}	number of series-connected IGBTs
n_{step}	number of voltage steps
ω	angular frequency of output system, $\omega = 2 \cdot \pi \cdot f$, or machine speed
ω_{N}	rated machine speed
ω_x	auxiliary angular frequency
P	transmitted active power
p	number of pole pairs
p_{b}	branch power
$p_{\mathrm{b}x}$	branch power of branch x
p_{D}	diode conduction losses
$p_{\mathrm{D,rec}}$	diode reverse-recovery losses
p_{i}	input power
$p_{\mathrm{loss,D}}$	total diode losses
$p_{\mathrm{loss,T}}$	total transistor losses
$P_{\mathrm{loss,tot}}$	total converter losses
P_{mech}	rated mechanical power
p_{o}	output power
$P_{\mathrm{sw,ref}}$	reference switching power of a single semiconductor switch
$p_{\mathrm{sw,rel}}$	relative switching power of a converter
p_{T}	transistor conduction losses
$p_{\mathrm{T,off}}$	transistor turn-off losses
$p_{\mathrm{T,on}}$	transistor turn-on losses
φ	angle between output current and output voltage
$\Psi_{\mathrm{f,d}}$	field-linked direct axis flux linkage of a synchronous machine (the flux induced by the field current linked in the stator windings)
ΔP	the difference between the input and output power
Q	reactive power
q	electric charge
Δq	variation of electric charge
R_{b}	branch resistance
R_{ch}	resistance of the resistor for precharging of the input capacitor during converter start-up
R_{i}	inner resistance of the input system
R_{o}	output resistance
R_{s}	machine's stator resistance

$R_{\vartheta,\mathrm{ref},x}$	thermal resistance of the x-th Foster-network section of the reference device
$R_{\vartheta,\mathrm{s}}$	thermal resistance of the sink
$R_{\vartheta,\mathrm{s,ref}}$	thermal resistance of the reference sink
$R_{\vartheta,x}$	thermal resistance of the x-th Foster-network section
S	apparent power
s	module switching state or complex Laplace variable
$\mathbf{s}_{\mathrm{b}x}$	vector of module switching states of branch x
s_{l}	switching state of the left half-bridge in a full bridge module
S_{N}	rated apparent electrical power
s_{r}	switching state of the right half-bridge in a full bridge module
T	time period or torque
t	time
$T_{\mathrm{bA,c}}$	time period in which the compensating current of branch A is active
$T_{\mathrm{bB,c}}$	time period in which the compensating current of branch B is active
T_{d}	delay period between switching instants of modules within a single branch
T_{DT}	length of IGBT's dead time (interlocking time)
T_{f}	duration of frozen state
T_{HF}	HF modulation period, $T_{\mathrm{HF}} = 1/f_{\mathrm{HF}}$
T_{N}	rated torque
T_{p}	prediction period (used in current controller)
T_{PWM}	PWM period, $T_{\mathrm{PWM}} = 1/f_{\mathrm{PWM}}$
t_{r}	rise time
T_{s}	sampling period
T_{T}	duration of transition state
T_{T1}	duration of transition state occurring first during a PWM period
T_{T2}	duration of transition state occurring second during a PWM period
$T_{\mathrm{T,bA}}$	time period in which the branch power peak is applied to branch A
$T_{\mathrm{T,bB}}$	time period in which the branch power peak is applied to branch B
$T_{\mathrm{T},i\mathrm{bAc}}$	time period required to change the leg current by the value of compensating current for branch A
$T_{\mathrm{T},i\mathrm{bBc}}$	time period required to change the leg current by the value of compensating current for branch B
$T_{\mathrm{T},i\mathrm{o}}$	time period required to change the leg current by the value of output current
ϑ	temperature difference
$\Delta\vartheta_{\mathrm{c,s}}$	case-to-sink temperature
$\Delta\vartheta_{\mathrm{j}}$	variation of the junction temperature during a single output period
$\Delta\vartheta_{\mathrm{j,max}}$	maximum allowed variation of the junction temperature
$\Delta\vartheta_{\mathrm{j,s}}$	junction-to-sink temperature
$\Delta\vartheta_{\mathrm{j,s,max}}$	maximum allowed junction-to-sink temperature
v_{b}	branch voltage
$v_{\mathrm{b}x}$	branch voltage of branch x

V_C	mean module capacitor voltage
v_C	module capacitor voltage
$\mathbf{v}_{C,\mathrm{b}x}$	vector with module capacitor voltages of branch x
$\overline{v}_{C,\mathrm{b}x}$	mean module capacitor voltage in branch x
v_{cm}	common-mode voltage
$v_{\mathrm{cm,3rdH}}$	third-harmonic component of common-mode voltage (used by third-harmonic injection)
$V_{C,\max}$	maximum allowed module capacitor voltage
$v_{\mathrm{cm,HF}}$	high-frequency component of the common-mode voltage
$V_{C,\min}$	selected minimum module capacitor voltage
v_{D}	voltage drop over a diode
$v_{\mathrm{D,ref}}$	voltage drop over a reference diode
V_{g}	grid voltage, RMS, line-to-line
v_{i}	input voltage
v'_{i}	inner voltage of the system connected to converter's input
v_{mod}	module's output voltage
v_{o}	output voltage
v'_{o}	inner voltage of the system connected to converter's output
$v_{\mathrm{o,err,DT}}$	output voltage error due to IGBT dead times
$v'_{\mathrm{o,err,DT}}$	output voltage error due to IGBT dead times caused during `STATE A` and `STATE B`
$v''_{\mathrm{o,err,DT}}$	output voltage error due to IGBT dead times caused during transition states
$v_{\mathrm{o,err,HF}}$	output voltage error due to HF modulation
$v_{\mathrm{o,err,}R\mathrm{b}}$	output voltage error due to branch resistances
$v_{\mathrm{o,err,T}}$	output voltage error due to transition states
$v_{\mathrm{o}x}$	output voltage of phase x
$v'_{\mathrm{o}x}$	inner voltage of phase x of the system connected to converter's output
V_{sN}	rated stator voltage, RMS, line-to-line
V_{step}	height of a voltage step
v_{T}	voltage drop over a transistor
$v_{\mathrm{T,ref}}$	voltage drop over a reference transistor
v_{wave}	wave propagation speed
$\Delta V_{C\mathrm{i},\max}$	maximum allowed peak-to-peak voltage variation at input capacitor within a single PWM period
ξ	converter losses relative to its rated apparent power
ζ	damping factor

1 Introduction

Power electronic converters currently play a very important role in numerous applications and are one of the key solutions increasing the efficiency of modern drive systems. Since the Insulated Gate Bipolar Transistor (IGBT) has become commercially mature, dc-ac converter solutions have been dominated by voltage-source inverters (VSI).

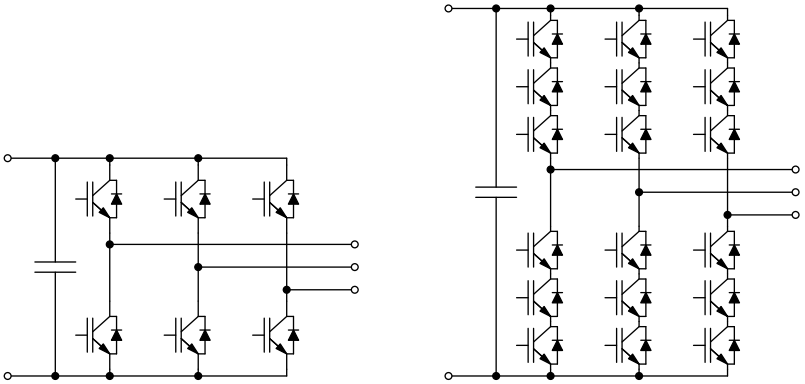


Figure 1.1: Two-level VSI. a) standard version, b) version with series-connected IGBTs to achieve higher voltages (in given example with three IGBTs in series)

In low voltage applications, two-level VSI (Figure 1.1a) is the standard converter topology for dc-ac conversion, due to its simple topology outline, low number of installed components, robustness and straight-forward control. Typical applications of two-level VSIs are grid-tied converters and machine drives. The application of a two-level VSI as a grid-tied converter has become very popular, as the converter's voltage harmonics can be influenced by the converter switching frequency and a bidirectional power flow is possible.

Although the application of the two-level VSI in variable-speed machine drives is generally advantageous, it leads to several issues. First, the converter's voltage harmonics cause additional losses in the machine. Second, the common-mode voltage generated by the converter causes bearing currents [1,2]. Finally, the reflections of the voltage wave cause a significant overvoltage at the machine terminals when long cables between the converter and machine are installed or the rate of voltage rise ($\mathrm{d}v/\mathrm{d}t$) of the semiconductor switches is too high [3]. These reflections must be taken into account, as they have the potential to destroy the applied insulation systems [4].

A seemingly straight-forward solution which addresses all three problems is to design the machine to withstand the additional losses and overvoltages and to isolate the motor bearings to limit the currents flowing through them. However, many machines have already been designed and built without consideration for operation with a power electronic converter (retrofit applications), or some of the aforementioned solutions cannot be applied with the available technologies for the machine design. In these cases, additional converter filters are often applied

(e.g. [5,6]). These can either be used to mitigate the long-cable voltage reflections (filtering only the very high frequencies in the MHz range), or to reduce all harmonics in the voltage spectrum, leading to almost pure sine voltage waveforms (so-called "sine filters"). While the first type of filters are complicated to design, the second type of filters are bulky and costly. Hence, it is generally desired to omit the filter when possible.

In high-power applications, the medium-voltage or high-voltage converters are applied. Aside from the grid-tied converters, the applications in medium-voltage drives, e.g. conveyors, fans, blowers, extruders, mills, compressors, and marine propulsion systems, are common [7, 8] .

For such applications, which require medium or high voltage, further challenges for the two-level VSI have to be addressed. There are two options that increase the achievable voltages of the two-level VSI. The first option is to use semiconductor switches capable of higher blocking voltages, such as high-voltage IGBTs (HV-IGBTs). However, since the maximum blocking voltage of the currently available semiconductor devices is limited to 6.5 kV, the maximum achievable voltage is limited as well. Additionally, these switches are significantly more costly than the standard low-voltage switches. The second option to increase the converter's voltage is to stack multiple identical semiconductor switches in series [see Figure 1.1b]. While very high voltages are also achievable using this method, the voltage sharing between the devices must be ensured using dedicated gate units or an additional passive balancing circuitry. Moreover, the low-inductive design of the critical commutation loops becomes more challenging. Additionally, when a very high number of semiconductor switches is applied, the reliability of the system is diminished. Finally, if the semiconductor switches are stacked in series, their $\mathrm{d}v/\mathrm{d}t$ is summed, massively increasing the significance of the long-cable reflection and bearing current problems for an application in medium-voltage drives.

A solution for medium-voltage drives that reduces the height of voltage steps at the converter output, and thus also the $\mathrm{d}v/\mathrm{d}t$ and the voltage harmonics, was introduced with multilevel converters. Because of the additional voltage levels resulting from the topologies, the voltage sharing between the devices can be ensured by control algorithms. The neutral-point-clamped multilevel converter [9] and the flying-capacitor multilevel converter [10] are the most common topologies. The main disadvantage of these topologies is their limited number of voltage levels for practical applications. Due to the increasing complexity of the control for the balancing of the dc-link capacitors and the physical construction with an increasing number of levels, only the three-level neutral-point-clamped multilevel converter is commercially available [8, 11]. Similarly, the number of voltage levels of flying-capacitor multilevel converter is limited to four in commercial applications, since each flying capacitor within the converter has to be designed for different requirements, and the balancing of the flying capacitors becomes more complex with the increasing number of levels [8, 11]. Furthermore, the switching frequencies of the converter have to be relatively high in order to reduce the capacitances of flying capacitors [8]. In summary, the scalability of these multilevel converters to a higher number of voltage levels is limited.

The first multilevel converter linearly scalable in voltage was the cascaded H-bridge (CHB) converter introduced by the company "Robicon" (Figure 1.2, [12]), and it is currently still a popular solution for medium-voltage drives. The converter topology is based on series-connected standardized modules, which are individually supplied by a complex isolating transformer. The phase shifts between the individual transformer windings are chosen to cancel the low-frequency grid harmonics caused by the diode rectifiers. Since the modules are galvanically insulated

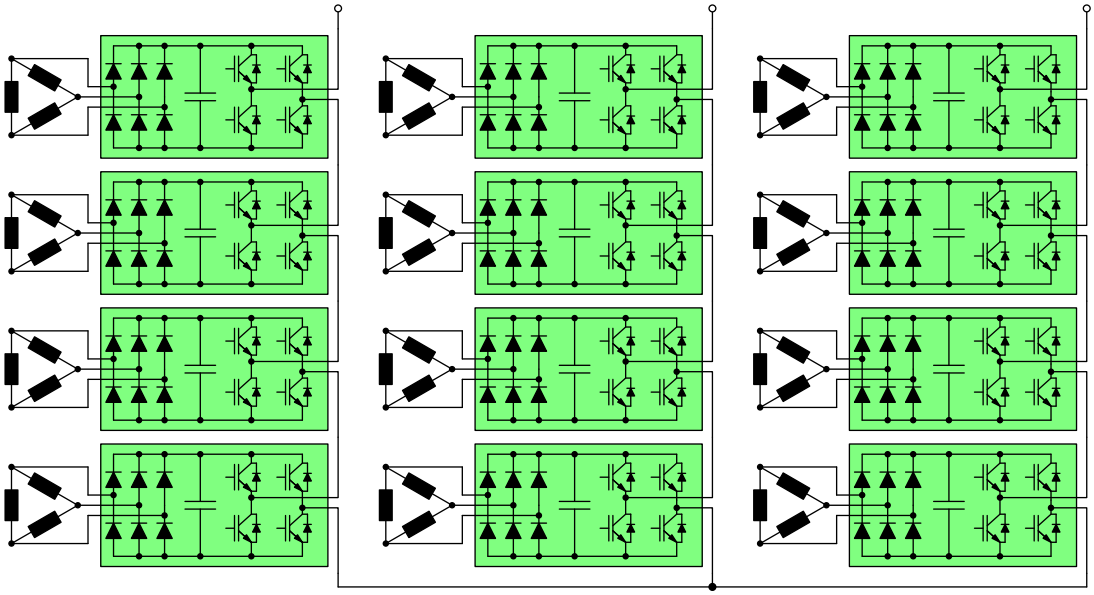


Figure 1.2: Cascaded H-bridge with multi-winding transformer. All displayed windings are coupled in a single transformer connected to the grid.

from each other, the number of voltage levels can be increased linearly, simply by adding additional modules. Furthermore, redundancy is possible, as faulty modules can be bypassed with a mechanical switch installed at the modules' output terminals [13]. The main drawback and limiting factor of this topology is the bulky and complex multi-winding transformer, which must be redesigned for each number of levels. Moreover, because of its complexity, this is mostly constructed as a dry-type transformer, limiting the converter's maximum achievable power.

A solution for dc-ac conversion, omitting the requirement of the bulky multi-winding transformer, was introduced with the Modular Multilevel Converter (MMC) proposed by Marquardt [14–16], which is depicted in Figure 1.3a. Because the modular construction provides superior voltage scalability, this topology has become a preferred solution for HVDC applications and is commercially available at several producers, i.e. *Siemens*, *ABB*, and *GE* [17–19]. According to a paper from 2017 [20], there are several on-shore and off-shore stations based on modular multilevel converters currently in use. While most of them are point-to-point connected, there are already a few multiterminal applications [20].

Although the modular multilevel converter possesses several properties that are very advantageous for medium-voltage drive systems, such as the aforementioned scalability, the small voltage steps, and possible redundancy, the application of the topology to medium-voltage drives is not widespread. The main reason for this limited adoption is that the amount of installed capacitance in the converter modules is inversely proportional to the converter's minimum output frequency. Hence, the converter's operation is unstable near machine standstill if no additional measures are applied. However, these measures, discussed extensively in the literature and also in this thesis, are a trade-off rather than a perfect solution. As a consequence, the modular multilevel converter is mostly utilized in applications requiring only low torque at low speeds. The MMCs for drive applications are commercially available at *Siemens* and *Benshaw* [21–23].

The main goal of this thesis is to show the derivation, implementation and investigation of a novel operation mode called "quasi-two-level PWM operation" for the modular multilevel

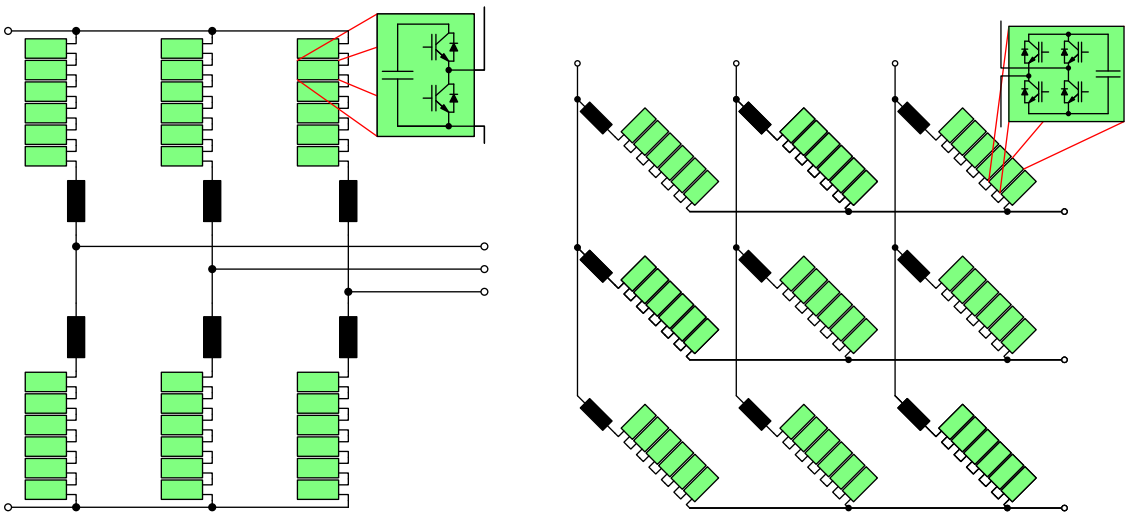


Figure 1.3: Modular multilevel topologies. a) modular multilevel converter (with half-bridge modules), b) modular multilevel matrix converter

converters, massively decreasing the installed module capacitance even at very low operation frequencies. To achieve this, a quasi-two-level PWM modulated voltage is applied at the converter output. Although this increases the current distortion at the machines, the machine inductance is expected to be high enough to keep this distortion sufficiently low. Moreover, all other crucial advantages, i.e. small voltage steps mitigating the long cable reflection issues, voltage scalability, and possible redundancy, are inherited from classical MMCs. This makes the operation mode a favorable candidate for low-speed medium-voltage drives.

In order to evaluate the converter suitability, the proposed operation mode will be compared to the conventional low-frequency mode of MMC, to the two-level VSI, and to the modular multilevel matrix converter (MMMC; 1.3b; proposed in [24] and explained in e.g. [25, 26]). The MMMC is, in contrary to the MMC, well-suited for low-frequency drive operation even with a full torque at zero speed [27, 28]. Nevertheless, the MMMC is solely an ac-ac converter topology and it is not commercially available on the market yet.

This thesis is structured as follows: In Chapter 2, the fundamental theory and operation of MMCs are explained. In Chapter 3, the quasi-two-level PWM operation mode is derived. The trade-offs and relationships within the design parameters of the quasi-two-level PWM-operated MMC are discussed in Chapter 4. The control scheme derivation and its implementation are described in Chapter 5. The proposed control is validated later using a downscaled converter prototype in Chapter 6. Furthermore, Chapter 6 provides a parameter variation study, showing the sensitivity of the proposed control to selected parameters. In Chapter 7, a further analysis of the different properties and extensions of the operation mode is presented. These include the voltage errors of the converter, the converter start-up process, and an application of discontinuous modulation. Finally, the design of the converter for machine drives is studied in Chapter 8 and compared to other feasible solutions such as the low-frequency mode of an MMC, the standard two-level VSI, and the MMMC. The conclusions are drawn in Chapter 9.

2 Fundamentals of Modular Multilevel Converters

This chapter explains the state of the art of the modular multilevel converter. It presents the topology and clarifies its functional principles. The common modulation and control strategies are briefly explained and possible model simplifications are shown. Using these simplifications, different operation modes are derived and demonstrated. At the end of the chapter, different approaches which enable the application of MMCs in variable-frequency drive systems are discussed.

2.1 Topology Description

The modular multilevel converter[1)] (MMC; Figure 2.1), is a single-phase to three-phase converter topology invented by Marquardt [14–16]. While it is typically considered to be a dc-ac topology, there are several applications in which an alternating-voltage link is connected to the single-phase terminals [30–33]. In this work, only the dc-ac topology will be considered. The dc link will be referred to as converter input and the ac system will be referred to as converter output.

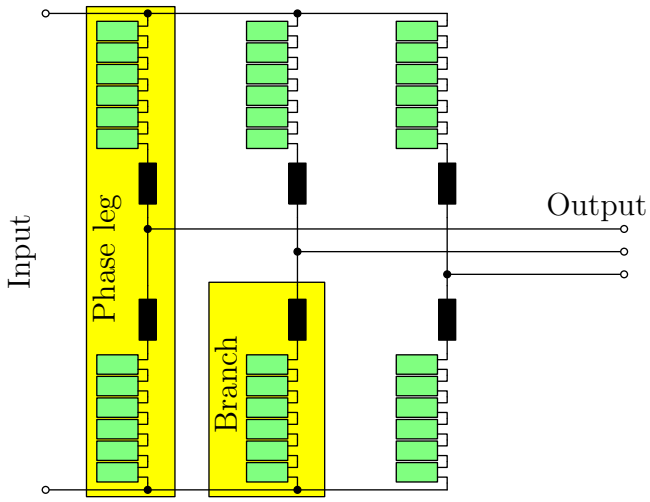


Figure 2.1: Modular multilevel converter topology (example with six modules per branch). The modules (filled green) can either be H-bridge modules or half-bridge modules (Figure 2.2).

[1)] Also known as Modular Multilevel Cascade Converter based on Double-Star Chopper (or Bridge) Cells [29].

As Figure 2.1 shows, the converter consists of three identical phase legs. Each of the converter's phase legs consists of two branches, comprising between several and few hundred identical modules and a branch inductor.[2)]

There are two typical[3)] types of modules which can be applied: H-bridge modules (Figure 2.2a) or half-bridge modules (Figure 2.2b).[4)] While it is possible to connect the module capacitor to the module output terminals in both directions with the H-bridge modules (Table 2.1), the output voltage of the half-bridge module can only be positive or zero (Table 2.2). Because of the lower number of installed semiconductor switches, the half-bridge modules are often preferred for the MMC drive applications. The H-bridge modules are advantageous for HVDC applications, when dc fault ride-through capability is desired.

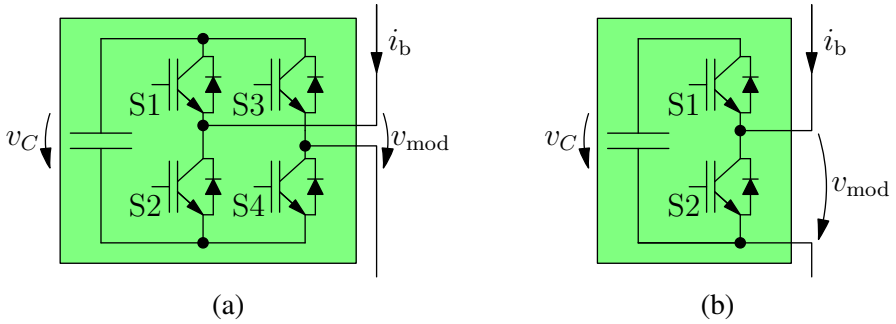


Figure 2.2: Typical module types used for an MMC: (a) H-bridge module, (b) half-bridge module. In this example, the modules are operated with IGBTs.

Table 2.1: Active switching states of an H-bridge module.

Switching state s	S1	S2	S3	S4	Module voltage v_mod
1	ON	OFF	OFF	ON	$+v_C$
0	ON	OFF	ON	OFF	0
0	OFF	ON	OFF	ON	0
-1	OFF	ON	ON	OFF	$-v_C$

Table 2.2: Active switching states of a half-bridge module.

Switching state s	S1	S2	Module voltage v_mod
1	ON	OFF	$+v_C$
0	OFF	ON	0

When the capacitor of a half-bridge module is connected to the output terminals ($s = 1$), the module's switching state is referred to in this thesis as "inserted". When the module terminals are short-circuited ($s = 0$), the module's switching state is referred to as "removed" or "short-circuited".

It is important to note that aside from the switching states listed in Table 2.1 and Table 2.2, there is also a passive state, in which all active semiconductor switches are turned off and only diodes

[2)] Some literature refers to branches as "arms" and to modules as "cells".

[3)] In the literature (e.g., [34, 35]), other types of modules are also presented. Nevertheless, these are relatively uncommon and thus will not be discussed in this thesis.

[4)] The H-bridge modules are also called "full-bridge modules" or "H-bridge cells" and the half-bridge modules are also called "chopper cells".

are conducting, depending on the current direction. However, this state occurs only during the converter start-up, converter turn off, or very shortly during the switching dead-time, which is necessary for the semiconductor switches.

Although various switching elements can be installed in the modules, IGBTs are typically applied (as depicted in Figure 2.2), because they provide numerous advantages. These include robustness, relatively high voltages and currents with sufficiently high achievable switching frequencies, and low costs per installed megawatt.

At this point, two important properties of the MMC can be noticed:

- The voltage sharing between the semiconductor switches (IGBTs) is not a significant problem because the voltage drops over the switches are clamped by the module capacitor, the voltage of which is kept within certain limits during the operation. This also enables the use of standard low-voltage semiconductor switches independently of the converter's output voltage level.
- The commutation loop, which must be designed to be low-inductive, is within the module. Therefore the connections between the modules do not have to be low-inductive and the complexity of the physical construction decreases.

These two properties are the main reasons for the superior scalability of the converter, as the achievable voltages can be increased simply by adding more modules in series to the others. Additionally, the option to produce large amounts of standardized modules could lead to cost reductions. The popularity of the CHB with an isolating transformer further supports this argument.

Another significant advantage of this topology is the straight-forward way of adding redundancy to the converter [16]. This is accomplished by stacking additional modules in each branch and installing a fast short-circuiting bi-directional switch[5)] at the output terminals of each module. If a module fails, this switch is activated and the module is removed from the modulation scheme, while the converter continues its operation uninterrupted. The options to implement these redundant modules in the control and modulation algorithms were studied e.g. in [37, 38]. In [39–42], techniques are shown which further increase the reliability of the MMC without the addition of more redundant modules by using a technique called neutral shift.

2.2 Branch Voltage Modulation and Module-Capacitor Voltage Balancing

As described above, the building blocks of MMCs are branches, each consisting of stacked modules and a branch inductor (Figure 2.3a). In order to be able to control the converter currents, a branch voltage v_b must be synthesized to match its setpoint value v_b^*. This is achieved by a modulation, leading to multilevel voltage waveforms, which match the setpoint voltage value as a mean value during a modulation period (Figure 2.3b).

[5)] Aside from mechanical solutions for the by-pass switch [17], a purposeful destruction of a press-pack thyristor is also feasible [36].

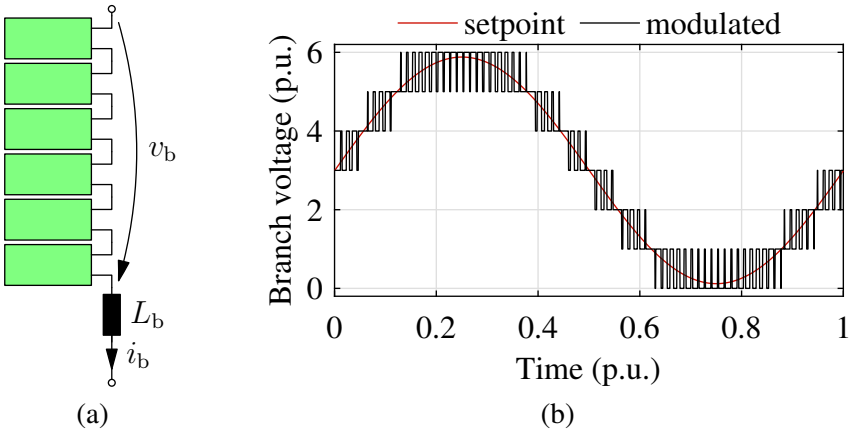


Figure 2.3: Branch of a modular multilevel converter (a), and an example of the modulated branch voltage (b). Example for six modules per branch. The base time is a single output period and the base voltage is a module capacitor voltage.

Since the modules' capacitors are not supplied by any external energy source, it is necessary to assure that the voltages of modules within the same branch are balanced. This task has to be accomplished in the modulation.

The approaches proposed in the literature which handle the modulation and balancing can be divided into two main philosophies:

- Multi-Carrier Modulation – there are different carriers for each module and the balancing is achieved either by adjusting duty-cycle setpoint values for each module or by re-arranging the carriers.
- Two-Step Modulation – the modulated waveform is determined in the first step (e.g., by PWM) and the particular modules applied to synthesize the waveform are selected in the second step in a way that keeps the modules' capacitor voltages balanced.

In the following sections, these philosophies are briefly explained for converters with half-bridge modules. Nevertheless, the principles are generally transferable to converters with H-bridge modules.

2.2.1 Multi-Carrier Modulation Approaches

Multi-carrier modulation is a common modulation approach used with classical multilevel converters (such as the neutral-point-clamped multilevel converter or the flying-capacitor multilevel converter). The approaches can be further divided into two groups: phase-shifted multi-carrier modulation and level-shifted multi-carrier modulation.

The **phase-shifted multi-carrier modulation**, shown in Figure 2.4a, employs one carrier for each module. These carriers are phase-shifted to each other. For a branch with half-bridge modules, the best voltage spectrum is achieved when the carriers are shifted by one n_mpb-th of period; with n_mpb being the number of installed modules per branch [43]. The switching signal for a particular module is generated using pulse-width modulation (PWM), by comparing its duty-cycle setpoint signal with the corresponding carrier.

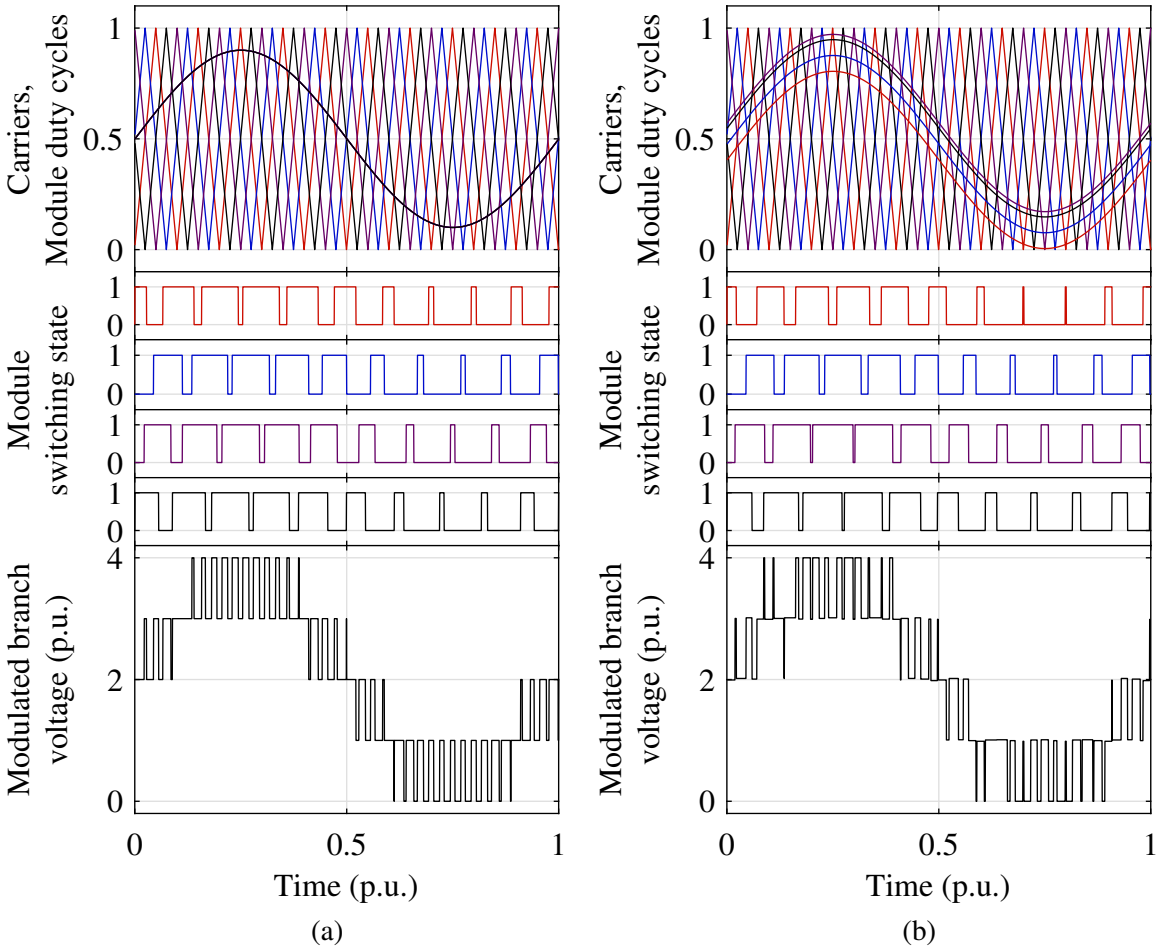


Figure 2.4: Example of phase-shifted multi-carrier modulation for one branch with four half-bridge modules: (a) the module capacitor voltages are balanced, (b) the module capacitor voltages are unbalanced. The base time is a single output period and the base voltage is a module capacitor voltage.

Using this modulation strategy, the module-capacitor voltages are theoretically balanced without any additional measures [44]. However, the quality of balancing is diminshed if the module capacitances are not equal. Moreover, the modules are not balanced at all when an integer ratio between the carrier frequency and the converter output frequency is chosen [45].

A better suited approach for achieving voltage balancing between the modules of phase-shifted multi-carrier modulated MMC is to modify the setpoint duty-cycle value for each module using proportional controllers [46]. The duty cycle of module i

$$\delta_i = \frac{v_\mathrm{b}^*}{\overline{v}_C \cdot n_\mathrm{mpb}} + \mathrm{sign}(i_\mathrm{b}) \cdot G_\mathrm{P} \cdot \left(v_C^* - v_{C,i}\right) \tag{2.1}$$

is calculated as a sum of two components. The first component is common for each module, calculated by dividing the branch voltage setpoint v_b^* evenly between all modules of the single branch. The second component is an output of a proportional controller with gain G_P, controlling the capacitor voltage value $v_{C,i}$ of module i to the module-capacitor voltage setpoint value v_C^*. The sign of the controller output is dependent on the branch current's direction, as this determines whether the module will be charged or discharged. For instance, if the capacitor voltage of a

module is too low and the branch current is positive, the duty cycle of this module is increased so that the module is charged for a longer period of time.

As Figure 2.4a and (2.1) indicate, the setpoint duty-cycle signals are identical for all modules when the modules' capacitor voltages are balanced. However, if the module-capacitor voltages are significantly unbalanced (and the duty-cycle setpoints are not identical for each module), the quality of the branch voltage spectrum is decreased [47], as can be indirectly observed in Figure 2.4b.

The main advantages of this modulation strategy are the evenly distributed switching losses between the modules [48] and the possibility to implement the modulation with carriers and controllers de-centrally at each module. The disadvantages are the aforementioned decrease in quality of the voltage spectrum when module capacitor voltages are unbalanced, and poor performance with very low carrier frequencies [49].

In order to improve the performance with low carrier frequencies, selection of the optimal carrier frequency selection was studied [48] and a rotation of the carriers was proposed [49].

The second group of multi-carrier approaches is **level-shifted multi-carrier modulation**. This is traditionally divided into three variants based on the arrangement of the carriers [35]:

- phase disposition (PD),
- phase opposition disposition (POD),
- alternative phase opposition disposition (APOD).

In Figure 2.5a, the PD modulation is demonstrated. As can be observed, the distribution of the switching signals is very uneven, leading to unbalanced capacitor voltages and uneven distribution of semiconductor losses. A significantly better distribution can be achieved by a permutation of the carrier positions for each module [50], as shown in Figure 2.5b.

Nevertheless, the carrier permutation can lead to additional switching instants (as can also be confirmed by comparison of Figure 2.4a and Figure 2.5b), which is undesirable for the semiconductor switching losses.

Although the simple carrier permutation without any additional balancing measures was proposed for MMC (e.g., [44]), the capacitor voltages are balanced only during symmetric operation [51] and thus this modulation technique must be extended to be practically applicable. An active balancing of the modules' capacitor voltages can be achieved by changing the arrangement of the particular carriers based on the module-capacitor voltages and the branch current direction [47][6)] or by assigning a particular carrier arrangement for a longer period of time [51, 52].

The described level-shifted multi-carrier modulation approach seems to be advantageous for cascaded H-bridge (CHB) with modules connected to photo-voltaic panels [47, 52]. In the vast majority of cases, level-shifted multi-carrier modulation is only used with an MMC to generate the scaled waveform in the first step of two-step modulation approaches.

[6)] This approach can theoretically be transformed into a two-step modulation approach if the carriers are rearranged very often.

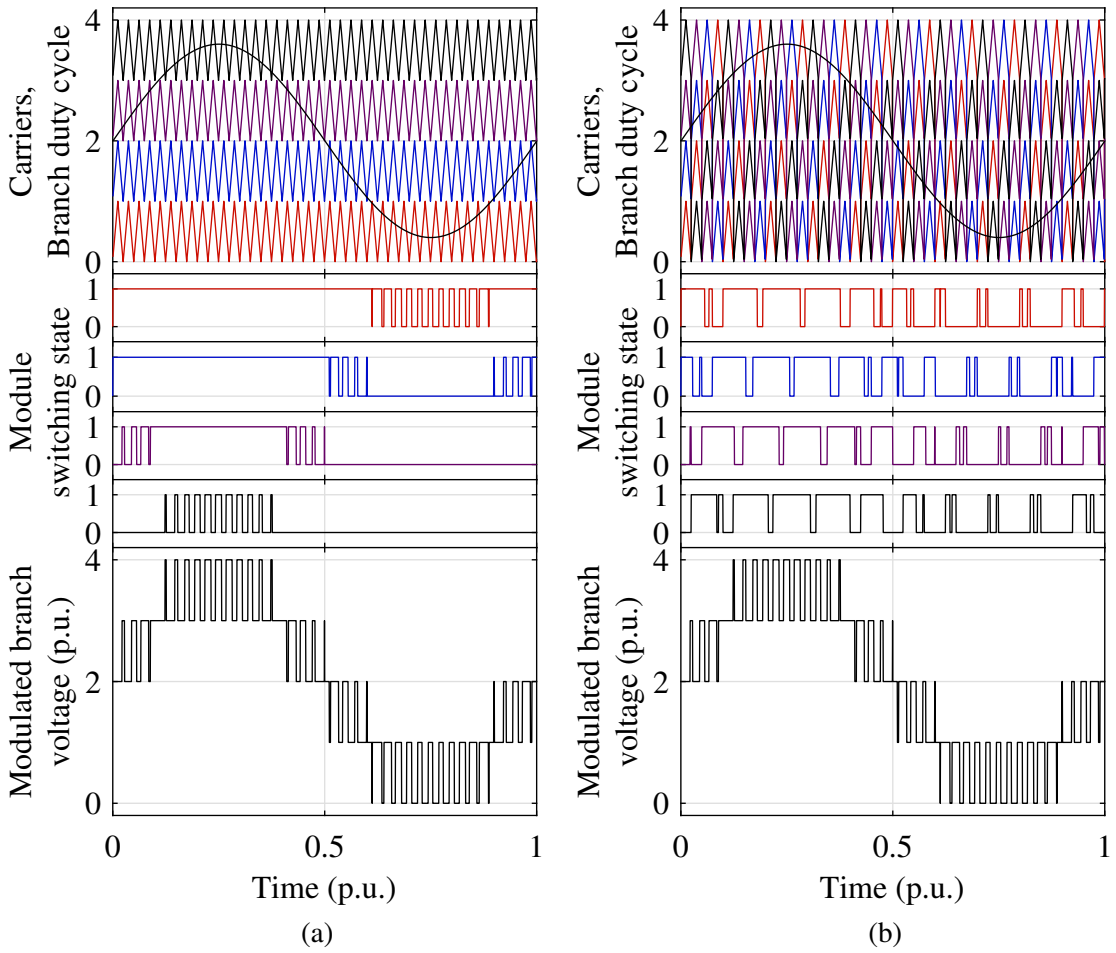


Figure 2.5: Example of level-shifted multi-carrier modulation for one branch: (a) normal, (b) carrier permutation. The base time is a single output period and the base voltage is a module capacitor voltage.

2.2.2 Two-Step Modulation Approaches

In the first step of **two-step modulation approaches**, the waveform of the modulated branch voltage scaled to a single module-capacitor voltage is determined, i.e. the number of inserted modules is assigned for each point in time. While the number of inserted modules is known after the first step, it is not determined which modules are going to be inserted in particular. This is determined in the second step dependent on the current direction in a manner that keeps the module-capacitor voltages balanced.

In the literature, many options for the first step, i.e. synthesizing the scaled waveform of the branch voltage, can be found. This can be achieved using a multi-carrier modulation approach (e.g., [53, 54] for phase-shifted multi-carrier modulation and [55] for level-shifted multi-carrier modulation), dedicated PWM algorithm [56–58] (shown in top of Figure 2.6), space-vector approach [16], nearest level modulation [59–61] (shown in bottom of Figure 2.6), an optimized pattern [62, 63], or even a waveform obtained from a tolerance band controller [64].

It is important to note that some of the methods mentioned do not directly generate the scaled branch voltage waveform, but the scaled output voltage waveform. The number of inserted modules in each branch is then calculated by a simple equation to keep the sum of inserted

modules in upper and lower branch constant. This is mainly the case when open-loop control, which does not control the internal MMC currents, is applied. This control approach is discussed in the next section.

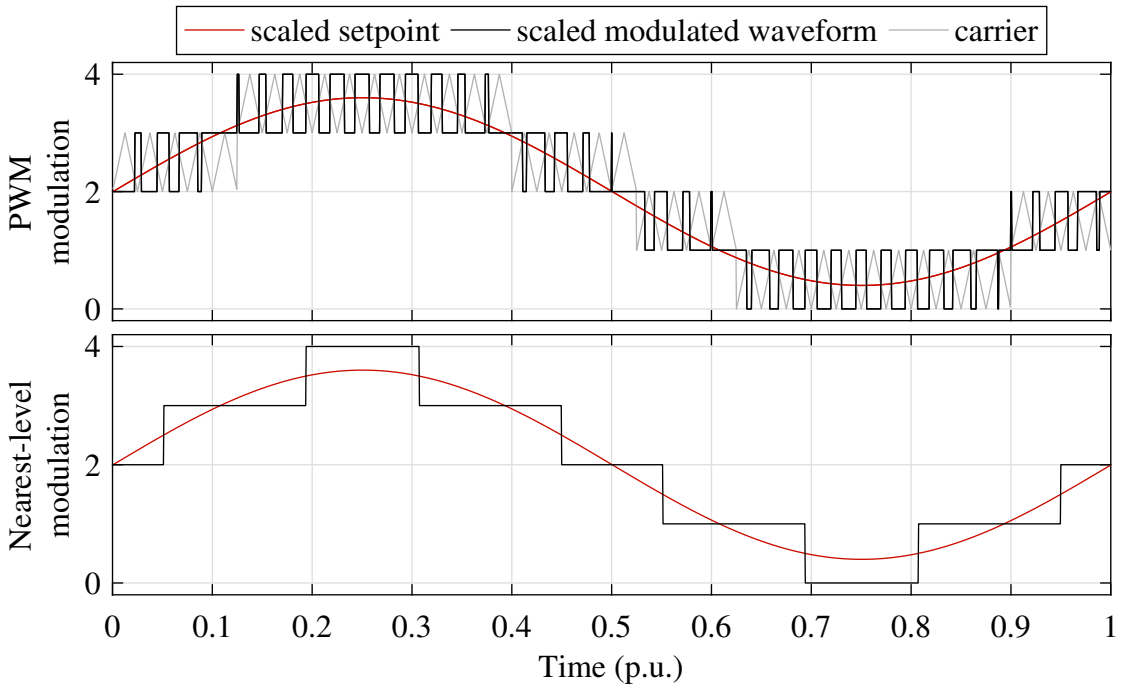


Figure 2.6: Two methods for synthesizing of the scaled branch-voltage waveform. The base time is a single output period.

Although some differences can be observed, the various PWM and multi-carrier techniques lead to comparable qualities of voltage spectra [65]. It can be shown that if a proper common-mode voltage injection is chosen, the space vector modulation leads to the same results as multi-carrier modulation strategies [66].

In contrast to these methods, the nearest level modulation leads to significantly worse spectra for a low number of modules per branch, as demonstrated in Figure 2.6, since the number of inserted modules in a branch is determined simply by rounding. On the other hand, this method is very simple and reduces semiconductor switching losses, as every module must (theoretically) be switched only once per output voltage period. Moreover, the disadvantage of lower spectrum quality becomes less relevant in HVDC applications, where the number of installed modules is very high.

More sophisticated strategies for reducing the disadvantages of low spectrum quality while maintaining low switching frequency are the optimized patterns. These are calculated offline to either cancel specific harmonics in the voltage spectrum (selective harmonic elimination) [62,67] or to optimize the voltage THD [63].

The original method [16] for the selection of the particular modules to be inserted (second modulation step) is based on sorting of the module capacitor voltages. If the branch current is positive and the inserted modules' capacitors are being charged, the modules with the lowest voltages are selected. When the current is negative and the inserted modules' capacitors are being discharged, the modules with the highest capacitor voltages are inserted. While this approach achieves superior quality of balancing, it can lead to very high and variable switching

frequency and poor distribution of switching losses between the modules dependent on the branch current, the module capacitance, and the chosen modulation period [48].

To limit the number of switching instants per module, different methods were proposed. The tolerance-band modulation methods [64] suggest freezing the sorted list of module-capacitor voltages until one of those exceeds the specified limits. This way the voltage balancing (and therefore also additional module switching) is stopped until it is urgently necessary. The main issue with this method is the difficulty to determine the tolerance band. Reference [53] proposes selecting only the newly inserted or removed modules resulting from the change in the required sum of inserted modules. This means, for instance, that if a module was once assigned to be short-circuited, its switching state cannot change until the required sum of inserted modules is increased. The approach in [59] minimizes the switching losses using a heuristic computational optimization. While predicting the current and voltage waveforms, this method leads to a higher alternation of inserted modules while the branch currents are low and less frequent module switching during the high branch currents.

To improve the distribution of the switching losses between the modules, [68] restricts the repeated switching of the previously switched module by adding an offset to its capacitor voltage. Reference [58] uses a finite-state machine to divide the pulses equally between the modules. Balancing is then achieved by swapping some part of the pulse between the module with the highest capacitor voltage and the module with the lowest capacitor voltage.

Nevertheless, the described improvements of the balancing approaches, which reduce the switching losses, lead to worse performance in voltage balancing and thus possibly to larger module capacitors [69, 70]. The selection of the proper methods for the first and second modulation steps depends on the given application, the desired output voltage quality, and the chosen maximum switching frequency.

2.3 Control Principle

Similar to modulation, there are numerous approaches to control the MMCs. In this section, the main philosophies are listed and the principles of the decoupled current control and the closed-loop branch-energy control are explained.

The first MMCs were proposed as open-loop controlled [16, 55], meaning they did not control the circulating currents (internal currents of the converter), the dc-link current, or the branch energies. With this open-loop approach, a stable operation can be achieved as long as there is sufficient passive damping in the system. However, the damping in the system is linked to converter losses, and thus is desired to be as low as possible. Consequently, the open-loop controlled MMCs can become unstable if a load step is applied [34]. Moreover, [71] suggests that an open-loop controlled MMC becomes unstable at certain operating points when operating as a rectifier.

Additionally, the open-loop control leads to a dominant second-harmonic component in the circulating currents, causing additional losses [72]. In the literature, designing the branch inductance accordingly high to shift the resonant frequency below the operation frequency [72] or applying a closed-loop controller to control the second-harmonic components in circulating currents to zero was proposed. The solutions for controllers are based on resonant controllers in

stationary reference frame [73–75], on proportional-integral controllers in rotating reference frame [76, 77] or even on repetitive controllers [78–80], which also control the other less significant even harmonics in the circulating currents.

Another approach, which increases the natural stability of the dc-ac MMC, is active damping or "active resistance" [81]. This is accomplished by adding additional components to the branch voltages, which emulates the presence of additional resistors in the branches. Consequently, the damping in the system is increased and the circulating-current second harmonic is decreased without an actual increase in losses. This method was also proved to be asymptotically stable in [82].

The last option, studied extensively in the literature, is the decoupled current control with an active branch-energy control, e.g. [46, 83–93]. In this philosophy, all currents are controlled to fit the desired values in order to actively balance the energies of the particular branches. While this approach is the most complex one, it has two crucial advantages. First, the energies can be controlled more dynamically, potentially leading to better transient behavior. Second, the circulating current is not only reduced but can have any required shape. The second property is necessary for the low-frequency modes, thereby enabling an application in variable-speed drives, since these operation modes require a precise control of the converters' internal currents [see Section 2.5.3].

In the following two sections, the decoupled current control and the branch-energy control based on generalized control theory for a class of modular multilevel topologies, proposed by Karwatzki *et al.* in [91–93], are shortly explained. Although the other approaches for the current and energy control mentioned above do not lead to significantly different results, the chosen theory gives a clear explanation of how the particular parts of the control scheme are designed.

2.3.1 Current Control

In the generalized control theory for a class of modular multilevel topologies [92], the current control is the inner control loop. Its main task is to control the converter currents by adjusting the branch voltages' setpoint values. The current control is derived using an averaged state-space model of the converter.

Assuming the modulation and module balancing are working perfectly, i.e. the module capacitor voltages within a branch are balanced and the modulation sets the required voltage within one modulation period exactly, an averaged model for an MMC branch can be introduced – Figure 2.7.

When this simplification is further applied to the converter topology, the averaged model of an MMC results – Figure 2.8. The input system is modeled as a voltage source v'_{i} with an inner inductance L_{i} and an inner resitance R_{i}. The output system's phases are modeled with inductors L_{o}, resistors R_{o} and voltage sources $v'_{\mathrm{o}1..3}$. The losses in the MMC's branches are represented by the resistors R_{b}. This model is the basis for the derivation of the state-space system. Applying the circuit analysis to the scheme in Figure 2.8, it can be stated that there are five independent currents that could be controlled.

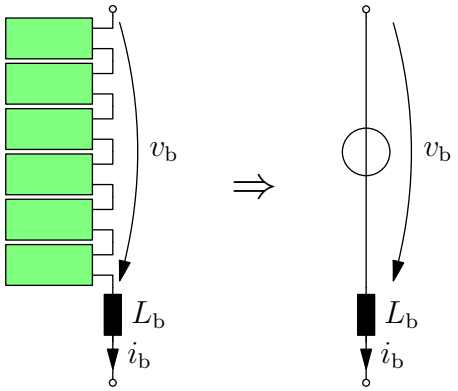


Figure 2.7: Averaged model of an MMC branch.

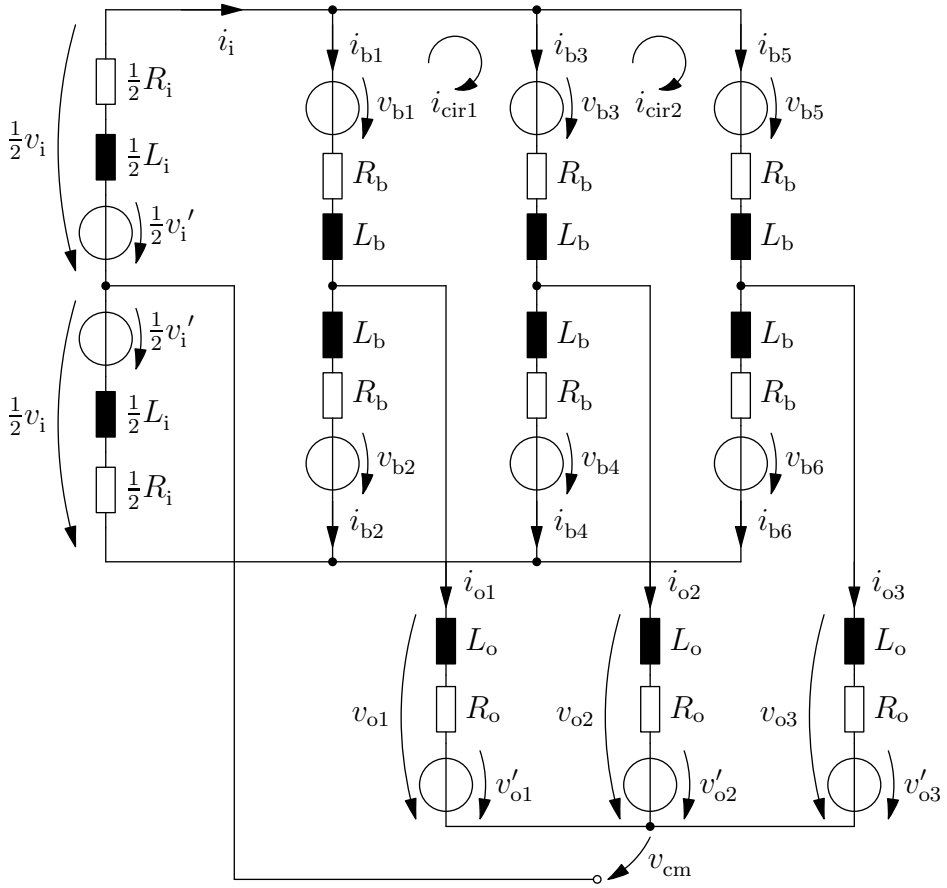


Figure 2.8: Averaged model of an MMC.

A straight-forward decision is to control the output currents (two independent variables). Frequently, the leg currents

$$\begin{bmatrix} i_\mathrm{leg1} \\ i_\mathrm{leg2} \\ i_\mathrm{leg3} \end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix} i_\mathrm{b1} + i_\mathrm{b2} \\ i_\mathrm{b3} + i_\mathrm{b4} \\ i_\mathrm{b5} + i_\mathrm{b6} \end{bmatrix} \quad , \tag{2.2}$$

flowing through both branches of a respective phase leg, are controlled (e.g., [46, 58, 94]). However, if the dc-link inductance L_i is considerably high, a cross-coupling between these currents follows [see equations in Appendix A].

Consequently, it is advantageous to control the dc-link current i_i, the output currents in alpha-beta coordinates (using an amplitude invariant Clarke's transformation)

$$\begin{bmatrix} i_{\mathrm{o}\alpha} \\ i_{\mathrm{o}\beta} \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{o}1} \\ i_{\mathrm{o}2} \\ i_{\mathrm{o}3} \end{bmatrix} \quad , \tag{2.3}$$

and two circulating currents

$$\begin{bmatrix} i_{\mathrm{cir}1} \\ i_{\mathrm{cir}2} \end{bmatrix} = \frac{1}{4} \cdot \begin{bmatrix} i_{\mathrm{b}1} + i_{\mathrm{b}2} - i_{\mathrm{b}3} - i_{\mathrm{b}4} \\ i_{\mathrm{b}3} + i_{\mathrm{b}4} - i_{\mathrm{b}5} - i_{\mathrm{b}6} \end{bmatrix} \tag{2.4}$$

flowing internally in the converter. These currents are chosen along the essential meshes of the topology depicted in Figure 2.8. It is important to note that other circulating current definitions are also possible (for example the definition obtained by alpha-beta transformation of leg currents [83, 84, 89]). Any of these definitions can be used, as long as the chosen definition describes two independent internal currents. The selection of the circulating current definition has no impact on the converter behavior, as the first definition can be linearly transformed to the second and vice versa.

The resulting state-space representation for the chosen state variables (currents) is

$$\frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\mathrm{cir}1} \\ i_{\mathrm{cir}2} \\ i_\mathrm{i} \\ i_{\mathrm{o}\alpha} \\ i_{\mathrm{o}\beta} \end{bmatrix} = \mathbf{A} \cdot \begin{bmatrix} i_{\mathrm{cir}1} \\ i_{\mathrm{cir}2} \\ i_\mathrm{i} \\ i_{\mathrm{o}\alpha} \\ i_{\mathrm{o}\beta} \end{bmatrix} + \mathbf{B} \cdot \begin{bmatrix} v_{\mathrm{b}1} \\ v_{\mathrm{b}2} \\ v_{\mathrm{b}3} \\ v_{\mathrm{b}4} \\ v_{\mathrm{b}5} \\ v_{\mathrm{b}6} \end{bmatrix} + \mathbf{E} \cdot \begin{bmatrix} v'_\mathrm{i} \\ v'_{\mathrm{o}\alpha} \\ v'_{\mathrm{o}\beta} \\ v'_{\mathrm{o}0} \end{bmatrix} \quad , \tag{2.5}$$

with system matrix

$$\mathbf{A} = \begin{bmatrix} -\frac{R_\mathrm{b}}{L_\mathrm{b}} & 0 & 0 & 0 & 0 \\ 0 & -\frac{R_\mathrm{b}}{L_\mathrm{b}} & 0 & 0 & 0 \\ 0 & 0 & -\frac{2R_\mathrm{b}+3R_\mathrm{i}}{2L_\mathrm{b}+3L_\mathrm{i}} & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_\mathrm{b}+2R_\mathrm{o}}{L_\mathrm{b}+2L_\mathrm{o}} & 0 \\ 0 & 0 & 0 & 0 & -\frac{R_\mathrm{b}+2R_\mathrm{o}}{L_\mathrm{b}+2L_\mathrm{o}} \end{bmatrix} \quad , \tag{2.6}$$

input matrix

$$\mathbf{B} = \begin{bmatrix} -\frac{1}{4L_\mathrm{b}} & -\frac{1}{4L_\mathrm{b}} & \frac{1}{4L_\mathrm{b}} & \frac{1}{4L_\mathrm{b}} & 0 & 0 \\ 0 & 0 & -\frac{1}{4L_\mathrm{b}} & -\frac{1}{4L_\mathrm{b}} & \frac{1}{4L_\mathrm{b}} & \frac{1}{4L_\mathrm{b}} \\ -\frac{1}{2L_\mathrm{b}+3L_\mathrm{i}} & -\frac{1}{2L_\mathrm{b}+3L_\mathrm{i}} & -\frac{1}{2L_\mathrm{b}+3L_\mathrm{i}} & -\frac{1}{2L_\mathrm{b}+3L_\mathrm{i}} & -\frac{1}{2L_\mathrm{b}+3L_\mathrm{i}} & -\frac{1}{2L_\mathrm{b}+3L_\mathrm{i}} \\ -\frac{2}{3L_\mathrm{b}+6L_\mathrm{o}} & \frac{2}{3L_\mathrm{b}+6L_\mathrm{o}} & \frac{1}{3L_\mathrm{b}+6L_\mathrm{o}} & -\frac{1}{3L_\mathrm{b}+6L_\mathrm{o}} & \frac{1}{3L_\mathrm{b}+6L_\mathrm{o}} & -\frac{1}{3L_\mathrm{b}+6L_\mathrm{o}} \\ 0 & 0 & -\frac{\sqrt{3}}{3L_\mathrm{b}+6L_\mathrm{o}} & \frac{\sqrt{3}}{3L_\mathrm{b}+6L_\mathrm{o}} & \frac{\sqrt{3}}{3L_\mathrm{b}+6L_\mathrm{o}} & -\frac{\sqrt{3}}{3L_\mathrm{b}+6L_\mathrm{o}} \end{bmatrix} \quad , \tag{2.7}$$

and disturbance matrix

$$\mathbf{E} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{3}{2L_\mathrm{b}+3L_\mathrm{i}} & 0 & 0 & 0 \\ 0 & -\frac{2}{L_\mathrm{b}+2L_\mathrm{o}} & 0 & 0 \\ 0 & 0 & -\frac{2}{L_\mathrm{b}+2L_\mathrm{o}} & 0 \end{bmatrix} . \tag{2.8}$$

The output system voltages $v'_{\mathrm{o}1}$, $v'_{\mathrm{o}2}$ and $v'_{\mathrm{o}3}$ are transformed by the Clarke's transformation:

$$\begin{bmatrix} v'_{\mathrm{o}\alpha} \\ v'_{\mathrm{o}\beta} \\ v'_{\mathrm{o}0} \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} v'_{\mathrm{o}1} \\ v'_{\mathrm{o}2} \\ v'_{\mathrm{o}3} \end{bmatrix} . \tag{2.9}$$

Using the derived state-space representation, the following observations can be made:

- There is no cross-coupling in the system, because the system matrix is diagonal.
- The effective inductance which affects the input current is composed of the input inductance and the branch inductances ($L_\mathrm{i} + \frac{2}{3}L_\mathrm{b}$), as visible in the disturbance matrix.
- The effective inductances which affect the output currents are composed of the output inductance and the branch inductances ($L_\mathrm{o} + \frac{1}{2}L_\mathrm{b}$), as visible in the disturbance matrix.
- The circulating currents are only affected by the branch inductances.
- The zero-voltage component $v'_{\mathrm{o}0}$ does not influence any of the currents.

Furthermore, the input matrix **B** explains how to adjust a particular current using the branch voltages without affecting the other currents:

- The input current can be adjusted by inserting an identical voltage component into all branch voltages.
- The output currents are adjusted by the difference between the voltage of the upper branches and the voltage of the lower branches.
- The circulating currents are adjusted by increasing the sum of branch voltages in one converter leg while decreasing the voltage sum in the other converter legs.

Although the input matrix **B** describes how the branch voltages influence the controlled currents, to design the current control it is necessary to know how the branch voltages must be synthesized to cause a desired change in the controlled currents. There are an infinite number of solutions which describe this relationship, since there are five independent variables (currents) which are controlled by six independent input variables (branch voltages). To overcome this problem, the common mode voltage

$$v_\mathrm{cm} = \frac{1}{6} \cdot (-v_\mathrm{b1} + v_\mathrm{b2} - v_\mathrm{b3} + v_\mathrm{b4} - v_\mathrm{b5} + v_\mathrm{b6}) \tag{2.10}$$

is used as a sixth independent variable, which should be controlled. Using (2.10), an extended input matrix

$$\mathbf{B}' = \begin{bmatrix} \mathbf{B} \\ -\frac{1}{6} & \frac{1}{6} & -\frac{1}{6} & \frac{1}{6} & -\frac{1}{6} & \frac{1}{6} \end{bmatrix} \tag{2.11}$$

can be derived, including an additional row for the common-mode voltage. In contrary to matrix $\mathbf{B}$, matrix $\mathbf{B}'$ can be inverted ($\mathbf{B}'^{-1}$). Hence it uniquely describes the relationship between the controlled variables and the setpoint branch voltages:

$$\begin{bmatrix} v^*_{\mathrm{b}1} \\ v^*_{\mathrm{b}2} \\ v^*_{\mathrm{b}3} \\ v^*_{\mathrm{b}4} \\ v^*_{\mathrm{b}5} \\ v^*_{\mathrm{b}6} \end{bmatrix} = \underbrace{\begin{bmatrix} -\frac{4L_\mathrm{b}}{3} & -\frac{2L_\mathrm{b}}{3} & -\frac{2L_\mathrm{b}+3L_\mathrm{i}}{6} & -\frac{L_\mathrm{b}+2L_\mathrm{o}}{2} & 0 & -1 \\ -\frac{4L_\mathrm{b}}{3} & -\frac{2L_\mathrm{b}}{3} & -\frac{2L_\mathrm{b}+3L_\mathrm{i}}{6} & \frac{L_\mathrm{b}+2L_\mathrm{o}}{2} & 0 & 1 \\ \frac{2L_\mathrm{b}}{3} & -\frac{2L_\mathrm{b}}{3} & -\frac{2L_\mathrm{b}+3L_\mathrm{i}}{6} & \frac{L_\mathrm{b}+2L_\mathrm{o}}{4} & -\frac{\sqrt{3}(L_\mathrm{b}+2L_\mathrm{o})}{4} & -1 \\ \frac{2L_\mathrm{b}}{3} & -\frac{2L_\mathrm{b}}{3} & -\frac{2L_\mathrm{b}+3L_\mathrm{i}}{6} & -\frac{L_\mathrm{b}+2L_\mathrm{o}}{4} & \frac{\sqrt{3}(L_\mathrm{b}+2L_\mathrm{o})}{4} & 1 \\ \frac{2L_\mathrm{b}}{3} & \frac{4L_\mathrm{b}}{3} & -\frac{2L_\mathrm{b}+3L_\mathrm{i}}{6} & \frac{L_\mathrm{b}+2L_\mathrm{o}}{4} & \frac{\sqrt{3}(L_\mathrm{b}+2L_\mathrm{o})}{4} & -1 \\ \frac{2L_\mathrm{b}}{3} & \frac{4L_\mathrm{b}}{3} & -\frac{2L_\mathrm{b}+3L_\mathrm{i}}{6} & -\frac{L_\mathrm{b}+2L_\mathrm{o}}{4} & -\frac{\sqrt{3}(L_\mathrm{b}+2L_\mathrm{o})}{4} & 1 \end{bmatrix}}_{\mathbf{B}'^{-1}} \cdot \begin{bmatrix} \mathrm{d}i^*_{\mathrm{cir}1}/\mathrm{d}t \\ \mathrm{d}i^*_{\mathrm{cir}2}/\mathrm{d}t \\ \mathrm{d}i^*_{\mathrm{i}}/\mathrm{d}t \\ \mathrm{d}i^*_{\mathrm{o}\alpha}/\mathrm{d}t \\ \mathrm{d}i^*_{\mathrm{o}\beta}/\mathrm{d}t \\ v^*_{\mathrm{cm}} \end{bmatrix} . \tag{2.12}$$

While the setpoint common-mode voltage v^*_{cm} is open-loop controlled, the setpoint values for the derivatives of the currents ($\mathrm{d}i^*_{\mathrm{cir}1}/\mathrm{d}t$, $\mathrm{d}i^*_{\mathrm{cir}2}/\mathrm{d}t$, $\mathrm{d}i^*_{\mathrm{i}}/\mathrm{d}t$, $\mathrm{d}i^*_{\mathrm{o}\alpha}/\mathrm{d}t$, $\mathrm{d}i^*_{\mathrm{o}\beta}/\mathrm{d}t$) are determined by close-loop controllers [see Figure 2.9]. The output currents can be controlled directly in alpha-beta coordinates using proportional-resonant (PR) controllers or using proportional-integral (PI) controllers in the rotating d,q-coordinates. The input current can be controlled with a PI controller. The circulating currents can contain several harmonic components at different frequencies. Hence the use of PR controllers with individual resonant controllers for each controlled frequency is recommended.

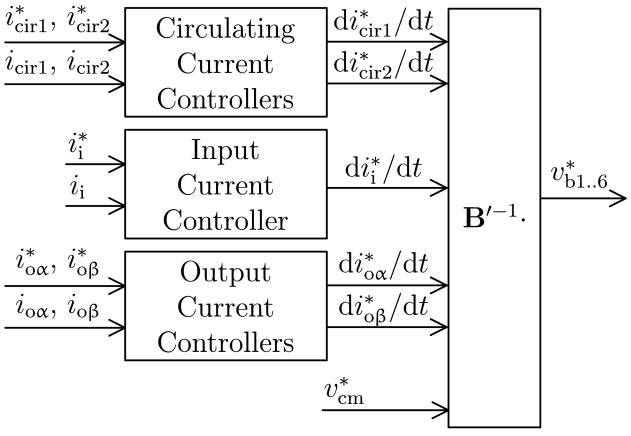


Figure 2.9: MMC current control based on generalized control theory.

For practical implementation, it is advantageous to include an additional feed-forward compensation of the disturbance matrix $\mathbf{E}$, as also presented in [93]. The influence of system matrix $\mathbf{A}$ is not compensated by an additional feed-forward control, since the resistances of the system are low, non-linear, and mostly unknown. The voltage drops over these resistances are compensated by the integral parts of the current controllers.

Since the decoupled current control has a unique solution for a selected set of controlled currents and the set of controlled currents is selected similarly in the literature, e.g., [83, 85, 87, 89, 93], there are only minor differences in these decoupled current control approaches.

2.3.2 Branch-Energy Control

The branch-energy control is the outer control loop, actively balancing the total energies stored in module capacitors between the MMC branches. Assuming the current control works perfectly, a further simplification of the MMC branch depicted in Figure 2.10 can be made. This simplification handles the MMC branch as an ideal current source and neglects the voltage drops over inductances and resistances.

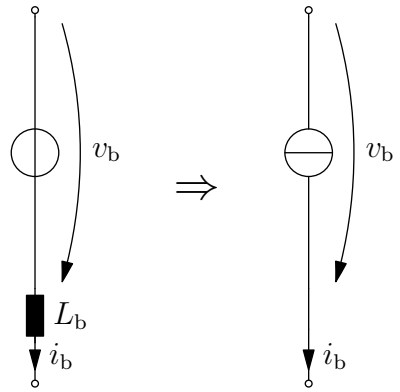


Figure 2.10: Further simplification of an MMC branch.

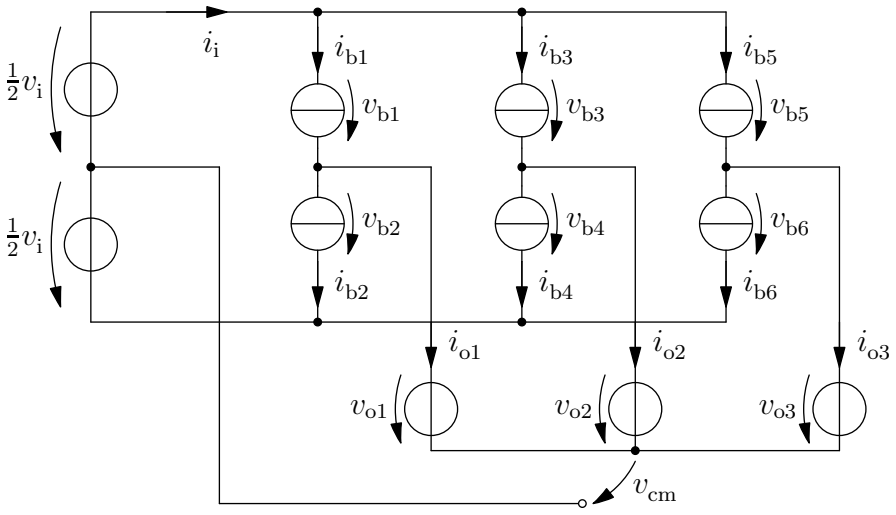


Figure 2.11: Model of an MMC, simplifying branches as current sources.

When this simplification is applied to the whole MMC and the converter losses are neglected

(Figure 2.11), the branch voltages

$$\begin{bmatrix} v_{\mathrm{b1}} \\ v_{\mathrm{b2}} \\ v_{\mathrm{b3}} \\ v_{\mathrm{b4}} \\ v_{\mathrm{b5}} \\ v_{\mathrm{b6}} \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \end{bmatrix} \cdot \frac{v_{\mathrm{i}}}{2} + \begin{bmatrix} -1 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & -1 \\ 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{\mathrm{o1}} \\ v_{\mathrm{o2}} \\ v_{\mathrm{o3}} \end{bmatrix} + \begin{bmatrix} -1 \\ 1 \\ -1 \\ 1 \\ -1 \\ 1 \end{bmatrix} \cdot v_{\mathrm{cm}} \tag{2.13}$$

and the branch currents

$$\begin{bmatrix} i_{\mathrm{b1}} \\ i_{\mathrm{b2}} \\ i_{\mathrm{b3}} \\ i_{\mathrm{b4}} \\ i_{\mathrm{b5}} \\ i_{\mathrm{b6}} \end{bmatrix} = \begin{bmatrix} \frac{1}{3} \\ \frac{1}{3} \\ \frac{1}{3} \\ \frac{1}{3} \\ \frac{1}{3} \\ \frac{1}{3} \end{bmatrix} \cdot i_{\mathrm{i}} + \begin{bmatrix} \frac{1}{2} & 0 & 0 \\ -\frac{1}{2} & 0 & 0 \\ 0 & \frac{1}{2} & 0 \\ 0 & -\frac{1}{2} & 0 \\ 0 & 0 & \frac{1}{2} \\ 0 & 0 & -\frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{o1}} \\ i_{\mathrm{o2}} \\ i_{\mathrm{o3}} \end{bmatrix} + \begin{bmatrix} \frac{4}{3} & \frac{2}{3} \\ \frac{4}{3} & \frac{2}{3} \\ \frac{2}{3} & \frac{2}{3} \\ -\frac{2}{3} & \frac{2}{3} \\ -\frac{2}{3} & \frac{2}{3} \\ -\frac{2}{3} & -\frac{4}{3} \\ -\frac{2}{3} & -\frac{4}{3} \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{cir1}} \\ i_{\mathrm{cir2}} \end{bmatrix} \tag{2.14}$$

can be expressed as a function of the input voltage, the input current, the output voltages, the output currents, the common-mode voltage, and the circulating currents.

For the design of the energy control scheme, the input current

$$i_{\mathrm{i}} = I_{\mathrm{i}} \tag{2.15}$$

is assumed to be a direct current, the input voltage

$$v_{\mathrm{i}} = V_{\mathrm{i}} \tag{2.16}$$

to be a direct voltage, and the output currents

$$\begin{bmatrix} i_{\mathrm{o1}} \\ i_{\mathrm{o2}} \\ i_{\mathrm{o3}} \end{bmatrix} = \sqrt{2} \cdot I_{\mathrm{o}} \cdot \begin{bmatrix} \cos(\omega \cdot t - \varphi) \\ \cos(\omega \cdot t - \frac{2 \cdot \pi}{3} - \varphi) \\ \cos(\omega \cdot t - \frac{4 \cdot \pi}{3} - \varphi) \end{bmatrix} \tag{2.17}$$

and the output voltages

$$\begin{bmatrix} v_{\mathrm{o1}} \\ v_{\mathrm{o2}} \\ v_{\mathrm{o3}} \end{bmatrix} = \sqrt{2} \cdot V_{\mathrm{o}} \cdot \begin{bmatrix} \cos(\omega \cdot t) \\ \cos(\omega \cdot t - \frac{2 \cdot \pi}{3}) \\ \cos(\omega \cdot t - \frac{4 \cdot \pi}{3}) \end{bmatrix} \tag{2.18}$$

are assumed to each solely include a single component at angular frequency $\omega = 2\pi f$.

The common-mode voltage

$$v_{\mathrm{cm}} = V_{\mathrm{cm0}} + \sqrt{2} \cdot V_{\mathrm{cm}\alpha} \cdot \cos(\omega \cdot t - \varphi) + \sqrt{2} \cdot V_{\mathrm{cm}\beta} \cdot \sin(\omega \cdot t - \varphi) + \sqrt{2} \cdot V_{\mathrm{cm}x} \cdot \cos(\omega_x \cdot t) \tag{2.19}$$

and circulating currents

$$\begin{bmatrix} i_{\mathrm{cir1}} \\ i_{\mathrm{cir2}} \end{bmatrix} = \begin{bmatrix} I_{\mathrm{cir10}} \\ I_{\mathrm{cir20}} \end{bmatrix} + \sqrt{2} \cdot \begin{bmatrix} I_{\mathrm{cir1\alpha}} \\ I_{\mathrm{cir2\alpha}} \end{bmatrix} \cdot \cos(\omega \cdot t) + \sqrt{2} \cdot \begin{bmatrix} I_{\mathrm{cir1\beta}} \\ I_{\mathrm{cir2\beta}} \end{bmatrix} \cdot \sin(\omega \cdot t) \ldots + \sqrt{2} \cdot \begin{bmatrix} I_{\mathrm{cir1}x} \\ I_{\mathrm{cir2}x} \end{bmatrix} \cdot \cos(\omega_x \cdot t) \quad (2.20)$$

are chosen to contain components at the input frequency (0 Hz), the output frequency (ω) and at the angular frequency ω_x ($\omega_x \neq \omega$ and $\omega_x \neq 0$).

By substituting (2.17) – (2.20) into (2.13) and (2.14), the branch currents and the branch voltages can be expressed as functions of time. These expressions can be further used to calculate the branch powers

$$p_{\mathrm{b}k}(t) = v_{\mathrm{b}k}(t) \cdot i_{\mathrm{b}k}(t), \quad k = 1..6 \quad . \quad (2.21)$$

By applying a Fourier transformation to the resulting branch power equations, the branch-power components at zero frequency can be isolated. These components are the degrees of freedom, which are capable of transmitting energy between branches and thus can be used for the branch-energy control. The branch-power components at frequencies higher than zero only determine the energy variation in the branches and can be ignored during the branch-energy controller design. As shown in Table 2.3, the available degrees of freedom can be divided into four groups according to their properties.

Table 2.3: Degrees of freedom for branch-energy control.

Group I	Group II	Group III	Group IV
ΔP	$I_{\mathrm{cir1\alpha}} \cdot V_{\mathrm{o}}$, $I_{\mathrm{cir2\alpha}} \cdot V_{\mathrm{o}}$,	$V_{\mathrm{cm\alpha}} \cdot I_{\mathrm{o}}$,	$I_{\mathrm{cir1}x} \cdot V_{\mathrm{cm}x}$,
	$I_{\mathrm{cir1\beta}} \cdot V_{\mathrm{o}}$, $I_{\mathrm{cir2\beta}} \cdot V_{\mathrm{o}}$,	$V_{\mathrm{cm\beta}} \cdot I_{\mathrm{o}}$,	$I_{\mathrm{cir2}x} \cdot V_{\mathrm{cm}x}$
	$I_{\mathrm{cir10}} \cdot V_{\mathrm{i}}$, $I_{\mathrm{cir20}} \cdot V_{\mathrm{i}}$	$V_{\mathrm{cm0}} \cdot I_{\mathrm{i}}$	

The first group consists only of the difference between the input power P_{i} and the output power P_{o}

$$\Delta P = P_{\mathrm{i}} - P_{\mathrm{o}} = V_{\mathrm{i}} \cdot I_{\mathrm{i}} - 3 \cdot V_{\mathrm{o}} \cdot I_{\mathrm{o}} \cdot \cos\varphi \quad . \quad (2.22)$$

This degree of freedom must always be used in the control scheme, as it controls the total amount of energy stored in the converter's modules.

The second group includes the degrees of freedom resulting from the combination of the circulating currents' components and the input-voltage and output-voltage components. The third group combines the common-mode voltage components with the input current and the output currents. The components from the second and third group should not be used for the branch-energy control simultaneously, as they would cause additional cross-coupling power components resulting from the components of the common-mode voltage and circulating currents [92]. To date, no methodology has been proposed which uses both groups at the same time while omitting the cross coupling.

The fourth group comprises the combination of common-mode voltage components and circulating current components at the frequency ω_x.

In most cases, it is sufficient to only use the components of the first group and the second group. This is advantageous because the energy control uses only currents and thus the maximum branch voltage, which must be synthesized, is increased only marginally (due to the voltage drops over inductances).

There are six branch energies which must be controlled by branch powers, but seven power components from the first and second groups to control these energies. For this case, the generalized control theory [93] proposes searching for an optimal solution for minimizing the RMS value of branch currents. This leads to the optimized solution

$$\begin{bmatrix} I_{\mathrm{cir10}} \cdot V_{\mathrm{i}} \\ I_{\mathrm{cir20}} \cdot V_{\mathrm{i}} \\ I_{\mathrm{cir1\alpha}} \cdot V_{\mathrm{o}} \\ I_{\mathrm{cir1\beta}} \cdot V_{\mathrm{o}} \\ I_{\mathrm{cir2\alpha}} \cdot V_{\mathrm{o}} \\ I_{\mathrm{cir2\beta}} \cdot V_{\mathrm{o}} \\ \Delta P \end{bmatrix} = \underbrace{\begin{bmatrix} \frac{1}{2} & \frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} & 0 & 0 \\ 0 & 0 & \frac{1}{2} & \frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{3}{8} & \frac{3}{8} & -\frac{1}{8} & \frac{1}{8} & \frac{1}{8} & -\frac{1}{8} \\ -\frac{1}{\sqrt{3}\cdot 8} & \frac{1}{\sqrt{3}\cdot 8} & \frac{5}{\sqrt{3}\cdot 8} & -\frac{5}{\sqrt{3}\cdot 8} & -\frac{1}{\sqrt{3}\cdot 8} & \frac{1}{\sqrt{3}\cdot 8} \\ 0 & 0 & \frac{1}{4} & -\frac{1}{4} & -\frac{1}{4} & \frac{1}{4} \\ \frac{1}{\sqrt{3}\cdot 4} & -\frac{1}{\sqrt{3}\cdot 4} & -\frac{1}{\sqrt{3}\cdot 2} & \frac{1}{\sqrt{3}\cdot 2} & -\frac{1}{\sqrt{3}\cdot 2} & \frac{1}{\sqrt{3}\cdot 2} \\ 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}}_{\mathbf{M}_{\mathrm{N}}} \cdot \begin{bmatrix} P^*_{\mathrm{b1}} \\ P^*_{\mathrm{b2}} \\ P^*_{\mathrm{b3}} \\ P^*_{\mathrm{b4}} \\ P^*_{\mathrm{b5}} \\ P^*_{\mathrm{b6}} \end{bmatrix} \quad , \tag{2.23}$$

defining how the required branch powers $P^*_{\mathrm{b1..6}}$, which control the branch energies, should be synthesized using the chosen degrees of freedom[7)]. Please note that the solution can also be extended by the fourth group [93]. This is advantageous if there is some common-mode voltage component already generated for other reasons – e.g. the third-harmonic injection.

Nevertheless, there are also applications, e.g. motor drives, in which the output voltages can approach zero. Consequently, the circulating currents would have to be exceedingly high to generate an active power using the degrees of freedom from the second group. Reference [93] proposes using the components of the first group, third group and fourth group simultaneously. The fourth group is a welcome set of degrees of freedom in this case, because a high-frequency component must be injected into the common-mode voltage due to Low-Frequency Mode (described later). The main issue with this solution is the degree of freedom $V_{\mathrm{cm0}} \cdot I_{\mathrm{i}}$, as the input current is expected to be very low at low machine speeds. The solution for the energy control used with Low-Frequency Mode in this thesis is based on allowing an additional input-current distortion at frequency ω_x:

$$i_{\mathrm{i}} = I_{\mathrm{i}} + \sqrt{2} \cdot I_{\mathrm{i}x} \cdot \cos(\omega_x t) \quad . \tag{2.24}$$

This leads to an additional degree of freedom $I_{\mathrm{i}x} \cdot V_{\mathrm{cm}x}$ in the fourth group.

Choosing the six independent branch power components to control the six branch energies, a

[7)] According to [93], this solution for branch-energy control can be transformed into the one presented in [83].

unique solution

$$\begin{bmatrix} V_{\mathrm{cm}\alpha} \cdot I_{\mathrm{o}} \\ V_{\mathrm{cm}\beta} \cdot I_{\mathrm{o}} \\ I_{\mathrm{cir}1x} \cdot V_{\mathrm{cm}x} \\ I_{\mathrm{cir}2x} \cdot V_{\mathrm{cm}x} \\ I_{\mathrm{i}x} \cdot V_{\mathrm{cm}x} \\ \Delta P \end{bmatrix} = \underbrace{\begin{bmatrix} -\frac{2}{3} & -\frac{2}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \\ 0 & 0 & -\frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \\ -\frac{1}{4} & \frac{1}{4} & \frac{1}{4} & -\frac{1}{4} & 0 & 0 \\ 0 & 0 & -\frac{1}{4} & \frac{1}{4} & \frac{1}{4} & -\frac{1}{4} \\ -\frac{1}{2} & \frac{1}{2} & -\frac{1}{2} & \frac{1}{2} & -\frac{1}{2} & \frac{1}{2} \\ 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}}_{\mathbf{M}_{\mathrm{LF}}} \cdot \begin{bmatrix} P^*_{\mathrm{b}1} \\ P^*_{\mathrm{b}2} \\ P^*_{\mathrm{b}3} \\ P^*_{\mathrm{b}4} \\ P^*_{\mathrm{b}5} \\ P^*_{\mathrm{b}6} \end{bmatrix} \tag{2.25}$$

can be found explicitly.

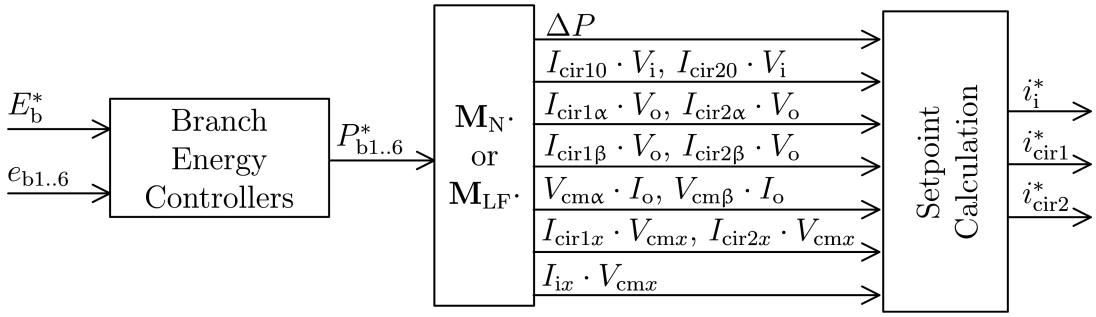


Figure 2.12: MMC branch-energy control based on generalized control theory.

The resulting branch-energy control scheme is depicted in Figure 2.12. The branch energies $e_{\mathrm{b}1..6}$ are calculated as the sum of module capacitor energies for each branch using the measured module voltage values and the module capacitance. These are controlled to their setpoint value E^*_{b} by six independent PI controllers, determining the branch power setpoint values $P^*_{\mathrm{b}1..6}$. The branch powers are then transformed either by matrix $\mathbf{M}_{\mathrm{N}}$ (2.23) during the normal operation or by matrix $\mathbf{M}_{\mathrm{LF}}$ (2.25) during low machine speeds into the selected degrees of freedom. These transformed values, together with the voltage values V_{o}, V_{i} and $V_{\mathrm{cm}x}$, the current value I_{o}, and the system angles ωt, $\omega_x t$ and φ, can be used to calculate the setpoint value for the input current, the circulating currents, and the common-mode voltage. These setpoint values are later used in the current control.

2.4 Variations of the MMC Topology

Different variations of the MMC topology can be found in the literature. These include either the coupling of the branch inductors or adding a central dc-link capacitor at the converter input, both of which are discussed below.

2.4.1 Center-Tapped Branch Inductors

The center-tapped branch inductors are commonly used for MMCs [46, 95, 96] to reduce the inductor size and costs, and to reduce the inductance which affects the output currents [96]. The modified MMC with center-tapped branch inductors is depicted in Figure 2.13.

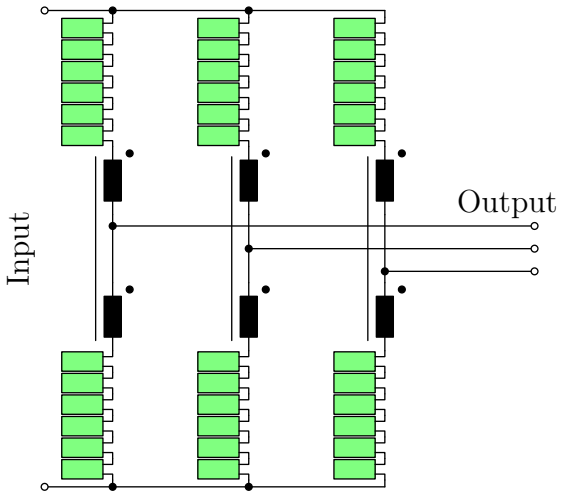


Figure 2.13: Scheme of an MMC with center-tapped branch inductors.

Assuming the branch inductors are ideally coupled with a common-mode inductance L_{leg} and the differential-mode inductance is zero, the state-space representation matrices change accordingly:

$$\mathbf{A} = \begin{bmatrix} -\frac{2R_\text{b}}{L_\text{leg}} & 0 & 0 & 0 & 0 \\ 0 & -\frac{2R_\text{b}}{L_\text{leg}} & 0 & 0 & 0 \\ 0 & 0 & -\frac{2R_\text{b}+3R_\text{i}}{L_\text{leg}+3L_\text{i}} & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_\text{b}+2R_\text{o}}{2L_\text{o}} & 0 \\ 0 & 0 & 0 & 0 & -\frac{R_\text{b}+2R_\text{o}}{2L_\text{o}} \end{bmatrix}, \tag{2.26}$$

$$\mathbf{B} = \begin{bmatrix} -\frac{1}{2L_\text{leg}} & -\frac{1}{2L_\text{leg}} & \frac{1}{2L_\text{leg}} & \frac{1}{2L_\text{leg}} & 0 & 0 \\ 0 & 0 & -\frac{1}{2L_\text{leg}} & -\frac{1}{2L_\text{leg}} & \frac{1}{2L_\text{leg}} & \frac{1}{2L_\text{leg}} \\ -\frac{1}{L_\text{leg}+3L_\text{i}} & -\frac{1}{L_\text{leg}+3L_\text{i}} & -\frac{1}{L_\text{leg}+3L_\text{i}} & -\frac{1}{L_\text{leg}+3L_\text{i}} & -\frac{1}{L_\text{leg}+3L_\text{i}} & -\frac{1}{L_\text{leg}+3L_\text{i}} \\ -\frac{1}{3L_\text{o}} & \frac{1}{3L_\text{o}} & \frac{1}{6L_\text{o}} & -\frac{1}{6L_\text{o}} & \frac{1}{6L_\text{o}} & -\frac{1}{6L_\text{o}} \\ 0 & 0 & -\frac{\sqrt{3}}{6L_\text{o}} & \frac{\sqrt{3}}{6L_\text{o}} & \frac{\sqrt{3}}{6L_\text{o}} & -\frac{\sqrt{3}}{6L_\text{o}} \end{bmatrix}, \tag{2.27}$$

$$\mathbf{E} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{3}{L_\text{leg}+3L_\text{i}} & 0 & 0 & 0 \\ 0 & -\frac{1}{L_\text{o}} & 0 & 0 \\ 0 & 0 & -\frac{1}{L_\text{o}} & 0 \end{bmatrix}. \tag{2.28}$$

As can be seen in the matrices, the influence of the branch inductors on the output current is completely eliminated.

A deeper analysis (including for an additional coupling topology) and the impact of the coupling on the design can be found in [96].

2.4.2 Central DC-Link Capacitance

The central dc-link capacitance can be added to an MMC (Figure 2.14) when an additional distortion of the input current is utilized for energy balancing.

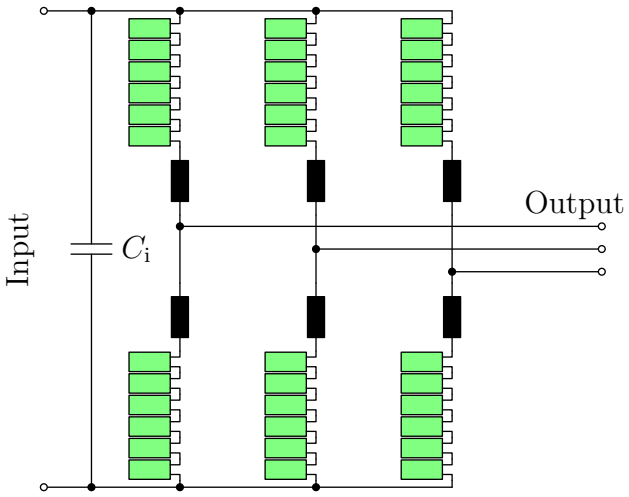


Figure 2.14: Modular multilevel converter topology with an additional DC-link capacitor.

The impact of the dc-link capacitance on the converter is that the input inductance L_i and the input resistance R_i are almost reduced to zero. Consequently, this removes the cross-coupling between the leg currents mentioned in Section 2.3.1 and each phase leg of the converter can be controlled independently.

2.5 Operation Modes

In this section, the converter operation modes are derived and explained. The basis for the steady-state investigation is the simplified MMC model shown in Figure 2.11 used for the derivation of the energy control in Section 2.3.2, which substitutes the converter branches with controlled current sources.

The corresponding equations (2.13) and (2.14) define how the branch voltages and the branch currents are determined dependent on output currents $i_{\mathrm{o}1..3}$, output voltages $v_{\mathrm{o}1..3}$, input current i_i, input voltage v_i, circulating currents $i_{\mathrm{cir}1..2}$ and common-mode voltage v_cm. Identically to the energy control derivation, the input current and input voltage are assumed to be constant values (2.15), (2.16), and the output currents and the output voltages to be symmetric three-phase systems with only a fundamental frequency component (2.17), (2.18). In the following investigations, the additional current and voltage components obtained from the energy control are assumed to be zero.

It is important to note that if half-bridge modules are applied, the branch voltages cannot be negative. Consequently, by observing (2.14), it can be concluded that the sum of the output voltage and the common-mode voltages in each phase must always be lower or equal to the half of the input voltage:

$$|v_{\mathrm{o},k} + v_\mathrm{cm}| \leq \frac{v_\mathrm{i}}{2}, \quad k = 1..3 \quad . \tag{2.29}$$

If H-bridge modules are utilized, this limitation does not apply.

While the output voltages, the output currents and the input voltage are determined by outside circumstances (e.g., the chosen operating point of an MMC-driven machine or the available input voltage source), the steady-state input current is chosen to fulfill the power balance:

$$V_\mathrm{i} \cdot I_\mathrm{i} = 3 \cdot V_\mathrm{o} \cdot I_\mathrm{o} \cdot \cos\varphi \quad , \tag{2.30}$$

and the circulating currents and common-mode voltage are degrees of freedom (besides the negligible components necessary for energy control). Using these degrees of freedom, the properties of the converter can be significantly influenced. The different strategies for using these degrees of freedom are called MMC operation modes.

Next to the branch voltage waveforms and the branch current waveforms, the branch energy time function

$$e_{\mathrm{b}k}(t) = \int p_{\mathrm{b}k}(t)\,\mathrm{d}t = \int i_{\mathrm{b}k}(t) \cdot v_{\mathrm{b}k}(t)\,\mathrm{d}t, \quad k = 1..6 \tag{2.31}$$

is a significant design indicator, as the branch energy variation

$$\Delta E_{\mathrm{b}k} = \max(e_{\mathrm{b}k}(t)) - \min(e_{\mathrm{b}k}(t)), \quad k = 1..6 \tag{2.32}$$

determines the size of module capacitors. The required module capacitance is directly proportional to the maximum branch energy variation for a defined maximum capacitor voltage ripple.

In the following investigations of the MMC operation modes, the converter waveforms are plotted for an exemplary operation point, the parameters of which are summarized in Table 2.4. The circulating currents and common-mode voltage are chosen according to the operation mode. Note that only selected well-known operation modes are derived in this section. The other operation modes are shortly discussed in Section 2.6.

In the control implementation, the operation mode dependent values for the circulating currents and the common-mode voltage are simply added to the setpoints obtained from the branch-energy control, behaving as a feed-forward control.

Table 2.4: Parameters of the operation point used for the investigations of different operation modes.

Parameter		Value
Transmitted active power	P	10 MW
Output power factor	$\cos\varphi$	0.95
Input voltage	V_i	10 kV
Output voltage	V_o	2.3 kV
Output frequency	f	10 Hz

2.5.1 Normal Operation Mode

In the normal operation mode, both circulating currents

$$\begin{bmatrix} i_{\mathrm{cir1}} \\ i_{\mathrm{cir2}} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{2.33}$$

are zero (neglecting the components necessary for the branch-energy control) as well as the common-mode voltage

$$v_{\mathrm{cm}} = 0 \tag{2.34}$$

(if the third-harmonic injection is not applied).

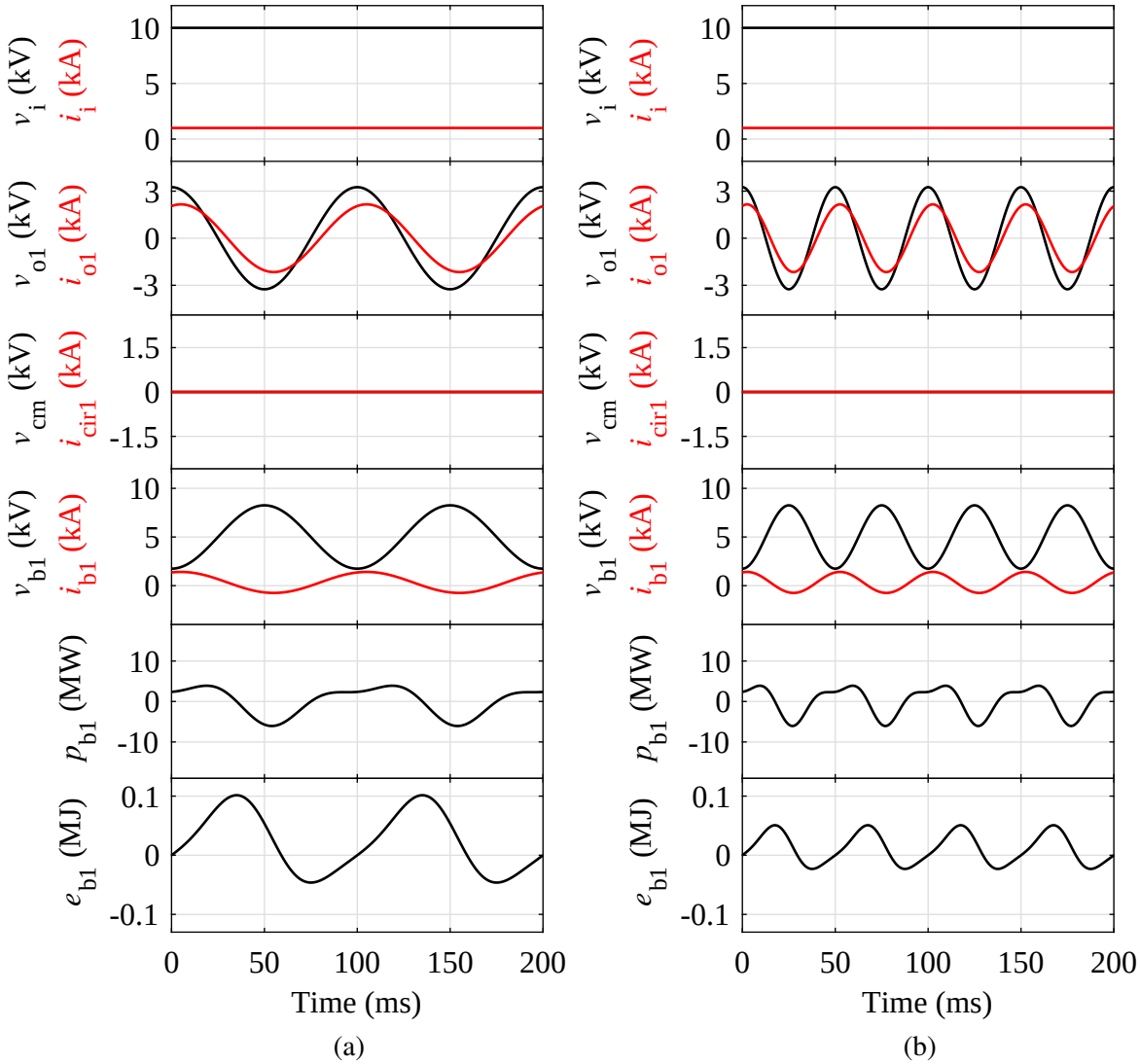


Figure 2.15: Example waveforms for an MMC operated in normal operation mode: (a) at f = **10 Hz**, (b) at f = **20 Hz**. The operation point parameters are summarized in Table 2.4. The common-mode voltage v_{cm} is not visible because its waveform is identical to that of circulating current i_{cir1}.

The corresponding waveforms for the normal operation mode are plotted in Figure 2.15. It can

be observed that both the branch voltage and the branch current comprise two components: one with the frequency of the output system and one direct component linked to the input system.

If the active power balance described by (2.30) is achieved, the branch powers of first two branches

$$\begin{bmatrix} p_{\mathrm{b1}}(t) \\ p_{\mathrm{b2}}(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 1 \\ -1 \end{bmatrix} \cdot \frac{\sqrt{2} \cdot I_{\mathrm{o}} \cdot V_{\mathrm{i}}}{4} \cdot \cos(\omega t - \varphi) + \begin{bmatrix} -1 \\ 1 \end{bmatrix} \cdot \frac{\sqrt{2} \cdot I_{\mathrm{i}} \cdot V_{\mathrm{o}}}{3} \cdot \cos(\omega t)}_{\text{differential}} \ldots \\ \underbrace{- \begin{bmatrix} 1 \\ 1 \end{bmatrix} \cdot \frac{I_{\mathrm{o}} \cdot V_{\mathrm{o}}}{2} \cdot \cos(2\omega t - \varphi)}_{\text{common}} \quad (2.35)$$

can be described as a function of time. The equation can be split into two parts: the differential part and the common part. The common part consists of only one component at double output frequency with an amplitude linked to the output apparent power. The differential part consists of two components at the single output frequency. The amplitude of the resulting power component depends on the phase angle and the voltage ratio between the input voltage and the output voltage. The differential part of the branch powers can even reach zero, when only active power is generated ($\varphi = 0$) and the input voltage value equals the double output voltage RMS value $V_{\mathrm{i}} = 2V_{\mathrm{o}}$. This represents an operating point with the modulation index $M = \sqrt{2} \approx 1.41$, which is not achievable with half-bridge modules. The farther away the distance of the chosen operating point is from this operating point, the higher the differential part of the branch powers becomes.

The branch energies

$$\begin{bmatrix} e_{\mathrm{b1}}(t) \\ e_{\mathrm{b2}}(t) \end{bmatrix} = \begin{bmatrix} 1 \\ -1 \end{bmatrix} \cdot \frac{\sqrt{2} \cdot I_{\mathrm{o}} \cdot V_{\mathrm{i}}}{4 \cdot \omega} \cdot \sin(\omega t - \varphi) + \begin{bmatrix} -1 \\ 1 \end{bmatrix} \cdot \frac{\sqrt{2} \cdot I_{\mathrm{i}} \cdot V_{\mathrm{o}}}{3 \cdot \omega} \cdot \sin(\omega t) \ldots \\ - \begin{bmatrix} 1 \\ 1 \end{bmatrix} \cdot \frac{I_{\mathrm{o}} \cdot V_{\mathrm{o}}}{2 \cdot 2\omega} \cdot \sin(2\omega t - \varphi) + \begin{bmatrix} E_{\mathrm{b1},0} \\ E_{\mathrm{b2},0} \end{bmatrix} \quad , \quad (2.36)$$

which must be buffered in the modules' capacitors, can be calculated by integrating (2.35). Through examining these equations, the largest drawback of modular multilevel converters becomes clear: The energy which must be buffered in the module capacitors is inversely proportional to the output frequency. This leads to a large amount of energy compared to e.g. two-level VSI, since the dc-link capacitor of the two-level VSI must buffer power components at frequencies near the multiples of the switching frequency only. Moreover, this means that if the output frequency is reduced to half, the energy variation doubles (as also demonstrated in Figure 2.15), making the converter topology rather impractical for variable-speed drives. Finally, the module capacitors form a large part of the converter's weight, volume, and cost. Consequently, it is generally desirable to find an operation mode reducing these.

2.5.2 Instantaneous Power Mode

A method which compensates for the differential component in branch powers to reduce the branch energy variation (and thus module capacitance) is Instantaneous Power Mode (IPM). This method, first presented by Winkelnkemper *et al.* in [97] and studied later by Pou *et*

al. in [98], shapes the leg currents in a way that the leg powers (the sum of power in upper and lower branches in one converter leg) are instantaneously zero. This is achieved when the power transmitted from the dc-link into a converter's phase leg (input voltage multiplied by the respective leg current)

$$\begin{bmatrix} i_{\mathrm{leg1}} \\ i_{\mathrm{leg2}} \\ i_{\mathrm{leg3}} \end{bmatrix} \cdot v_{\mathrm{i}} = \begin{bmatrix} i_{\mathrm{o1}} \cdot v_{\mathrm{o1}} \\ i_{\mathrm{o2}} \cdot v_{\mathrm{o2}} \\ i_{\mathrm{o3}} \cdot v_{\mathrm{o3}} \end{bmatrix} \tag{2.37}$$

equals the instantaneous power transmitted from the phase leg to the output load.

Using the definitions for leg currents (2.2) and circulating currents (2.4), (2.37) can be transformed to express the required circulating currents

$$\begin{bmatrix} i_{\mathrm{cir1}} \\ i_{\mathrm{cir2}} \end{bmatrix} = \frac{1}{2 \cdot v_{\mathrm{i}}} \begin{bmatrix} i_{\mathrm{o1}} \cdot v_{\mathrm{o1}} - i_{\mathrm{o2}} \cdot v_{\mathrm{o2}} \\ i_{\mathrm{o2}} \cdot v_{\mathrm{o2}} - i_{\mathrm{o3}} \cdot v_{\mathrm{o3}} \end{bmatrix} \tag{2.38}$$

as a function of instantaneous values for input voltage v_{i}, output voltage $v_{\mathrm{o1..3}}$ and output currents $i_{\mathrm{o1..3}}$.

In Figure 2.16, the waveforms of an MMC operated in normal operation mode and in IPM are compared. As can be seen, the circulating current with IPM includes a second harmonic component, compensating for the common branch power component in combination with the input voltage V_{i}. This influences the shape of branch current, leading to higher currents when the branch voltages are low and to lower branch currents when the branch voltages are high, which reduces the branch powers and consequently the branch energies. However, the peak values and the RMS values of branch currents are increased, which has a negative effect on the converter losses.

The branch powers in IPM

$$\begin{aligned} \begin{bmatrix} p_{\mathrm{b1}} \\ p_{\mathrm{b2}} \end{bmatrix} &= \begin{bmatrix} 1 \\ -1 \end{bmatrix} \cdot \frac{\sqrt{2} \cdot I_{\mathrm{o}} \cdot V_{\mathrm{i}}}{4} \cdot \cos(\omega t - \varphi) \dots \\ &+ \begin{bmatrix} -1 \\ 1 \end{bmatrix} \cdot \frac{\sqrt{2} \cdot V_{\mathrm{o}}^2 \cdot I_{\mathrm{o}}}{V_{\mathrm{i}}} \cdot \left(\cos(\omega t - \varphi) + \frac{1}{2} \cdot \cos(\omega t + \varphi) + \frac{1}{2} \cos(3\omega t - \varphi) \right) \end{aligned} \tag{2.39}$$

comprise only differential components, as the common component is canceled out. The components are at the single output frequency and at triple output frequency. Like with normal operation mode, the component at the single output frequency can reach zero, when only active power is being transmitted ($\varphi = 0$). However, this occurs with lower output voltage, when $V_{\mathrm{i}} = \sqrt{6} \cdot V_{\mathrm{o}}$, which corresponds to modulation index $M = \frac{2}{\sqrt{3}} \approx 1.15$.

Observing the equations for branch power, two facts can be stated: First, while the branch power of IPM is reduced compared to normal operation mode, it is still linked to the output frequency. Hence, the branch energy is still inversely proportional to the output frequency. Consequently, the required module capacitance rises towards infinity when the output frequency approaches zero. Second, the difference between the normal operation mode and IPM becomes smaller when the output voltage decreases. When the output voltage is zero, the equations for branch powers (2.35) and (2.39) become identical.

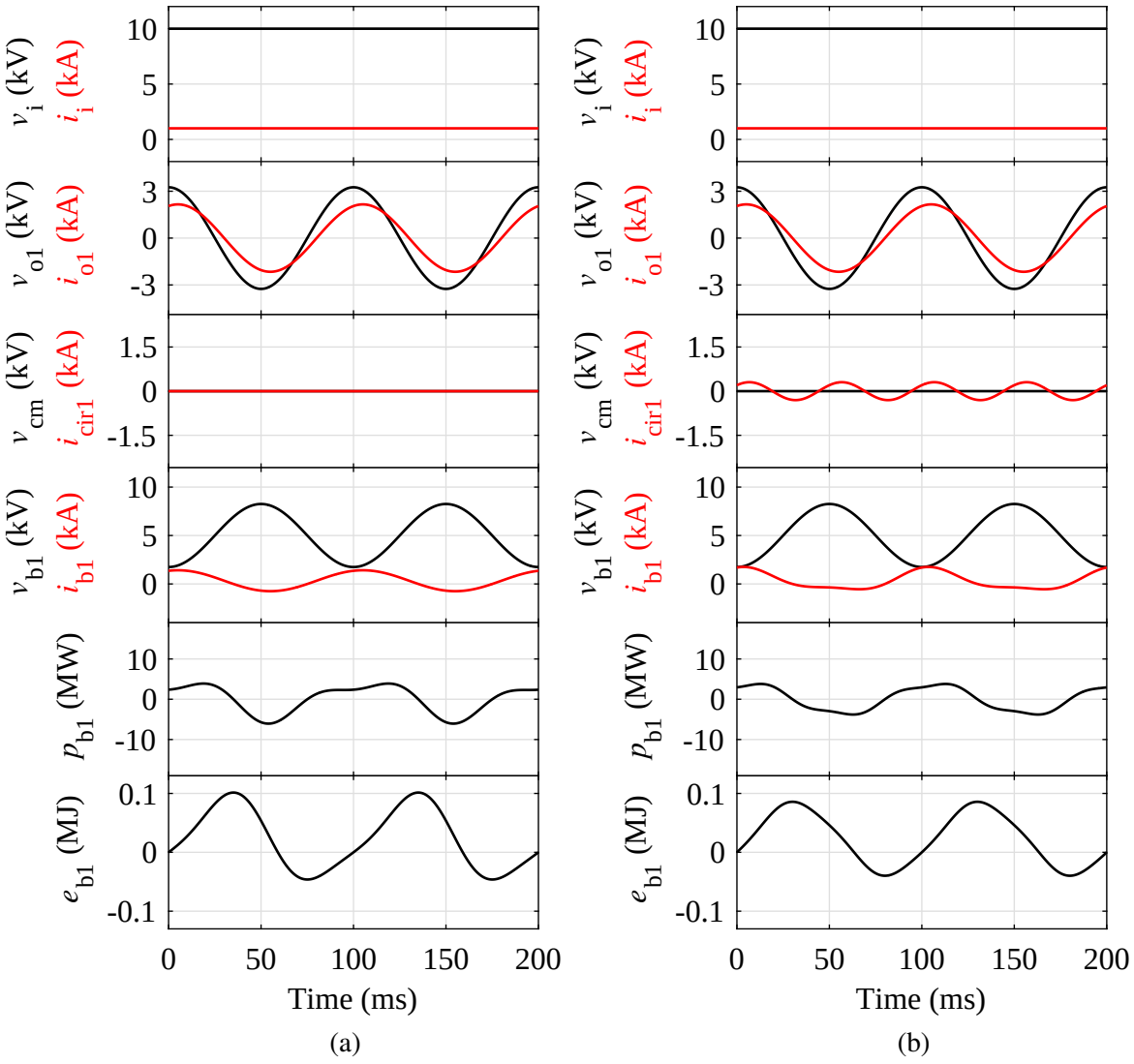


Figure 2.16: Comparison of example waveforms for an MMC operated in normal operation mode (a), and in instantaneous power mode (b). The operation point parameters are summarized in Table 2.4.

A similar second-harmonic injection in circulating currents to decrease the branch energy variation was derived using a numeric optimization by Picas *et al.* in [99]. Furthermore, Engel *et al.* [100] propose to apply a multi-goal numeric optimization not only to the second harmonic, but also to the fourth harmonic, in order to optimize both the branch energy variation and the rms values of branch currents (and thus also the converter losses).

2.5.3 Low-Frequency Mode

The low-frequency mode (LFM) was proposed by Korn *et al.* in [101] to enable stable operation at low machine speeds. It uses a high-frequency component in common-mode voltage

$$v_{cm} = v_{cm,HF}(t) \quad , \tag{2.40}$$

which enables compensation of the differential branch-power components linked to the output frequency without disturbing the output currents. The waveform of this high-frequency voltage $v_{\mathrm{cm,HF}}(t)$ can either be a sine wave or a square wave. Hagiwara *et al.* show in [102] that the square waveform is more advantageous. In the following investigations, a square waveform with frequency f_{HF} and RMS value $V_{\mathrm{cm,HF}}$ are assumed as the high-frequency common-mode voltage component.

The derivation of this mode is based on converter-leg basis. Therefore, the branch currents of the first converter leg

$$\begin{bmatrix} i_{\mathrm{b1}} \\ i_{\mathrm{b2}} \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \end{bmatrix} \cdot i_{\mathrm{leg1}} + \begin{bmatrix} \frac{1}{2} \\ -\frac{1}{2} \end{bmatrix} \cdot i_{\mathrm{o1}} \tag{2.41}$$

are redefined, using the leg currents instead of the circulating currents for the derivation. The leg currents

$$\begin{bmatrix} i_{\mathrm{leg1}} \\ i_{\mathrm{leg2}} \\ i_{\mathrm{leg3}} \end{bmatrix} = \frac{1}{v_{\mathrm{i}}} \cdot \begin{bmatrix} i_{\mathrm{o1}} \cdot v_{\mathrm{o1}} \\ i_{\mathrm{o2}} \cdot v_{\mathrm{o2}} \\ i_{\mathrm{o3}} \cdot v_{\mathrm{o3}} \end{bmatrix} + \begin{bmatrix} i_{\mathrm{leg1,HF}} \\ i_{\mathrm{leg2,HF}} \\ i_{\mathrm{leg3,HF}} \end{bmatrix} \tag{2.42}$$

are assumed to consist of two parts: the first part represents the compensation of the common branch-power component, as derived in (2.37) for IPM, and the second high-frequency component represents a new degree of freedom.

Using these equations, the branch powers of the first converter leg

$$\begin{aligned} \begin{bmatrix} p_{\mathrm{b1}} \\ p_{\mathrm{b2}} \end{bmatrix} = & \underbrace{\begin{bmatrix} 1 \\ -1 \end{bmatrix} \cdot \left(\frac{i_{\mathrm{o1}} \cdot v_{\mathrm{i}}}{4} - \frac{v_{\mathrm{o1}}^2 \cdot i_{\mathrm{o1}}}{v_{\mathrm{i}}} \right)}_{\text{low frequency}} - \underbrace{\begin{bmatrix} 1 \\ -1 \end{bmatrix} \cdot i_{\mathrm{leg1,HF}} \cdot v_{\mathrm{cm,HF}}}_{\text{degree of freedom}} \cdots \\ & \underbrace{- \begin{bmatrix} 1 \\ -1 \end{bmatrix} \cdot \left(i_{\mathrm{leg1,HF}} \cdot v_{\mathrm{o1}} + \frac{i_{\mathrm{o1}} \cdot v_{\mathrm{o1}} \cdot v_{\mathrm{cm,HF}}}{v_{\mathrm{i}}} \right) + \begin{bmatrix} 1 \\ 1 \end{bmatrix} \cdot \left(\frac{i_{\mathrm{leg1,HF}} \cdot v_{\mathrm{i}}}{2} - \frac{i_{\mathrm{o1}} \cdot v_{\mathrm{cm,HF}}}{2} \right)}_{\text{high frequency}} \end{aligned} \tag{2.43}$$

can be expressed. The equations can be split into three parts. The first part includes the low-frequency power components linked to the output frequency. The second part consists of the high-frequency common-mode voltage component multiplied by the high-frequency leg-current component, which are both degrees of freedom. If the high-frequency leg currents are chosen as:

$$\begin{bmatrix} i_{\mathrm{leg1,HF}} \\ i_{\mathrm{leg2,HF}} \\ i_{\mathrm{leg3,HF}} \end{bmatrix} = \frac{v_{\mathrm{i}}}{4 \cdot v_{\mathrm{cm,HF}}} \cdot \begin{bmatrix} i_{\mathrm{o1}} \\ i_{\mathrm{o2}} \\ i_{\mathrm{o3}} \end{bmatrix} - \frac{1}{v_{\mathrm{i}} \cdot v_{\mathrm{cm,HF}}} \cdot \begin{bmatrix} v_{\mathrm{o1}}^2 \cdot i_{\mathrm{o1}} \\ v_{\mathrm{o2}}^2 \cdot i_{\mathrm{o2}} \\ v_{\mathrm{o3}}^2 \cdot i_{\mathrm{o3}} \end{bmatrix} \quad , \tag{2.44}$$

the second part of the equation can generate low-frequency power components, which compensate for the first low-frequency part of the equations. The third part consists of the low-frequency currents or voltages multiplied by high-frequency voltages or currents. The resulting power components of the third part are all of high frequency and therefore are expected to have only a small impact on the branch energies. Note that the common-mode voltage component $v_{\mathrm{cm,HF}}$ is assumed to have only values $\pm V_{\mathrm{cm,HF}}$ and thus the division by its instantaneous value is allowed.

If the sinusoidal common-mode voltage component is used, a different leg current calculation according to [101] should be applied.

The leg currents required by LFM can be calculated by substituting (2.44) into (2.42). These currents can then be transformed into the required input current and the required circulating currents:

$$\begin{bmatrix} i_{\mathrm{i}} \\ i_{\mathrm{cir1}} \\ i_{\mathrm{cir2}} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ \frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{1}{2} & -\frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{leg1}} \\ i_{\mathrm{leg2}} \\ i_{\mathrm{leg3}} \end{bmatrix} \quad . \tag{2.45}$$

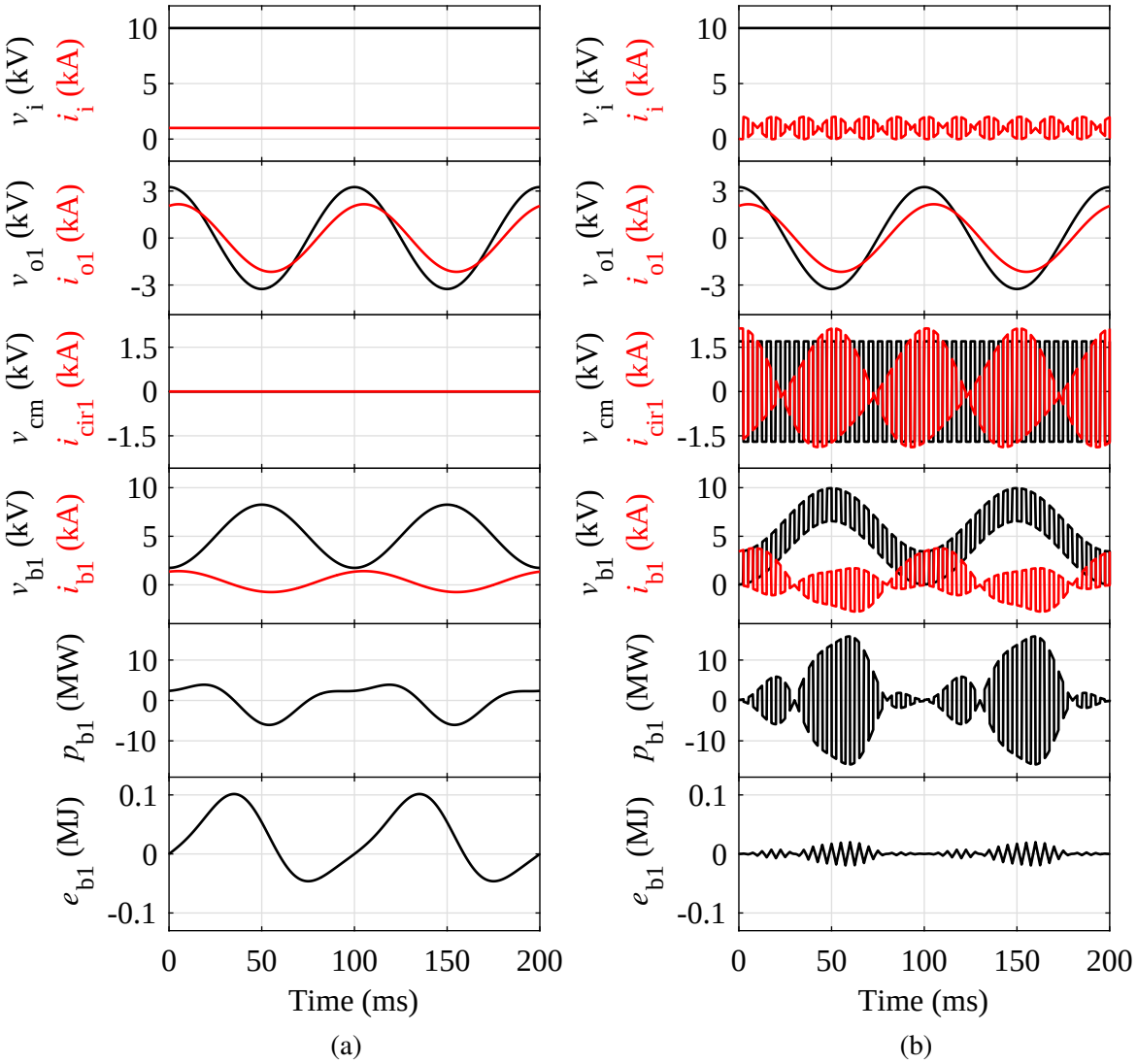


Figure 2.17: Comparison of example waveforms for an MMC operated in normal operation mode (a) and in LFM (b). The operation point parameters are summarized in Table 2.4.

In Figure 2.17, the waveforms of LFM-operated MMC are compared to those of normal operation mode. The frequency of the square-function common-mode voltage is $f_{\mathrm{HF}} = 200$ Hz and the RMS value is $V_{\mathrm{cm,HF}} = 1.7$ kV. While the branch energy variation is minimized by the LFM due to the high frequency of the branch power, the branch voltage and the branch current are significantly increased. Moreover, the converter switching losses are expected to increase

as well, since the branch voltage changes with a higher frequency over a higher number of voltage levels, increasing the number of module switching instants. These are the reasons why the LFM should only be used at low machine speeds and with reduced machine torques [101]. If full-torque is desired over the whole operating range, a converter oversizing results, due to the low-frequency operating range [103]. Additionally, the fact that the LFM should only be used below the rated machine speed means that the MMC module capacitance is still considerably high when the rated electrical frequency is very low.

As can also be seen in Figure 2.17b, the LFM causes a distortion of the input current. This is often undesired as the input voltage sources might not tolerate it. A possible countermeasure is to force the input current not to have any harmonics besides its dc part. Such operation is described in this thesis as “extended LFM” and its waveforms are compared to the normal LFM in Figure 2.18. The comparison shows that the branch energy variation of the extended LFM is slightly increased, which might be still acceptable, as this significantly decreases the input current harmonics.

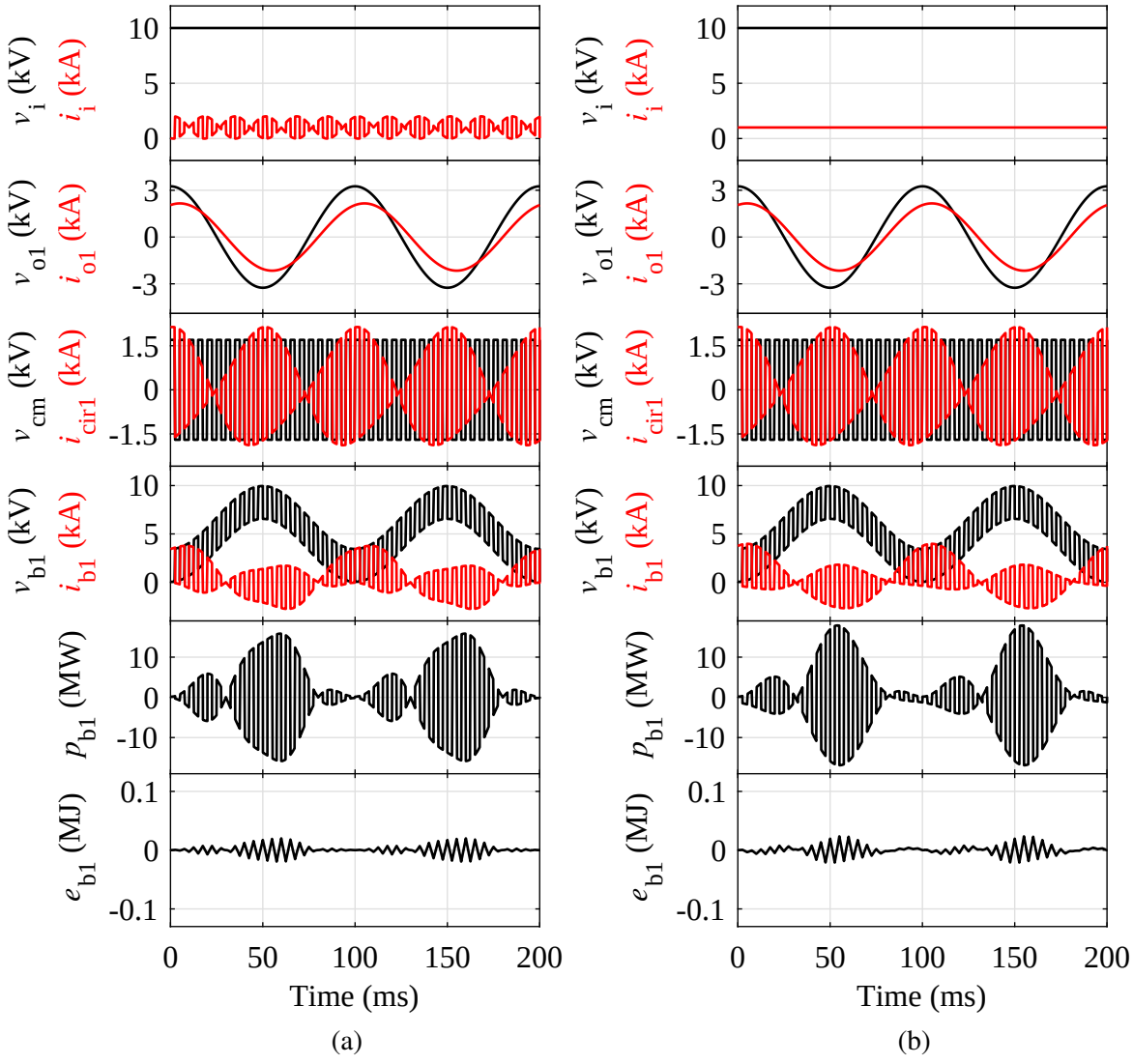


Figure 2.18: Comparison of example waveforms for an MMC operated in a normal LFM (a) and an extended LFM (b). The operation point parameters are summarized in Table 2.4.

2.5.4 Third-Harmonic Injection

To enable higher output voltages without increasing the required branch voltages, the third-harmonic injection can be applied as an additional component of common-mode voltage

$$v_{\mathrm{cm,3rdH}}(t) = \frac{1}{6} \cdot \sqrt{2} \cdot V_{\mathrm{o}} \cdot \cos\left(3 \cdot \omega \cdot t\right) \quad . \tag{2.46}$$

This technique is well-known for all different kinds of VSIs and increases the maximum modulation index by approximately 15 %.

With the normal operation mode or IPM, this component is simply added to the common-mode voltage setpoint value:

$$v_{\mathrm{cm}} = v_{\mathrm{cm,3rdH}}(t) \quad . \tag{2.47}$$

However, if the common part of the branch powers should be canceled out in IPM, the common-mode voltage must be included in the equation for circulating currents, extending (2.38) to

$$\begin{bmatrix} i_{\mathrm{cir1}} \\ i_{\mathrm{cir1}} \end{bmatrix} = \frac{1}{2 \cdot v_{\mathrm{i}}} \begin{bmatrix} i_{\mathrm{o1}} \cdot \left(v_{\mathrm{o1}} + v_{\mathrm{cm,3rdH}}\right) - i_{\mathrm{o2}} \cdot \left(v_{\mathrm{o2}} + v_{\mathrm{cm,3rdH}}\right) \\ i_{\mathrm{o2}} \cdot \left(v_{\mathrm{o2}} + v_{\mathrm{cm,3rdH}}\right) - i_{\mathrm{o3}} \cdot \left(v_{\mathrm{o3}} + v_{\mathrm{cm,3rdH}}\right) \end{bmatrix} \quad . \tag{2.48}$$

With LFM, the third-harmonic common-mode voltage component can also be added, leading to the following expression for common-mode voltage:

$$v_{\mathrm{cm}} = v_{\mathrm{cm,HF}}(t) + v_{\mathrm{cm,3rdH}}(t) \quad . \tag{2.49}$$

Similarly to IPM, the low-frequency third-harmonic common-mode voltage component has to be included in the equations for branch power compensation using the leg currents (2.42) and (2.44). After substituting (2.44) into (2.42), the following expression for the leg currents can be derived:

$$\begin{aligned} \begin{bmatrix} i_{\mathrm{leg1}} \\ i_{\mathrm{leg2}} \\ i_{\mathrm{leg3}} \end{bmatrix} = \frac{1}{v_{\mathrm{i}}} \cdot \begin{bmatrix} i_{\mathrm{o1}} \cdot \left(v_{\mathrm{o1}} + v_{\mathrm{cm,3rdH}}\right) \\ i_{\mathrm{o2}} \cdot \left(v_{\mathrm{o2}} + v_{\mathrm{cm,3rdH}}\right) \\ i_{\mathrm{o3}} \cdot \left(v_{\mathrm{o3}} + v_{\mathrm{cm,3rdH}}\right) \end{bmatrix} + \frac{v_{\mathrm{i}}}{4 \cdot v_{\mathrm{cm,HF}}} \cdot \begin{bmatrix} i_{\mathrm{o1}} \\ i_{\mathrm{o2}} \\ i_{\mathrm{o3}} \end{bmatrix} \dots \\ - \frac{1}{v_{\mathrm{i}} \cdot v_{\mathrm{cm,HF}}} \cdot \begin{bmatrix} \left(v_{\mathrm{o1}} + v_{\mathrm{cm,3rdH}}\right)^2 \cdot i_{\mathrm{o1}} \\ \left(v_{\mathrm{o2}} + v_{\mathrm{cm,3rdH}}\right)^2 \cdot i_{\mathrm{o2}} \\ \left(v_{\mathrm{o3}} + v_{\mathrm{cm,3rdH}}\right)^2 \cdot i_{\mathrm{o3}} \end{bmatrix} \quad . \end{aligned} \tag{2.50}$$

2.6 Application of MMCs in Drives

In general, the approaches enabling the operation of MMC for variable-speed machine drives can be separated into two groups. The first group consists of different operating modes without changes to the MMC topology. In order to enable the low-frequency operation, these operating modes inject some high-frequency components into both branch voltages and branch currents. These are chosen in a way that compensates for the low-frequency components in branch powers.

In the second group, the MMC topology is modified, adding new converter paths or converter stages.

The vast majority of the publications in the first group use normal operation mode during higher machine speeds and an operation mode based on high-frequency common-mode voltage during the low speeds. The **low-frequency mode** (or its extended version) is the most common choice, e.g. [83, 84, 94, 102, 104–106]. Although the approaches from [103] and [107] calculate the setpoints for the circulating currents differently, they lead to almost identical results. References [83, 84, 103, 104] propose not to turn off the low-frequency mode immediately but to reduce the compensating currents linearly with the frequency instead. While the application in drives with quadratic torque characteristics does not theoretically require the low-frequency mode [108] (although it is advantageous to use LFM to stabilize the operation at very low speeds), if high torques are necessary at low speeds, the low-frequency mode has to be used. Moreover, Antonopoulos *et al.* demonstrate in [103] that if full torque is desired over the whole operating range, a converter oversizing is required due to low speeds. A possible countermeasure, proposed by Antonopoulos *et al.* in [109], is to decrease the module capacitor voltage setpoint during the low speeds. This is possible because only lower output voltages are necessary at low speeds and thus the required branch voltages are lower. Consequently, a higher energy variation is allowed in the modules without a risk of module capacitors reaching dangerous levels of voltages. An implementation of this approach in the drives with LFM can be found e.g. in [104].

A similar idea to the low-frequency mode is **asymmetric mode control** presented by Yang *et al.* in [110]. The method also utilizes the square waveform of the common-mode voltage. However, in contrast to the low-frequency mode, the circulating currents are not chosen to compensate for the low-frequency branch-power components, but to only reduce these. This is done by selecting the leg currents in a way that the branch in a phase leg with the currently higher voltage does not conduct any current and all current is conducted by the branch with lower branch voltage.[8)] The main drawback of this method is that it cannot operate at near zero speed when the output voltage is unequal to zero [110]. Furthermore, no results were presented for operating points below one Hertz.

Another approach by Wang *et al.* [111, 112], called **switching-cycle capacitor voltage control** and also belonging to the first group of approaches, is to use the high-frequency voltage components of the voltage ripple caused by the converter modulation to compensate for the low-frequency power components. Since only the natural voltage ripple is used, no common-mode voltage has to be applied. Nonetheless, this approach has two issues. First of all, since the current has to be controlled with a bandwidth higher than the modulation frequency, a very complex predictive control based on the resonant circuits within the converter has to be applied. The even more important issue is, however, that since the amplitude of the modulation voltage ripple generated by the MMC is quite low, the circulating currents used to generate the compensating power have to be quite high. While this is not significantly visible for the MMC with two modules per branch presented in [111, 112], it can be seen that the peak current of the dc-dc converter presented in [113] is roughly four times higher than the output current. This leads to high chip area of installed semiconductors and high converter losses for higher numbers of modules per branch than two.

[8)] Please note that this principle is similar to the quasi-two-level PWM operation derived later in this thesis. Nevertheless, the main difference is that the lower-voltage branch has zero voltage with quasi-two-level PWM operation. Hence, the quasi-two-level PWM operation is capable of even lower branch energy variation.

The **quasi-two-level PWM operation** also belongs to the first group, since it does not modify the converter topology (besides the requirement of a central dc-link capacitor). The operation principle is explained in the next chapter.

The second group of approaches can be further divided into two subgroups: an enhancement of the topology with additional converter stages, and a redesign of topology, introducing new power paths within the converter.

The first idea in the first subgroup can be derived by observing (2.36). Besides the constants $E_{\mathrm{b1,0}}$ and $E_{\mathrm{b2,0}}$, which determine the initial values of branch energies, the equation consists of three components. Since the ratio between the output voltage and output frequency V_{o}/ω is approximately constant with most types of electric machines, the second and third components are approximately constant as well and thus only the the first component is inversely proportional to the output frequency ω. However, this component can be forced to be constant when **the converter's input voltage is adjusted** in a manner that leads to a constant ratio V_{i}/ω. To achieve this, an additional converter stage is necessary. This additional stage can be, for instance, an active front-end based on an H-bridge MMC [114, 115][9)]. A more advanced idea, presented by Li *et al.* in [116], is to use a single unidirectional switch consisting of soft-switching HV-IGBTs or thyristors operating as a chopper to modulate the input voltage for the converter, so that only a mean value of the input voltage is adjusted. Nevertheless, all mentioned methods are ineffective for speeds near zero, where the V_{o}/ω ratio cannot be held constant (the constant ratio would mean that no output voltage can be generated at zero speed). To overcome this problem, Kumar *et al.* [117] propose applying a special operation mode at low frequencies, injecting high-frequency components into the input current. The necessity to install an additional converter stage and to apply H-bridge modules remain disadvantages.

The second idea in the first subgroup is to apply a **high-frequency voltage to the converter input** [31, 33] instead of the dc link. As a consequence, the branch energy variation is significantly decreased independently of the output frequency. Nevertheless, there are two main disadvantages to this approach: First, the converter has to be built using H-bridge modules, since the ac-ac version of MMC is applied. Second, an additional converter stage is necessary to generate the high-frequency voltage. This can be, for instance, another H-bridge MMC as a front-end [33] or even a thyristor-based VSI [31]. Both of these disadvantages lead to additional costs and losses. The application of these approaches might be advantageous when a galvanic isolation is necessary or significantly different voltage levels are present at the converter's input and output, since the high-frequency voltage can be transferred through a relatively small medium-frequency transformer.

One idea in the second subgroup, proposed by Du *et al.* and which modifies the MMC topology, is to **split each of the MMC's branches into two**, providing one new connection point at the upper branch and one new connection point at the lower branch. Between these connection points, either an additional MMC branch [118] or a flying capacitor [119] can be connected. These provide new current paths to transfer energy from the lower "branch" to the upper "branch", and new options to generate high-frequency voltages. Consequently, the low-frequency operation mode can be applied without generating any common-mode voltage. On the other hand, both of these approaches have several disadvantages. These disadvantages include a higher volume of installed semiconductor switches and a higher module capacitance than in

[9)] The input voltage is varied indirectly in [114] by controlling the front-end MMC as a constant current source.

other operation modes[10]. Moreover, the high number of branches makes the redundancy more complex and costly.

The second idea of the second subgroup, proposed by Diab *et al.* in [121, 122], is to exchange the energy between the MMC branches by installing **a dual-active-bridge converter at each module**. Consequently, the module capacitance can be decreased significantly and the branch currents are also lower. Similarly to the previous topology modification, the common-mode voltage is no longer necessary and can be set to zero. The largest drawback is the additional dual-active-bridges, which increase the volume of installed semiconductor switches, the volume of inductive components (since each dual-active-bridge is connected to a medium-voltage transformer), and possibly the losses. A comprehensive study regarding the comparison to other solutions is not available yet.

[10] The storage constant H of the converter, as introduced in [120], used for simulations in [118] is 104.5 ms and in [119] is 76.5 ms, while it is typically about 50 ms with low-frequency mode (e.g., 52 ms in the experimental setup of [104]). With quasi-two-level PWM operation, energy storage constants as low as a few milliseconds are possible, as is presented in the following chapters. Note that the storage constant value given in [118] is not calculated for the whole converter as usual, but only for a single module.

3 Derivation of Quasi-Two-Level PWM Operation Using a Phase-Leg Model

The idea of quasi-two-level operation for multilevel converters is not particularly new. Before being proposed for MMCs, quasi-two-level operation was applied to diode-clamped multilevel converters [123, 124]. In these papers, the multilevel converter was modulated with a two-level PWM. The two-level rectangular output-voltage waveform was enriched with intermediate voltage levels (possible with multilevel converters), leading to a staircase trapezoidal waveform as depicted in Figure 3.1, and thus efficiently limiting the output $\mathrm{d}v/\mathrm{d}t$. Since the intermediate voltage levels are only active for a very short time, the operation mode rapidly decreases the requirements for installed capacitors and the complexity of their balancing. This operation mode with diode-clamped multilevel converters has three main drawbacks: a worse output-voltage harmonic spectrum (due to the sacrifice of the multilevel waveform), increased switching losses because all transistors are switched once each PWM period, and the duty cycle being limited to a certain value below one (0.937 in [123, 124]) due to the time in each period necessary for balancing the converter's capacitors.

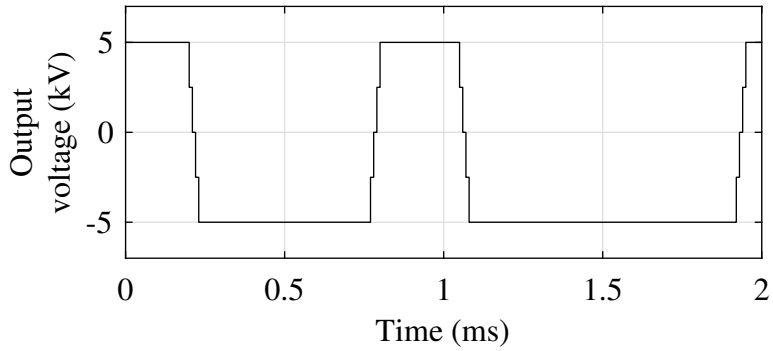


Figure 3.1: Quasi-two-level waveform. Example for PWM period of 1 ms and five voltage levels.

The quasi-two-level operation with MMCs was first proposed in [125] by Gowaid *et al.* for isolated dc-dc transmission in high-voltage applications based on two MMCs coupled through a medium-frequency transformer. Similar to diode-clamped multilevel converters, staircase quasi-two-level voltage waveforms are used. This voltage shape limits the $\mathrm{d}v/\mathrm{d}t$ at the transformer's terminals and thus reduces the requirements for its insulation system. The simple square-wave output with constant duty cycle applied in [125] was later extended by variation of the pulse width by Sun *et al.* in [126], improving the performance over a wider voltage range. In these applications, the converter energy balancing is straight-forward, since the branch-energy distortion occurring in the first half of the output voltage period has the same absolute value in the opposite direction as the energy distortion in the second half of the period.

In [127, 128], Aiello *et al.* propose varying the phase shift between the individual carriers of the phase-shifted multi-carrier modulation used in an open-loop controlled MMC. The optimum

phase shift (as shown in Figure 2.4) is applied when the converter operates at high output frequencies, which leads to an operation typical for an open-loop controlled MMC. When low output frequencies are required, the phase-shift angle is decreased to almost zero, which leads to a quasi-two-level output voltage waveform. While the branch inductance of open-loop controlled MMCs is typically set relatively high to reduce the circulating currents, in the approach by Aiello *et al.* it is significantly decreased to set the natural resonance frequency of the MMC higher than the modulation (and control) frequency. The natural resonance frequency of an MMC

$$f_0 = \frac{1}{2 \cdot \pi \cdot \sqrt{2 \cdot L_\mathrm{b} \cdot \frac{C_\mathrm{mod}}{n_\mathrm{mpb}}}} \tag{3.1}$$

is determined by the series connection of two branch inductors and n_mpb series-connected module capacitors with capacitance C_mod [127]. The low value of branch inductances leads to time constants for the leg currents which are significantly shorter than the modulation period. Consequently, the proposed MMC behaves as a conventional open-loop controlled MMC switched between two quasi-stationary states: when the output voltage is $V_\mathrm{i}/2$ and when it is $-V_\mathrm{i}/2$. Similarly to conventional open-loop controlled MMCs, the converter operation is stable as long as the branch resistances provide sufficient damping to the converter. In addition to the conventional operation, the switch-over between the two quasi-stationary states leads to damped oscillations between the module capacitors and the branch inductors.

A similar approach was recently applied to a nine-branch MMC for six-phase medium-voltage motor drives by Diab *et al.* in [129]. In addition to the open-loop control proposed by Aiello *et al.*, this approach was also inspired by the the quasi-two-level PWM operation investigated in this thesis. Thus, the quasi-two-level waveform is generated by PWM and is applied over the whole operation range.

The main issue with Gowaid's, Aiello's, and Diab's approaches, which is not deeply analyzed in any of the papers, is the necessity for a high damping factor

$$\zeta = \frac{2 \cdot R_\mathrm{b}}{2} \cdot \sqrt{\frac{\frac{C_\mathrm{mod}}{n_\mathrm{mpb}}}{2 \cdot L_\mathrm{b}}} \tag{3.2}$$

to enable a stable converter operation and to limit the resonant branch current overshoot after the module switching (the peak branch current is almost three times higher than the peak output current in [129]). One way to increase the damping factor is to increase the branch resistance. However, the branch resistance represents converter losses and must remain as low as possible. The second option is to increase the module capacitance while decreasing the branch inductance, which keeps the desired resonance frequency unchanged [see (3.1)]. However, this means that the module capacitance cannot be chosen freely and must have a relatively high value, despite the low energy variation typical for quasi-two-level operation (this is also one of the observations made by Aiello *et al.* in [127]).

The novel quasi-two-level PWM operation investigated in this thesis generates the quasi-two-level voltage waveform by two-level PWM and is applicable for a wide range of output frequencies. Contrary to the aforementioned approaches, it actively damps the resonant circuit within the MMC by a closed-loop current controller, and thus can be applied even if the converter

losses were zero. Moreover, since the module capacitance is no longer required for designing the damping factor, significantly lower module capacitances are achievable. This chapter presents the derivation of the quasi-two-level PWM operation using a phase-leg model of an MMC, with the main goal of reducing the module capacitance as much as possible. In the following parts of this chapter, the phase-leg model is presented, simplified, and used for the derivation of the operation mode.

3.1 Phase-Leg Model

Since the quasi-two-level PWM operation mode for modular multilevel converters is applied on a phase-leg basis, the phase-leg model has to be studied first.

A detailed phase-leg model of an MMC is displayed in Figure 3.2a. To decouple the leg currents, a dc-link capacitor C_i is installed at the converter input [see Section 2.4.2]. Using the simplification presented in Section 2.3.1, the equivalent electrical circuit in Figure 3.2b can be derived. For the equivalent electrical circuit, the input capacitance is assumed to be very large ($C_\mathrm{i} \to \infty$), and thus the converter input can be substituted with a center-tapped constant direct voltage source V_i. The load is assumed to be inductive, with a relatively high inductance L_o. The converter losses are represented by the branch inductances R_b. The upper MMC branch is referred to as Branch A, and the lower branch as Branch B. The equivalent variable labels for the phase legs of the three-phase MMC model defined in the previous chapter are listed in Table 3.1.

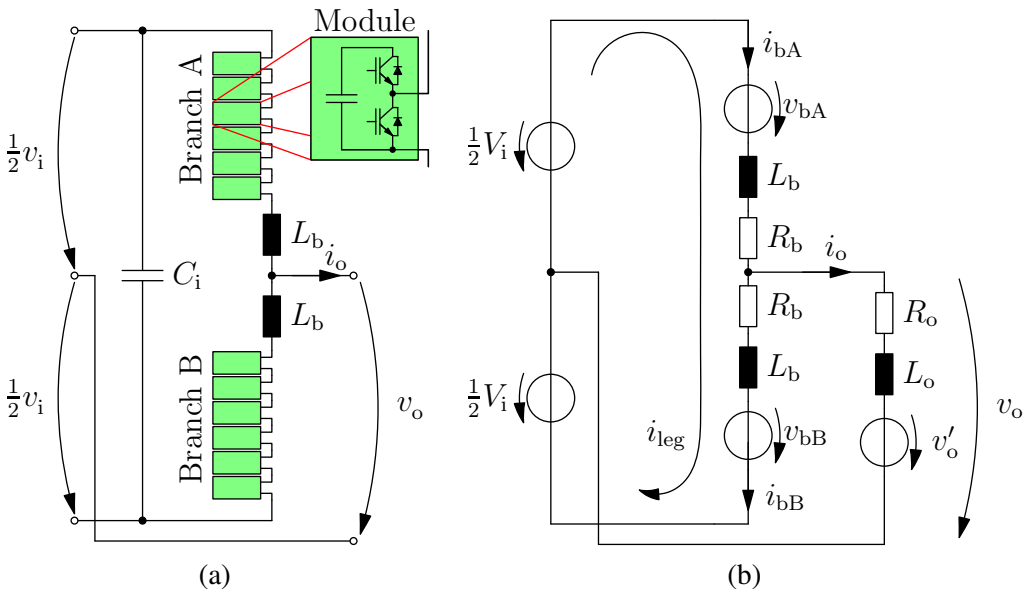


Figure 3.2: MMC phase-leg model: (a) detailed model with half-bridge modules, (b) equivalent electrical circuit.

As Figure 3.2b shows, two independent currents, interacting with the converter input and output, can be found within the topology: the output current i_o and the leg current i_leg. These can be

Table 3.1: Equivalent variable labels of the phase-leg model for the particular phase-legs of the three-phase MMC model defined in Chapter 2.

	Phase-Leg Model	Three-Phase Model		
		Phase 1	Phase 2	Phase 3
Output current	i_o	i_o1	i_o2	i_o3
Output voltage	v_o	v_o1	v_o2	v_o3
Leg current	i_leg	i_leg1	i_leg2	i_leg3
Upper branch current	i_bA	i_b1	i_b3	i_b5
Lower branch current	i_bB	i_b2	i_b4	i_b6
Upper branch voltage	v_bA	v_b1	v_b3	v_b5
Lower branch voltage	v_bB	v_b2	v_b4	v_b6

expressed as a linear combination of the converter branch currents i_bA and i_bB:

$$\begin{bmatrix} i_\mathrm{o} \\ i_\mathrm{leg} \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} i_\mathrm{bA} \\ i_\mathrm{bB} \end{bmatrix} \quad . \tag{3.3}$$

The output current and the leg current can be further used for the derivation of the state-space representation:

$$\frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_\mathrm{o} \\ i_\mathrm{leg} \end{bmatrix} = \underbrace{\begin{bmatrix} -\frac{\frac{1}{2}R_\mathrm{b}+R_\mathrm{o}}{L_\mathrm{o,eff}} & 0 \\ 0 & -\frac{2R_\mathrm{b}}{L_\mathrm{leg}} \end{bmatrix}}_{\mathbf{A}} \cdot \begin{bmatrix} i_\mathrm{o} \\ i_\mathrm{leg} \end{bmatrix} + \underbrace{\begin{bmatrix} -\frac{1}{2\cdot L_\mathrm{o,eff}} & \frac{1}{2\cdot L_\mathrm{o,eff}} \\ -\frac{1}{L_\mathrm{leg}} & -\frac{1}{L_\mathrm{leg}} \end{bmatrix}}_{\mathbf{B}} \cdot \begin{bmatrix} v_\mathrm{bA} \\ v_\mathrm{bB} \end{bmatrix} \cdots + \underbrace{\begin{bmatrix} -\frac{1}{L_\mathrm{o,eff}} & 0 \\ 0 & \frac{1}{L_\mathrm{leg}} \end{bmatrix}}_{\mathbf{E}} \cdot \begin{bmatrix} v'_\mathrm{o} \\ V_\mathrm{i} \end{bmatrix} \quad . \tag{3.4}$$

With **non-coupled branch inductors** (as depicted in Figure 3.2a), the effective leg inductance

$$L_\mathrm{leg} = 2 \cdot L_\mathrm{b} \tag{3.5}$$

is the sum of both branch inductances L_b, and the effective output inductance

$$L_\mathrm{o,eff} = L_\mathrm{o} + \frac{1}{2} \cdot L_\mathrm{b} \tag{3.6}$$

is effected by the output inductor L_o and the branch inductors L_b.

If the **center-tapped (coupled) inductors** are applied [see Section 2.4.1], the effective leg inductance L_leg is equal to the common-mode inductance of the coupled inductors. As the differential-mode inductance is ideally zero, the effective output inductance

$$L_\mathrm{o,eff} = L_\mathrm{o} \tag{3.7}$$

is effected by the output inductor only.

3.2 Derivation of Quasi-Two-Level PWM Operation Mode

The main goal for the derivation of the new operation mode was to minimize the branch energy variation. As was already presented in the section about MMC operation modes, the only way to reduce the branch energy variation is to compensate for the low-frequency branch-power components using additional high-frequency components in branch voltages and branch currents. In LFM, a high-frequency common-mode voltage component is used for this purpose, as this component does not influence any of the converter currents. In contrast to LFM, Ferreira in [130] proposes injecting high-frequency voltage components directly into the output voltages and then choosing a proper passive filter at the converter's output terminals to diminish the influence of these additional high-frequency voltage components on the output currents. This way, one is significantly less limited when choosing the form of additional components in branch voltages. Furthermore, the principle can also be applied to a single phase leg, which does not have any common-mode voltage from the topology.

Although Ferreira's principle was originally proposed for modular multilevel dc-dc converters, it can be applied to the MMC's phase leg as well. When the output inductance L_o is assumed to be high enough, additional high-frequency components can be injected into the output voltage v_o, while having only a minor influence on the output currents. Moreover, when the leg inductance L_leg is significantly lower than the effective output inductance $L_\mathrm{o,eff}$, the leg current can be changed more dynamically than the output current, allowing for the use of high-frequency components. These high-frequency components in the leg current with similar frequencies to those of the additional components in the output voltage are a possible degree of freedom to compensate for the low-frequency branch power components.

This fundamental idea can be further extended by searching for conditions under which both branch powers are zero:

$$\begin{bmatrix} p_\mathrm{bA} \\ p_\mathrm{bB} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad . \tag{3.8}$$

For this initial investigation, the branch voltages

$$\begin{bmatrix} v_\mathrm{bA} \\ v_\mathrm{bB} \end{bmatrix} = \begin{bmatrix} \frac{1}{2} & -1 \\ \frac{1}{2} & 1 \end{bmatrix} \cdot \begin{bmatrix} V_\mathrm{i} \\ v_\mathrm{o} \end{bmatrix} \tag{3.9}$$

are simplified by neglecting the voltage drops over the branch resistances and the branch inductances. By multiplication of the simplified branch voltages with the branch currents

$$\begin{bmatrix} i_\mathrm{bA} \\ i_\mathrm{bB} \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{2} \\ 1 & -\frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} i_\mathrm{leg} \\ i_\mathrm{o} \end{bmatrix} \quad , \tag{3.10}$$

the branch powers

$$\begin{bmatrix} p_\mathrm{bA} \\ p_\mathrm{bB} \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \end{bmatrix} \cdot \left(\frac{1}{2} \cdot V_\mathrm{i} \cdot i_\mathrm{leg} - \frac{1}{2} \cdot v_\mathrm{o} \cdot i_\mathrm{o} \right) + \begin{bmatrix} 1 \\ -1 \end{bmatrix} \cdot \left(\frac{1}{4} \cdot V_\mathrm{i} \cdot i_\mathrm{o} - v_\mathrm{o} \cdot i_\mathrm{leg} \right) \tag{3.11}$$

can be expressed. When observing a relatively short period of time, the output current i_o can be considered to have a constant value, due to its low dynamics caused by the high output inductance. As assumed in the previous section, the input voltage V_i is also a constant value, due

to the high input capacitance. The leg current and the output voltage can be changed dynamically and thus are the possible degrees of freedom to diminish the branch powers.

There are two different solutions

$$\begin{bmatrix} v_\mathrm{o} \\ i_\mathrm{leg} \end{bmatrix} = \pm\frac{1}{2} \cdot \begin{bmatrix} V_\mathrm{i} \\ i_\mathrm{o} \end{bmatrix} \quad , \tag{3.12}$$

in which both branch powers are zero. These solutions state that if the branch powers are desired to be instantaneously zero in each moment, a two-level voltage waveform with an amplitude $\frac{1}{2} \cdot V_\mathrm{i}$ is required at the converter output terminals. The leg current has to be set to either $\frac{1}{2} \cdot i_\mathrm{o}$ or $-\frac{1}{2} \cdot i_\mathrm{o}$ depending on the selected output voltage state. In addition to these two restrictions, it has to be assured that the two levels of the output voltage are altered so that the low-frequency components of the output voltage fit their setpoint values.

A simple way to satisfy both of these restrictions is to apply a two-level PWM to the output voltage. This solution is advantageous because it guarantees the two-level output waveform, while the low-frequency voltage components controlling the output current are set precisely. Moreover, the PWM-generated output-voltage spectrum comprises, next to the desired low-frequency components, only high-frequency voltage components near multiples of the switching frequency. These can be efficiently filtered by the output inductance.

The waveforms for two-level PWM-operated MMC are plotted in Figure 3.3. As the figure shows, the output voltage waveform is generated by comparing the triangle carrier function c to the duty cycle value

$$\delta = \frac{v_\mathrm{o}^*}{\frac{1}{2}V_\mathrm{i}} \quad , \tag{3.13}$$

calculated using the setpoint output voltage value v_o^*. The branch voltages

$$\begin{bmatrix} v_\mathrm{bA} \\ v_\mathrm{bB} \end{bmatrix} = \begin{cases} \begin{bmatrix} 0 \\ V_\mathrm{i} \end{bmatrix} & \text{when } \delta \geq c \\ \begin{bmatrix} V_\mathrm{i} \\ 0 \end{bmatrix} & \text{when } \delta < c \end{cases} \tag{3.14}$$

and the branch currents

$$\begin{bmatrix} i_\mathrm{bA} \\ i_\mathrm{bB} \end{bmatrix} = \begin{cases} \begin{bmatrix} i_\mathrm{o} \\ 0 \end{bmatrix} & \text{when } \delta \geq c \\ \begin{bmatrix} 0 \\ i_\mathrm{o} \end{bmatrix} & \text{when } \delta < c \end{cases} \tag{3.15}$$

can be calculated by substituting the solution (3.12) into their definitions in (3.9) and (3.10). The obtained equations (3.14) and (3.15) show (and Figure 3.3 confirms) that the branch voltage has either the value of input voltage V_i or is zero and that the branch current has either the value of output current i_o or is zero. Moreover, the current and voltage of a single branch are never high at the same time, forcing the corresponding branch power to be zero.

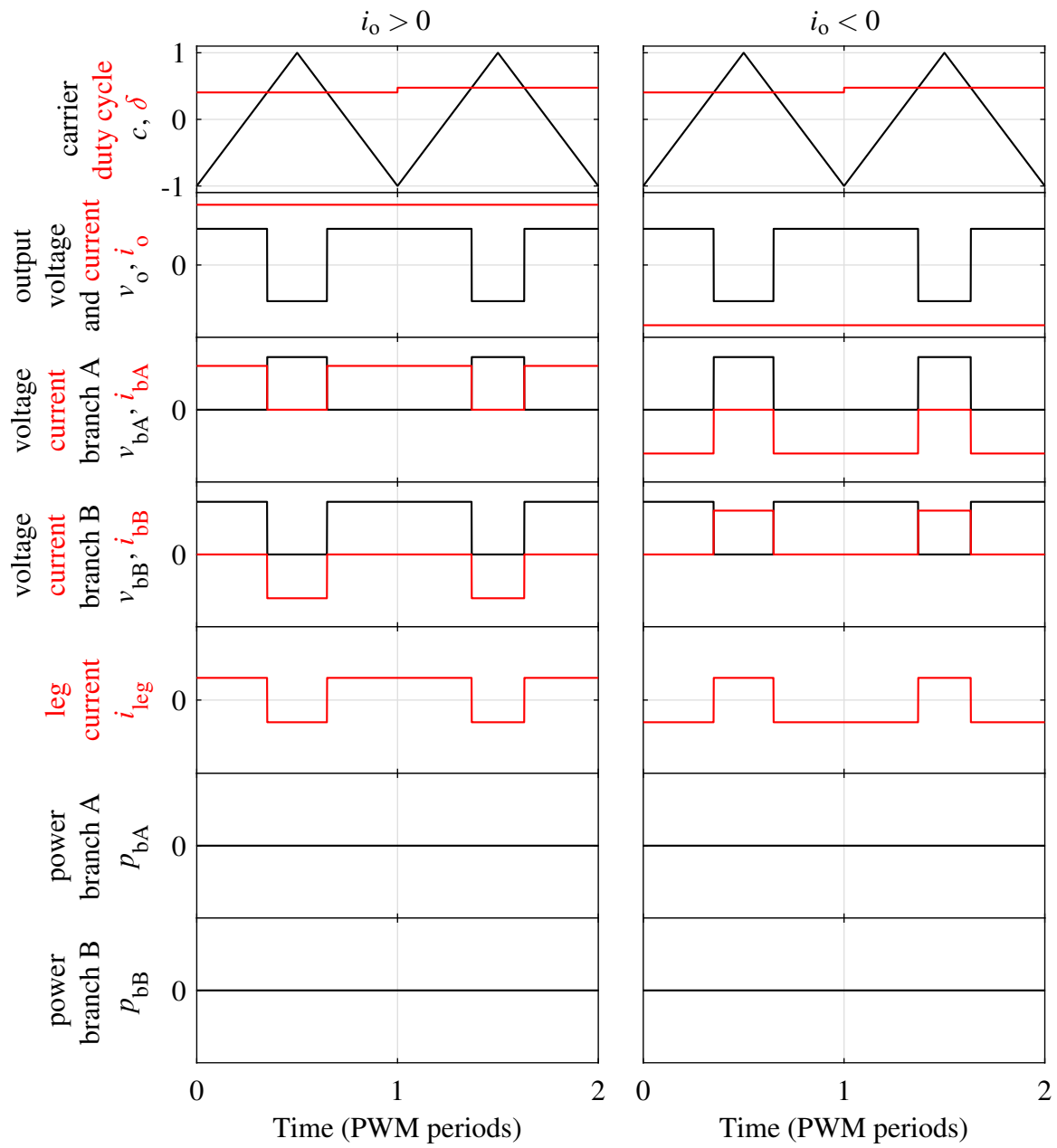


Figure 3.3: The prinicple of quasi-two-level PWM operation shown for a simplified model neglecting the voltage drops over branch inductors.

It is worth mentioning that the waveforms depicted in Figure 3.3 directly represent the idealized operation of the two-level VSI, where the branch currents and the branch voltages represent the currents through the two-level VSI's idealized switches and the voltage drops over these switches. For this reason, the quasi-two-level operation of the MMC can be viewed as an MMC which mimics the two-level VSI.

Up to this point, two crucial simplifications have been made:

- the leg current can be changed instantaneously with an infinite rate of change ($\mathrm{d}i_{\mathrm{leg}}/\mathrm{d}t \to \infty$),
- and the voltage drops over the branch inductances (caused by $\mathrm{d}i_{\mathrm{leg}}/\mathrm{d}t$) are zero.

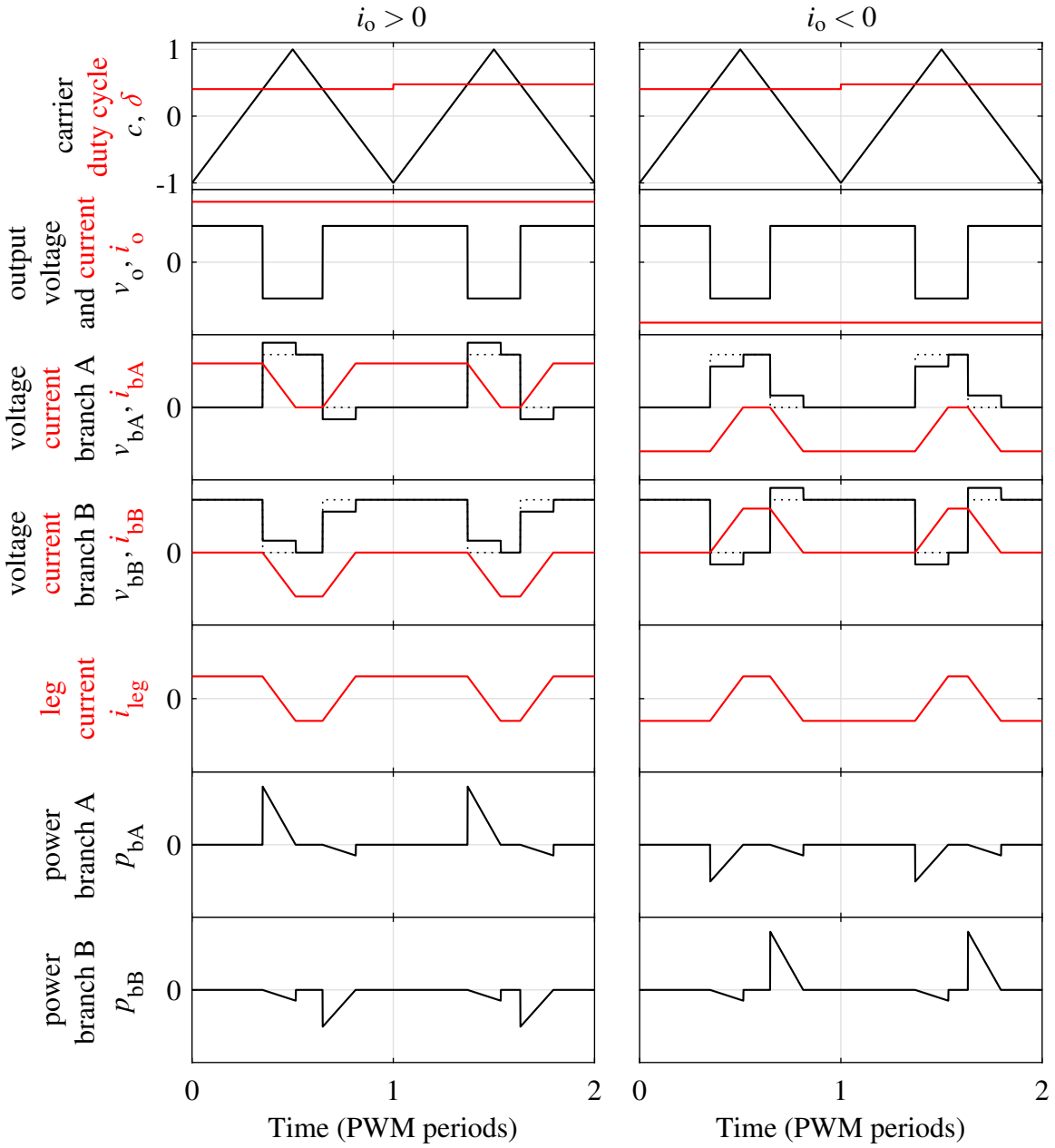


Figure 3.4: The prinicple of quasi-two-level PWM operation shown for a simplified model considering the voltage drops over branch inductors.

When these simplifications are removed, i.e. $\mathrm{d}i_{\mathrm{leg}}/\mathrm{d}t$ is limited to a finite value, and the branch voltages

$$\begin{bmatrix} v_{\mathrm{bA}} \\ v_{\mathrm{bB}} \end{bmatrix} = \begin{bmatrix} \frac{1}{2} & -1 \\ \frac{1}{2} & 1 \end{bmatrix} \cdot \begin{bmatrix} V_{\mathrm{i}} \\ v_{\mathrm{o}} \end{bmatrix} - \begin{bmatrix} \frac{1}{2} \\ \frac{1}{2} \end{bmatrix} \cdot L_{\mathrm{leg}} \cdot \frac{\mathrm{d}i_{\mathrm{leg}}}{\mathrm{d}t} \tag{3.16}$$

are extended by the voltage drop over the branch inductors, the MMC waveforms are modified as plotted in Figure 3.4.

As Figure 3.4 shows, the voltage drops over the branch inductors cause the required branch voltage to increase and at some points in time even to become negative. While the increased

branch voltage requires a higher number of installed modules, the negative branch voltage is not achievable at all if half-bridge modules are used. Therefore, in practice the plotted branch voltage values would have to be clipped, leading to a distortion of the leg current and the output current. However, the effect on the output current is relatively small and the leg current non-linearity due to the clipping can be compensated by the close-loop control. The first publications regarding quasi-two-level PWM operation [131, 132] were based on similar waveforms.

Additionally, Figure 3.4 demonstrates that the branch powers are non-zero while the leg current is being changed. Moreover, their mean value during a PWM period is also not zero. This means that if no countermeasures are applied, the branch power includes low-frequency components linked to the output frequency. Consequently, this leads to large branch energy variation, when the desired output frequency is low. Such countermeasures are explained later in this chapter.

A better method for changing the leg current is presented in [133] and is depicted in Figure 3.5. The main difference to the method described above is that the voltage necessary to change the leg current is generated by the overlap of the branch voltages or a gap between them. This way, the leg current is changed as quickly as possible without increasing the maximum necessary branch voltage above the input voltage value or requiring the branch voltages to become negative.

However, this method modifies the output voltage waveform, as the output voltage is zero when both branch voltages have the same value (3.9). Despite the deviation of the output voltage waveform, its mean value during one PWM period is not influenced, as the missing part of the positive voltage has the same time-voltage area as the missing part of the negative voltage. Nevertheless, this claim is only valid if the output current does not change during the PWM period. Otherwise, a voltage error occurs, which is thoroughly studied in Section 7.4.

Similarly to the method in Figure 3.4, the mean branch powers of the method in Figure 3.5 are also not equal to zero within one PWM period, and thus the branch powers comprise fundamental-frequency power components by default. If the output current changes between its negative and positive value within each PWM period, as presented for quasi-two-level operated MMCs with medium-frequency transformers for dc-dc applications in [125, 126], the branch powers are canceled out and the resulting branch energy variation is very small. However, when the output frequency, modulated by the PWM, approaches zero, the branch energy variation increases greatly. Thus, an active compensation of the branch power peaks depicted in Figure 3.5 is necessary[1)].

Such compensation is demonstrated in Figure 3.6. As the figure shows, the power peaks caused by the process of changing the leg current are compensated by a small branch current while the voltage of the corresponding branch is high. This small branch current value can be set in either branch by adjusting the leg current value i_{leg}:

$$\begin{bmatrix} i_{\mathrm{bA}} \\ i_{\mathrm{bB}} \end{bmatrix} = \begin{bmatrix} \frac{1}{2} & 1 \\ -\frac{1}{2} & 1 \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{o}} \\ i_{\mathrm{leg}} \end{bmatrix} \quad . \tag{3.17}$$

Consequently, the leg current is slightly increased, as can also be observed by comparing Figure 3.6 to Figure 3.5. If the described compensation is applied correctly, the mean value of

[1)] Recently, Wang *et al.* proposed a new control strategy in [134] with the goal of simplifying the control of the quasi-two-level PWM operation investigated in this thesis. The approach of Wang *et al.* does not implement the active compensation. Thus, a high module capacitor voltage variation linked to the output frequency is visible in the simulation results in [134] despite the relatively high module capacitance.

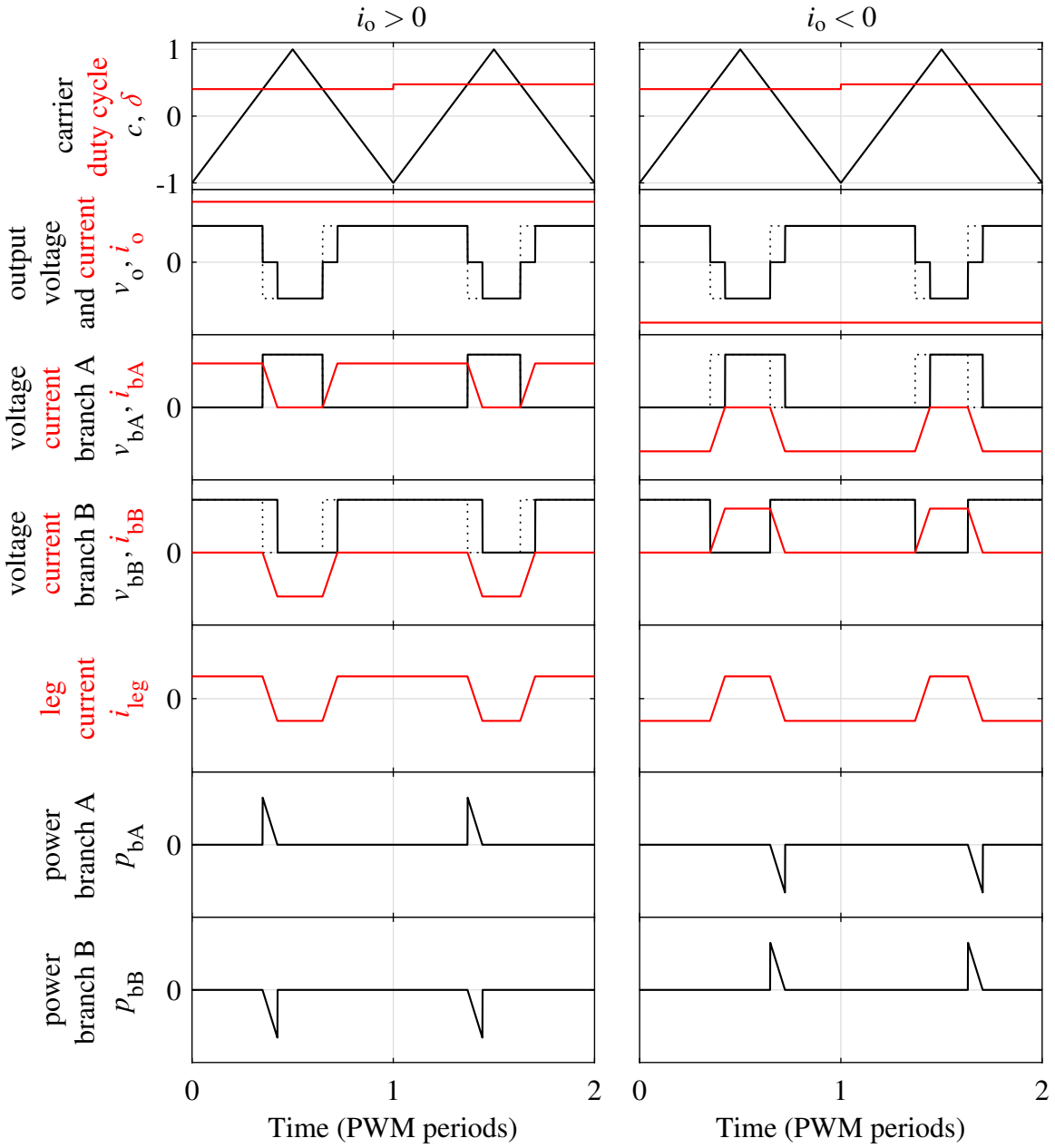


Figure 3.5: The prinicple of quasi-two-level PWM operation shown for a simplified model considering the voltage drops over branch inductors with improved branch voltage waveforms.

the branch power during a PWM period becomes zero, and thus the branch energy variation is no longer dependent on the output frequency. Now, it depends only on the output current value and the time period required to change the leg current.

For further discussion it is useful to introduce names for the individual parts of the PWM period. The fast changing of the leg current is referred to in this thesis as `TRANSITION STATE`. The state when the voltage of branch A is high and that of branch B is zero is referred to as `STATE A`. When branch voltage A is zero and branch voltage B is high, the state is referred to as `STATE B`.

At this point, a restriction of the quasi-two-level PWM-operated MMCs can be recognized: When duty cycle δ approaches 1 or -1, the time available for the compensation of branch-power

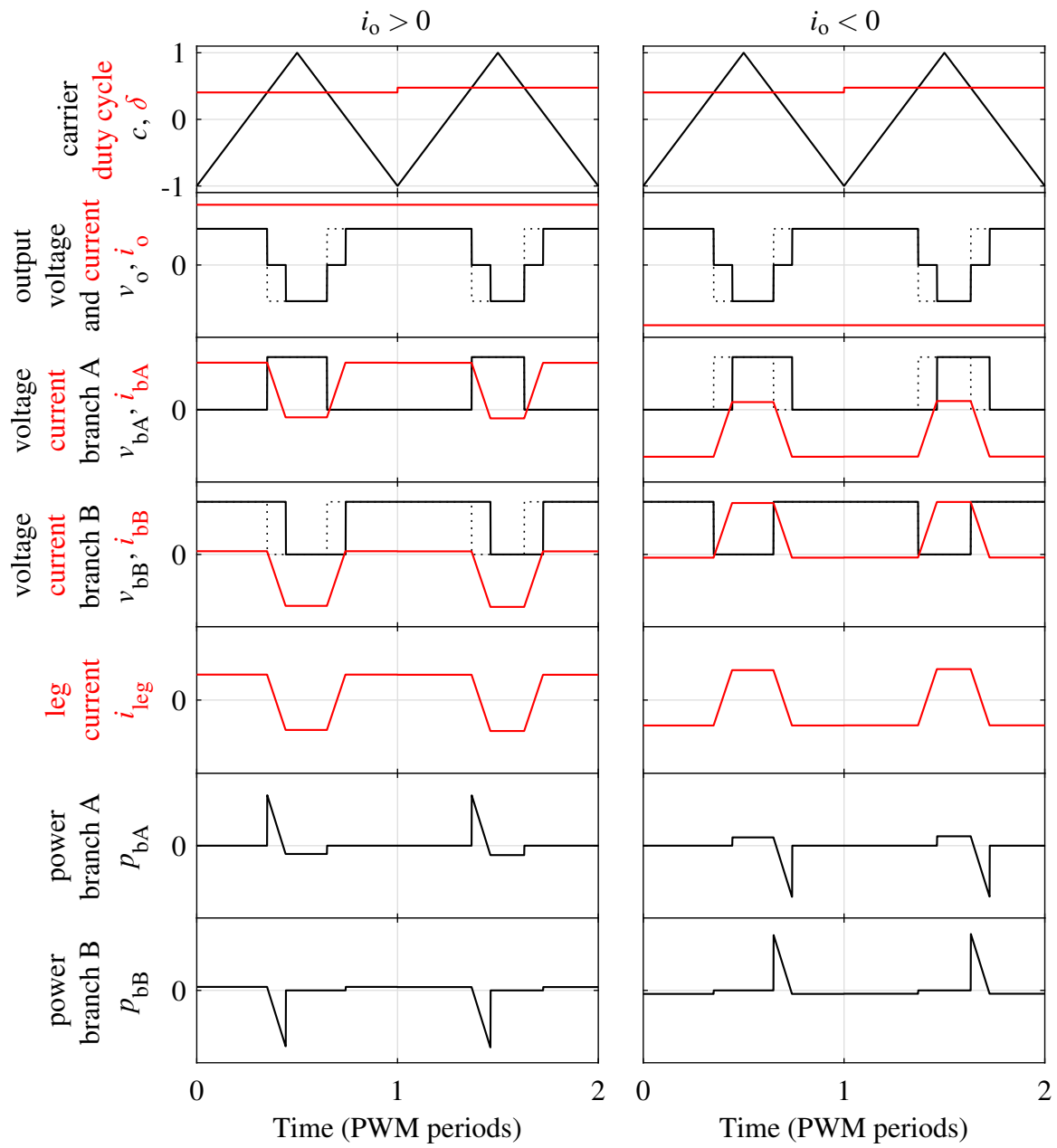


Figure 3.6: The prinicple of quasi-two-level PWM operation shown for a simplified model considering the voltage drops over branch inductors with improved branch voltage waveforms and branch power compensation.

peaks (the duration of `STATE A` or `STATE B`) becomes very short and the branch current required for compensation rises rapidly. Consequently, the maximum achievable duty cycle is limited to some value below one, similar to the quasi-two-level-operated diode-clamped multilevel converters in [123, 124]. This value is a design parameter. Note that the duty cycle being exactly 1 or -1 is not a problem, as in this case the `TRANSITION STATE` does not occur and thus there are no power peaks to be compensated.

The quasi-two-level PWM operation derived up to this point is based on a severely simplified model. To enable a practical application, it is necessary to extend this operation mode for the more detailed model considering the particular modules [see Figure 3.2a]. In such a model,

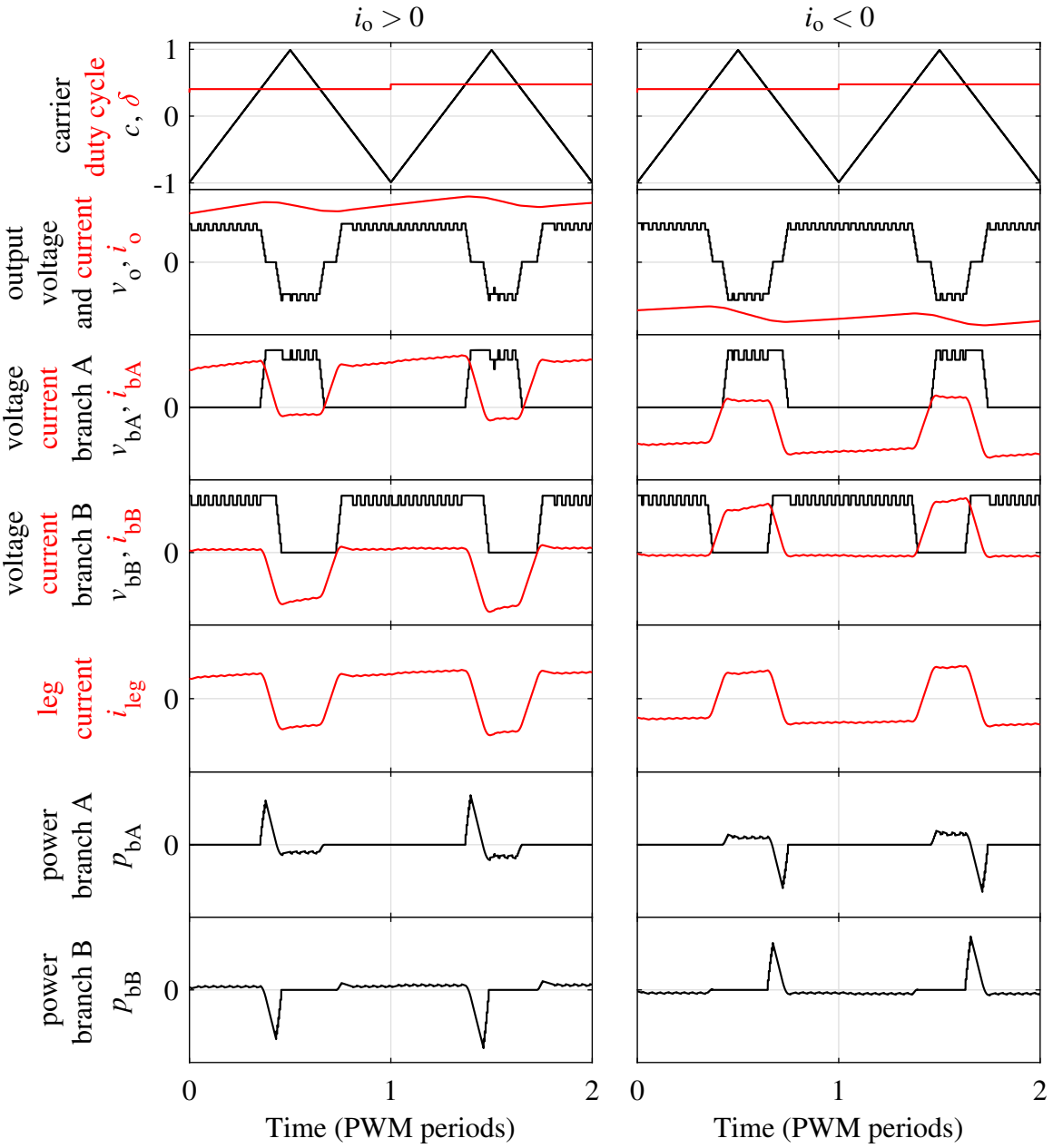


Figure 3.7: The prinicple of quasi-two-level PWM operation shown for a detailed simulation phase-leg MMC model with six modules per branch. The converter parameters are chosen to exaggerate different effects of the operation.

the branch voltage cannot be instantaneously set to a precise value, but only switched between the discrete voltage levels determined by the voltages of module capacitors. In Figure 3.7, the simulation of the quasi-two-level PWM operation including the individual modules is shown. During `TRANSITION STATE` all modules in both converter branches are short-circuited (the branch voltages are zero) to increase the leg current as fast as possible or all modules are inserted (the branch voltages are at their maximum achievable value) to quickly decrease the leg

current[2)]. During `STATE A` and `STATE B`, the branch voltage of Branch A or Branch B is set to actively control the leg current and its value approximates the input voltage value. Since the branch voltages must precisely fit their setpoint values, they are modulated with an additional high-frequency modulation (HF modulation). The HF modulation operates as the dedicated multilevel PWM described in the top part of Figure 2.6. As can be seen in Figure 3.7, the HF modulation mainly switches between two voltage levels with an amplitude of one module capacitor's voltage, which is typical for MMCs. Despite the high modulation frequency of the HF modulation, the additional switching losses are expected to be acceptable, as the branch currents of Branch A and Branch B are low during `STATE A` and `STATE B`, respectively. Note that the active closed-loop control of the leg current with the HF modulation is effectively damping the natural resonant circuit within the MMC. Consequently, the current overshoots, typical for approaches in [125, 127, 129], do not appear in the branch currents.

As explained at the beginning of this chapter, one of the general goals of a quasi-two-level operation is to limit the $\mathrm{d}v/\mathrm{d}t$ of the output voltage by the application of a trapezoidal staircase voltage waveform. This voltage shape can be achieved by forcing a minimum delay time between each two module switching instants within one branch. Consequently, these delays lead to staircase waveforms of both branch voltages, which subsequently lead to a staircase waveform of the output voltage [see Figure 3.7].

Since the form of branch voltages results from two overlaying modulations (PWM modulation and HF modulation), the module balancing within a branch must be based on the principles described for the two-step modulation approaches [see Section 2.2.2].

The presented operation mode can be further extended to MMCs consisting of more than a single phase leg. In Figure 3.8, simulated waveforms for the first phase leg of a three-phase MMC are plotted. Since the star point of the load is usually not grounded, a common-mode voltage occurs as a superposition of the output voltages of the individual phase legs. This modifies the phase voltage waveform. Nevertheless, its $\mathrm{d}v/\mathrm{d}t$ remains limited (as does the $\mathrm{d}v/\mathrm{d}t$ of the common-mode voltage). The modified phase voltage translates into a lower output-current ripple. Moreover, since the common-mode voltage does not influence the output currents, common-mode-voltage injection techniques, well-known from the two-level VSIs, can be applied. The application is further studied in Section 7.1.

[2)] Note that the state where all modules of both branches are inserted does not increase the insulation requirements for the converter modules, the mechanical construction of branches, or the input dc-link capacitor because the additional voltage component generated in the branch voltages is applied to the branch inductors. The insulation system of the inductors must be designed accordingly to withstand this voltage.

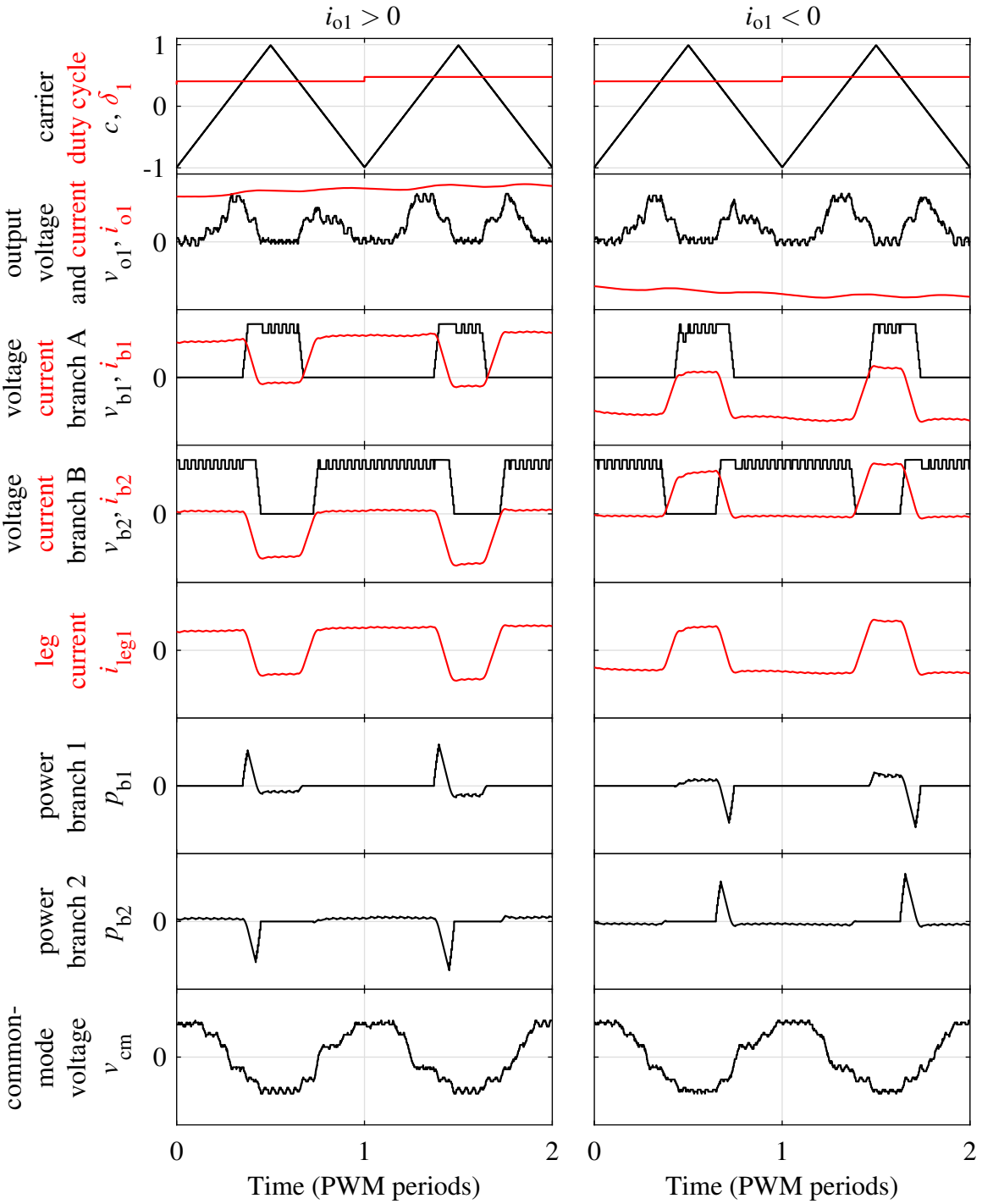


Figure 3.8: The prinicple of quasi-two-level PWM operation shown for a detailed three-phase simulation model. The converter parameters are chosen to exaggerate different effects of the operation. The labels for branches and phases correspond to definitions from Chapter 2.

4 Design Trade-Offs of Quasi-Two-Level PWM-Operated MMCs

This chapter studies the design of quasi-two-level PWM-operated MMCs and investigates the relationships between the particular design parameters. The derivations made are based on the simplified modeling presented in the previous chapter. Selected equations are validated in Appendix B.

4.1 Derivation of Branch Energy Variation and Compensating Current

To understand the trade-offs within the design, the maximum branch energy variation, which determines the size of module capacitors, and the required value of the branch current for its compensation must be derived first. The basis for the derivation is the simplified modeling presented in the previous chapter and demonstrated in Figure 3.6. As can be observed in the figure, the direction of the output current does not influence the absolute values of compensating currents nor the absolute peak branch power values, and thus only the part that involves positive output currents is considered. The waveforms relevant to the following investigations are displayed in more detail in Figure 4.1.

The branch energy variation of Branch A and Branch B

$$\begin{bmatrix} \Delta e_{\mathrm{bA}} \\ \Delta e_{\mathrm{bB}} \end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix} |\hat{p}_{\mathrm{bA}}| \cdot T_{\mathrm{T,bA}} \\ |\hat{p}_{\mathrm{bB}}| \cdot T_{\mathrm{T,bB}} \end{bmatrix} \tag{4.1}$$

can be calculated as the triangle area under the branch-power peak. The height of the triangle is the branch-power peak value

$$\begin{bmatrix} \hat{p}_{\mathrm{bA}} \\ \hat{p}_{\mathrm{bB}} \end{bmatrix} = \hat{v}_{\mathrm{b}} \cdot \begin{bmatrix} \hat{i}_{\mathrm{bA}} \\ \hat{i}_{\mathrm{bB}} \end{bmatrix} \quad , \tag{4.2}$$

determined by the peak value of the branch voltages $\hat{v}_{\mathrm{b}}$ (assumed to be equal for both branches) and the peak value of the corresponding branch currents $\hat{i}_{\mathrm{bA}}$ and $\hat{i}_{\mathrm{bB}}$. The length of the triangle of Branch A is the time period $T_{\mathrm{T,bA}}$ between when the `TRANSITION STATE` started and the branch current i_{bA} reached zero. The length of the triangle of Branch B is the time period $T_{\mathrm{T,bB}}$ between when the branch current i_{bB} reached zero and the `TRANSITION STATE` ended.

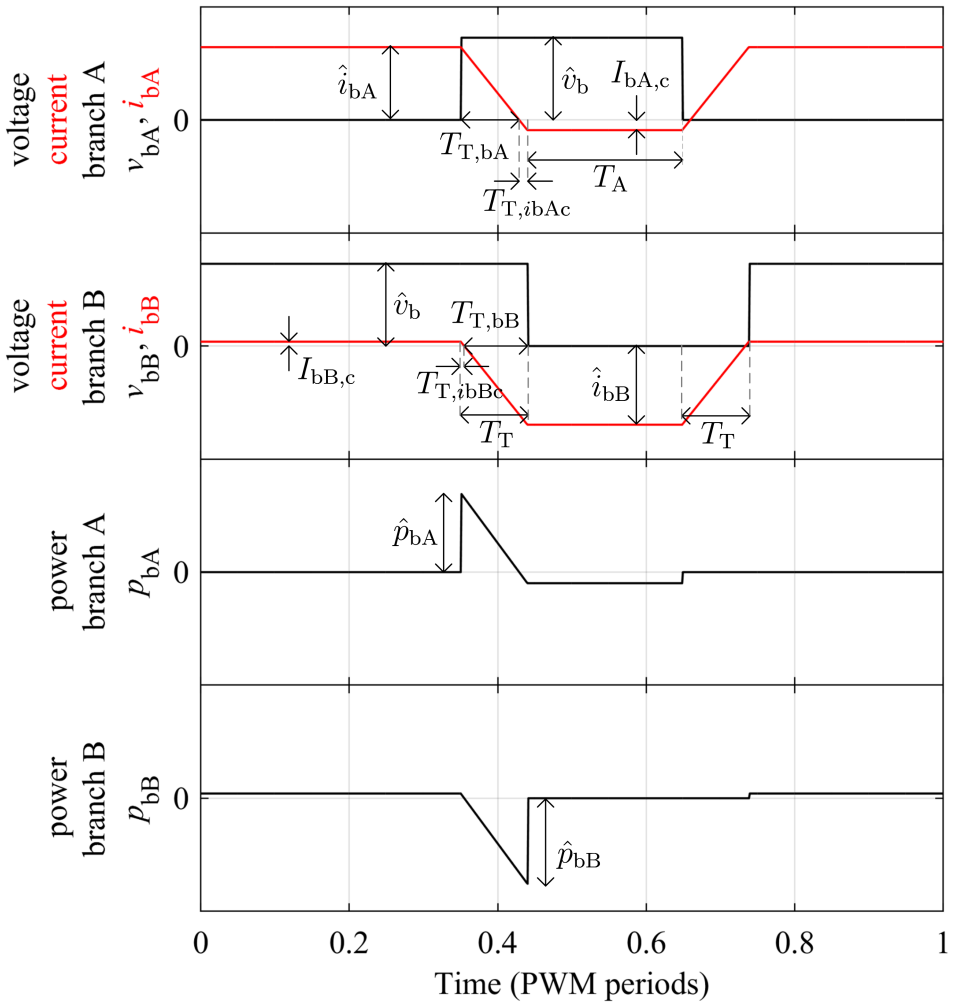


Figure 4.1: Waveforms of quasi-two-level PWM operation based on the simplified model, used for the derivation of the branch energy variation and the compensating current values. The figure is a detail of Figure 3.6.

Assuming the branch resistances are both zero $R_b \approx 0$, the part of the state-space representation in (3.4) regarding the leg current can be expressed as:

$$V_i - v_{bA} - v_{bB} = L_{leg} \cdot \frac{\Delta i_{leg}}{\Delta T} \quad . \tag{4.3}$$

Both branch voltages

$$\begin{bmatrix} v_{bA} \\ v_{bB} \end{bmatrix} = \hat{v}_b \cdot \begin{bmatrix} 1 \\ 1 \end{bmatrix} \tag{4.4}$$

have the same constant value $\hat{v}_b$ during the relevant `TRANSITION STATE`. During the time period $\Delta T = T_{T,bA}$, the leg current must be changed by the value of $\Delta i_{leg} = -|\hat{i}_{bA}|$. During the time period $\Delta T = T_{T,bB}$, it must be changed by the value of $\Delta i_{leg} = -|\hat{i}_{bB}|$.

Substituting these values into (4.3), the time periods determining the branch energy variation

$$\begin{bmatrix} T_{\mathrm{T,bA}} \\ T_{\mathrm{T,bB}} \end{bmatrix} = \frac{L_{\mathrm{leg}}}{2 \cdot \hat{v}_{\mathrm{b}} - V_{\mathrm{i}}} \cdot \begin{bmatrix} |\hat{i}_{\mathrm{bA}}| \\ |\hat{i}_{\mathrm{bB}}| \end{bmatrix} \tag{4.5}$$

can be expressed. These can be further substituted together with (4.2) into (4.1) to obtain the branch energy variation for Branch A and Branch B

$$\begin{bmatrix} \Delta e_{\mathrm{bA}} \\ \Delta e_{\mathrm{bB}} \end{bmatrix} = \frac{1}{2} \cdot \frac{\hat{v}_{\mathrm{b}}}{2 \cdot \hat{v}_{\mathrm{b}} - V_{\mathrm{i}}} \cdot L_{\mathrm{leg}} \cdot \begin{bmatrix} \hat{i}^2_{\mathrm{bA}} \\ \hat{i}^2_{\mathrm{bB}} \end{bmatrix} \quad . \tag{4.6}$$

For the idealized case that no compensating currents are necessary, the peak value of the branch currents is $\pm i_{\mathrm{o}}$ [see (3.15)]. However, since the compensating current $I_{\mathrm{bA,c}}$ is applied in Branch A during `STATE A`, the leg current is increased, and thus the branch current in Branch B is also increased by this value [see (3.17)]. Analogously, the compensating current of Branch B $I_{\mathrm{bB,c}}$ increases the branch current of Branch A during `STATE B`. Consequently, the absolute peak values of the branch currents can be expressed as the sum of the output-current absolute value (assumed constant during a PWM period) and the absolute value of the necessary compensating current in the opposite branch:

$$\begin{bmatrix} |\hat{i}_{\mathrm{bA}}| \\ |\hat{i}_{\mathrm{bB}}| \end{bmatrix} = \begin{bmatrix} |i_{\mathrm{o}}| \\ |i_{\mathrm{o}}| \end{bmatrix} + \begin{bmatrix} |I_{\mathrm{bB,c}}| \\ |I_{\mathrm{bA,c}}| \end{bmatrix} \quad . \tag{4.7}$$

Substituting these values into (4.6) and assuming the branch voltages have approximately the same value as the input voltage during the investigated `TRANSITION STATE` $\hat{v}_{\mathrm{b}} \approx V_{\mathrm{i}}$ leads to the following expression for the branch energy variation:

$$\begin{bmatrix} \Delta e_{\mathrm{bA}} \\ \Delta e_{\mathrm{bB}} \end{bmatrix} = \frac{1}{2} \cdot L_{\mathrm{leg}} \cdot \begin{bmatrix} \left(|i_{\mathrm{o}}| + |I_{\mathrm{bB,c}}|\right)^2 \\ \left(|i_{\mathrm{o}}| + |I_{\mathrm{bA,c}}|\right)^2 \end{bmatrix} \quad . \tag{4.8}$$

In the next step, the expression for the compensating current is derived. The basis for the derivation is the fact that the branch energy disturbance in Branch A and Branch B (Δe_{bA} and Δe_{bB}), described by (4.8), must be compensated for with the corresponding compensating currents $I_{\mathrm{bA,c}}$ and $I_{\mathrm{bB,c}}$ multiplied with the branch voltage $v_{\mathrm{bA}} \approx V_{\mathrm{i}}$ or $v_{\mathrm{bB}} \approx V_{\mathrm{i}}$:

$$\begin{bmatrix} \Delta e_{\mathrm{bA}} \\ \Delta e_{\mathrm{bB}} \end{bmatrix} = V_{\mathrm{i}} \cdot \begin{bmatrix} |I_{\mathrm{bA,c}}| \cdot T_{\mathrm{A}} \\ |I_{\mathrm{bB,c}}| \cdot T_{\mathrm{B}} \end{bmatrix} + \frac{1}{2} \cdot V_{\mathrm{i}} \cdot \begin{bmatrix} |I_{\mathrm{bA,c}}| \cdot T_{\mathrm{T},i\mathrm{bAc}} \\ |I_{\mathrm{bB,c}}| \cdot T_{\mathrm{T},i\mathrm{bBc}} \end{bmatrix} \quad . \tag{4.9}$$

The first part of (4.9) represents the compensation during `STATE A` with time period T_{A} and during `STATE B` with time period T_{B}. The second part of the equation represents the small triangle of the compensating current during `TRANSITION STATE`.

The time duration of `STATE A` and `STATE B`

$$\begin{bmatrix} T_{\mathrm{A}} \\ T_{\mathrm{B}} \end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix} 1-\delta \\ 1+\delta \end{bmatrix} \cdot \frac{1}{f_{\mathrm{PWM}}} - T_{\mathrm{T}} \cdot \begin{bmatrix} 1 \\ 1 \end{bmatrix} \quad , \tag{4.10}$$

are determined by the duty cycle δ [defined in (3.13)], the modulation frequency of the PWM

f_{PWM}, and the duration of `TRANSITION STATE` T_{T}.

The duration of each `TRANSITION STATE`

$$T_{\mathrm{T}} = T_{\mathrm{T},i\mathrm{o}} + T_{\mathrm{T},i\mathrm{bAc}} + T_{\mathrm{T},i\mathrm{bBc}} \tag{4.11}$$

is the sum of the time necessary to change the leg current by a value of the output current, the time necessary to change it by the value of the compensating current of Branch A, and the time necessary to change it by the value of the compensating current of Branch B. These time periods

$$\begin{bmatrix} T_{\mathrm{T},i\mathrm{o}} \\ T_{\mathrm{T},i\mathrm{bAc}} \\ T_{\mathrm{T},i\mathrm{bBc}} \end{bmatrix} = \frac{L_{\mathrm{leg}}}{V_{\mathrm{i}}} \cdot \begin{bmatrix} |i_{\mathrm{o}}| \\ |I_{\mathrm{bA,c}}| \\ |I_{\mathrm{bB,c}}| \end{bmatrix} \tag{4.12}$$

can be calculated using (4.3) by setting $V_{\mathrm{i}} - v_{\mathrm{bA}} - v_{\mathrm{bB}} \approx V_{\mathrm{i}}$ and setting the change of leg current Δi_{leg} to $|i_{\mathrm{o}}|$, $|I_{\mathrm{bA,c}}|$ or $|I_{\mathrm{bB,c}}|$.

Eliminating Δe_{bA}, Δe_{bB}, T_{A}, T_{B}, $T_{\mathrm{T},i\mathrm{bAc}}$, $T_{\mathrm{T},i\mathrm{bBc}}$, $T_{\mathrm{T},i\mathrm{o}}$, and T_{T} from the set of equations described by (4.8) – (4.12), the values of the compensating currents

$$\begin{bmatrix} |I_{\mathrm{bA,c}}| \\ |I_{\mathrm{bB,c}}| \end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix} 1+\delta \\ 1-\delta \end{bmatrix} \cdot \left(\frac{V_{\mathrm{i}}}{L_{\mathrm{leg}} \cdot f_{\mathrm{PWM}}} \cdot \frac{1-\delta^2}{4} - |i_{\mathrm{o}}| \ldots \right. \\ \left. - \sqrt{\left(\frac{V_{\mathrm{i}}}{L_{\mathrm{leg}} \cdot f_{\mathrm{PWM}}} \cdot \frac{1-\delta^2}{4} \right)^2 - \frac{V_{\mathrm{i}} \cdot |i_{\mathrm{o}}|}{L_{\mathrm{leg}} \cdot f_{\mathrm{PWM}}} \cdot \frac{1-\delta^2}{2}} \right) \tag{4.13}$$

can be expressed as a function of the input voltage V_{i}, the output current $|i_{\mathrm{o}}|$ and the duty cycle δ.

4.2 Influence of the Design Parameters on the Design of the Components

Using the expression for $|I_{\mathrm{bA,c}}|$ from (4.13) and substituting for it with its maximum allowed value $I_{\mathrm{b,c,max}}$, the required value of the leg inductance L_{leg} can be determined. The maximum value of the compensating current occurs when the maximum output current $i_{\mathrm{o,max}}$ and the required maximum duty cycle δ_{max} are applied at the same time. Thus, the required value of the leg inductance can be expressed as:

$$L_{\mathrm{leg}} \leq \frac{1-\delta_{\mathrm{max}}}{f_{\mathrm{PWM}}} \cdot V_{\mathrm{i}} \cdot \frac{I_{\mathrm{b,c,max}}}{\left(i_{\mathrm{o,max}} + \frac{I_{\mathrm{b,c,max}}}{\frac{1+\delta_{\mathrm{max}}}{2}} \right)^2} \quad , \tag{4.14}$$

dependent on the design parameters:

- chosen PWM frequency f_{PWM},

- maximum achievable duty cycle $\delta_{\max}$,
- maximum output current $i_{\mathrm{o,max}}$, and
- maximum allowed compensating current in any of the branches $I_{\mathrm{b,c,max}}$.

While the maximum output current $i_{\mathrm{o,max}}$ and the PWM frequency f_{PWM} are mainly a direct result of the application requirements, the maximum duty cycle $\delta_{\max}$ and the maximum allowed compensating current $I_{\mathrm{b,c,max}}$ should be used to find the design optimum (assuming the input voltage is a degree of freedom).

Generally, the duty cycle is desired to be as high as possible, since this increases the achievable output voltage of the converter for a given input voltage. The maximum compensating current is desired to be as low as possible, since it increases the converter losses and has the potential to reduce the maximum achievable output current. Nevertheless, if the maximum duty cycle is selected too high and the compensating current is selected too low, an extremely low leg inductance must be installed at the converter. While this would be advantageous for the inductor size, it would also lead to a very high HF-modulation frequency

$$f_{\mathrm{HF}} \geq \frac{1}{4} \cdot \frac{V_C}{L_{\mathrm{leg}} \cdot \Delta i_{\mathrm{b,r,max}}}, \tag{4.15}$$

for the defined maximum peak-to-peak current ripple $\Delta i_{\mathrm{b,r,max}}$ and module capacitor voltage V_C[1)]. Consequently, a trade-off between the maximum duty cycle $\delta_{\max}$, the maximum allowed compensating current $I_{\mathrm{b,c,max}}$, and the HF-modulation frequency f_{HF} must be chosen.

Besides the inductance of the leg inductors and the HF-modulation frequency, the third significant parameter is the module capacitance

$$C_{\mathrm{mod}} = k_e \cdot \frac{2}{V_{C,\max}^2 - V_{C,\min}^2} \cdot \left(\frac{\Delta e_{\mathrm{b,max}}}{n_{\mathrm{mpb}}} + \Delta e_{\mathrm{mod,d,max}} \right) \quad . \tag{4.16}$$

This is designed according to the maximum branch energy variation $\Delta e_{\mathrm{b,max}}$ divided equally between n_{mpb} modules in a branch, the worst-case module energy imbalance between the modules of a same branch $\Delta e_{\mathrm{mod,d,max}}$ caused by the staircase waveforms of branch voltages, and the module capacitor voltage boundaries $V_{C,\min}$ and $V_{C,\max}$. The factor k_e (typically in the range from 1.05 to 1.5) is chosen to provide a sufficient margin for the converter control and transient states. The maximum branch energy variation

$$\Delta e_{\mathrm{b,max}} = \frac{1}{2} \cdot L_{\mathrm{leg}} \cdot \left(i_{\mathrm{o,max}} + I_{\mathrm{b,c,max}} \right)^2 \tag{4.17}$$

can be expressed using (4.8) and is proportional to the leg inductance value and the squared value of the maximum branch current.

The worst-case module energy variation caused by delayed switching $\Delta e_{\mathrm{mod,d,max}}$ accounts for the energy imbalance between the modules of a single branch. This energy imbalance is caused by the fact that the branch voltage is not changed instantaneously, but step-wise module-by-module with a time delay T_{d} between each two subsequent switching instants. This can be seen

[1)] Since only one branch is active while the HF-modulation is applied, the basis for the derivation of (4.15) is a symmetric PWM applied to a single module switched with a worst-case duty-cycle value of 50 %.

in Figure 3.7. As a consequence, the module inserted first (or short-circuited last) is inserted for a longer period of time than the module inserted last (or short-circuited first) by the time period $\left(n_{\mathrm{mpb}}-1\right)\cdot T_{\mathrm{d}}$. Additionally, it can be assumed that the branch current has its maximum value $\hat{i}_{\mathrm{b}} = i_{\mathrm{o,max}} + I_{\mathrm{b,c,max}}$ and does not change significantly during the time period in which the branch voltage rises or falls (T_{T} is assumed significantly longer than $\left(n_{\mathrm{mpb}}-1\right)\cdot T_{\mathrm{d}}$). Thus, in the worst case, the maximum module power

$$\hat{p}_{\mathrm{mod}} = V_{C,\mathrm{max}} \cdot \hat{i}_{\mathrm{b}} = V_{C,\mathrm{max}} \cdot \left(i_{\mathrm{o,max}} + I_{\mathrm{b,c,max}}\right) \tag{4.18}$$

applies to the modules during the time period in which they are inserted. The worst-case module energy variation caused by delayed switching

$$\Delta e_{\mathrm{mod,d,max}} = \left(n_{\mathrm{mpb}}-1\right)\cdot T_{\mathrm{d}} \cdot V_{C,\mathrm{max}} \cdot \left(i_{\mathrm{o,max}} + I_{\mathrm{b,c,max}}\right) - 0 \tag{4.19}$$

is then calculated as the difference of the energy of the module inserted for longest time $\left(n_{\mathrm{mpb}}-1\right)\cdot T_{\mathrm{d}}$ and that of the module inserted for shortest time 0.

In the following part of the chapter, the design trade-offs will be discussed and demonstrated based on a variation of design parameters. The required module capacitance is investigated indirectly, using only the branch energy variation as an indicator.

In Figure 4.2, the leg inductance, the branch energy variation and the HF-modulation frequency are plotted in relation to the maximum allowed duty cycle and the maximum compensating current. As expected, the leg inductance can be increased by allowing only lower duty cycles or by increasing the maximum allowed compensating current. The higher leg inductance leads to lower required HF-modulation frequencies, which is generally welcome. While decreasing the maximum allowed duty cycle increases the leg inductance linearly, increasing the maximum compensating current is efficient only for low values. As can be observed in Figure 4.2, increasing the maximum compensating current above 60 % of the maximum output current is rather impractical, since it only increases the branch energy variation, while the HF-modulation frequency is influenced only slightly.

While the leg inductance and the branch energy variation are dependent on the maximum output current, the HF-modulation frequency

$$f_{\mathrm{HF}} \geq \frac{1}{4}\cdot\frac{1}{1-\delta_{\mathrm{max}}}\cdot\frac{\left(1+\frac{I_{\mathrm{b,c,rel}}}{\frac{1+\delta_{\mathrm{max}}}{2}}\right)^2}{I_{\mathrm{b,c,rel}}\cdot\Delta i_{\mathrm{b,r,rel}}}\cdot\frac{V_C}{V_{\mathrm{i}}}\cdot f_{\mathrm{PWM}} \quad , \tag{4.20}$$

depends only on the relative values of the maximum compensating current and of the maximum allowed peak-to-peak branch-current ripple

$$\begin{bmatrix} I_{\mathrm{b,c,rel}} \\ \Delta i_{\mathrm{b,r,rel}} \end{bmatrix} = \frac{1}{i_{\mathrm{o,max}}}\cdot\begin{bmatrix} I_{\mathrm{b,c,max}} \\ \Delta i_{\mathrm{b,r,max}} \end{bmatrix} \quad . \tag{4.21}$$

Equation (4.20) was obtained by substituting (4.14) and (4.21) into (4.15).

Approximating the ratio between the input voltage and the module capacitor voltage with the

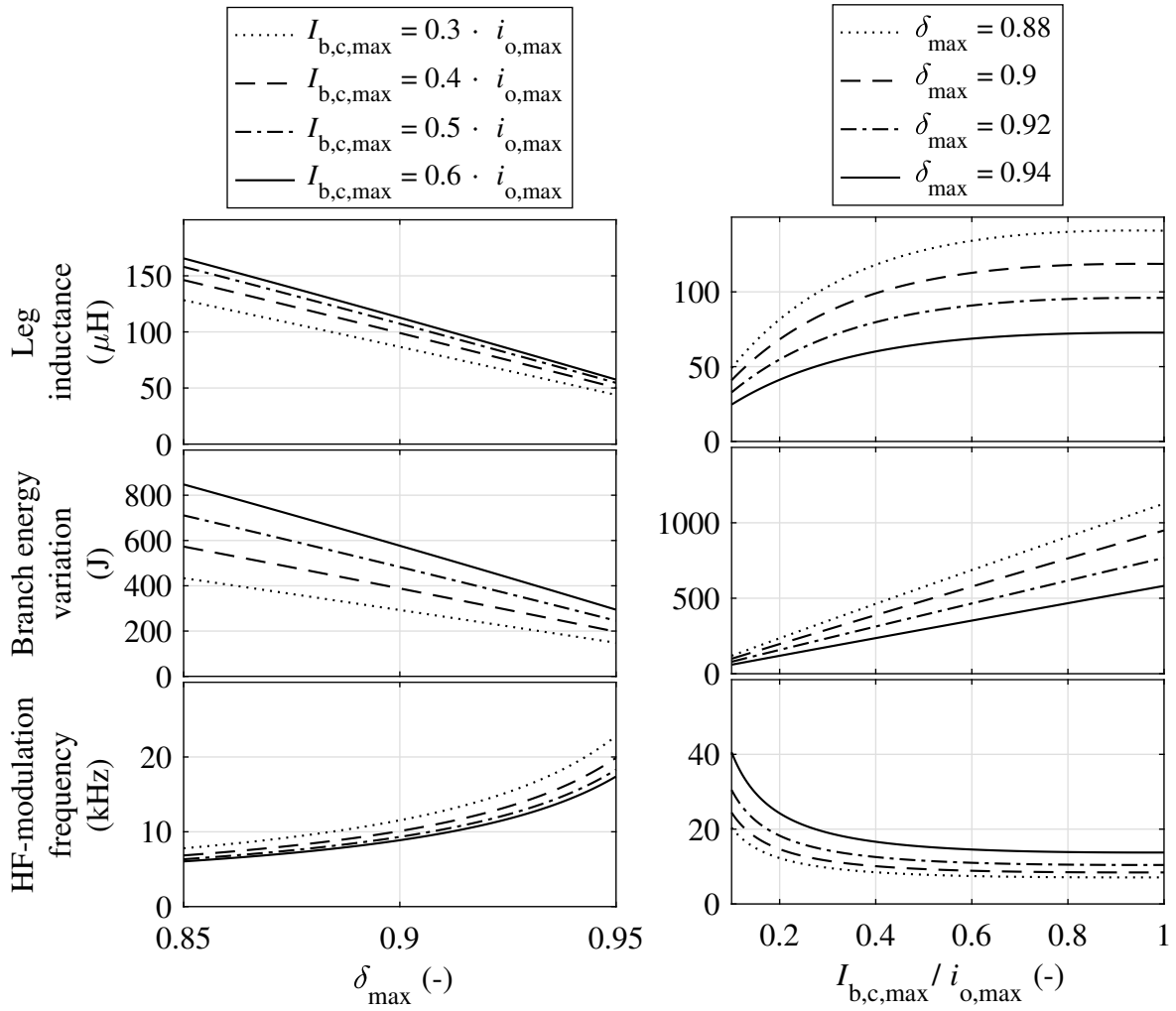


Figure 4.2: The dependence of the maximum leg inductance, the branch energy variation and the minimum HF-modulation frequency on the maximum duty cycle $\delta_{\max}$ and the maximum compensating current $I_{\mathrm{b,c,max}}$. The maximum output current is $i_{\mathrm{o,max}} = 2$ kA, the input voltage is $V_{\mathrm{i}} = 10$ kV, the PWM frequency is $f_{\mathrm{PWM}} = 1$ kHz, the module capacitor voltage is $V_C = 800$ V, and the maximum branch current ripple is $\Delta i_{\mathrm{b,r,max}} = 0.1 \cdot i_{\mathrm{o,max}}$.

number of required modules per branch

$$\frac{V_{\mathrm{i}}}{V_C} \approx n_{\mathrm{mpb}} \quad , \tag{4.22}$$

(4.20) can be transformed into the following form:

$$\delta_{\max} \approx 1 - \frac{1}{4} \cdot \frac{\left(1 + \frac{I_{\mathrm{b,c,rel}}}{\frac{1+\delta_{\max}}{2}}\right)^2}{I_{\mathrm{b,c,rel}} \cdot \Delta i_{\mathrm{b,r,rel}}} \cdot \frac{1}{n_{\mathrm{mpb}}} \cdot \frac{f_{\mathrm{PWM}}}{f_{\mathrm{HF}}} \quad . \tag{4.23}$$

This describes the maximum duty cycle as a function of the relative factors for the maximum compensating current $I_{\mathrm{b,c,rel}}$ and the maximum allowed peak-to-peak current ripple $\Delta i_{\mathrm{b,r,rel}}$, the number of modules per branch n_{mpb}, the PWM frequency f_{PWM}, and the HF-modulation frequency f_{HF}. Note that the equation is not in its explicit form, since the explicit form is very complex and has numerous solutions. Instead, the equation is solved numerically. For an

interpretation of this equation, the maximum duty cycle can be assumed to be near one, and thus the following approximation is valid:

$$\left(1+\frac{I_{\mathrm{b,c,rel}}}{\frac{1+\delta_{\max}}{2}}\right)^2 \approx \left(1+I_{\mathrm{b,c,rel}}\right)^2 \quad . \tag{4.24}$$

Equation (4.23) expresses several facts. The first is that the number of modules per branch significantly influences the maximum achievable duty cycle. Consequently, the number of installed modules per branch has to be above a certain value if the quasi-two-level PWM operation is to be applied. The second and previously described fact is that increasing the maximum compensating current increases the maximum duty cycle. However, the improvement becomes more marginal the higher the compensating current is. Moreover, an increase in the relative compensating current above approximately one leads to a decrease of the maximum achievable duty cycle. The third aforementioned fact is that increasing the HF-modulation frequency also increases the maximum duty cycle.

Figure 4.3 shows the dependence of the maximum achievable duty cycle on the number of installed modules per branch for different (reasonable) values of the compensating current. The other chosen parameters are listed in the figure's caption. As can be observed in the figure, the maximum duty cycle is strongly dependent on the number of installed modules and the increase of the compensating current leads to higher achievable duty cycles.

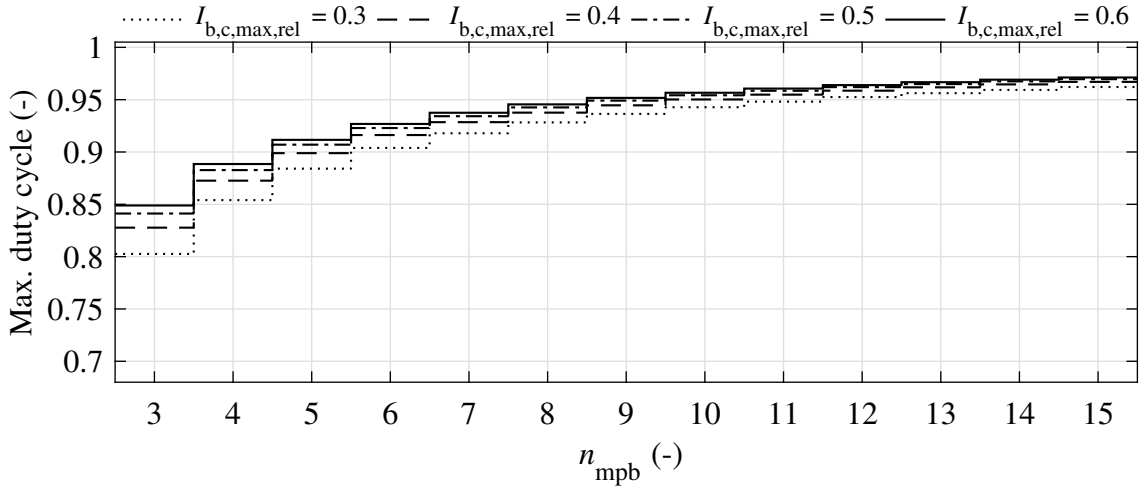


Figure 4.3: Maximum achievable duty cycle $\delta_{\max}$ versus the number of installed modules per branch n_{mpb} for various compensating current values. The HF-modulation frequency is $f_{\mathrm{HF}} = 25$ kHz, the PWM frequency is $f_{\mathrm{PWM}} = 1$ kHz, and the maximum relative peak-to-peak current ripple is $\Delta i_{\mathrm{b,r,rel}} = 0.1$.

For many designs there is a maximum HF-modulation frequency, which is determined by the capability of the semiconductor switches. The HF-modulation frequency can be set relatively high even with low-frequency switching semiconductors, since the HF modulation causes only small losses. This is because the switched current has approximately the same value as the compensating current, which is very low for most of the time. Furthermore, the compensating current achieves high values (up to $I_{\mathrm{b,c,max}}$) only when the duty cycle approaches its maximum

value ($\delta \approx \pm\delta_{\max}$), and thus the corresponding `STATE A` or `STATE B` is very short. Consequently, HF modulation is applied only for a very short period of time when the switched currents are high. This can be observed, e.g., in Figure 3.7.

In Figure 4.4, the dependency of the maximum duty cycle on the number of installed modules and different HF-modulation frequencies is displayed. The figure clearly shows that increasing the HF-modulation frequency leads to higher achievable duty cycles.

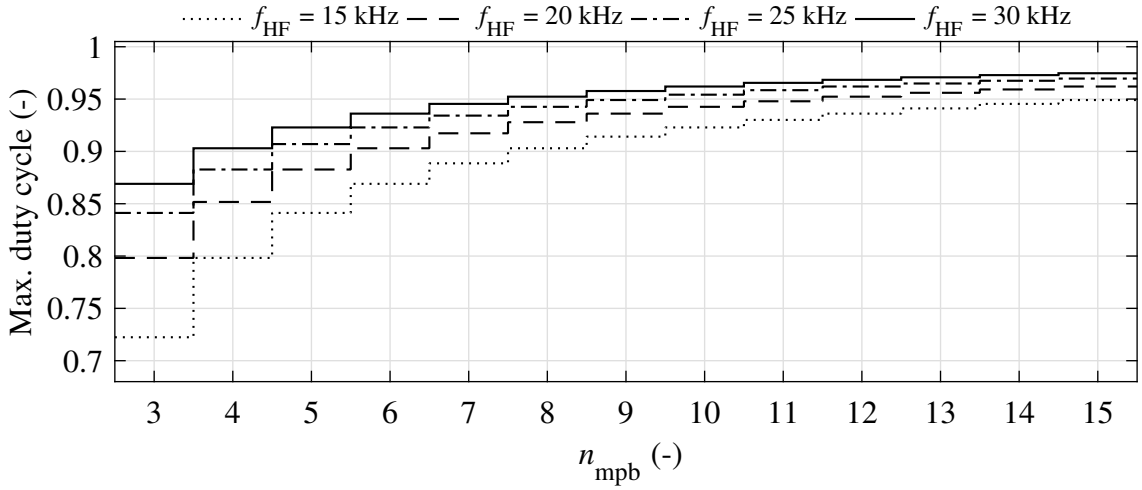


Figure 4.4: Maximum achievable duty cycle $\delta_{\max}$ versus the number of installed modules per branch n_{mpb} for various HF-modulation frequencies. The maximum allowed relative compensating current value is $I_{\mathrm{b,c,rel}} = 0.5$, the PWM frequency is $f_{\mathrm{PWM}} = 1$ kHz, and the maximum relative peak-to-peak current ripple is $\Delta i_{\mathrm{b,r,rel}} = 0.1$.

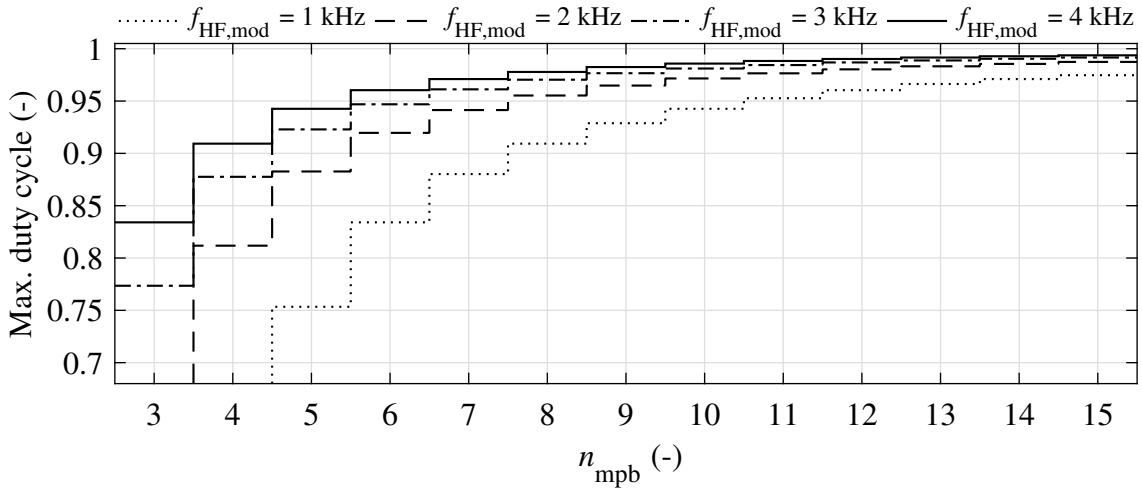


Figure 4.5: Maximum achievable duty cycle $\delta_{\max}$ versus the number of installed modules per branch n_{mpb} for various mean HF-modulation frequencies per module. The maximum allowed relative compensating current value is $I_{\mathrm{b,c,rel}} = 0.5$, the PWM frequency is $f_{\mathrm{PWM}} = 1$ kHz, and the maximum relative peak-to-peak current ripple is $\Delta i_{\mathrm{b,r,rel}} = 0.1$.

In practical applications, the mean switching frequency per module

$$f_{\mathrm{HF,mod}} = \frac{1}{2} \cdot \frac{f_{\mathrm{HF}}}{n_{\mathrm{mpb}}} \quad , \tag{4.25}$$

rather than the HF-modulation frequency itself, is often more limiting for the design. Since the mean value of the duty cycle is usually zero over an output period, the HF modulation is applied to both of the branches for approximately one half of the time. Hence, a factor of $\frac{1}{2}$ is introduced in the definition (4.25).

Using this definition, (4.23) can be transformed into:

$$\delta_{\max} \approx 1 - \frac{1}{8} \cdot \frac{\left(1 + \frac{I_{\mathrm{b,c,rel}}}{\frac{1+\delta_{\max}}{2}}\right)^2}{I_{\mathrm{b,c,rel}} \cdot \Delta i_{\mathrm{b,r,rel}}} \cdot \frac{1}{n_{\mathrm{mpb}}^2} \cdot \frac{f_{\mathrm{PWM}}}{f_{\mathrm{HF,mod}}} \quad . \tag{4.26}$$

As the equation shows, the dependence of the duty cycle on the number of installed modules is even stronger when the HF modulation frequency per module is used as the limiting factor instead of the HF modulation frequency. This statement is further supported by Figure 4.5, showing the dependence of the maximum duty cycle on the installed number of modules per branch for various mean values of HF-modulation frequencies per module.

The investigated design trade-offs can be summarized as follows:

- There is always a trade-off between the maximum achievable duty cycle, the maximum compensating current (and consequently the maximum branch current), and the HF modulation frequency.
- The value of the maximum compensating current should not be selected to be above approximately 60 % of the maximum output current value, since it provides only minor advantages above this point. Moreover, for values above 100 % of the maximum output current, the maximum compensating current even decreases the maximum achievable duty cycle.
- A higher number of modules per branch is generally advantageous for all investigated design indicators. As a rule of thumb, the number of modules per branch should not be below five. (A design of MMC with four modules per branch might also be conceivable as long as relatively high HF frequency is allowed.)

5 Control Implementation

As described in Chapter 3, quasi-two-level PWM operation can be implemented for each phase leg independently. The proposed control, described in this chapter, is derived for implementation in an FPGA (or an ASIC) with fast branch-current measurements. The main idea is that the MMC's phase leg should appear as a phase leg of a two-level inverter to the high-level control system (DSP or micro-controller) for a simpler integration into existing systems. In such applications, the DSP or the micro-controller provide the higher-level control (e.g. of the machine currents and the machine's speed) and the only value sent to the converter is the duty-cycle setpoint value δ^* for each phase leg. The internal MMC control implemented in the FPGA can provide the necessary measured values to the control system, such as output currents (calculated from branch currents) and input voltage. An overview of the control system is depicted in Figure 5.1.

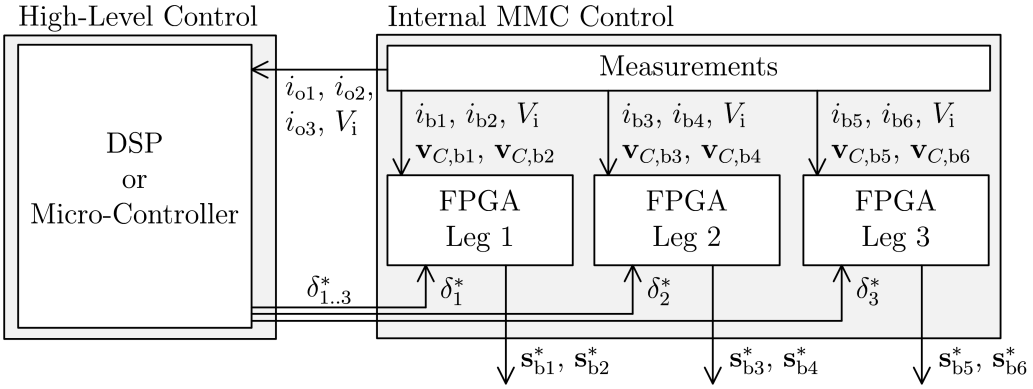


Figure 5.1: Control system overview for quasi-two-level PWM-operated MMCs (example for three phase legs). The variables are labeled according to defintions for three-phase MMCs defined in Chapter 2.

The control scheme for a single quasi-two-level PWM operated MMC leg is displayed in Figure 5.2. The inputs are the setpoint duty-cycle value δ^*, the measured input voltage V_i, the measured branch currents i_{bA} and i_{bB}, the output current i_o calculated from measured branch currents, and the vectors with measured module-capacitor voltages $\mathbf{v}_{C,bA}$ and $\mathbf{v}_{C,bB}$. The module-capacitor voltages are further used to calculate the actual mean values of capacitor voltages

$$\overline{v}_{C,bx} = \frac{1}{n_{mpb}} \cdot \sum_{n=1}^{n_{mpb}} \mathbf{v}_{C,bx,n} \quad , \quad x \in \{A,B\} \tag{5.1}$$

and the branch energies

$$e_{bx} = \frac{1}{2} \cdot C_{mod} \cdot \sum_{n=1}^{n_{mpb}} \mathbf{v}^2_{C,bx,n} \quad , \quad x \in \{A,B\} \quad , \tag{5.2}$$

where n represents the position of the module-capacitor voltage in the corresponding module-capacitor voltage vector. The outputs of the control scheme are the setpoint switching vectors $\mathbf{s}^*_{\mathrm{bA}}$ and $\mathbf{s}^*_{\mathrm{bB}}$, which determine the switching state of each module within the corresponding branch.

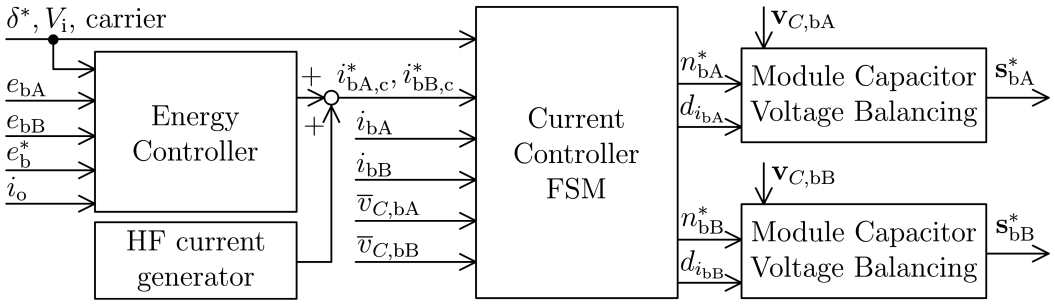


Figure 5.2: Internal MMC control for a single phase leg.

The control scheme in Figure 5.2 consists of module-capacitor voltage balancing units, two closed control loops, and a high-frequency (HF) current generator. The outer control loop is the energy control, which determines the setpoint values for compensating currents $i^*_{\mathrm{bA,c}}$ and $i^*_{\mathrm{bB,c}}$ in order to maintain the branch energies e_{bA} and e_{bB} at their setpoint value e^*_b. The inner control loop is the leg-current control, which adjusts the branch current i_{bA} (i_{bB}) to the value of the corresponding compensating current $i^*_{\mathrm{bA,c}}$ ($i^*_{\mathrm{bB,c}}$) during `STATE A` (`STATE B`). The current control is only one part of a large finite-state machine (FSM), which switches between the particular states and consequently generates the PWM-modulated output voltage waveform. The FSM determines the setpoint numbers of inserted modules n^*_{bA} and n^*_{bB} and the estimated directions of branch currents $d_{i_{\mathrm{bA}}}$ and $d_{i_{\mathrm{bB}}}$ for each point in time. These data are further used in module-capacitor voltage balancing units to determine which modules should be inserted and which short-circuited, in order to keep the module-capacitor voltages within the branch balanced. Furthermore, these units ensure that a minimum period of time T_d is inserted between every two switching instants to limit the $\mathrm{d}v/\mathrm{d}t$. The HF current generator adds additional alternating high-frequency current setpoints to the compensating current setpoint to improve the quality of module-capacitor voltage balancing within a branch. This unit is optional and does not impact the branch-energy control. The details of this unit and its particular purpose will be explained later in Section 5.4.

The carrier signal is a simple triangle waveform, as typically used for two-level PWM. The waveform is generated in the individual FPGAs and must be synchronized between the legs in order to not diminish the output-voltage waveform's quality. The triangle function can also be dynamically inverted to improve the energy control with flat-top modulation (studied later in Section 7.1). While the inversion does not have an influence on the implemented current control, it influences the spread of branch-power peaks between the branches and thus the predictive branch-energy control is derived for both non-inverted and inverted triangle carriers.

In the following sections, the control is explained in detail from the bottom to the top, starting with the module-capacitor voltage-balancing units. At the end of the chapter, the high-level control used for validation is briefly explained.

5.1 Module-Capacitor Voltage Balancing Within a Single Branch

The module-capacitor voltage balancing unit has two tasks. The first task is to choose which modules should be inserted or short-circuited (removed) to maintain the setpoint value for the sum of inserted modules n_{b}^{*}, while keeping the module capacitor voltages of each branch balanced. This task practically corresponds to the second step of the two-step modulation approaches for modular multilevel converters described in Section 2.2.2. The second task is to assure the minimum delay time between the switching instants in order to limit the output voltage's $\mathrm{d}v/\mathrm{d}t$.

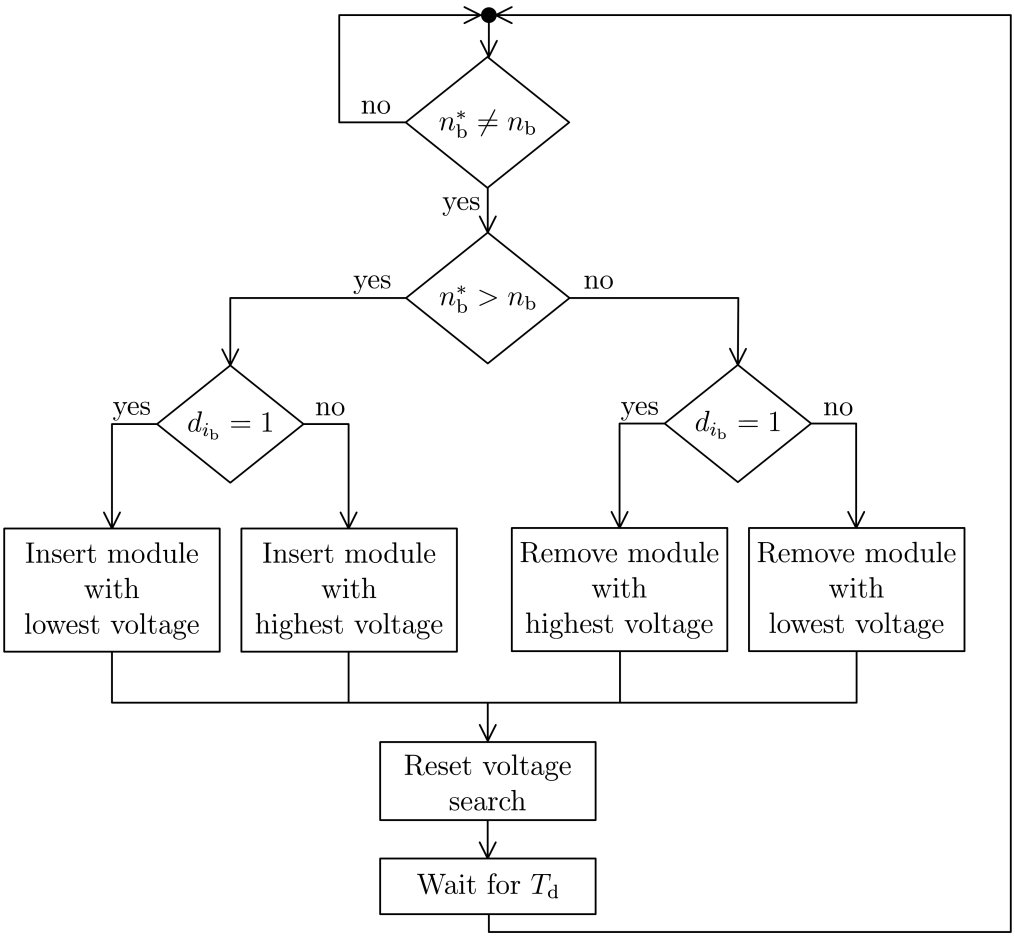


Figure 5.3: Principle of module-capacitor voltage balancing.

In Figure 5.3, the module-capacitor voltage balancing scheme is shown. In the first step, the number of inserted modules n_{b} is compared to the corresponding setpoint value n_{b}^{*}. The process waits until these two values differ. If the setpoint value is higher than the actual value, one additional module must be inserted. If the setpoint value is lower, one module must be removed (short-circuited). The particular module to be inserted or removed is selected according to the estimated branch-current direction $d_{i_{\mathrm{b}}}$. If the current is estimated to be positive $d_{i_{\mathrm{b}}} = 1$ (the inserted capacitors are charged), the inserted module with the highest voltage is removed and the short-circuited module with the lowest voltage is inserted. Conversely, if the estimated current is negative (the inserted capacitors are discharged), the inserted module with the lowest voltage

is removed and the short-circuited module with the highest voltage is inserted.

Afterwards, the search for maximum and minimum voltages of inserted and removed modules is reset and a delay period of time elapses before the process begins again.

As can be deducted from the control scheme in Figure 5.3, four modules have to be identified:

- the inserted module with the highest capacitor voltage,
- the inserted module with the lowest capacitor voltage,
- the short-circuited module with the highest capacitor voltage, and
- the short-circuited module with the lowest capacitor voltage.

Since the minimum delay time T_d between two switching instants is typically significantly longer than the FPGA's clock period, even a relatively slow and resource-saving algorithm can be used. In the applied implementation, the modules are identified by comparing the currently stored minimum and maximum values to the values of one module at each FPGA's clock period. Each period, a different module from the branch is compared, requiring only one comparing register fed by a pipelined multiplexer.

5.2 Current Control

The current control is based on a finite-state machine (FSM), depicted in Figure 5.4. For the majority of the time, the FSM is in `STATE A` or `STATE B` in order to generate the PWM-modulated output voltage. During `STATE A`, the branch voltage of Branch A v_bA is high and the branch energy e_bA is controlled by the compensating current $i_\mathrm{bA,c}$. The branch B carries the majority of the output current during this state. During `STATE B`, the branch voltage of Branch B v_bB is high and the branch energy e_bB is controlled by the compensating current $i_\mathrm{bB,c}$. During both, `STATE A` and `STATE B`, dead-beat control is utilized to adjust the leg-current value in order to achieve the desired branch-current setpoint – the compensating current setpoint values $i^*_\mathrm{bA,c}$ and $i^*_\mathrm{bB,c}$.

A transition between these two states is initiated by PWM when the carrier function c crosses the duty-cycle setpoint value δ^*. Since the leg current has a significantly different setpoint value during `STATE A` than during `STATE B`, a `TRANSITION STATE` is applied between these states to change the leg current as fast as possible [see Section 3.2].

As depicted in Figure 5.4, `TRANSITION STATE` can be initiated either from `STATE A` (`TRANSITION A→B`), or from `STATE B` (`TRANSITION B→A`). The transition states are further distinguished dependent on whether it is desired that the leg current is increased "$\mathrm{d}i^*_\mathrm{leg}/\mathrm{d}t > 0$" or decreased "$\mathrm{d}i^*_\mathrm{leg}/\mathrm{d}t < 0$".

During `TRANSITION STATE`, a predictive control is employed to control the leg current. Because of the minimum time delays T_d applied between two module switching instants, the branch voltages cannot instantaneously follow their setpoint values. Consequently, the leg current changes even after the `TRANSITION STATE` ends, and thus cannot be easily controlled. As a solution, the control applied during `TRANSITION STATE` does not use the measured value of the branch current i_bA or i_bB, but rather the corresponding predicted value $\tilde{i}_\mathrm{bA}$ or $\tilde{i}_\mathrm{bB}$ for the moment after the staircase rising (or falling) edge is over. The process of waiting

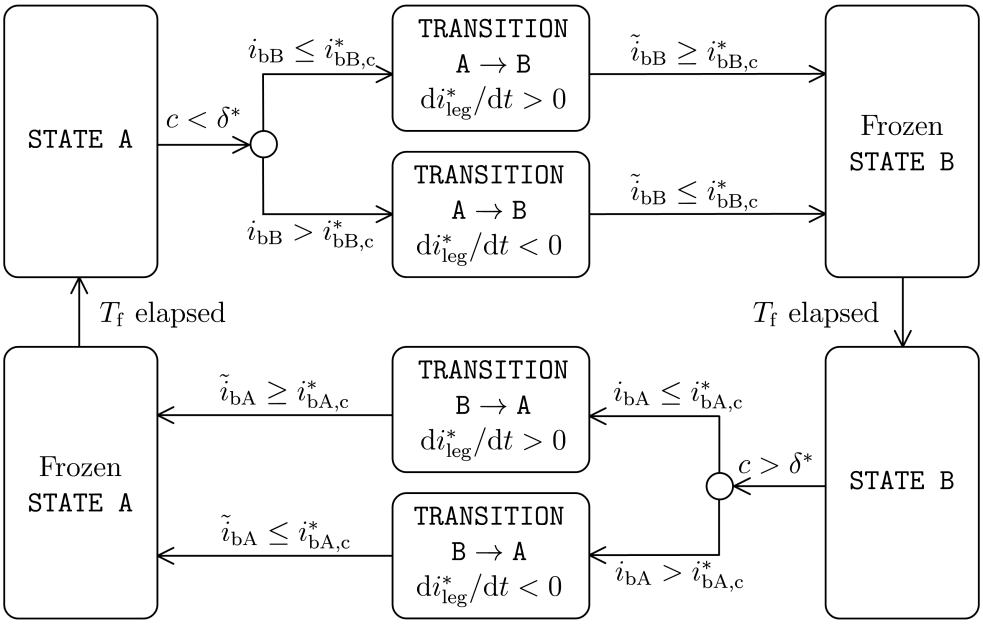


Figure 5.4: Current control FSM.

until the rising and falling edges of branch voltages are over is labeled as Frozen `STATE A` and Frozen `STATE B`, in which the currents are not actively controlled. Only after a sufficient period of time T_{f} has elapsed is `STATE A` or `STATE B` activated. The predictive control and the necessity of the frozen states are explained in more detail in the next section.

As mentioned above, the current control is based on adjusting the leg current – either predictively or by a dead-beat controller. Thus, it is important to describe the dynamic behavior of this current. This can be done by the following equation for the phase-leg model, derived in Section 3.1:

$$V_{\mathrm{i}} - v_{\mathrm{bA}} - v_{\mathrm{bB}} = 2 \cdot R_{\mathrm{b}} \cdot i_{\mathrm{leg}} + L_{\mathrm{leg}} \cdot \frac{\mathrm{d}i_{\mathrm{leg}}}{\mathrm{d}t} \quad . \tag{5.3}$$

In the following sections, the control during `TRANSITION STATE`, frozen states, `STATE A` and `STATE B` is derived and explained.

5.2.1 Transition States and Frozen States

As the FSM in Figure 5.4 shows, there are four different transition states. An overview of these is displayed in Figure 5.5.

If `TRANSITION A→B` is activated, the leg current must be changed so that the branch current i_{bB} reaches the setpoint value of the corresponding compensating current $i^*_{\mathrm{bB,c}}$. With `TRANSITION B→A`, the branch current i_{bA} is controlled to fit the setpoint value $i^*_{\mathrm{bA,c}}$. If the controlled branch current is higher than the corresponding setpoint value, the leg current must be decreased ($\mathrm{d}i^*_{\mathrm{leg}}/\mathrm{d}t < 0$). Consequently, both branch voltages are maximized by inserting all modules of both branches. This leads to the setpoint numbers of inserted modules

$$\begin{bmatrix} n^*_{\mathrm{bA}} \\ n^*_{\mathrm{bB}} \end{bmatrix} = \begin{bmatrix} n_{\mathrm{mpb}} \\ n_{\mathrm{mpb}} \end{bmatrix} \tag{5.4}$$

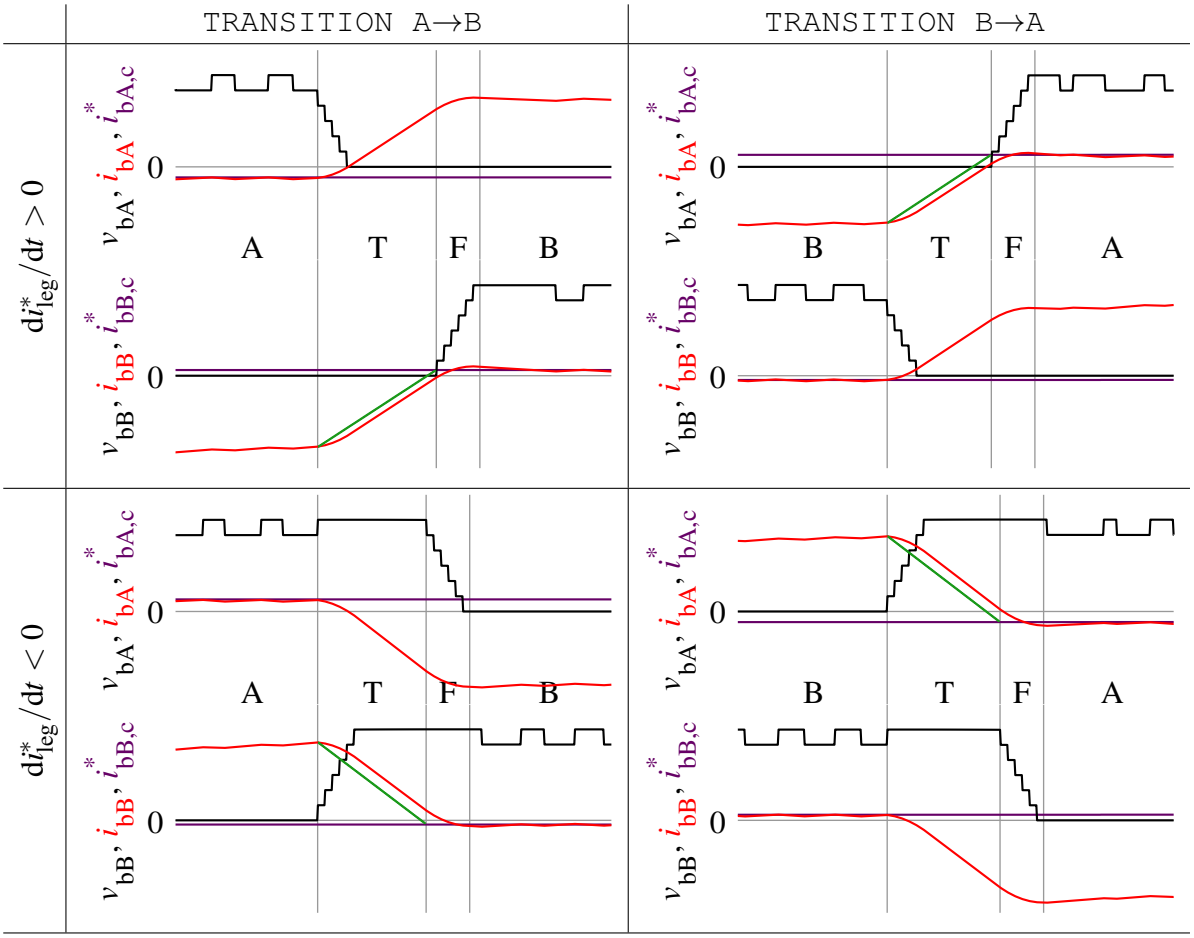


Figure 5.5: Overview of possible transition states. The branch voltages are plotted in black. The branch currents are red. The setpoint compensating currents are violet. The estimated branch current during the `TRANSITION STATE` is green. `STATE A` is marked with "A", `STATE B` with "B", `TRANSITION STATE` with "T" and frozen states with "F".

being equal to the number of installed modules per branch n_{mpb}. If the corresponding branch current must be increased ($\mathrm{d}i^*_{\mathrm{leg}}/\mathrm{d}t > 0$), both branches are short-circuited and the setpoint numbers of modules

$$\begin{bmatrix} n^*_{\mathrm{bA}} \\ n^*_{\mathrm{bB}} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{5.5}$$

are both zero. These setpoint numbers of inserted modules are then held for as long as necessary to achieve the setpoint value.

However, it is difficult to determine how long the necessary time period is, since the leg current changes even after `TRANSITION STATE` ends [see Figure 5.5]. This is caused by the fact that the number of inserted modules n_{bA} and n_{bB} cannot instantaneously follow the corresponding setpoint numbers n^*_{bA} and n^*_{bB}, as the minimum period of time T_{d} is assured between each two switching instants in the module-capacitor voltage balancing units [see Section 5.1]. Consequently, the additional component of the branch current that is generated after the end of the `TRANSITION STATE` has to be predicted and added to the actual value, leading to the estimated branch current $\tilde{i}_{\mathrm{bA}}$ or $\tilde{i}_{\mathrm{bB}}$. This estimated branch current is then compared to the corresponding setpoint value of the compensating current in order to determine the end

of TRANSITION STATE [see the FSM in Figure 5.4]. After TRANSITION STATE ends, frozen STATE A ($n^*_{\mathrm{bA}} = n_{\mathrm{mpb}}, n^*_{\mathrm{bB}} = 0$) or frozen STATE B ($n^*_{\mathrm{bA}} = 0, n^*_{\mathrm{bB}} = n_{\mathrm{mpb}}$) are initiated for a period of time

$$T_{\mathrm{f}} = T_{\mathrm{d}} \cdot n_{\mathrm{mpb}} \tag{5.6}$$

to let the branch current achieve its predicted value. Once the frozen state is finished, STATE A or STATE B is activated.

For practical implementation, it is advantageous to predict the complete branch current during the whole TRANSITION STATE instead of adding the predicted part to the measured value. This way, the predictive control behaves as an open-loop controller and it is not necessary to measure the branch current precisely while it is being changed quickly. Moreover, if this kind of prediction is applied and the branch resistance is assumed to be very low $R_{\mathrm{b}} \approx 0$, the value can be estimated using n^*_{bA} and n^*_{bB}, as if the delay period T_{d} was zero. This is because the missing time-voltage area, which is missing due to the staircase form of voltage, in one branch is equal to the additional time-voltage area in the other branch [see Figure 5.5]. Since the duration of TRANSITION STATE is very short, it can be assumed that the output current does not change during this period. Consequently, the estimated branch currents in the next time step $k+1$

$$\begin{bmatrix} \tilde{i}_{\mathrm{bA}}(k+1) \\ \tilde{i}_{\mathrm{bB}}(k+1) \end{bmatrix} = \begin{bmatrix} \tilde{i}_{\mathrm{bA}}(k) \\ \tilde{i}_{\mathrm{bB}}(k) \end{bmatrix} + \Delta\tilde{i}_{\mathrm{leg}}(k) \tag{5.7}$$

can be calculated by the values in the previous step and the estimated change of leg current $\Delta\tilde{i}_{\mathrm{leg}}$, with $\tilde{i}_{\mathrm{bA}}(0)$ and $\tilde{i}_{\mathrm{bB}}(0)$ being the measured branch current values right before the transition state started.

The estimated change of leg current

$$\Delta\tilde{i}_{\mathrm{leg}}(k) = \frac{T_{\mathrm{p}}}{L_{\mathrm{leg}}} \cdot \left(V_{\mathrm{i}}(k) - v_{\mathrm{bA}}(k) - v_{\mathrm{bB}}(k)\right) \tag{5.8}$$

can be calculated in time step k by discretizing (5.3) with a time period T_{p}, referred to as a prediction period, and assuming $R_{\mathrm{b}} \approx 0$[1)]. The leg inductance L_{leg} is known and the input voltage value $V_{\mathrm{i}}(k)$ is obtained through measurement. The branch voltages

$$\begin{bmatrix} v_{\mathrm{bA}}(k) \\ v_{\mathrm{bB}}(k) \end{bmatrix} = \begin{bmatrix} n^*_{\mathrm{bA}}(k) \cdot \overline{v}_{C,\mathrm{bA}}(k) \\ n^*_{\mathrm{bB}}(k) \cdot \overline{v}_{C,\mathrm{bB}}(k) \end{bmatrix} \tag{5.9}$$

are calculated by multiplying the setpoint numbers of inserted modules with the mean value of measured module-capacitor voltages of a branch.

Note that in practical implementation, the prediction period T_{p} is not selected to be identical to the FPGA clock period. If the prediction period is set too short, either many bits are required in the integer based calculations, or the numeric precision is low.

[1)] The error caused by this simplification is very low because the leg current is changed from approximately $\pm i_{\mathrm{o}}/2$ to approximately $\mp i_{\mathrm{o}}/2$. Consequently, the mean value of the leg current during TRANSITION STATE is approximately zero, and so is the mean value of the voltage drop over the branch resistances.

5.2.2 State A and State B

During `STATE A` and `STATE B`, the leg current is controlled by a dead-beat controller. To derive this, (5.3) is transformed into the following form:

$$v_{\mathrm{bA}} + v_{\mathrm{bB}} = V_{\mathrm{i}} - 2 \cdot R_{\mathrm{b}} \cdot i_{\mathrm{leg}} + L_{\mathrm{leg}} \cdot \frac{\mathrm{d}i_{\mathrm{leg}}}{\mathrm{d}t} \quad . \tag{5.10}$$

Assuming the dead-beat period is $1/f_{\mathrm{HF}}$, the time constant $L_{\mathrm{leg}}/(2R_{\mathrm{b}})$ is significantly longer than the dead-beat period, and that the leg current achieves its setpoint i^*_{leg} at the end of the time period, the equation can be approximated as follows:

$$v^*_{\mathrm{bA}} + v^*_{\mathrm{bB}} = V_{\mathrm{i}} - 2 \cdot R_{\mathrm{b}} \cdot \frac{i^*_{\mathrm{leg}} + i_{\mathrm{leg}}}{2} + L_{\mathrm{leg}} \cdot f_{\mathrm{HF}} \cdot \left(i^*_{\mathrm{leg}} - i_{\mathrm{leg}} \right) \quad , \tag{5.11}$$

with v^*_{bA} and v^*_{bB} being the setpoint voltages during the dead-beat period.

During `STATE A`, the branch voltage v_{bB} is zero:

$$v^*_{\mathrm{bB}} = 0, \tag{5.12}$$

and so is the corresponding setpoint number of inserted modules: $n^*_{\mathrm{bB}} = 0$. Since the branch current i_{bA} is controlled to fit the setpoint value $i^*_{\mathrm{bA,c}}$, the desired change in the leg current is as high as the desired change in branch current A:

$$i^*_{\mathrm{leg}} - i_{\mathrm{leg}} = i^*_{\mathrm{bA,c}} - i_{\mathrm{bA}} \quad . \tag{5.13}$$

The mean value of the leg current can be reshaped as follows:

$$\frac{i^*_{\mathrm{leg}} + i_{\mathrm{leg}}}{2} = \frac{\left(i^*_{\mathrm{leg}} - i_{\mathrm{leg}} \right) + 2 \cdot i_{\mathrm{leg}}}{2} \quad . \tag{5.14}$$

Substituting (5.13) and the leg current definition

$$i_{\mathrm{leg}} = \frac{1}{2} \cdot (i_{\mathrm{bA}} + i_{\mathrm{bB}}) \tag{5.15}$$

into (5.14), the following form can be obtained:

$$\frac{i^*_{\mathrm{leg}} + i_{\mathrm{leg}}}{2} = \frac{i^*_{\mathrm{bA,c}} + i_{\mathrm{bB}}}{2} \quad . \tag{5.16}$$

Finally, by substituting (5.12), (5.13) and (5.16) into (5.11), the calculation of the dead-beat controller

$$v^*_{\mathrm{bA}} = V_{\mathrm{i}} - 2 \cdot R_{\mathrm{b}} \cdot \frac{1}{2} \cdot (i^*_{\mathrm{bA,c}} + i_{\mathrm{bB}}) + L_{\mathrm{leg}} \cdot f_{\mathrm{HF}} \cdot (i^*_{\mathrm{bA}} - i_{\mathrm{bA}}) \tag{5.17}$$

during `STATE A` can be derived. The values i_{bA}, i_{bB}, and V_{i} are measured. While the leg inductance value L_{leg} is known and can simply be measured during converter design, the branch resistance R_{b} also depends on the current semiconductor state. This value can be roughly estimated during the converter design. When IGBTs are used in the modules, their

non-linear voltage-current characteristic can either be linearized, leading to a constant resistor approximation, or a non-linear resistance-current characteristic can be saved into a look-up table and estimated depending on the actual branch current value. The influence of the branch resistance estimation error is further studied in Section 6.5.

Analogously, the voltage v^*_{bA} is zero during `STATE B` ($n^*_{\mathrm{bA}} = 0$), and the dead-beat controller is executed by Branch B:

$$v^*_{\mathrm{bB}} = V_{\mathrm{i}} - 2 \cdot R_{\mathrm{b}} \cdot \frac{1}{2} \cdot (i^*_{\mathrm{bB,c}} + i_{\mathrm{bA}}) + L_{\mathrm{leg}} \cdot f_{\mathrm{HF}} \cdot (i^*_{\mathrm{bB}} - i_{\mathrm{bB}}) \quad . \tag{5.18}$$

The resulting branch voltages v^*_{bA} and v^*_{bB} are synthesized using HF modulation, which determines n^*_{bA} and n^*_{bB}. As mentioned in Section 3.2, the HF modulation is based on a dedicated PWM algorithm typical for two-step modulation approaches of MMCs, explained in e.g. [56]. The principle of this algorithm is demonstrated by the top graph of Figure 2.6. The application of the HF modulation is visible before and after the `TRANSITION STATE` in Figure 5.5. The HF-modulation carrier is synchronized at the beginning of `STATE A` or `STATE B`. The branch voltage setpoint values v^*_{bA} and v^*_{bB} are sampled with HF modulation frequency each time the HF-modulation carrier reaches zero.

5.2.3 Estimation of Branch Current's Direction

The directions of branch current A $d_{i_{\mathrm{bA}}}$ and of branch current B $d_{i_{\mathrm{bB}}}$, required for module voltage balancing, are estimated dependent on the actual FSM state. An overview of the estimation is shown in Table 5.1.

Table 5.1: Estimation of branch currents' direction in dependence on the actual state.

State	$d_{i_{\mathrm{bA}}}$	$d_{i_{\mathrm{bB}}}$
`STATE A`	$\mathrm{sign}(i^*_{\mathrm{bA,c}})$	-
`STATE B`	-	$\mathrm{sign}(i^*_{\mathrm{bB,c}})$
`TRANSITION A→B` "$\mathrm{d}i^*_{\mathrm{leg}}/\mathrm{d}t > 0$" + Frozen `STATE B`	$\mathrm{sign}(i_{\mathrm{bA}})$	$\mathrm{sign}(i^*_{\mathrm{bB,c}})$
`TRANSITION A→B` "$\mathrm{d}i^*_{\mathrm{leg}}/\mathrm{d}t < 0$" + Frozen `STATE B`	$\mathrm{sign}(i^*_{\mathrm{bB,c}} + i_{\mathrm{o}})$	$\mathrm{sign}(i_{\mathrm{bB}})$
`TRANSITION B→A` "$\mathrm{d}i^*_{\mathrm{leg}}/\mathrm{d}t > 0$" + Frozen `STATE A`	$\mathrm{sign}(i^*_{\mathrm{bA,c}})$	$\mathrm{sign}(i_{\mathrm{bB}})$
`TRANSITION B→A` "$\mathrm{d}i^*_{\mathrm{leg}}/\mathrm{d}t < 0$" + Frozen `STATE A`	$\mathrm{sign}(i_{\mathrm{bA}})$	$\mathrm{sign}(i^*_{\mathrm{bA,c}} - i_{\mathrm{o}})$

During `STATE A` and `STATE B`, the setpoint values of the corresponding currents are used for the estimation, as the measured values are distorted by the current ripple. When the current ripple is higher than the current setpoint value, the sign of the mean current during the HF-modulation

period could be determined incorrectly, leading to unbalanced capacitor voltages. The direction of the branch current B does not matter during `STATE A`, since all modules are short-circuited. Similarly, the direction of the branch current A does not matter during `STATE B`.

The current direction during Frozen `STATE A` and Frozen `STATE B` is determined according to the `TRANSITION STATE`, which was activated previously. The estimation of current direction for the branch, the voltage of which is changed first during `TRANSITION STATE`, is based on the measured values. The direction of the other branch, changed during frozen state, is estimated using the setpoint value of the compensating current and an actual value of the output current. Although the measured values could also have been used, a use of setpoint values is advantageous for the cases when the current changes the direction shortly after a module switching instant. Such a case can be seen in Figure 5.5 for `TRANSITION A→B` and $\mathrm{d}i^*_{\mathrm{leg}}/\mathrm{d}t > 0$. As the figure shows, when the first module is switched on, the measured current is slightly negative. Consequently, the module with the highest capacitor voltage would have been inserted if the current sign had been determined using the measured values. However, since the current direction changes shortly after the module is switched, the module with the highest voltage would be charged the longest, diminishing the quality of balancing. If the setpoint current values are used instead of measured values, these cases do not occur.

5.3 Branch-Energy Control

There are two options for the branch-energy control presented in this thesis. The first one is based on a fast proportional closed-loop control, in which the setpoints for the compensating currents are calculated continuously. The second is based on the prediction of the energy disturbance caused by the power peaks, a method which changes the compensating current setpoints only once per PWM period.

5.3.1 Fast Proportional Branch-Energy Control

The fast proportional energy control employs two proportional controllers to continuously generate the branch power setpoints for each branch. The outputs of the controllers are the setpoint branch powers p^*_{bA} and p^*_{bB}, which are supposed to be set by the compensating currents over a PWM period.

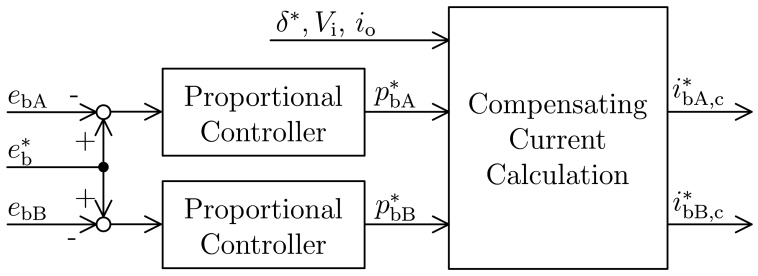


Figure 5.6: Branch-energy control based on fast proportional controllers.

However, the setpoint compensating currents are not applied during the whole PWM period, but only during `STATE A` and `STATE B`. Consequently, the values of setpoint compensating

currents

$$i^*_{\mathrm{bA,c}} = \frac{p^*_{\mathrm{bA}}}{V_\mathrm{i}} \cdot \frac{1}{\frac{T_{\mathrm{bA,c}}}{T_{\mathrm{PWM}}}}$$
$$i^*_{\mathrm{bB,c}} = \frac{p^*_{\mathrm{bB}}}{V_\mathrm{i}} \cdot \frac{1}{\frac{T_{\mathrm{bB,c}}}{T_{\mathrm{PWM}}}} \tag{5.19}$$

are calculated using the branch-power setpoints p^*_{bA} and p^*_{bB}, the measured input voltage V_i, and the relative part of the PWM period, in which the compensating currents of the corresponding branch are active. This relative period can be calculated by a division of the time available for the compensation in the corresponding branch $T_{\mathrm{bA,c}}$ or $T_{\mathrm{bB,c}}$ by the length of PWM period T_{PWM}. The time periods for compensation

$$\begin{bmatrix} T_{\mathrm{bA,c}} \\ T_{\mathrm{bB,c}} \end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix} 1-\delta^* \\ 1+\delta^* \end{bmatrix} \cdot T_{\mathrm{PWM}} - T_\mathrm{T} \cdot \begin{bmatrix} 1 \\ 1 \end{bmatrix} \tag{5.20}$$

can be calculated by the setpoint duty cycle δ^*, the PWM period T_{PWM}, and a substraction of the time duration of `TRANSITION STATE` T_T.

Nevertheless, the calculation of the transition-state duration is rather complex [see Section 4.1]. Therefore, the time period

$$T_\mathrm{T} \approx \frac{L_{\mathrm{leg}} \cdot |i_\mathrm{o}|}{V_\mathrm{i}} \tag{5.21}$$

is approximated by the time necessary to change the leg current from $-i_\mathrm{o}/2$ to $i_\mathrm{o}/2$ with a value of input voltage, neglecting the time to reach the correct value of compensating currents.

Finally, the calculation of setpoints for the compensating currents, depicted in Figure 5.6, is based on the following expressions:

$$i^*_{\mathrm{bA,c}} = \frac{p^*_{\mathrm{bA}}}{V_\mathrm{i} \cdot \frac{1-\delta^*}{2} - f_{\mathrm{PWM}} \cdot L_{\mathrm{leg}} \cdot |i_\mathrm{o}|}$$
$$i^*_{\mathrm{bB,c}} = \frac{p^*_{\mathrm{bB}}}{V_\mathrm{i} \cdot \frac{1+\delta^*}{2} - f_{\mathrm{PWM}} \cdot L_{\mathrm{leg}} \cdot |i_\mathrm{o}|} \quad . \tag{5.22}$$

Since a division by a variable is undesired for implementation in an FPGA, the denominators of (5.22) can be calculated in the CPU once per PWM period and their inverse value is transferred to the FPGA with the setpoint duty cycle δ^*.

The gain $G_{\mathrm{P},e}$ of the proportional controller can be chosen by observing the closed-loop behavior of the controlled system. When the required leg current (and thus the power) is assumed to be controlled sufficiently fast and the converter losses are neglected, the controlled plant can be simplified to a single integrator:

$$e_{\mathrm{b}x} = \int p^*_{\mathrm{b}x}\, \mathrm{d}t, \quad x \in \{\mathrm{A},\mathrm{B}\} \quad . \tag{5.23}$$

The transfer function of the resulting closed-loop system

$$H(s) = \frac{1}{\frac{1}{G_{\mathrm{P},e}} \cdot s + 1} \tag{5.24}$$

represents a first-order lag element with a time constant $T = \frac{1}{G_{\mathrm{P},e}}$. By setting this time constant two times lower than the PWM period, approximately 86 % of the disturbance occurring at the beginning of the PWM period is compensated for at the end of the PWM period and the peak value of compensating current occurring at the beginning of the PWM period is approximately two times higher than its mean value during the PWM period. This yields the following relationship for the proportional gain:

$$G_{\mathrm{P},e} \approx 2 \cdot f_{\mathrm{PWM}} \quad . \tag{5.25}$$

If the proportional gain is set lower, the peak value of the compensating current is reduced but the remaining deviation of the module capacitor voltage from its setpoint value rises. Conversely, when set higher, the peak value of the compensating current rises and the control deviation is reduced.

In theory, an integral part could be added to the controller to reduce the remaining control deviation. However, this option was not implemented in this thesis, due to the difficult setup of the integral gain and of the anti-windup for the integrators because of the non-linear behavior of the converter.

5.3.2 Predictive Branch-Energy Control

The principle of predictive branch-energy control is very similar to that of fast proportional branch-energy control, with the main difference being that the energy disturbance is predicted and the proportional controller has to compensate for only a small mismatch in the prediction. Unlike the fast proportional branch-energy control algorithm, the predictive energy control updates the setpoints for compensating currents only once per PWM period, thus reducing the peak values of compensating currents. The implemented predictive controller can be viewed as a proportional controller with a feed-forward control which predicts the branch energy disturbances. However, the feed-forward part of the controller determining the compensating current for Branch B depends on the value of the compensating current for Branch A, and vice versa [see (4.8)]. Consequently, simplifications have to be derived and the controller values are computed by a sequential algorithm. The algorithm of the predictive branch-energy controller is explained using a flow chart displayed in Figure 5.7. Since the algorithm is implemented in an FPGA, the setpoints for compensating currents can be calculated continuously. The most recent values of the setpoints are sampled at the beginning of each PWM period.

The branch energy disturbance depends on many factors, such as setpoint duty cycle δ^*, the output current i_{o}, and whether the PWM carrier is inverted or not[2)]. All possible cases are demonstrated using examples with a simplified model in Figures 5.8 and 5.9. These two figures are the basis for the following considerations regarding the derivation of predictive branch-energy control.

[2)] The inverting of the PWM carrier is advantageous for flat-top modulation. More details are given in Section 7.1.

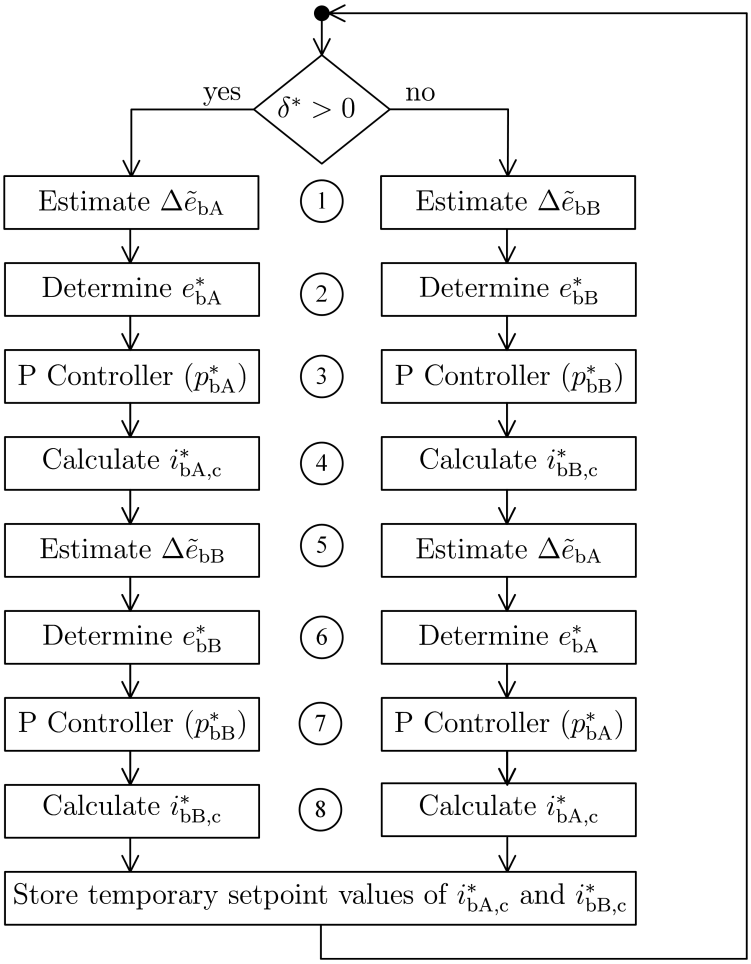


Figure 5.7: Flow chart of predictive energy controller.

An important part of predictive energy control is the estimation of the branch energy disturbance in Branch A $\Delta\tilde{e}_{\mathrm{bA}}$ and in Branch B $\Delta\tilde{e}_{\mathrm{bB}}$, caused by the power peaks during `TRANSITION STATE`. The estimated branch energy disturbances

$$\begin{bmatrix} |\Delta\tilde{e}_{\mathrm{bA}}| \\ |\Delta\tilde{e}_{\mathrm{bB}}| \end{bmatrix} = \frac{1}{2} \cdot L_{\mathrm{leg}} \cdot \begin{bmatrix} \left(|i_{\mathrm{o}}| + |i^*_{\mathrm{bB,c}}|\right)^2 \\ \left(|i_{\mathrm{o}}| + |i^*_{\mathrm{bA,c}}|\right)^2 \end{bmatrix} \tag{5.26}$$

can be calculated using (4.8), derived in Section 4.1.

However, calculation of the setpoint compensating currents is rather complex for an FPGA implementation [see (4.13)]. Thus, estimation of the branch energy disturbances is simplified. As can be observed in Figures 5.8 and 5.9, the compensating current $i_{\mathrm{bB,c}}$ is very low when $\delta^* > 0$. Therefore, the estimation can be simplified to

$$\begin{bmatrix} |\Delta\tilde{e}_{\mathrm{bA}}| \\ |\Delta\tilde{e}_{\mathrm{bB}}| \end{bmatrix} \approx \frac{1}{2} \cdot L_{\mathrm{leg}} \cdot \begin{bmatrix} |i_{\mathrm{o}}|^2 \\ \left(|i_{\mathrm{o}}| + |i^*_{\mathrm{bA,c}}|\right)^2 \end{bmatrix} \tag{5.27}$$

for positive duty-cycle setpoints. As a consequence, if $\delta^* > 0$, the branch energy disturbance $\Delta\tilde{e}_{\mathrm{bA}}$ and compensating current setpoint $i^*_{\mathrm{bA,c}}$ are first calculated for Branch A. The branch

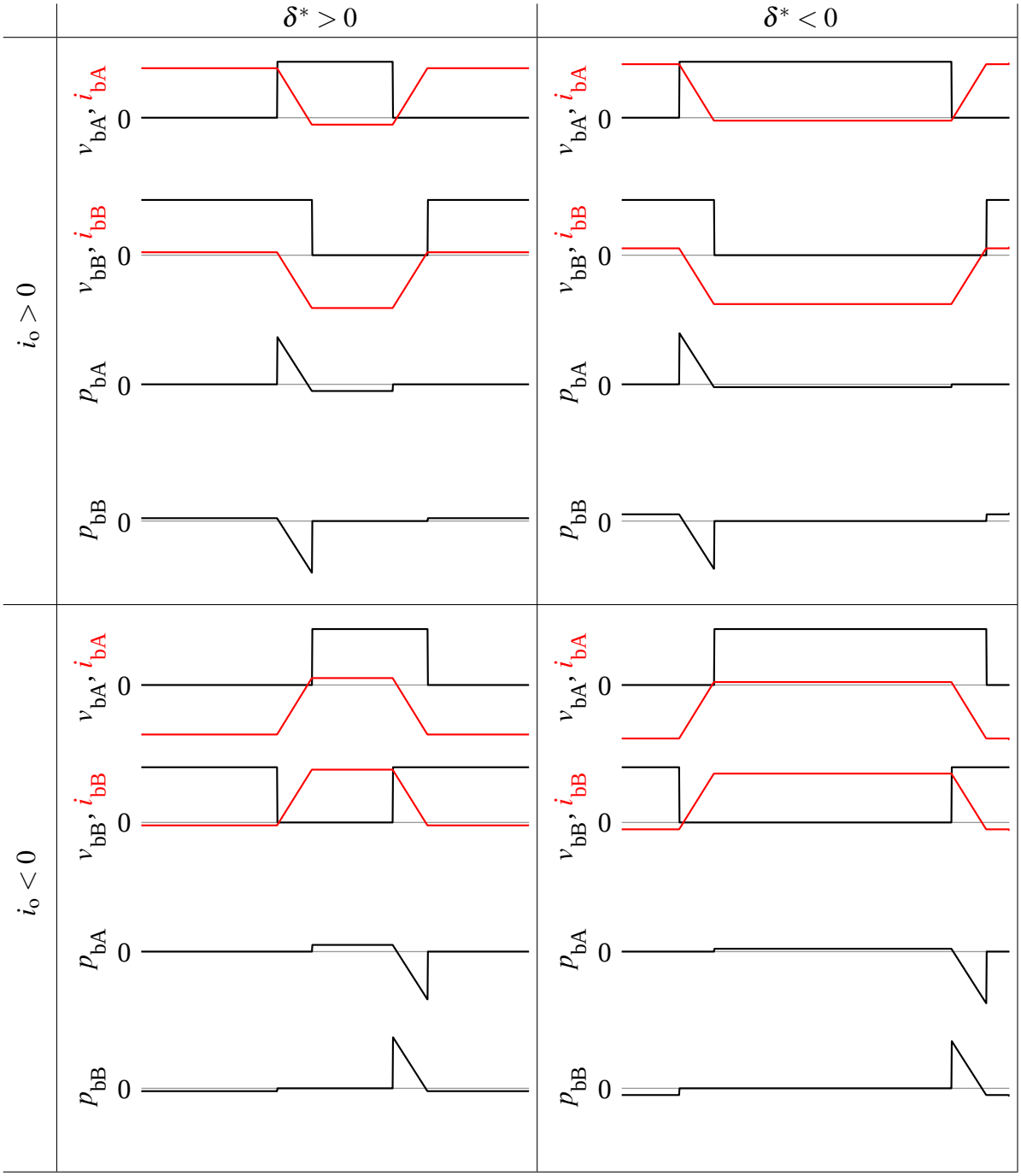


Figure 5.8: Overview of possible waveforms of branch currents, branch voltages, and branch powers, depending on the duty cycle sign and the output current sign. **The PWM carrier is non-inverted.**

energy disturbance of Branch B $\Delta\tilde{e}_{bB}$ is estimated subsequently according to (5.27), using the previously calculated compensating current value for Branch A. This sequence of the energy-disturbance calculation for the positive duty cycles can be observed in the flow chart in Figure 5.7.

Conversely, if $\delta^* \leq 0$, the values for Branch B are calculated first and then the branch energy

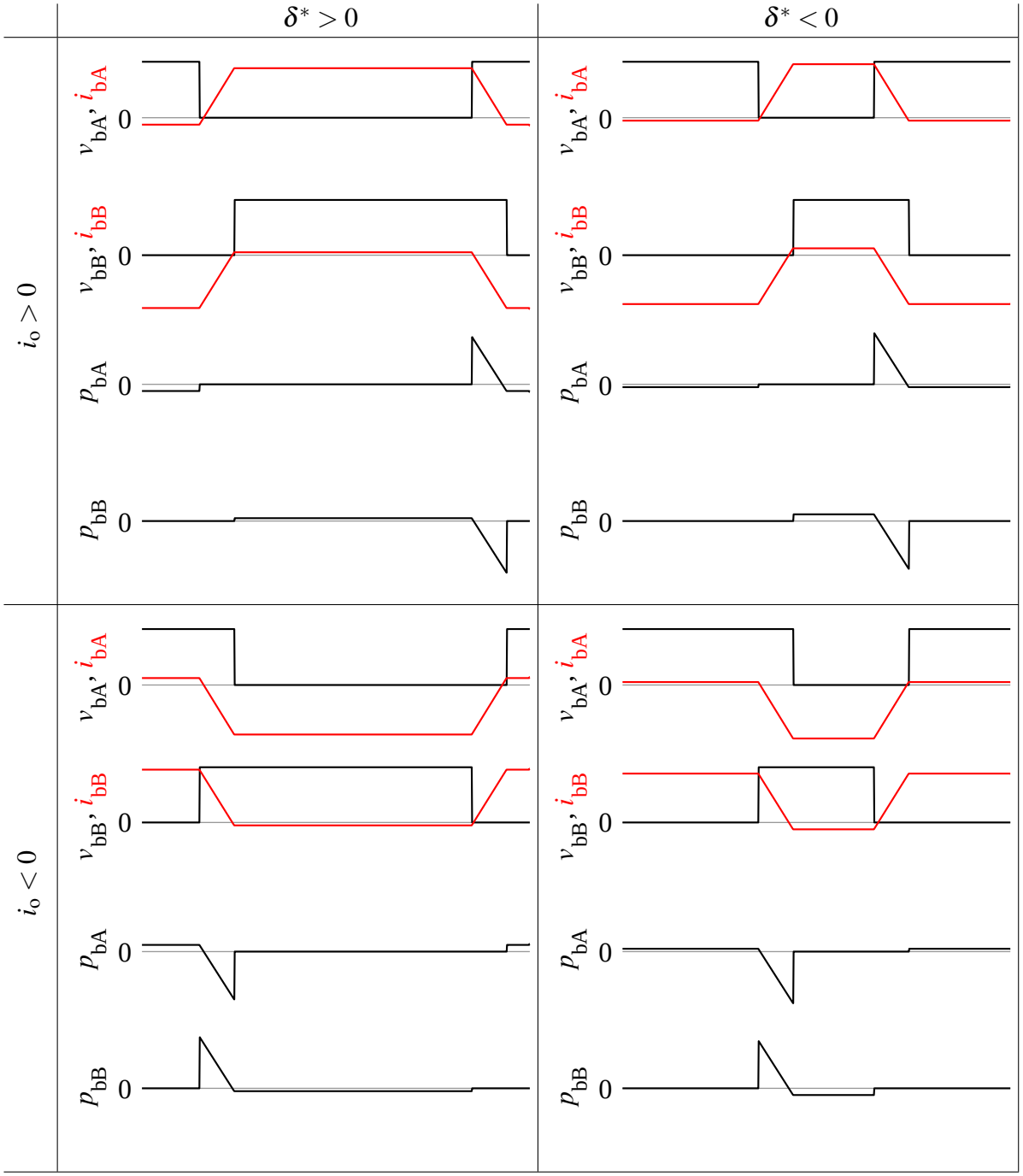


Figure 5.9: Overview of possible waveforms of branch currents, branch voltages, and branch powers, depending on the duty cycle sign and the output current sign. **The PWM carrier is inverted.**

disturbance of Branch A is estimated:

$$\begin{bmatrix} |\Delta\tilde{e}_{bA}| \\ |\Delta\tilde{e}_{bB}| \end{bmatrix} \approx \frac{1}{2} \cdot L_{leg} \cdot \begin{bmatrix} \left(|i_o| + |i^*_{bB,c}|\right)^2 \\ |i_o|^2 \end{bmatrix} \quad . \tag{5.28}$$

The branch-energy estimation error caused by the derived simplification is compensated for by the close-loop energy controller.

Next, each step of the predictive branch-energy controller described in Figure 5.7 is described.

The estimation of the branch energy disturbances (steps ① and ⑤ in Figure 5.7) for a particular duty cycle and an output current sign are summarized in Table 5.2. The absolute values in the table are in concordance with (5.27) for positive duty cycles and in concordance with (5.28) for negative duty cycles. The signs are determined using Figures 5.8 and 5.9.

After the branch energy disturbance is estimated, the branch energy setpoint value is adjusted according to Table 5.3 (steps ② and ⑥ in Figure 5.7). While in some cases the branch power waveform is positive-negative-positive or negative-positive-negative during a PWM period [e.g. branch power p_{bB} in Figure 5.8], in other cases, the branch power waveform is only positive-negative [e.g. branch power p_{bA} in Figure 5.8], leading to unipolar branch energy peaks. The distribution of this branch energy variation around the setpoint can be improved by dynamically changing the branch energy setpoint in the second group of cases.

Table 5.2: Estimation of the branch energy disturbance caused by the transition state.

		$\Delta\tilde{e}_{\mathrm{bA}}$	$\Delta\tilde{e}_{\mathrm{bB}}$
$\delta^* > 0$	$i_{\mathrm{o}} > 0$	$\frac{1}{2} \cdot L_{\mathrm{leg}} \cdot i_{\mathrm{o}}^2$	$-\frac{1}{2} \cdot L_{\mathrm{leg}} \cdot (-i_{\mathrm{o}} + i_{\mathrm{bA,c}}^*)^2$
	$i_{\mathrm{o}} \leq 0$	$-\frac{1}{2} \cdot L_{\mathrm{leg}} \cdot i_{\mathrm{o}}^2$	$\frac{1}{2} \cdot L_{\mathrm{leg}} \cdot (-i_{\mathrm{o}} + i_{\mathrm{bA,c}}^*)^2$
$\delta^* \leq 0$	$i_{\mathrm{o}} > 0$	$\frac{1}{2} \cdot L_{\mathrm{leg}} \cdot (i_{\mathrm{o}} + i_{\mathrm{bB,c}}^*)^2$	$-\frac{1}{2} \cdot L_{\mathrm{leg}} \cdot i_{\mathrm{o}}^2$
	$i_{\mathrm{o}} \leq 0$	$-\frac{1}{2} \cdot L_{\mathrm{leg}} \cdot (i_{\mathrm{o}} + i_{\mathrm{bB,c}}^*)^2$	$\frac{1}{2} \cdot L_{\mathrm{leg}} \cdot i_{\mathrm{o}}^2$

Table 5.3: Calculation of the branch energy setpoint values.

		e_{bA}^*	e_{bB}^*
Non-inverted	$i_{\mathrm{o}} > 0$	$e_{\mathrm{b}}^* - \frac{1}{2} \cdot \Delta\tilde{e}_{\mathrm{bA}}$	e_{b}^*
carrier	$i_{\mathrm{o}} \leq 0$	$e_{\mathrm{b}}^* + \frac{1}{2} \cdot \Delta\tilde{e}_{\mathrm{bA}}$	e_{b}^*
Inverted	$i_{\mathrm{o}} > 0$	e_{b}^*	$e_{\mathrm{b}}^* + \frac{1}{2} \cdot \Delta\tilde{e}_{\mathrm{bB}}$
carrier	$i_{\mathrm{o}} \leq 0$	e_{b}^*	$e_{\mathrm{b}}^* - \frac{1}{2} \cdot \Delta\tilde{e}_{\mathrm{bB}}$

Once the branch energy setpoint is assigned, the closed-loop proportional (P) controller can be calculated (steps ③ and ⑦ in Figure 5.7), correcting the imprecision of the energy disturbance prediction. The controller determines the mean value of the setpoint branch power for the next PWM period p_{bA}^* or p_{bB}^*.

Using this setpoint branch power and the branch energy disturbance, the setpoint value for compensating currents

$$
\begin{aligned}
i_{\mathrm{bA,c}}^* &= \frac{p_{\mathrm{bA}}^* - \Delta\tilde{e}_{\mathrm{bA}} \cdot f_{\mathrm{PWM}}}{V_{\mathrm{i}} \cdot \frac{1-\delta^*}{2} - f_{\mathrm{PWM}} \cdot L_{\mathrm{leg}} \cdot |i_{\mathrm{o}}|} \\
i_{\mathrm{bB,c}}^* &= \frac{p_{\mathrm{bB}}^* - \Delta\tilde{e}_{\mathrm{bB}} \cdot f_{\mathrm{PWM}}}{V_{\mathrm{i}} \cdot \frac{1+\delta^*}{2} - f_{\mathrm{PWM}} \cdot L_{\mathrm{leg}} \cdot |i_{\mathrm{o}}|}
\end{aligned}
\tag{5.29}
$$

can be calculated by a modification of (5.22). This can be seen as steps ④ and ⑧ in Figure 5.7.

In this case, the gain $G_{\mathrm{P},e}$ of the proportional controller could be designed as a dead-beat

controller by transforming (5.23) to a discrete form:

$$e_{\mathrm{b}x}(k+1) = T_{\mathrm{PWM}} \cdot p^*_{\mathrm{b}x}(k) + e_{\mathrm{b}x}(k), \quad x \in \{\mathrm{A},\mathrm{B}\} \quad . \tag{5.30}$$

This can be further transformed to express the branch power setpoint

$$p^*_{\mathrm{b}x} = f_{\mathrm{PWM}} \cdot \Delta e_{\mathrm{b}x}, \quad x \in \{\mathrm{A},\mathrm{B}\} \quad . \tag{5.31}$$

As can be seen in (5.31), the proportional gain could be set equal to the PWM frequency. However, since the branch power is not always set precisely and the converter losses are neglected in the predictive control, a slightly higher gain of the controller

$$G_{\mathrm{P},e} = (1.1..1.4) \cdot f_{\mathrm{PWM}} \tag{5.32}$$

is recommended to reduce the remaining control deviation from the module capacitor voltage setpoint. Note that the impact of increased gain on the steady-state behavior is relatively low, since the closed-loop control only eliminates the error in prediction of the branch energy disturbances.

5.4 HF Current Generation

Especially when the output current is low, the setpoint compensating currents can approach zero. While this is good for keeping the branch energy variation and the switching losses caused by the HF modulation low, it can lead to module balancing problems if the steady-state error of the current controller is higher than the actual setpoint current. As explained in Section 5.1, the module capacitor voltage balancing is based on the estimation of the branch-current direction. If this cannot be estimated correctly over a longer period of time, the module capacitor voltages within a branch are not balanced, leading to potentially dangerous values.

This is a general problem with MMCs and it has been reported for drive applications with a corresponding solution in [135]. The solution is based on the injection of additional circulating currents, which increases the branch currents and thus makes the estimation of the branch current significantly simpler. The circulating currents are chosen so they do not influence the constant part of branch powers and hence do not impact the branch-energy control.

Similarly, an additional HF component can be injected into leg currents with the quasi-two-level PWM operation. This is achieved by adding an additional HF current component to the setpoints of the compensating current, as shown in Figure 5.2.

There are two methods proposed in this thesis for the generation of the HF current, which are explained below.

5.4.1 Constant HF Current Generation

A simple method to generate the additional HF current is to inject the same values into all three phase legs, disregarding the setpoint compensating currents. The preferred function is a square-wave function with a frequency equal to that of the PWM, and an amplitude $\hat{i}_{\mathrm{HF}}$

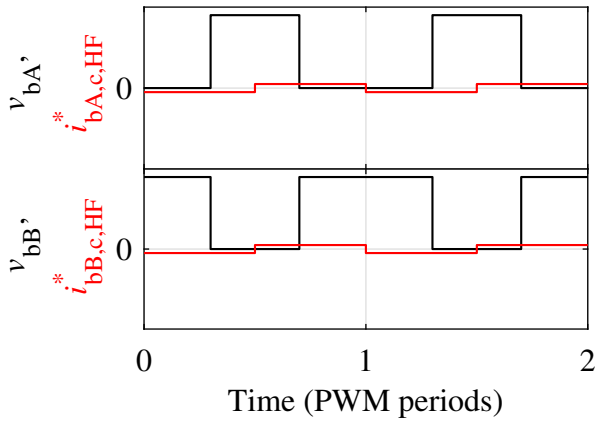


Figure 5.10: Example explaining the generation of the additional HF-current setpoints $i^*_{bA,c,HF}$ and $i^*_{bA,c,HF}$ over two PWM periods using the constant HF current generation method.

that is in a single percent range of the maximum output current. Under these conditions, the additional branch power caused by the HF current has a mean value of zero during a PWM period. Example waveforms that show the additional HF current components applied to branch currents are plotted with corresponding voltages in Figure 5.10.

5.4.2 Smart HF Current Generation

While the previously described method can be implemented very simply, it causes additional current loading at the branches and even additional distortion of the input current, which has to be buffered by the input capacitor C_i. In order to decrease these effects, the additional injection can be dynamically disabled when the absolute value of the setpoint compensating current determined by the branch-energy control block is above a defined threshold $I_{c,thr}$. Hence, when the compensating current is high enough for its sign to be estimated correctly, the additional HF current for the particular compensating current is deactivated. Nevertheless, in order to apply this method, the setpoint value of the compensating current has to be constant during the PWM period. Otherwise, the HF current could potentially be turned on and off several times within the PWM period, causing a disturbance for the energy controller. As a consequence, it can only be applied with the predictive branch-energy control.

5.5 Implemented High-Level Control

To test the converter prototype, two options for high-level control are implemented: an open-loop control for passive loads and a closed-loop control for driving a synchronous machine. In the sections below, these are explained briefly. Please note that the high-level control is not limited to these two options. These two options are implemented in particular to test the converter.

5.5.1 Open-Loop Control for Passive Load

The open-loop control is used to test the converter prototype with passive loads. It solely calculates the symmetric duty-cycle values

$$\begin{bmatrix} \delta_1' \\ \delta_2' \\ \delta_3' \end{bmatrix} = M \cdot \begin{bmatrix} \cos(\omega \cdot t) \\ \cos(\omega \cdot t - \frac{2 \cdot \pi}{3}) \\ \cos(\omega \cdot t - \frac{4 \cdot \pi}{3}) \end{bmatrix} \tag{5.33}$$

for selected angular frequency $\omega = 2 \cdot \pi \cdot f$ and selected modulation index M. These symmetric duty cycles are further extended with a zero duty-cycle component δ_0, leading to the setpoint duty-cycle values for the converter

$$\begin{bmatrix} \delta_1 \\ \delta_2 \\ \delta_3 \end{bmatrix} = \begin{bmatrix} \delta_1' + \delta_0 \\ \delta_2' + \delta_0 \\ \delta_3' + \delta_0 \end{bmatrix} \quad . \tag{5.34}$$

The zero component can either be zero

$$\delta_0 = 0 \quad , \tag{5.35}$$

not injecting any common-mode voltage component (Sine Modulation, SM), or a carrier-based space vector modulation (SVM), commonly applied in two-level inverters, is used to inject a common mode voltage component in order to increase the maximum achievable modulation index:

$$\delta_0 = -\frac{\max(\delta_1', \delta_2', \delta_3') + \min(\delta_1', \delta_2', \delta_3')}{2} \quad . \tag{5.36}$$

The third option considered in this thesis is an injection leading to the flat-top modulation. This option is studied in Section 7.1.

5.5.2 Closed-Loop Control for Synchronous Machines

The implemented closed-loop control of synchronous machines is based on the standard field oriented control in dq-coordinates consisting of two control loops and feed-forward terms for the output voltages [136]. For the sake of simplicity, no field weakening is applied. The outer control loop controls the machine speed with a proportional-integral (PI) controller. The inner control loop controls the stator currents with two PI controllers.

The speed PI controller is designed using symmetric optimum criterion [137]. The speed setpoint value is filtered to improve the input response, since the symmetric optimum criterion only optimizes the disturbance response. The output of the controller is solely the q-axis current setpoint value. The d-axis current setpoint is set to zero.

The current controllers are designed using an approach similar to the magnitude optimum criterion [137]. The main difference is that the damping factor of the resulting second-order lag system approximation is set to one instead of $\frac{1}{\sqrt{2}}$. The output of the current controllers are the output voltages in dq-coordinates. These are transformed into the 123-coordinates using

a measured rotor angle. The measured angle is adapted to compensate for the control delay, based on the measured speed. The resulting transformed voltages are divided by half of the input voltage to obtain the duty cycles. To increase the maximum achievable voltage (and thus also the speed), SVM injection according to (5.36) is applied.

For the control implementation with the converter prototype, an additional filtering of the speed is added to reduce the noise in the measured signal and to improve the control behavior. The filter cutoff frequency is set to 50 Hz and the filter is considered in the speed-controller design.

6 Control Validation

This chapter presents the validation of the control proposed in the previous chapter. First, the simulation model is presented and validated using a converter prototype for various operating points. At the end of this chapter this model is further used to perform a parameter variation study in order to evaluate the sensibility of the proposed control. Furthermore, the feasibility of the proposed converter operation is demonstrated for a dynamic operation with a synchronous machine. In addition to the validations presented in this chapter, frequency and modulation-index sweeps are performed with the MMC prototype in Appendix C.

6.1 Simulation Model and Downscaled Experimental Prototype

6.1.1 Simulation Model

The simulation model is implemented as a hybrid system[1)] in *Mathworks Simulink* using a *Plexim Plecs* toolbox for the physical part of the model. While the converter control is modeled as a time-discrete system, the physical part is modeled as time-continuous. The overview of the model can be seen in Figure 6.1.

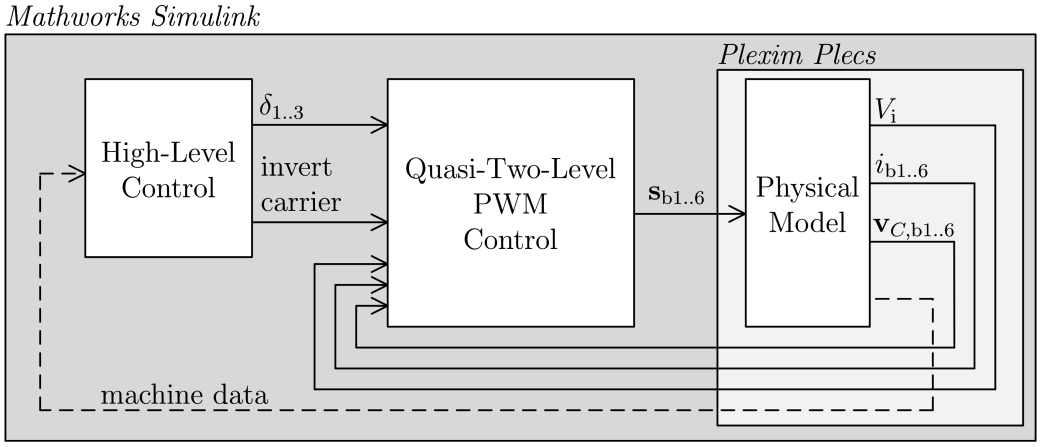


Figure 6.1: Overview of the simulation model implemented in *Mathworks Simulink*.

The converter control is implemented according to the control presented in Chapter 5. Since a large part of the control is based on FSMs, it is implemented as a set of *Matlab script* functions for *Simulink*. The main difference between the control implemented for simulations and the

[1)] A hybrid system combines time-continuous and time-discrete blocks in a single simulation model.

control implemented for the converter prototype is that the modeling of the FPGA pipe-lining is omitted. Thus, a significantly lower discrete-system frequency can be used (typically 2 MHz), leading to significantly lower simulation times.

The physical part of the model implemented in *Plecs* consists of a custom MMC block, which is fed from a direct voltage source and connected to a passive load or to a synchronous machine. The direct voltage source is center-tapped to simplify the common-mode voltage measurement. The passive load is modeled as a star connection of a series connected inductor and resistor. Since a constant field-linked flux linkage is assumed for the machine, a simple linear model of a permanent-magnet synchronous machine (PMSM) available at the *Plecs* library can be used. The constant flux linkage of permanent magnets represents the constant flux linkage induced by a constant field current.

The MMC model, displayed in Figure 6.2, is a custom-made *Plecs* subsystem block consisting of six branches, each comprising a branch resistor, a coupled center-tapped branch inductor, and a custom block modeling the modules. The center-tapped branch inductors are modeled in the magnetic domain of *Plecs*.

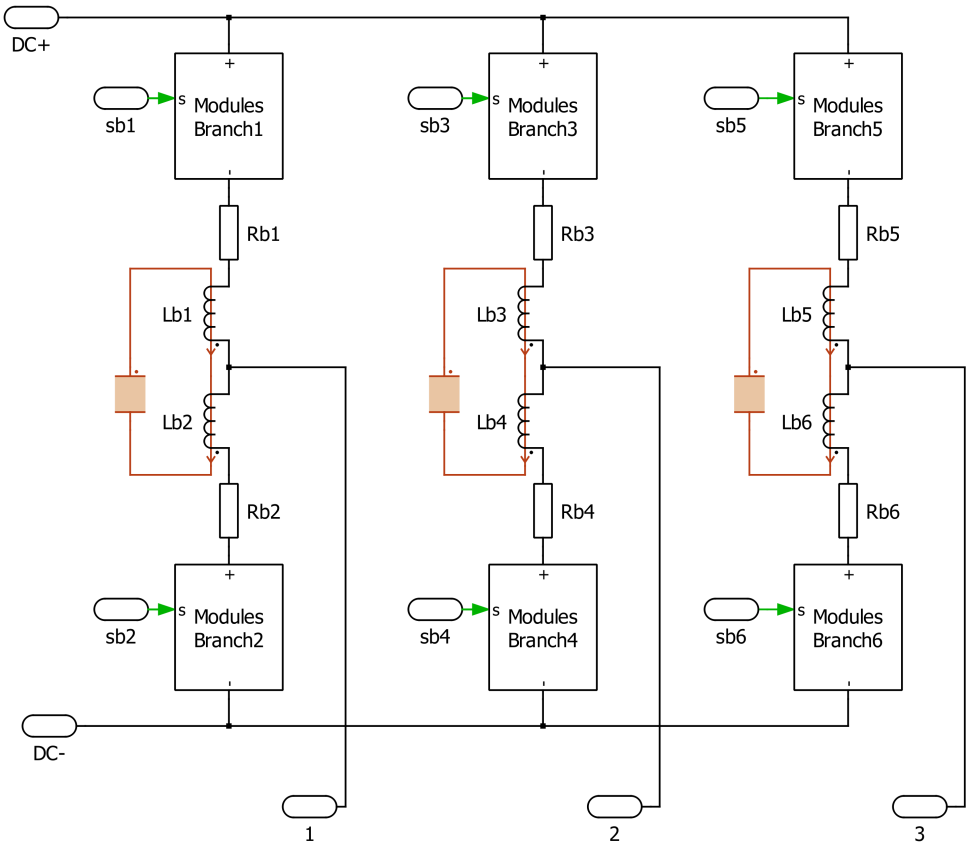


Figure 6.2: Custom MMC model implemented in *Plexim Plecs*.

A classical approach for modeling of the branch modules would be to create a half-bridge module consisting of two IGBT modules and a module capacitor and then to connect n_{mpb} of these in series. However, this approach leads to two major problems: First, the scalability of the model for different numbers of installed modules per branch is very low, since the model would have to be edited manually each time a change is required. Second, the simulation speed would

be relatively low, since *Plecs* generates a different simulation matrix for each switching state and there is a very high number of possible switching states with MMCs.

Instead, a different modeling approach, displayed in Figure 6.3, is derived. This model utilizes a mathematical representation of the modules, similar to the one derived as "switched model" in [138]. The input of the model is a switching-state vector labeled as "s" with a length equal to the number of modules per branch. The module capacitors are represented by a vector integrator (integrating each component of the vector separately), which integrates the capacitor currents. These currents are obtained by multiplying the switching-state vector with the measured branch current value. This means that if a module capacitor is inserted (switching function is one), the module capacitor current has the value of the branch current. If the module output is short circuited (the switching function is zero), the capacitor current is zero. The voltages at the module outputs are obtained by element-wise multiplication of the switching function vector and the integrator output vector, representing the voltages at the particular module capacitors. The resulting branch voltage is a sum over the vector representing the module output voltages.

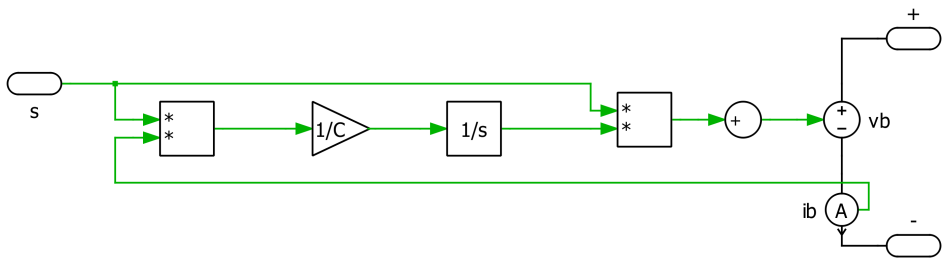
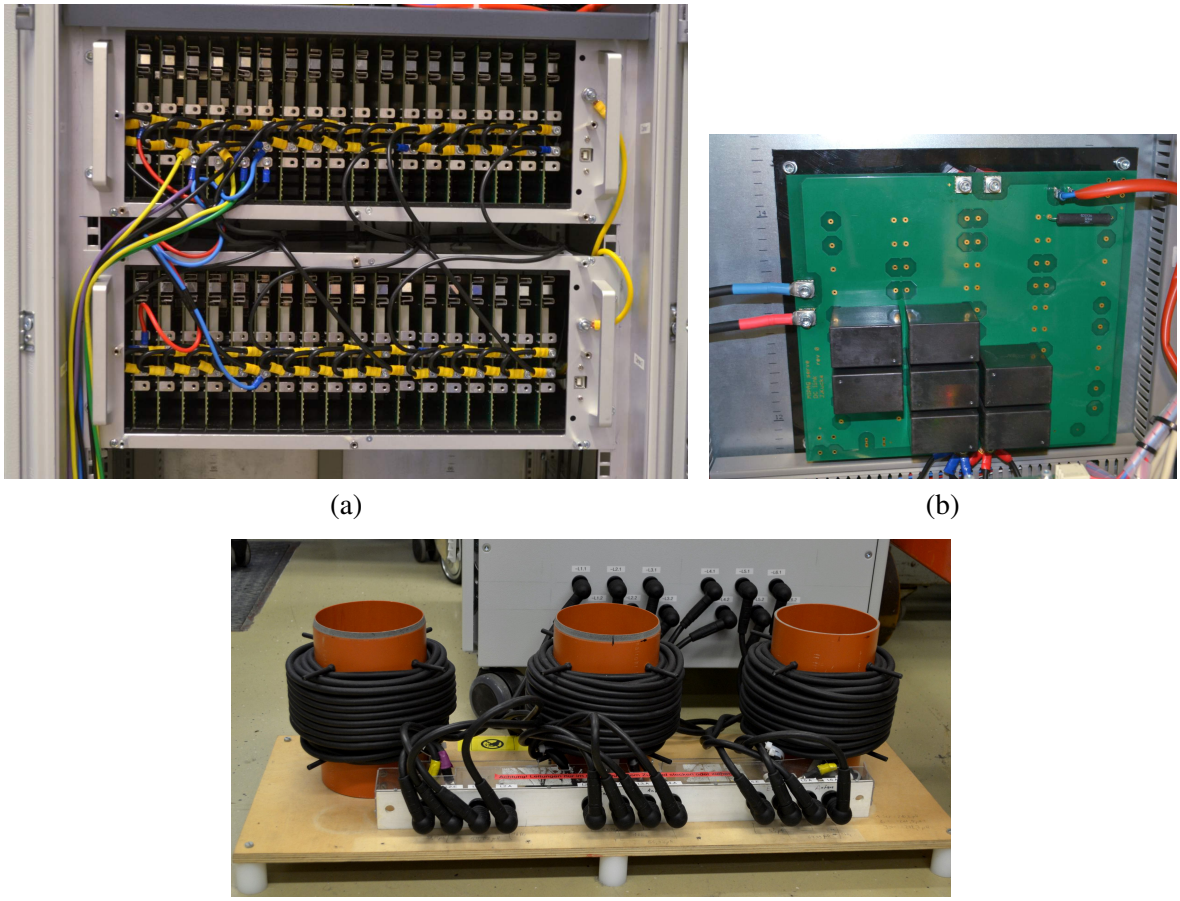


Figure 6.3: The simulation-speed optimized model of branch modules implemented in *Plexim Plecs*.

While this modeling approach can be extended for any number of modules per branch and leads to higher simulation speed, it has two major disadvantages: the indirect modeling of the modules increases the complexity of the loss calculation (studied later in Section 8.3.2), and the passive state, when both IGBTs are turned off, cannot be activated. The second disadvantage means that the switching dead-time and the rectifying function of the diodes during converter start-up are not considered in the model. If these have to be studied in particular, the classical modeling approach is necessary. By default, the simulation-speed optimized approach from Figure 6.3 is used.

6.1.2 Downscaled Experimental Prototype

To validate the simulation model and to demonstrate the general feasibility of the quasi-two-level PWM operation of MMCs, an experimental downscaled prototype has been developed. The power circuit is based on 36 versatile MOSFET H-bridge modules, designed by the company *Protolar GmbH* and installed in two racks (Figure 6.4a), a dc-link capacitor PCB (Figure 6.4b), and three center-tapped air-core branch inductors (Figure 6.4c). The H-bridge modules are connected with branch inductors to form the six MMC branches, using only a single half-bridge per module (and thus being half-bridge modules). The modules are rated at a peak current of 50 A and at a peak capacitor voltage of 70 V. The module capacitance is $C_{\mathrm{mod}} = 200\ \mu\mathrm{F}$. At each module, there is an isolated $\Delta\Sigma$ ADC for the module capacitor voltage measurement and an additional isolating dc-dc converter powering the auxiliary circuits and precharging the



(a) (b)

(c)

Figure 6.4: Photos of the converter prototype components: a) two racks with 18 modules each – the upper rack comprises branches 1,3 and 5 and the lower rack branches 2, 4 and 6 b) dc-link capacitor PCB c) air-core center-tapped branch inductors.

module capacitors, enabling a simpler converter start-up. At the rear side of each rack, there is a PCB board installed, providing an auxiliary power supply to the modules and connecting the modules' signals to the rack's FPGA *Xilinx Spartan 6*. The FPGA is connected to the main control system via 12 optical fibers (six input, six output) with a baud rate of 10 MHz at each channel, providing an interface between the control system and the modules.

The platform for the main control system is a *Protolar ControlCube*, shown in Figure 6.5. The main board of the modular control system comprises a system-on-chip unit *Xilinx Zynq 7000*, which integrates an FPGA with a double-core ARM processor. Besides the main computing card, one fiber-optic card and one 24 V IO card are installed at the *ControlCube*, together with an expansion measurement card developed for this particular project. The expansion measurement card enables the connection of up to seven 14-bit voltage or current measurement cards. To minimize the number of necessary pins, the channels are multiplexed with high-speed digital multiplexers. The voltage and current measurement cards are based on a 14-bit ADC *Analog Devices' AD9240ASZ*, which continuously converts 10 Mega-samples per second. A parallel magnetically isolating digital data transfer is used to provide a galvanic isolation for the measurements. Voltages are measured using passive resistor networks and currents are measured using current-measuring PCB shunts. In total, there are six current measurement cards to measure the branch currents, and a single voltage measurement card to measure the dc-link

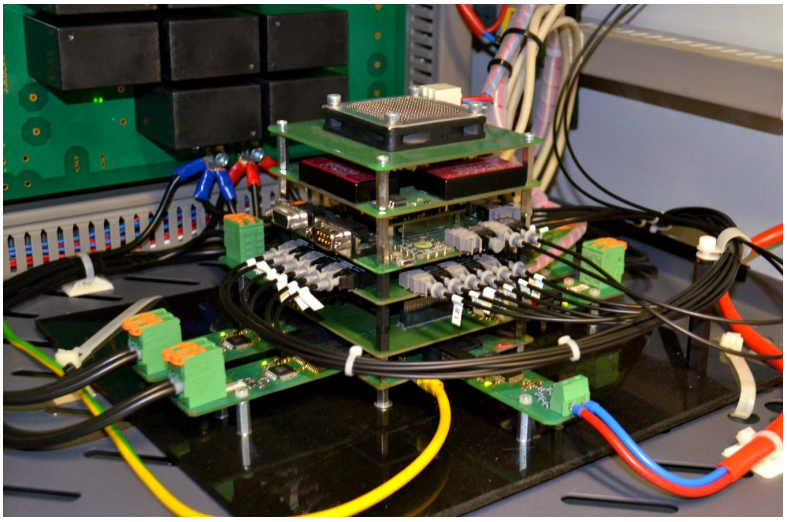


Figure 6.5: *Protorlar ControlCube* with a custom-made expansion measurement card (at the bottom).

voltage. The 24 V IO card enables communication with the relays installed in the prototype's cabinet, e.g. to disconnect the power circuit in the case of system failure.

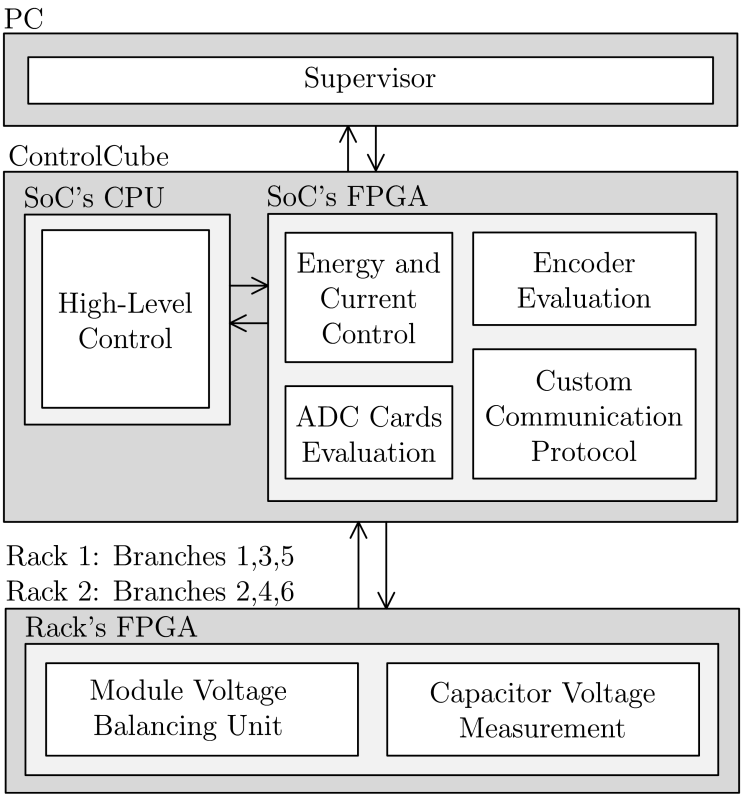


Figure 6.6: The partition of the control system implemented in the quasi-two-level PWM-operated MMC prototype.

The basic partition of the control system can be found in Figure 6.6. The central unit in the control system is the *ControlCube*, comprising the high-level control, the branch-energy control and the current control FSM for all three phase legs, a decoding logic for the data obtained from the rotor-position encoder, and an evaluation unit for ADC cards, which controls the

channel multiplexing. The decision to carry out implementation in a single chip, instead for each phase leg separately, enables simple supervision of the system, which is advantageous for debugging and data logging. The module voltage balancing is implemented directly at the Rack's FPGAs, together with the Sinc^3 filtering of the ΔΣ-ADC signals, which measure the module capacitor voltages. The actual setpoint number of inserted modules in each branch and the estimated branch current direction are sent to each rack over six optical fibres using a custom-made protocol with an update frequency of approximately 2 MHz. The measured branch energy and mean values of branch voltages for each branch are sent asynchronously over five optical fibres with a data tranfer rate of approximately 340 kHz to be directly used in the control. The voltages of particular modules required for the system observation are transferred slowly through a single optical fibre with an approximate data transfer rate of 80 kHz. All communication protocols are custom made and include an eight bit cyclic redundancy check (CRC) to assure data consistency.

The system is supervised, observed and logged using *Protolar Supervisor* running on a personal computer (PC) using *Microsoft Windows*. The data-logging period of the control system is approximately 35 µs and the logging system is used for a part of the measurements presented later. The PC communicates with CPU1 of the *ControlCube* via Ethernet. The CPU1 exchanges the observed data with CPU0 via shared memory. The CPU0 executes the high-level control and collects the data from a custom-made observation FPGA unit. The observation unit ensures that all observed data from the internal FPGA control are synchronized before being transferred to *Protolar Supervisor*.

The parameters of the prototype are summarized in Table 6.1 together with the control settings. The branch resistance is estimated using the datasheet values for the applied MOSFETs and

Table 6.1: Parameters of the downscaled converter prototype.

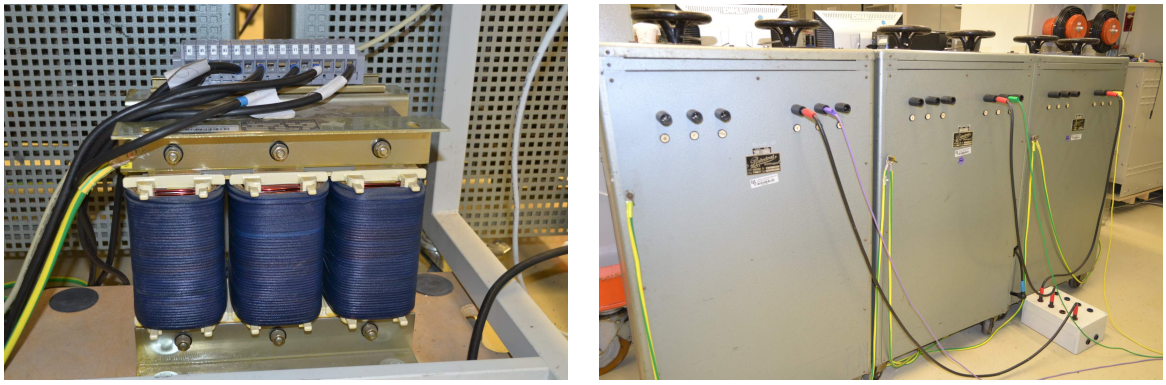
Parameter		Fast proportional	Predictive
Peak output current	$\hat{i}_\mathrm{o}$	up to 20 A	up to 20 A
Maximum allowed duty cycle	δ_max	0.9	0.9
Leg inductance (coupled)	L_leg	210 µH	210 µH
Modules per branch	n_mpb	6	6
Module capacitance	C_mod	200 µF	200 µF
DC-link capacitance	C_i	280 µF	280 µF
Energy storage constant [a]	H	3.6 ms	3.6 ms
Setpoint module capacitor voltage	V_C^*	40 V	40 V
PWM frequency	f_PWM	1 kHz	1 kHz
HF modulation frequency	f_HF	25 kHz	25 kHz
Delay between switch. instants	T_d	1 µs	1 µs
Prediction period	T_p	250 ns	250 ns
Energy controller gain	$G_{\mathrm{P},e}$	2000 $\frac{1}{\mathrm{s}}$	1200 $\frac{1}{\mathrm{s}}$
HF current amplitude	$\hat{i}_\mathrm{HF}$	0.2 A (const.)	0.3 A (smart)
HF current threshold	$I_\mathrm{c,thr}$	-	0.15 A (smart)
Estimated branch resistance	$\tilde{R}_\mathrm{b}$	75 mΩ	75 mΩ

[a] The energy storage constant is defined in [120] as a ratio between the total energy stored in passive components (mostly capacitors) and the rated apparent power of the converter. It is assumed that SVM is applied.

measured values for the branch inductors. The value was further increased to account for the connections between the modules based on an observation of the converter's behavior.

6.2 Validation of the Simulation Model Using Passive Loads

In this section, the simulation model is validated using a comparison to measured data obtained from the downscaled converter prototype. The simulations and measurements are both performed for identical converter parameters, listed in Table 6.1. To guarantee the same operating point with both the simulation model and the converter prototype, an open-loop control with a passive inductive-resistive load is applied. The load comprises a three-phase inductor (Figure 6.7a) and three resistors with adjustable resistance (Figure 6.7b). The converter is fed by a central laboratory dc link with a rated voltage of 220 V. The overview of the parameters used for the validation can be found in Table 6.2.



(a) (b)

Figure 6.7: Utilized passive load components for tests of downscaled MMC prototype: a) three-phase iron-core inductor b) three discrete resistors with adjustable resistance connected in star.

Table 6.2: Parameters of the passive load and voltage source used for the model validation.

Input voltage	V_i	220 V
Output inductance (passive load)	L_o	13 mH
Output resistance	R_o	0..5.5 Ω

The measured waveforms are captured by an eight-channel 1 GHz high-definition oscilloscope *Teledyne LeCroy HDO8108*, using three current probes and five differential voltage probes. The following values were determined during the measurements:

- branch currents
  - branch 1 i_{b1} – 10 MHz current probe *Keysight N2781B*
  - branch 2 i_{b2} – 10 MHz current probe *Keysight N2781B*
- output currents
  - phase 1 i_{o1} – calculated using i_{b1} and i_{b2}

  - phase 2 i_{o2} – 10 MHz current probe *Keysight N2781B*
  - phase 3 i_{o2} – calculated using i_{o1} and i_{o2}
- branch voltages
  - branch 1 v_{b1} – 100 MHz differential voltage probe *TESTEC TT-SI 9101*
  - branch 2 v_{b2} – 100 MHz differential voltage probe *TESTEC TT-SI 9101*
- module capacitor voltages
  - branch 1, nr. 4 $v_{b1,4}$ – 100 MHz differential voltage probe *TESTEC TT-SI 9101*
  - branch 1, nr. 5 $v_{b1,5}$ – 100 MHz differential voltage probe *TESTEC TT-SI 9101*
  - branch 1, nr. 6 $v_{b1,6}$ – 100 MHz differential voltage probe *TESTEC TT-SI 9101*

Since a relatively long time scale is viewed during the following experiments, the raw data is post-processed by a high-order 1 MHz low-pass filter in *Mathworks Matlab* to remove the electromagnetic interference (EMI) caused by semiconductor switching.

6.2.1 Duty Cycle Variation

The first step in the validation of the simulation model is to compare the short-period data for different constant duty cycle values. In the experiment, the duty cycle value of the first phase δ_1 is varied from -0.9 up to 0.9. The duty cycles for the second and third phase

$$\delta_2 = \delta_3 = -\frac{1}{2} \cdot \delta_1 \tag{6.1}$$

are chosen symmetrically to the first phase. The output resistance value R_o is adjusted to keep the output current value $\hat{i}_o$ constant at 20 A.

In Figures 6.8 and 6.9, the simulation and experimental results are shown for the fast proportional branch-energy control. In Figures 6.10 and 6.11, the results are plotted for the predictive branch-energy control. The figures show the waveforms of the first phase leg for two PWM periods. These waveforms are: the output current, the branch voltages, the branch currents and the module capacitor voltages. Since the number of oscilloscope channels during the measurement is limited to eight, only three module capacitor voltages of branch 1 are measured. For completeness, all simulated module capacitor voltages are shown.

In general, almost a perfect match between the simulation model and measurements for both branch-energy control approaches can be stated for the output current, branch voltage and branch current waveforms. There are slight deviations between the module capacitor voltage waveforms of the measured system and those obtained from simulation. These are most likely caused by the parameter deviations within the system and the capacitor voltage measurement offsets. Nevertheless, these deviations are rather small and acceptable. In conclusion, the short-period experiment validates the simulation model.

Taking a closer look at the figures, several other points can be observed. First, the branch current is always low when the branch voltage is high and vice versa, which is the main principle of quasi-two-level PWM operation. Second, the capacitor voltage values are reset to their original value at the end of each period, leading to extremely low branch energy variation, even with

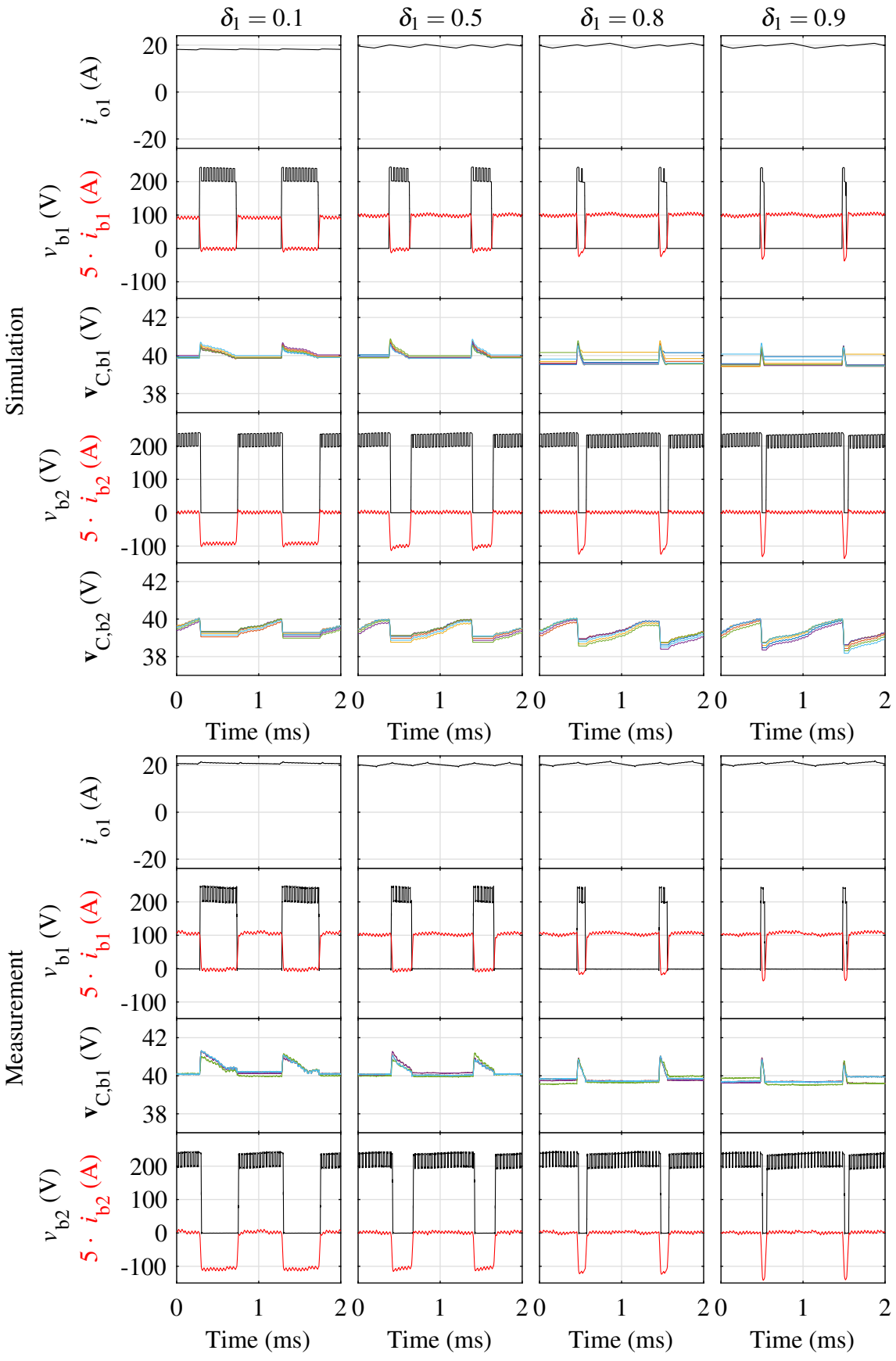


Figure 6.8: Simulated and measured data of a quasi-two-level PWM-operated downscaled converter prototype for various positve duty cycle values δ_1. The output current of phase 1 is kept constant at 20 A. **Fast proportional branch-energy control** is applied.

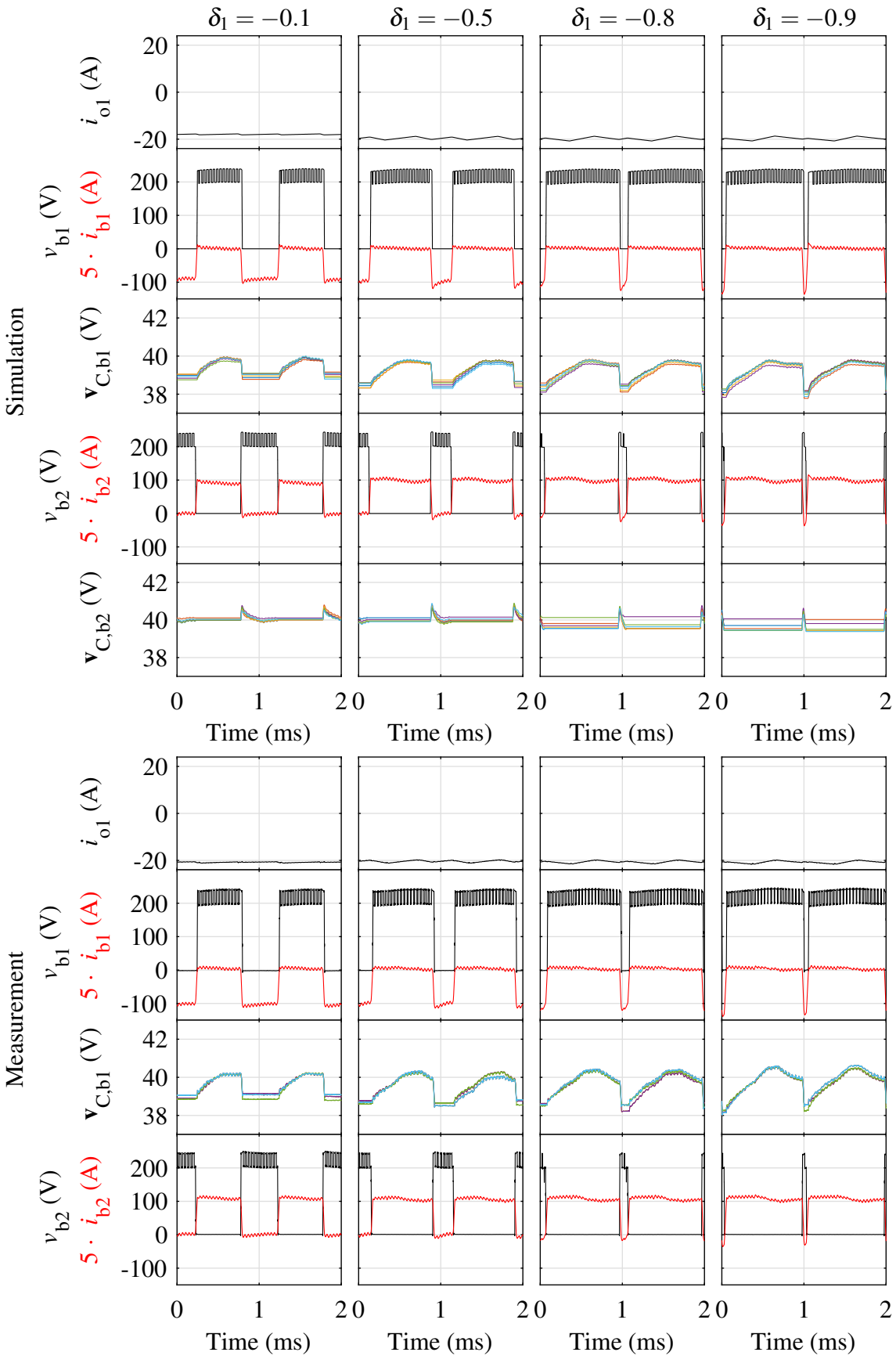


Figure 6.9: Simulated and measured data of a quasi-two-level PWM-operated downscaled converter prototype for various negative duty cycle values δ_1. The output current of phase 1 is kept constant at 20 A. **Fast proportional branch-energy control** is applied.

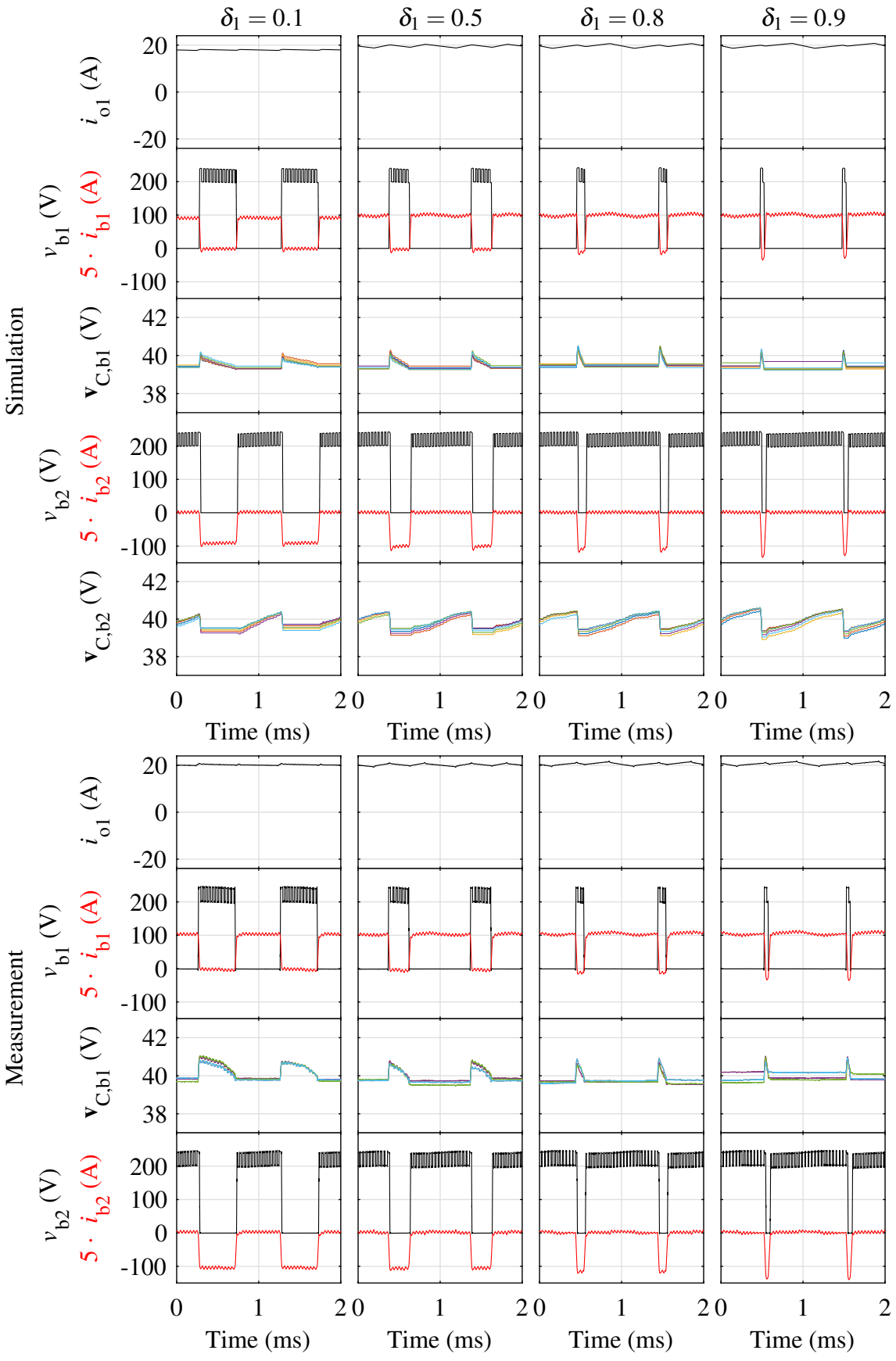


Figure 6.10: Simulated and measured data of a quasi-two-level PWM-operated downscaled converter prototype for various positve duty cycle values δ_1. The output current of phase 1 is kept constant at 20 A. **Predictive branch-energy control** is applied.

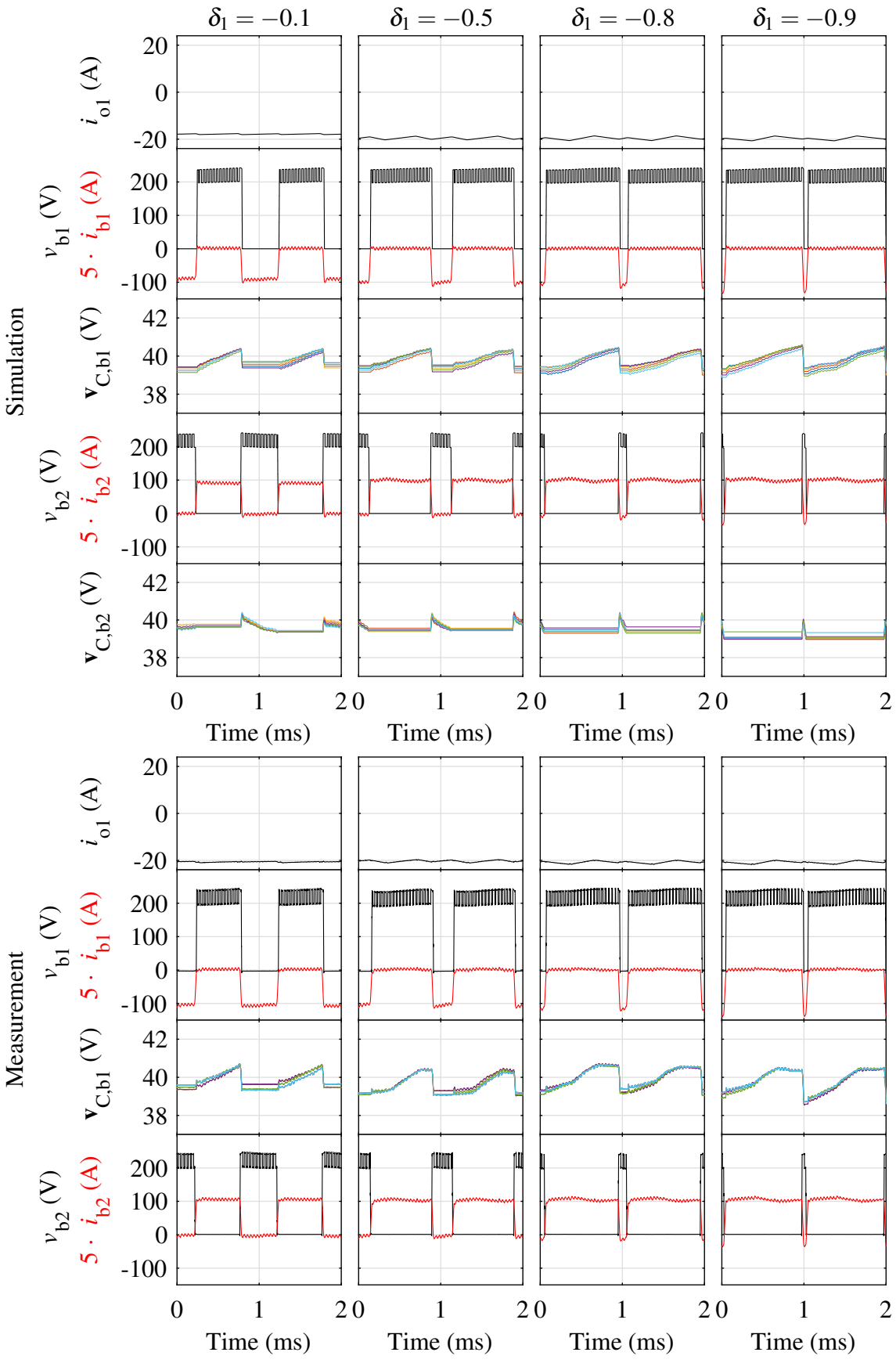


Figure 6.11: Simulated and measured data of a quasi-two-level PWM-operated downscaled converter prototype for various negative duty cycle values δ_1. The output current of phase 1 is kept constant at 20 A. **Predictive branch-energy control** is applied.

very low output frequencies (zero Hertz in this case). Third, the module capacitor voltage variation becomes more severe the higher the duty cycle is. Finally, comparing the predictive branch-energy control to the fast proportional one, it can be stated that the predictive energy control leads to steadier compensating current setpoints and has lower module capacitor voltage variation.

6.2.2 Modulation Index and Output Frequency Variation

In the second experiment carried out to validate the simulation model, the output currents as well as the voltages and currents of Branch 1 are investigated over a longer time scale for different modulation indices M and different output frequencies f, showing one output period. Similar to the previous case, both types of branch-energy control are considered.

In Figures 6.12–6.14, an operation at $f = 5$ Hz is shown for different modulation indices. The output resistance value is adjusted to keep the output current amplitude $\hat{i}_\mathrm{o} = 20$ A constant. In addition to a very good match between the simulation and the measured waveforms, it can be seen that the higher the modulation index is, the higher the compensating currents (and thus higher branch currents) and the module capacitor voltage variation. Additionally, the predictive-branch-energy control leads to lower module capacitor voltage variation than fast proportional branch-energy control. This is mainly visible with high modulation indices, at which the fast proportional energy control has only a short time to compensate for the power peaks, since these have to happen prior to the compensation, unlike with the predictive branch-energy control.

In Figure 6.15, the operation with the modulation index $M = 0.1$ and lower output current is plotted. It can be seen that lowering the output current decreases the module capacitor voltage variation significantly. This confirms the theoretical findings from Chapter 4, which state that the branch energy variation is quadratically dependent on the peak output current value.

Figure 6.16 shows the converter operation at higher output frequency $f = 15$ Hz with a modulation index $M = 0.9$ and output current amplitude $\hat{i}_\mathrm{o} = 20$ A. Comparing this figure to Figure 6.12, it can be confirmed that the peak values of the branch currents or module capacitor voltages are independent of the output frequency. This is due to the fact that the branch energy disturbance is compensated within each PWM period.

6.2.3 Common-Mode Voltage Injection

Figures 6.17 and 6.18 show an application of the common-mode techniques, i.e., carrier-based space vector modulation and flat-top modulation, for their maximum achievable modulation indices $M = 1.05$ and $M = 1.1$, respectively.

Observing the figures, it can be stated that the simulation model matches the experimental setup and that the operation is stable. The flat-top modulation will be studied more deeply in Section 7.1.

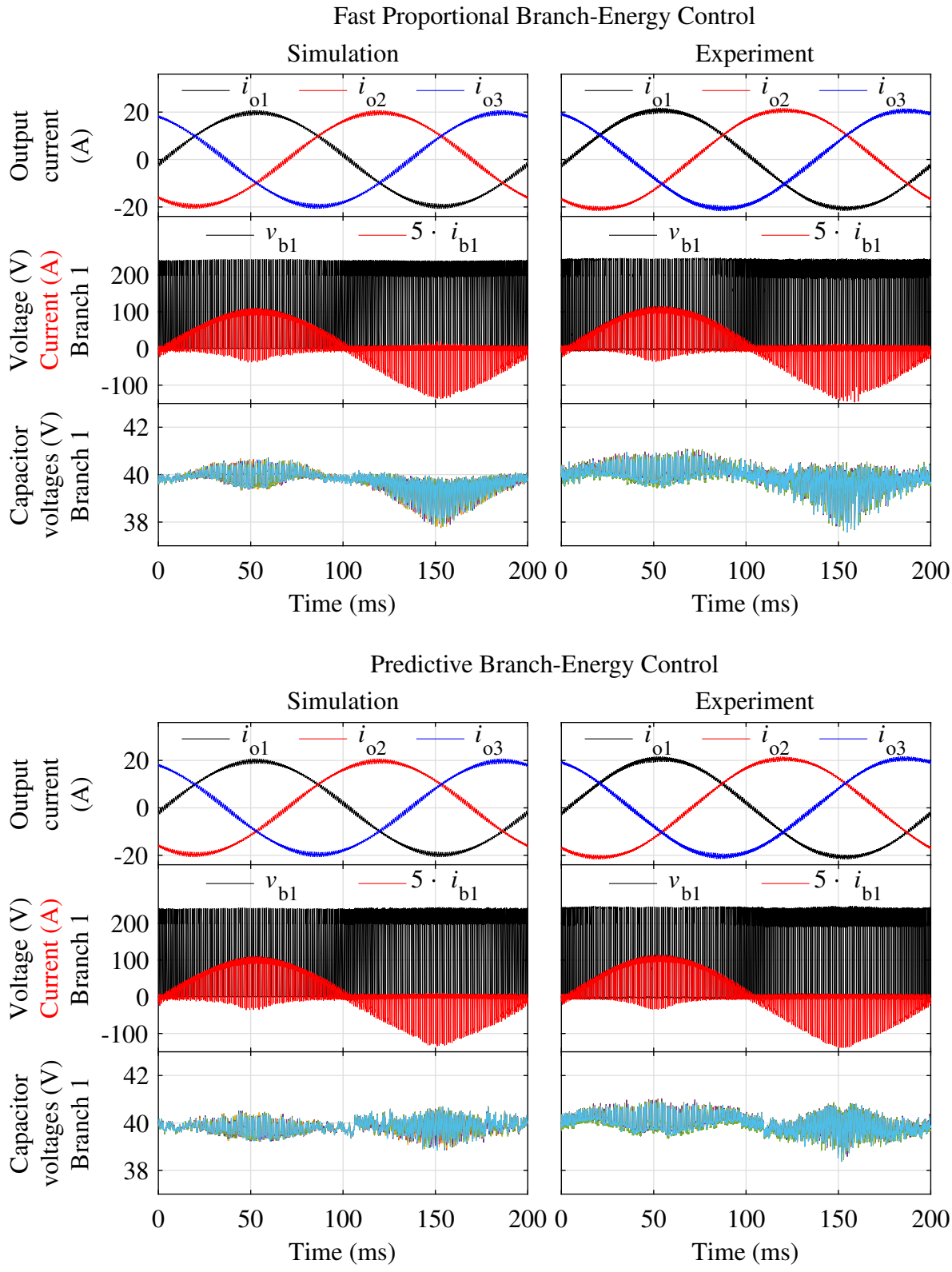


Figure 6.12: Simulated and measured data of a quasi-two-level PWM-operated downscaled converter prototype for modulation index $M = \mathbf{0.9}$ and the output frequency $f = \mathbf{5\ Hz}$. The output current amplitude is $\hat{i}_o = 20$ A. Top: fast proportional branch-energy control, bottom: predictive energy control.

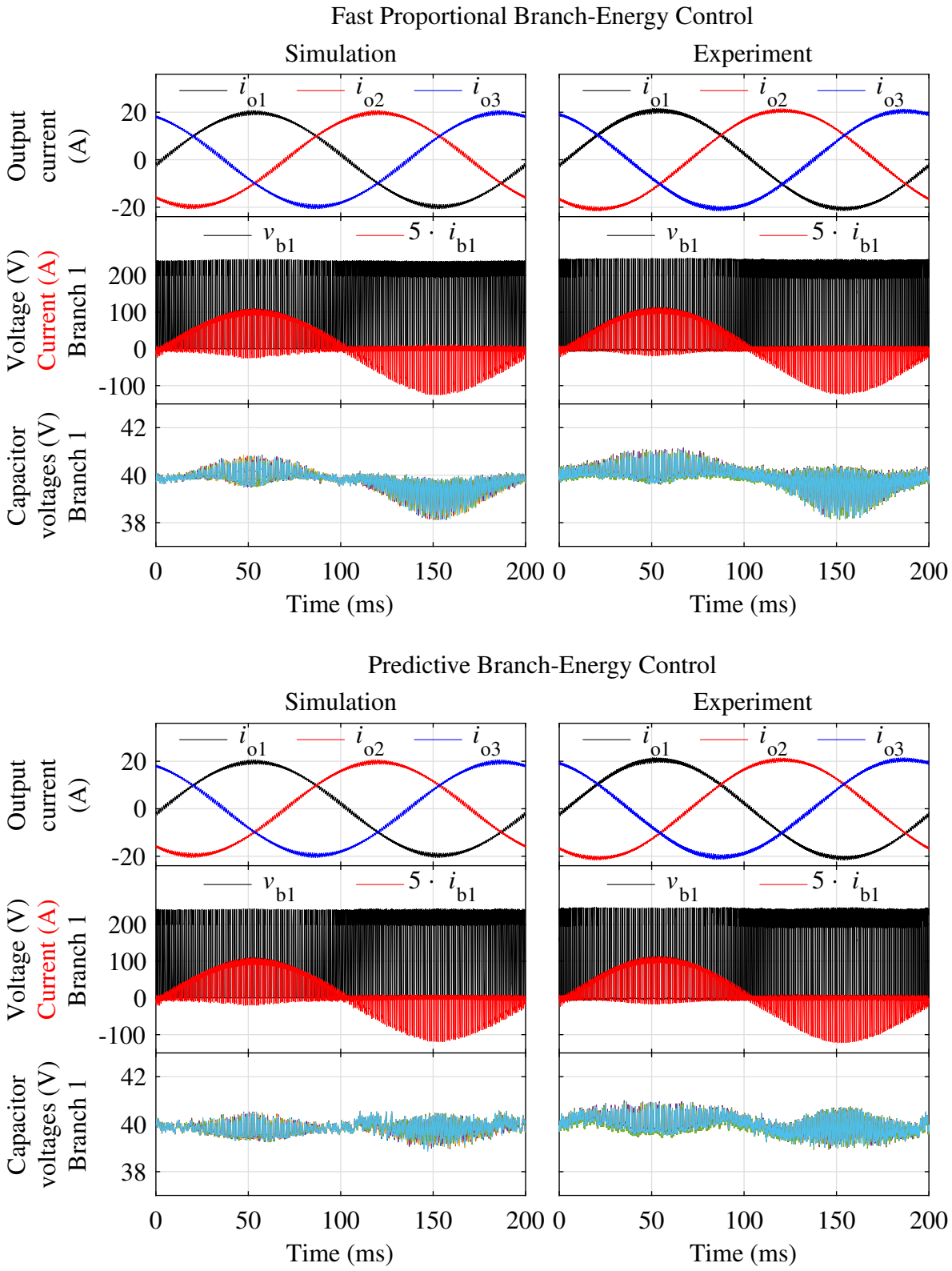


Figure 6.13: Simulated and measured data of a quasi-two-level PWM-operated downscaled converter prototype for modulation index $M = \mathbf{0.8}$ and the output frequency $f = \mathbf{5\ Hz}$. The output current amplitude is $\hat{i}_o = 20$ A. Top: fast proportional branch-energy control, bottom: predictive energy control.

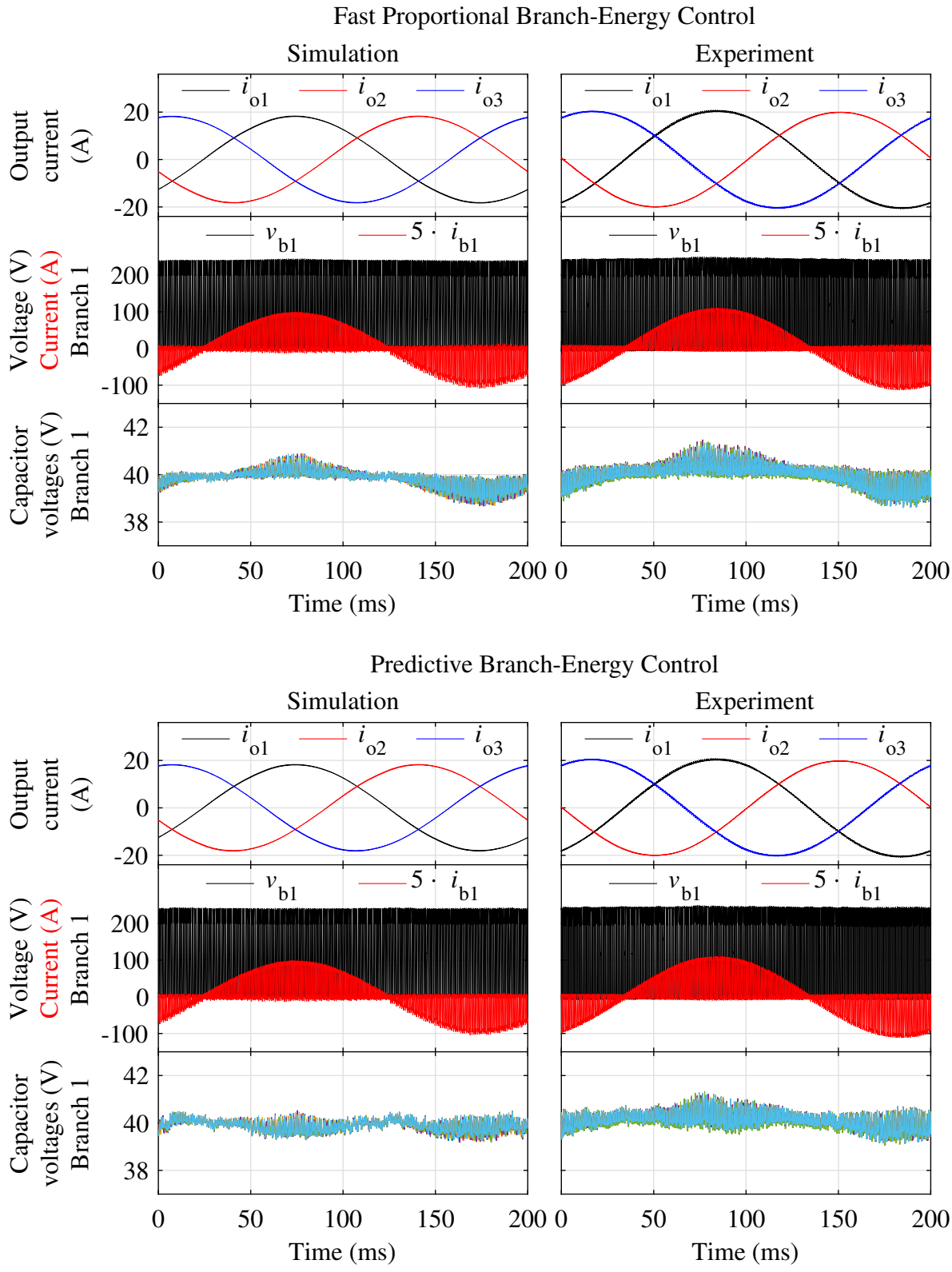


Figure 6.14: Simulated and measured data of a quasi-two-level PWM-operated downscaled converter prototype for modulation index $M = \mathbf{0.1}$ and the output frequency $f = \mathbf{5\ Hz}$. The output current amplitude is $\hat{i}_o = 20$ A. Top: fast proportional branch-energy control, bottom: predictive energy control.

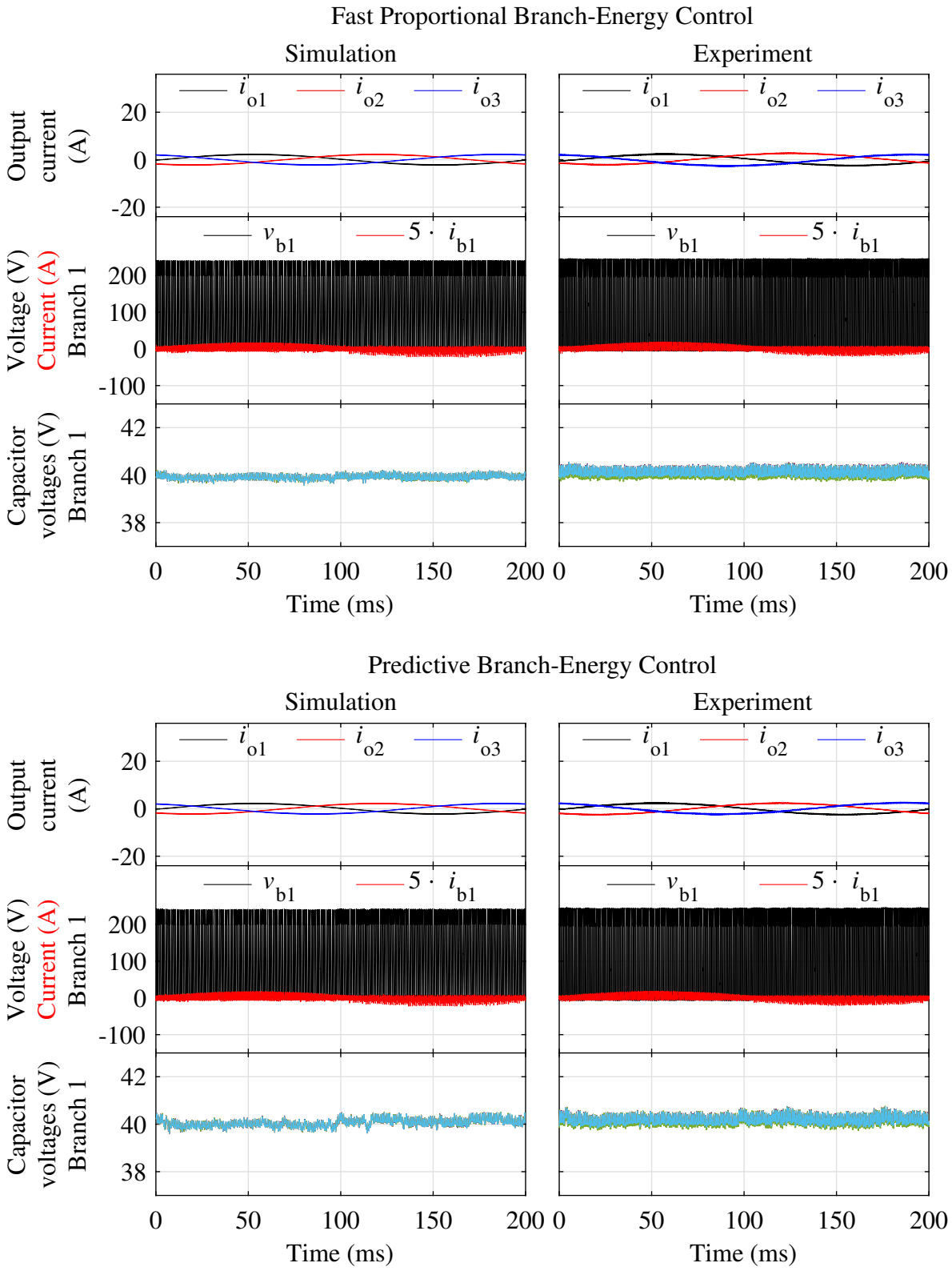


Figure 6.15: Simulated and measured data of a quasi-two-level PWM-operated downscaled converter prototype for modulation index $M = \mathbf{0.1}$ and the output frequency $f = \mathbf{5\ Hz}$. The output resistance is $R_o = \mathbf{4.95}\ \Omega$. Top: fast proportional branch-energy control, bottom: predictive energy control.

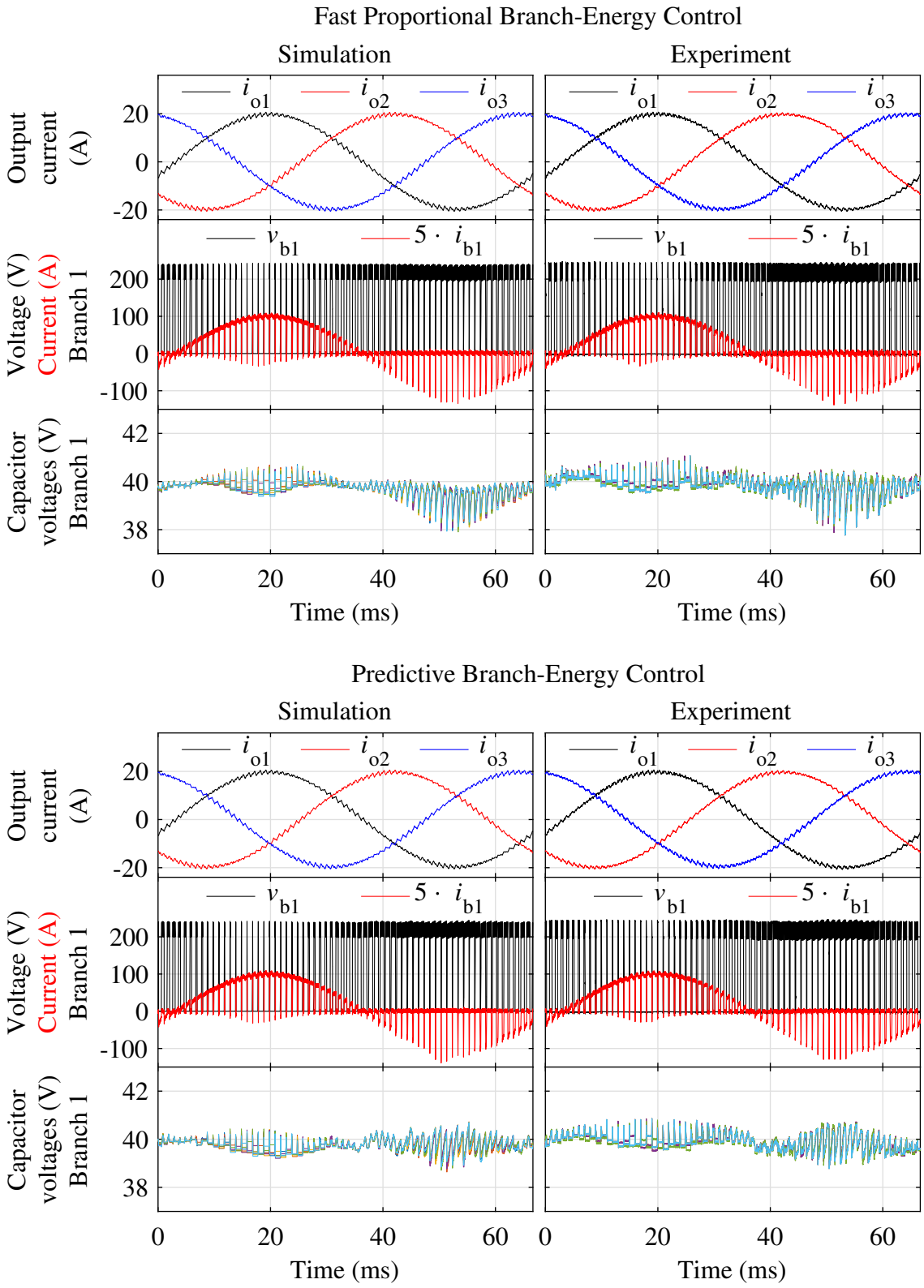


Figure 6.16: Simulated and measured data of a quasi-two-level PWM-operated downscaled converter prototype for modulation index $M = \mathbf{0.9}$ and the output frequency $f = \mathbf{15\ Hz}$. The output current amplitude is $\hat{i}_o = 20$ A. Top: fast proportional branch-energy control, bottom: predictive energy control.

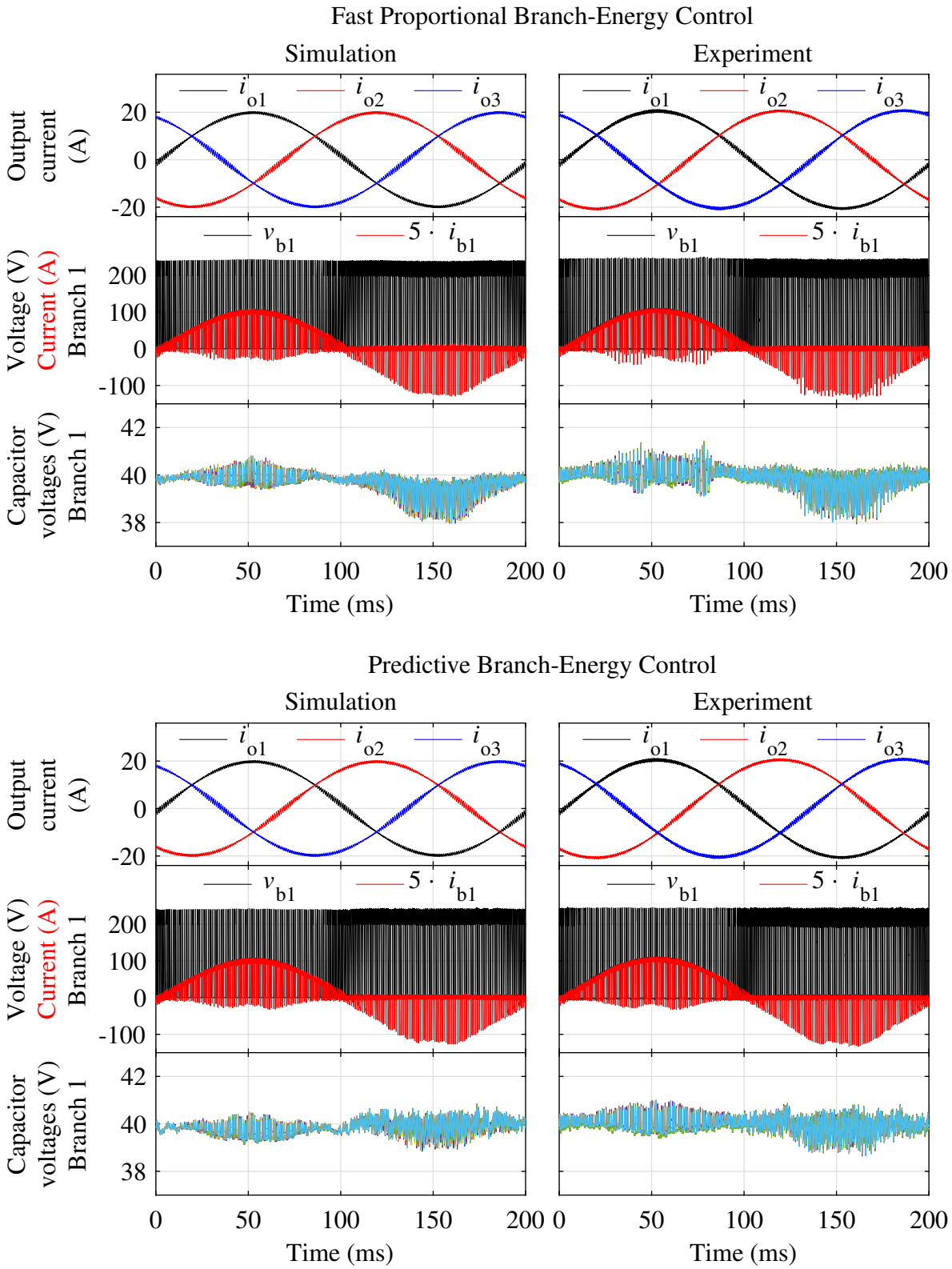


Figure 6.17: Simulated and measured data of a quasi-two-level PWM-operated downscaled converter prototype with activated **carrier-based space vector modulation** for modulation index $M = 1.05$ and the output frequency $f = 5$ Hz. The output current amplitude is kept constant at $\hat{i}_o = 20$ A. Top: fast proportional branch-energy control, bottom: predictive energy control.

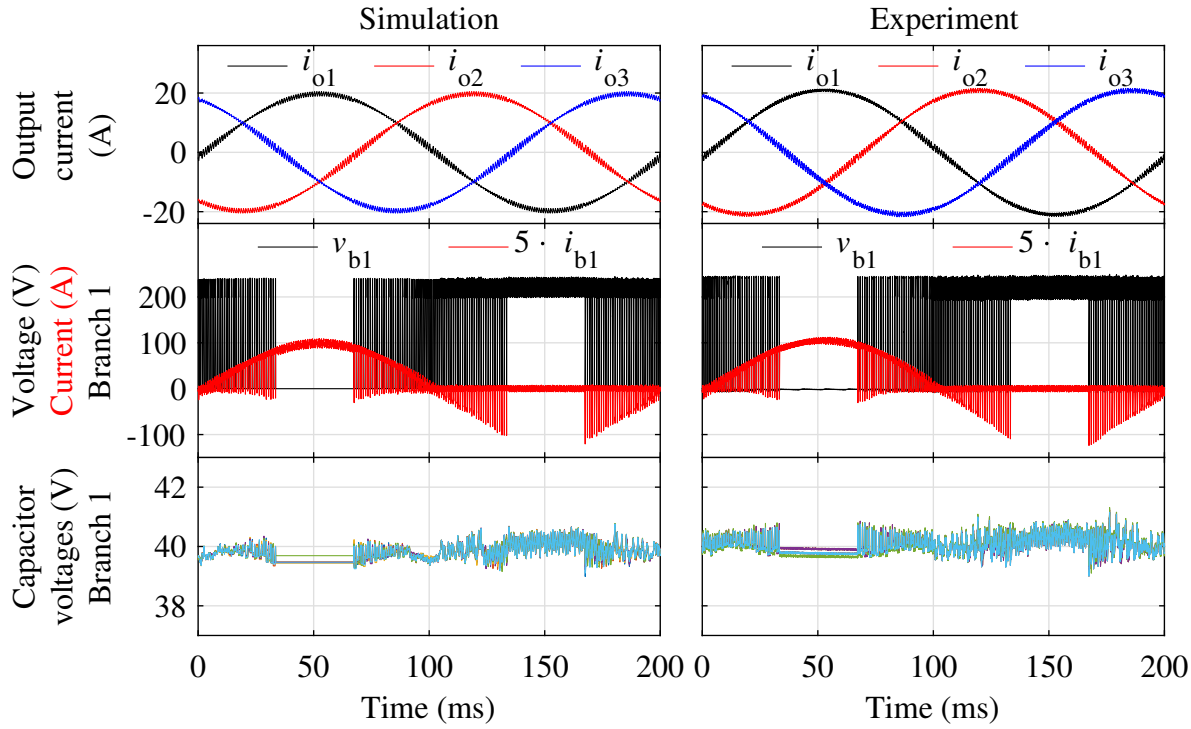


Figure 6.18: Simulated and measured data of a quasi-two-level PWM-operated downscaled converter prototype with activated **flat-top modulation** for modulation index $M = 1.1$ and the output frequency $f = 5$ Hz. The output current amplitude is kept constant at $\hat{i}_o = 20$ A. Predictive branch-energy control is applied.

6.3 Influence of HF-Current Injection

To demonstrate the purpose and necessity of the HF-current injection, an experiment deactivating the unit is carried out. The measured results are plotted in Figure 6.19. The parameters and measurement setup are identical to those used in Section 6.2.

If the branch currents are low and their ripple is relatively high, the branch current sign could be determined incorrectly. As can be observed in the left part of the figure in the time range from 80 to 180 ms, this could cause a malfunction of the module capacitor voltage balancing unit, increasing the voltage spread between the modules within one branch. Depending on the operating point, this voltage spread between the modules could lead to potentially dangerous voltage levels. This does not happen when the HF-current injection is activated, as demonstrated on the right side of the figure.

Note that the additional HF current has an amplitude of only $\hat{i}_{HF} = 300$ mA and thus does not cause a visible difference in the branch-current waveforms between the left part and the right part of Figure 6.19. On the other hand, this further confirms the expectation that the HF currents do not impact the current loading of branches significantly.

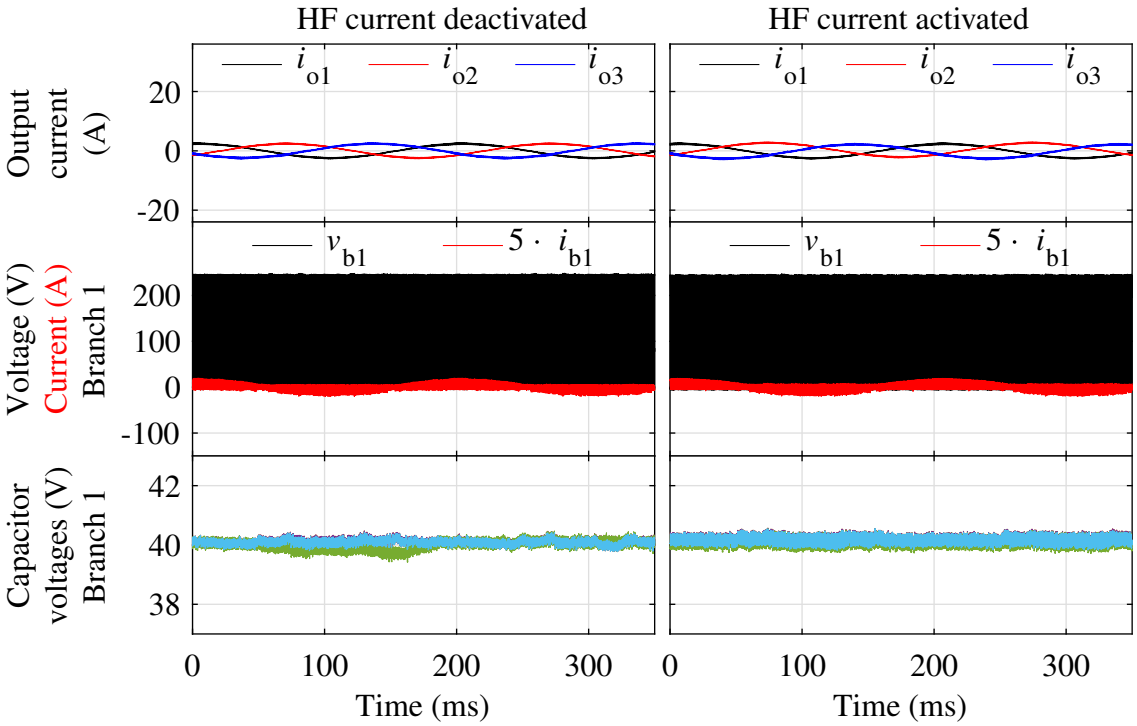


Figure 6.19: Measured data of a quasi-two-level PWM-operated downscaled converter prototype using a fast proportional branch-energy control. The modulation index is $M = 0.1$. Left: the HF-current injection is deactivated, right: the HF-current injection is activated.

6.4 Operation with a Synchronous Machine

To test the converter prototype under dynamic conditions over a wide range of output frequencies, an experiment of synchronous machine acceleration is conducted. The experiment is applied to an available $50/3$ Hz synchronous machine (Figure 6.20) manufactured by *AEG* and rated at 220 V and 66 A, the parameters of which are listed in Table 6.3. The machine is driven by the converter prototype through a very long cable with an estimated length of approximately 40 meters. The rotor position is measured by a 17 bit magnetic absolute-position encoder *Baumer MHAP100 K5 SG17N*. The gray-coded data are transferred via two optical fibers using SSI protocol. During the first part of the experiments, the converter is fed from the 220 V central laboratory dc link. The converter control parameters are identical to those in Table 6.1. The machine control is described in Section 5.5.2.

For the measurements of machine acceleration, the logging system of *Protolar Supervisor* is utilized, since this is capable of tracking a large number of traces over a long period of time. The asynchronous sampling period is approximately 35 µs.

Figure 6.21 depicts the results of the machine acceleration experiment using fast proportional branch-energy control. The same experiment is repeated for the predictive energy control with the corresponding results in Figure 6.22. In both cases, the machine is accelerated with a constant current of 20 A, representing the MMC's maximum. The converter remains stable during the whole acceleration process and the module capacitor voltages are kept within the defined limits. As a result, the figures confirm the feasibility of quasi-two-level PWM-operated MMCs as a machine drive.

Figure 6.20: 50/3 Hz synchronous machine used for tests of the downscaled MMC prototype.

Table 6.3: Parameters of the synchronous machine used for the investigations.

Rated stator voltage	V_{sN}	220 V
Rated stator current	I_{sN}	66 A
Rated stator frequency	f_{sN}	50/3 Hz
d-axis inductance	L_d	11 mH
q-axis inductance	L_q	5 mH
Stator resistance	R_s	0.35 Ω
Field-linked direct axis flux linkage	$\Psi_{f,d}$	1.91 Vs
Pole pairs	p	2
Rotational inertia	J	6 kg m^2

Comparing the performance of the fast proportional branch-energy control and the predictive branch-energy control, it can be observed that they have a small impact on the machine-control behavior, thus not influencing the machine currents. While the predictive branch-energy control manages the balancing of module capacitors better when the output currents are high, the module voltage variation is lower using the fast proportional branch-energy control when the output currents are low. Furthermore, the module voltage variation is almost the same for the high output currents as for the low output currents when predictive branch-energy control is applied. The main reasons for this rather unexpected occurrence are the non-matching current ratings of the machine and the converter. Consequently, the machine inductance is relatively low and the current ripple is very high, compared to the rated converter current. Since predictive energy control assumes that the output current will not change significantly during a PWM period, performance is diminished when the output current ripple is too high. If the machine ratings match the converter ratings, the predictive branch-energy control is expected to perform better and is generally the preferable choice. This is confirmed by simulations conducted for an MMC matched for the applied machine in Appendix D.

Since the machine is fed from the converter through a long cable, the reflections at the end of the machine cable are of interest. Figure 6.23 shows the measured line-to-line voltages directly at

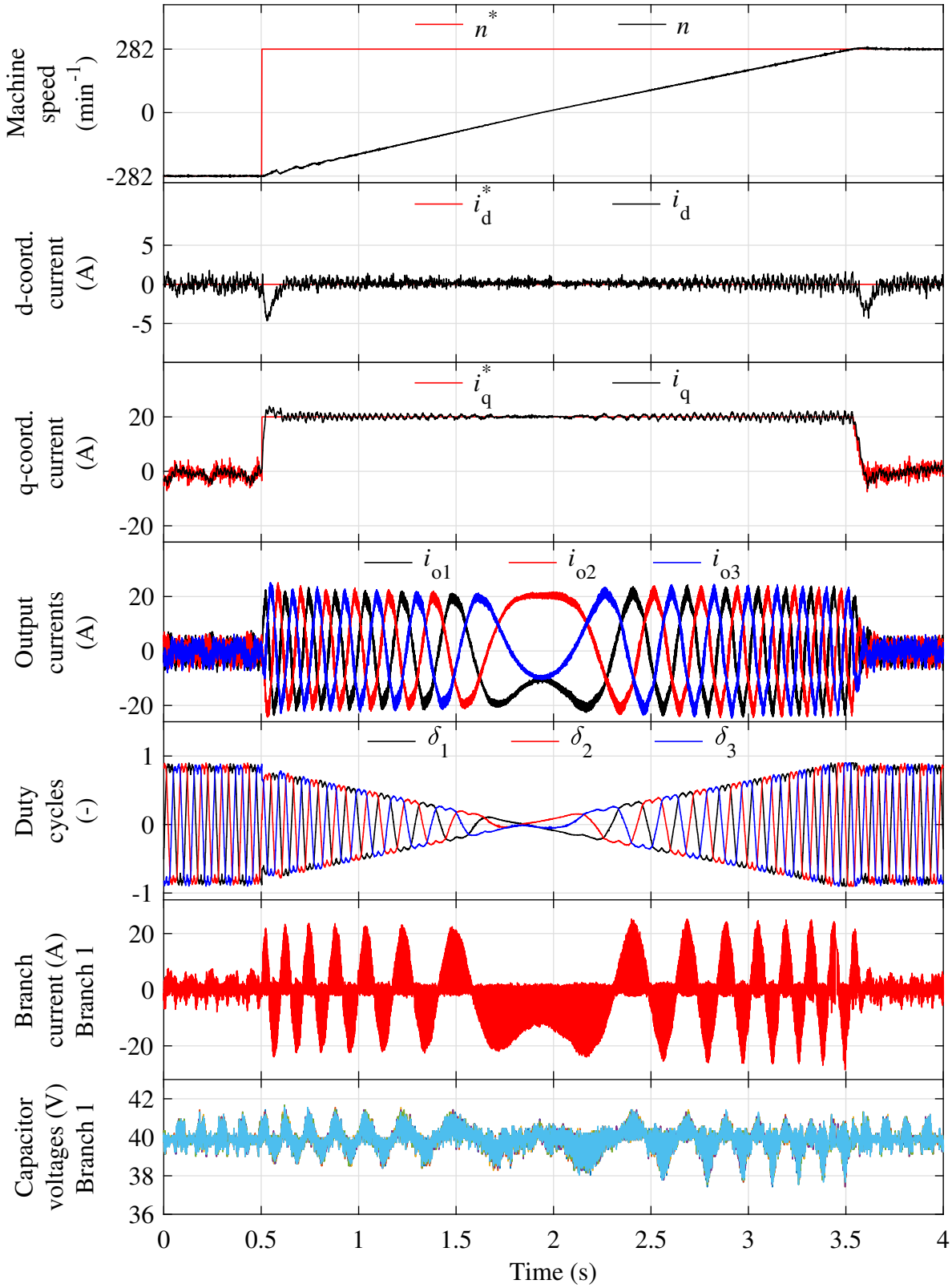


Figure 6.21: Measured waveforms of the quasi-two-level PWM operated MMC prototype driving a synchronous machine. **Fast proportional branch-energy control** is applied.

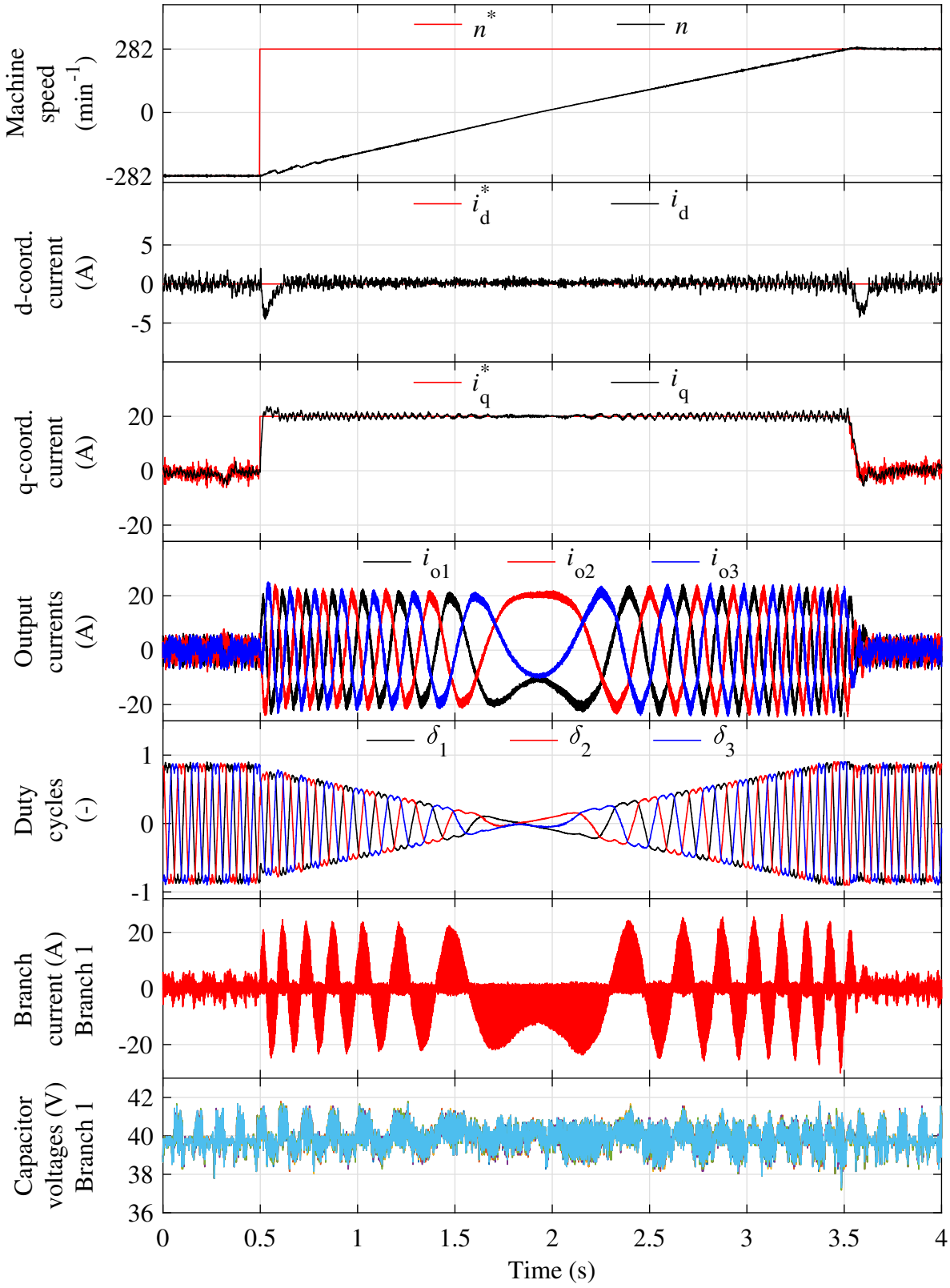


Figure 6.22: Measured waveforms of the quasi-two-level PWM operated MMC prototype driving a synchronous machine. **Predictive branch-energy control** is applied.

the converter output and at the machine terminals. At the converter terminals, a quasi-two-level waveform can be observed, representing a typical two-level PWM waveform with superimposed pulses caused by HF modulation. By examining the line-to-line voltage measured directly at the machine terminals, an overvoltage of a few percent can be found. This is caused by the voltage reflections. Since the quasi-two-level waveform is applied, the voltage reflections have an amplitude of only a single module capacitor voltage. Note that the measurements at the converter terminals and at the machine terminals are not synchronized but are measured subsequently at the same machine speed.

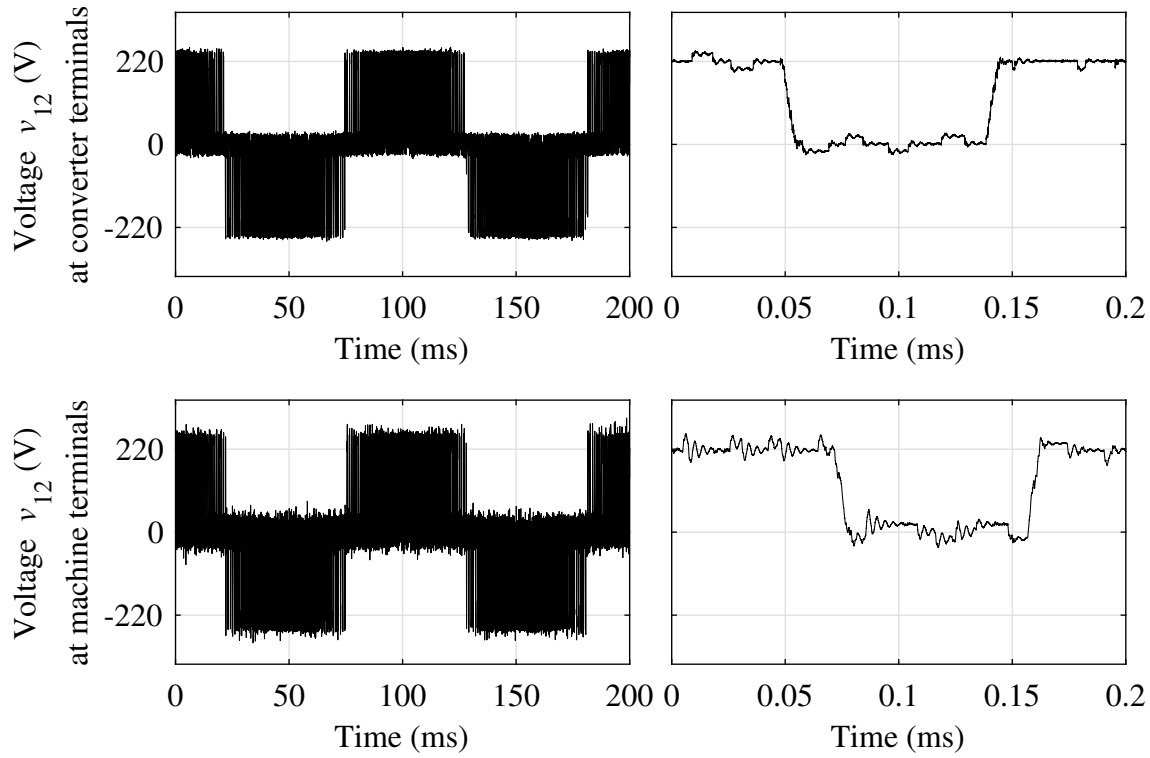


Figure 6.23: Waveforms of line-to-line voltage between phases 1 and 2: top) measured at the converter terminals, bottom) measured at the machine terminals. On the right side of the figure, the detailed view of the left waveforms is plotted. The MMC is operated in quasi-two-level PWM operation with predictive branch-energy control. The converter is fed from a 220 V central laboratory dc link. The measurements at converter and machine terminals are not synchronized.

To evaluate the improvement of the cable reflections, an additional experiment is conducted, comparing the quasi-two-level PWM-operated MMC to a standard IGBT-based two-level VSI. The VSI comprises IGBT module *Infineon IFS150V12PT4* of the intelligent power module series, integrating six independent IGBTs rated at 1200 V and 150 A. Both converters are fed by the same 110 V central laboratory dc link and use the same control algorithms. The dc-link voltage is lowered, since overvoltages are expected with two-level VSI, which could possibly destroy the machine's insulation. The same machine and cable are used as in the previous experiment. The results of the experiment are plotted in Figure 6.24. Note that similarly to the previous experiment, the measurements at the converter terminals are not synchronized with those at the machine terminals.

Figure 6.24 shows that the two-level VSI leads to significantly higher voltages at the machine

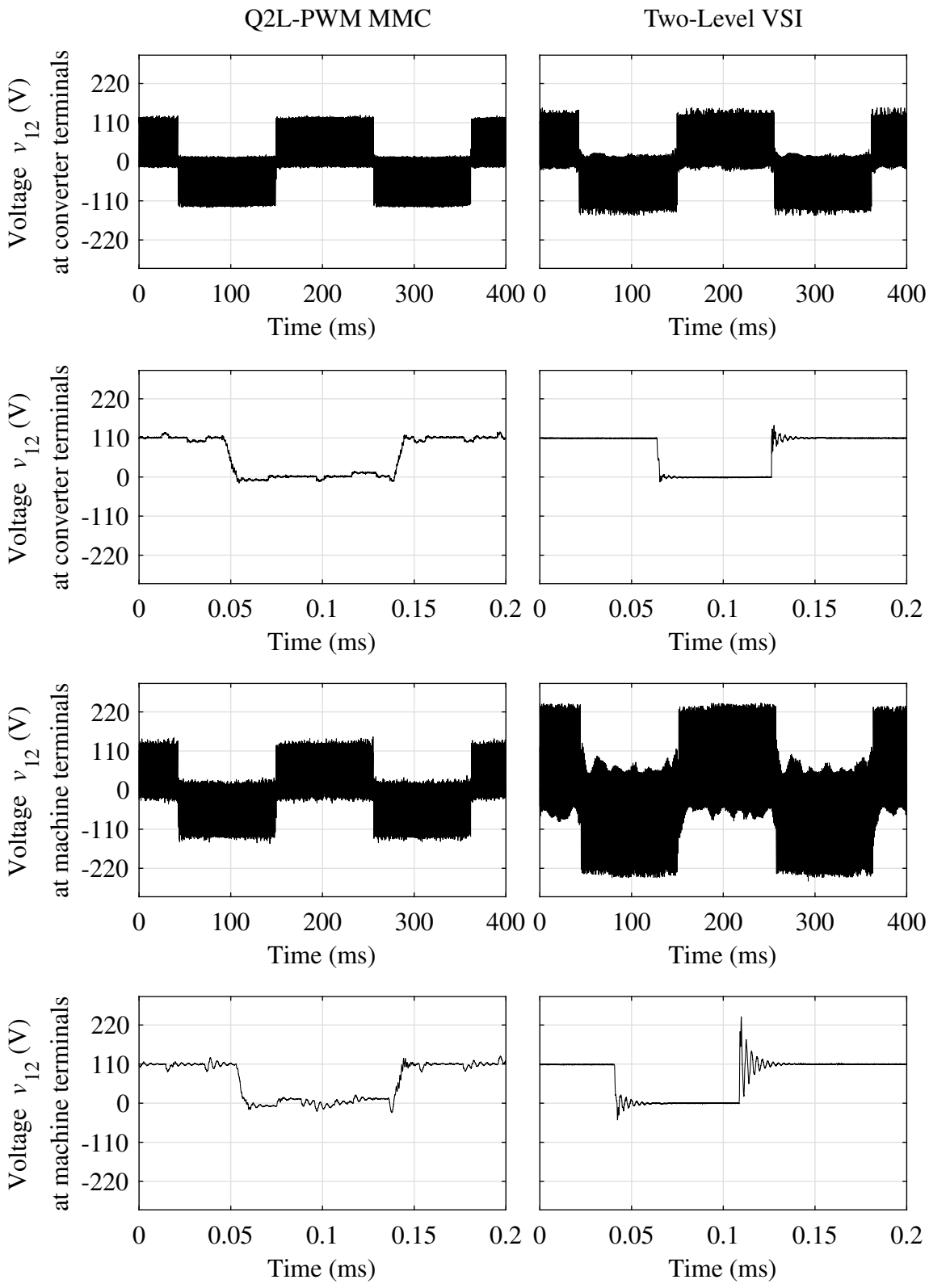


Figure 6.24: Waveforms of line-to-line voltage between phases 1 and 2: top) measured at the converter terminals, bottom) measured at the machine terminals, left) quasi-two-level PWM-operated MMC, right) two-level VSI. The second and fourth row show the detailed view of the first and third row. The MMC is operated in quasi-two-level PWM operation with predictive branch-energy control. Both converters are fed from a 110 V central laboratory dc link. The measurements at converter and machine terminals are not synchronized.

terminals than the quasi-two-level PWM-operated MMC. This is due to the fact that the quasi-two-level PWM operation changes the output voltage step-wise and thus the influence of the cable reflections is diminished. This figure confirms one of the key advantages of quasi-two-level PWM operation, which is the mitigation of the cable-reflection problems typical for converters with series connected IGBT switches.

6.5 Parameter Sensitivity Study

It is a well-known fact that both the dead-beat control and the predictive control rely strongly on the knowledge of the system parameters. To evaluate the influence of imprecisely estimated parameters on the converter control, a short study based on simulations is performed. Since the predictive branch-energy control is expected to be more parameter sensitive, only this control method is investigated. The study is performed for an up-scaled converter system (scaled by a factor of 25 for both currents and voltages), representing a more realistic medium-voltage converter. Since medium-voltage converters generally have lower resistances, the branch resistance is decreased. The altered parameters can be found in Table 6.4. The rest of the parameters remain unchanged from those used in Table 6.1. For the study, a passive load is applied with an output inductance $L_\mathrm{o} = 13$ mH, chosen as in previous experiments, and the output resistance is chosen to achieve an output current amplitude of $\hat{i}_\mathrm{o} = 500$ A for modulation index $M = 0.9$. The output frequency is $f = 5$ Hz.

Table 6.4: Parameters used for the parameter sensitivity study differing from Table 6.1.

Peak output current	$\hat{i}_\mathrm{o}$	500 A
Leg inductance (coupled)	L_leg	210 µH
Setpoint module capacitor voltage	V_C^*	1000 V
HF current amplitude	$\hat{i}_\mathrm{HF}$	7.5 A (smart)
HF current threshold	$I_\mathrm{c,thr}$	3.75 A (smart)
Branch resistance	R_b	20 mΩ

Taking a closer look at the dead-beat controller, determined by (5.11), and the prediction of the compensating current, determined by (5.8), one can estimate that the performance of the current controller is dependent on the precise knowledge of the leg inductance L_leg and the branch resistance R_b, fast measurement of the branch currents, and the ability to set the branch voltages v_bA and v_bB precisely. The ability to set the voltages precisely is influenced by several factors, such as the bandwidth of the module capacitor voltage measurements and the dead-times[2)] of the internal switches within the module. Furthermore, the predictive part of the branch-energy controller also relies on the precise knowledge of the leg inductance [see Section 5.3.2]. In the following sections, the sensitivity to these parameters is briefly investigated and discussed.

6.5.1 Sensitivity to Estimated Leg Inductance

Although the control is expected to be very sensitive to the correct estimation of the leg inductance, this is not necessarily a problem, since this inductance is determined by the installed

[2)] Also called interlock time.

branch inductors, which are an internal part of the converter. Thus, the inductance can be measured apriori.

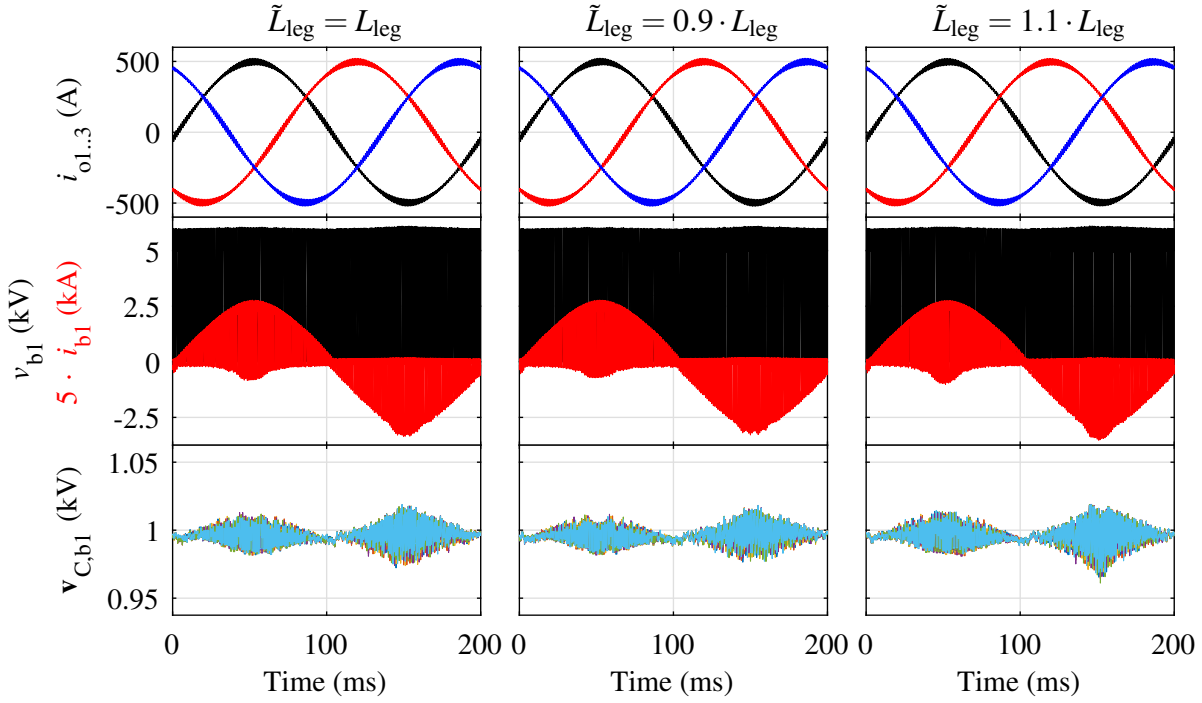


Figure 6.25: Sensitivity of the controller performance of the quasi-two-level PWM-operated MMC to the estimated value of the **leg inductance** $\tilde{L}_{\text{leg}}$ utilized by the controllers. $i_{\text{o1..3}}$ are the output currents. v_{b1} and i_{b1} are the branch voltage and the branch current of Branch 1. $\mathbf{v}_{C,\text{b1}}$ is a vector of all module capacitor voltages of Branch 1.

In Figure 6.25, the converter waveforms are plotted for different estimated values of the leg inductance $\tilde{L}_{\text{leg}}$ used in the control. In the first column, the waveforms are presented for the scenario when the leg inductance is estimated correctly. In the second column, the leg inductance is estimated 10 % lower. In the third column, the leg inductance is estimated 10 % higher. As can be seen, even the relatively high estimation error leads to acceptable results and the converter stability is hardly influenced.

Estimating the leg inductance at a lower value causes the predicted branch current to be overestimated during `TRANSITION STATE`, and thus the value has to be corrected during `STATE A` and `STATE B` with the dead-beat controller. The dead-beat controller causes slight branch current overshoots and the controlled current oscillates around the setpoint value. This means that in the case of estimating the leg inductance too low, the two effects partly compensate each other.

In contrary, if the leg inductance is estimated too high, a branch current overshoot occurs during the `TRANSITION STATE`, since the current is estimated too low. The dead-beat controller applied during `STATE A` and `STATE B` is not capable of removing the remaining deviation between the setpoint and measured current value. The combination of these two effects represents a non-linearity for the branch-energy control, the performance of which is diminished. Consequently, this leads to increased variation of the module capacitor voltages.

An interesting occurrence, which can be observed in Figure 6.25, is that both the module capacitor voltage variation and the maximum branch currents are slightly lower when the leg

inductance is underestimated than when it is estimated correctly. One of the explanations for this occurrence is that the assumptions and simplifications for the prediction of the branch energy deviation used in Section 5.3.2 lead to a slightly higher value. Nevertheless, this error is most likely dependent on the operating point and the converter design. In general, a lower estimated branch inductance means that the predicted branch energy deviation is also lower and a larger part has to be compensated by the closed-loop branch energy proportional controller.

In conclusion, the simulations show that it is preferable to slightly underestimate the leg inductance rather than to overestimate it to improve the converter behavior.

6.5.2 Sensitivity to Estimated Branch Resistance

The second parameter which has to be estimated is the branch resistance. In practical applications this is significantly harder to estimate than the leg inductance, since the value is very small and non-linear due to the characteristics of the semiconductor switches installed in the modules.

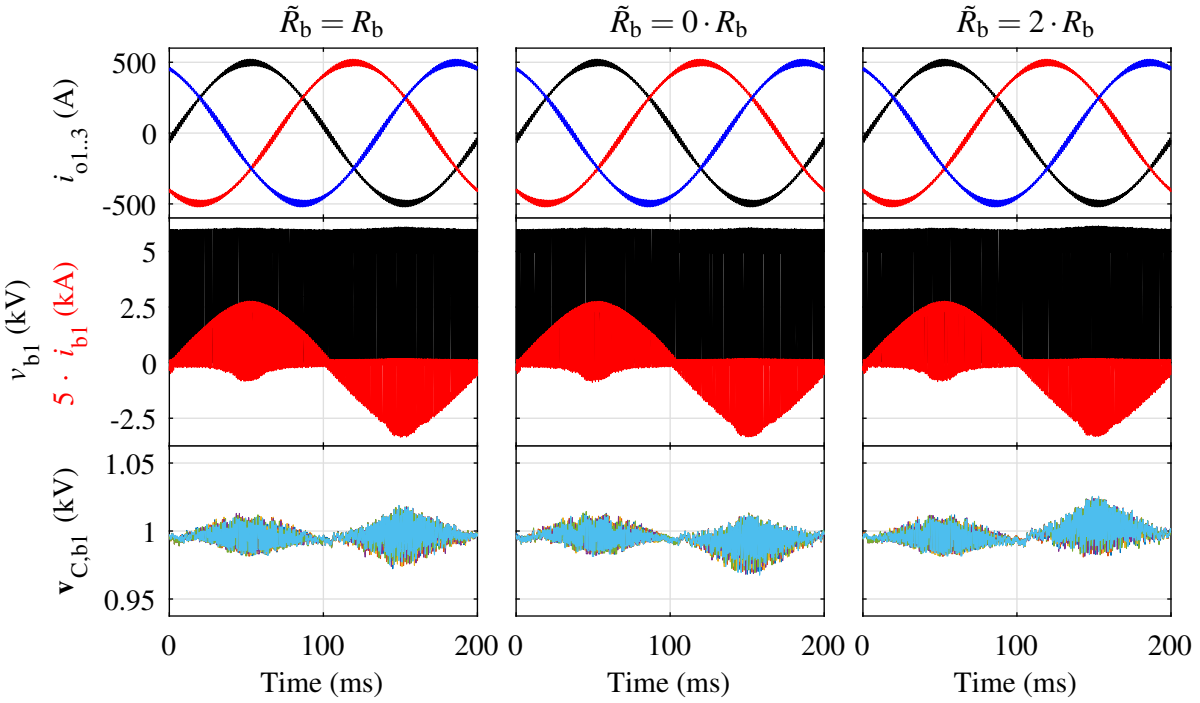


Figure 6.26: Sensitivity of the controller performance of the quasi-two-level PWM-operated MMC to the estimated value of the **branch resistance** $\tilde{R}_b$ utilized by the controllers. $i_{o1..3}$ are the output currents. v_{b1} and i_{b1} are the branch voltage and the branch current of Branch 1. $\mathbf{v}_{C,b1}$ is a vector of all module capacitor voltages of Branch 1.

Nevertheless, the low value is also an advantage, since the impact of an incorrect estimation is not critical. In Figure 6.26, the same converter waveforms as in the previous case are shown for different values of estimated branch resistance. The first column of the figure shows the scenario in which the branch resistance is estimated correctly. In the second column, the branch resistance is simply assumed to be zero. In the third column, the branch resistance is overestimated by a factor of two. As can be observed in the figure, even a very incorrect estimation of the branch resistance leads to acceptable controller performance.

Since the estimated branch resistance value is used in the dead-beat controller during `STATE A` and `STATE B`, its incorrect value causes a small remaining deviation between the setpoint value and the measured value of the compensating current. Taking a closer look at Figure 6.26, it can be observed that the module capacitor voltage variation in Branch 1 is more severe when duty cycles are negative (when the output current is negative). This is caused by the fact that the setpoint compensating current is generally lower for low duty cycles, and thus the relative error of the compensating current, caused by the incorrectly estimated branch resistance value, is significantly higher. Consequently, this leads to higher module capacitor voltage variation in Branch 1.[3)]

6.5.3 Sensitivity to Variation of Installed Module Capacitance

The next investigated effect is the sensitivity of the control to the variation of the installed module capacitance. In this experiment, the capacitance of the first module in Branch 1 is chosen differently than in the other modules. This can either happen in the production, mostly within a specified tolerance – e.g. ±5 %, or due to a failure caused by aging.

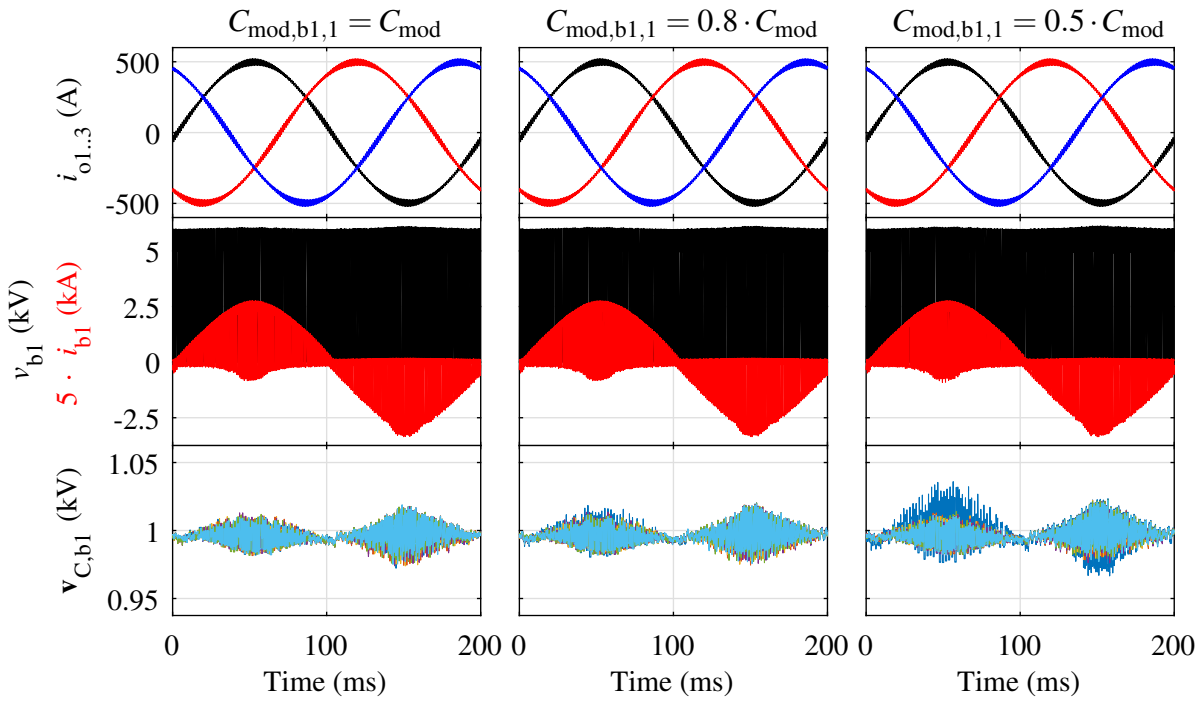


Figure 6.27: Sensitivity of the controller performance of the quasi-two-level PWM-operated MMC to deviation of the **module capacitance** of the first module in Branch 1 $C_{\mathrm{mod,b1,1}}$ from its designed value C_{mod}. $i_{\mathrm{o1..3}}$ are the output currents. v_{b1} and i_{b1} are the branch voltage and the branch current of Branch 1. $\mathbf{v}_{C,\mathrm{b1}}$ is a vector of all module capacitor voltages of Branch 1. The voltage of the first module is plotted in dark blue.

In Figure 6.27, three scenarios are plotted: the capacitance of the first module being exactly the same as that of other modules (first column), the capacitance of the first module being reduced by 20 % (second column) and the capacitance being reduced by 50 % (third column). Beside

[3)] Please note that the situation is similar in Branch 2. However, the effect is more severe for positive duty cycles when compensating current in this branch is lower.

the module capacitor voltage varying more significantly than that of the other modules, there is almost no effect on the current control observable in the figure.

Regarding the MMCs in general, an incorrect value of capacitance in one module causes two effects: First, the setpoint number of inserted modules calculated according to the mean value of module capacitor voltage can lead to a wrong branch voltage value, since the module capacitor voltages within a branch are not balanced. Second, the distribution of the losses will be worse, since a module with a lower capacitance is inserted for a shorter time (to balance the module capacitor voltages). Nevertheless, both of these effects are weak with quasi-two-level PWM operation, because either almost all modules are inserted or all modules are short-circuited. Thus, the relative error by a calculation of setpoint number of inserted modules is rather small and the module with lower capacitance is effectively forced to be inserted and switched almost as frequently as other modules, leading to an almost equal distribution of losses.

6.5.4 Sensitivity to Measurement Bandwidth

In the following study, the sensitivity of the control to the bandwidth of the measurements is investigated. For the sake of the investigation, the module capacitor voltages and the branch currents are low-pass filtered before entering the converter control block, modeling the limited bandwidth of the measurements. This simplified model uses a first-order low-pass filter with a cutoff frequency of f_{LP}.

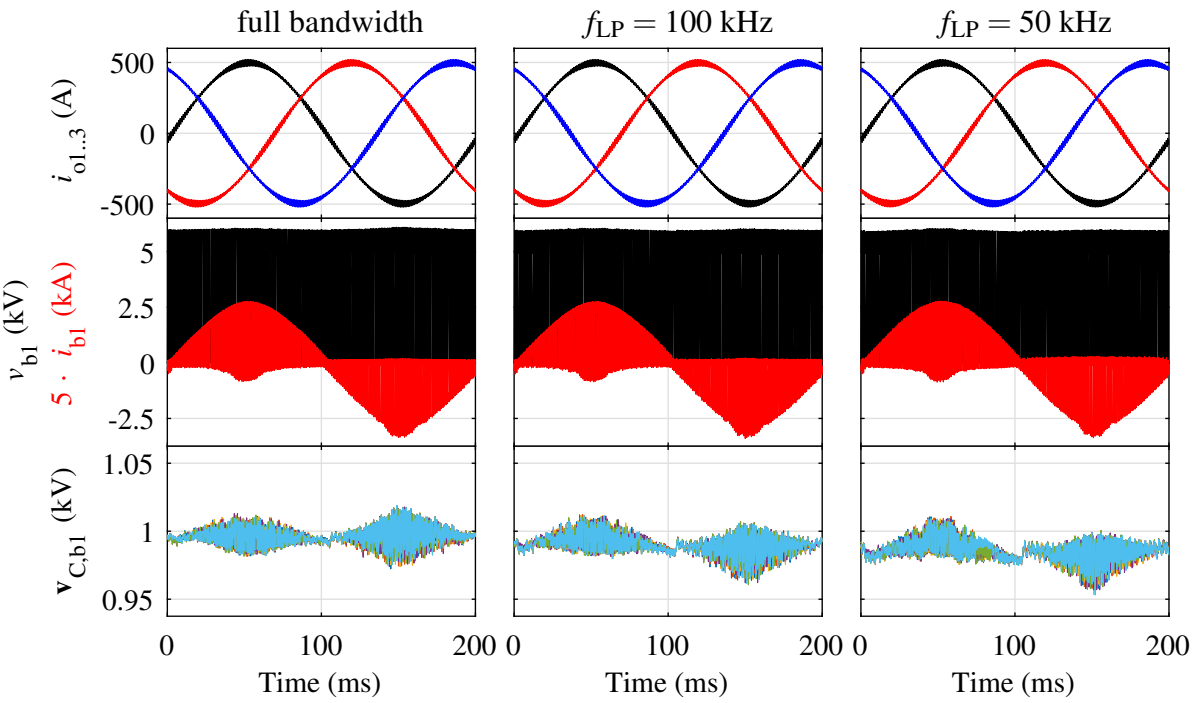


Figure 6.28: Sensitivity of the controller performance of the quasi-two-level PWM-operated MMC to the **bandwidth of the branch current measurement and the module capacitor voltage measurement**. The measurement bandwidth is modeled with a first-order low-pass filter with a cutoff frequency of f_{LP}. $i_{\mathrm{o1..3}}$ are the output currents. v_{b1} and i_{b1} are the branch voltage and the branch current of Branch 1. $\mathbf{v}_{C,\mathrm{b1}}$ is a vector of all module capacitor voltages of Branch 1.

Since the leg-current control is based on dead-beat and predictive controllers, it relies on a correctly measured value with a low delay. Consequently, if a considerable delay is introduced to the measurements, the current is not controlled correctly to its setpoint value anymore. This represents a non-linearity for the branch-energy controller, the performance of which is diminished. Although the bandwidth of the measurements has a significant impact on the current control performance for the scenarios with limited bandwidth in Figure 6.28, the module capacitor voltages are still controlled sufficiently by the closed-loop branch-energy controller. Nevertheless, the controlled module capacitor voltages have a remaining control deviation from their setpoint value.

Moreover, if the measurement bandwidth is too low, it can diminish the capability of the module capacitor voltage balancing within a branch, since the branch current direction might not be estimated correctly anymore. The estimation might be improved up to a certain level by increasing the injected HF current.

6.5.5 Sensitivity to Dead-Time of Module Switches

Figure 6.29 shows the influence of the dead-time for the modules' semiconductor switches on the converter control. Since the dead-time effect causes a very small voltage error, when the PWM frequency is relatively low, the converter control is hardly influenced. The output voltage error is further analyzed in Section 7.4.

In contrast, the dead-time effect has a more significant impact on the output voltage waveforms.

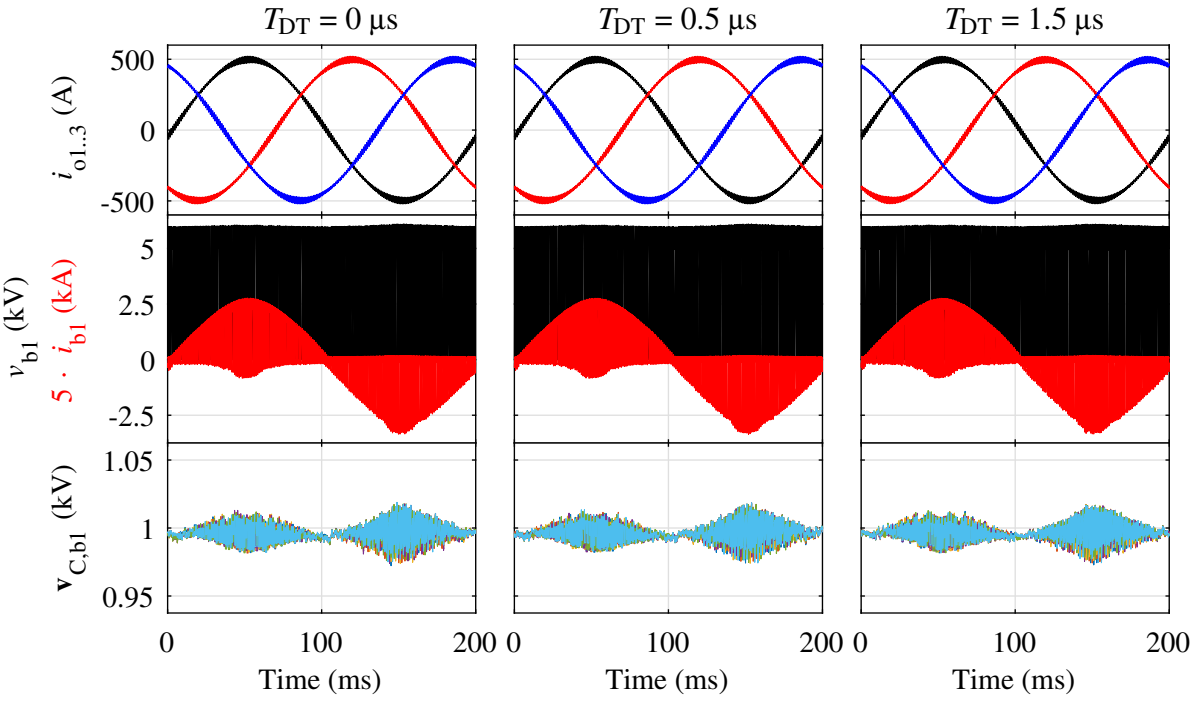


Figure 6.29: Sensitivity of the controller performance of the quasi-two-level PWM-operated MMC to the applied **dead-time** T_{DT} for the modules' switches. $i_{o1..3}$ are the output currents. v_{b1} and i_{b1} are the branch voltage and the branch current of Branch 1. $\mathbf{v}_{C,b1}$ is a vector of all module capacitor voltages of Branch 1.

As can be seen in Figure 6.30, the application of dead-time changes the waveform of the rising and falling edge of the output voltages. This happens when the branch current suddenly changes direction during the voltage transition and can even lead to additional voltage steps, which are undesired because they can excite the resonances within the machine and the cable. As demonstrated in the figure, the effect is stronger the longer the dead-time period is. As a general rule, the delay period of time T_d (in this case 1µs), applied to limit the $\mathrm{d}v/\mathrm{d}t$ of the output voltage, should be chosen to be longer than the dead-time period.

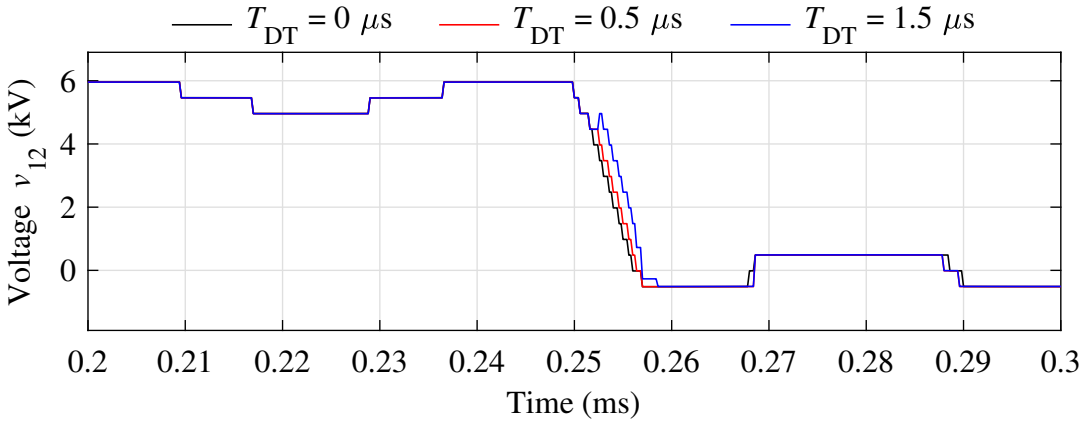


Figure 6.30: Imapct of the applied dead-time T_DT for the modules' switches on the line-to-line voltage between phases 1 and 2.

7 Further Analyses

This chapter analyzes further options for and properties of the quasi-two-level PWM-operated MMCs. The investigations presented here can be divided into three groups.

The first group studies the options to increase the modulation indices despite a limited maximum duty cycle value, which is specified during converter design. These options include the application of flat-top modulation (Section 7.1) and a reduction of output current with high modulation indices (Section 7.2).

The second group analyzes the effects resulting from non-idealities. These are the voltage-wave reflections occuring with long machine cables (Section 7.3) and the output voltage errors (Section 7.4).

The third group deals with the start-up of the converter when the module capacitors cannot be precharged directly with isolating transformers (Section 7.5).

In this chapter, several simulations are executed to validate the derived results. The converter parameters used for the validation are listed in Table 7.1. The parameters are similar to those used for the parameter sensitivity study in Section 6.5. The predictive branch-energy control is applied to the converter.

Table 7.1: Parameters of a medium-voltage quasi-two-level PWM-operated MMC used for validations in this chapter.

Peak output current	$\hat{i}_\mathrm{o}$	up to 500 A
Maximum allowed duty cycle	δ_max	0.9
Leg inductance (coupled)	L_leg	210 µH
Branch resistance	R_b	0 Ω
Modules per branch	n_mpb	6
Module capacitance	C_mod	200 µF
DC-link capacitance	C_i	250 µF or ∞
Input voltage	V_i	5.5 kV
Setpoint module capacitor voltage	V_C^*	1000 V
PWM frequency	f_PWM	1 kHz
HF modulation frequency	f_HF	25 kHz
Delay between switch. instants	T_d	1 µs
Energy controller gain	$G_{\mathrm{P},e}$	1200 $\frac{1}{\mathrm{s}}$
HF current amplitude	$\hat{i}_\mathrm{HF}$	0 A

7.1 Flat-Top Modulation

The flat-top modulation (FTM), also called "discontinuous modulation", is a well-known modulation technique for two-level VSIs. This modulation technique obtained its name due to its characteristic waveforms, depicted in Figure 7.1. The figure shows that each duty cycle waveform is either one or minus one for one third of the output period. As a consequence, the two-level VSI is not switched during these periods and the converter switching losses are significantly reduced. Nevertheless, another consequence is the higher distortion of the output current. In this section, application of flat-top modulation to the quasi-two-level PWM-operated MMCs is investigated.

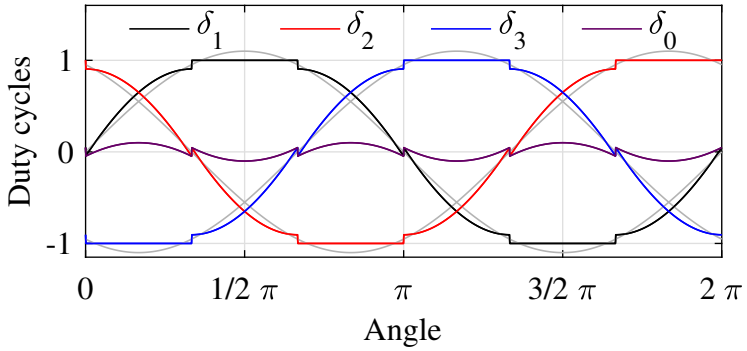


Figure 7.1: Example of the duty cycle waveforms when flat-top modulation is applied. The modulation index is $M = 1.1$. The gray lines represent the sinusoidal duty-cycle components δ_1', δ_2', and δ_3' without any common-mode component.

The common-mode component of the duty cycle for the FTM, depicted in Figure 7.1, can be calculated as:

$$\delta_0 = \text{sign}\left(\max\left(\delta_1', \delta_2', \delta_3'\right) + \min\left(\delta_1', \delta_2', \delta_3'\right)\right) \cdot \left(1 - \max\left(|\delta_1'|, |\delta_2'|, |\delta_3'|\right)\right) \quad . \tag{7.1}$$

Note that there are other modified versions of this technique, where the position of the "flat top" is shifted according to the output current, since the switching losses are highest at the peak of the output current [139]. Since the method according to (7.1) increases the achievable modulation index most significantly, the other versions will not be considered here.

One drawback of quasi-two-level PWM operation, described in Section 4.2, is the limited maximum achievable duty cycle. The limitation depends on the selected design parameters and is necessary to provide sufficient time for the compensation of branch power peaks, which occur during `TRANSITION STATE`. However, Section 3.2 states that the duty cycle δ being exactly 1 or -1 is not a problem, since the branch power peaks do not occur if switching between `STATE A` and `STATE B` is not required. This makes practical application of the FTM possible and even advantageous.

In Figure 7.2 the maximum required duty cycle (excluding the duty cycle being exactly one) is plotted as a function of the modulation index for sine modulation (SM), space vector modulation (SVM), and FTM. The SM (basically no injection) and the SVM were defined in Section 5.5.1.

Figure 7.2 shows that the maximum duty cycles of SM and SVM increase linearly with the modulation index. With SM, the modulation index is limited to the same value as the maximum achievable duty cycle. The SVM is capable of increasing this modulation index by a factor

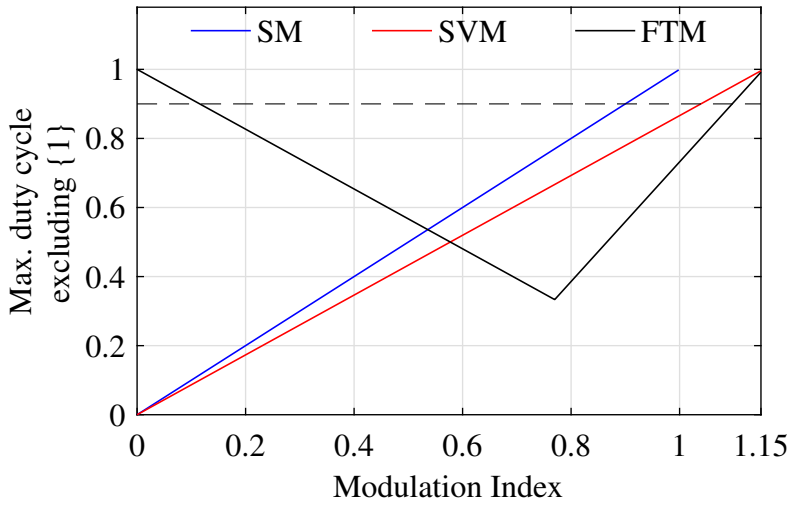


Figure 7.2: Maximum required duty cycle (exluding the duty cycle being exactly one) versus the required modulation index for sine modulation (SM), carrier-based space vector modulation (SVM), and flat-top modulation (FTM). The dashed line represents an example limitation of the maximum achievable modulation index being $\delta_{\max} = 0.9$.

of ≈ 1.15 for each chosen maximum achievable duty cycle. This is different for FTM. The maximum required duty cycle is very high for low modulation indices. This is caused by the relatively high common-mode component δ_0. The higher the modulation index is, the lower the common-mode component δ_0 becomes. Consequently, the required duty cycle also decreases up to $M \approx 0.77$. At this point, the first harmonic becomes dominant for the maximum required duty cycle and the maximum required duty cycle increases until it reaches 1. This means that not only is the maximum modulation index limited, but that there is also a limitation for the minimum achievable modulation index when FTM is applied. On the other hand, Figure 7.2 also shows that with FTM, even higher modulation indices are achievable than with SVM. For instance, if the maximum achievable duty cycle is limited to $\delta_{\max} = 0.9$ (the limit is marked with a dashed line in Figure 7.2), the maximum achievable modulation index of FTM is approximately 1.1, while with SVM only ≈ 1.05.

If FTM is applied to quasi-two-level PWM operation directly without any additional measures, a large disturbance of the module capacitor voltages occurs. This case is depicted in Figure 7.3a and the disturbance is visible near 170 ms. The cause of the disturbance can be explained using Figure 7.4a. As can be seen in that figure, the flat-top modulation causes two branch power peaks during a single PWM period after the duty cycle was minus one [see fifth period in Figure 7.4a]. Consequently, the branch energy disturbance, visible at the module capacitor voltages in Figure 7.3a, is doubled.

Taking a closer look at Figure 7.4a, it can be observed that with a non-inverted PWM carrier, branch voltage v_{bA} is first low, then high, and then low again, during each respective PWM period. Branch voltage v_{bB} is first high, then low, and then high again. Nevertheless, if the duty cycle is minus one, branch voltage v_{bA} is continuously high and branch voltage v_{bB} is continuously low. As a consequence, there is one additional transition from high to low in Branch A and from low to high to low in Branch B, once the duty cycle is no longer minus one. While this additional power peak could be compensated for in Branch A shortly before the switching, compensation in Branch B is first possible after the branch energy disturbance has occurred.

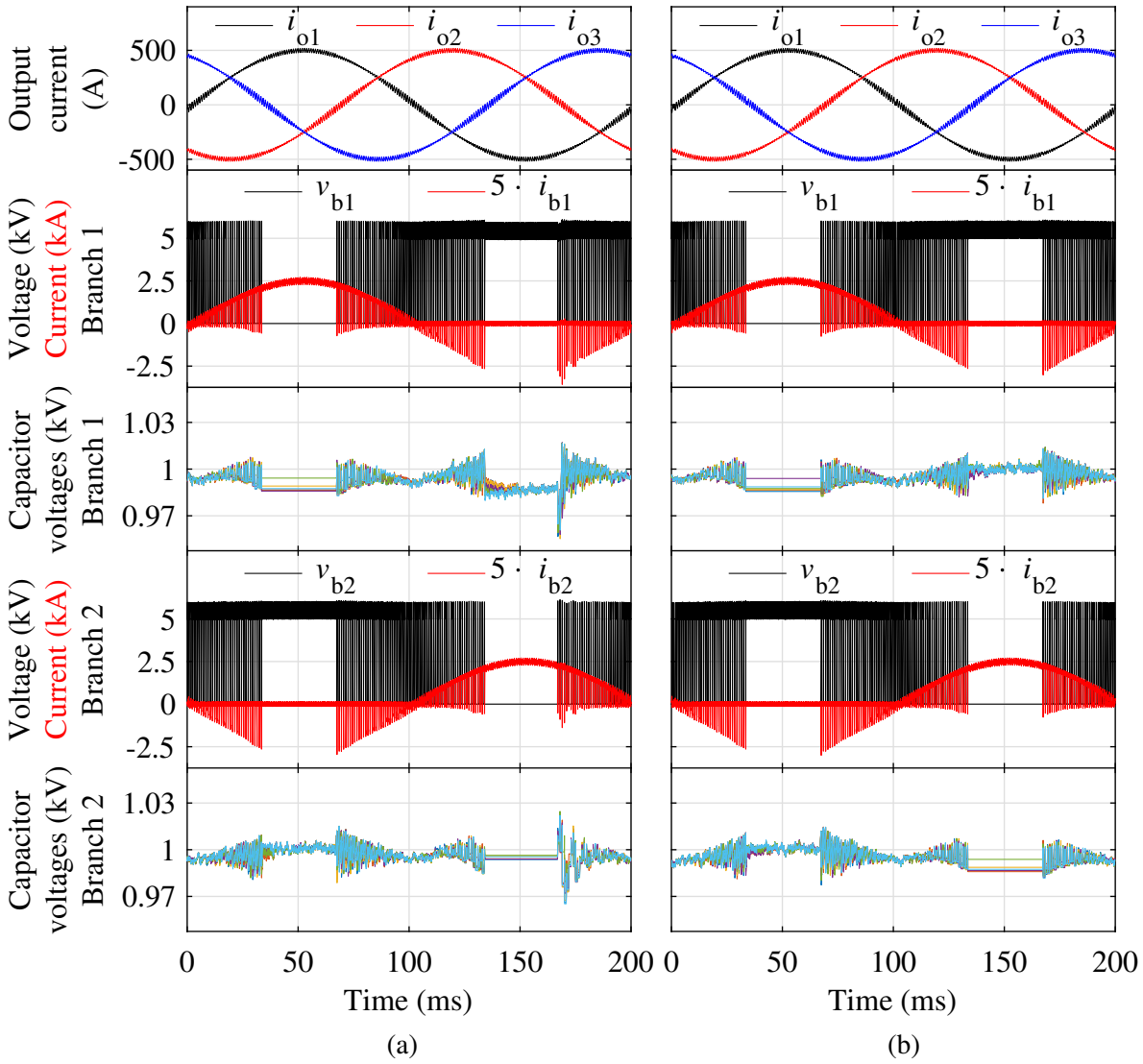


Figure 7.3: Simulated data of a quasi-two-level PWM-operated MMC with flat-top modulation feeding a passive load. a) the carrier is non-inverted, b) the carrier is inverted when duty cycle δ' is negative. The modulation index is $M = 1.1$, the output frequency is $f = 5$ Hz, and the output current amplitude is $\hat{i}_o = 500$ A. The output inductance is $L_o = 13$ mH. The converter parameters are listed in Table 7.1. Predictive energy control was applied.

A possible solution to this problem is to invert the carrier for negative duty cycles, as depicted in Figure 7.4b. This way, during each PWM period the voltage patterns are high-low-high in Branch A and low-high-low in Branch B, and thus the duty cycle being minus one no longer causes additional power peaks anymore. The PWM carrier must be non-inverted during the positive duty cycles, since the inverted carrier would cause additional branch energy disturbance after the duty cycle was one. The validity of the proposed carrier inverting is proven by a simulation in Figure 7.3b. Additionally, the flat-top modulation (applying the proposed inversion of carriers) with quasi-two-level PWM operation is also validated using a down-scaled MMC prototype in Section 6.2.3.

It is important to note that the switch-over between the inverted and non-inverted carriers causes an additional branch voltage transition and thus also branch energy disturbance. Consequently, if low power factors are also necessary, the switch-over could be applied while the output current

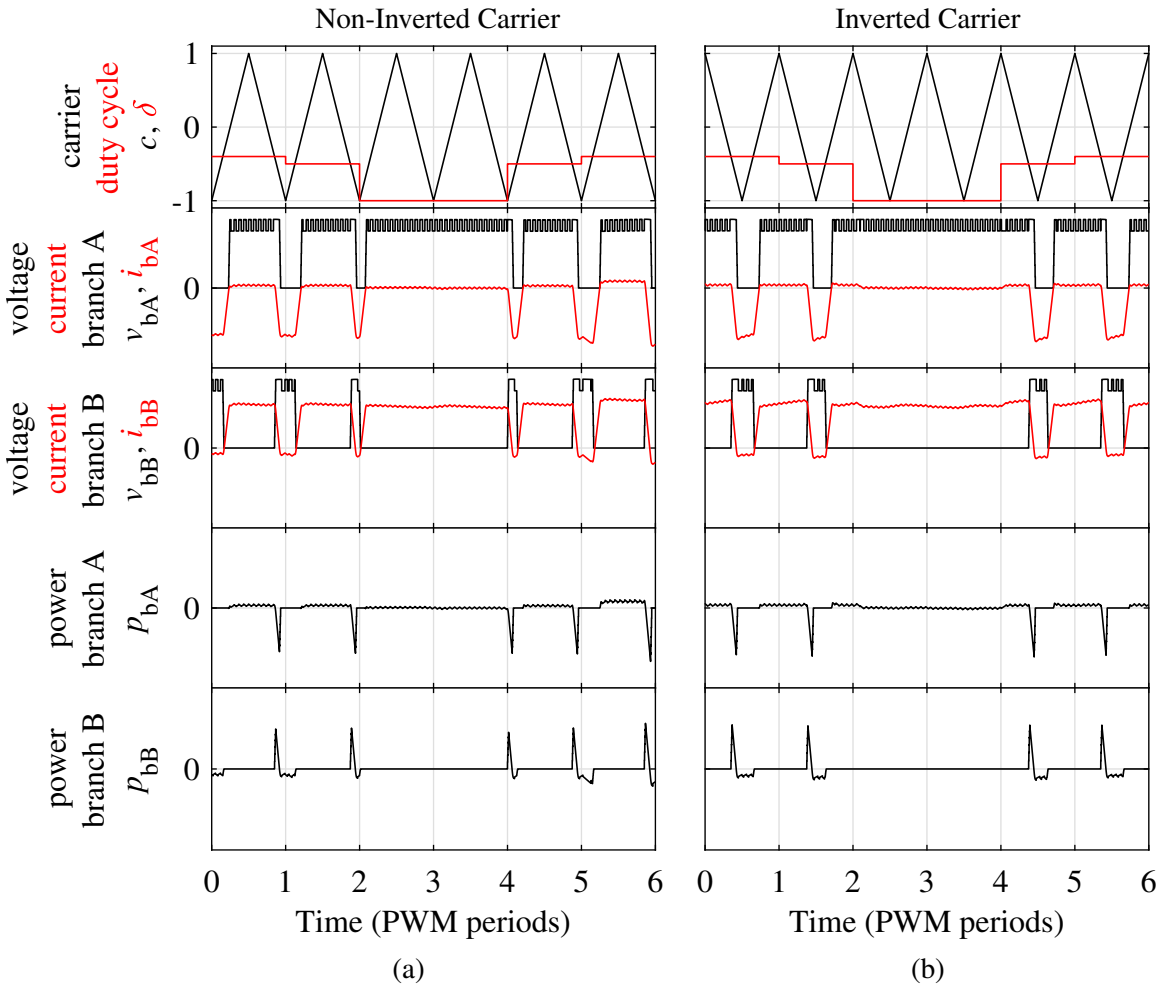


Figure 7.4: Explanation of the branch-energy disturbance caused by FTM during negative duty cycles: a) the carrier is non-inverted, b) the carrier is inverted.

is zero, instead of being dependent on the sign of the duty cycle. Another option would be to apply the switch-over while the duty cycle is one or minus one, and thus not generating any additional switching. Nevertheless, this would make the transition from SVM or SM to FTM more complex.

An application of the common-mode voltage injection techniques for quasi-two-level PWM operation is investigated comprehensively in [140, 141]. In addition to the investigations presented in this section, the influence of the injection techniques on the converter losses was also evaluated. The results from [140, 141] show that FTM signficantly reduces the losses in the modules. Moreover, the branch energy variation and the module capacitor currents are also lower with FTM as long as the output power factor is high enough, because in this method the maximum output current does not appear simultaneously with the maximum duty cycle (excluding $\delta = 1$). The increased distortion of the output currents with FTM was also confirmed in the paper.

In conclusion, FTM can be used optionally for a given MMC design above a particular modulation index to reduce the converter losses and to increase the achievable modulation index, as long as the additional output current distortion is acceptable.

7.2 Output Current Reduction for Duty Cycles Above the Designed Maximum

In Section 4.2 the design trade-offs were discussed and evaluated. One of the design parameters is the maximum peak output current, which has to be achievable at the maximum duty cycle. However, this also means that if the output current of an existing converter is decreased, the maximum duty cycle can be increased. In this section this option is investigated.

Using (4.13), the maximum achievable current

$$\hat{i}_\mathrm{o} = \sqrt{\frac{1-\delta_\mathrm{max}}{f_\mathrm{PWM}} \cdot V_\mathrm{i} \cdot \frac{I_\mathrm{b,c,max}}{L_\mathrm{leg}}} - \frac{2 \cdot I_\mathrm{b,c,max}}{1+\delta_\mathrm{max}} \tag{7.2}$$

can be expressed as a function of the following design parameters: PWM frequency f_PWM, input voltage V_i, and leg inductance L_leg. The duty cycle is an independent variable and the compensating current is a degree of freedom, since its value can be chosen to maximize the output current.

The maximum achievable output current for different duty cycles can be determined by searching the compensating current, at which the maximum of (7.2) occurs:

$$\frac{\mathrm{d}\hat{i}_\mathrm{o}}{\mathrm{d}I_\mathrm{b,c}} = 0 \quad . \tag{7.3}$$

This yields the optimum value for the compensating current

$$I_\mathrm{b,c} = \frac{(1-\delta)\cdot(1+\delta)^2}{16 \cdot f_\mathrm{PWM}} \cdot \frac{V_\mathrm{i}}{L_\mathrm{leg}} \quad , \tag{7.4}$$

at which the maximum current is achieved. Finally, substituting (7.4) into (7.2), the maximum achievable output current

$$\hat{i}_\mathrm{o} = \frac{1-\delta^2}{8 \cdot f_\mathrm{PWM}} \cdot \frac{V_\mathrm{i}}{L_\mathrm{leg}} \tag{7.5}$$

can be determined as a function of the duty cycle.

Nevertheless, the optimized solution for the maximum achievable current can lead to a higher peak branch current

$$\hat{i}_\mathrm{b} = \hat{i}_\mathrm{o} + I_\mathrm{b,c} \tag{7.6}$$

than the one the converter was designed for. In this case, the semiconductor losses would be too high. Moreover, the branch energy variation would also exceed its designed limits, since the branch energy variation is directly proportional to the squared value of the maximum branch current [see (4.6)]. To solve this problem, (7.6) can be substituted into (7.2) for the compensating

current, leading to the expression of the maximum achievable output current

$$\hat{i}_\mathrm{o} = \frac{2}{1-\delta} \cdot \left(\hat{i}_\mathrm{b} - \frac{(1+\delta)^2}{4} \cdot \frac{V_\mathrm{i}}{L_\mathrm{leg} \cdot f_\mathrm{PWM}} \right) + \frac{1+\delta}{1-\delta} \cdot \sqrt{\left(\frac{1+\delta}{2} \cdot \frac{V_\mathrm{i}}{L_\mathrm{leg} \cdot f_\mathrm{PWM}} \right)^2 - (1+\delta) \cdot \frac{V_\mathrm{i}}{L_\mathrm{leg} \cdot f_\mathrm{PWM}} \cdot \hat{i}_\mathrm{b}} \quad (7.7)$$

as a function of the maximum branch current.

For practical applications, the optimized solution according to (7.5) should be tested for the chosen duty cycle in the first step to establish whether the branch current, determined by substituting (7.4) and (7.5) into (7.6), will exceed its maximum. If this is not the case, the calculated output current can be applied. Otherwise, the output current should be calculated according to (7.7).

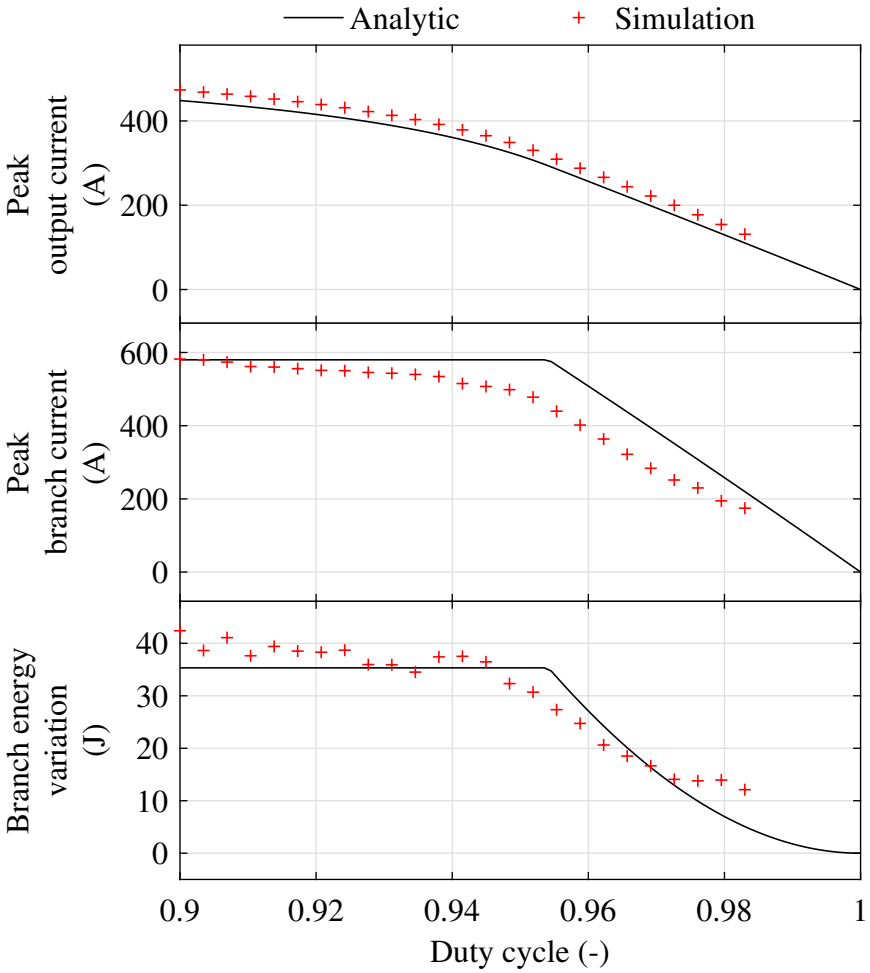


Figure 7.5: Reduction of the output current to achieve modulation indices above the designed value. Comparison of the analytically derived relationships with simulation results.

To validate the derived relationships, a set of simulations was carried out. In the simulation, the MMC fed a passive load. The output frequency was $f = 0$ Hz, the output inductance $L_\mathrm{o} = 13$ mH, and the resistance was adjusted to achieve the correct mean value of the output current. The MMC parameters are listed in Table 7.1 at the beginning of this chapter. The maximum allowed

peak branch current was selected to be $\hat{i}_{\mathrm{b,max}} = 580$ A. Note that this value is set relatively low to make both of the cases (the optimized solution for the output current and the solution limited by the maximum branch current) recognizable.

In Figure 7.5 the results of the simulations, i.e. the peak value of the output currents, the peak value of the branch currents, and the branch energy variation in relation to the peak duty cycle, are compared to the analytically derived values. Taking a closer look at the curves, two ranges can be recognized: In the first range, for duty cycles up to approximately $\delta = 0.955$, the maximum output current is limited by the maximum allowed peak branch current and the setpoint output current is calculated according to (7.7). In the second range, above $\delta \approx 0.955$, the optimized solution (7.5) for the output current is used.

Comparing the analytically determined curves with the simulation results in Figure 7.5, it can be observed that the peak output currents obtained from the simulation are slightly higher. This is caused by the current ripple. The peak value of the branch currents and the branch energy variation match the analytic curves well. Note that the higher the modulation index is, the higher the influence of the staircase waveform is, which was not considered in the derivation. Consequently, the results become less precise for increasing modulation indices. This imprecision also leads to instability in simulations for modulation indices above $M \approx 0.983$.

In conclusion, this section shows that it is possible to increase the output voltage by decreasing the output current. Nevertheless, this option is rather impractical for implementation in drives where full torque is required at rated speed.

7.3 Cable Reflection Analysis

As mentioned in the introduction, one of the crucial problems for machines fed from two-level VSIs are the overvoltages caused by the reflections occurring with long machine cables. In this section the influence of the quasi-two-level operation on these reflections is briefly investigated. A simplified modeling approach similar to the one presented in [142] is used to assure generality of the results. Examination of the resonances in the cables is out of the scope of this thesis.

The investigated model consists of three parts: a converter generating the quasi-two-level waveform, the cable transmitting the voltage waves, and the machine reflecting the waves. The model is solved using a simple discrete-time numeric calculation, calculating the values of the wave and its reflections for each point in time for equidistant positions in the cable. The discrete time period is approximately 2 ns and is matched according to the cable length and the wave propagation speed to obtain an integer number of investigated positions in the cable. This way, the translation of the wave (and its reflections) in time can be implemented as simple vector shifting.

The **quasi-two-level waveform**, depicted in Figure 7.6a, is simplified, assuming six voltage steps $n_{\mathrm{step}} = 6$ with a constant delay of T_{d} between each step. In the model, the waveform is generated as a superposition of two-level waveforms, depicted in Figure 7.6b. The rise time is $t_{\mathrm{r}} = 100$ ns, which is a value typical for IGBTs. The voltage of each voltage step is scaled to be $V_{\mathrm{step}} = 1/n_{\mathrm{step}}$ to enable a more straight-forward evaluation of the overvoltages. The converter behaves as a short-circuit for the reflected waves and thus its reflection coefficient is approximated with $\Gamma_{\mathrm{VSI}} = -1$.

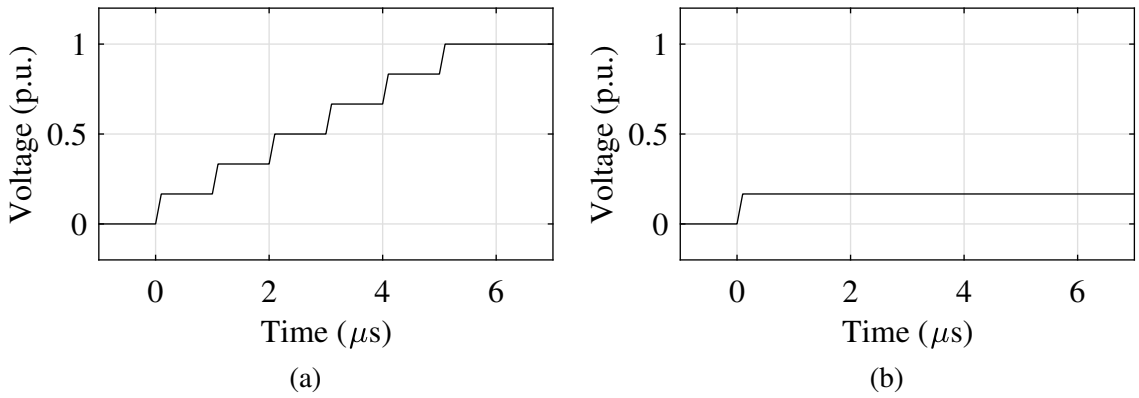


Figure 7.6: The voltage waveform generated by the investigated converter. The six-step quasi-two-level waveform (a) is generated as a superposition of two-level waveforms (b). The step delay time is $T_\mathrm{d} = 1$ µs and the rise time is $t_\mathrm{r} = 100$ ns.

The **machine cable** is modeled as a transmission line with a wave propagation speed of $v_\mathrm{wave} = 173.08$ m/µs. This represents a relative permeability of $\mu_\mathrm{r} = 1$, and a relative permittivity of $\varepsilon_\mathrm{r} = 3$, which are typical values for machine cables ($\varepsilon_\mathrm{r} = 2..8$ for thermoplastics according to [143]).

The **machine** is modeled as a wave-reflecting impedance with a reflection coefficient of $\Gamma_\mathrm{machine} = 0.6$. According to *IEC 61800-8*, this is a typical value for 355 kW machines, which are the largest machines of those listed in the norm.

The parameters used for the investigations are summarized in Table 7.2.

Table 7.2: Parameters used for investigation of the overvoltages due to long machine cables with quasi-two-level voltage waveforms.

Relative permittivity of the cable	ε_r	3
Relative permeability of the cable	μ_r	1
Propagation speed of the wave in the cable	v_wave	173.08 m/µs
Reflection coefficient of the converter	Γ_VSI	-1
Reflection coefficient of the machine	Γ_machine	0.6
Rise time of the IGBT	t_r	100 ns
Cable length	l	5 m .. 500 m
Number of voltage steps	n_step	6
Voltage step level	V_step	1/6 (p.u.)
Step delay time	T_d	{0 µs, 0.5 µs, 1 µs}

In Figure 7.7, the calculated voltage waveforms at the machine terminals are shown for different step delays T_d and different cable lengths. The investigated step delay times are 0 µs, 0.5 µs, and 1 µs. The delay of 0 µs is not practical for quasi-two-level operation and represents a two-level VSI with series-connected IGBTs. The cable length was varied between 5 m and 500 m.

As can be seen in the first column of Figure 7.7, the overvoltage of two-level VSI with series-connected IGBTs is still acceptable when the cable is 5 m long. However, once the cable length exceeds the critical cable length

$$l_\mathrm{crit} = \frac{1}{2} \cdot v_\mathrm{wave} \cdot t_\mathrm{r} = 8.65 \text{ m} \quad , \tag{7.8}$$

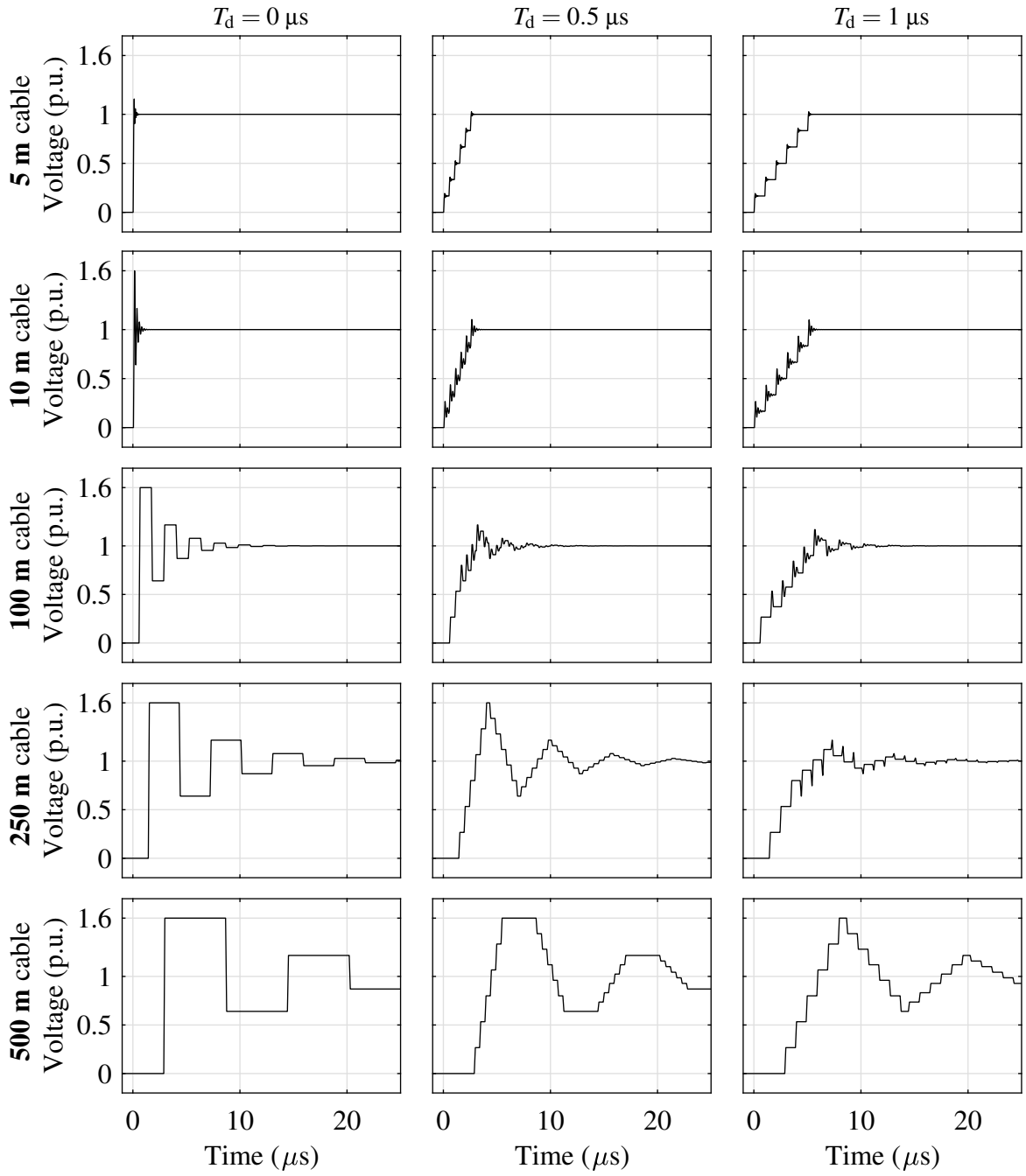


Figure 7.7: The voltage waveforms at the machine clamps for different step delays T_d and different cable lengths. The zero time delay represents a two-level VSI with series-connected IGBTs.

the relative overvoltage is identical to the machine reflection coefficient $\Gamma_{\text{machine}} = 0.6$.

If a delay between the voltage steps is applied (second and third columns of Figure 7.7), the overvoltage due to the IGBT's rise time is limited to 0.6 times of a single voltage step V_{step}. This leads to a relative overvoltage of only 0.1 for the quasi-two-level waveform with six voltage steps. Starting at a particular length (100 m in Figure 7.7), the overvoltage caused by

the quasi-two-level waveform is dominated by the overvoltage due to the overall rise time

$$t_{\mathrm{r,q2l}} = T_{\mathrm{d}} \cdot (n_{\mathrm{step}} - 1) \quad , \tag{7.9}$$

which is independent of the IGBT rise time t_{r}. Using this rise time, the critical cable length for the quasi-two-level waveform

$$l_{\mathrm{crit,q2l}}(T_{\mathrm{d}}) = \frac{1}{2} \cdot v_{\mathrm{wave}} \cdot t_{\mathrm{r,q2l}} = \frac{1}{2} \cdot v_{\mathrm{wave}} \cdot T_{\mathrm{d}} \cdot (n_{\mathrm{step}} - 1) \tag{7.10}$$

can be defined as a function of the step delay T_{d}. These critical cable lengths are $l_{\mathrm{crit,q2l}}(0.5\,\mu\mathrm{s}) = 216$ m and $l_{\mathrm{crit,q2l}}(1\,\mu\mathrm{s}) = 433$ m for the step delay times 0.5 µs and 1 µs, respectively. Once the machine cable is longer than this critical length, the overvoltage is identical to the machine reflection coefficient $\Gamma_{\mathrm{machine}} = 0.6$, which is also supported by Figure 7.7.

In conclusion, the quasi-two-level waveform contributes significantly to the mitigation of the machine overvoltages with long machine cables. Moreover, the critical length can be adjusted by selection of the delay time between the voltage steps. The theoretical findings described in this section were also proven in Section 6.4 using the down-scaled MMC prototype and a two-level VSI. In the experiment, a machine with lower power and thus a higher reflection coefficient is applied. Therefore, higher overvoltages are observable in the measurements.

Note that the simplified quasi-two-level waveform used for the presented investigations is a worst-case scenario for the line-to-line voltages of a quasi-two-level PWM-operated MMC. This scenario occurs when both branch voltages are changed at the same time, which happens when the output current is zero and thus the duration of `TRANSITION STATE` is zero as well. If the output current is non-zero, `TRANSITION STATE` prolongs one of the voltage steps, and thus further mitigates the overvoltages [this prolonged voltage step can be observed in the phase output voltage plotted in Figure 3.7].

Bertoldi *et al.* investigate further suppression of the overvoltages generated by the quasi-two-level waveforms with an additional $\mathrm{d}v/\mathrm{d}t$ filter in [144]. The method is beneficial when the machine tolerates only very small overvoltages.

7.4 Output Voltage Errors

The output voltage error is defined as the difference between the setpoint output voltage and the output voltage measured over the load within a single PWM period. There are several causes of the output voltage errors in quasi-two-level PWM-operated MMCs. In this section, these causes are explained, a worst-case error estimation is derived, and possible countermeasures are discussed.

Voltage Error Due to Branch Resistances

The first investigated error is the error due to branch resistances. The value of this voltage error depends on the output current value. This dependency can be derived using the phase-leg model

presented in Section 3.1. Assuming ideally coupled inductors for the phase leg model, the output voltage can be expressed as follows:

$$v_{\mathrm{o}} = \frac{v_{\mathrm{bB}} - v_{\mathrm{bA}} - R_{\mathrm{b}} \cdot i_{\mathrm{o}}}{2} \quad . \tag{7.11}$$

This means that there is an effective voltage drop over the branch resistances within the converter

$$v_{\mathrm{o,err},R\mathrm{b}} = -\frac{1}{2} \cdot R_{\mathrm{b}} \cdot i_{\mathrm{o}} \quad , \tag{7.12}$$

which causes an output voltage error. This additional resistance can also be observed in the system matrix $\mathbf{A}$ in (3.4).

This error can be compensated for simply by predicting the mean value of the output current for the upcoming PWM period and adding the estimated error value to the output voltage setpoint. Nevertheless, the compensation is effective only as long as the branch resistance is known and constant, and the mean value of the output current within the upcoming PWM period is predicted correctly.

To exclude this error from the following investigations, the branch resistance values are assumed to be zero [see Table 7.1].

Voltage Error Due to Transition States

One of the main assumptions applied during the derivation of quasi-two-level PWM operation was that the output current does not change during a PWM period. Nevertheless, this assumption is valid only to a certain degree. Even if the output inductance is very high, there is always some remaining current ripple. Moreover, unless the converter is operated at zero Hertz, the output currents are changed each PWM period to follow the sinusoidal setpoint values. The varying value of the output current not only impacts the predictive energy control, but also causes an output voltage error. This error is further analyzed in this section.

Since the two branch voltages have approximately the same value during the transition state ($v_{\mathrm{bA}} \approx v_{\mathrm{bB}}$), the output voltage is approximately zero during this period [see (7.11) and Figure 3.7]. However, the PWM generating the output voltage expects the output voltage to be $\pm V_{\mathrm{i}}/2$. Consequently, the `TRANSITION STATE` can impact the mean value of the output voltage during the PWM period, causing a voltage error.

When the duration of the `TRANSITION STATE` can be neglected (ideal case; depicted in Figure 3.3), the mean value of the output voltage during one PWM period can be calculated as

$$\overline{v}_{\mathrm{o}} = \frac{1}{T_{\mathrm{PWM}}} \cdot \left(\frac{V_{\mathrm{i}}}{2} \cdot \frac{1+\delta}{2} \cdot T_{\mathrm{PWM}} + \frac{-V_{\mathrm{i}}}{2} \cdot \frac{1-\delta}{2} \cdot T_{\mathrm{PWM}} \right) = \delta \cdot \frac{V_{\mathrm{i}}}{2} \quad . \tag{7.13}$$

If the duration of the two transition states is included and a non-inverted PWM carrier is applied (depicted in Figure 3.6), the mean value of the output voltage changes to

$$\begin{aligned}\overline{v}_{\mathrm{o}} &= \frac{1}{T_{\mathrm{PWM}}} \cdot \left(\frac{V_{\mathrm{i}}}{2} \cdot \left(\frac{1+\delta}{2} \cdot T_{\mathrm{PWM}} - T_{\mathrm{T2}} \right) + \frac{-V_{\mathrm{i}}}{2} \cdot \left(\frac{1-\delta}{2} \cdot T_{\mathrm{PWM}} - T_{\mathrm{T1}} \right) \right) \\ &= \left(\delta + (T_{\mathrm{T1}} - T_{\mathrm{T2}}) \cdot f_{\mathrm{PWM}} \right) \cdot \frac{V_{\mathrm{i}}}{2} \quad . \end{aligned} \tag{7.14}$$

The first `TRANSITION STATE` reduces the duration of `STATE A` and thus reduces the time when the negative voltage $-V_{\mathrm{i}}/2$ is assigned to the output by its duration T_{T1}. The second `TRANSITION STATE` reduces the duration of `STATE B` and thus reduces the time when the positive voltage $V_{\mathrm{i}}/2$ is assigned to the output by its duration T_{T2}.

When the output current is negative, the duration of the first `TRANSITION STATE`

$$T_{\mathrm{T1}} = \frac{L_{\mathrm{leg}}}{V_{\mathrm{i}}} \cdot \left(|i_{\mathrm{o,T1}}| + |I_{\mathrm{bA,c}}| + |I_{\mathrm{bB,c}}| \right), \quad i_{\mathrm{o}} < 0 \tag{7.15}$$

can be calculated by substituting (4.12) into (4.11), with the value $i_{\mathrm{o,T1}}$ being the value of the output current sampled at the first `TRANSITION STATE` during the PWM period. Note that the output current is assumed to be constant for the duration of the `TRANSITION STATE`. The duration of the second `TRANSITION STATE`

$$T_{\mathrm{T2}} = \frac{L_{\mathrm{leg}}}{2 \cdot n_{\mathrm{mpb}} \cdot V_C - V_{\mathrm{i}}} \cdot \left(|i_{\mathrm{o,T2}}| + |I_{\mathrm{bA,c}}| + |I_{\mathrm{bB,c}}| \right), \quad i_{\mathrm{o}} < 0 \tag{7.16}$$

can be calculated using (4.3) and (4.11), and assuming that $v_{\mathrm{bA}} = v_{\mathrm{bB}} = n_{\mathrm{mpb}} \cdot V_C$ during the second `TRANSITION STATE` [this can be observed on the right side of Figure 3.7]. Similar to (7.15), the change of the leg current Δi_{leg} during the second `TRANSITION STATE` equals the sum of compensating currents and the output current value $i_{\mathrm{o,T2}}$ sampled at the second `TRANSITION STATE` within the same PWM period as $i_{\mathrm{o,T1}}$. The equations further assume that the compensating currents $i_{\mathrm{bA,c}}$ and $i_{\mathrm{bB,c}}$ do not change during the PWM period[1)].

When the output current is positive, the duration of the first `TRANSITION STATE`

$$T_{\mathrm{T1}} = \frac{L_{\mathrm{leg}}}{2 \cdot n_{\mathrm{mpb}} \cdot V_C - V_{\mathrm{i}}} \cdot \left(|i_{\mathrm{o,T1}}| + |I_{\mathrm{bA,c}}| + |I_{\mathrm{bB,c}}| \right), \quad i_{\mathrm{o}} \geq 0 \tag{7.17}$$

and the second `TRANSITION STATE`

$$T_{\mathrm{T2}} = \frac{L_{\mathrm{leg}}}{V_{\mathrm{i}}} \cdot \left(|i_{\mathrm{o,T2}}| + |I_{\mathrm{bA,c}}| + |I_{\mathrm{bB,c}}| \right), \quad i_{\mathrm{o}} \geq 0 \tag{7.18}$$

can be calculated analogously by observing the branch voltages during transition states on the left side of Figure 3.6.

Substituting (7.15) – (7.18) into (7.14), the mean value of the output voltage considering the

[1)] This assumption is correct when the predictive branch-energy control is applied. With fast proportional branch-energy control, the correctness of the assumption is limited, since the compensating current changes during the PWM period. Nevertheless, the assumption does not lead to a large relative error, since the compensating currents have rather low values when the duty cycles are low.

output voltage error $\Delta v_{\mathrm{o,err,T}}$ can be expressed as

$$\begin{aligned}
\overline{v}_{\mathrm{o}} &= \underbrace{\delta \cdot \frac{V_{\mathrm{i}}}{2}}_{v_{\mathrm{o}}^{*}} + \underbrace{\left(|i_{\mathrm{o,T1}}| - |i_{\mathrm{o,T2}}| \cdot \lambda + (1-\lambda) \cdot \left(|I_{\mathrm{bA,c}}| + |I_{\mathrm{bB,c}}|\right)\right) \cdot \frac{L_{\mathrm{leg}} \cdot f_{\mathrm{PWM}}}{2}}_{\Delta v_{\mathrm{o,err,T}}}, \quad i_{\mathrm{o}} < 0 \\
\overline{v}_{\mathrm{o}} &= \underbrace{\delta \cdot \frac{V_{\mathrm{i}}}{2}}_{v_{\mathrm{o}}^{*}} + \underbrace{\left(|i_{\mathrm{o,T1}}| \cdot \lambda - |i_{\mathrm{o,T2}}| + (\lambda-1) \cdot \left(|I_{\mathrm{bA,c}}| + |I_{\mathrm{bB,c}}|\right)\right) \cdot \frac{L_{\mathrm{leg}} \cdot f_{\mathrm{PWM}}}{2}}_{\Delta v_{\mathrm{o,err,T}}}, \quad i_{\mathrm{o}} > 0
\end{aligned} \tag{7.19}$$

dependent on the output current direction and with

$$\lambda = \frac{V_{\mathrm{i}}}{2 \cdot n_{\mathrm{mpb}} \cdot V_C - V_{\mathrm{i}}} \tag{7.20}$$

being the ratio of the voltage drops over the leg inductance in the two different types of transition states. Equation (7.19) is only valid when the direction of the output current does not change during the PWM period. If this is not the case, the voltage error has to be calculated using (7.15) – (7.18).

Since the compensating currents are expected to be significantly lower than the output current and the value λ is generally expected to be near 1, (7.19) can be further simplified to:

$$\begin{aligned}
\overline{v}_{\mathrm{o}} &\approx \underbrace{\delta \cdot \frac{V_{\mathrm{i}}}{2}}_{v_{\mathrm{o}}^{*}} + \underbrace{\left(|i_{\mathrm{o,T1}}| - |i_{\mathrm{o,T2}}| \cdot \lambda\right) \cdot \frac{L_{\mathrm{leg}} \cdot f_{\mathrm{PWM}}}{2}}_{\Delta v_{\mathrm{o,err,T}}}, \quad i_{\mathrm{o}} < 0 \\
\overline{v}_{\mathrm{o}} &\approx \underbrace{\delta \cdot \frac{V_{\mathrm{i}}}{2}}_{v_{\mathrm{o}}^{*}} + \underbrace{\left(|i_{\mathrm{o,T1}}| \cdot \lambda - |i_{\mathrm{o,T2}}|\right) \cdot \frac{L_{\mathrm{leg}} \cdot f_{\mathrm{PWM}}}{2}}_{\Delta v_{\mathrm{o,err,T}}}, \quad i_{\mathrm{o}} > 0 \quad .
\end{aligned} \tag{7.21}$$

Note that in practical implementations, the maximum achievable branch voltage $n_{\mathrm{mpb}} \cdot V_C$ has to be higher than the input voltage V_{i} to provide a sufficient voltage reserve for the deadbeat controller controlling the leg current. Hence, the voltage ratio λ is always slightly higher than one.

As can be seen in (7.21), the voltage error depends on the leg inductance L_{leg} and the PWM frequency f_{PWM}, which are both well-known converter parameters. Furthermore, the voltage error depends on the difference between the output currents during the first and the second `TRANSITION STATE`s and on the voltage-ratio factor λ. The equation states that the less the output current changes, the lower the voltage error is. In the ideal case that the output current is constant during the PWM period and $\lambda \approx 1$, the voltage error is zero [see (7.21)].

Since the voltage error described in (7.19) does not depend on the output voltages, it becomes more significant when the output voltages are very low (e.g. machine start-up). Hence, the impact of the voltage error is similar to the dead-time voltage error experienced in classic two-level VSIs.

If the output current waveform can be predicted or a fast measurement of this waveform ca be made in the controlling FPGA, the error could be compensated for by increasing the required

duty cycle δ accordingly. This option was not further investigated nor implemented in this thesis.

To validate the derived voltage error expressions, a set of simulations for a model of a single phase leg is conducted. The applied duty cycle is varied in range $\delta \in [0.45\ ,\ 0.55]$ in 41 steps. A passive load is applied with an output resistance adjusted to set up the mean output current to either 500 A or 200 A. The output inductance is varied in range $L_\mathrm{o} \in [10\,\mathrm{mH}\ ,\ 40\,\mathrm{mH}]$ in 11 steps to vary the ripple of the output current. The rest of the converter parameters are summarized in Table 7.1. For the given parameters, the voltage ratio λ is 1.09.

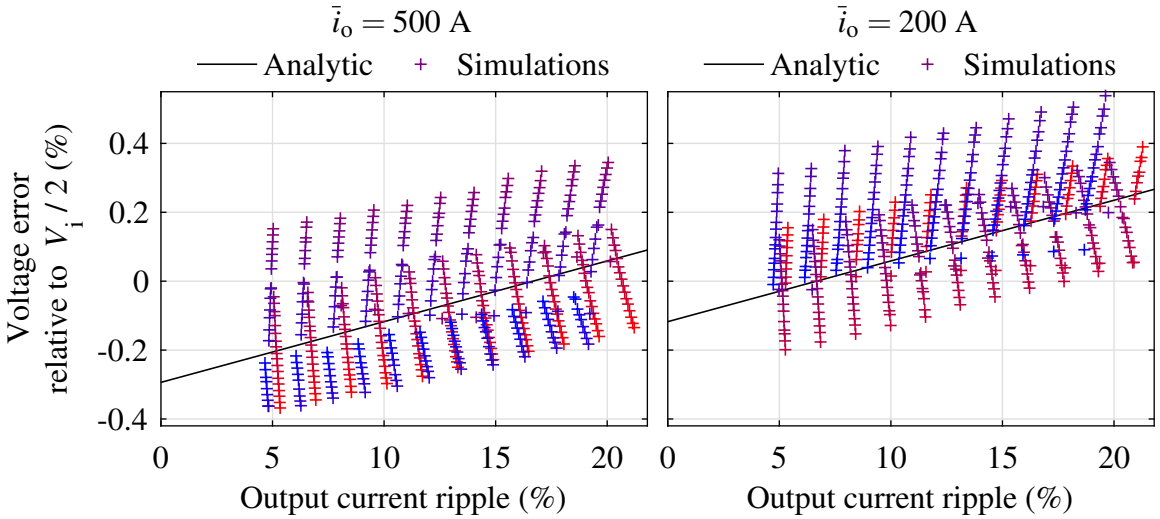


Figure 7.8: Relative voltage error versus the output current ripple: comparison of the analytic results for the **output voltage error due to transition states** $\Delta v_{\mathrm{o,err,T}}$ according to (7.21) to the simulations, which additionally include a voltage error due to HF modulation. The output current ripple displayed on the x-axis is a value relative to the peak output current $\hat{i}_\mathrm{o} = 500$ A. The output current is 500 A in the left graph, and 200 A in the right graph. The duty cycle δ is varied from 0.45 (red) to 0.55 (blue).

Figure 7.8 shows the results of the validating simulations. It can be stated that the analytic equation fits the trend of the simulation results for both investigated mean values of the output current. The simulated results are spread in a range around the analytic equation in a pattern depending on the modulation index, which suggests that there is an additional cause of the output voltage error. This additional voltage error is caused by HF modulation and is discussed in the next section. Furthermore, the figure shows that the voltage error is generally small and impacts the duty cycle first at the third digit after the decimal point.

Voltage Error Due to HF Modulation

The cause of the additional voltage error superimposed in Figure 7.8 can be explained by observing the output voltage waveform depicted in Figure 7.9. In addition to the different lengths of transition states in the figure, it can be seen that the output voltage is approximately $V_\mathrm{i}/2$ or $-V_\mathrm{i}/2$ most of the time. The exact value is set indirectly through the deadbeat controller and the HF modulation, which are applied during `STATE A` and `STATE B` [see Chapter 5 for further details]. Since the HF modulation is not synchronized with the switch-over from `STATE A` or `STATE B` to `TRANSITION STATE`, a part of the HF-modulation period is cut off at

the end of `STATE A` and `STATE B`. This can be seen near 0.4 ms and 0.6 ms in Figure 7.9. Consequently, the mean value of the branch voltage during this HF-modulation period does not match its setpoint. The voltage errors also impact the output voltage.

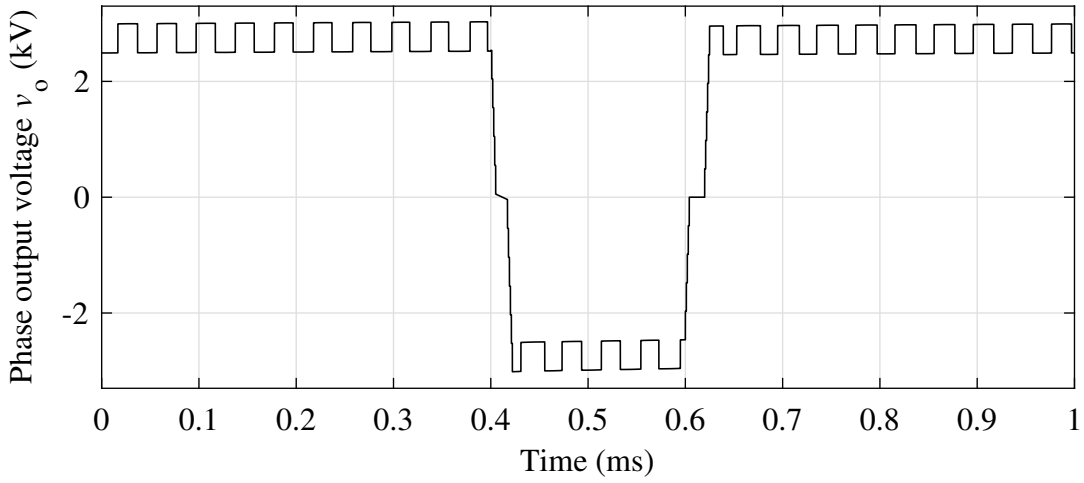


Figure 7.9: An example of output voltage waveform of quasi-two-level PWM-operated MMC over one PWM period. The duty cycle is $\delta = 0.6$. The mean value of the output current is $\bar{i}_o = 500$ A.

Assuming the voltage step generated by HF modulation is switched between two levels in each HF modulation period T_{HF} with a 50 % duty cycle (as depicted in the voltage waveform in Figure 7.9) and that the voltage step has a value of the module capacitor voltage V_C, the maximum error caused in any of the branches over one PWM period T_{PWM} is within the following range[2)]:

$$\Delta v_{bA,err,HF},\ \Delta v_{bB,err,HF} \in \left[-\frac{1}{T_{PWM}} \frac{T_{HF}}{4} \cdot V_C\ ,\ \frac{1}{T_{PWM}} \frac{T_{HF}}{4} \cdot V_C \right] \quad . \tag{7.22}$$

Applying these ranges to the equation describing the output voltage

$$v_o = \frac{v_{bB} - v_{bA}}{2} \tag{7.23}$$

obtained from (7.11) by neglecting the branch resistances, the range for the output voltage error

$$\Delta v_{o,err,HF} \in \left[-\frac{1}{4} \cdot \frac{f_{PWM}}{f_{HF}} \cdot V_C\ ,\ \frac{1}{4} \cdot \frac{f_{PWM}}{f_{HF}} \cdot V_C \right] \tag{7.24}$$

can be determined.

As can be seen in (7.24), the potential output voltage error due to HF modulation becomes higher when the PWM frequency is higher or the HF modulation frequency is lower. Furthermore, the relative value of the error, representing the error in the setpoint duty cycle δ, is proportional to the ratio between the module capacitor voltage V_C and the input voltage V_i. Consequently, the relative voltage error caused by HF modulation is lower for converters with higher numbers of modules per branch.

[2)] The maximum error occurs when the `TRANSITION STATE` starts at exactly one fourth or three fourths of the HF-modulation period. This is because the HF modulation generates symmetric pulses.

An online calculation of the error for the compensation thereof is too complex, as it depends on many factors that cannot be estimated exactly, such as duration of the transition state. However, since the time of switch-over to `TRANSITION STATE` is already well known at the beginning of the PWM period, the errors could be removed at their root cause by actively adjusting the last HF modulation period with the corresponding HF modulation carrier before the switch-over to `TRANSITION STATE` takes place. This option is not further investigated in this thesis.

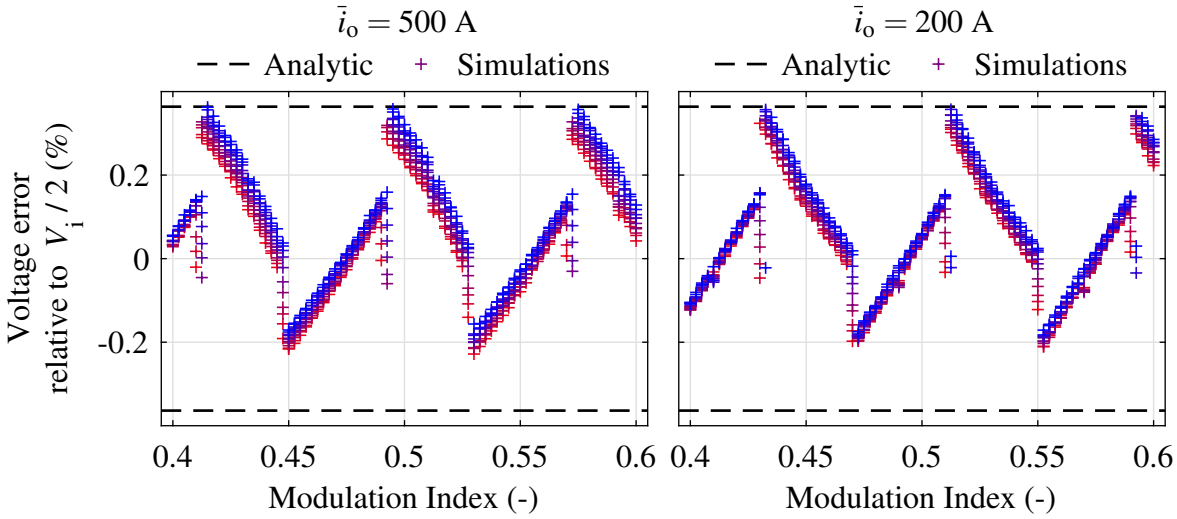


Figure 7.10: Relative output voltage error due to HF modulation $\Delta v_{o,err,HF}$ versus the modulation index: comparison of the analytically determined error range to the resulting output voltage errors from the simulations. The voltage errors resulting from simulations are reduced by the value of the voltage error due to transition states calculated analytically according to (7.21) to isolate the error due to HF modulaiton. The output current is 500 A in the left graph and 200 A in the right graph. The output inductance L_o is varied from 10 mH (red) to 40 mH (blue).

To validate the analytically determined range of output voltage error due to HF modulation, the same simulations were repeated for a range of duty cycles $\delta \in [0.4\ ,\ 0.6]$ in 81 steps. To exclude the voltage error due to transition states, the voltage errors resulting from simulations are reduced by the errors due to transition states $v_{o,err,T}$, calculated according to (7.21). The results are plotted in Figure 7.10. The figure confirms that the simulated voltage error due to HF modulation is within the analytically derived range. The slight dependence of the simulated error on the output inductance, visible in Figure 7.10, is most likely caused by neglecting the compensating currents when calculating the voltage error due to transition states.

Voltage Error Due to IGBT Dead-Times

The voltage error due to IGBT dead-times

$$v_{o,err,DT} = v'_{o,err,DT} + v''_{o,err,DT} \tag{7.25}$$

can be split into two parts. The first part $\Delta v'_{o,err,DT}$ is responsible for the errors during `STATE A` and `STATE B`. The second part $\Delta v''_{o,err,DT}$ consists of the voltage error due to dead-times during `TRANSITION STATE`.

To understand the output voltage error due to IGBT dead-times, the error in the voltage of a single module has to be studied first. Using the half-bridge module definition from Section 2.1, the mean voltage errors during a HF modulation period $T_{\mathrm{HF}} = 1/f_{\mathrm{HF}}$ caused by dead-time T_{DT} for the switching state transitions ($s = 1 \rightarrow s = 0$ representing the short-circuiting of the module output or $0 \rightarrow 1$ representing the insertion of the module) can be determined. These mean voltage errors are listed in Table 7.3 in relation to the branch current direction.

Table 7.3: The mean half-bridge module voltage error $v_{\mathrm{mod,err}}$ due to IGBT dead-time T_{DT} over a HF modulation period T_{HF} caused by changing the switching state s.

	$i_{\mathrm{b}} > 0$	$i_{\mathrm{b}} < 0$
$s = 0 \rightarrow s = 1$	$v_{\mathrm{mod,err}} = 0$	$v_{\mathrm{mod,err}} = f_{\mathrm{HF}} \cdot T_{\mathrm{DT}} \cdot V_C$
$s = 1 \rightarrow s = 0$	$v_{\mathrm{mod,err}} = -f_{\mathrm{HF}} \cdot T_{\mathrm{DT}} \cdot V_C$	$v_{\mathrm{mod,err}} = 0$

Observing Figures 5.8 and 5.9, it can be recognized that the branch current of Branch A is negative during `STATE A` and the branch current of Branch B is positive during `STATE B` when the output current is positive. Consequently, the mean voltage error in Branches A and B

$$\begin{bmatrix} \Delta v'_{\mathrm{bA,err,DT}} \\ \Delta v'_{\mathrm{bB,err,DT}} \end{bmatrix} = \frac{1}{T_{\mathrm{PWM}}} \cdot \begin{bmatrix} T_{\mathrm{A}} \\ -T_{\mathrm{B}} \end{bmatrix} \cdot f_{\mathrm{HF}} \cdot T_{\mathrm{DT}} \cdot V_C, \quad i_{\mathrm{o}} > 0 \tag{7.26}$$

can be calculated over a PWM period T_{PWM}, assuming that one module is inserted and one is short-circuited during each HF modulation period. T_{A} is the duration of `STATE A` and T_{B} is the duration of `STATE B`.

Analogously, the branch current of Branch B is positive during `STATE A` and the branch current of Branch B is negative during `STATE B` when output current is negative. Hence, the mean voltage error in branches A and B

$$\begin{bmatrix} \Delta v'_{\mathrm{bA,err,DT}} \\ \Delta v'_{\mathrm{bB,err,DT}} \end{bmatrix} = \frac{1}{T_{\mathrm{PWM}}} \cdot \begin{bmatrix} -T_{\mathrm{A}} \\ T_{\mathrm{B}} \end{bmatrix} \cdot f_{\mathrm{HF}} \cdot T_{\mathrm{DT}} \cdot V_C, \quad i_{\mathrm{o}} < 0 \quad . \tag{7.27}$$

has opposite signs for negative output currents.

Finally, applying the expressions for the branch voltage errors (7.26) and (7.27) to the output voltage equation (7.23), the voltage error caused by dead-times during `STATE A` and `STATE B` can be expressed as

$$v'_{\mathrm{o,err,DT}} = -\mathrm{sign}(i_{\mathrm{o}}) \cdot \frac{T_{\mathrm{A}} + T_{\mathrm{B}}}{T_{\mathrm{PWM}}} \cdot \frac{f_{\mathrm{HF}} \cdot T_{\mathrm{DT}} \cdot V_C}{2} \quad , \tag{7.28}$$

depending on the direction of the output current. When the duration of the `TRANSITION STATE` can be neglected, then $T_{\mathrm{PWM}} = T_{\mathrm{A}} + T_{\mathrm{B}}$ and thus a simplified form can be used to estimate the voltage error:

$$v'_{\mathrm{o,err,DT}} = -\mathrm{sign}(i_{\mathrm{o}}) \cdot \frac{f_{\mathrm{HF}} \cdot T_{\mathrm{DT}} \cdot V_C}{2} \quad . \tag{7.29}$$

Equation (7.29) indicates that the absolute value of the voltage error caused by IGBT dead-times during `STATE A` and `STATE B` is constant and only its sign depends on the output current.

The error becomes more significant the higher the ratio between the applied dead-time and the HF modulation period is. Similar to the output voltage error due to HF modulation, the relative voltage error becomes less significant the higher the number of modules per branch is.

Note that in practical applications, a large part of the voltage error $v'_{\mathrm{o,err,DT}}$ is reduced by the closed-loop leg-current controller, since the voltage error also causes a deviation in the leg current.

Using Figures 5.8 and 5.9, an interesting observation can be made for the voltage errors due to dead-times during the `TRANSITION STATE`. The modules are inserted ($s = 0 \rightarrow s = 1$) only when the branch current is positive and short-circuited ($s = 1 \rightarrow s = 0$) only when the branch current is negative. Consequently, the resulting branch voltage errors and resulting output voltage error are zero [see Table 7.3]:

$$v''_{\mathrm{o,err,DT}} = 0 \quad . \tag{7.30}$$

However, Figures 5.8 and 5.9 show the operation of a severely simplified model. In practical implementation, delay times T_{d} are applied between the modules' switching instants, leading to a trapezoidal staircase waveform. As a consequence, the branch currents change while the modules are switched [see the discussion on the frozen states in Section 5.2]. Observing Figures 5.8 and 5.9, it can be seen that during one transition the modules are switched when the branch currents are high. Hence, it is less likely that the branch current changes its direction while the modules are switched. However, during the second transition the modules are switched when the branch currents have approximately the same value as the compensating currents. Hence, it is possible that the branch current changes its direction while the modules are switched. Consequently, some of the modules can generate voltage errors due to IGBT dead-times during the transition state.

To observe this effect, output voltage waveforms with and without the IGBT dead-time were simulated. According to Figure 5.8, the branch currents are low while the modules are switching in the second `TRANSITION STATE`. The simulated waveforms showing this `TRANSITION STATE` are plotted in Figure 7.11 for two different values of mean output current. As can be seen in the figure, the modules generate voltage errors for part of `TRANSITION STATE` (until the branch currents change their signs). These voltage errors are visible in Figure 7.11 as the difference between the green and black lines. Comparing the left graph and the right graph of Figure 7.11, not only it can be observed that the duration of the `TRANSITION STATE` is longer with higher output currents but also that the sum of the voltage errors generated by the modules is higher for the lower output current ($\bar{i}_{\mathrm{o}} = 200$ A). The total voltage error due to IGBT dead-times during `TRANSITION STATE` $\Delta v''_{\mathrm{o,err,DT}}$ is generally expected to be more severe for lower output currents, since these require lower compensating currents and thus the branch currents change their signs later (and the modules cause errors over a longer period of time).

The worst-case error in this transition state can be estimated for each branch by assuming that every module generates the IGBT dead-time error:

$$\begin{bmatrix} \Delta v''_{\mathrm{bA,err,DT,max}} \\ \Delta v''_{\mathrm{bB,err,DT,max}} \end{bmatrix} = \mathrm{sign}(i_{\mathrm{o}}) \cdot \frac{1}{T_{\mathrm{PWM}}} \cdot \begin{bmatrix} 1 \\ -1 \end{bmatrix} \cdot T_{\mathrm{DT}} \cdot n_{\mathrm{mod}} \cdot V_C \quad . \tag{7.31}$$

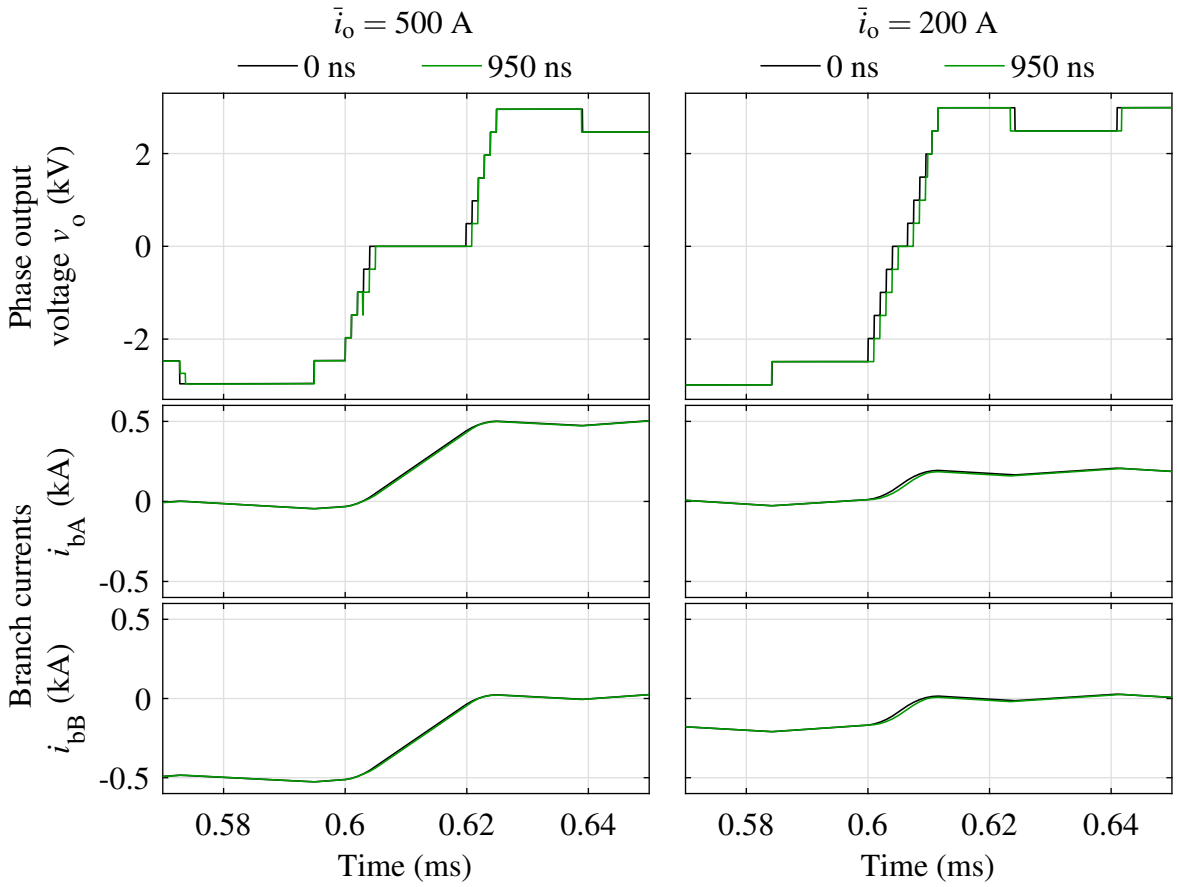


Figure 7.11: Detailed view of output voltage waveform of quasi-two-level PWM-operated MMC showing the second `TRANSITION STATE` for an idealized operation without dead-time (black) and for an operation with an IGBT dead-time of $T_{DT} = 950$ ns. The duty cycle is $\delta = 0.6$. The mean value of the output current is $\bar{i}_o = 500$ A on the left side and $\bar{i}_o = 200$ A on the right side.

Substituting these branch voltage errors into (7.23), the worst-case estimation of the output voltage error during the `TRANSITION STATE`

$$v''_{o,err,DT,max} = -\text{sign}(i_o) \cdot \frac{T_{DT} \cdot n_{mod}}{T_{PWM}} \cdot V_C \tag{7.32}$$

can be derived.

To validate the estimated voltage error due to IGBT dead-times, the last simulations were repeated with an IGBT dead-time of $T_{DT} = 950$ ns included in simulations. The additional error caused by the IGBT dead-time, plotted in Figure 7.12, is estimated as the difference between the results from the simulations with a dead-time and the simulations without consideration of the dead-time.

Comparing the simulation results with the analytically calculated value according to (7.29), both of which are shown in Figure 7.12, it can be stated that the voltage error estimation from simulation is significantly lower than the analytically calculated value[3)]. The dead-time error

[3)] The two points exceeding the value in the left graph near modulation index $M \approx 0.57$ are most likely not caused by the IGBT dead-times but by the discontinuity in the voltage error due to HF modulation observable in the left graph of Figure 7.10 near modulation index $M \approx 0.57$.

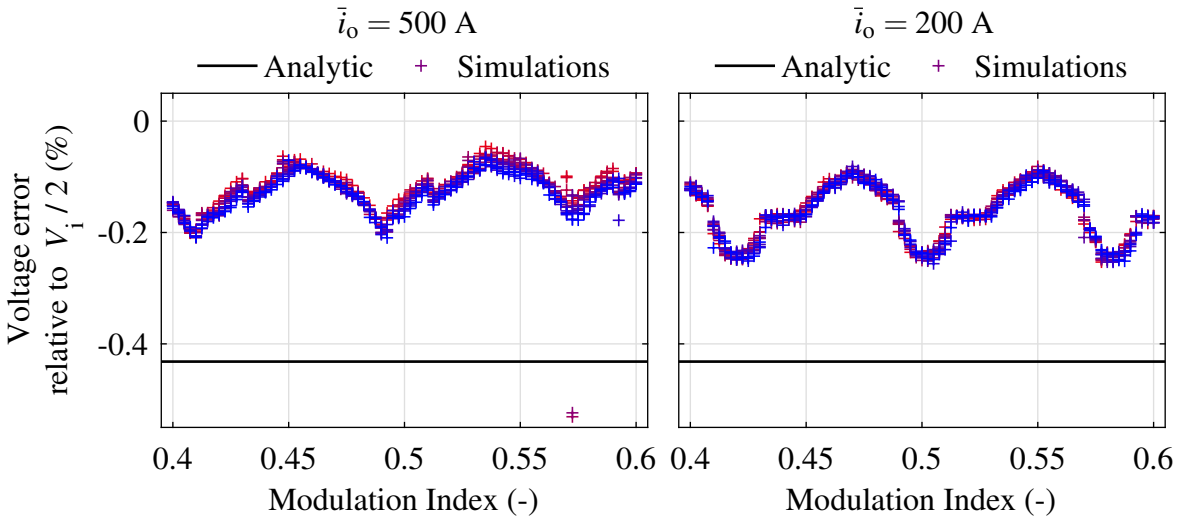


Figure 7.12: Relative output voltage error due to IGBT dead-times ($T_{DT} = 950$ ns) versus the modulation index: comparison of the analytically determined error value according to (7.29) to the resulting output voltage errors from the simulations. The voltage errors resulting from simulations with IGBT dead-time are reduced by the value of the voltage error obtained by simulations without dead-time. The output current is 500 A in the left graph, and 200 A in the right graph. The output inductance L_o is varied from 10 mH (red) to 40 mH (blue).

during transition states is assumed to be zero according to (7.30). If the worst-case estimation for this error were applied according to (7.32), the difference between the estimation and the simulated errors would be further increased by a relative voltage error of 0.21 %.

The cause of the difference between the errors calculated analytically according to (7.29) and those obtained from simulation is the aforementioned compensation by the closed-loop leg-current controller. Additionally, a changing sign of the branch current within a HF-modulation period when the compensating current value is lower than the branch current ripple also reduces the voltage error. In such a case, neither of the branches generates voltage errors or both branches generate voltage errors with the same absolute value and with an opposite sign [see Table 7.3]. Consequently, the voltage error is zero during the longer of the two states – either `STATE A` or `STATE B`, and thus the total output voltage error is significantly decreased.

Comparing the simulation results for 500 A (Figure 7.12 left) with those for 200 A (Figure 7.12 right), it can be stated that lower output currents (and thus lower compensating currents) lead to higher voltage errors due to IGBT dead-times. This can be explained by the aforementioned voltage errors during the transition states, which are demonstrated in Figure 7.11.

The voltage errors due to IGBT dead-times could be compensated for directly in the FPGA by an estimation of the branch voltage errors, estimated through a measurement of the current direction shortly before the switching state is changed. Nevertheless, such active compensation is expected to be prone to false estimation of the voltage error, since the sign of the branch currents, which are often very low, has to be estimated correctly.

Comparison to Conventional MMCs and Two-Level VSI

In this section, the comparison of voltage errors occurring with quasi-two-level PWM-operated MMCs to those of conventionally operated MMCs and of two-level VSIs is briefly discussed. While some causes for voltage errors are specific to quasi-two-level PWM operated MMCs, i.e. the voltage errors due to transition states and due to the HF modulation, the other causes also occur with the conventional operation of MMCs and the two-level VSIs. These are the voltage errors due to branch resistances and due to IGBT dead-times.

The voltage error due to branch resistances of conventional MMCs occurs the same way as that of quasi-two-level PWM operation. With VSI, the branch resistances are represented by the voltage drops over the currently conducting semiconductors. Consequently, if the same value of "branch resistance" is assumed, the voltage drop with two-level VSIs is double compared to that of quasi-two-level PWM-operated MMCs. Nevertheless, the voltage drops over the converter components are generally not crucial, since the closed-loop output-current controller can handle the corresponding resistances as if they were a part of the load.

Since there are no transition states in the conventional operation of MMCs, the voltage errors due to dead-times occur on a similar basis as those of quasi-two-level PWM operation during `STATE A` and `STATE B`. Assuming the same modulation frequency as HF modulation frequency, this error can be almost double to that of quasi-two-level PWM operation when conventional operation is applied, since both branch voltages of a single phase leg are being modulated concurrently. On the other hand, the modulation frequency of a conventionally operated MMC is expected to be lower. Thus, the voltage error is expected to be lower as well.

The cause for the voltage error due to dead-times in a two-level VSI can be described similarly to the voltage error due to dead-times of a quasi-two-level PWM-operated MMC during transition states. This is confirmed by the fact that the worst-case error estimation for a quasi-two-level PWM-operated MMC described by (7.32) equals the voltage error estimation of a two-level VSI when the following approximation is made: $n_{\mathrm{mod}} \cdot V_C \approx V_{\mathrm{i}}$. However, the voltage error due to dead-times is expected to be more significant for two-level VSIs, since (7.32) describes only the worst-case scenario for the quasi-two-level PWM operation of MMCs and the dead-times of typical medium-voltage two-level VSIs are likely to be significantly higher.

7.5 Converter Start-Up Process

While the converter prototype is capable of precharging the module capacitors through isolating dc-dc converters installed at the converter racks, this is usually not the case with unscaled medium voltage MMCs. Instead, a precharging scheme has to be applied. In this section, the process of converter start-up is investigated using a simulation model.

The investigated converter is a medium-voltage converter feeding a passive load ($L_{\mathrm{o}} = 13$ mH, $R_{\mathrm{o}} = 5\ \Omega$), for the sake of simplicity. The converter design and control parameters are listed in Table 7.1. The dc-link capacitor is chosen to have a capacitance $C_{\mathrm{i}} = 250\ \mu$F and the input voltage source is modeled as a series connection of an ideal voltage source with a voltage V_{i}, an inner resistance $R_{\mathrm{i}} = 500\ \mathrm{m}\Omega$, and a stray inductance $L_{\mathrm{i}} = 500\ \mu$H. The scheme of the simulated converter is depicted in Figure 7.13. The precharge resistor was chosen to be $R_{\mathrm{ch}} = 20\ \Omega$. Note that since the passive module state, when both module's switches are turned off, is also

necessary for the simulation, the detailed model, which implements each switch separately, is applied.

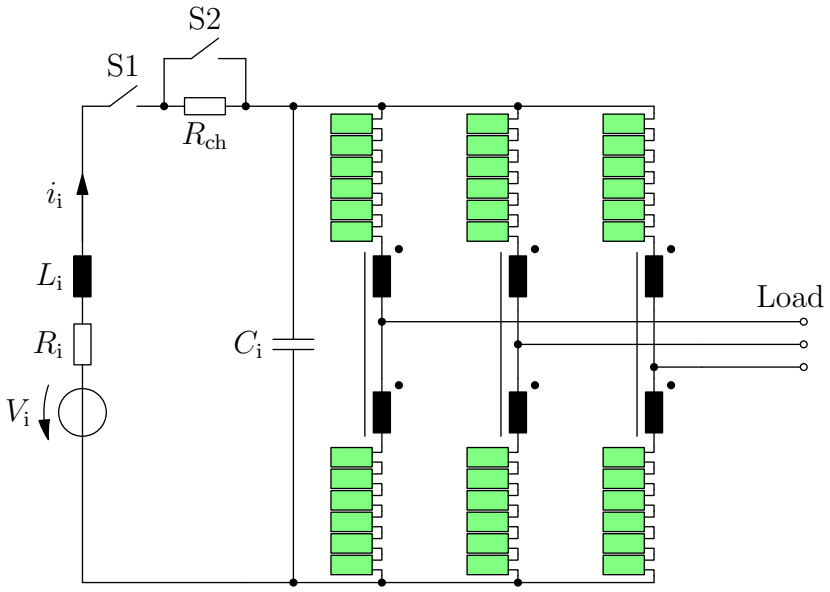


Figure 7.13: Scheme of the simulated model used for a demonstration of the converter start-up.

The waveforms of the simulated converter, plotted in Figure 7.14, demonstrate the whole start-up process. This process consists of the following steps:

1. **Precharging the capacitors through a precharge resistor** – from 5 ms to 30 ms:
   In this step, switch S1 is closed and the dc-link capacitor is charged with an exponentially decreasing current. The initial value of the current and the charge time can be adjusted by a proper selection of the precharge resistor. At the same time, the module capacitors are precharged through the upper diodes of each module. There are oscillations visible in the branch currents, caused by the weakly damped resonant circuit consisting of the dc-link, the branch inductors and the module capacitances.

2. **Short-circuiting the prechage resistor** – from 30 ms to 35 ms:
   Once the dc-link capacitor voltage and module capacitor voltages have almost reached their steady value, the precharge resistor is short-circuited with switch S2. This causes small peaks in the branch currents and the input current, and the capacitors are charged to their steady value more quickly. While the steady voltage value is identical to the rated value for the dc-link capacitor, the module capacitor voltages are roughly at half of their setpoint value. This voltage should be high enough for the modules' logic to turn on if they are powered from the module capacitor.

3. **Charging the module capacitors with a constant current** – from 35 ms to 45 ms:
   After the precharge resistor is short-circuited, the modules can be actively charged. In the given example, a dead-beat controller controls the leg current of each leg to be 20 A. Unlike during `STATE A` and `STATE B`, the setpoint value for the sum of branch voltages is split equally between the upper and lower branches. The branch voltages are set using HF modulation. Since both branches have the same voltage setpoint value, they

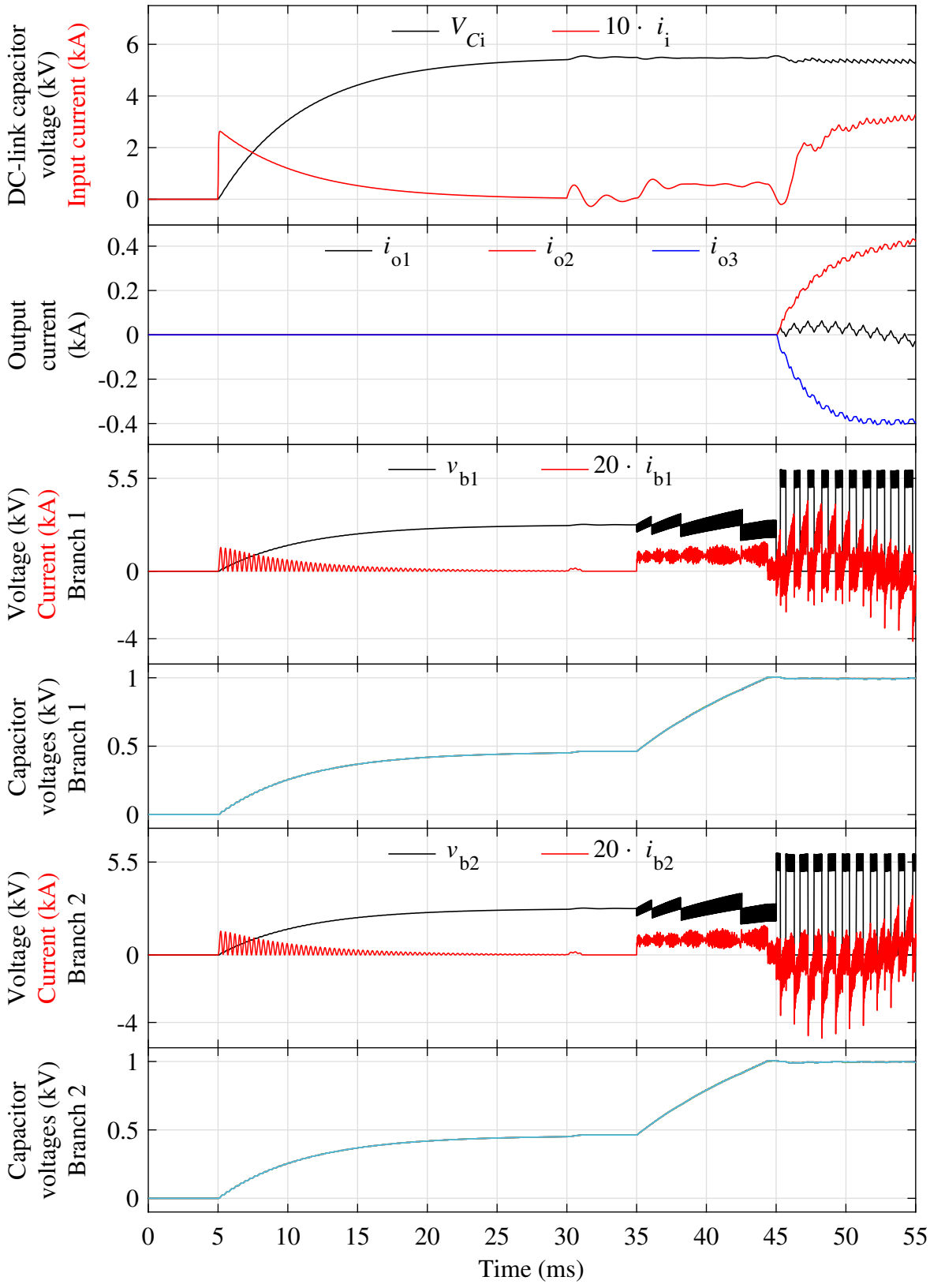


Figure 7.14: Start-up of the quasi-two-level PWM operated MMC from a direct voltage source.

are charged equally and the output voltage is zero.[4)] Once the module capacitor voltages achieve their setpoint value, the leg current is controlled to zero and normal converter operation can be started.

4. **Starting the MMC in quasi-two-level PWM operation mode** – from 45 ms:
   The quasi-two-level PWM operation can be started without any significant delay, directly generating output voltages and output currents.

Please note that the described process does not significantly differ from the start-up process of the conventionally operated MMC described e.g. in [95]. The main differences are the high-frequency oscillations in branch currents caused by the relatively low module capacitance and low leg inductance. The amplitude of these oscillations can effectively be reduced by choosing a higher precharge resistance, which leads to a longer start-up time.

[4)] Note that if the capacitances between the upper and lower branch differ significantly, their final voltages would also be different. If the resulting difference is unacceptable, the common-mode voltage could be used as a degree of freedom to control the energy split.

8 Application in Medium-Voltage Drives

In this chapter, a design of quasi-two-level PWM-operated MMCs is presented for several study cases in drive applications. Additionally, the design is carried out for the conventional operation of MMCs, for two-level VSIs, and for MMMCs.

Note that this chapter does not provide a perfect way to design quasi-two-level PWM-operated MMCs. The main purpose is rather to show how particular parameters can be selected and to evaluate different trends in converter properties compared to other operation modes and converter topologies.

8.1 Study Cases and Parameters

In this chapter, four study cases are investigated: A, B, C, and D. These are further distinguished according to characteristics of the load torque: I and II.

The four study cases represent four different machines, each of which is a different scaling of a single machine. The machine per unit (p.u.) parameters are listed in Table 8.1. These parameters are based on an existing low-speed synchronous machine with a rated power of several megawatts.

Table 8.1: Per unit values, relative to rated apparent power S_N and rated stator voltage V_sN, used for the scaling of the synchronous machine.

Reactance in d direction	0.8 (p.u.)
Reactance in q direction	0.5 (p.u.)
Stator resistance	0.015 (p.u.)

The machines, which represent the study cases, are listed in Table 8.2. It can be seen that two voltage levels, typical for medium-voltage drive systems, are investigated: 3.3 kV (study cases A and B) and 6.6 kV (study cases C and D). The machines are further distinguished by their rated electrical stator frequency f_sN: 30 Hz (study cases A and C) and 5 Hz (study cases B and D). The rated stator currents are selected in all study cases to be 600 A. Note that the number of pole pairs is one in all study cases to enable a simpler transformation between the speed and the electrical frequency. The number of pole pairs does not influence the converter, as long as the p.u. values remain unchanged.

The total rotational inertia of the system J is set relatively high to stabilize the steady-state behavior of the machine by setting the time constant $\frac{J \cdot 2 \cdot \pi \cdot f_\mathrm{N}}{T_\mathrm{N}}$ to 15 seconds. T_N is the machine's rated torque.

Table 8.2: Parameters of the investigated synchronous machines representing the different study cases. The stator voltage is a line-to-line RMS value. The stator current is a RMS value.

		Study Case			
Parameter		A	B	C	D
Rated stator voltage	V_{sN} (kV)	3.3	3.3	6.6	6.6
Rated stator frequency	f_{sN} (Hz)	30	5	30	5
Rated stator current	I_{sN} (A)	600	600	600	600
Rated apparent el. power	S_N (MVA)	3.43	3.43	6.86	6.86
Rated power factor	$\cos\varphi_N$ (-)	0.87	0.87	0.87	0.87
Rated mechanical power	P_{mech} (MW)	2.92	2.92	5.84	5.84
Rated torque	T_N (kNm)	15.5	92.9	31.0	186
Number of pole pairs	p (-)	1	1	1	1
Stator resistance	R_s (mΩ)	47.6	47.6	95.3	95.3
Inductance in d-direction	L_d (mH)	13.5	80.9	27.0	162
Inductance in q-direction	L_q (mH)	8.40	50.5	16.8	101
Field-linked direct axis flux linkage	$\Psi_{f,d}$ (Vs)	12.6	73.0	24.3	146
Total rotational inertia	J ($10^3\cdot$ kg m^2)	1.23	44.4	2.46	88.7

As stated above, the study cases are further divided into two groups according to the characteristics of the load's torque. The torque is either constant, independent of the speed (characteristic I), or it rises quadratically with the speed until it reaches its rated value (characteristic II). The two characteristics are depicted in Figure 8.1.

Note that the two characteristics are selected to cover a large number of applications. Although the characteristic II is typically not required at a single application over the whole speed range, the converter designed for this characteristic can be applied to pumps and blowers (operated at positive speed) as well as to wind turbines (operated at negative speed).

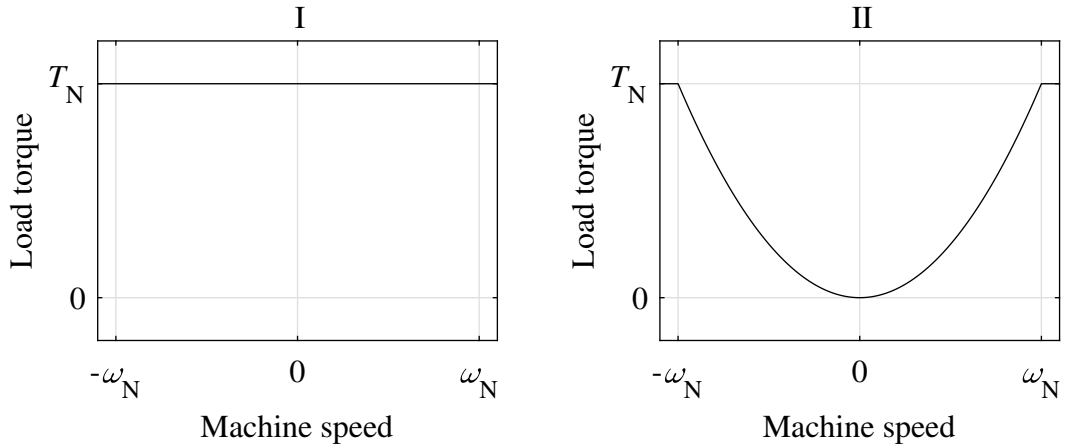


Figure 8.1: Considered load torque characteristics: I – constant torque, II – quadratic torque. Machine speed $\omega_N = 2\cdot\pi\cdot\frac{f_{sN}}{p}$.

To make a fair comparison between the operation modes and topologies, it is assumed that the dc-link voltage (or the grid voltage with MMMC) can be chosen freely to match the optimum for the particular converter. This assumption can be made because the drive systems usually

employ an isolating transformer. To simplify the investigations, the in-feed voltage sources are assumed to be ideal without any tolerances.

The comparison between the different operation modes and topologies are based on the following indicators:

- total chip area of semiconductor switches,
- total energy stored in passive components (capacitors and inductors),
- the maximum RMS current of module capacitors and of the dc-link capacitor,
- the total harmonic distortion (THD) of the output current,
- and the converter losses.

All of these parameters are evaluated considering 60 operating points that represent the machine speed. The 60 operating points are located equidistantly in the range from negative rated machine speed to positive rated machine speed. The zero speed operation is not investigated, since this point is problematic to evaluate due to the infinite number of initial rotor angles. The resulting simulation data is evaluated over one output period $1/f$ and the data is captured first after the simulation model reached its steady-state operation. The simulation data is in discrete time with sampling period $T_\mathrm{s} = 2\ \mu\mathrm{s}$. Note that the simulation runs with shorter simulation steps and the sampling time period T_s only determines the points in time when the raw data is captured.

To evaluate the total chip area of semiconductor switches and the converter efficiency, the existing model has to be enhanced with a semiconductor loss model and a thermal model. Furthermore, the scaling of the module's chip area has to be introduced. These additional models are presented in the next sections. For the semiconductor chip area scaling, a 1700 V IGBT module *Infineon FZ600R17KE4* [145] is chosen as a reference device. It is assumed that the reference IGBT module is applied with a sink thermal resistance of $R_{\vartheta,\mathrm{s,ref}} = 50$ K/kW. This value is based on the customer-ready water coolers for IGBT modules in 62 mm housing from [146] with thermal resistances ranging from 16 K/kW to 50 K/kW under reference conditions.

The IGBT module is scaled in a way that the maximum junction-to-sink temperature difference does not exceed $\Delta\vartheta_{\mathrm{j,s,max}} = 50$ K at any time and the maximum variation of the junction temperature does not exceed $\Delta\vartheta_{\mathrm{j,max}} = 15$ K. The variation of the junction temperature is considered a limiting factor only for speeds above 20 % of the rated speed, since it is assumed that the operating points below this speed have to be applied only shortly during machine start-up. For the following investigations, a maximum allowed blocking voltage, which can be repetitively present at the module capacitor, is $V_{C,\mathrm{max}} = 1$ kV.

8.2 Design Process

The overall design process is described by the diagram depicted in Figure 8.2.

In the first step, the parameters of the converter and the machine are initialized for the particular study case. Next, a loop is initiated which iterates over all 60 investigated operating points. For each operating point, representing a different machine speed, the drive system, including the converter and the machine, is simulated. Once the simulation is finished, several calculations

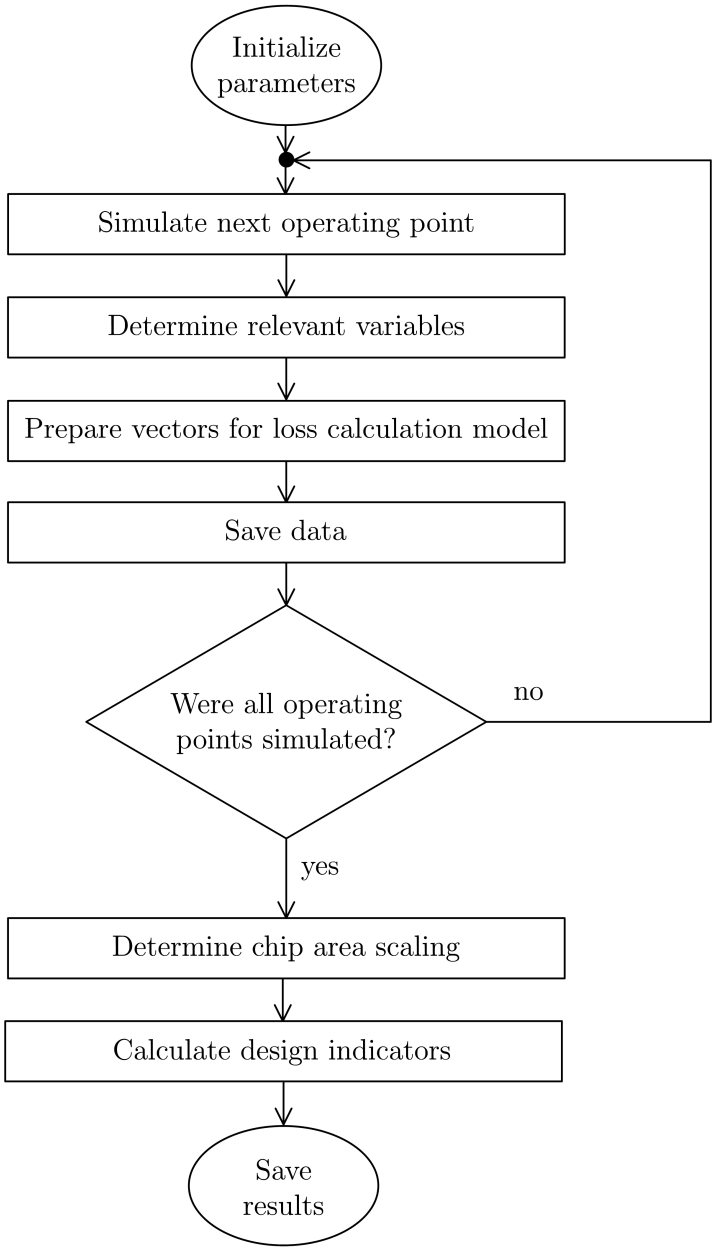


Figure 8.2: Process applied to design the investigated converters.

are done to determine variables relevant for the design indicators. These are e.g. RMS values of module capacitor currents or the THD of output currents. Furthermore, the current vectors for the individual semiconductor switches of each module are prepared for later evaluation in the loss model. Finally, the current vectors and the variables relevant for the design indicators are saved and the next operating point can be simulated.

When all simulations are finished, the chip area scaling factors for the semiconductor switches are determined. In the last two steps, the values of the design indicators are determined from available data and the final results are saved.

The individual calculations and the additional models required for the design process are presented in the next section.

8.3 Additional Models and Calculations

This section presents the implemented loss model, thermal model, calculation of the input capacitor, and determination of the particular design indicators. The loss model and thermal model are validated using the *Plexim Plecs* toolbox in Appendix E.

8.3.1 Scaling of Semiconductor Switches

The semiconductor switches are scaled according to the process described by Figure 8.3.

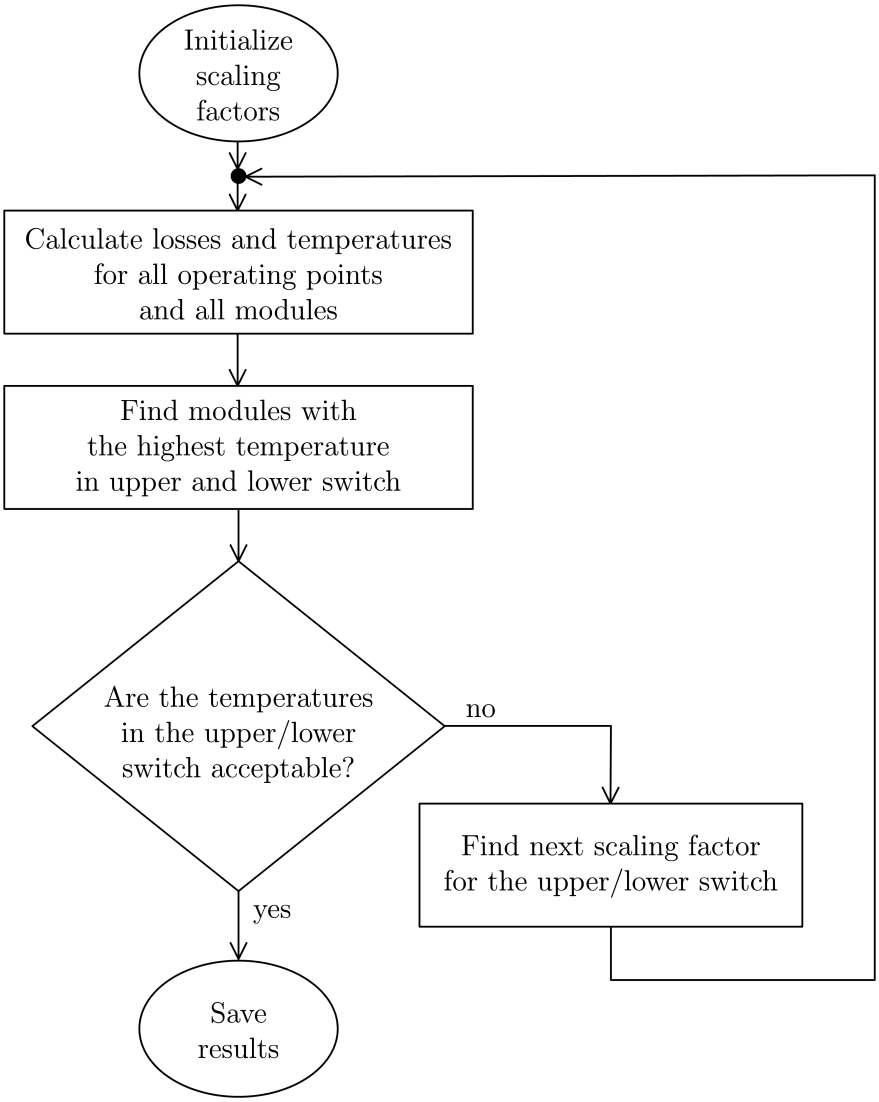


Figure 8.3: Process for scaling of the IGBT modules.

In the first step, the scaling factors for the area of the upper switch a_1 and the lower switch a_2 are initialized. A scaling factor

$$a = \frac{A}{A_{\text{ref}}} \tag{8.1}$$

represents the ratio between the scaled chip area A and the chip area of the reference module *Infineon FZ600R17KE4* A_{ref}. The values are initialized with the minimum possible values. The minimum possible value of the scaling factor is determined by the maximum allowed peak current density in the module and the maximum peak branch current of all operating points. The maximum allowed density is defined to be triple that of the rated current density. Above this current density the module might become saturated[1)].

Once the scaling factors are assigned, the losses in each of the modules and for each of the investigated operating points of a single study case are calculated. Afterwards, the losses are fed into the thermal model to obtain the maximum temperature difference between the junction temperature and the sink temperature $\Delta\vartheta_{\mathrm{j,s}}$ as well as the temperature variation $\Delta\vartheta_{\mathrm{j}}$ at the IGBT's and diode's junctions.

Next, the two modules with the highest temperature differences in the upper switch and in the lower switch are identified. Higher priority is given either to the junction-sink temperature $\Delta\vartheta_{\mathrm{j,s}}$ or to the junction temperature variation $\Delta\vartheta_{\mathrm{j}}$, depending on which temperature value exceeds its boundary values specified for the IGBT and the diode ($\Delta\vartheta_{\mathrm{j,s,max}}$ and $\Delta\vartheta_{\mathrm{j,max}}$, respectively) with a higher absolute difference.

If both $\Delta\vartheta_{\mathrm{j,s}}$ and $\Delta\vartheta_{\mathrm{j}}$ are within their limits ($\Delta\vartheta_{\mathrm{j,s,max}}$ and $\Delta\vartheta_{\mathrm{j,max}}$, with an accuracy of 0.05 K) in both the upper and lower modules, the scaling process ends and the results are saved. If this is not the case, a new scaling factor is determined for the upper or lower switch (or both) and the process is repeated.

The new scaling factors are determined using only the single module with the highest temperature. At the beginning, the scaling factor is doubled, until the module has an acceptable $\Delta\vartheta_{\mathrm{j,s}}$ and $\Delta\vartheta_{\mathrm{j}}$. Once this has been achieved, the scaling factor is determined using a bisection searching algorithm in 10 iteration steps. This algorithm can be applied because the temperature is expected to rise monotonically with a decreasing scaling factor.

8.3.2 Loss Model

After each simulation, the raw data, i.e. the vectors including the switching states of particular modules for discrete points in time and the branch currents for discrete points in time, is processed to obtain the vectors of currents causing losses in all semiconductor devices of each module. These resulting vectors can later be used to determine the switching and conduction losses in each device for different chip area scaling factors without needing to process the vectors with switching states and branch currents again [see Figure 8.2].

Table 8.3 shows how the current passing through the module's semiconductor devices, causing the conduction losses, is determined in each discrete point in time k. The module labels are those from Section 2.1. Variable s represents the switching state of the investigated MMC module. T1 is the upper IGBT and T2 is the lower IGBT. D1 and D2 are their respective anti-parallel diodes. These current vectors are further used to determine the conduction losses in the particular switches for each discrete point in time.

[1)] The modules are usually defined only up to double the value of the rated current, since this is required for the most of applications. Generally, a typical IGBT module can be operated safely up to currents three times higher than the rated current. Nevertheless, the short-circuit capability and other properties may not be guaranteed anymore.

Table 8.3: Determination of currents through particular devices of a single MMC module, which are used for calculation of conduction losses.

	$s(k)=1$		$s(k)=0$	
	$i_\mathrm{b}(k)>0$	$i_\mathrm{b}(k)\leq 0$	$i_\mathrm{b}(k)>0$	$i_\mathrm{b}(k)\leq 0$
$i_{\mathrm{T1}}(k)$	0	$\lvert i_\mathrm{b}(k)\rvert$	0	0
$i_{\mathrm{D1}}(k)$	$\lvert i_\mathrm{b}(k)\rvert$	0	0	0
$i_{\mathrm{T2}}(k)$	0	0	$\lvert i_\mathrm{b}(k)\rvert$	0
$i_{\mathrm{D2}}(k)$	0	0	0	$\lvert i_\mathrm{b}(k)\rvert$

The conduction losses of an IGBT $p_\mathrm{T}(k)$ for a point in time k are calculated by multiplying the IGBT current $i_\mathrm{T}(k)$ by the voltage drop over the transistor $v_\mathrm{T}(k)$. Similarly, the conduction losses of a diode p_D are calculated by multiplication of the diode current $i_\mathrm{D}(k)$ and the diode voltage drop $v_\mathrm{D}(k)$. The voltage drops are determined by scaling the characteristics of the IGBT $v_{\mathrm{T,ref}}$ and the diode $v_{\mathrm{D,ref}}$ given for the module *Infineon FZ600R17KE4* in [145] and displayed in Figure 8.4. The main idea behind the chip area scaling, presented e.g. in [147], is that the voltage drop over a semiconductor device is determined by the current density in the device. Consequently, this voltage drop can be calculated using the reference voltage value from a datasheet by determining an equivalent device current, leading to the same current density as in the scaled device. Finally, the calculation of the conduction losses can be expressed by the following two equations:

$$p_\mathrm{T}(a,k) = i_\mathrm{T}(k)\cdot v_{\mathrm{T,ref}}\left(i_\mathrm{T}(k)\cdot\frac{1}{a}\right) \quad , \tag{8.2}$$

$$p_\mathrm{D}(a,k) = i_\mathrm{D}(k)\cdot v_{\mathrm{D,ref}}\left(i_\mathrm{D}(k)\cdot\frac{1}{a}\right) \quad . \tag{8.3}$$

A similar principle can be applied to determine the switching losses. In the first step, the current vectors, which sample the device currents during their switching, are determined for each point in time k according to Table 8.4. The semiconductor switching is detected when $s(k)\neq s(k+1)$.

Table 8.4: Determination of currents occuring at particular devices of a single MMC module during the switching instants. These currents are further used for calculation of switching losses.

	$s(k)=1$ & $s(k+1)=0$		$s(k)=0$ & $s(k+1)=1$		else
	$i_\mathrm{b}(k)>0$	$i_\mathrm{b}(k)\leq 0$	$i_\mathrm{b}(k)>0$	$i_\mathrm{b}(k)\leq 0$	
$i_{\mathrm{T1,on}}(k)$	0	0	0	$\lvert i_\mathrm{b}(k)\rvert$	0
$i_{\mathrm{T1,off}}(k)$	0	$\lvert i_\mathrm{b}(k)\rvert$	0	0	0
$i_{\mathrm{D1,rec}}(k)$	$\lvert i_\mathrm{b}(k)\rvert$	0	0	0	0
$i_{\mathrm{T2,on}}(k)$	$\lvert i_\mathrm{b}(k)\rvert$	0	0	0	0
$i_{\mathrm{T2,off}}(k)$	0	0	$\lvert i_\mathrm{b}(k)\rvert$	0	0
$i_{\mathrm{D2,rec}}(k)$	0	0	0	$\lvert i_\mathrm{b}(k)\rvert$	0

If switching did not occur, the current value at position k is assigned the value zero. The currents $i_{\mathrm{T1,on}}(k)$ and $i_{\mathrm{T2,on}}(k)$ represent the currents for turn on loss calculation for upper and lower IGBTs. The currents $i_{\mathrm{T1,off}}(k)$ and $i_{\mathrm{T2,off}}(k)$ are used to determine the turn off losses of the IGBTs. The currents $i_{\mathrm{D1,rec}}(k)$ and $i_{\mathrm{D2,rec}}(k)$ determine the diodes' reverse recovery losses.

In the second step, the losses are determined for each point in time k by scaling the loss energies of the reference IGBT and the reference diode according to their datasheet values [145], displayed in Figure 8.4. Similar to the conduction losses, the equivalent current, leading to the same current density in the semiconductor device, is calculated according to the scaling factor. However, since the switching losses are also proportional to the chip area, the resulting switching loss energies have to be multiplied by the scaling factor:

$$p_{\mathrm{T,on}}(a,k) = E_{\mathrm{T,on,ref}}\left(i_{\mathrm{T,on}}(k)\cdot\frac{1}{a}\right)\cdot a\cdot\frac{1}{T_\mathrm{s}} \quad , \tag{8.4}$$

$$p_{\mathrm{T,off}}(a,k) = E_{\mathrm{T,on,ref}}\left(i_{\mathrm{T,off}}(k)\cdot\frac{1}{a}\right)\cdot a\cdot\frac{1}{T_\mathrm{s}} \quad , \tag{8.5}$$

$$p_{\mathrm{D,rec}}(a,k) = E_{\mathrm{D,rec,ref}}\left(i_{\mathrm{D,rec}}(k)\cdot\frac{1}{a}\right)\cdot a\cdot\frac{1}{T_\mathrm{s}} \quad . \tag{8.6}$$

The loss energy is assumed to be divided equally over the whole sampling period T_s, leading to discrete time power values. $E_{\mathrm{T,on,ref}}$ is the turn on energy of the reference IGBT, $E_{\mathrm{T,off,ref}}$ is the turn off energy of the reference IGBT, and $E_{\mathrm{D,rec,ref}}$ is the reverse recovery loss energy of the reference diode.

The resulting loss power waveforms of a single IGBT $p_{\mathrm{loss,T}}$ or a diode $p_{\mathrm{loss,D}}$ are calculated by adding the conduction loss power values to the switching loss power values for each point in time.

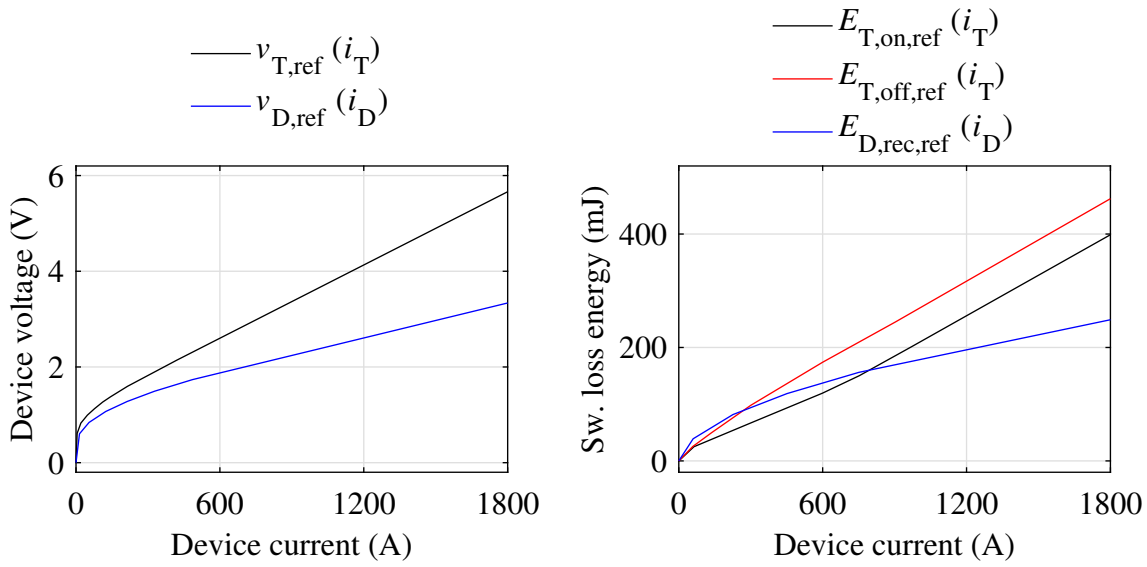


Figure 8.4: The voltage drop over the reference diode and the reference IGBT versus the current flowing through them (left). The switching losses of the reference IGBT and the reference diode versus the current passing through them, during the switching event (right). The characteristics are obtained from datasheet [145] and are linearly extrapolated above 1200 A. The characteristics are assuming a constant junction temperature of 125 °C and a capacitor voltage of 900 V for switching losses.

In the loss-model implementation, the datasheet characteristics ($v_{\mathrm{T,ref}}(i_\mathrm{T})$, $v_{\mathrm{T,ref}}(i_\mathrm{D})$, $E_{\mathrm{T,on,ref}}(i_\mathrm{T})$, $E_{\mathrm{T,off,ref}}(i_\mathrm{T})$, and $E_{\mathrm{D,rec,ref}}(i_\mathrm{D})$) acquired from datasheet [145] are sampled in 9000 equal steps. To increase the speed of calculation, a nearest value is used instead of interpolation between two values. The characteristics are extrapolated above the double nominal current (1200 A) up

to the triple nominal current (1800 A). The characteristics for a junction temperature of 125 °C and a blocked voltage of 900 V are used. Neither the temperature nor the module capacitor voltage are used to dynamically update the reference loss characteristics. The dependence of the voltage drops for conduction loss calculation and the switching loss energies of the reference devices on the device current are displayed in Figure 8.4.

8.3.3 Thermal Model

The thermal model of an IGBT and a diode is based on the series connection of four Foster-network sections between the junction and the case, which model the dynamic thermal impedance [see Figure 8.5]. The same model with different parameters can be used for both the diode and the IGBT. The parameters for these sections ($R_{\vartheta,\mathrm{ref},1..4}$ and $C_{\vartheta,\mathrm{ref},1..4}$) are obtained from the IGBT module datasheet [145]. Since the thermal capacitance of the sink is assumed to be very large $C_{\vartheta,\mathrm{s,ref}} \to \infty$, the case-to-sink temperature difference

$$\Delta\vartheta_{\mathrm{c,s}} = R_{\vartheta,\mathrm{s}} \cdot \left(\overline{p}_{\mathrm{loss,D}} + \overline{p}_{\mathrm{loss,T}}\right) \tag{8.7}$$

is assumed to be constant for each operating point and is determined by the mean losses of the diode $\overline{p}_{\mathrm{loss,D}}$ and of the transistor $\overline{p}_{\mathrm{loss,T}}$. As mentioned at the beginning of this chapter, the reference value of sink resistance $R_{\vartheta,\mathrm{s,ref}}$ is chosen to be 50 $\frac{\mathrm{mK}}{\mathrm{W}}$.

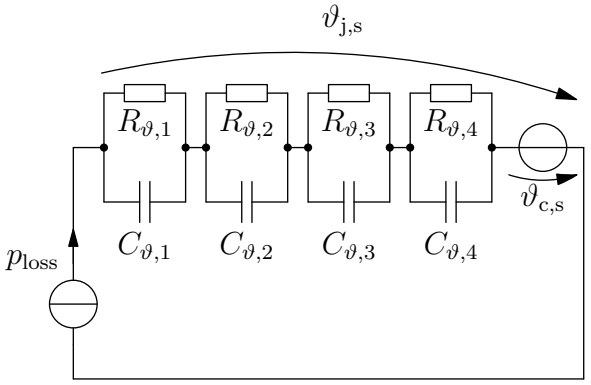


Figure 8.5: The foster network used to investigate the temperatures of the diode and the IGBT. The same model with different parameters can be used for both the diode and the IGBT. The loss power p_{loss} is either $p_{\mathrm{loss,D}}$ for a diode or $p_{\mathrm{loss,T}}$ for an IGBT.

The spatial thermal spreading is neglected and thus all thermal resistances and capacitances

$$R_{\vartheta}(a) = R_{\vartheta,\mathrm{ref}} \cdot \frac{1}{a} \tag{8.8}$$

$$C_{\vartheta}(a) = C_{\vartheta,\mathrm{ref}} \cdot a \tag{8.9}$$

can be scaled linearly with the chip area scaling factor [147]. Although this simplification diminishes the accuracy of the model, the impact on the results is not expected to be significant because the IGBT modules are typically constructed using several discrete chips. Furthermore, with this simplification, the calculation can be done even without an exact knowledge of the system's geometry.

An overview of the reference thermal parameters is given in Table 8.5.

Table 8.5: Overview of the reference thermal parameters for the thermal model.

	i	$R_{\vartheta,\mathrm{ref},i}$	$C_{\vartheta,\mathrm{ref},i}$
IGBT	1	2.8 mK/W	0.8 mJ/K
	2	10.7 mK/W	13 mJ/K
	3	28.3 mK/W	50 mJ/K
	4	3.2 mK/W	600 mJ/K
Diode	1	4.1 mK/W	0.8 mJ/K
	2	15.5 mK/W	13 mJ/K
	3	40.9 mK/W	50 mJ/K
	4	4.6 mK/W	600 mJ/K
Sink	s	50 mK/W	$\to \infty$

The rest of the thermal model, besides the constant case-to-sink temperature difference $\Delta\vartheta_{\mathrm{c,s}}$, is solved by a simple backward-euler integration. Since the foster-network approximation is used, each section can be calculated independently:

$$\vartheta_i(k+1) = \vartheta_i(k) + \frac{1}{C_{\vartheta,i}} \cdot \left(p_{\mathrm{loss}}(k+1) - \frac{\vartheta_i(k)}{R_{\vartheta,i}} \right) \cdot T_{\mathrm{s}}, \quad i \in 1..4 \quad . \tag{8.10}$$

The steady-state values are sought iteratively. Thus, the thermal model is calculated over the investigated time period multiple times for different initial temperature values $\vartheta_i(0)$. At the first iteration, the initial temperature values are calculated using the mean loss power:

$$\vartheta_i(0) = R_{\vartheta,i} \cdot \overline{p}_{\mathrm{loss}} \quad . \tag{8.11}$$

The initial temperature values of the next iteration are set according to the final values of the previous iteration. This process is repeated until the difference between the initial and the final values in all sections is smaller than one percent of the maximum temperature value, which was detected in the sections during the last iteration. Assuming that 50 % of the total junction-to-sink temperature can occur within a single Foster-network section, the worst-case accuracy of the model is 0.25 K for the semiconductors that do not exceed the defined maximum junction-to-sink temperature $\Delta\vartheta_{\mathrm{j,s,max}} = 50$ K.

8.3.4 Calculation of Input Capacitance

As mentioned several times in this thesis, a quasi-two-level PWM-operated MMC requires an input capacitor to filter the high-frequency components of input current. This can either be designed the same way as the dc-link capacitor of a two-level VSI, or the capacitance can be estimated using the simulation data. In the following investigations both options are considered.

The design of a dc-link capacitor for two-level VSIs has been studied comprehensively in the literature, e.g. [148]. This is advantageous for the quasi-two-level PWM operation of MMC, since the the dc-link capacitor can be designed similarly. The worst-case dc-link capacitance

$$C_{\mathrm{i}}^{\mathrm{ana}} = \frac{\sqrt{2} \cdot I_{\mathrm{sN}}}{4 \cdot \Delta V_{C\mathrm{i,max}} \cdot f_{\mathrm{PWM}}} \tag{8.12}$$

can be designed according to the peak output current $\sqrt{2} \cdot I_{\mathrm{sN}}$, the PWM frequency f_{PWM}, and the maximum allowed peak-to-peak voltage variation at the capacitor $\Delta V_{C\mathrm{i,max}}$ [149]. In the following investigations, the maximum allowed peak-to-peak voltage variation at the capacitor is selected to be 5 % of the input voltage:

$$\Delta V_{C\mathrm{i,max}} = 0.05 \cdot V_{\mathrm{i}} \quad . \tag{8.13}$$

The second option is to design the input capacitor by an estimation of its electric charge variation during each PWM period T_{PWM}. The electric charge

$$q(k+1) = q(k) + i_{C\mathrm{i}}(k) \cdot T_{\mathrm{s}} \tag{8.14}$$

can be calculated by a backward-euler integration of the current flowing through the capacitor

$$i_{C\mathrm{i}}(k) = i_{\mathrm{i}}(k) - \bar{i}_{\mathrm{i}} \quad , \tag{8.15}$$

which is calculated using the converter's input current (the sum of three leg currents) i_{i} and its mean value during the PWM period $\bar{i}_{\mathrm{i}}(k)$. The initial value of electric charge $q(0)$ can be assumed to be zero, since only the variation of the electric charge

$$\Delta q = \max(q) - \min(q) \tag{8.16}$$

is of interest. The maximum variation of electric charge $\Delta q_{\max}$ can be used to determine the required capacitor value

$$C_{\mathrm{i}}^{\mathrm{sim}} = \frac{\Delta q_{\max}}{\Delta V_{C\mathrm{i,max}}} \quad , \tag{8.17}$$

using the maximum allowed peak-to-peak voltage variation at the capacitor $\Delta V_{C\mathrm{i,max}}$.

Note that the input capacitor is not a part of time-domain simulations, since the models comprise ideal voltage sources. Nevertheless, it is included as a passive component for the design indicators.

The calculation of the RMS value of the input capacitor's current is presented in the next section.

8.3.5 Calculation of Design Indicators

The designed converters are compared according to the design indicators listed at the beginning of the chapter, indicating the converter costs, weight, and volume. In this section, their calculations are presented.

Total Chip Area of Semiconductor Switches and Relative Switching Power

The total relative chip area of semiconductor switches

$$a_{\mathrm{tot}} = n_{\mathrm{mod,tot}} \cdot (a_1 + a_2) \tag{8.18}$$

is calculated by summing the scaled chip area factor of the upper module a_1 and the lower module a_2 over all installed modules in the converter $n_{\mathrm{mod,tot}}$.

To enable a comparison of the relative chip areas for converters rated at different powers, the relative switching power

$$p_{\mathrm{sw,rel}} = \frac{a_{\mathrm{tot}} \cdot P_{\mathrm{sw,ref}}}{S_{\mathrm{N}}} \tag{8.19}$$

is evaluated. The relative switching power is the total switching power of the converter scaled to the converter's rated apparent power. The reference switching power

$$P_{\mathrm{sw,ref}} = 1700\ \mathrm{V} \cdot 600\ \mathrm{A} = 1.02\ \mathrm{MW} \tag{8.20}$$

is determined by multiplying the reference IGBT module's maximum collector-emitter voltage by its datasheet nominal current.

Total Energy Stored in Passive Components

The total energy in the passive components consists of three main components: The first component is the maximum energy stored in module capacitors

$$E_{C\mathrm{mod,tot}} = n_{\mathrm{mod,tot}} \cdot \frac{1}{2} \cdot C_{\mathrm{mod}} \cdot V_{C,\mathrm{max}}^2 \quad . \tag{8.21}$$

The second component is the maximum energy which can be stored in the inductors

$$E_{L,\mathrm{tot}} = n_{L\mathrm{leg,tot}} \cdot \frac{1}{2} \cdot L_{\mathrm{leg}} \cdot i_{\mathrm{leg,max}}^2 \quad , \tag{8.22}$$

determined by the number of leg inductors $n_{L\mathrm{leg,tot}}$ and the maximum leg current $i_{\mathrm{leg,max}}$ identified during simulations. The third component is the energy stored in the input capacitor

$$E_{C\mathrm{i}} = \frac{1}{2} \cdot C_{\mathrm{i}}^{\mathrm{ana}} \cdot \left(V_{\mathrm{i}} + \frac{1}{2} \cdot \Delta V_{C\mathrm{i,max}} \right)^2 \quad . \tag{8.23}$$

This component is assumed to be zero for the conventional operation of MMC. For quasi-two-level PWM operation of MMC and the two-level VSI, the input capacitance $C_{\mathrm{i}}^{\mathrm{ana}}$, which is calculated analytically according to (8.12), is used in (8.23).

To make the converters at different power levels comparable, the energies are described by the energy storage constant

$$H = \frac{E}{S_{\mathrm{N}}} \tag{8.24}$$

from [120], scaling the energy by the rated apparent power.

RMS Current of Module Capacitors and DC-Link Capacitor

The current through the n-th capacitor of a single branch

$$i_{C,n}(k) = s_n(k) \cdot i_\mathrm{b}(k) \tag{8.25}$$

can be calculated at time point k by multiplying the branch current i_b by the module's switching state s_n [see the switching state definition and module construction in Section 2.1].

The current through the dc-link capacitor at time point k

$$i_{C\mathrm{i}}(k) = i_\mathrm{i}(k) - \bar{i}_\mathrm{i} \tag{8.26}$$

is calculated similarly to the expression used in Section 8.3.4 by assuming that the capacitor buffers all high-frequency components of the input current i_i. In contrast to the previous section, the mean value of input current $\bar{i}_\mathrm{i}$ is calculated over one output period $1/f$.

The RMS current value for both module capacitors and dc-link capacitors is then calculated by a following generic discrete-time equation:

$$I = \sqrt{\frac{1}{k_\mathrm{max}} \cdot \sum_{k=1}^{k_\mathrm{max}} i(k)^2} \quad . \tag{8.27}$$

The highest RMS values are evaluated considering all operating points.

Output Current THD

The THD of the output current

$$\mathrm{THD}_i = \frac{\sqrt{I_\mathrm{o}^2 - I_\mathrm{o,FH}^2}}{I_\mathrm{o,FH}} \tag{8.28}$$

is calculated using the RMS value of the output current I_o and the RMS value of its fundamental harmonic $I_\mathrm{o,FH}$ over one output period $1/f$.

The fundamental harmonic is calculated using Fast Fourier Transformation (FFT). The converter output phase with the highest THD value is evaluated.

Converter Losses

The converter losses are extracted from the loss model for the final chip scaling. Similar to the energies stored in the passive components, the converter losses are scaled by the rated apparent power, leading to relative converter losses

$$\xi = \frac{P_\mathrm{loss,tot}}{S_\mathrm{N}} \quad . \tag{8.29}$$

Besides the converter losses, the converter efficiency

$$\eta_{\mathrm{N}} = 1 - \xi_{\mathrm{N}} \tag{8.30}$$

is also given for the rated operating point.

Note that only semiconductor losses are considered in these investigations. The losses in passive components are neglected.

8.4 Design of Quasi-Two-Level PWM-Operated MMC

In this section, the design process of quasi-two-level PWM-operated MMCs is shown step-by-step for the four study cases. The particular decisions made are discussed and the design results are presented.

The simulation model presented and validated in Chapter 6 is used for the investigations. Since the current ripple at the converter output is expected to be relatively low, predictive branch-energy control is employed. The converter and machine control implemented for this study was presented in Chapter 5.

Design Process

The first decision during the design of a quasi-two-level PWM-operated MMC is to select the **PWM frequency** applied to the MMC's output. In study cases A and C, the PWM frequency $f_{\mathrm{PWM}} = 1$ kHz is selected, since the machine's inductances are relatively high and the maximum stator frequency $f_{\mathrm{sN}} = 30$ Hz is sufficiently lower than the modulation frequency. Although the PWM frequency could be set lower for study cases B and D, it is set identically to study cases A and C ($f_{\mathrm{PWM}} = 1$ kHz), so that similar converters can be used in study cases A and B, and in study cases C and D. This decision is based on the expectation that the reduced converter losses due to the lower PWM frequency would not necessarily be lower than the increased harmonic losses in the machine [150].

Next, the **input voltage** value V_{i} is selected. The basis for this decision is the maximum required peak output voltage

$$\hat{v}^{*}_{\mathrm{o,max}} = \sqrt{\frac{2}{3}} \cdot \frac{1}{1-k_{\mathrm{cr}}} \cdot V_{\mathrm{sN}} \quad , \tag{8.31}$$

which is determined by the rated stator voltage and the dynamic control reserve factor k_{cr}, which is necessary for machine control. This is selected to be $k_{\mathrm{cr}} = 2$ % for all of the following investigations. The minimum required input voltage value

$$V_{\mathrm{i,min}} = \frac{2 \cdot \hat{v}^{*}_{\mathrm{o,max}}}{M_{\mathrm{max}}} \tag{8.32}$$

is further determined by the maximum achievable modulation index $M_{\max}$. Since the SVM is applied[2)], the maximum modulation index is

$$M_{\max} = \frac{2}{\sqrt{3}} \cdot \delta_{\max} \quad . \tag{8.33}$$

The maximum achievable duty cycle in study cases A and B is chosen to be:

$$\delta_{\max}^{\mathrm{A,B}} = 0.9 \quad , \tag{8.34}$$

which is a good trade-off for a low number of installed modules (low output voltages) [see the discussion on selection of the maximum achievable duty cycle in Section 4.2]. Since the number of modules is expected to be roughly double in study cases C and D, Section 4.2 recommends increasing the maximum achievable duty cycle, which is selected to be

$$\delta_{\max}^{\mathrm{C,D}} = 0.94 \quad . \tag{8.35}$$

This leads to a minimum input voltage value

$$V_{\mathrm{i,min}}^{\mathrm{A,B}} = 5.32 \text{ kV} \tag{8.36}$$

in study cases A and B, and

$$V_{\mathrm{i,min}}^{\mathrm{C,D}} = 10.17 \text{ kV} \tag{8.37}$$

in study cases C and D.

The **number of modules per branch**

$$n_{\mathrm{mpb}} \geq \frac{V_{\mathrm{i}}}{V_{C,\mathrm{min}}} \tag{8.38}$$

can be selected according to the maximum input voltage V_{i} and the minimum module capacitor voltage $V_{C,\mathrm{min}}$. Since the module energy variation is expected to be relatively low, only 5 % of the module is used for energy buffering. Hence, the minimum module capacitor voltage is $V_{C,\mathrm{min}} = 950$ V. This leads to

$$n_{\mathrm{mpb}}^{\mathrm{A,B}} = 6 \quad , \tag{8.39}$$

$$n_{\mathrm{mpb}}^{\mathrm{C,D}} = 11 \quad . \tag{8.40}$$

Note that the maximum voltage $V_{C,\mathrm{min}} \cdot n_{\mathrm{mpb}}$, which can be synthesized by modules of a branch in the worst case, should be slightly higher than the maximum input voltage in order to provide sufficient reserve for the leg current control. The **setpoint value of the capacitor voltage**

$$V_C^* = \frac{V_{C,\mathrm{min}} + V_{C,\mathrm{max}}}{2} = 975 \text{ V} \tag{8.41}$$

is selected as a mean value of the maximum and the minimum capacitor voltage.

The **leg inductance** is selected according to (4.14), derived in Section 4.2, by choosing the

[2)] In this study, the flat-top modulation is not considered as an option in order to mitigate the current THD.

relative value of the maximum compensating current to be $I_{\mathrm{b,c,rel}} = 0.5$. The rounded value of leg inductance for study cases A and B is

$$L_{\mathrm{leg}}^{\mathrm{A,B}} = 140\ \mu\mathrm{H} \tag{8.42}$$

and for study cases C and D is

$$L_{\mathrm{leg}}^{\mathrm{C,D}} = 160\ \mu\mathrm{H} \quad . \tag{8.43}$$

Since only the losses in semiconductors are considered in the presented investigations, the **branch resistance**

$$R_{\mathrm{b}} = 0 \tag{8.44}$$

is completely neglected.

The **HF modulation frequency** is determined according to (4.15), derived in Section 4.2. The maximum relative peak-to-peak branch current ripple is chosen to be $\Delta i_{\mathrm{b,r,rel}} = 8\ \%$ and the setpoint capacitor voltage value v_C^* is used for the calculation. The resulting rounded HF modulation frequency is

$$f_{\mathrm{HF}}^{\mathrm{A,B}} = f_{\mathrm{HF}}^{\mathrm{C,D}} = 25\ \mathrm{kHz} \quad . \tag{8.45}$$

If a lower HF modulation frequency is required, the output PWM frequency has to be set lower, the maximum achievable duty cycle has to be decreased or the allowed branch current ripple has to be increased. After these adjustments are made, the design must be repeated from the beginning.

The **module capacitance** C_{mod} can be calculated according to (4.16), derived in Section 4.2. The branch energy variation can be calculated according to (4.17) and the additional module energy variation, due to the switching delay, according to (4.19). The estimated maximum branch energy variation

$$\Delta e_{\mathrm{b,max}}^{\mathrm{A,B}} = 113.4\ \mathrm{J} \tag{8.46}$$

$$\Delta e_{\mathrm{b,max}}^{\mathrm{C,D}} = 129.6\ \mathrm{J} \tag{8.47}$$

is almost constant, since there are only minor differences between the peak branch currents and the leg inductances in study cases A, B, C, and D. Setting the **delay time between switching instants** to $T_{\mathrm{d}} = 1\ \mu\mathrm{s}$ for all study cases, the additional module energy variation due to the switching delays

$$\Delta e_{\mathrm{mod,d,max}}^{\mathrm{A,B}} = 6.36\ \mathrm{J} \tag{8.48}$$

$$\Delta e_{\mathrm{mod,d,max}}^{\mathrm{C,D}} = 12.72\ \mathrm{J} \tag{8.49}$$

is roughly proportional to the number of installed modules, and thus its value is double for study cases C and D compared to study cases A and B. Finally, the safety factor k_e, which accounts for the control reserve, is selected to be identical

$$k_e = 1.1 \tag{8.50}$$

in all study cases. Nevertheless, comparing the resulting module capacitances for study cases A and B

$$C_{\mathrm{mod}}^{\mathrm{A,B}} = 570\ \mu\mathrm{F} \tag{8.51}$$

and for study cases C and D

$$C_{\mathrm{mod}}^{\mathrm{C,D}} = 530\ \mu\mathrm{F} \quad , \tag{8.52}$$

it can be observed that despite the higher additional module energy variation due to delayed switching, study cases C and D require a lower module capacitance. This can be explained by observing the branch energy per module multiplied by the safety factor k_e

$$\Delta e_{\mathrm{b,max}}^{\mathrm{A,B}} / n_{\mathrm{mpb}}^{\mathrm{A,B}} \cdot k_e = 20.79\ \mathrm{J} \tag{8.53}$$

$$\Delta e_{\mathrm{b,max}}^{\mathrm{C,D}} / n_{\mathrm{mpb}}^{\mathrm{C,D}} \cdot k_e = 12.96\ \mathrm{J} \quad , \tag{8.54}$$

which is almost double for study cases A and B compared to study cases C and D. Furthermore, it can be recognized that the module capacitance in study cases A and B, with a lower number of modules per branch, is determined mainly by the branch energy variation. In contrast, the impact of the branch energy variation and the additional module energy variation due to the switching delays is approximately the same for study cases C and D, which require more modules per branch.

Finally, the **proportional gain of the energy controller** is $G_{\mathrm{P},e} = 1.2 \cdot f_{\mathrm{PWM}}$ and the **HF-current amplitude** is 1.5 % of the peak output current. Because predictive branch-energy control is applied, smart HF-current injection is selected. The threshold value for the smart HF-current injection is selected to be 50 % of the HF-current amplitude.

Design Results

The converter parameters discussed up to this point are summarized in Table 8.6. These are independent of the torque characteristics. The dc-link capacitance is calculated according to worst-case estimation (8.12), assuming the maximum allowed peak-to-peak voltage variation at the capacitor is 5 % of the input voltage value.

The parameters listed in Table 8.6 are further used in simulations to determine the output current's THD, the module capacitor's RMS current, the input capacitance, and the chip area scaling for the upper and the lower switches. These results are presented and discussed below.

It is only meaningful to evaluate the output-current THD when the rated output current is applied, since the current ripple is almost independent of the output current amplitude. Consequently, only the evaluation for the torque characteristic I is shown in Figure 8.6. The THD curves displayed in the figure are in concordance with the investigations performed in [140, 141] and are very similar to those expected for two-level VSIs. Since the PWM frequency is constant and the machine inductances are increased when the machines have lower rated speeds, study cases B and D have significantly lower output-current THD. If these THD values are unacceptable for the machine, the PWM frequency has to be increased. However, this requires a major redesign of the converter parameters, as discussed in the previous section.

Table 8.6: Simulation parameters of the **quasi-two-level PWM-operated MMCs**, designed for study cases A, B, C, and D. The parameters are identical for both load torque characteristics.

		Study Cases	
Parameter		A and B	C and D
Input voltage	V_i	5.32 kV	10.17 kV
Maximum allowed duty cycle	δ_max	0.9	0.94
Modules per branch	n_mpb	6	11
Leg inductance (coupled)	L_leg	140 µH	160 µH
Branch resistance	R_b	0	0
Module capacitance	C_mod	570 µF	530 µF
DC-link capacitance (analytic)	$C_\mathrm{i}^\mathrm{ana}$	797 µF	417 µF
PWM frequency	f_PWM	1 kHz	1 kHz
HF modulation frequency	f_HF	25 kHz	25 kHz
Setpoint module capacitor voltage	V_C^*	975 V	975 V
Delay between switch. instants	T_d	1 µs	1 µs
Energy controller gain	$G_{\mathrm{P},e}$	1200 $\frac{1}{\mathrm{s}}$	1200 $\frac{1}{\mathrm{s}}$
HF current amplitude	$\hat{i}_\mathrm{HF}$	12.7 A (smart.)	12.7 A (smart)
HF current threshold	$I_\mathrm{c,thr}$	6.4 (smart)	6.4 (smart)

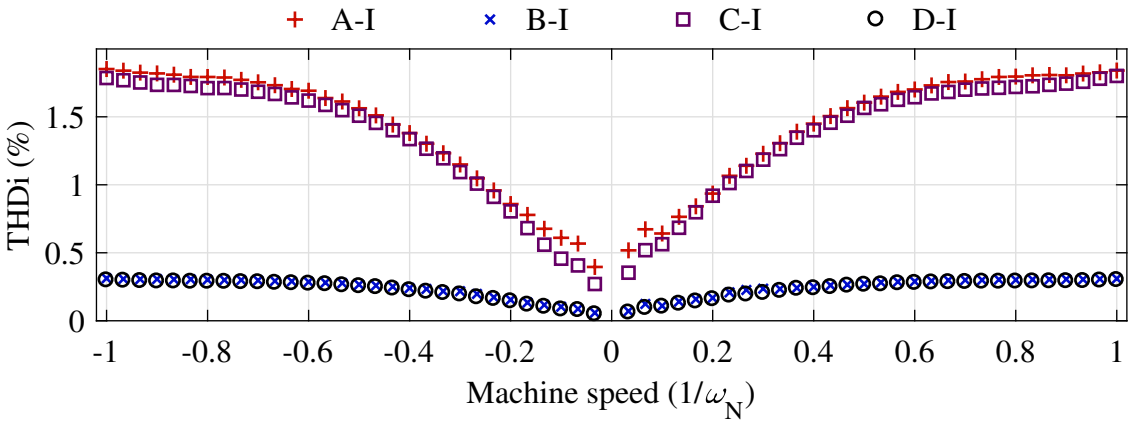


Figure 8.6: Output current THD of the quasi-two-level PWM-operated MMCs with load torque characteristic I.

Table 8.7 shows the results of the chip scaling and the calculation of the input capacitance. The estimated capacitances in the simulations $C_\mathrm{i}^\mathrm{sim}$, listed in Table 8.7, are lower than the worst-case analytic value $C_\mathrm{i}^\mathrm{ana}$ from Table 8.6.

Several observations can be made for the scaling factors: First, the scaling factors for upper switches a_1 are significantly lower than the scaling factors for the lower switches a_2, and their values are approximately constant for all study cases. This is because the upper switch conducts the maximum branch current for a very short period of time – only during transition states. Consequently, the chip area is determined by the maximum current density in the switches, rather than by the thermal properties. This is further supported by Figures 8.7 and 8.8, showing the maximum temperature differences and variations for both switches at all operated points. As these figures show, the maximum junction-sink temperature never reaches its limit $\Delta\vartheta_\mathrm{j,s,max} = 50$ K and the maximum variation of the junction temperature is reached

Table 8.7: Resulting scaling factors a_1 and a_2 and resulting input capacitance (calculated from simulation data) $C_\mathrm{i}^\mathrm{sim}$ for **quasi-two-level PWM-operated MMCs** designed for all study cases.

	Study Cases							
	A-I	A-II	B-I	B-II	C-I	C-II	D-I	D-II
a_1 (-)	0.69	0.69	0.74	0.64	0.73	0.73	0.75	0.60
a_2 (-)	2.21	1.55	3.22	2.99	2.22	1.53	3.25	3.06
$C_\mathrm{i}^\mathrm{sim}$ (µF)	460	459	464	461	243	243	244	241

$\Delta\vartheta_\mathrm{j,max} = 15$ K only with study cases B and D. Remember that the variation of the junction temperature is used as a limit first for the machine speeds above 20 % of the rated.

Second, the scaling factor for lower switches a_2 is almost independent of the output voltage, as the study cases A-I, A-II, B-I, and B-II lead to almost the same results as study cases C-I, C-II, D-I, and D-II, respectively. This is further supported by the fact that the respective temperature characteristics displayed in Figure 8.7 and Figure 8.8 are almost identical.

Third, the scaling factor for lower switches a_2 is higher when the machine's rated speed is decreased, as study cases A-I, A-II, C-I, and C-II lead to significantly lower scaling factors a_2 than study cases B-I, B-II, D-I, and D-II, respectively. This is because the lower machine speeds (study cases B and D) lead to more severe junction temperature variation, as visible in Figures 8.7 and 8.8.

Fourth, a constant torque characteristic (characteristic I) leads to higher scaling factors of lower switches a_2 than the quadratic characteristic (characteristic II), as study cases A-I, B-I, C-I, and D-I have higher scaling factors than study cases A-II, B-II, C-II, and D-II, respectively. This is because the converter's output currents are significantly lower with quadratic torque characteristic when the machine speeds are low. It can also be observed that the difference between the scaling factors for study cases A-I and A-II, and study cases C-I and C-II is higher than for study cases B-I and B-II, and study cases D-I and D-II. This is because the study cases B-I and D-I already have relatively high scaling factors.

The scaling factors from Table 8.7 are further used to determine the total chip area and the relative switching power, which is one of the design indicators.

The design indicators for all study cases are listed in Table 8.8. Besides the indicators, the table also lists the total chip area and shows how the total energy in passive components is split between the particular component types.

The relative switching power mainly reflects the findings for the chip area scaling: the constant torque characteristic (characteristic I) requires more switching power than the quadratic torque characteristic (characteristic II), and the machines with lower rated speeds lead to higher switching powers. Nevertheless, study cases C and D have lower relative switching powers than study cases A and B, respectively. Since higher duty cycles are achievable with study cases C and D, the number of modules per output voltage is lower. Hence, with a higher number of modules per branch, the relative switching power also decreases.

It can be observed that the quasi-two-level PWM operated MMCs with higher output voltages (higher number of modules per branch) generally have smaller components and higher efficiency

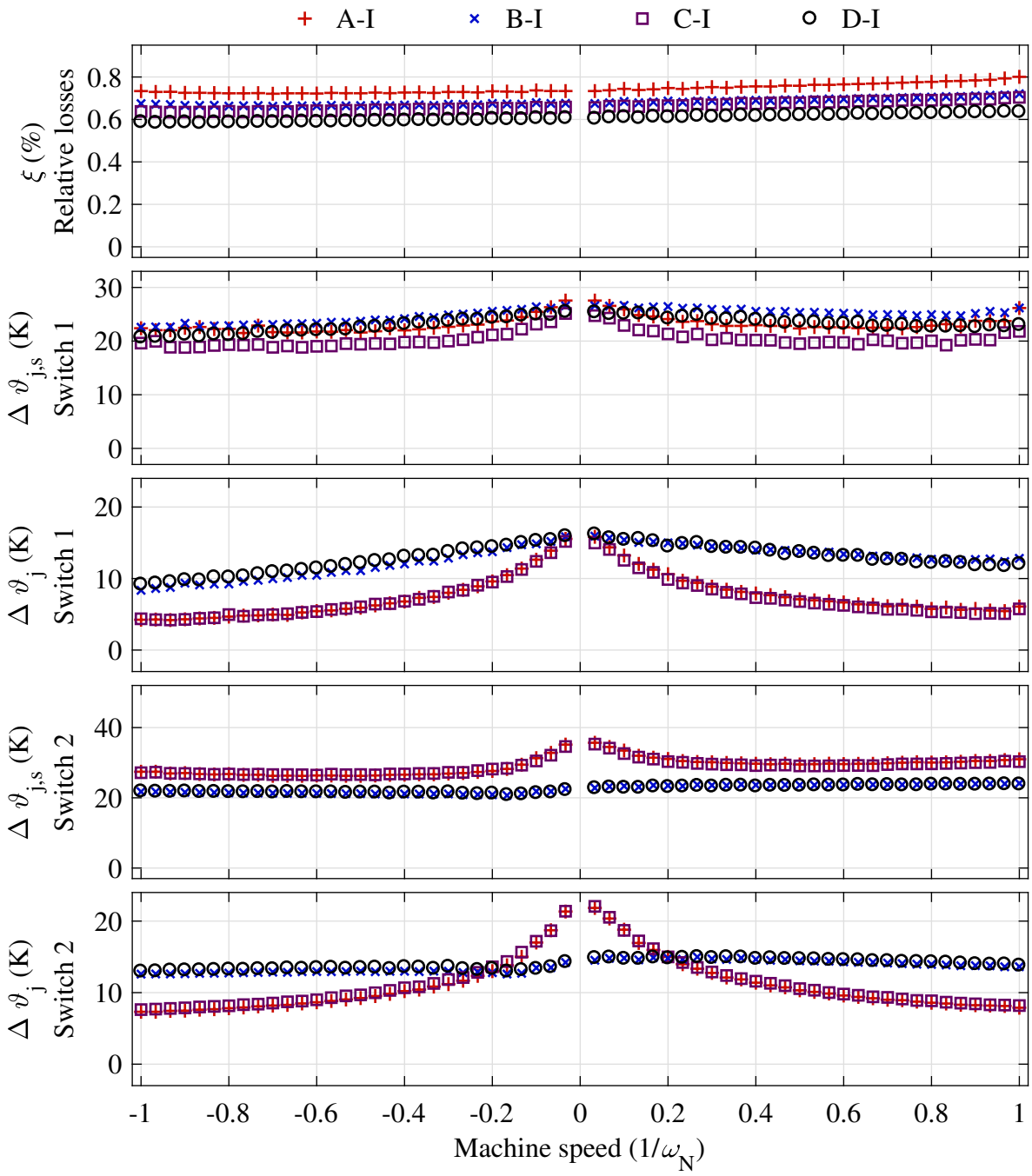


Figure 8.7: The relative total losses and the maximum temperatures in upper and lower switches (switch 1 and 2, respectively) of the quasi-two-level PWM-operated MMCs with load torque characteristic I.

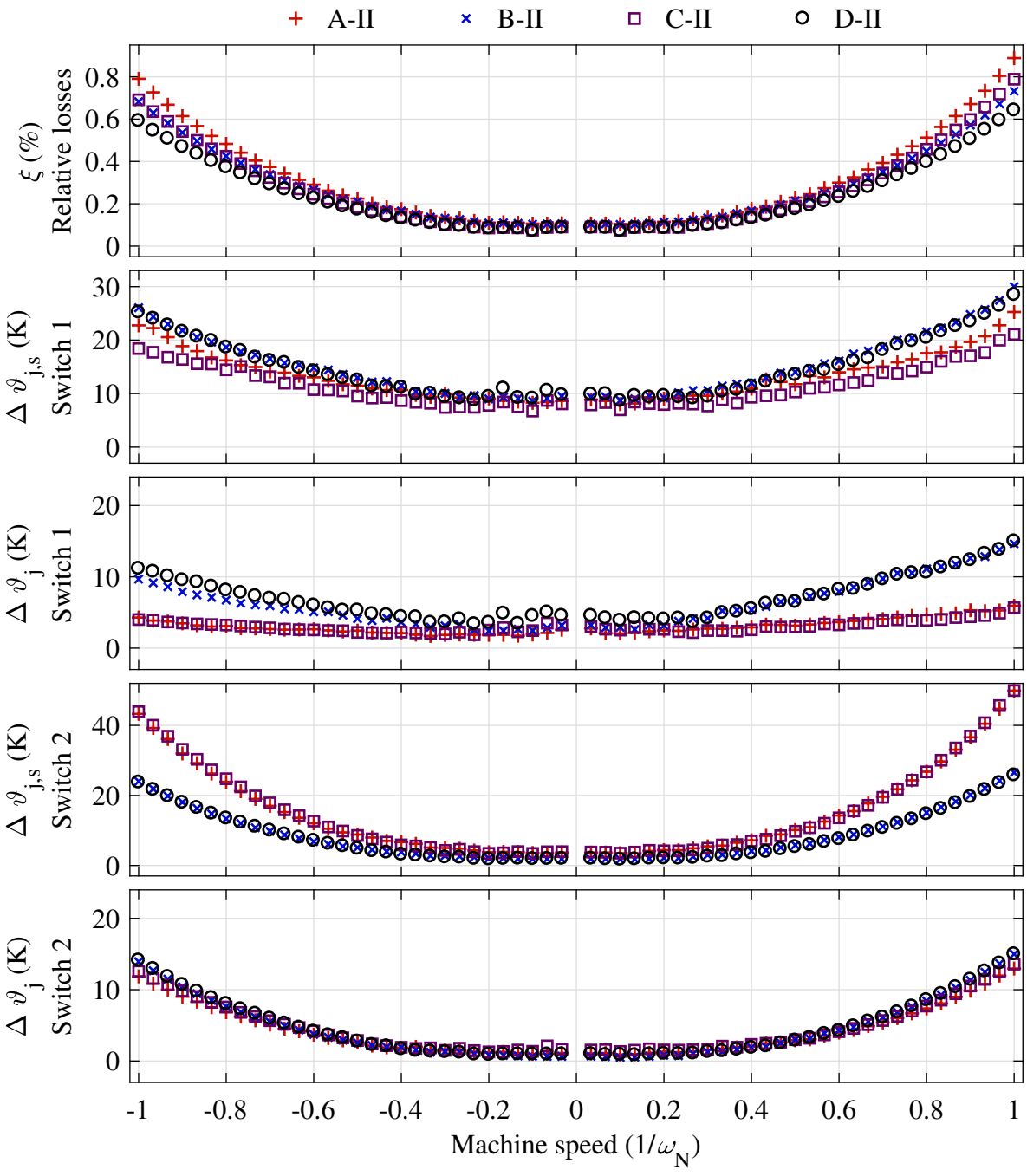


Figure 8.8: The relative total losses and the maximum temperatures in upper and lower switches (switch 1 and 2, respectively) of the quasi-two-level PWM-operated MMCs with load torque characteristic II.

Table 8.8: Design indicators for the **quasi-two-level PWM-operated MMCs**, designed for study cases A..D and both characteristics of load torque.

Torque Characteristic I

		Study Cases			
		A-I	B-I	C-I	D-I
Relative switching power	$p_{\mathrm{sw,rel}}$ (-)	31.0	42.3	29.0	39.2
Total energy in pass. components	H_{tot} (ms)	6.49	6.48	5.88	5.88
Mod. capacitor RMS current	$I_{C,\mathrm{mod}}$ (A)	59.9	55.4	50.1	46.5
Output current THD at ω_{N}	THD_i (%)	1.84	0.31	1.80	0.30
Converter efficiency at ω_{N}	η_{N} (%)	99.20	99.28	99.30	99.36
Input capacitor RMS current	$I_{C\mathrm{i}}$ (A)	378	373	374	371
Total chip area (relative to A_{ref})	a_{tot} (-)	104	142	195	263
Energy in module capacitors	$H_{C\mathrm{mod,tot}}$ (ms)	2.99	2.99	2.55	2.55
Energy in inductors	$H_{L,\mathrm{tot}}$ (ms)	0.04	0.03	0.03	0.02
Energy in dc-link capacitor	$H_{C\mathrm{i}}$ (ms)	3.46	3.46	3.30	3.31

Torque Characteristic II

		Study Cases			
		A-II	B-II	C-II	D-II
Relative switching power	$p_{\mathrm{sw,rel}}$ (-)	24.0	38.8	22.2	35.9
Total energy in pass. components	H_{tot} (ms)	6.49	6.48	5.88	5.88
Mod. capacitor RMS current	$I_{C,\mathrm{mod}}$ (A)	59.9	55.5	49.7	46.2
Output current THD at ω_{N}	THD_i (%)	1.84	0.31	1.80	0.30
Converter efficiency at ω_{N}	η_{N} (%)	99.11	99.27	99.21	99.36
Input capacitor RMS current	$I_{C\mathrm{i}}$ (A)	339	334	317	314
Total chip area (relative to A_{ref})	a_{tot} (-)	80.8	131	150	241
Energy in module capacitors	$H_{C\mathrm{mod,tot}}$ (ms)	2.99	2.99	2.55	2.55
Energy in inductors	$H_{L,\mathrm{tot}}$ (ms)	0.04	0.03	0.03	0.02
Energy in dc-link capacitor	$H_{C\mathrm{i}}$ (ms)	3.46	3.46	3.30	3.31

than those with lower voltage. This can be observed for all indicators in Table 8.8 when comparing study case A with study case C, and study case B with study case D.

Comparing the total amount of energy stored in the particular converters H_{tot} for different study cases in Table 8.8, it can be stated that the value is almost independent of the rated machine speed and torque characteristic, which is one of the main advantages of quasi-two-level PWM operation. Similarly, the maximum module capacitor RMS current is almost independent of these parameters as well.

An interesting observation is that more than a half of the total amount of energy in passive components H_{tot} is stored in the input capacitor. Furthermore, the energy which can be stored in inductors is almost negligible, which is typical for MMCs.

The input capacitor RMS current is higher for torque characteristic I than for torque characteristic II, which is an occurrence that is also expected for two-level VSIs.

In the next sections, the design is repeated for the conventional operation of MMC, two-level VSI, and MMMC. The resulting design indicators are compared to those of quasi-two-level

PWM-operated MMCs.

The designed converters are also tested in dynamic conditions for a machine start-up in Appendix F. In conclusion, the simulations conducted validate the designed converters.

8.5 Comparison to Conventional Operation Modes of MMC

In this section, the design process of conventionally operated MMCs, which utilize LFM, IPM, and normal operation mode, is presented. Since the conventional operation modes are not well-suited for very low rated operation frequencies [27], only an investigation of study cases A and C, which are have higher rated stator frequency, is accomplished.

The modeling of the converter and machine is identical to that of quasi-two-level PWM-operated MMC. The machine control also remains unchanged. The converter control is based on the generalized control theory for a class of modular multilevel topologies, as described in Section 2.3. The modulation is based on a two step approach [see Section 2.2.2 for further details], with module capacitor balancing restricting the frequent module switching, similar to [53]. The applied operation modes are explained in Section 2.5.

Since the components of the branch currents and branch voltages contain two independent non-zero frequencies when LFM is applied, the loss and thermal model might become inaccurate if the data is investigated over only one machine electrical period. Consequently, longer simulation times are applied. The investigation time period is selected to be an integer multiple of the machine electrical period so that at least 20 periods of the HF injected common-mode voltage are investigated.

Design Process

The **input voltage** V_i for conventional operation modes of half-bridge MMC is designated similarly to the selection process for the quasi-two-level PWM-operated MMCs. The main difference is the higher achievable duty cycle index being $\delta_\mathrm{max} = 0.98$. This is selected to be slightly below one to leave a small reserve for internal MMC control. Consequently, the input voltages for study case A and study case C

$$V_\mathrm{i}^\mathrm{A} = 4.9\ \mathrm{kV} \tag{8.55}$$

$$V_\mathrm{i}^\mathrm{C} = 9.8\ \mathrm{kV} \tag{8.56}$$

are lower than those of quasi-two-level PWM operated MMCs.

The **number of modules per branch** can be determined in a same way as for quasi-two-level PWM operation, according to (8.38). Nevertheless, since higher module energy variation is expected with conventional operation modes, higher voltage variation at the module capacitor is allowed. As a result, 17 % of the maximum module capacitor voltage is used for energy buffering, which represents a good trade-off between the module capacitance and the number of installed modules per branch. This leads to a minimum voltage $V_{C,\mathrm{min}} = 830$ V and to a voltage

setpoint of $V_C^* = 915$ V. The number of installed modules per branch in study case A and study case C is

$$n_{\mathrm{mpb}}^{\mathrm{A}} = 6 \tag{8.57}$$

$$n_{\mathrm{mpb}}^{\mathrm{C}} = 12 \quad . \tag{8.58}$$

Depending on the machine speed, different **operation modes** are applied. An overview of the application ranges for the particular modes, depending on machine speed, is displayed in Figure 8.9. When the speed is above approximately 0.7 of the rated speed, the normal operation mode is applied, reducing the converter's currents. Below this frequency, the IPM is applied. As shown in Figure 8.9, the circulating currents required by IPM are not deactivated instantaneously, but linearly decreased between approximately 0.6 and 0.7 of ω_{N}. Below a speed of approximately $0.4 \cdot \omega_{\mathrm{N}}$, the LFM is applied. IPM is not deactivated, since it is a part of LFM [see derivation in Section 2.5]. Furthermore, the additional currents caused by LFM are decreased slowly between the speeds of ≈ 0.3 and ≈ 0.4 of ω_{N}. The additional square-wave common-mode voltage necessary for LFM is deactivated linearly together with the currents. The speed at which the LFM is deactivated is chosen as a trade-off between the maximum branch currents and the branch energy variation. These trade-offs are discussed and demonstrated in [95].

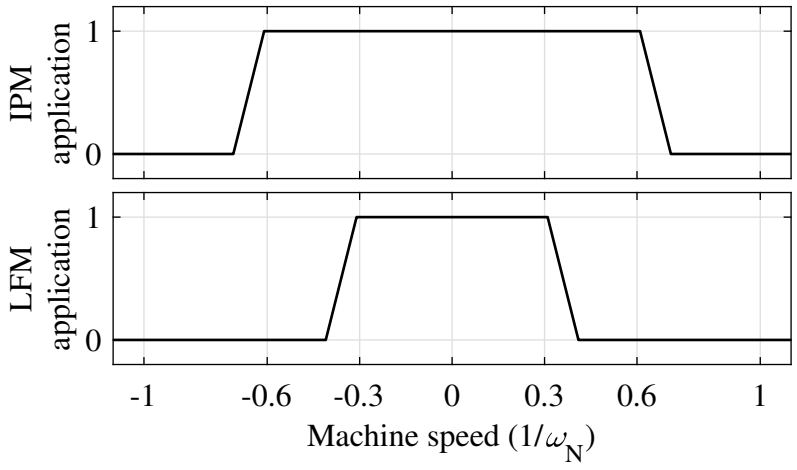


Figure 8.9: Application of LFM and IPM dependent on the machine speed. The resulting factor is multiplied with the operation modes' common-mode voltages and circulating currents.

The **frequency of the common-mode voltage for LFM** is selected to be $f_{\mathrm{HF}} = 50$ Hz, since this value provides sufficient reduction of the branch energy variation at low frequencies. Higher frequencies are undesirable, since they would increase the switching losses and require a higher modulation frequency. The **amplitude of common-mode voltage**

$$\hat{v}_{\mathrm{cm,HF}} = 0.9 \cdot \frac{\sqrt{3}}{2} \cdot \sqrt{\frac{2}{3}} \cdot V_{\mathrm{sN}} \cdot \frac{|\omega_{\mathrm{N}} - \omega|}{\omega_{\mathrm{N}}} \tag{8.59}$$

is chosen to be 90 % of the theoretically available value to provide a sufficient voltage margin for the circulating-current controller. The factor $\frac{\sqrt{3}}{2}$ is applied due to the SVM.

Since the branch powers are open-loop controlled during LFM, circulating currents have to be controlled very precisely. Consequently, a high cutoff frequency of the circulating-current

controller is necessary. Hence, the control and **modulation frequency** is chosen to be $f_\mathrm{m} = 5$ kHz. As mentioned above, a two step modulation approach with restricted module switching is applied.

The leg inductance is calculated by extending (4.15), derived for quasi-two-level PWM-operation. Unlike with quasi-two-level PWM-operation, both branches contribute to current ripple, and thus the leg inductance

$$L_\mathrm{leg} = \frac{1}{2} \cdot \frac{V_C}{f_\mathrm{m} \cdot \Delta i_\mathrm{b,r,max}} \tag{8.60}$$

is doubled for identical modulation frequency and current ripple. The maximum relative current ripple is selected identically to the previous case: $\Delta i_\mathrm{b,r,rel} = 8\ \%$. The resulting leg inductance is

$$L_\mathrm{leg}^\mathrm{A,C} = 1.36\ \mathrm{mH} \quad . \tag{8.61}$$

Although the **module capacitance** C_mod can be determined analytically, this process is relatively complex due to the high number of operation modes. In this thesis, it is determined using simulations. First, the capacitance is chosen to have some high value (e.g. 100 mF) and the simulations are performed to determine the maximum module energy variation. This value is then used to determine the final module capacitance.

Design Results

The parameters resulting from the design process described above are summarized in Table 8.9. These are further used in simulations to determine the chip area scaling factors, which are listed for all investigated study cases in Table 8.10.

Table 8.9: Simulation parameters of **conventionally operated MMCs**, designed for study cases A and C. Aside from the module capacitance, the parameters are identical for both load torque characteristics.

		Study Cases	
Parameter		A	C
Input voltage	V_i	4.9 kV	9.8 kV
Modules per branch	n_mpb	6	12
Leg inductance (coupled)	L_leg	1.36 mH	1.36 mH
Branch resistance	R_b	0	0
Module capacitance (char. I)	C_mod	34 mF	34 mF
Module capacitance (char. II)	C_mod	10.5 mF	10.5 mF
DC-link capacitance	C_i	0	0
Modulation frequency	f_m	5 kHz	5 kHz
Setpoint module capacitor voltage	V_C^*	915 V	915 V

The data from Table 8.9 and Table 8.10 can be further evaluated to determine the design indicators. These are listed in Table 8.11.

Table 8.10: Resulting scaling factors a_1 and a_2 for **conventionally operated MMCs** designed for study cases A and C.

	Study Cases			
	A-I	A-II	C-I	C-II
a_1 (-)	1.69	0.63	1.47	0.63
a_2 (-)	3.58	1.32	3.33	1.22

Table 8.11: Design indicators for the **conventionally operated MMCs**, designed for study cases A and C and both characteristics of load torque.

		Study Cases			
		A-I	A-II	C-I	C-II
Relative switching power	$p_{\mathrm{sw,rel}}$ (-)	55.3	20.9	51.4	19.8
Total energy in pass. components	H_{tot} (ms)	179	55.1	179	55.1
Mod. capacitor RMS current	$I_{C,\mathrm{mod}}$ (A)	262	155	261	163
Output current THD at ω_{N}	THD_i (%)	0.07	0.06	0.04	0.04
Converter efficiency at ω_{N}	η_{N} (%)	99.32	99.18	99.44	99.26
Total chip area (relative to A_{ref})	a_{tot} (-)	189	70.4	349	133
Energy in module capacitors	$H_{C\mathrm{mod,tot}}$ (ms)	178	55.1	178	55.1
Energy in inductors	$H_{L,\mathrm{tot}}$ (ms)	0.56	0.03	0.28	0.02
Energy in dc-link capacitor	$H_{C\mathrm{i}}$ (ms)	0	0	0	0

Comparing the design indicators for study cases A-I and C-I with indicators of study cases A-II and C-II, it can be recognized that the constant load torque characteristic (characteristic I) leads to significantly higher switching power and energy stored in passive components than the quadratic load torque characteristic (characteristic II). This confirms the observations of Antonopoulus *et al.* presented in [103].

The higher efficiency at the rated point for the study cases with constant torque characteristic (A-I and C-I) is caused by the higher chip areas applied to the modules. These have to be high due to the operation at very low frequencies. Nevertheless, when normal operation mode is applied during high speeds, the conduction losses are significantly decreased, leading to higher efficiency.

In the next section the indicators of conventional operation modes of MMCs are compared to those of quasi-two-level PWM operation.

Similar to quasi-two-level PWM operation, the designed conventionally operated MMCs are tested in dynamic conditions for a machine start-up in Appendix F.

Comparisons to Quasi-Two-Level PWM Operation

The designed indicators of quasi-two-level PWM operation of MMC from Table 8.8 and of conventional operation of MMC from Table 8.11 are graphically compared in Figure 8.10.

The figure clearly shows that quasi-two-level PWM operation leads to a significantly lower amount of energy stored in passive components and lower module capacitors' RMS currents.

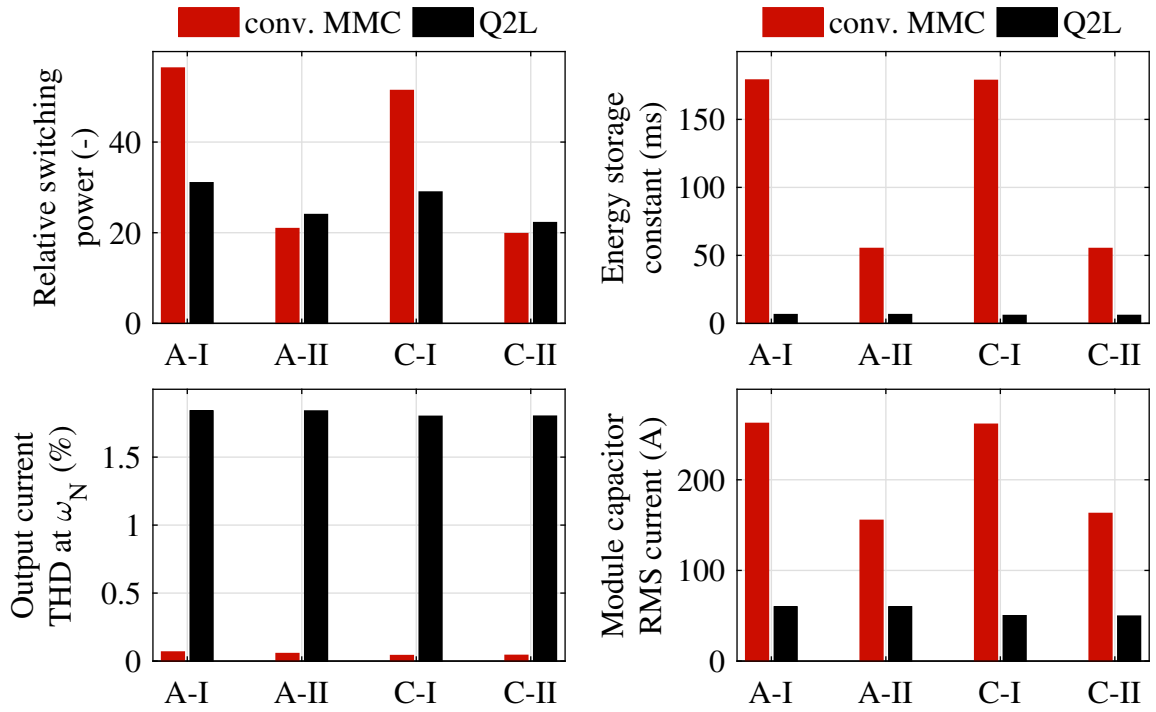


Figure 8.10: Comparison of design indicators of conventional operation of MMC (denoted as "conv. MMC" and plotted in red) and quasi-two-level PWM operation (denoted as "Q2L" and plotted in black) for study cases A-I, A-II, C-I, and C-II.

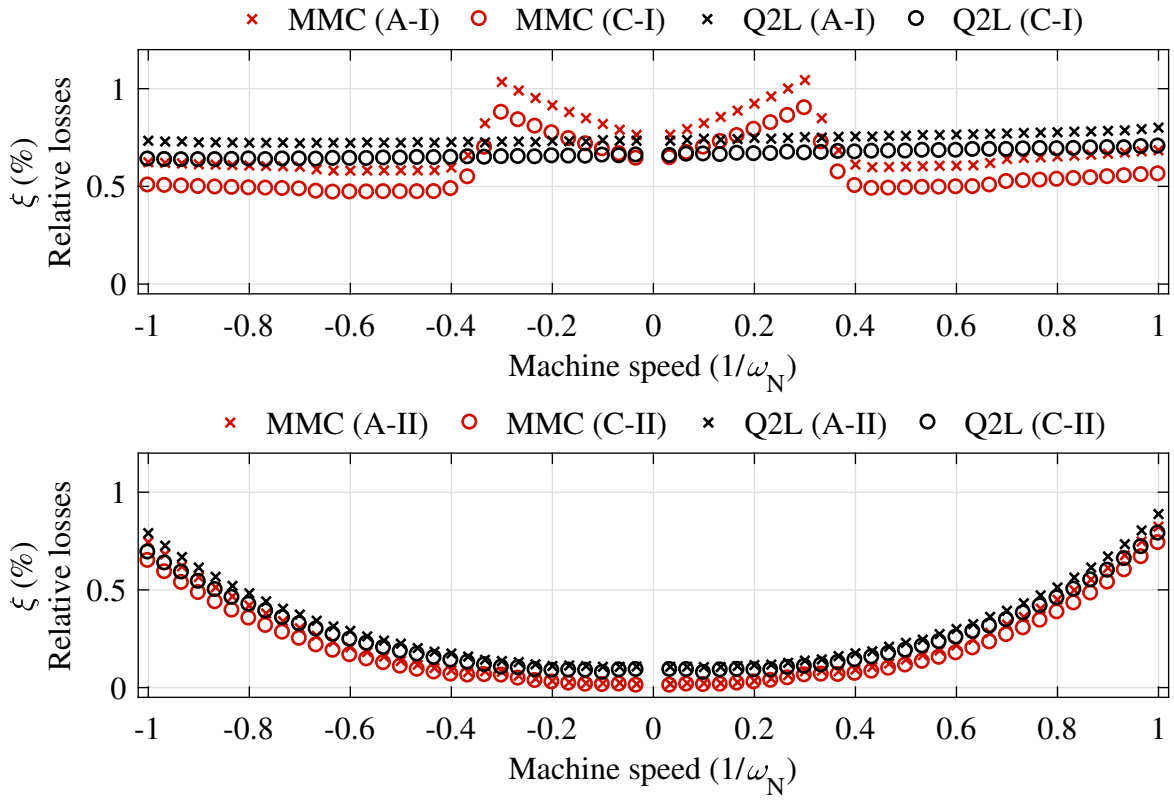


Figure 8.11: Comparison of relative converter losses ξ of conventional operation of MMC (denoted as "MMC" and plotted in red) and quasi-two-level PWM operation (denoted as "Q2L" and plotted in black) for study cases A-I, A-II, C-I, and C-II.

On the other hand, as expected, the output current distortion is significantly higher for quasi-two-level PWM operation. The installed switching power is slightly higher with quasi-two-level PWM operation compared to conventional operation when quadratic load torque characteristic is applied (study cases A-II and C-II). However, if constant load torque characteristic is applied (study cases A-I and C-I), the quasi-two-level PWM operation requires significantly lower switching power.

The comparison of relative converter losses is depicted in Figure 8.11. For the study cases with quadratic torque characteristic (study cases A-II and C-II), the losses of conventionally operated MMCs are slightly lower than those of quasi-two-level PWM operation. This is because the MMC in normal operation mode has lower branch currents and the modules are switched less frequently (in quasi-two-level PWM operation all modules have to be switched at least once within one PWM period). The same argumentation can be applied to the study cases with constant torque characteristic (study cases A-I and C-I). However, the difference between the losses is even higher at the rated operating point. This is due to the relatively high chip area applied to conventionally operated MMCs, caused by high losses of LFM visible at approximately 30 % of rated speed.

8.6 Comparison to Two-Level VSI With Series-Connected IGBTs

Even though the two-level VSI would not be designed with the same low-voltage IGBT modules as the modular multilevel topologies, such a converter is a good reference for quasi-two-level PWM-operated MMC. Since the two-level VSI with series-connected switches represents the idealized quasi-two-level PWM operation, a comparison of these two converters can be used to evaluate the additional effort.

The converter is modeled using a simple two-level VSI model in *Plecs* without semiconductor dead-times. The machine and the machine control implementation is the same as in previous investigations. Each phase leg of the two-level VSI, consisting of a single half-bridge, is integrated into the chip area scaling model as a virtual MMC branch with a single half-bridge module. Hence, the same loss and thermal models can be applied as in the previous cases.

Design Process

The **input voltage** V_i can be calculated identically to the design process used for quasi-two-level PWM operation. Unlike for the quasi-two-level PWM operation of MMC, the duty cycle index $\delta_\mathrm{max} = 1$ is achievable. As a consequence, the input voltages

$$V_\mathrm{i}^{\mathrm{A,B}} = 4.8\ \mathrm{kV} \tag{8.62}$$

$$V_\mathrm{i}^{\mathrm{C,D}} = 9.6\ \mathrm{kV} \tag{8.63}$$

are lower than those of quasi-two-level PWM operated MMCs.

Assuming each of the modules can block up to 1 kV, the **number of series-connected IGBT modules** is

$$n_{\mathrm{s}}^{\mathrm{A,B}} = 5 \tag{8.64}$$

for study cases A and B, and

$$n_{\mathrm{s}}^{\mathrm{C,D}} = 10 \tag{8.65}$$

for study cases C and D.

The **PWM frequency** is identical to that of the quasi-two-level PWM-operated MMC

$$f_{\mathrm{PWM}} = 1\ \mathrm{kHz} \quad . \tag{8.66}$$

Design Results

The parameters designed in the last section are summarized in Table 8.12. These are used as

Table 8.12: Simulation parameters of **two-level VSI** with series-connected IGBT modules, designed for study cases A, B, C, and D. The parameters are identical for both load torque characteristics.

		Study Cases	
Parameter		A and B	C and D
Input voltage	V_{i}	4.8 kV	9.6 kV
Number of series-connected IGBTs	n_{s}	5	10
DC-link capacitance (analytic)	$C_{\mathrm{i}}^{\mathrm{ana}}$	839 µF	442 µF
PWM frequency	f_{PWM}	1 kHz	1 kHz

input for simulations to determine the chip area scaling a (identical for the upper and lower switches) and the required size of input capacitor $C_{\mathrm{i}}^{\mathrm{sim}}$. The simulation results are summarized in Table 8.13.

Table 8.13: Resulting chip area scaling factor a for IGBTs and resulting input capacitance (calculated from simulation data) $C_{\mathrm{i}}^{\mathrm{sim}}$ for **two-level VSI** designed for all study cases.

	Study Cases							
	A-I	A-II	B-I	B-II	C-I	C-II	D-I	D-II
a (-)	2.55	1.65	3.89	3.60	2.55	1.65	3.89	3.60
$C_{\mathrm{i}}^{\mathrm{sim}}$ (µF)	514	514	516	516	257	257	258	258

Table 8.13 reveals that the input capacitance obtained from simulation $C_{\mathrm{i}}^{\mathrm{sim}}$ is lower than the analytically calculated value listed in Table 8.12, similar to quasi-two-level PWM operation of MMCs. Additionally, it can be seen that the chip area is independent of the machine voltage, as long as the converter currents are identical, and that the constant load torque characteristic (characteristic I) requires higher chip area scaling factors than the quadratic characteristic (characteristic II).

Table 8.14: Design indicators for the **two-level VSI** with series-connected IGBTs, designed for study cases A..D and both characteristics of load torque.

Torque Characteristic I

		Study Cases			
		A-I	B-I	C-I	D-I
Relative switching power	$p_{\mathrm{sw,rel}}$ (-)	22.8	34.7	22.8	34.7
Total energy in pass. components	H_{tot} (ms)	3.12	3.12	3.12	3.12
Output current THD at ω_{N}	THD_i (%)	1.77	0.29	1.77	0.29
Converter efficiency at ω_{N}	η_{N} (%)	99.39	99.43	99.39	99.43
Input capacitor RMS current	$I_{C\mathrm{i}}$ (A)	361	361	361	361
Total chip area (relative to A_{ref})	a_{tot} (-)	76.5	117	153	234
Energy in module capacitors	$H_{C\mathrm{mod,tot}}$ (ms)	0	0	0	0
Energy in inductors	$H_{L,\mathrm{tot}}$ (ms)	0	0	0	0
Energy in dc-link capacitor	$H_{C\mathrm{i}}$ (ms)	3.12	3.12	3.12	3.12

Torque Characteristic II

		Study Cases			
		A-II	B-II	C-II	D-II
Relative switching power	$p_{\mathrm{sw,rel}}$ (-)	14.7	32.2	14.7	32.2
Total energy in pass. components	H_{tot} (ms)	3.12	3.12	3.12	3.12
Output current THD at ω_{N}	THD_i (%)	1.77	0.29	1.77	0.29
Converter efficiency at ω_{N}	η_{N} (%)	99.32	99.42	99.32	99.42
Input capacitor RMS current	$I_{C\mathrm{i}}$ (A)	272	271	272	271
Total chip area (relative to A_{ref})	a_{tot} (-)	49.6	108	99.1	216
Energy in module capacitors	$H_{C\mathrm{mod,tot}}$ (ms)	0	0	0	0
Energy in inductors	$H_{L,\mathrm{tot}}$ (ms)	0	0	0	0
Energy in dc-link capacitor	$H_{C\mathrm{i}}$ (ms)	3.12	3.12	3.12	3.12

The design indicators are listed in Table 8.14. Comparing study cases A-I, A-II, B-I, and B-II with study cases C-I, C-II, D-I, and D-II, respectively, it can be stated that all relative design indicators, i.e. switching power, total energy stored in passive components, output current THD, and converter efficiency at rated speed are identical. Hence, the voltage level does not influence these design parameters. While the energy storage constant, composed solely of energy stored in the input capacitor, is constant in all study cases, the switching power is lower for cases with quadratic load torque characteristic (characteristic I) and for the machines with higher speeds (study cases A and C).

Comparisons to Quasi-Two-Level PWM Operation

In Figure 8.12, the comparison between the design indicators of two-level VSIs with series-connected IGBT switches and quasi-two-level PWM operation of MMCs is drawn graphically for all study cases. The comparison between the relative losses dependent on the machine speed is plotted in Figure 8.13.

The trends in the relative switching power, relative losses at rated speed, output-current THD, and the input-capacitor-current RMS values of quasi-two-level PWM operation of MMCs are

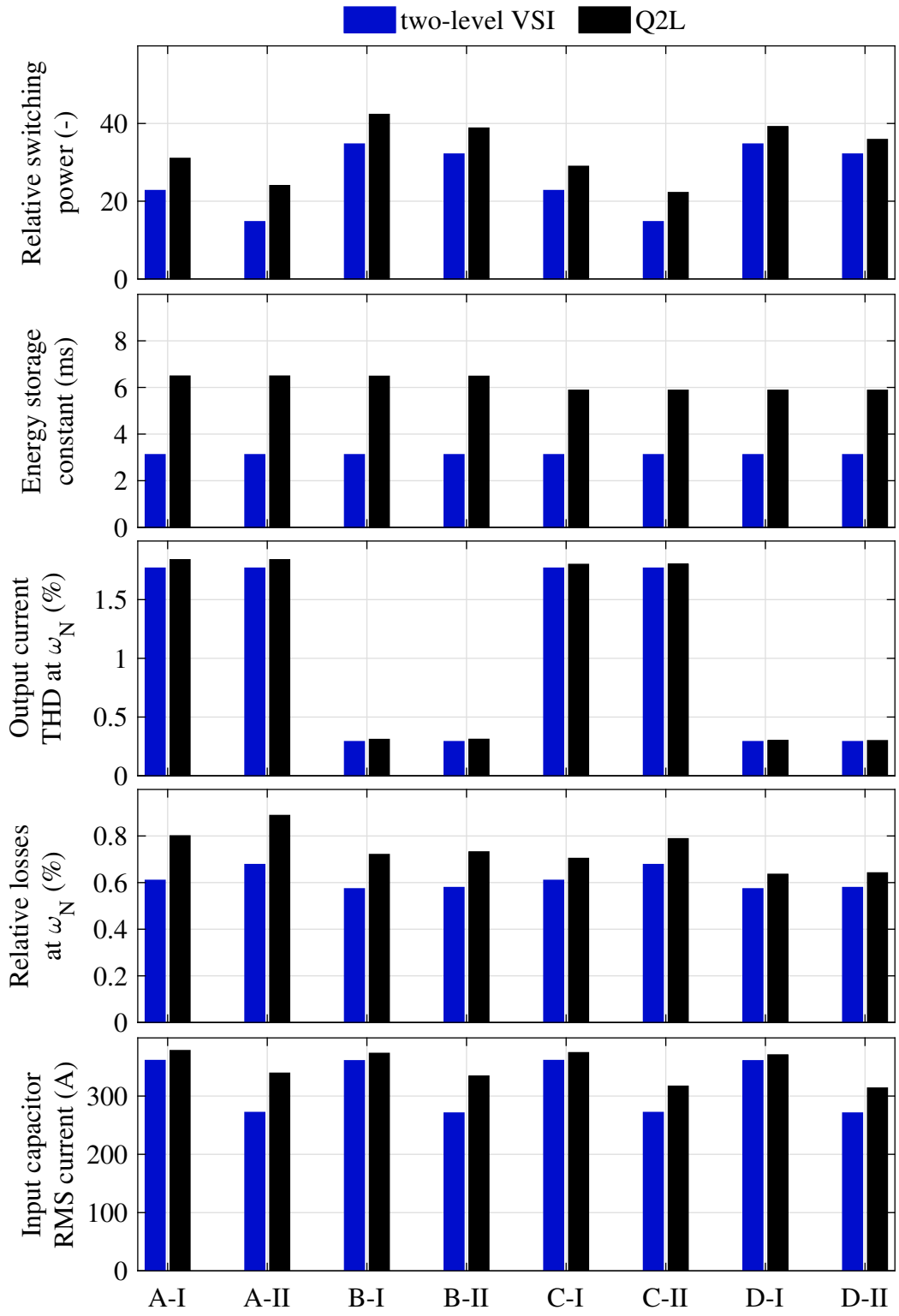


Figure 8.12: Comparison of design indicators of two-level VSI with series-connected IGBTs (denoted as "two-level VSI" and plotted in blue) and quasi-two-level PWM operation (denoted as "Q2L" and plotted in black) for all study cases.

similar to those of the two-level VSIs. However, all design indicators are higher for all study cases with quasi-two-level PWM operation.

Nevertheless, as mentioned at the beginning of this chapter, these data should be interpreted

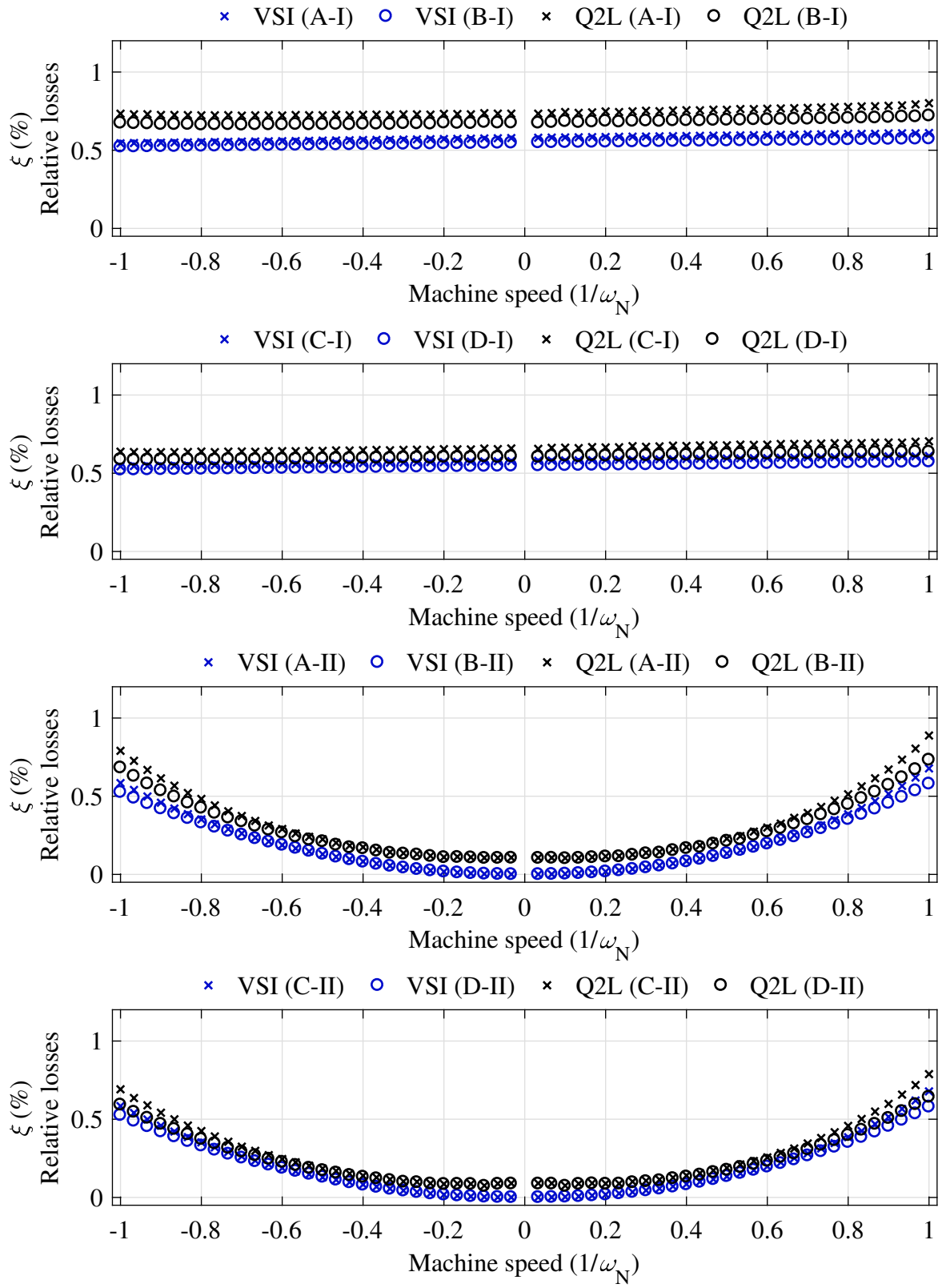


Figure 8.13: Comparison between the relative converter losses ξ of the VSIs (denoted as "VSI" and plotted in blue) and of the quasi-two-level PWM-operated MMCs (denoted as "Q2L" and plotted in black) for all study cases.

as a comparison of the quasi-two-level PWM operation to its idealized form rather than as a realistic comparison to two-level VSI. In practical implementation of two-level VSI, different IGBT modules would be utilized, making the comparison between topologies more challenging. Most likely, a $\mathrm{d}v/\mathrm{d}t$ filter would be required for two-level VSI, causing additional losses and increasing the energy stored in passive components. Moreover, the output current THD is expected to increase due to the dead-time effects, which are caused by the relatively long dead-times of HV-IGBTs.

8.7 Comparison to MMMC

This section presents the design of MMMCs. In contrast to conventional operation of MMC, MMMCs are well-suited for operation frequencies below the grid frequency [27] even for start-up torques higher than the rated torque [28]. Hence, all study cases are investigated. Since the MMMC is an ac-ac converter, a direct comparison to an MMC is rather unfair. Therefore, an MMC active front-end (AFE) is designed for the quasi-two-level PWM-operated MMCs and the comparison to MMMCs is accomplished on the ac-ac system basis.

The machine model and machine control are identical to those used in previous investigations. The grid is modeled using sinusoidal ideal voltage sources. Since H-bridge modules are used, the switching state $s \in \{-1, 0, 1\}$. While the simulation model of the converter branch can remain unchanged, the chip-area scaling model has to be updated. This is done by splitting each H-bridge module into two half-bridge modules. The exact implementation is explained below.

The MMMC control is implemented based on the generalized control approach for a class of modular multilevel converters according to [91, 92]. Thus, the control scheme is similar to that applied for the conventionally operated MMC. To stabilize the operation at speeds near zero, the instantaneous power mode (IPM) according to [151] is applied. A two-step modulation approach similar to that of MMC is utilized.

Similar to the LFM of MMC, there are two independent non-zero frequencies in the system. Hence, the investigated simulation time is selected to be a multiple of the machine electrical period in a way that at least 20 grid periods are simulated. Due to long amounts of time required for the simulation runs, no variation of initial angle between the grid and the machine is applied.

Incorporation of H-bridge Modules in the Chip Area Scaling Model

As mentioned above, the H-bridge modules are incorporated into the existing chip area scaling model as two half-bridge modules. Consequently, the nine H-bridge module branches are handled as 18 half-bridge module branches by the chip-area scaling model. The rest of the model does not have to be changed.

The switching states for the left half-bridge and right half-bridge are determined according to the switching state of the H-bridge module as described by Table 8.15. The table is in concordance with the H-bridge module and half-bridge module definitions from Section 2.1.

Table 8.15: Calculation of switching states for the half-bridges using the H-bridge switching state.

H-bridge switching state	s	1	0	0	-1
Switching state of left half-bridge	s_l	1	1	0	0
Switching state of right half-bridge	s_r	0	1	0	1

As can be seen in Table 8.15, there are two options for achieving the zero switching state of H-bridge modules. In this implementation, these two are alternated in each module every time a switching transition to zero state is required.

The "virtual" branch current for the left half-bridge modules

$$i_{\mathrm{b,l}} = i_\mathrm{b} \tag{8.67}$$

is identical to the branch current of the H-bridge module. The "virtual" branch current for the right half-bridge modules

$$i_{\mathrm{b,r}} = -i_\mathrm{b} \tag{8.68}$$

is inverted.

MMMC Design Process

In the first step of the MMMC design process, the **grid voltage** is assigned. Its line-to-line RMS value

$$V_\mathrm{g} = V_\mathrm{sN} \tag{8.69}$$

is selected to be equal to the value of the rated stator voltage. The **grid frequency** is selected to be $f_\mathrm{g} = 50$ Hz, which is a common grid frequency in many countries.

The **number of modules per branch**

$$n_\mathrm{mpb} \leq \frac{\hat{v}_\mathrm{b}}{V_{C,\mathrm{min}}} \tag{8.70}$$

is determined by the required peak branch voltage $\hat{v}_\mathrm{b}$ and the minimum capacitor voltage value $V_{C,\mathrm{min}}$, which is selected identically to that of conventionally operated MMCs: $V_{C,\mathrm{min}} = 830$ V. The required peak branch voltage

$$\hat{v}_\mathrm{b} = \frac{1}{1-k_\mathrm{cr}} \cdot \frac{\sqrt{3}}{2} \cdot \left(\sqrt{\frac{2}{3}} \cdot V_\mathrm{g} + \sqrt{\frac{2}{3}} \cdot V_\mathrm{sN} \right) \tag{8.71}$$

can be calculated as a sum of peak grid voltage and peak stator voltage. The factor $\frac{\sqrt{3}}{2}$ in (8.71) accounts for the SVM applied to both converter sides. The control reserve factor k_cr is 2 %, the same value as in previous investigations. This leads to

$$n_\mathrm{mpb}^\mathrm{A,B} = 6 \tag{8.72}$$

for study cases A and B, and

$$n_{\mathrm{mpb}}^{\mathrm{C,D}} = 12 \tag{8.73}$$

for study cases C and D.

Although there are options to couple the branch inductors in order to reduce their volume and costs [152, 153], simple non-coupled branch inductors are implemented, since the inductors in general are not expected to significantly impact the total energy storage constant of the converter. The **branch inductance**

$$L_{\mathrm{b}} = \frac{1}{4} \cdot \frac{V_C}{f_{\mathrm{m}} \cdot \Delta i_{\mathrm{b,r,max}}} = 0.68 \text{ mH} \tag{8.74}$$

is calculated similarly to the branch inductance of MMC and its value is half of the conventionally operated MMC's leg inductance. The control and **modulation frequency** $f_{\mathrm{m}} = 5$ kHz and the maximum allowed branch current ripple $\Delta i_{\mathrm{b,r,max}} = 0.08 \cdot \sqrt{2} \cdot I_{\mathrm{sN}}$ are selected identically to conventionally operated MMC.

The **branch resistance** is zero, as in previous investigations, and the module capacitance is sought iteratively, as was done for conventionally operated MMCs.

The IPM for MMMCs [151] is similar to the IPM for MMCs. It is based on splitting the grid currents between the branches in a way that the branch power components at double stator frequency are compensated. Unlike for MMC, a stable operation at zero speeds is possible with IPM for MMMCs without any additional measures. Nevertheless, the IPM becomes unstable when the stator frequency approaches one third of the grid frequency [154][3)]. Consequently, the IPM is deactivated when the stator frequency f_{s} approaches 20 percent of the grid frequency f_{g}. As Figure 8.14 shows, the IPM is not deactivated instantaneously, but its circulating current setpoints are decreased linearly up to 25 percent of the grid frequency. Above this frequency, the normal operation mode is used, which sets the additional circulating current setpoints to zero, similar to the normal operation mode for MMCs.

Figure 8.14 also shows that the SVM is deactivated when the stator frequency approaches one third of the grid frequency. This is necessary because constant power components in branch powers would otherwise be generated by the third-harmonic component injected into the branch voltages by SVM and the branch current components at the grid frequency, leading to unstable converter operation.

MMMC Design Results

The parameters of MMMCs designed for each particular study case are listed in Table 8.16. The parameters are identical for study cases A-I, A-II, B-I, and B-II and for study cases C-I, C-II, D-I, and D-II, except for the module capacitance value, which depends on both the rated stator frequency and the torque characteristic.

[3)] This problem was solved with an approach by Kawamura *et al.* proposed in [154] as "Control III". Since the impact on the final design is not expected to be significant and the approach is not defined for non-sinusoidal waveforms, it is not considered in this thesis.

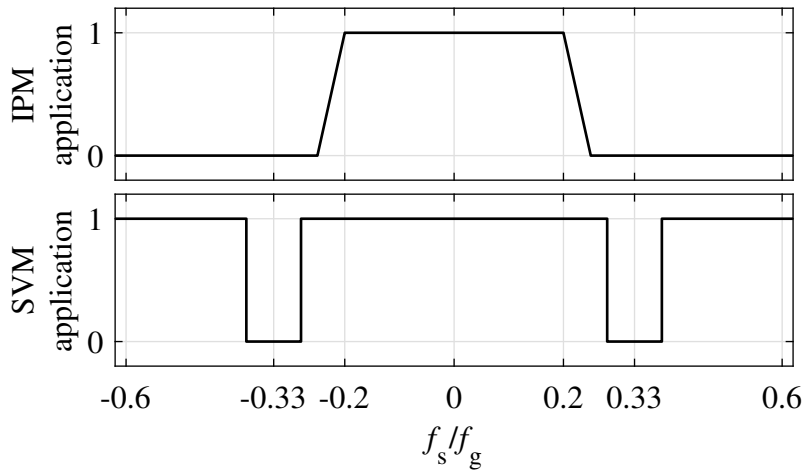


Figure 8.14: Application of IPM and SVM dependent on the ratio of actual stator frequency f_s and the grid frequency f_g. The resulting factor for IPM is multiplied by the circulating currents required by IPM. If the factor for SVM is one, SVM is activated. It is deactivated otherwise.

Table 8.16: Simulation parameters of **MMMC**, designed for study cases A, B, C, and D. Aside from the module capacitance, the parameters are identical for both load torque characteristics.

		Study Cases			
Parameter		A	B	C	D
Grid voltage	V_{gN}	3.3 kV	3.3 kV	6.6 kV	6.6 kV
Grid frequency	f_g	50 Hz	50 Hz	50 Hz	50 Hz
Modules per branch	n_{mpb}	6	6	12	12
Branch inductance (uncoupled)	L_b	0.68 mH	0.68 mH	0.68 mH	0.68 mH
Branch resistance	R_b	0	0	0	0
Module capacitance (char. I)	C_{mod}	7.6 mF	9.6 mF	7.6 mF	9.6 mF
Module capacitance (char. II)	C_{mod}	5.2 mF	9.6 mF	5.2 mF	9.6 mF
Modulation frequency	f_m	5 kHz	5 kHz	5 kHz	5 kHz
Setpoint module capacitor voltage	V_C^*	915 V	915 V	915 V	915 V

As in previous investigations, these parameters are used in simulations to determine the scaling factor of the H-bridge modules' semiconductor switches and the design indicators. The scaling factors are listed for the particular study cases in Table 8.17, the design indicators are summarized in Table 8.18.

Table 8.17: Resulting chip area scaling factor a for IGBT modules of **MMMC** designed for all study cases.

	Study Cases							
	A-I	A-II	B-I	B-II	C-I	C-II	D-I	D-II
a (-)	1.22	0.92	2.12	1.85	1.24	0.93	2.17	1.89

Observing the design indicators for MMMCs in Table 8.18, several observations can be made: First, the constant torque characteristic (characteristic I) requires slightly higher switching powers than the quadratic torque characteristic (characteristic II). The energy storage constant is higher for the constant torque characteristic for the machines with higher rated speeds (study

Table 8.18: Design indicators for **MMMCs**, designed for study cases A..D and both characteristics of load torque.

Torque Characteristic I

		Study Cases			
		A-I	B-I	C-I	D-I
Relative switching power	$p_{\mathrm{sw,rel}}$ (-)	78.2	136	79.4	139
Total energy in pass. components	H_{tot} (ms)	60.1	76.2	60.0	75.9
Mod. capacitor RMS current	$I_{C,\mathrm{mod}}$ (A)	123	116	124	117
Stator current THD at ω_{N}	THD_i (%)	0.06	0.01	0.06	0.01
Converter efficiency at ω_{N}	η_{N} (%)	97.63	97.57	97.59	97.54
Total chip area (relative to A_{ref})	a_{tot} (-)	263	458	534	936
Energy in module capacitors	$H_{C\mathrm{mod,tot}}$ (ms)	59.8	75.6	59.8	75.6
Energy in inductors	$H_{L,\mathrm{tot}}$ (ms)	0.26	0.60	0.14	0.30

Torque Characteristic II

		Study Cases			
		A-II	B-II	C-II	D-II
Relative switching power	$p_{\mathrm{sw,rel}}$ (-)	59.0	119	59.9	122
Total energy in pass. components	H_{tot} (ms)	41.2	76.2	41.1	75.9
Mod. capacitor RMS current	$I_{C,\mathrm{mod}}$ (A)	111	99.5	112	104
Stator current THD at ω_{N}	THD_i (%)	0.08	0.01	0.07	0.01
Converter efficiency at ω_{N}	η_{N} (%)	97.58	97.56	97.54	97.54
Total chip area (relative to A_{ref})	a_{tot} (-)	198	400	402	818
Energy in module capacitors	$H_{C\mathrm{mod,tot}}$ (ms)	40.9	75.6	40.9	75.6
Energy in inductors	$H_{L,\mathrm{tot}}$ (ms)	0.26	0.60	0.14	0.30

cases A and C). For the machines with lower rated speeds (study cases B and D), the energy storage constant is independent of the torque characteristic. Second, the design indicators are almost independent of the output voltage level, as visible when comparing study case A with study case C, and study case B with study case D. Third, study cases B and D, which have with a lower rated machine speed, require higher switching power than the study cases A and C, which have a higher machine speed. A similar observation can be made for the energy storage constant. Fourth, the converter efficiency is almost identical in all study cases.

The designed MMMCs are also validated in dynamic conditions for machine acceleration in Appendix F.

Design of an MMC AFE for Quasi-Two-Level PWM-Operated MMC

The AFE is designed based on similar principles to those of conventionally operated MMC. The main difference is that the input voltage value is defined by the quasi-two-level PWM-operated MMCs, and the grid voltage is a degree of freedom. Since the grid has a constant frequency $f_{\mathrm{g}} = 50$ Hz, only the normal operation mode is applied. The converter parameters are summarized in Table 8.19 including the chip area scaling factors. The resulting design indicators are listed in Table 8.20. Since the operating point with the rated power is crucial for the design, the results are identical for both load torque characteristics.

Table 8.19: Resulting parameters of MMC **AFE** designed for quasi-two-level PWM-operated MMC. The parameters are identical for both load torque characteristics.

		Study Cases	
Parameter		A and B	C and D
Grid voltage	V_{gN}	3.5 kV	6.5 kV
Grid frequency	f_{g}	50 Hz	50 Hz
Input voltage	V_{i}	5.35 kV	10.2 kV
Modules per branch	n_{mpb}	7	13
Leg inductance (coupled)	L_{leg}	1.36 mH	1.36 mH
Branch resistance	R_{b}	0	0
Module capacitance	C_{mod}	3.2 mF	3.9 mF
DC-link capacitance	C_{i}	0	0
Modulation frequency	f_{m}	5 kHz	5 kHz
Setpoint module capacitor voltage	V_C^*	915 V	915 V
Chip area scaling factors	a_1	0.48	0.50
	a_2	1.10	1.08

Table 8.20: Design indicators for MMC **AFE** designed for quasi-two-level PWM-operated MMC. The indicators are identical for both load torque characteristics.

		Study Cases	
		A and B	C and D
Relative switching power	$p_{\mathrm{sw,rel}}$ (-)	19.7	18.3
Total energy in pass. components	H_{tot} (ms)	19.6	22.2
Mod. capacitor RMS current	$I_{C,\mathrm{mod}}$ (A)	111	129
Converter efficiency at ω_{N}	η_{N} (%)	99.24	99.29
Total chip area (relative to A_{ref})	a_{tot} (-)	66.2	123
Energy in module capacitors	$H_{C\mathrm{mod,tot}}$ (ms)	19.6	22.2
Energy in inductors	$H_{L,\mathrm{tot}}$ (ms)	0.03	0.02
Energy in dc-link capacitor	$H_{C\mathrm{i}}$ (ms)	0	0

Comparisons to Quasi-Two-Level PWM Operation of MMC

In Figure 8.15, a comparison between the design indicators of the MMMCs and those of quasi-two-level PWM-operated MMCs with a corrsponding AFE is shown. The design indicators of AFE are stacked on top of those for quasi-two-level PWM-operated MMCs to provide a comparison based on ac-ac systems.

Except for the output current distortion, the quasi-two-level PWM-operated MMCs with AFEs are advantageous for all indicators. The reason for the relatively high switching power of MMMCs is that all semiconductor switches must be designed to withstand the low-frequency junction temperature variation. In contrast, the MMCs' IGBTs can be designed optimally for each converter side. The higher losses of MMMCs are directly linked to the installed switching power. The dependency of the losses on the machine speed is plotted for all study cases and torque characteristics in Figure 8.16.

Note that the comparison might turn out differently if the upper and lower IGBTs in half bridge

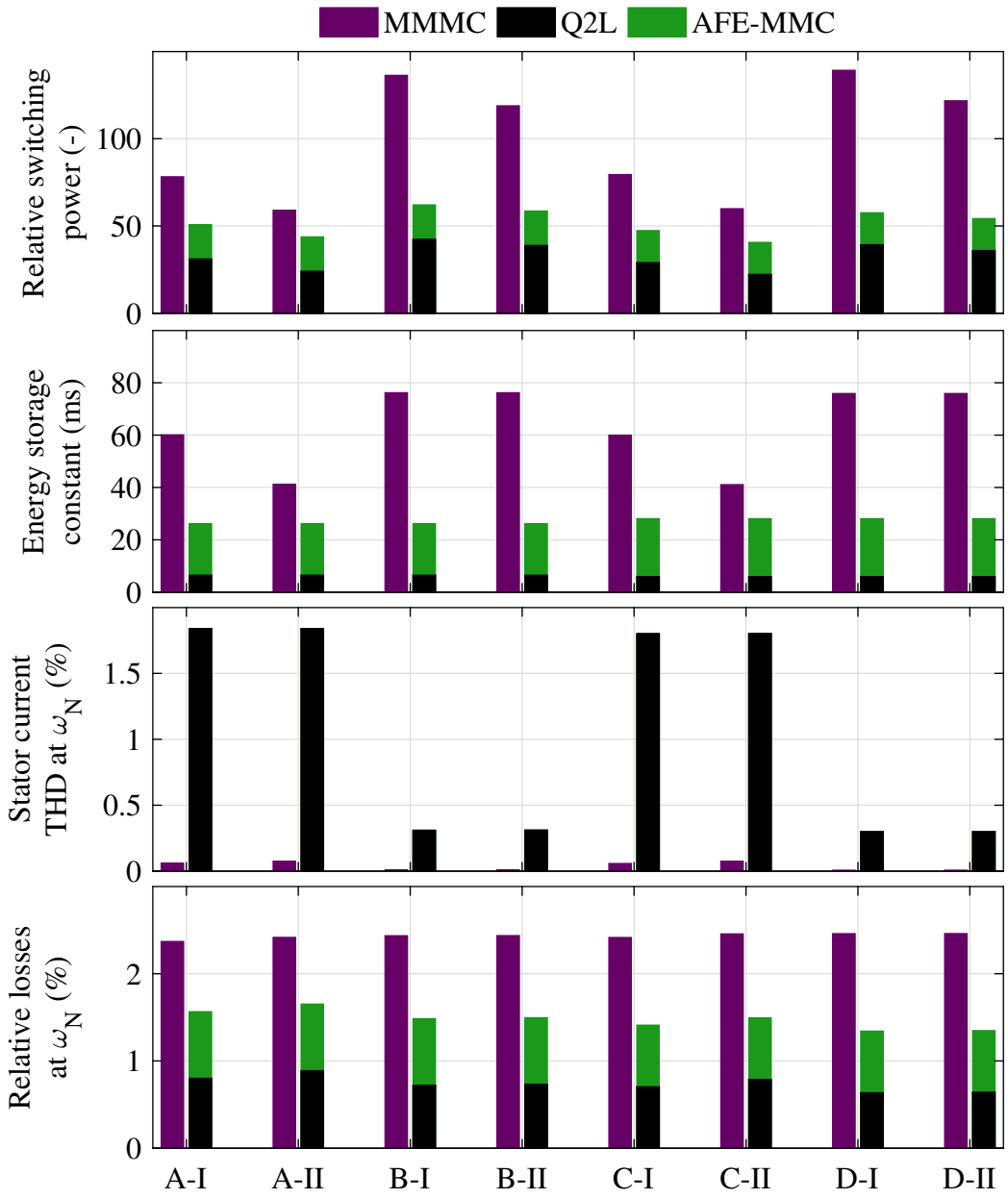


Figure 8.15: Comparison of design indicators of MMMCs (denoted as "MMMC" and plotted in violet) and quasi-two-level PWM operation of MMCs (denoted as "Q2L" and plotted in black) with MMC AFEs (denoted as "AFE" and plotted in green) for all study cases.

modules had to be identical or if the ac-ac systems were designed to have a fault ride-through capability, which is required by grid codes in many countries.

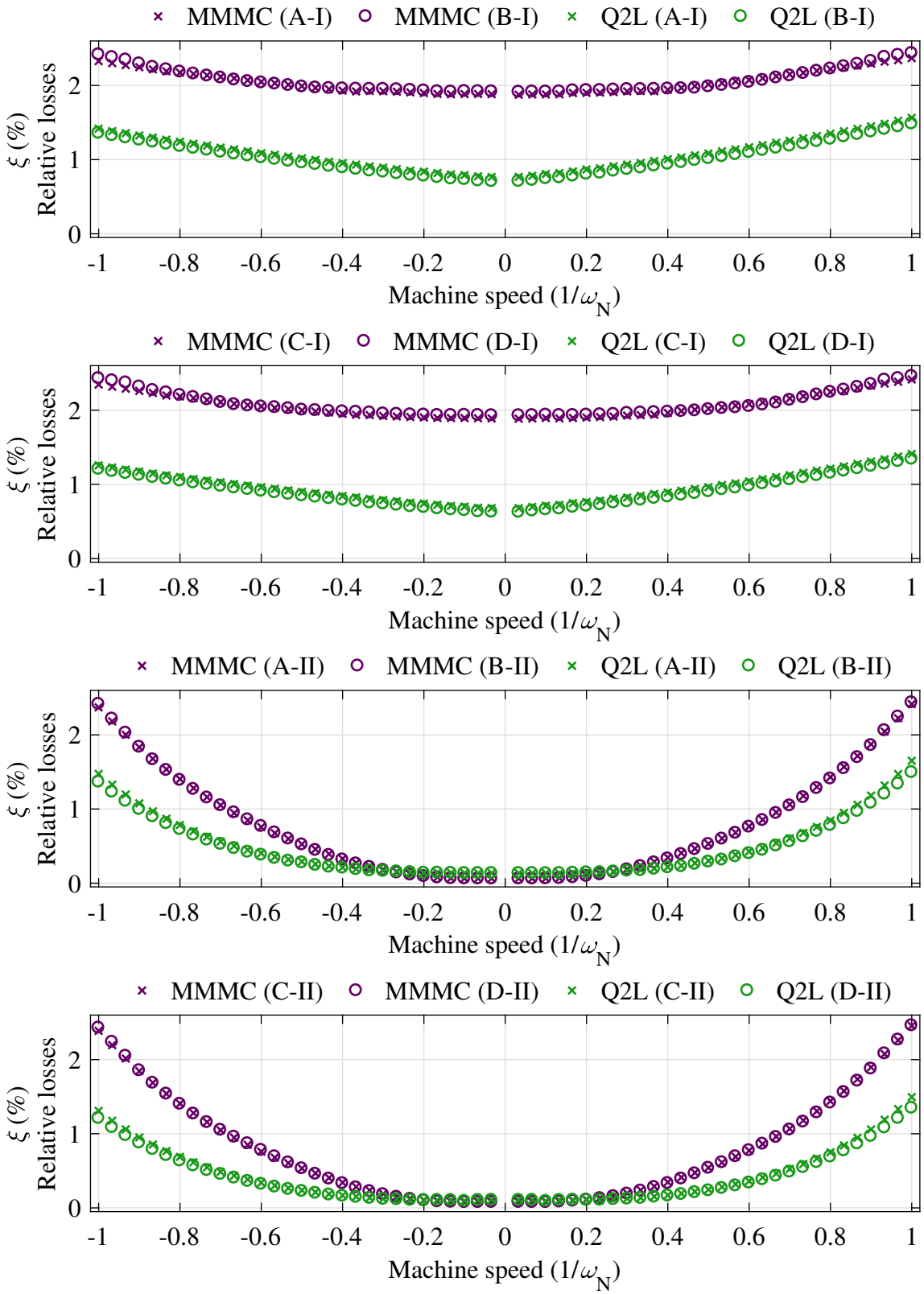


Figure 8.16: Comparison between the relative converter losses ξ of MMMC (denoted as "MMMC" and plotted in violet) and quasi-two-level PWM-operated MMC including the AFE (denoted as "Q2L" and plotted in green) for all study cases.

9 Conclusions and Outlook

This thesis has presented a novel operation mode for modular multilevel converters called *quasi-two-level PWM operation*. The main goal of the derivation was to find an operation mode with significantly reduced module capacitance even with low output frequencies, which are challenging for conventional converter operation. The key properties of quasi-two-level PWM-operated MMCs can be summarized as follows:

- The module capacitance can be chosen regardless of the rated output frequency and is significantly lower than the required capacitances for conventional operation modes of modular multilevel converters.
- The distortions of input and output currents are similar to those of classical two-level VSIs. Consequently, a capacitive input filter is required. An output filter can be omitted when the load (e.g. low-speed medium-voltage machine) provides sufficient inductance.
- The height of voltage steps of the applied quasi-two-level waveform is low. Hence, overvoltages with long machine cables are diminished. In addition, bearing currents or potential EMI problems are also expected to be reduced.
- Other advantages of modular construction, i.e. linear scalability of the converter's voltages and a straight-forward way to add redundancy, are inherited from the modular multilevel conveter topology.

Besides the theoretical background of MMCs and the derivation of the quasi-two-level PWM operation, the thesis studied converter control methods suitable for the operation mode, the trade-offs regarding the converter design, and other properties specific to this operation mode. The design of the quasi-two-level PWM-operated modular multilevel converter was conducted for several study cases in medium-voltage drives and the design indicators were compared to those of other potentially advantageous medium-voltage converter topologies designed for this application.

Both simulations and implementation on the downscaled converter prototype proved the concept of the operation mode and the proposed control schemes to be valid. The parameter sensitivity study conducted for the control algorithms shows that the proposed control algorithms are not critically sensitive to any of the parameters, as long as these are within a reasonable range. Comparing both options for the branch-energy control, the predictive branch-energy control has generally shown better performance, i.e. the compensating currents and the module capacitor voltage variation were lower. When the output current ripple is very high compared to the rated current which the converter was designed for, the fast proportional branch-energy control leads to better results. In conclusion, the predictive branch-energy control is the recommended solution. In future research, an option to combine these control methods should be investigated.

Several trade-offs were identified within the design. These are the maximum achievable duty cycle, the HF modulation frequency, the installed leg inductance, and the maximum allowed

compensating current. The derivation shows that the maximum achievable duty cycle is limited to a value below one, depending on the other design parameters. One of the conclusions resulting from these investigations is that quasi-two-level PWM operation is especially well-suited for modular multilevel converters with a relatively high number of modules per branch. As a rule of thumb, the number of modules per branch should be at least five.

The derived design relationships were further used to design the quasi-two-level PWM operated MMCs for several study cases in medium-voltage low-speed synchronous-machine drives. By comparing the resulting design indicators to those of the conventional operation mode of MMC and those of MMMC, the following conclusions can be drawn:

- As mentioned above, the output current distortion of quasi-two-level PWM-operated MMCs is similar to that of two-level VSI. Hence, the distortion of conventionally operated MMC's and MMMC's output currents is significantly lower. Nevertheless, the output current distortion did not appear to be crucial in the investigations.
- The quasi-two-level PWM-operated MMCs are seen to be clearly advantageous over the conventional operation modes of MMCs for the study cases with very low rated output frequencies. When the frequencies are higher, the quasi-two-level PWM-operated MMC is still clearly advantageous as long as the applications require high torques from zero speed. If the torque required at low speeds is low, the preferred operation mode should be decided on specifically for the application. The quasi-two-level PWM operation leads to a significantly lower installed capacitance and the conventional operation modes require slightly less semiconductor chip area and the converter losses are lower.
- Compared to MMMC, the quasi-two-level PWM operation of MMCs shows superior results for all investigated design scenarios.

In conclusion, this thesis has explored the quasi-two-level PWM operation mode for MMCs and has identified its properties. The operation mode proved advantageous in low-speed medium-voltage machine drives as well as in constant-torque drive applications.

Nonetheless, many scientific questions are yet to be answered and several improvements can be made. These mainly include the converter control and potential hardware improvements.

One of the unknown parameters required for the converter control is the branch resistance. In the future, an online estimation of these time-variant non-linear resistances should be implemented to improve the behavior of the leg current control. Furthermore, compensation for the small output voltage errors could be implemented. To reduce the remaining control deviations, the branch-energy control could be improved by the application of a proportional-integral controller.

This thesis has shown that more than half of the total energy stored in the converter's capacitors is stored in the central dc-link capacitor. Consequently, an operation mode reducing the input current variation should be explored to reduce the dc-link capacitance. It is expected that there should be a trade-off between the volume of the central dc-link capacitor and the volume of capacitors in the modules.

Although this thesis has shown clear expectations for the behavior of the full-size converter, the validation could only be accomplished for the downscaled converter. In the future, a full-size converter with a medium-voltage machine should be investigated to validate the converter behavior. Furthermore, the behavior of the full-size machine with an emphasis on overvoltages due to long in-feed cables and the bearing currents should be investigated.

A potential application of wide-band-gap semiconductor transistors in the modules should be explored. The high switching frequencies enabled by the use of these semiconductor devices could be utilized to increase the PWM frequency and HF-modulation frequency and to reduce the volume of passive components. A potential second option for design improvement could be achieved through the application of non-linear saturable inductors in the branches to minimize the energy which has to be stored in the system. Nevertheless, the aforementioned hardware improvements are rather speculative and should be assessed in future research.

Finally, the application of the principles presented in this thesis should also be studied for other MMC topologies, such as MMMC.

A Cross-Coupling in State-Space Description Using Leg Currents

As mentioned in Chapter 2, there is a cross-coupling in the state-space description, when the three leg currents are included in the state vector instead of the input current and two circulating currents. The cross-coupling is visible at system matrix $\mathbf{A}$. If the inner resistance R_i and the inductance L_i of the input system are both zero, the matrix $\mathbf{A}$ becomes diagonal and the cross-coupling disappears.

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{leg1}} \\ i_{\mathrm{leg2}} \\ i_{\mathrm{leg3}} \\ i_{\mathrm{o}\alpha} \\ i_{\mathrm{o}\beta} \end{bmatrix} = \mathbf{A}\cdot\begin{bmatrix} i_{\mathrm{leg1}} \\ i_{\mathrm{leg2}} \\ i_{\mathrm{leg3}} \\ i_{\mathrm{o}\alpha} \\ i_{\mathrm{o}\beta} \end{bmatrix} + \mathbf{B}\cdot\begin{bmatrix} v_{\mathrm{b1}} \\ v_{\mathrm{b2}} \\ v_{\mathrm{b3}} \\ v_{\mathrm{b4}} \\ v_{\mathrm{b5}} \\ v_{\mathrm{b6}} \end{bmatrix} + \mathbf{E}\cdot\begin{bmatrix} v'_{\mathrm{i}} \\ v'_{\mathrm{o}\alpha} \\ v'_{\mathrm{o}\beta} \\ v'_{\mathrm{o}0} \end{bmatrix}$$

$$\mathbf{A} = \begin{bmatrix} -\frac{2R_\mathrm{b}\cdot L_\mathrm{i}+(2R_\mathrm{b}+R_\mathrm{i})\cdot L_\mathrm{b}}{L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & \frac{R_\mathrm{b}\cdot L_\mathrm{i}-R_\mathrm{i}\cdot L_\mathrm{b}}{L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & \frac{R_\mathrm{b}\cdot L_\mathrm{i}-R_\mathrm{i}\cdot L_\mathrm{b}}{L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & 0 & 0 \\ \frac{R_\mathrm{b}\cdot L_\mathrm{i}-R_\mathrm{i}\cdot L_\mathrm{b}}{L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & -\frac{2R_\mathrm{b}\cdot L_\mathrm{i}+(2R_\mathrm{b}+R_\mathrm{i})\cdot L_\mathrm{b}}{L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & \frac{R_\mathrm{b}\cdot L_\mathrm{i}-R_\mathrm{i}\cdot L_\mathrm{b}}{L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & 0 & 0 \\ \frac{R_\mathrm{b}\cdot L_\mathrm{i}-R_\mathrm{i}\cdot L_\mathrm{b}}{L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & \frac{R_\mathrm{b}\cdot L_\mathrm{i}-R_\mathrm{i}\cdot L_\mathrm{b}}{L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & -\frac{2R_\mathrm{b}\cdot L_\mathrm{i}+(2R_\mathrm{b}+R_\mathrm{i})\cdot L_\mathrm{b}}{L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_\mathrm{b}+2R_\mathrm{o}}{L_\mathrm{b}+2L_\mathrm{o}} & 0 \\ 0 & 0 & 0 & 0 & -\frac{R_\mathrm{b}+2R_\mathrm{o}}{L_\mathrm{b}+2L_\mathrm{o}} \end{bmatrix}$$

$$\mathbf{B} = \begin{bmatrix} -\frac{2L_\mathrm{b}+2L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & -\frac{2L_\mathrm{b}+2L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & \frac{L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & \frac{L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & \frac{L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & \frac{L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} \\ \frac{L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & \frac{L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & -\frac{2L_\mathrm{b}+2L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & -\frac{2L_\mathrm{b}+2L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & \frac{L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & \frac{L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} \\ \frac{L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & \frac{L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & \frac{L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & \frac{L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & -\frac{2L_\mathrm{b}+2L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} & -\frac{2L_\mathrm{b}+2L_\mathrm{i}}{2L_\mathrm{b}\cdot(2L_\mathrm{b}+3L_\mathrm{i})} \\ -\frac{2}{3L_\mathrm{b}+6L_\mathrm{o}} & \frac{2}{3L_\mathrm{b}+6L_\mathrm{o}} & \frac{1}{3L_\mathrm{b}+6L_\mathrm{o}} & -\frac{1}{3L_\mathrm{b}+6L_\mathrm{o}} & \frac{1}{3L_\mathrm{b}+6L_\mathrm{o}} & -\frac{1}{3L_\mathrm{b}+6L_\mathrm{o}} \\ 0 & 0 & -\frac{\sqrt{3}}{3L_\mathrm{b}+6L_\mathrm{o}} & \frac{\sqrt{3}}{3L_\mathrm{b}+6L_\mathrm{o}} & \frac{\sqrt{3}}{3L_\mathrm{b}+6L_\mathrm{o}} & -\frac{\sqrt{3}}{3L_\mathrm{b}+6L_\mathrm{o}} \end{bmatrix}$$

$$\mathbf{E} = \begin{bmatrix} \frac{1}{2L_\mathrm{b}+3L_\mathrm{i}} & 0 & 0 & 0 \\ \frac{1}{2L_\mathrm{b}+3L_\mathrm{i}} & 0 & 0 & 0 \\ \frac{1}{2L_\mathrm{b}+3L_\mathrm{i}} & 0 & 0 & 0 \\ 0 & -\frac{2}{L_\mathrm{b}+2L_\mathrm{o}} & 0 & 0 \\ 0 & 0 & -\frac{2}{L_\mathrm{b}+2L_\mathrm{o}} & 0 \end{bmatrix}$$

B Validations of Derived Analytic Equations

In Chapter 4, design trade-offs for quasi-two-level PWM-operated MMCs are derived. In this appendix, a simulation of MMC according to Chapter 6 is conducted to validate the equations from Chapter 4.

The converter parameters used for the simulation are listed in Table B.1 and a passive resistive-inductive load is used ($L_\mathrm{o} = 13$ mH and R_o is adjusted for i_o1 to be 500 A). Besides the input voltage V_i, these parameters are in concordance with those from Table 7.1. The input voltage is slightly increased to obtain a voltage ratio λ, defined in Section 7.4, that is closer to one. This is expected to improve the match between the simplified model used for the derivation and the simulation model, since the simplified model assumes that the maximum branch voltage has approximately the value of the input voltage $\hat{v}_\mathrm{b} \approx V_\mathrm{i}$, and thus $\lambda \approx 1$.

Table B.1: Parameters of a medium-voltage quasi-two-level PWM-operated MMC used for validations of analytic equations derived in Chapter 4.

Output current amplitude	$\hat{i}_\mathrm{o}$	500 A
Applied duty cycle	δ_1	0.9
Leg inductance (coupled)	L_leg	210 µH
Branch resistance	R_b	0 Ω
Modules per branch	n_mpb	6
Module capacitance	C_mod	200 µF
DC-link capacitance	C_i	250 µF or ∞
Input voltage	V_i	5.72 kV
Setpoint module capacitor voltage	V_C^*	1000 V
PWM frequency	f_PWM	1 kHz
HF modulation frequency	f_HF	25 kHz
Delay between switch. instants	T_d	1 µs
Energy controller gain	$G_{\mathrm{P},e}$	1200 $\frac{1}{\mathrm{s}}$
HF current amplitude	$\hat{i}_\mathrm{HF}$	0 A

The results of the simulation are plotted in Figure B.1 together with analytically derived values of the compensating currents $I_\mathrm{bA,c}$ and $I_\mathrm{bB,c}$. The figure shows the waveforms for the first phase leg: the output current i_o1, the branch currents i_b1, i_b2 and the branch voltages v_b1, v_b2 for branches 1 and 2, respectively. Furthermore, the branch energies for Branch 1 e_b1 and Branch 2 e_b2, which describe the total energy in the module capacitors of the respective branches, are plotted. Since the branch energies do not account for the voltage (or energy) imbalance between the particular modules within the same branch, vectors $\Delta\mathbf{e}_{C,\mathrm{b1}}$ and $\Delta\mathbf{e}_{C,\mathrm{b2}}$, which represent the

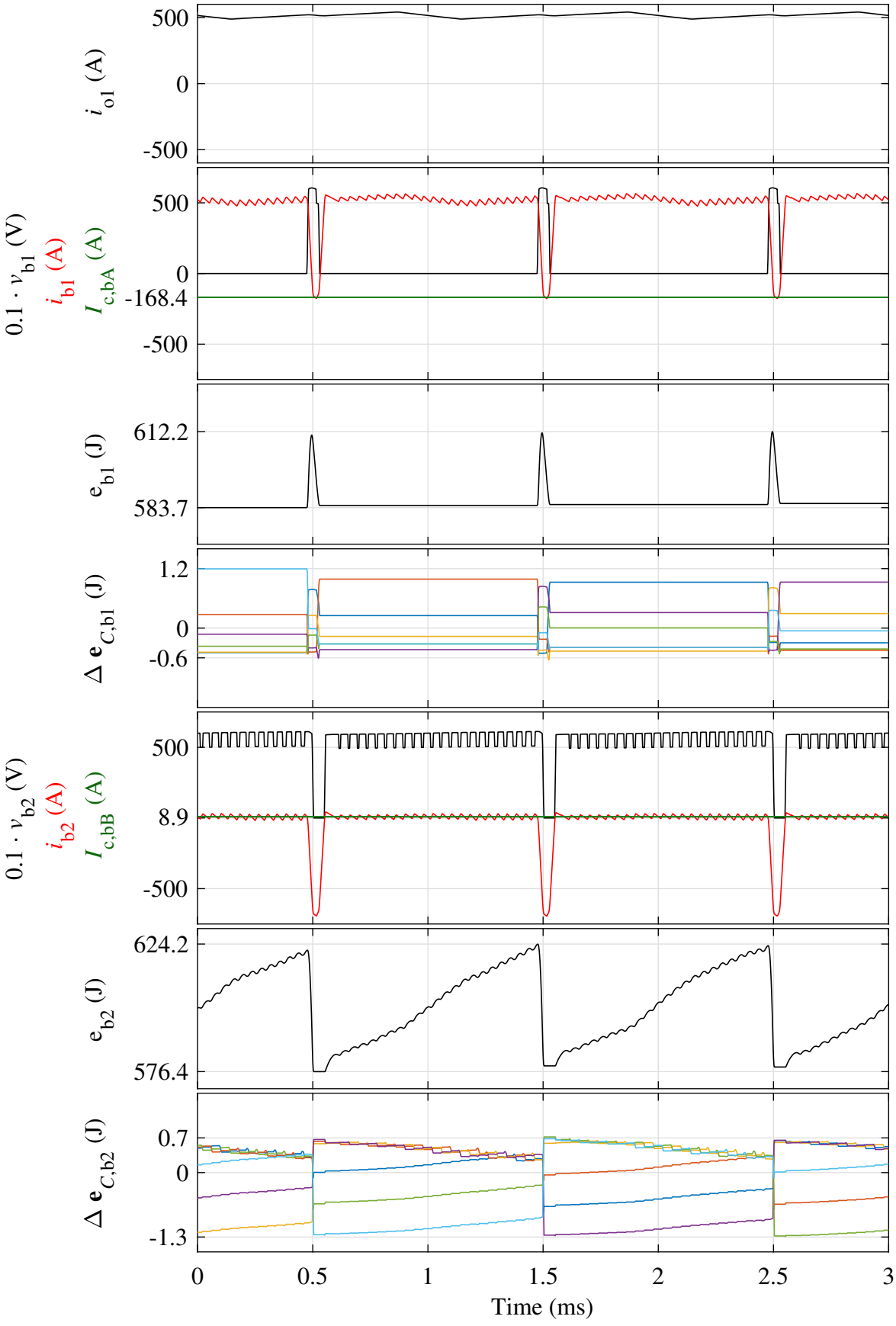


Figure B.1: Simulation results used for a validation of equations derived in Chapter 4. The applied duty cycles are $\delta_1 = 0.9$, $\delta_2 = -0.45$ and $\delta_3 = -0.45$. The predictive branch-energy control is employed.

energy spread between the individual module capacitors of the same branch, are plotted as well. The n-th component of vector $\Delta\mathbf{e}_{C,\mathrm{b1}}$

$$\Delta e_{C,\mathrm{b1},n} = e_{C,\mathrm{b1},n} - \frac{1}{n_{\mathrm{mpb}}} \cdot e_{\mathrm{b1}}, \quad n = 1..n_{\mathrm{mpb}} \tag{B.1}$$

can be calculated as a difference between the energy stored in the n-th module capacitor $e_{C,\mathrm{b1},n}$ and the total energy stored in branch e_{b1} equally divided between the n_{mpb} modules. The calculation for Branch 2 is done correspondingly.

Calculation of Compensating Currents

The compensating currents can be analytically calculated according to (4.13) derived in Section 4.1. Substituting the parameters from Table B.1 into (4.13), the compensating currents can be calculated:

$$\begin{aligned} |I_{\mathrm{bA,c}}| &= 168.4\ \mathrm{A} \quad , \\ |I_{\mathrm{bB,c}}| &= 8.9\ \mathrm{A} \quad . \end{aligned} \tag{B.2}$$

These values are also plotted in Figure B.1 in green. The figure shows that the analytically calculated values of $|I_{\mathrm{bA,c}}|$ and $|I_{\mathrm{bB,c}}|$ match the branch-current waveforms of i_{b1} and i_{b2} obtained from the simulation quite well during `STATE A` and `STATE B`, respectively.

Design of Leg Inductance

The selection of the leg inductance described by (4.14) is determined by solving (4.13) for $|I_{\mathrm{bA,c}}|$. Since this process is not straight-forward, the validity of (4.14) can be confirmed by substituting $I_{\mathrm{b,c,max}} = |I_{\mathrm{bA,c}}| = 168.4$ A according to (B.2), and $\delta_{\mathrm{max}} = \delta_{\mathrm{l}} = 0.9$ and $i_{\mathrm{o,max}} = \hat{i}_{\mathrm{o}} = 500$ A from Table B.1. This leads to a leg inductance value of

$$L_{\mathrm{leg}} = 210\ \mu\mathrm{H} \quad , \tag{B.3}$$

which is in concordance with the value in Table B.1.

Branch Energy Variation

The results obtained from the compensating current calculation in (B.2) can be further used to validate the calculation of the branch energy disturbance defined in (4.8). This equation is further simplified in (4.17), which is applied to design the module capacitors.

By substituting (B.2) into (4.8), as well as parameters from Table B.1, the branch energy disturbances can be estimated:

$$\begin{aligned} \Delta e_{\mathrm{bA}} &= 27.2\ \mathrm{J} \quad , \\ \Delta e_{\mathrm{bB}} &= 46.9\ \mathrm{J} \quad . \end{aligned} \tag{B.4}$$

Comparing these values to the branch energy variations obtained from the simulation results plotted in Figure B.1

$$\begin{aligned} \Delta e_{\mathrm{b1}} &= 612.2\ \mathrm{J} - 583.7\ \mathrm{J} = 28.5\ \mathrm{J} \quad , \\ \Delta e_{\mathrm{b2}} &= 624.2\ \mathrm{J} - 576.4\ \mathrm{J} = 47.8\ \mathrm{J} \quad , \end{aligned} \tag{B.5}$$

it can be stated that the analytic calculation matches the simulation with a high accuracy.

Module Energy Disturbance Due to Delayed Switching

Equation (4.19) estimates a worst-case peak-to-peak energy disturbance for the modules within the same branch, which is caused by the delayed switching of the modules in order to limit the $\mathrm{d}v/\mathrm{d}t$ of the branch voltage, and thus of the output voltage.

For the validation, the maximum compensating current $I_{\mathrm{b,c,max}}$ is assumed to be equal to the compensating current of Branch A $|I_{\mathrm{bA,c}}| = 168.4$ A according to (B.2) and the maximum capacitor voltage is assumed to have approximately the same value as the setpoint voltage value from Table B.1: $V_{C,\mathrm{max}} \approx V_C^* = 1$ kV. Substituting these parameters together with the remaining necessary parameters from Table B.1 into (4.19), the worst-case peak-to-peak estimation of energy imbalance between the modules can be calculated:

$$\Delta e_{\mathrm{mod,d,max}} = 3.34\ \mathrm{J}. \tag{B.6}$$

Comparing this worst-case estimation value to the values plotted in Figure B.1 (the minimum-to-maximum value of vector $\Delta\mathbf{e}_{C,\mathrm{b1}}$ is 1.8 J and of vector $\Delta\mathbf{e}_{C,\mathrm{b2}}$ is 2 J), it can be stated that the voltage imbalance between the modules is within the band defined by the analytic calculation. The difference between the analytic value and the simulated results can be explained by the changing values of branch currents during the rising and falling edges of branch voltages (in the analytic estimation, the branch currents are assumed to be constant within this period of time).

C Frequency and Modulation Index Sweep Experiments

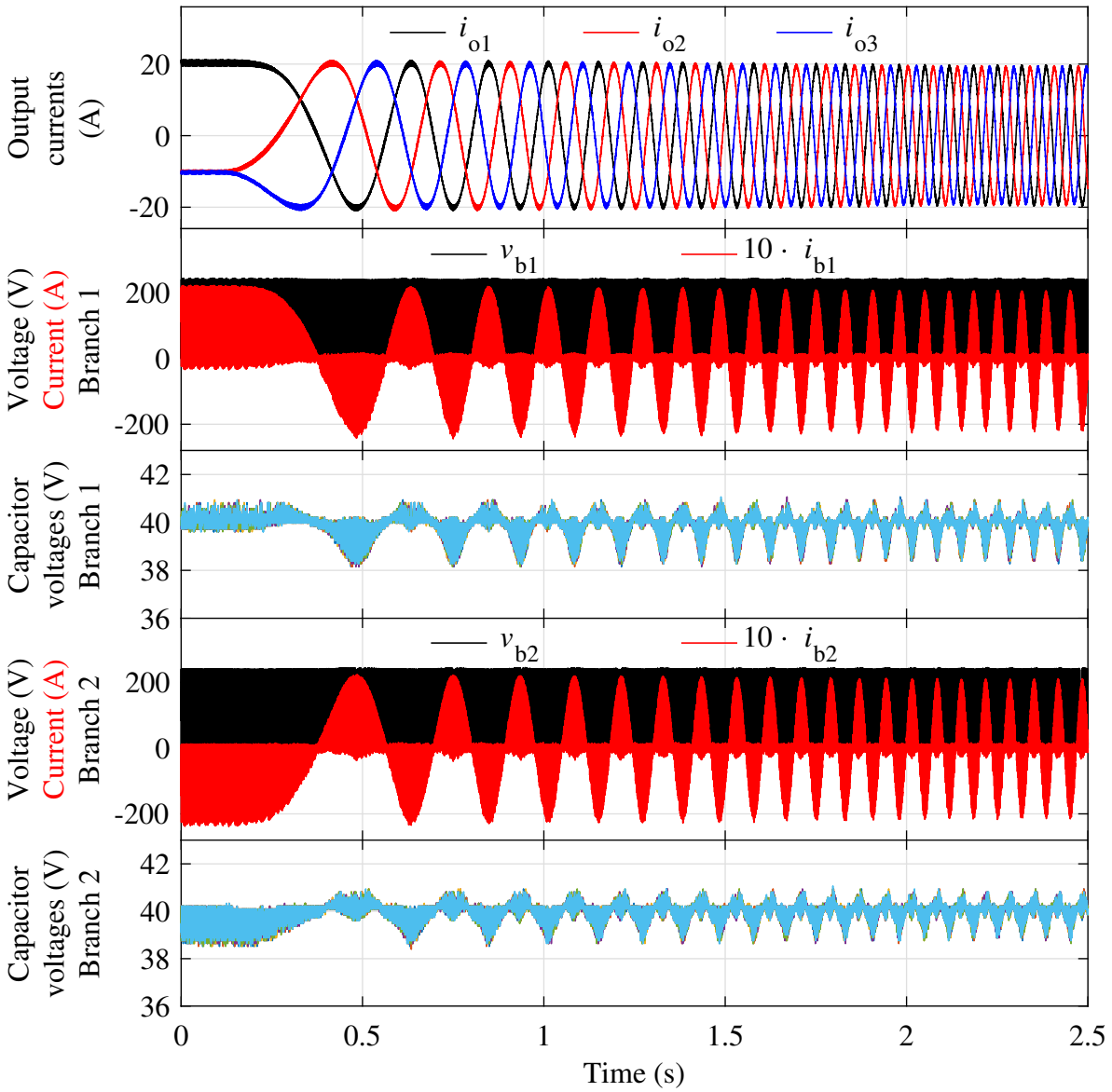


Figure C.1: Frequency sweep experiment measured on the downscaled quasi-two-level PWM-operated MMC prototype with a passive load. The output frequency f was varied from 0 Hz to 15 Hz. **Fast proportional branch-energy control** is applied. The modulation index is $M = 0.8$. The parameters of the MMC prototype are summarized in Table 6.1. The output inductance is $L_o = 13$ mH. The output resistance is $R_o \approx 4.5\ \Omega$. The waveforms are captured using *Protolar Supervisor*.

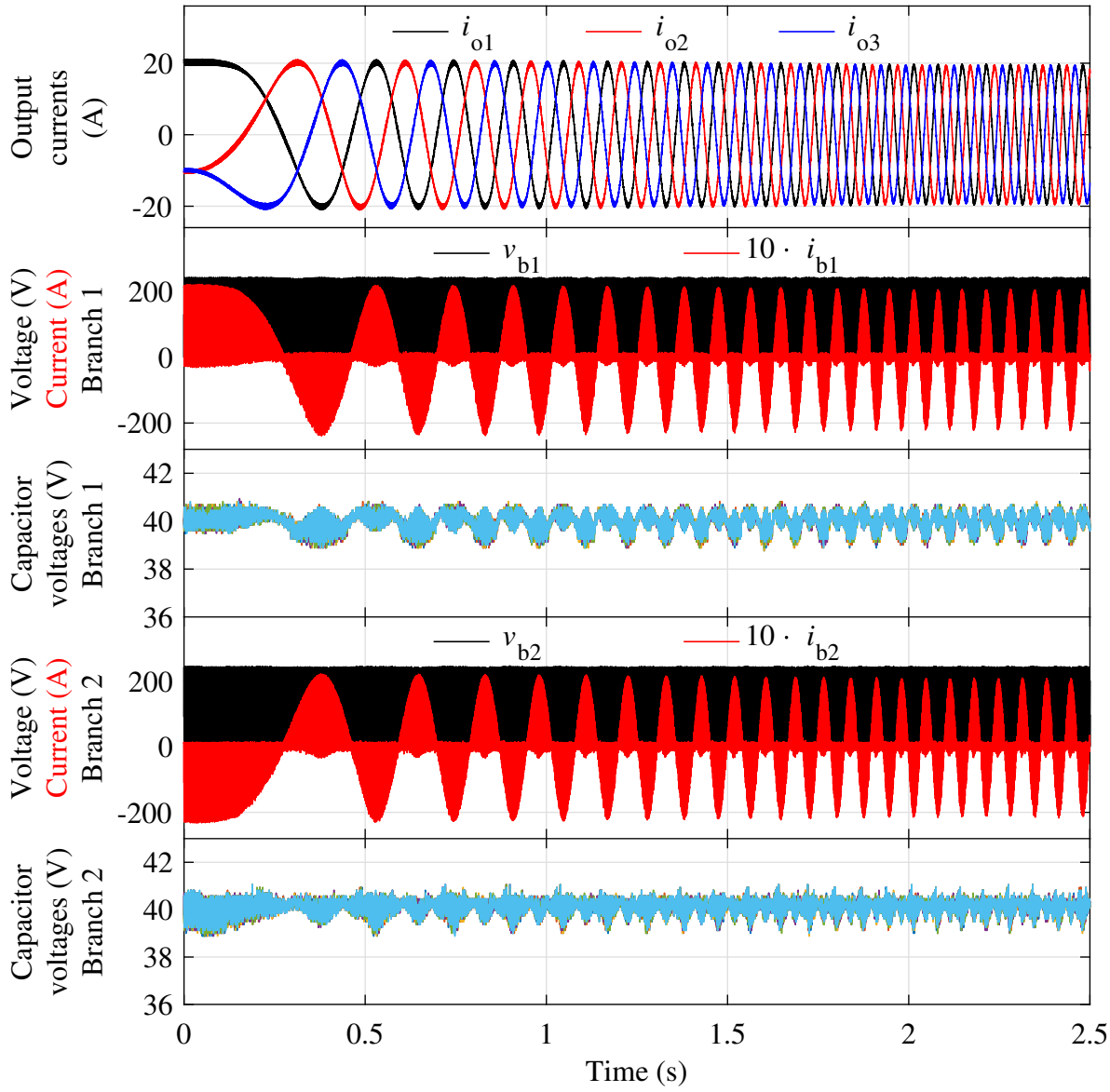


Figure C.2: Frequency sweep experiment measured on the downscaled quasi-two-level PWM-operated MMC prototype with a passive load. The output frequency f was varied from 0 Hz to 15 Hz. **Predictive branch-energy control** is applied. The modulation index is $M = 0.8$. The parameters of the MMC prototype are summarized in Table 6.1. The output inductance is $L_o = 13$ mH. The output resistance is $R_o \approx 4.5\ \Omega$. The waveforms are captured using *Protolar Supervisor*.

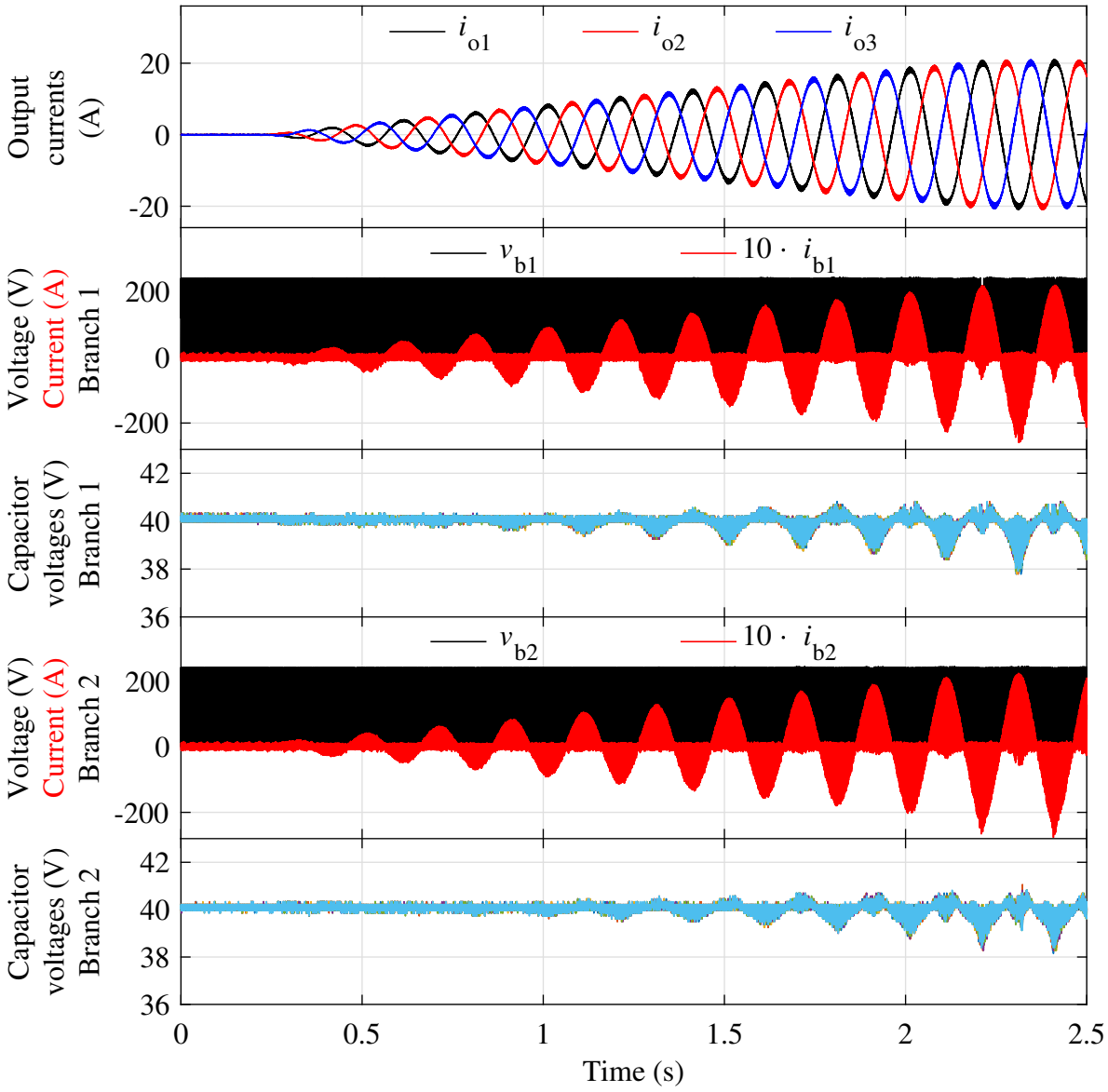


Figure C.3: Modulation index sweep experiment measured on the downscaled quasi-two-level PWM-operated MMC prototype with a passive load. The modulation index M was varied from 0 to 0.9. **Fast proportional branch-energy control** is applied. The output frequency is $f = 5$ Hz. The parameters of the MMC prototype are summarized in Table 6.1. The output inductance is $L_o = 13$ mH. The output resistance is $R_o \approx 5\ \Omega$. The waveforms are captured using *Protolar Supervisor*.

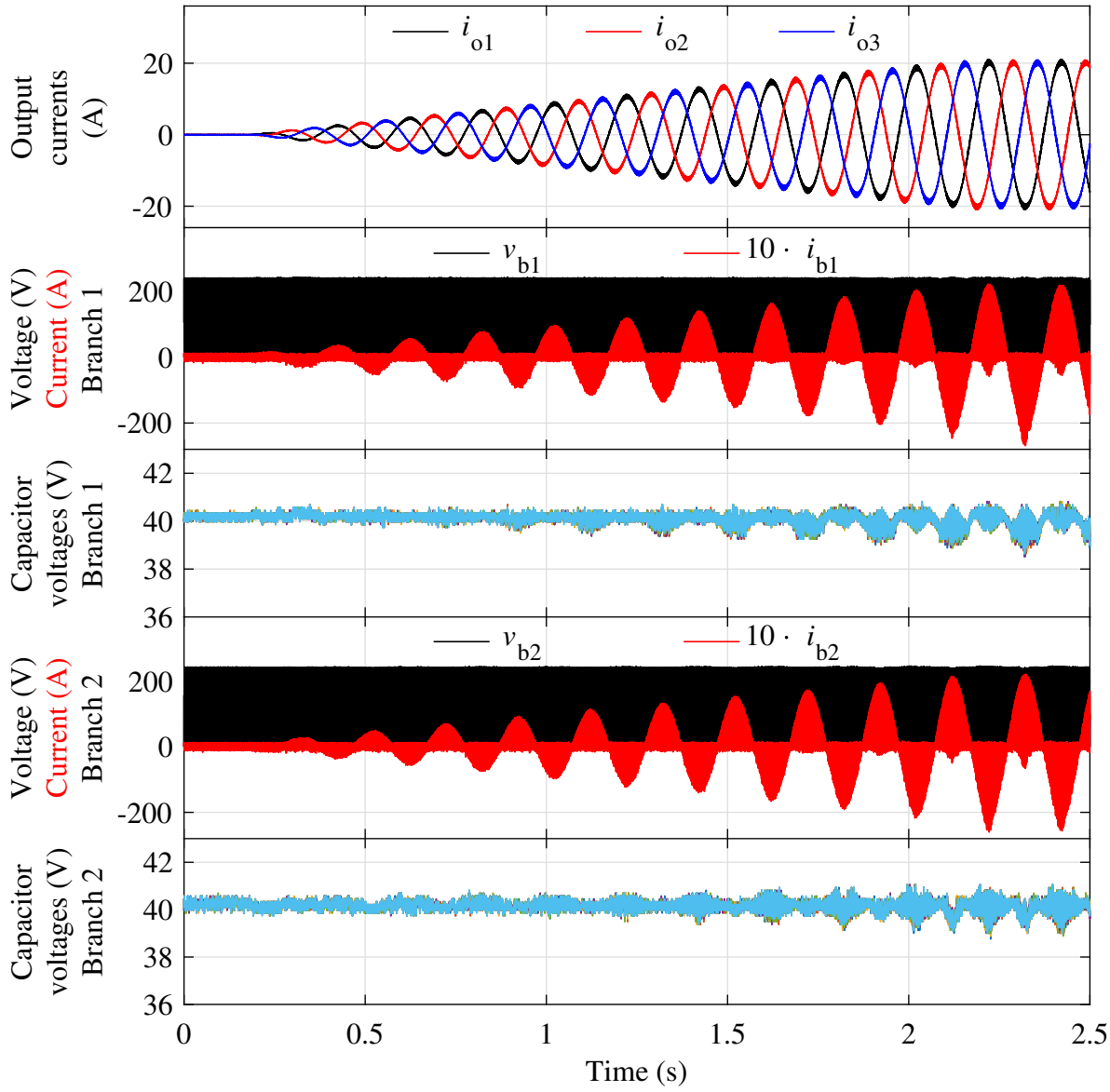


Figure C.4: Modulation index sweep experiment measured on the downscaled quasi-two-level PWM-operated MMC prototype with a passive load. The modulation index M was varied from 0 to 0.9. **Predictive branch-energy control** is applied. The output frequency is $f = 5$ Hz. The parameters of the MMC prototype are summarized in Table 6.1. The output inductance is $L_o = 13$ mH. The output resistance is $R_o \approx 5\ \Omega$. The waveforms are captured using *Protolar Supervisor*.

D Comparison of Branch-Energy Control Methods with Matched Converter Ratings

In Section 6.4, measurements of a downscaled quasi-two-level PWM-operated MMC with an accelerating synchronous machine are presented for both branch-energy control methods: fast proportional branch-energy control and predictive branch-energy control. While the predictive branch-energy control performs significantly better when high currents were required by the machine, the fast proportional branch-energy control leads to lower variation in the module capacitor voltages when output currents are very low. Although this finding is not surprising, the unexpected occurrence is that with the predictive branch-energy control the module capacitor voltage variation is almost the same for the low machine currents as it is for the high machine currents. The chapter concludes that this is caused by the severe output current ripple, which is a consequence of the unmatched current rating between the converter and the machine. Additionally, it is claimed that the predictive branch-energy control performs generally better than fast proportional branch-energy control if the converter were matched for the machine. This statement is confirmed in this chapter by simulations of a quasi-two-level PWM-operated MMC with ratings matched to those of the machine.

In order to operate the $50/3$ Hz synchronous machine at the rated current, the rated speed, and the rated voltage, the field-linked direct axis flux linkage has to be decreased. Additionally, the rotational inertia is increased to obtain a similar acceleration time to that seen in the measurements. The updated parameters of the machine are summarized in Table D.1.

Table D.1: Updated parameters of the synchronous machine used for the investigations.

Rated stator voltage	V_{sN}	220 V
Rated stator current	I_{sN}	66 A
Rated stator frequency	f_{sN}	50/3 Hz
d-axis inductance	L_{d}	11 mH
q-axis inductance	L_{q}	5 mH
Stator resistance	R_{s}	0.35 Ω
Field-linked direct axis flux linkage	Ψ_{fd}	1.34 Vs
Pole pairs	p	2
Rotational inertia	J	10.7 kg m^2

The quasi-two-level PWM-operated MMC from Chapter 6 is redesigned to match the machine ratings according to the design process described in Section 8.4. The updated parameters of the downscaled converter prototype are listed in Table D.2.

Table D.2: Updated parameters of the downscaled converter prototype.

Parameter		Fast proportional	Predictive
Input voltage	V_i	350 V	350 V
Peak output current	$\hat{i}_\mathrm{o}$	up to 95 A	up to 95 A
Maximum allowed duty cycle	δ_max	0.9	0.9
Leg inductance (coupled)	L_leg	80.5 µH	80.5 µH
Branch resistance	R_b	10 mΩ	10 mΩ
Modules per branch	n_mpb	6	6
Module capacitance	C_mod	560 µF	560 µF
Setpoint module capacitor voltage	V_C^*	65 V	65 V
PWM frequency	f_PWM	1 kHz	1 kHz
HF modulation frequency	f_HF	25 kHz	25 kHz
Delay between switch. instants	T_d	1 µs	1 µs
Energy controller gain	$G_{\mathrm{P},e}$	2000	1200
HF current amplitude	$\hat{i}_\mathrm{HF}$	0.9 A (const.)	1.35 A (smart)
HF current threshold	$I_\mathrm{c,thr}$	-	0.68 A (smart)

These parameters are used to carry out the simulations. In Figure D.1, the acceleration of a machine fed by quasi-two-level PWM-operated MMC employing fast-proportional branch-energy control is plotted. In Figure D.2, the results for the same case with predictive branch-energy control are shown.

As expected, the applied branch-energy control methods do not affect the machine control. Note that the dynamic behavior of the machine is slightly different from the measurements presented in Section 6.4. The reasons for this difference are the friction not being modeled in the simulations and the absence of speed low-pass filter in the simulated control system.

Similar to the measurements from Section 6.4, the predictive branch-energy control leads to higher module capacitor voltage variation than the fast proportional control when the output currents are very low. When the output currents are high, the predictive branch-energy control manages the energy control more effectively. In contrast to the measurements, the module capacitor voltage variation in simulations is significantly lower when output currents are low than when output currents are high. Hence, the statement that the predictive branch-energy control is more advantageous when the converter ratings are matched to the ratings of the machine is valid.

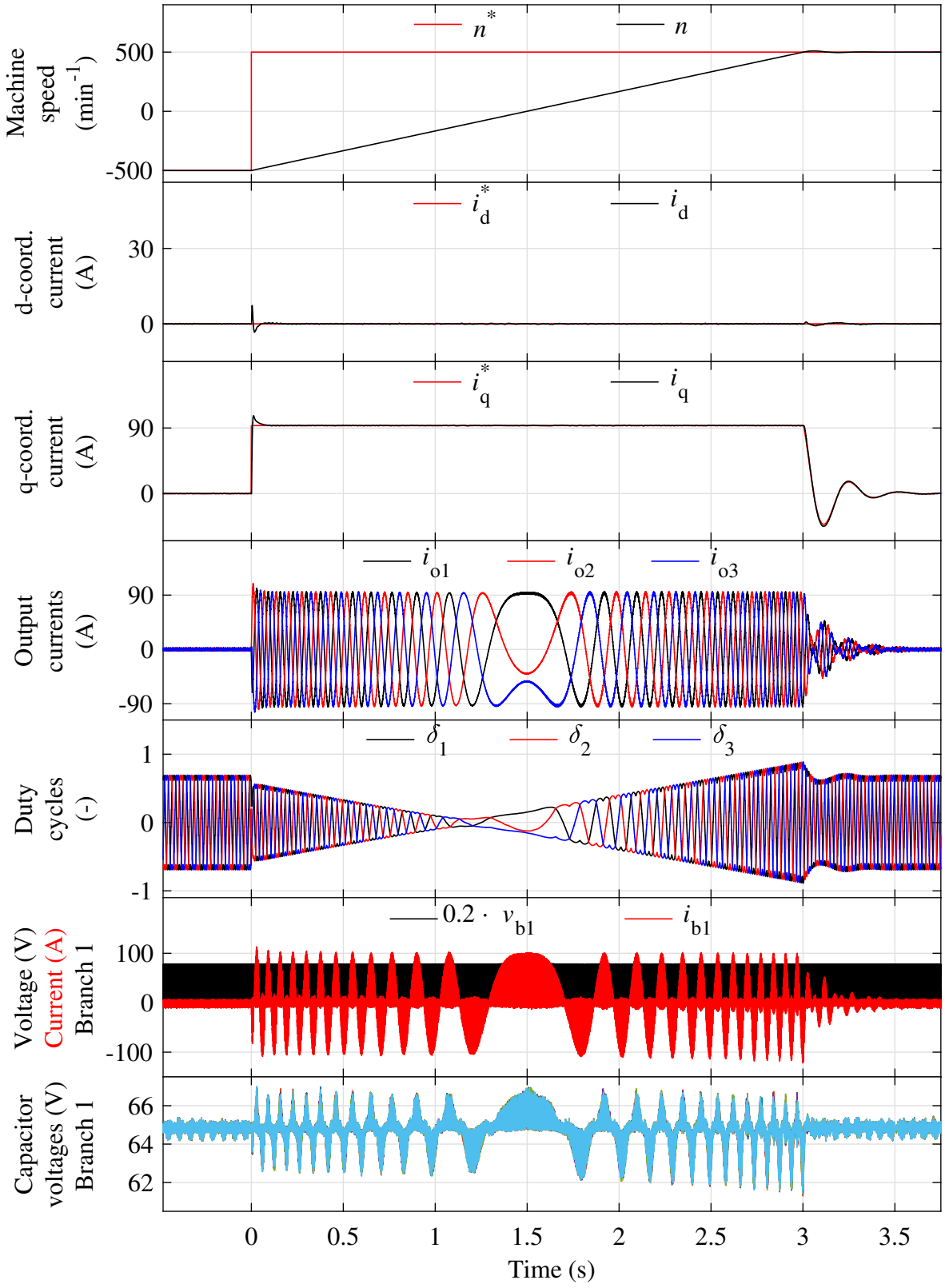


Figure D.1: Simulation of synchronous machine acceleration with quasi-two-level PWM-operated MMC. **Fast proportional branch-energy control** is applied. Machine parameters are listed in Table D.1. Converter parameters are listed in Table D.2.

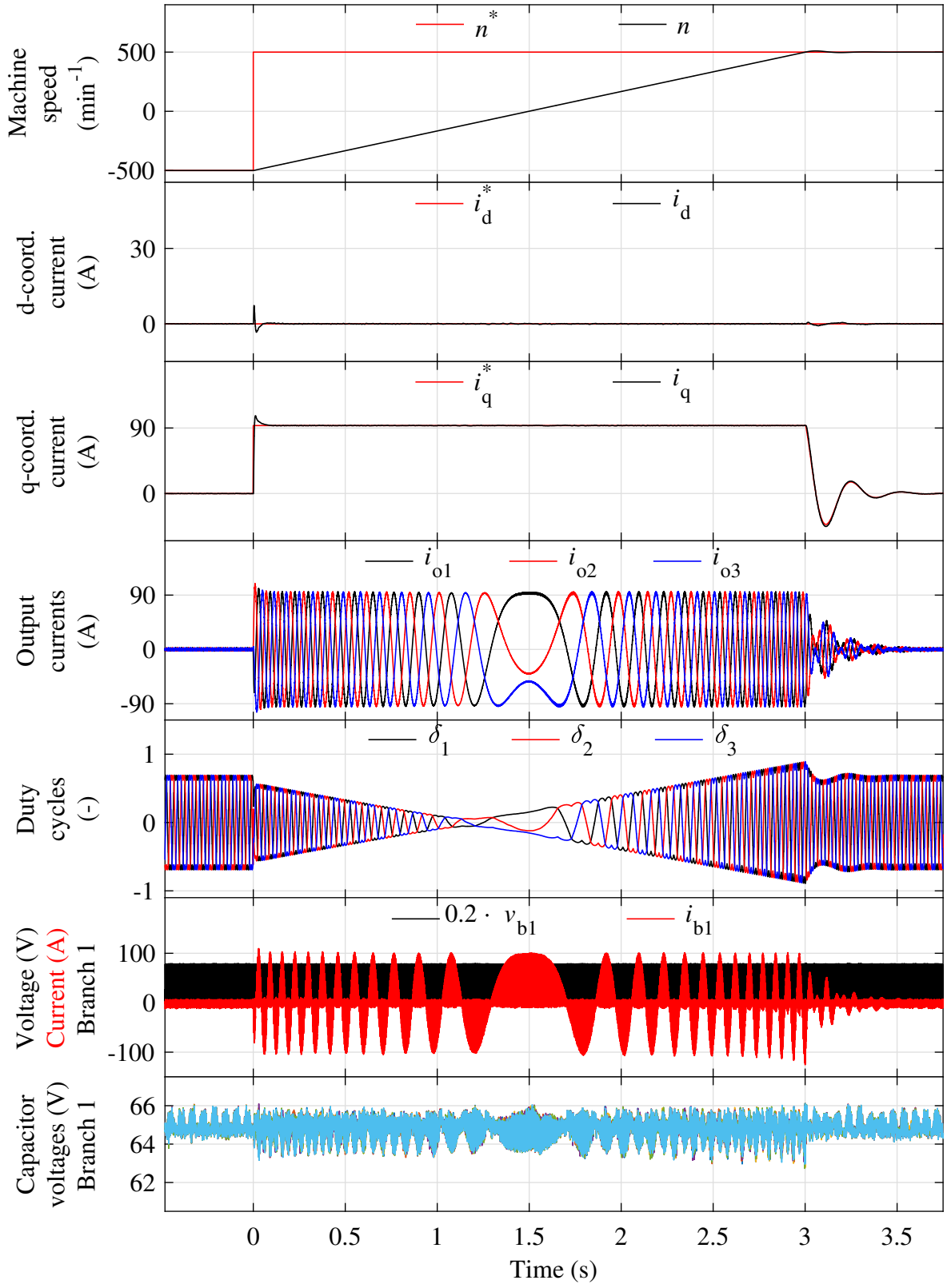


Figure D.2: Simulation of synchronous machine acceleration with quasi-two-level PWM-operated MMC. **Predictive branch-energy control** is applied. Machine parameters are listed in Table D.1. Converter parameters are listed in Table D.2.

E Validation of Loss and Thermal Models

The proposed semiconductor loss model and the proposed thermal model, described in Section 8.3.2 and Section 8.3.3, respectively, are validated using *Mathworks Simulink* simulations with *Plexim Plecs* toolbox. The applied simulation model created in *Plecs* is shown in Figure E.1. The inputs of the model are the branch current "ib" and the switching state "s". The time vectors for these inputs were generated by the simulations of the converter with a machine used for the converter design. The time vectors contain values over a single output period. In the following simulations, the waveforms from these vectors are repeated for multiple periods until a thermal steady-state is achieved. The model consists of a single half-bridge module, comprising two IGBTs and two diodes. The IGBT and diode models from *Plecs* provide calculation of losses and also include a Cauer model for the thermal domain simulations. The parameters of the Cauer model representation are generated from the Foster model representation parameters by a built-in function from *Plecs*.

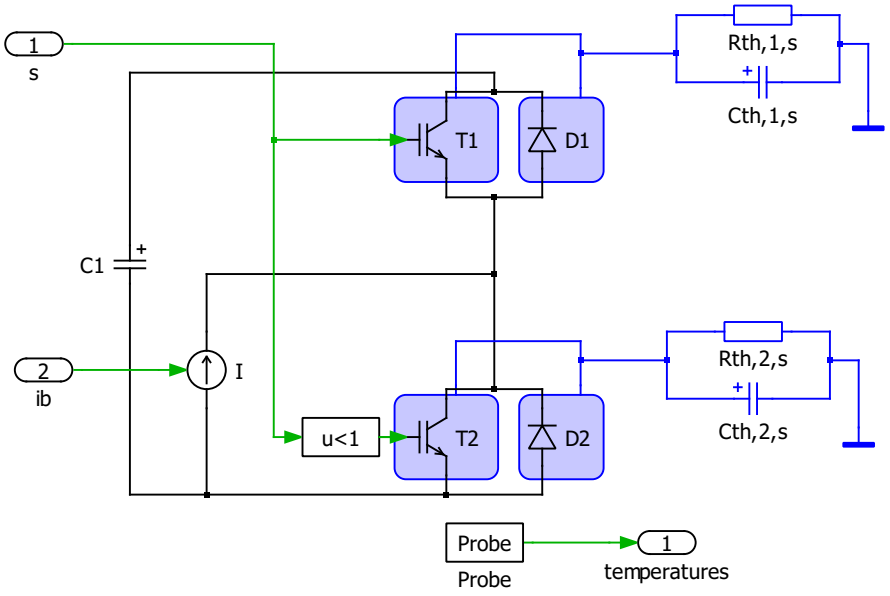


Figure E.1: Implementation of the thermal and loss model in *Plexim Plecs* toolbox.

All parameters for the calculation of losses and the thermal parameters are obtained from the IGBT module's datasheet [145]. The sink thermal resistance is chosen to be $R_{\vartheta,\mathrm{ref,s}} = 50$ mK/W, and the sink thermal capacitance is neglected $C_{\vartheta,\mathrm{ref,s}} = 0$ J/K to speed up the simulation. This simplification is possible because the last section of the Cauer model provides enough capacitance for the case temperature to remain almost constant.

In Figure E.2, the comparison between the proposed model and the *Plecs* model can be seen for the quasi-two-level PWM-operated MMC with unscaled modules ($a = 1$). The results for the LFM MMC operation are displayed in Figure E.3. Both figures show a good match between the

proposed model and the *Plecs* model with small absolute errors. The difference between the models is most likely caused by the discrete-time implementation of the proposed model. While the *Plecs* model is expected to be slightly more precise, the proposed model is significantly faster (approx. two hours with *Plecs* model vs. under one second with the proposed models at the same computer).

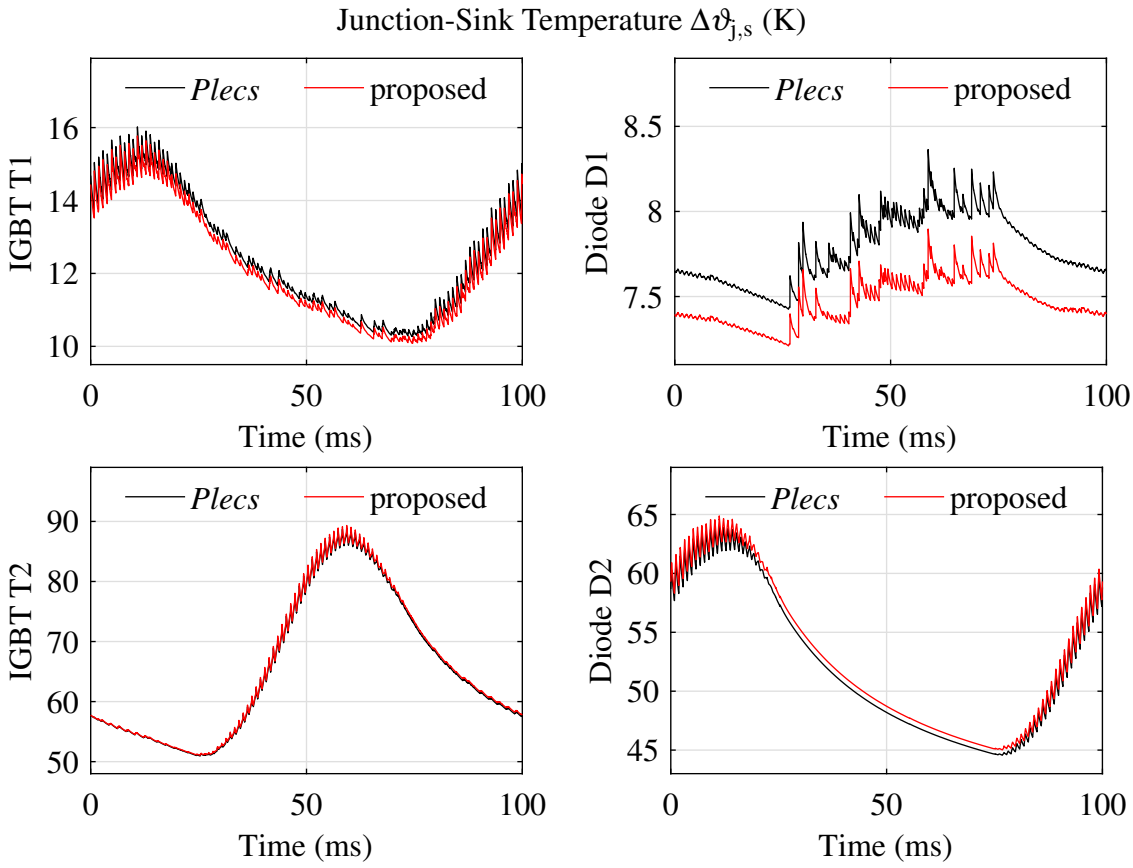


Figure E.2: Comparison of the resulting junction-sink temperature waveforms obtained from the *Plecs* model to those from the proposed model. The input data is from the first module in the first branch of the quasi-two-level PWM-operated MMC in study case A-I at 10 Hz.

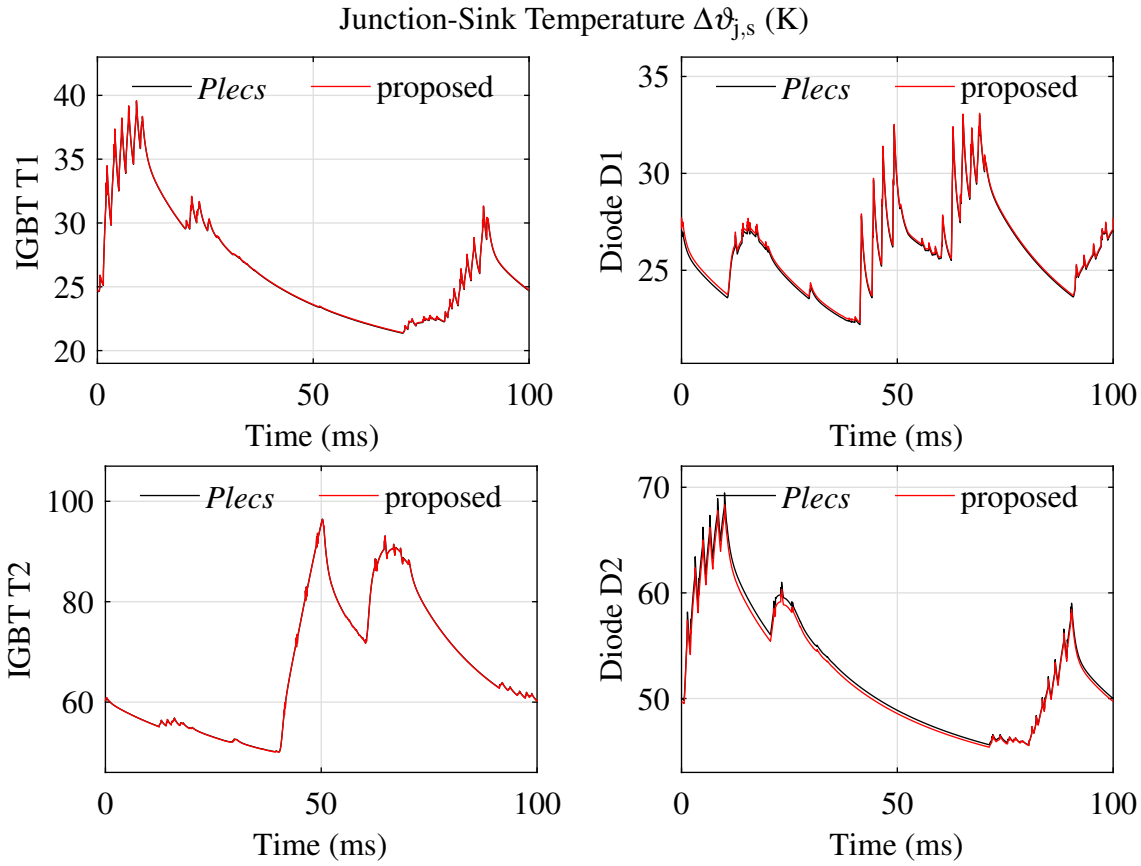


Figure E.3: Comparison of the resulting junction-sink temperature waveforms obtained from the *Plecs* model to those from the proposed model. The input data is from the first module in the first branch of the LFM operated MMC in study case A-I at 10 Hz.

F Dynamic Operation of Designed Converters

This appendix chapter shows the performance of the designed converters operating with machines. The operation starts at zero speed and the machine is accelerated with rated torque from time zero to its rated speed. During the whole simulation, the load torque value is one half of the machine's rated torque. The inertia of the system is adjusted so that the time required for acceleration is approximately five seconds.

Figures F.1 – F.4 show the dynamic machine operation of quasi-two-level PWM-operated MMCs designed for study cases A–D.

Figure F.5 and Figure F.6 show the operation of the standardly operated MMCs designed for study cases A-I and C-I.

Figures F.7 – F.10 show the operation of the two-level VSIs with series-connected IGBT modules designed for study cases A–D.

Figures F.11 – F.14 show the operation of the MMMCs designed for study cases A–D. Note that for MMMC, the plotted "virtual" duty cycles

$$\delta_x = \frac{v^*_{\mathrm{s}x}}{\sqrt{\frac{2}{3}} \cdot V_{\mathrm{sN}}}, \quad x \in \{1,2,3\} \tag{F.1}$$

are defined as a ratio between the setpoint stator voltage values and the rated phase voltage amplitude of the stator. Since the SVM is applied, the maximum value is approximately 0.87.

In conclusion, all designed converters are capable of stable operation with the selected synchronous machine over the whole investigated operating range.

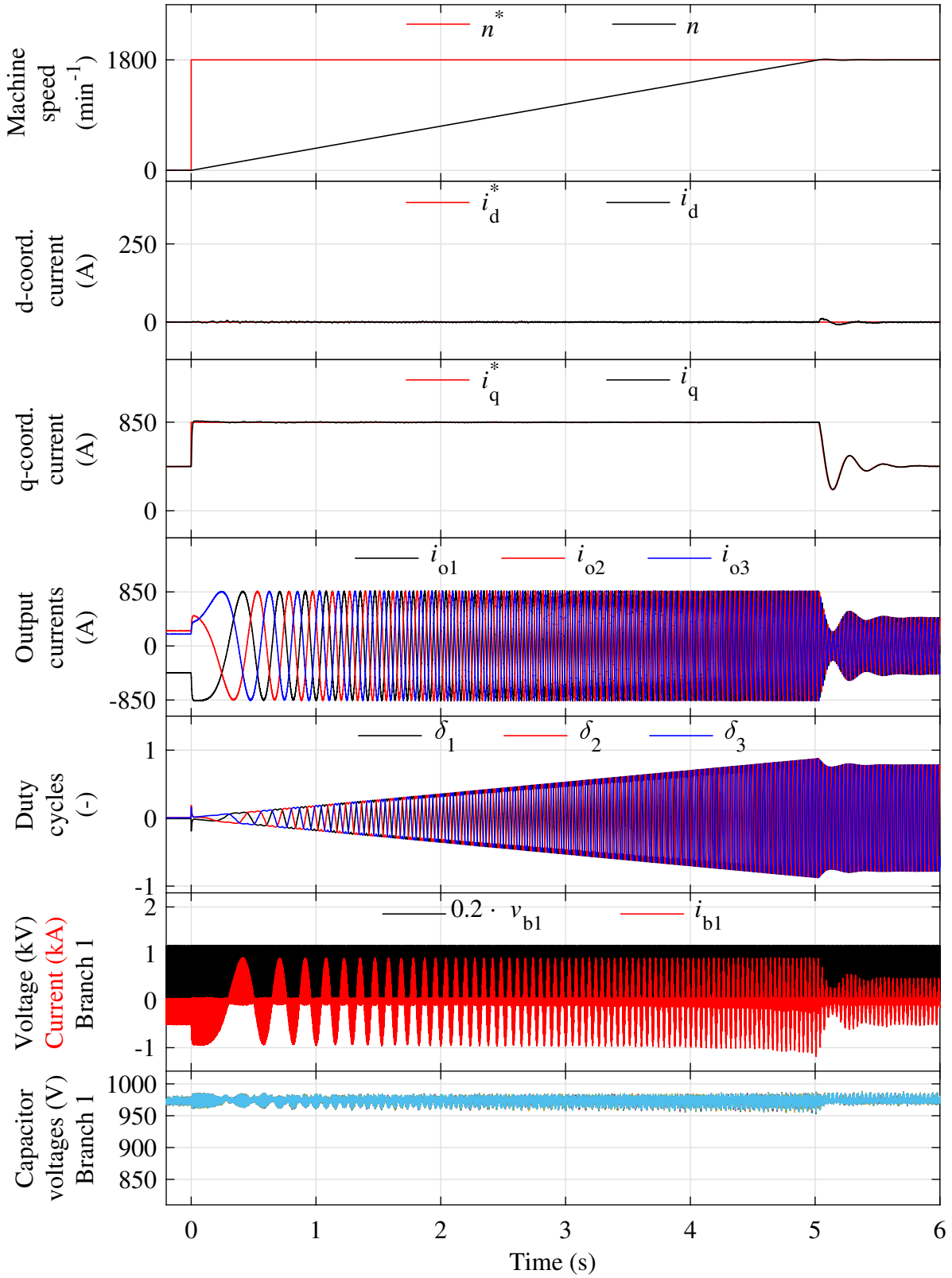


Figure F.1: Dynamic operation of the **quasi-two-level PWM-operated MMC** with a synchronous machine designed for study case **A**.

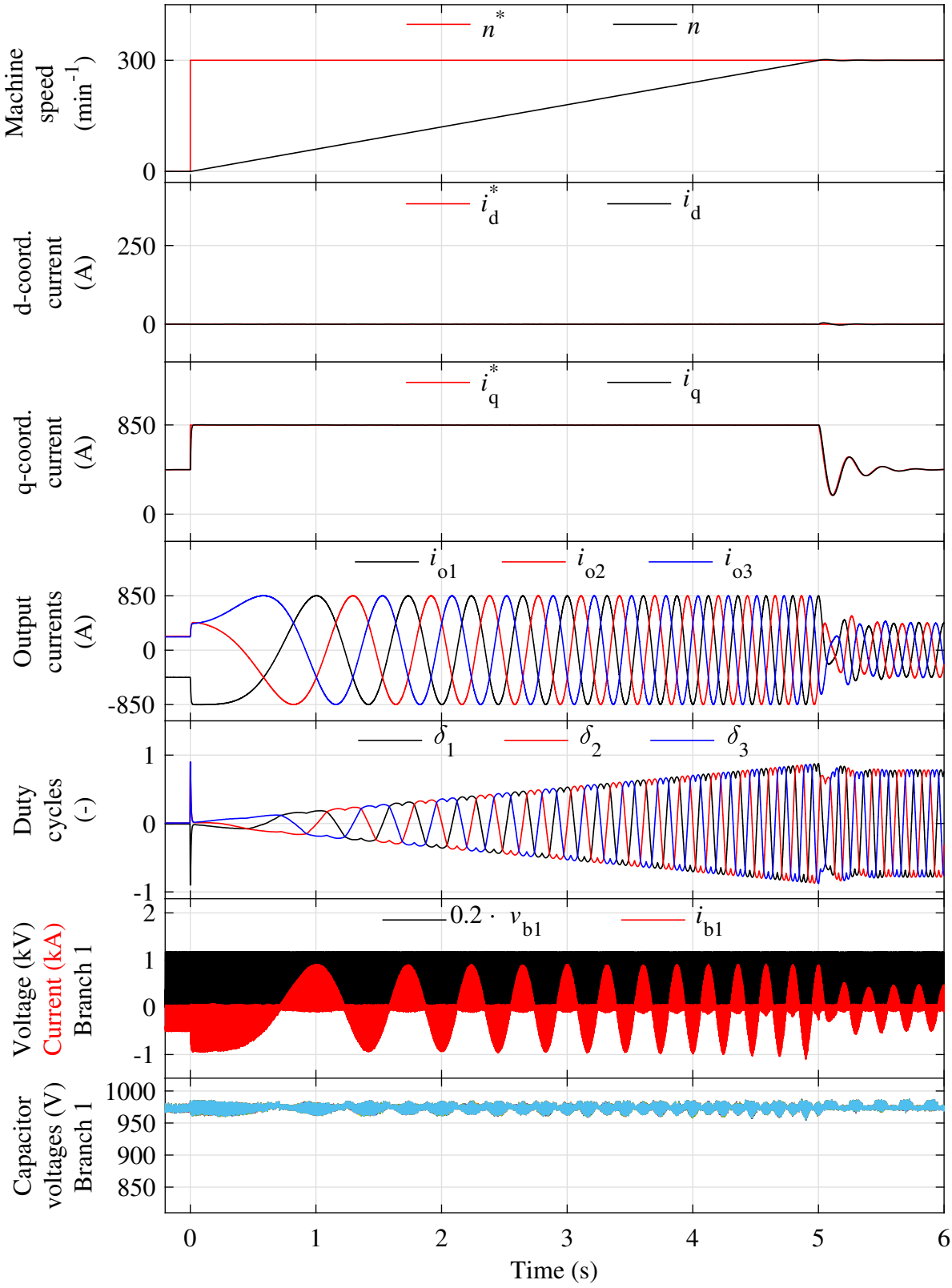


Figure F.2: Dynamic operation of the **quasi-two-level PWM-operated MMC** with a synchronous machine designed for study case **B**.

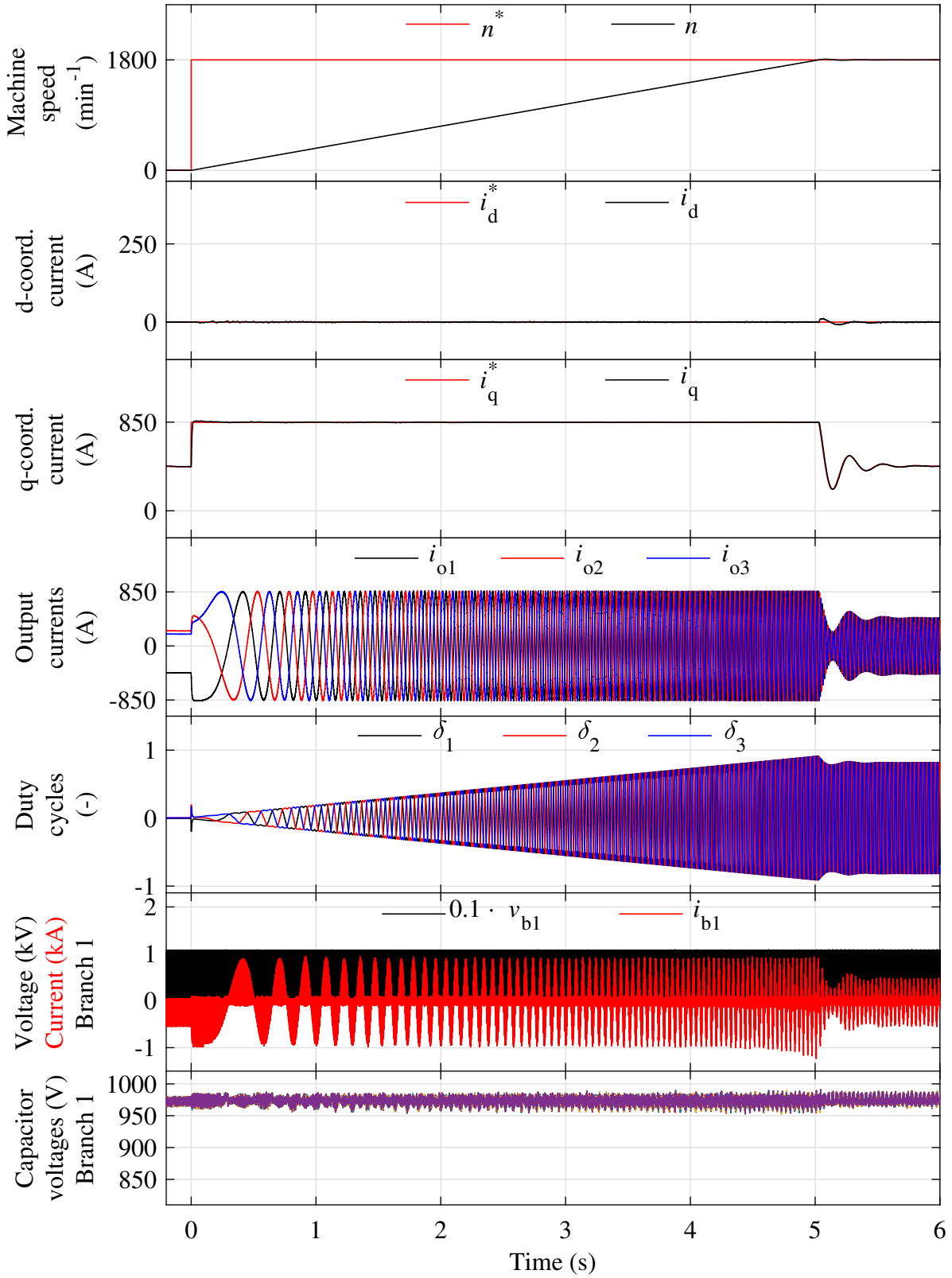


Figure F.3: Dynamic operation of the **quasi-two-level PWM-operated MMC** with a synchronous machine designed for study case **C**.

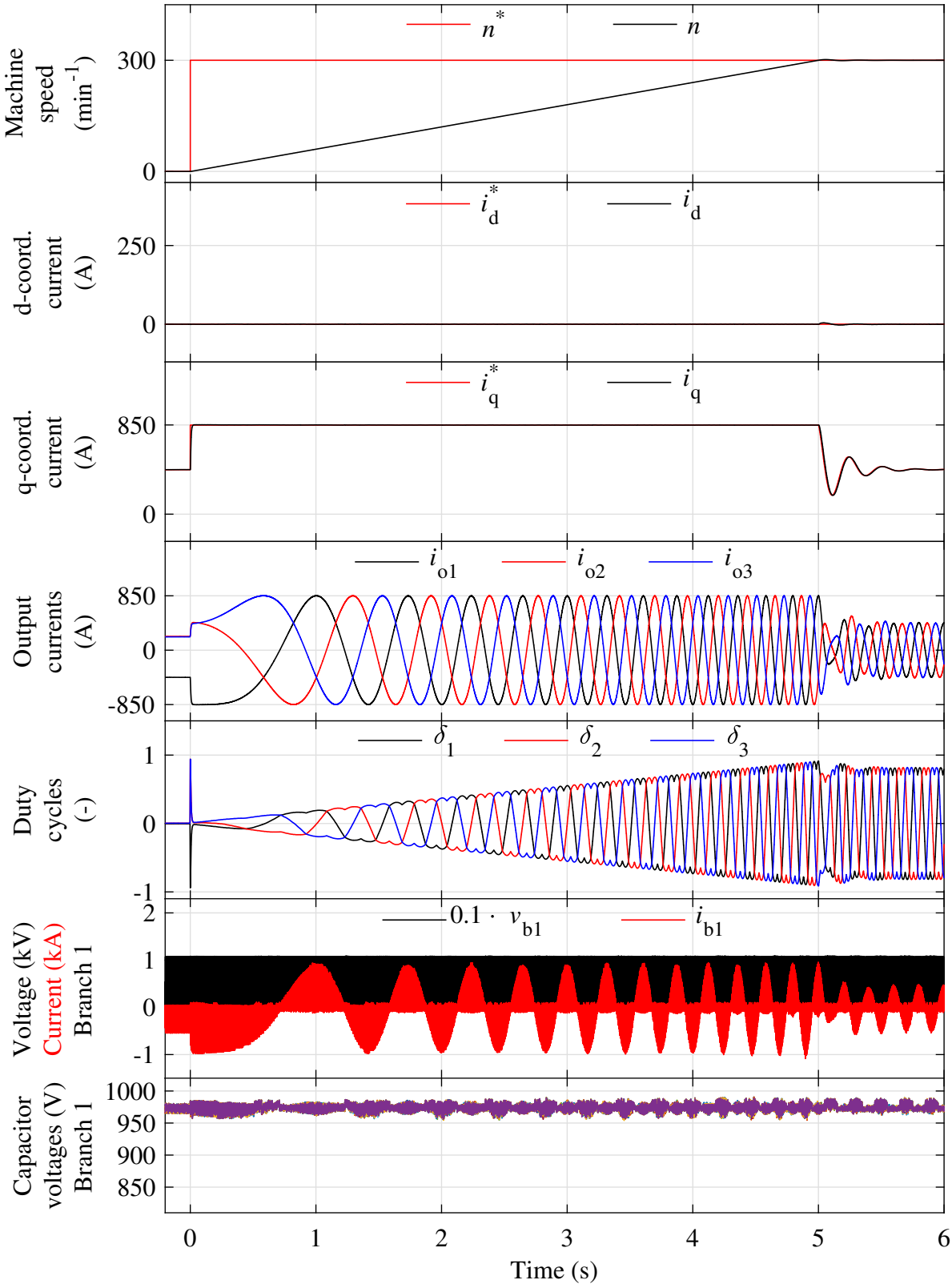


Figure F.4: Dynamic operation of the **quasi-two-level PWM-operated MMC** with a synchronous machine designed for study case **D**.

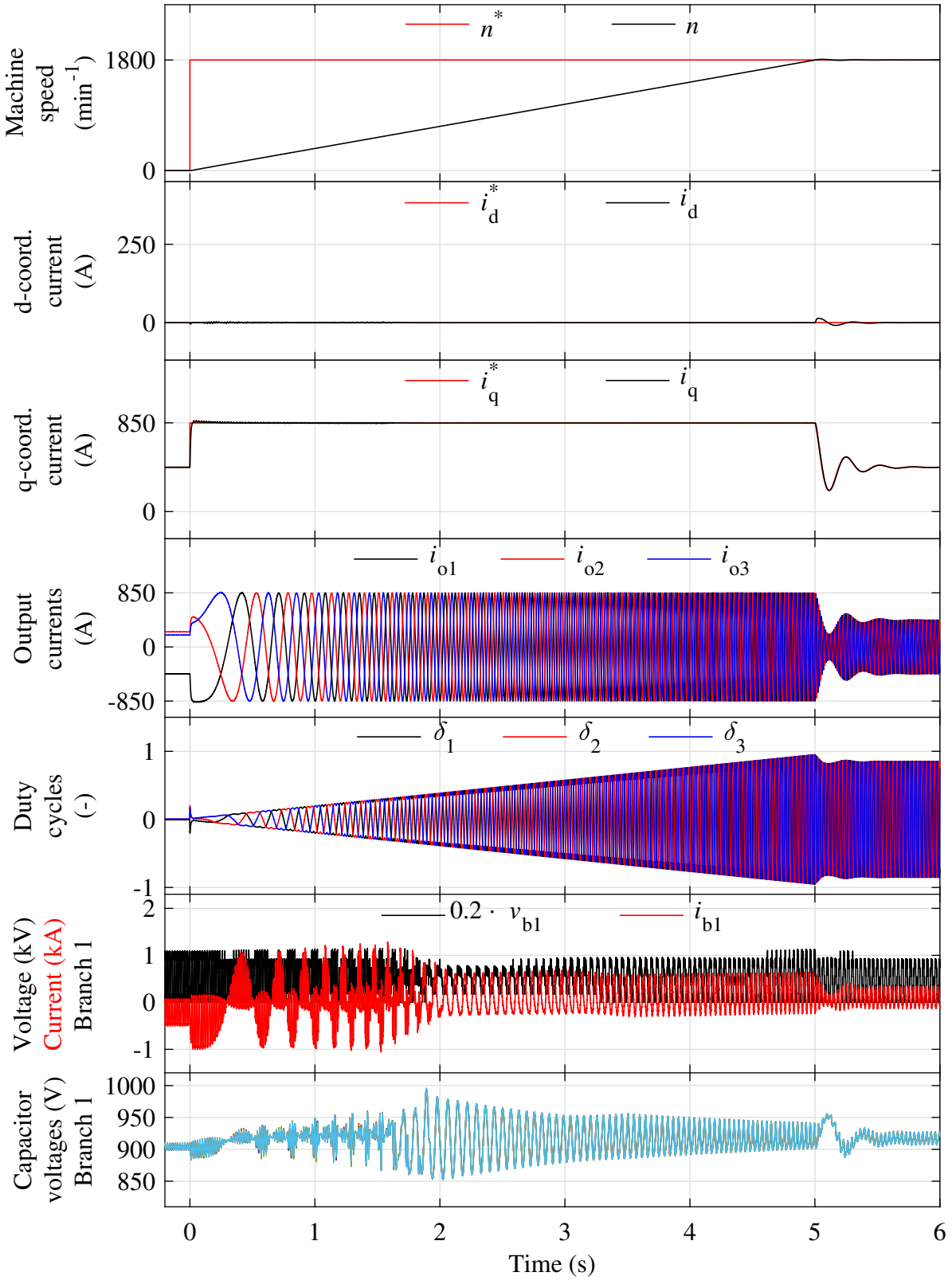


Figure F.5: Dynamic operation of the **standardly operated MMC** with a synchronous machine designed for study case **A-I**.

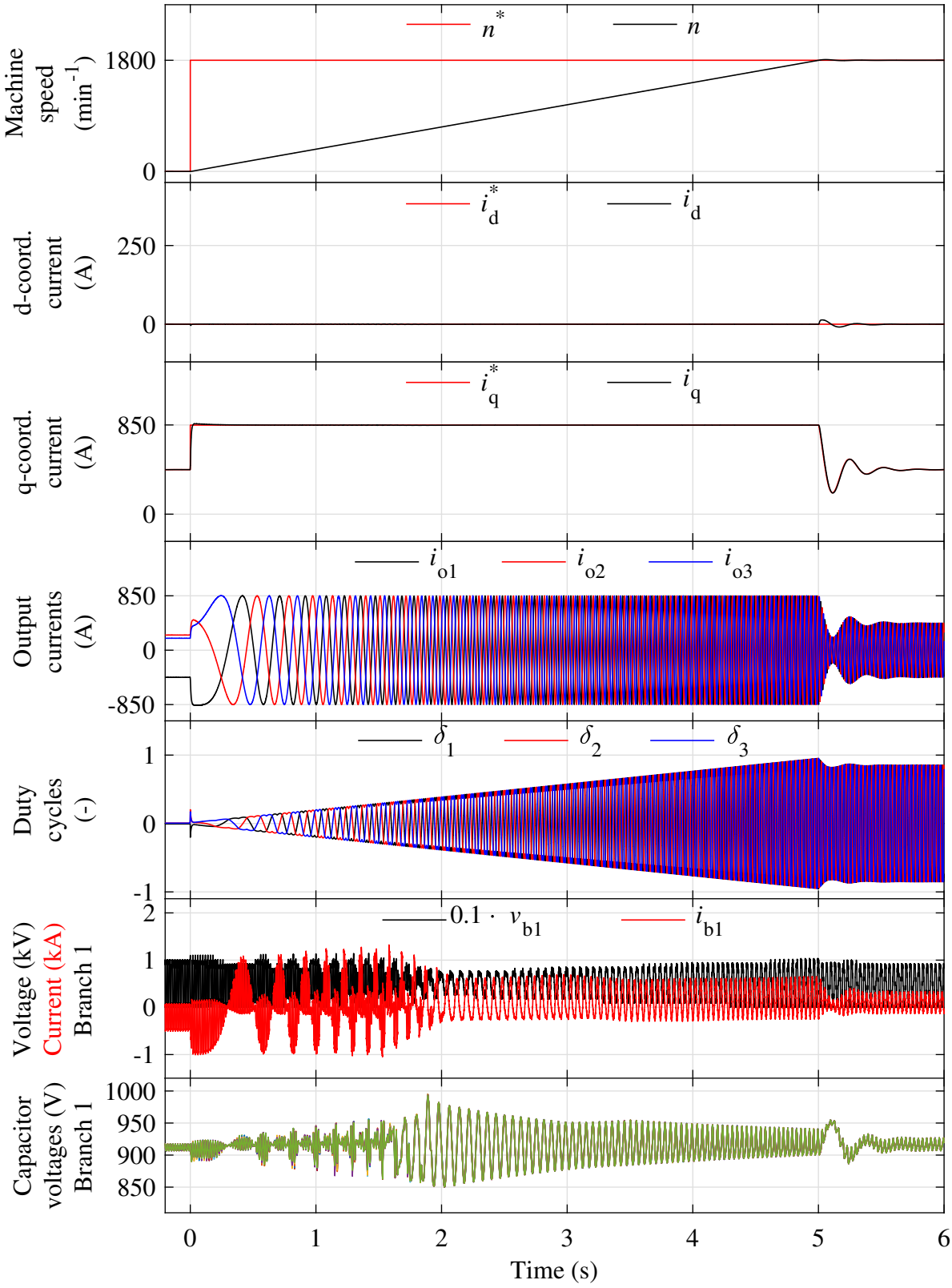


Figure F.6: Dynamic operation of the **standardly operated MMC** with a synchronous machine designed for study case **C-I**.

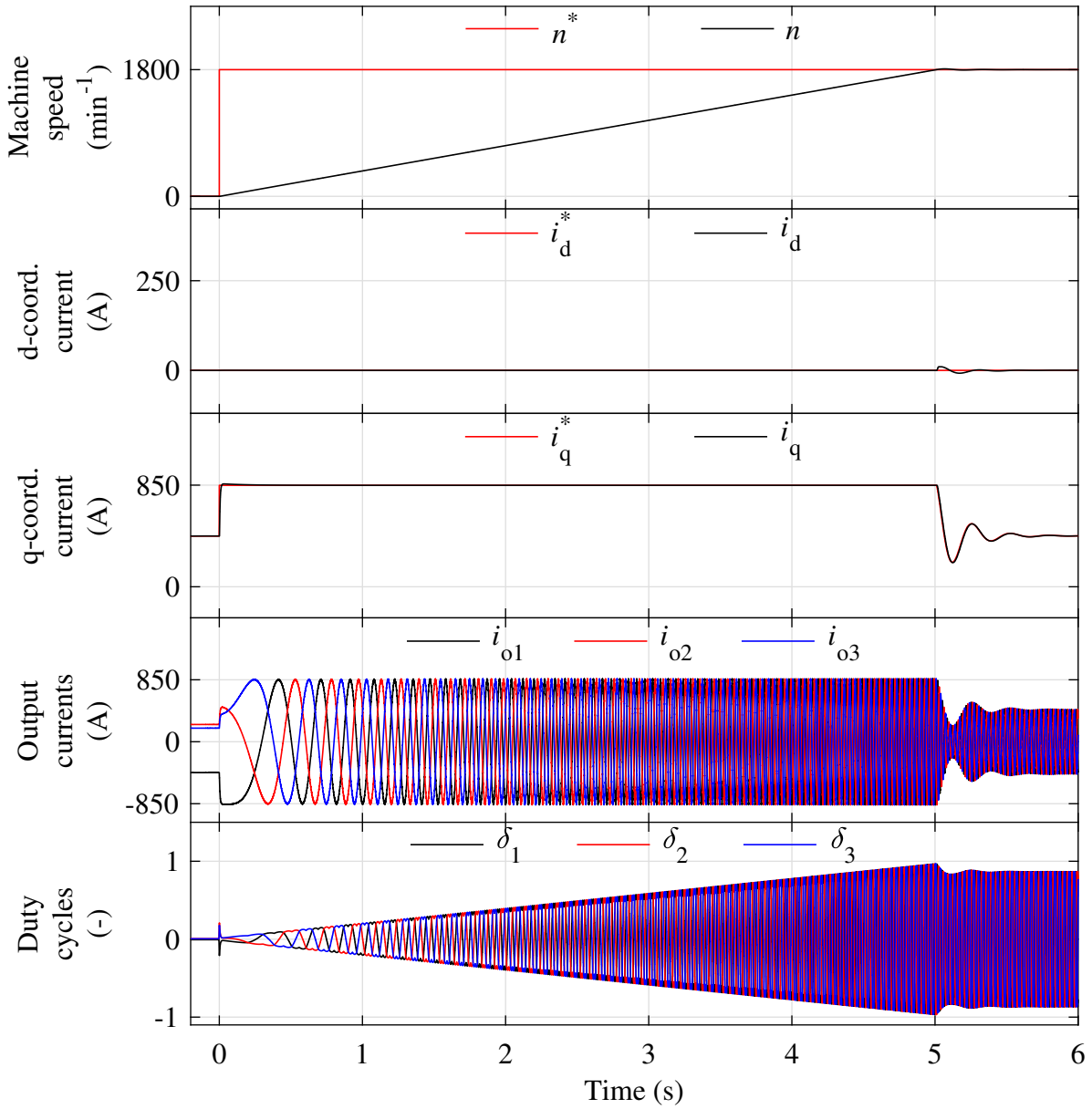


Figure F.7: Dynamic operation of the **two-level VSI** with synchronous a machine designed for study case **A**.

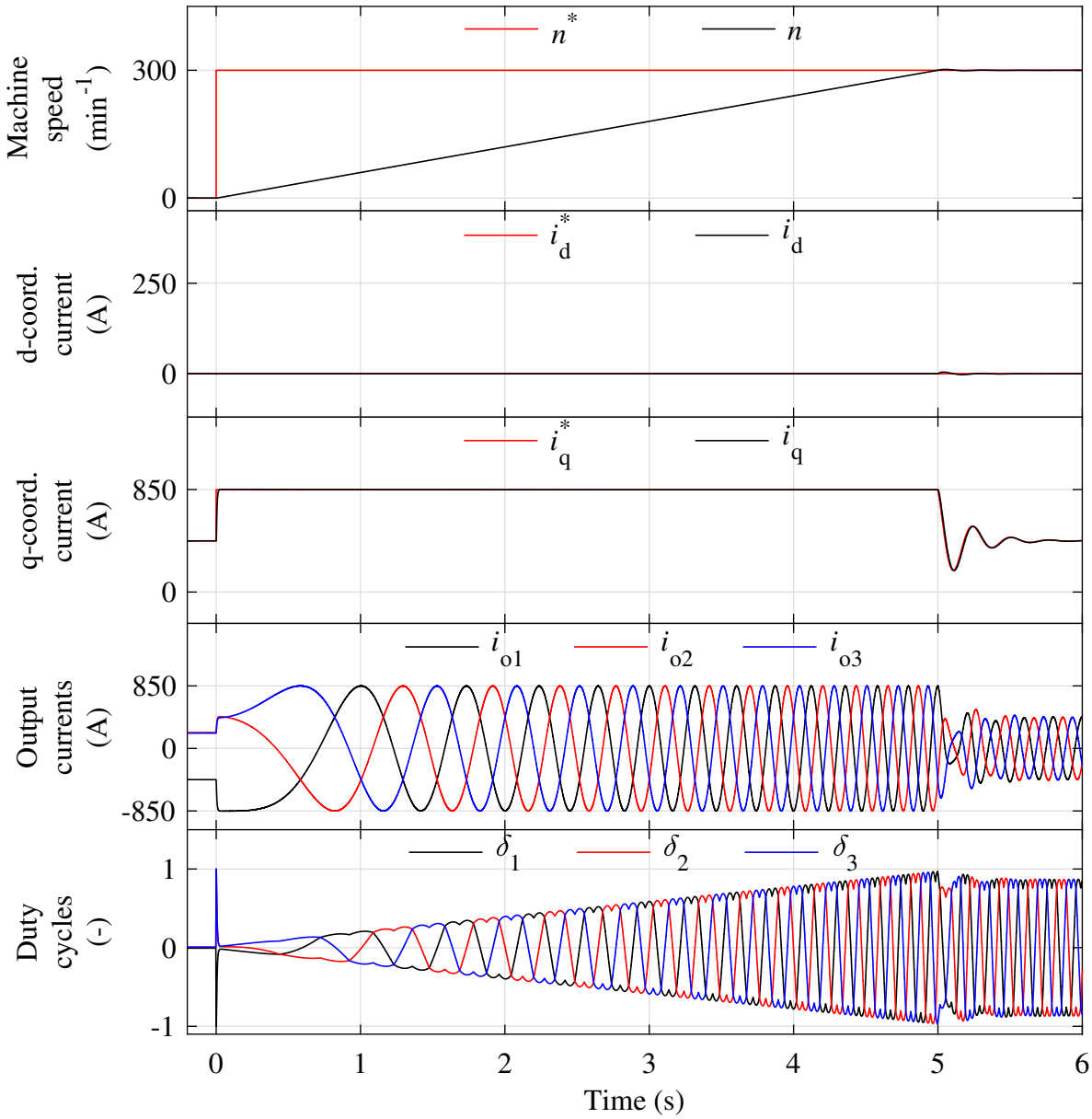


Figure F.8: Dynamic operation of the **two-level VSI** with synchronous a machine designed for study case **B**.

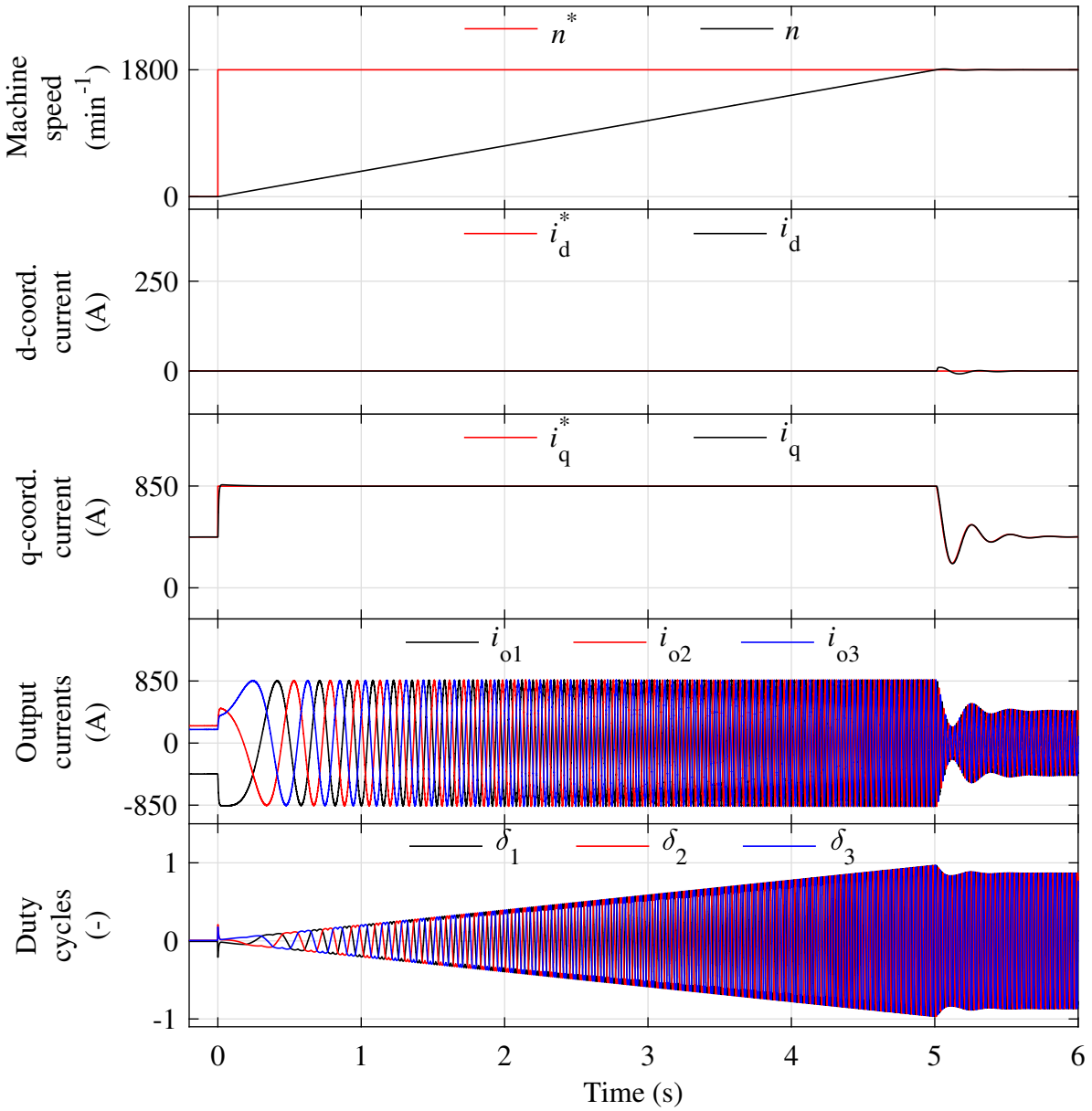


Figure F.9: Dynamic operation of the **two-level VSI** with synchronous a machine designed for study case **C**.

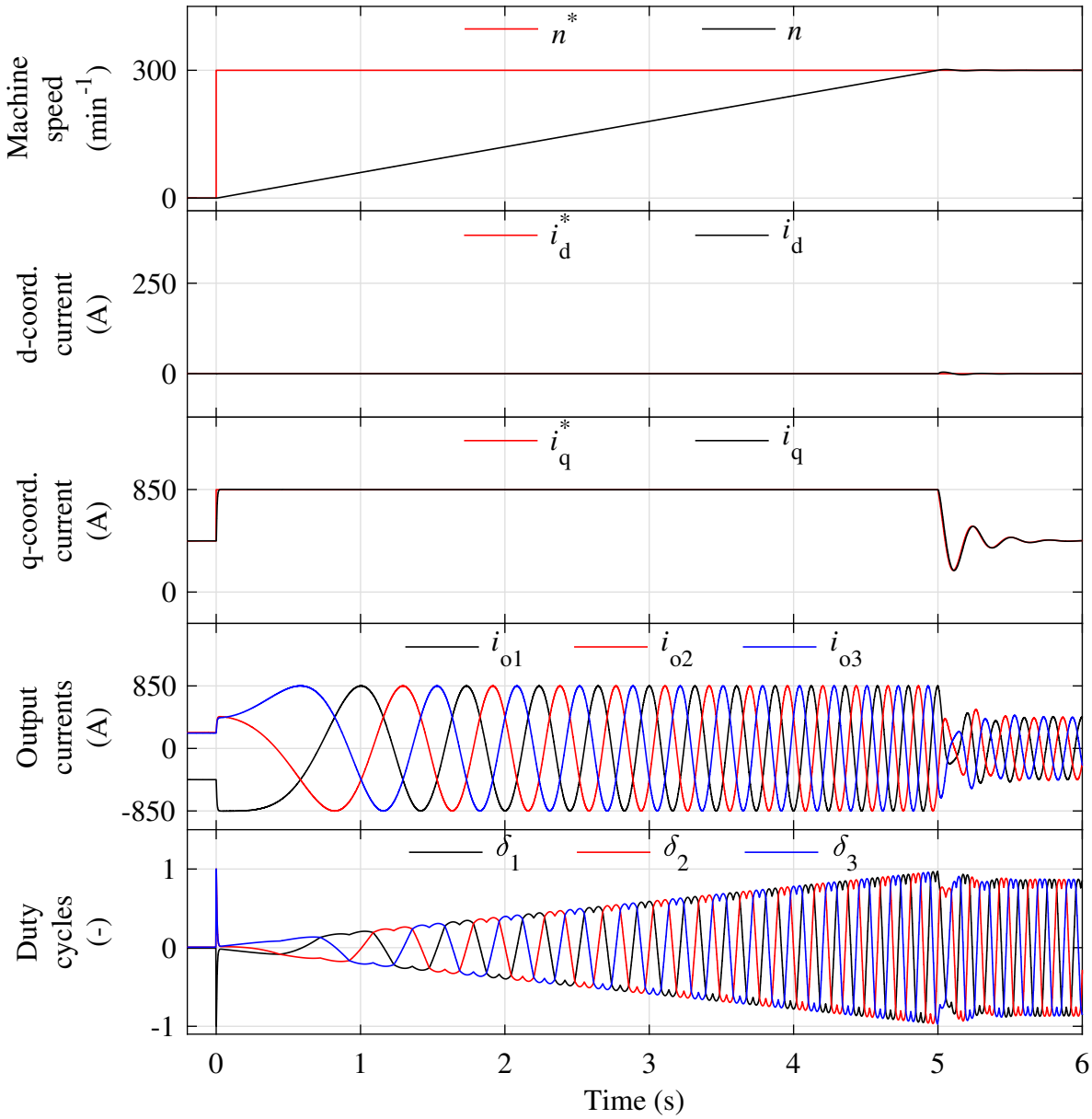


Figure F.10: Dynamic operation of the **two-level VSI** with synchronous a machine designed for study case **D**.

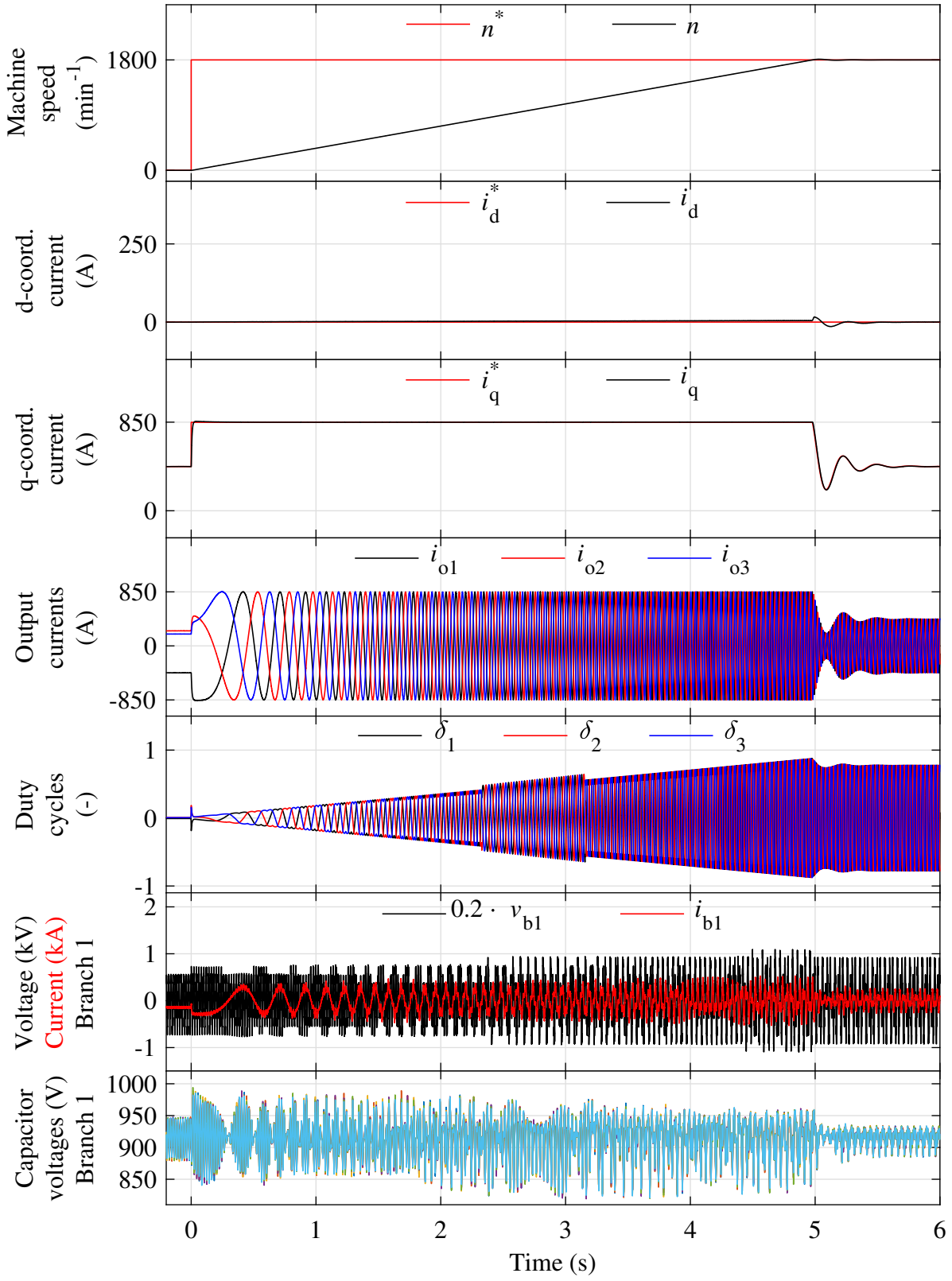


Figure F.11: Dynamic operation of the **MMMC** with a synchronous machine designed for study case **A**. The plotted duty cycles are defined as a ratio between the setpoint stator voltage values and the rated phase voltage amplitude of the stator.

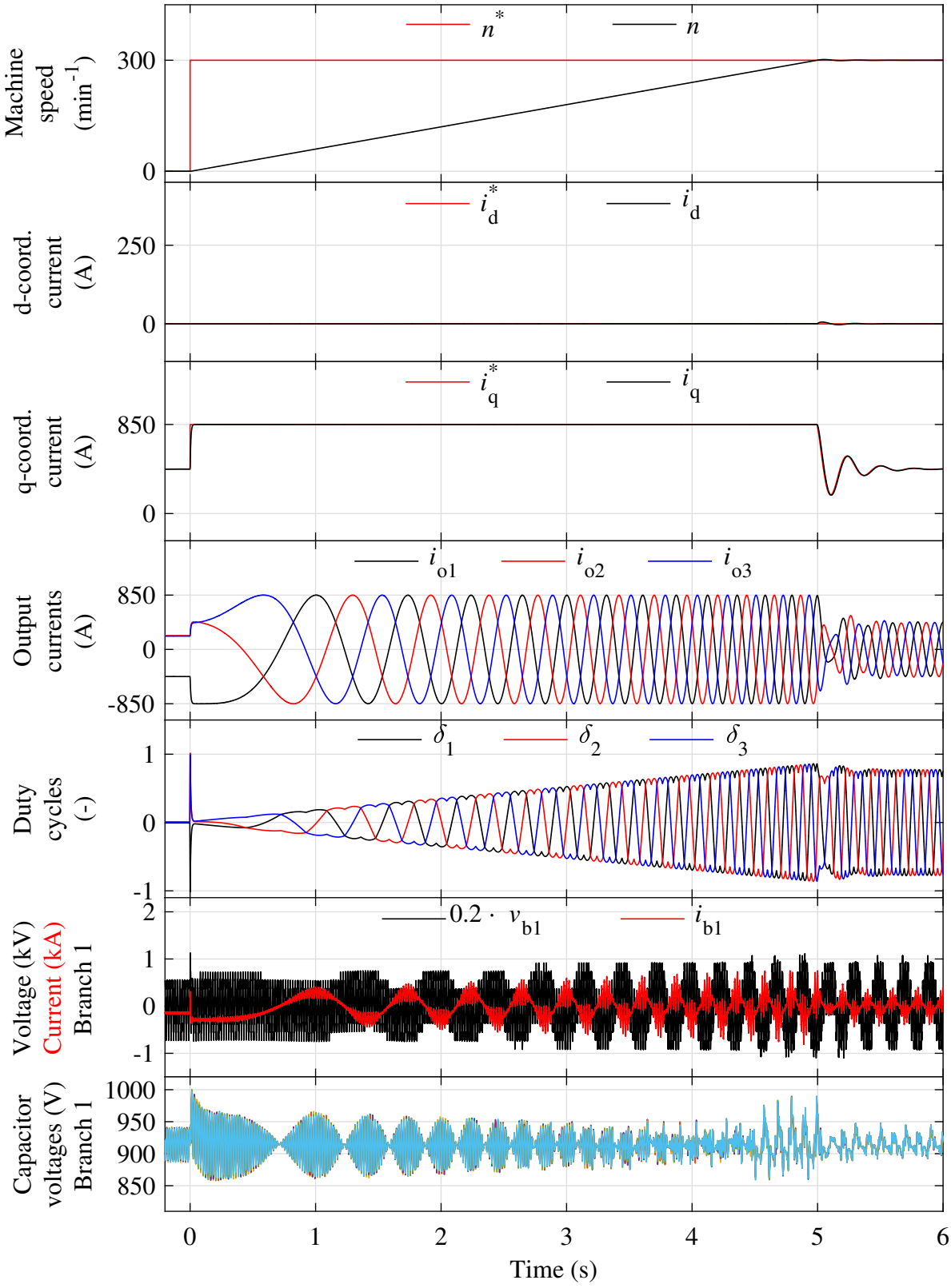


Figure F.12: Dynamic operation of the **MMMC** with a synchronous machine designed for study case **B**. The plotted duty cycles are defined as a ratio between the setpoint stator voltage values and the rated phase voltage amplitude of the stator.

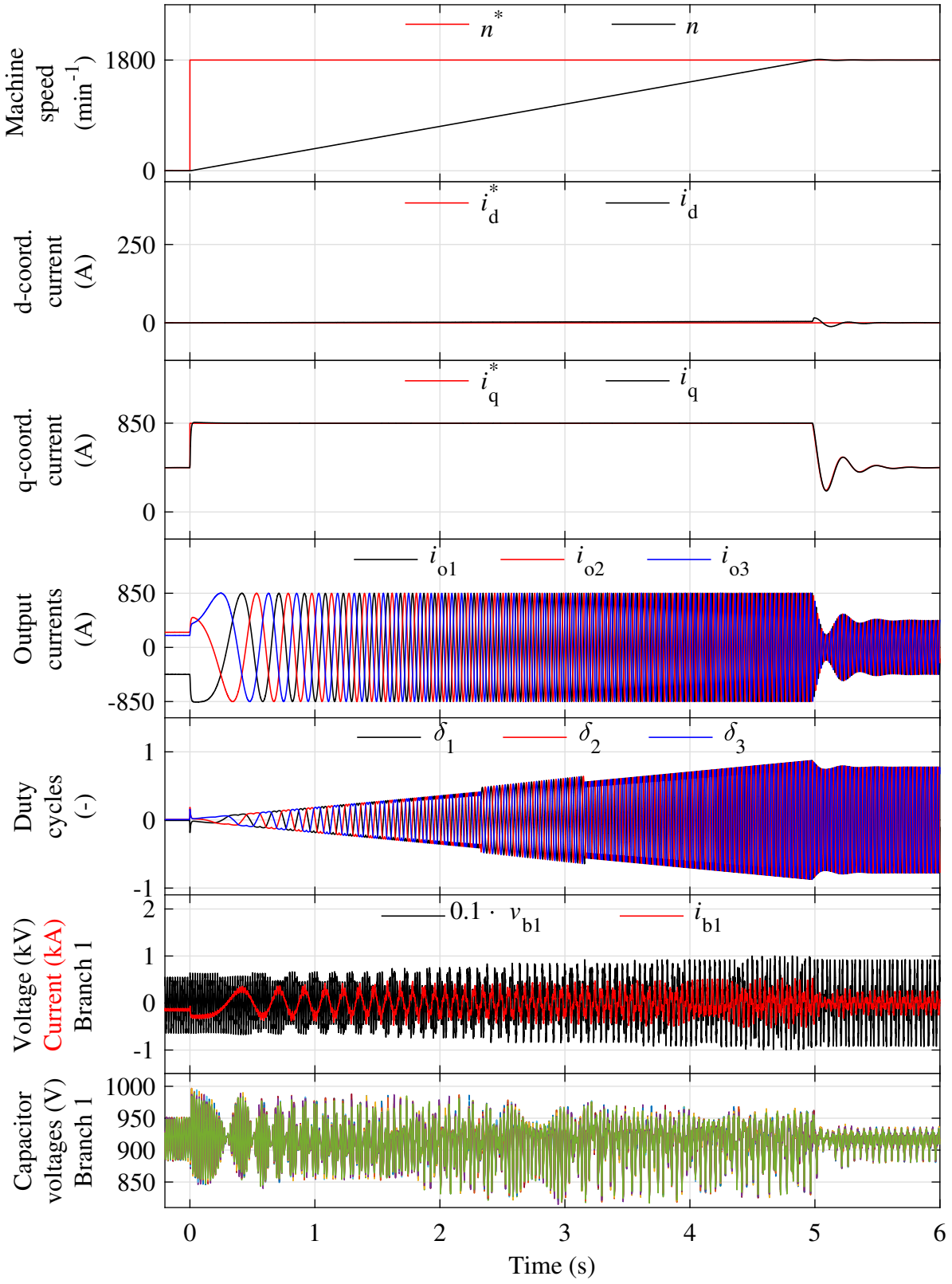


Figure F.13: Dynamic operation of the **MMMC** with a synchronous machine designed for study case **C**. The plotted duty cycles are defined as a ratio between the setpoint stator voltage values and the rated phase voltage amplitude of the stator.

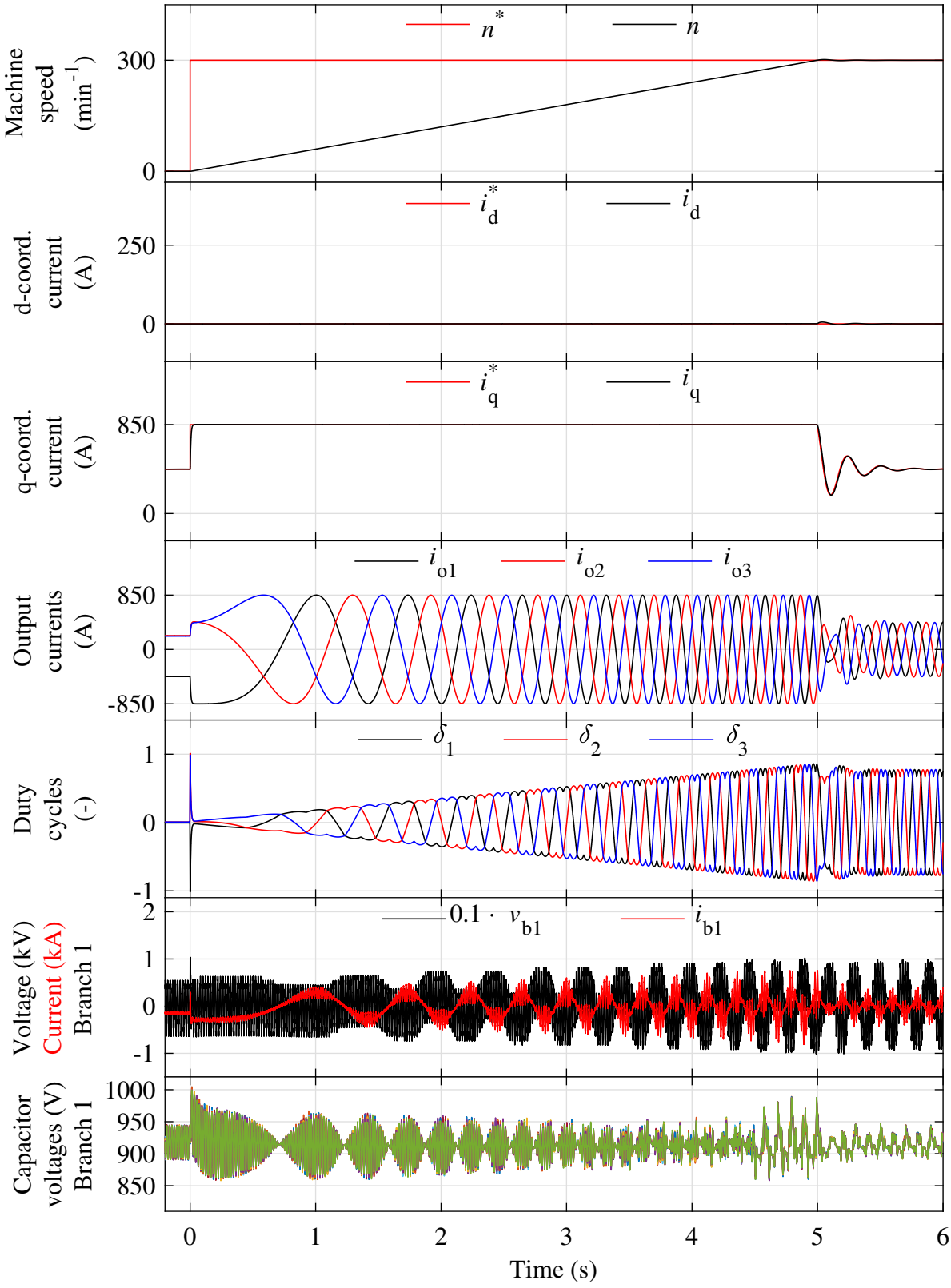


Figure F.14: Dynamic operation of the **MMMC** with a synchronous machine designed for study case **D**. The plotted duty cycles are defined as a ratio between the setpoint stator voltage values and the rated phase voltage amplitude of the stator.

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Curriculum Vitae

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Journal Publications

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2017 **J. Kucka, D. Karwatzki, and A. Mertens:** "Enhancing the Reliability of Modular Multilevel Converters Using Neutral Shift", *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 8953-8957.

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2018 **J. Kucka and A. Mertens:** "Improved Current Control of a Quasi-Two-Level PWM-Operated Modular Multilevel Converter", *Energy Conversion Congress and Exposition*, Portland (Oregon), USA.

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2016 **J. Kucka, D. Karwatzki, and A. Mertens:** "AC/AC Modular Multilevel Converters in Wind Energy Applications: Design Considerations", *European Conference on Power Electronics and Applications*, Karlsruhe, Germany.

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J. Kucka, D. Karwatzki, L. Baruschka, and A. Mertens: "Improved Modular Multilevel Converter Topology with Magnetically Coupled Branch Inductors", *Energy Conversion Congress and Exposition*, Montreal, Canada.

D. Karwatzki, L. Baruschka, J. Kucka, and A. Mertens: "Current Control and Branch Energy Balancing of the Modular Multilevel Converter", *Energy Conversion Congress and Exposition*, Montreal, Canada.

J. Kucka and L. Baruschka: "A Hybrid Modular Multilevel Converter", *European Conference on Power Electronics and Applications*, Geneva, Switzerland.

2014 **D. Karwatzki, L. Baruschka, J. Kucka, M. von Hofen, and A. Mertens:** "Improved Hexverter Topology with Magnetically Coupled Branch Inductors", *European Conference on Power Electronics and Applications*, Lapeenranta, Finland.

2012 **T. Haubert and J. Kucka:** "Design of Control for DC/DC Power Converter", *POSTER 2012 - 16th International Student Conference on Electrical Engineering*, Prague, Czech Republic.