

Electron and Hole Trap Signal with Similar Defect Parameters in Chalcopyrite Based Solar Cells

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Copper chalcopyrite based solar cells with different molar gallium to gallium plus indium ratio (GGI) are looked at, using deep level transient spectroscopy (DLTS) and admittance spectroscopy (AS). Depending on the respective measurement parameters, like reverse bias level, height and length of the voltage pulse applied, either a minority carrier or/and a majority carrier deep level signal is/are detected in the temperature range below 200 K. The AS investigations reveal only one trap signal. After a detailed description of the defect properties taking advantage of the two diode model, we discuss the origin of these trap signals in view of our experimental findings.

Key words: Thin Film Photovoltaic; Defect Spectroscopy.

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1. Introduction

At present, thin film solar cells based on Cu(In, Ga)Se₂ absorbers exhibit record efficiencies of almost 20% on laboratory cells and 13% on modules [1, 2]. The Cu chalcopyrite absorber has a molar gallium to gallium plus indium ratio (GGI) of about 0.28. However, in order to enlarge the band gap of the material by adding more gallium, the interest in the whole indium-gallium system has increased. In the present article, we report on the defect signal usually called N₁ or β in literature [3–6]. Although this trap signal has been subject to quite a number of reports, there is still a discussion about whether the defect is a minority or majority carrier trap, as different measurement techniques reveal contradictory results. In our own investigations, we applied deep level transient spectroscopy (DLTS) with variation of different measurement parameters and admittance spectroscopy (AS) to Cu(In,Ga)Se₂ based solar cells with different gallium content. We observed some remarkable properties of the N₁ signal that have, to our knowledge, not yet been reported. The article is structured as follows: First, we describe our experimental procedure and the samples used for investigation. Then, we present our experimental findings, which include several different parameter variation measurements concerning the

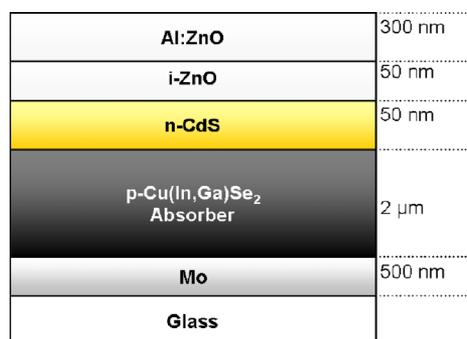


Fig. 1. Scheme of a Cu(In,Ga)Se₂ based heterostructure solar cell (thickness of the layers indicated on the right hand side).

DLTS like variation of the voltage pulse height, the reverse bias level or the voltage pulse length. In the subsequent discussion, we aim at forming some consistent picture of the N₁ defect based on our experiments in conjunction with information taken from the literature. In the conclusions, we summarize our main results and address some, as to our opinion, still open questions.

2. Experimental

The Cu chalcopyrite based solar cells investigated had a GGI of 0.00, 0.10, 0.28, 0.50, and 0.75. The exact preparation process is described in [7]. Figure 1 shows

a scheme of the solar cell. To these samples, we applied admittance spectroscopy (AS) and deep-level transient spectroscopy (DLTS) with variation of different measurement parameters [8, 9].

The device under test is stored in a cryostat cooled by a closed-cycle helium system, in order to probe a temperature range from 60 to 350 K. For the frequency and temperature dependent admittance measurements, we used a Hewlett-Packard 4914A and a Solartron 1260 impedance analyzer. The frequency was varied in the range from 100 Hz to 1 MHz, the amplitude of the alternating voltage kept at 30 mV. The resulting current was evaluated in terms of the complex admittance assuming a capacitor in parallel with a resistor as equivalent circuit [8].

We used a home built transient DLTS setup for the DLTS measurements. The system is based on a Boonton 7200 capacitance meter. The capacitance and conductance transients (equivalent circuit as in admittance spectroscopy), resulting from emission of charge carriers trapped during voltage pulse application, are stored by an analog-digital converter in conjunction with a personal computer. The transients were normalized to the respective equilibrium capacitance. Afterwards, they have been evaluated using the double-boxcar weighting function, in order to obtain the usual DLTS signal versus temperature graphs [10].

In the proceeding paragraphs, we will name the DLTS measurement parameters as follows: reverse bias U_R , height of the voltage pulse U_1 , and length of the filling pulse t_p .

3. Results

The majority carrier defect spectra (no injection of minority carriers; at maximum, a bias of 0 V is applied to the device during the whole measurement procedure) of Cu(In,Ga)Se₂ based solar cells can be divided into a low temperature part up to about 200 K and a high temperature part starting at about 280 K (Fig. 2). The latter usually exhibits two not well separated negative majority carrier defects, i. e., hole traps in our n⁺-p devices. Sometimes, we also find a positive minority carrier signal (electron defect signal) in this temperature range, but we do not want to go into detail concerning these defect signals. At temperatures below 200 K, we usually observe a majority carrier signal and/or a minority carrier signal depending on pulse parameters.

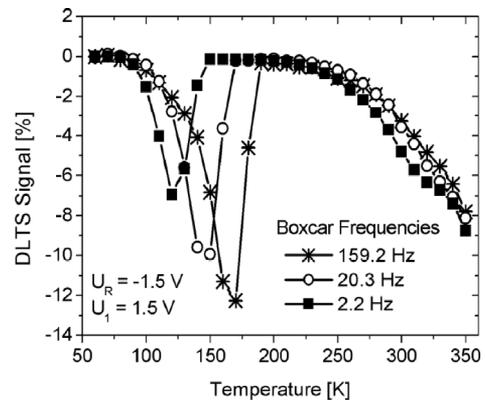


Fig. 2. DLTS signal versus temperature diagram of a Cu(In,Ga)Se₂ based solar cell with GGI = 0.50 for three different boxcar frequencies: 159.2 Hz (crosses), 20.3 Hz (open circles), 2.2 Hz (full squares). The measurement parameters are: $U_R = -1.5$ V, $U_1 = 1.5$ V, and $t_p = 1$ s.

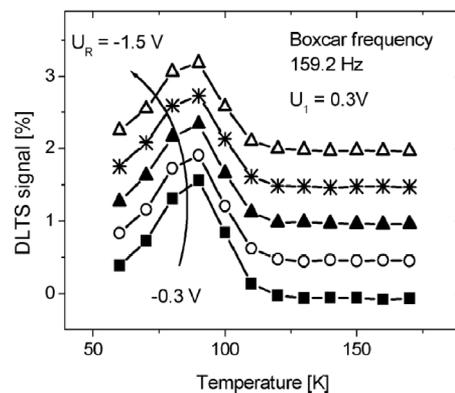


Fig. 3. DLTS signal versus temperature diagram of a Cu(In,Ga)Se₂ based solar cell with GGI = 0.10 under variation of the reverse bias from -0.30 V to -1.5 V ($\Delta U_R = 0.3$ V). The parameters $U_1 = 0.3$ V and $t_p = 1$ s were kept constant. The boxcar frequency was 159.2 Hz. The spectra were shifted for clarity.

The admittance measurements performed on these samples reveal only one defect signal that corresponds with the low temperature signals observed in DLTS (see Fig. 3).

In literature, most articles exclusively report the observation of the electron trap signal. There, it is often named N_1 or β [3, 4, 6]. A majority defect signal in about the same temperature range as the electron defect signal was only seldomly reported [11]. In the proceeding paragraphs, we will focus on these trap signals and present some DLTS parameter variation studies that reveal some interesting properties of these defect signals.

3.1. Variation of the Reverse Bias Voltage U_R

The variation of the reverse bias level U_R , while keeping the voltage pulse height U_1 fixed, is a method to determine concentration profiles of deep levels using DLTS [11]. Further on, we will call this kind of experiment U_R variation.

The results obtained from these measurements can be described as follows: irrespective of the level of reverse bias which was varied from -0.3 V to -1.5 V, we always detect a minority carrier signal as shown in Figure 3. We will name this electron trap signal E_1 . The amplitude of E_1 somewhat decreases with increasing reverse bias. The bias dependence probably results from a non-negligible edge region λ between the space charge region and the bulk which can lead to the aforementioned behaviour [12]. It should be noted that we applied a relatively small voltage pulse U_1 of 0.3 V. This will be important, if we compare the U_R variation to the measurement described in the next paragraph.

3.2. Variation of the Voltage Pulse Height U_1

Now, we vary the height of the voltage pulse, and the reverse bias level is kept fixed (called U_1 variation in the following). The latter provides an alternative technique to investigate defect concentration depth profiles [13]. Generally, the DLTS versus temperature spectra obtained at different heights of the voltage pulse show the following behaviour (see Fig. 4): If the voltage pulse applied remains relatively small, the positive signal E_1 is detected. With increasing pulse

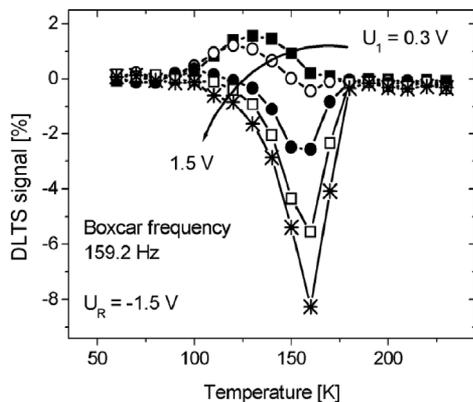


Fig. 4. DLTS signal versus temperature diagram of a Cu(In,Ga)Se₂ based solar cell with GGI = 0.50 under variation of the voltage pulse height U_1 from 0.3 V to 1.5 V ($\Delta U_1 = 0.3$ V). The parameters $U_R = -1.5$ V and $t_p = 1$ s were kept constant. The boxcar frequency was 159.2 Hz.

Table 1. Activation energies of the defect signals E_1 and H_1 determined by DLTS for different absorber compositions.

GGI	$E_a(E_1)$ [meV]	$E_a(H_1)$ [meV]
0.00	220–280	220–280
0.10	60–80	70–100
0.28	30–50	50–60
0.50	150–190	150–180
0.75	120–160	130–170

height, the minority carrier signal decreases, and a majority carrier signal starts to grow in at slightly higher temperatures (called H_1 in the following). This pulse height dependent sign change occurs within a relatively small range of voltage pulse heights, mostly a few tenths of millivolts.

We would like to emphasize that the phenomena described, in principle, are observed for samples of all GGI ratios investigated. However, for the solar cells with GGI equal to 0.28, the pulse height dependent sign change is often not completed for U_1 equal to 1.5 V. That means, besides signal H_1 , the defect signal E_1 can still be observed at this voltage pulse height, whereas for devices of other GGI, E_1 has vanished, and H_1 is exclusively detected.

The striking aspect of the defect parameters is that the values obtained for the minority and the majority carrier trap are quite similar. Some typical values of the activation energy E_a for the minority carrier signal (determined at U_1 equal to 0.3 V) and the majority carrier signal (at U_1 equal to 1.5 V) are listed in Table 1. The actual values of the activation energy should be taken as approximate ones, as sometimes the signals can be evaluated only in a narrow temperature range. As mentioned earlier, it has to be noted that the AS measurements performed on the respective samples reveal only one defect signal.

3.3. Variation of the Voltage Pulse Length t_p

In addition to the aforementioned variation measurements, we also changed the pulse length at a certain height of voltage pulse. (This method will be called t_p variation in the following).

A measurement with U_1 equal to 0.48 V shows Figure 5. For a short voltage pulse, the signal H_1 dominates the spectrum. With increasing pulse length, the negative signal decreases, and the positive signal E_1 comes into play. The latter finding will be called pulse length dependent sign change.

The general trend, i. e., a decrease in H_1 , respectively, an increase in E_1 with increasing pulse length

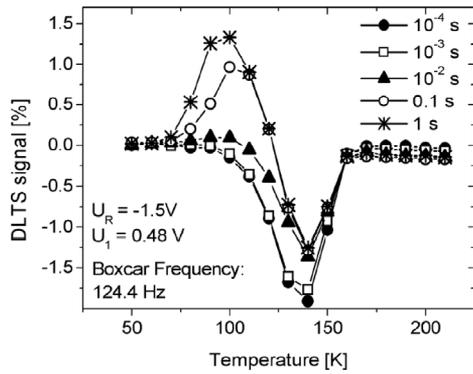


Fig. 5. DLTS signal versus temperature diagram of a Cu(In,Ga)Se₂ based solar cell with GGI = 0.10 under variation of the pulse length t_p from 10⁻⁴ s to 1 s. The parameters $U_R = -1.5$ V and $U_1 = 0.48$ V were kept constant. The boxcar frequency was 159.2 Hz.

is observed for all heights of the voltage pulse, even if the sign change does not occur (not shown).

3.4. Observation of the Voltage Pulse

In addition to the experiments described in the preceding sections, we monitored the changes in the sample capacitance not only after perturbation by the voltage pulse, but also during its application.

Moreover, we compared the temporal development of our conventional DLTS measurements with the device capacitance in the reverse bias DLTS mode (usually abbreviated RDLTS). In reverse DLTS, the reverse bias level abruptly increases during application of the voltage pulse, in order to empty the deep levels within the depletion region (we always refer to the absolute value of reverse bias). Therefore, after its application, one actually observes recapture of charge carriers instead of thermally activated emission as in conventional DLTS [14]. However, RDLTS and DLTS are not completely different measurement techniques. The only difference is that, because of the opposite direction of the voltage pulse applied, one observes the different processes at different times of the measurement sequence: increase in bias level takes place, for example, in RDLTS during the first part of the experiment, i. e., the actual application of the voltage pulse, whereas in conventional DLTS it is related to the second part of the experiment, i. e., the time interval after voltage pulse application.

Comparing the capacitive development during the whole voltage pulse sequence of a RDLTS measurement to the one observed in the conventional DLTS

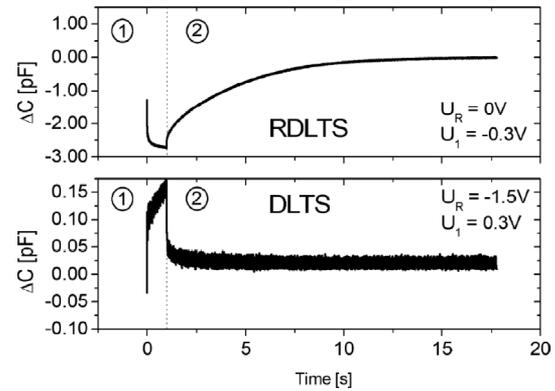


Fig. 6. Time development of the capacitance of a Cu(In,Ga)Se₂ based solar cell with GGI = 0.75 during and after application of a voltage pulse with small amplitude; upper diagram: RDLTS, lower one: DLTS. The parameters $U_R = -1.5$ V, $U_1 = 0.3$ V, and $t_p = 1$ s (DLTS) resp. $U_R = 0$ V, $U_1 = -0.3$ V, and $t_p = 1$ s (RDLTS) were kept constant. The temperature was 120 K.

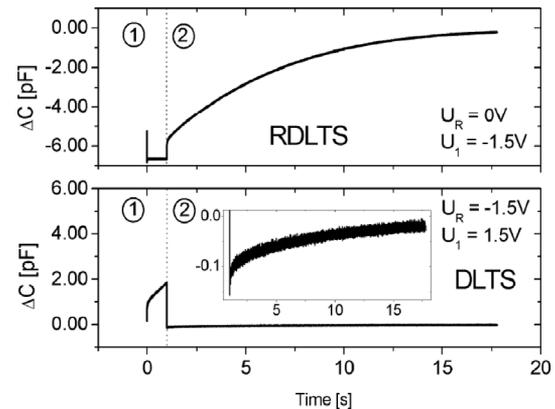


Fig. 7. Time development of the capacitance of a Cu(In,Ga)Se₂ based solar cell with GGI = 0.75 during and after application of a voltage pulse with large amplitude; upper diagram: RDLTS, lower one: DLTS. The parameters $U_R = -1.5$ V, $U_1 = 1.5$ V, and $t_p = 1$ s (DLTS) resp. $U_R = 0$ V, $U_1 = -1.5$ V, and $t_p = 1$ s (RDLTS) were kept constant. The temperature was 120 K.

experiment reveals that the changes correspond to each other. First, we look at the increase in reverse bias level. Here, two different cases can be discriminated: If the increase is small (see Fig. 6: RDLTS: part 1 of the experiment; DLTS: part 2 of the experiment), one observes a reduction of the capacitance which in classical DLTS/RDLTS interpretation corresponds to emission of minority carriers. If the increase in reverse bias is relatively large (see Fig. 7: RDLTS: part 1 of the experiment; DLTS: part 2 of the experiment), an increase in capacitance can be monitored which

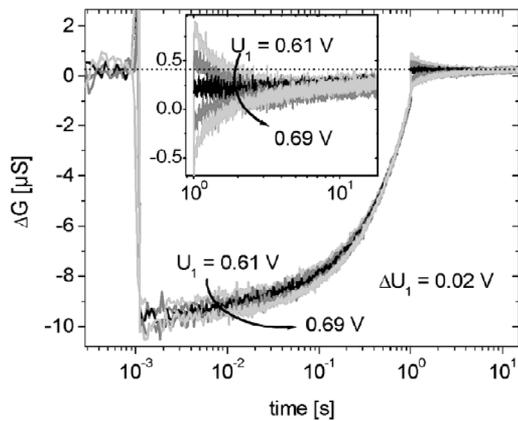


Fig. 8. Time dependent changes in conductance of a Cu(In,Ga)Se₂ based solar cell at 120 K with GGI = 0.50 before ($0 \text{ s} < 10^{-3} \text{ s}$), during ($10^{-3} \text{ s} \leq t \leq 1 \text{ s}$) and after ($t > 1 \text{ s}$) application of the voltage pulse. The voltage pulse height U_1 was varied from 0.61 V to 0.69 V ($\Delta U_1 = 0.02 \text{ V}$); the parameters $U_R = -1.5 \text{ V}$ and $t_p = 1 \text{ s}$ were kept constant. Note the unusual decrease in conductance ($\Delta G < 0 \mu\text{S}$) immediately after voltage pulse application (The overshoot at the beginning of the voltage pulse is due to the dead time of the capacitance/conductance bridge.).

would classically correspond to emission of majority carriers.

After reduction of the reverse bias level, one always detects an increase in capacitance (i. e., a capture of minority carriers) irrespective of the pulse height (see Figs. 6 and 7: RDLTS: part 2 of the experiment; DLTS: part 1 of the experiment).

In Figure 8, the time development before ($t < 10^{-3} \text{ s}$), during ($10^{-3} \text{ s} \leq t \leq 1 \text{ s}$), and after ($t > 1 \text{ s}$) application of the voltage pulse is displayed for a special case. Here, we show the changes in device conductance ΔG instead of ΔC , because the capacitance transients are affected by influences of a comparably large series resistance and, therefore, partly do not have the correct sign [15]. Before pulse application and long time afterwards, ΔG approaches the same level which indicates that the perturbation induced by the voltage pulse is reversible. (The deviation of this level from zero stems from imperfect balancing the sample's equilibrium conductance and the limited reading of this residual conductance offset.) Correspondingly to Figures 6 and 7, the conductance increases during the voltage pulse which usually indicated capture of minority carriers. After the voltage pulse, depending on its height, a positive or a negative transient is detected as described above. In contrast to Figures 6 and 7, an initial decrease in conductance upon reduction of the

reverse bias level can be observed. This behaviour is not explicable by a conventional single p-n junction. In fact, one expects an abrupt increase in conductance due to the reduced potential difference applied. The initial reduction in ΔG during pulse application is observed for positive and negative emission transients. As can be seen from Figure 8, the amplitude of ΔG stays negative and changes only slightly for the pulse height variation shown, whereas the sign change of the emission transient can be well observed. Therefore, no correlation between negative ΔG values during application of the voltage pulse and the sign change of the emission transient from positive to negative (with increasing voltage pulse height) becomes apparent.

4. Discussion

Considering the contradictory results from the two different defect concentration profiling techniques (U_R and U_1 variation), the interpretation as concentration gradients of two independent deep levels with opposite sign seems to be not valid. The t_p variation confirms this interpretation, as for independent defect levels no decrease in signal amplitude with increasing pulse length is expected, as observed for the negative signal H_1 . Moreover, the quite similar trap parameters obtained for the positive and the negative signal – if evaluated as deep levels – give the impression that both might stem from the same origin that, for some reason, exhibits a sign change. But how can a sign change of a DLTS signal be explained? One option that, in principle, has the potential to induce an inversion of the original signal direction is a misfit of the applied equivalent circuit [15]. We performed several plausibility checks of the equivalent circuit, a capacitor in parallel to a resistor, connecting an additional resistor in series to the device under test. However, these tests demonstrate that the observed sign change is definitely not induced by a non-negligible series resistance [16]. Moreover, as indicated in the preceding section, we compared the capacitance and conductance transients for the experiments shown in Figures 6 to 8 and, if necessary, took the data for ΔG instead of ΔC to evaluate our measurements.

Considering the other experimental findings presented, specially the investigations on the temporal development of the capacitance and the conductance, respectively, reveal some peculiar aspects: Whereas the capacitive response for small voltage pulses (see Fig. 6) is consistent with a minority carrier trap, the

RDLTS and DLTS experiments with large voltage pulses demonstrate that the capacitance during and after application of the voltage pulse change in the same direction which is not explicable by a simple, reversible capture-emission process.

The latter results are consistent with the experimental findings from Igalson *et al.* [17] on Cu(In,Ga)Se₂ solar cells: They reported about a minority trap signal in RDLTS and a majority defect signal in DLTS after annealing in the dark. As explanation, they propose that the defect is actually a minority carrier trap which in RDLTS exhibits the classical emission-capture process. However, in DLTS, they assume a somewhat different behaviour of this defect: During application of the voltage pulse, some traps occupied by electrons might capture holes. After the pulse, thermal emission of these holes to the valence band does not happen because of the large energy required. The traps occupied by holes do capture electrons instead which causes the negative transient majority trap signal in DLTS [17]. However, our monitored transients do not show any substantial difference between the capacitive response in RDLTS and DLTS mode. The data could not reveal two different processes during increase of the reverse bias level, either.

Even more questions arise from the time development of conductance shown in Figure 8, where ΔG abruptly falls to values smaller than the equilibrium conductance at $U_R = -1.5$ V upon application of the voltage pulse and then increases steadily during the filling process. This behaviour is not consistent with the instantaneous decrease in the width of the space charge region upon reduction of the potential difference applied to the device under test.

To account for all these aforementioned experimental results, including the different ways of temporal development of the capacitance or conductance detected, we propose an extra series capacitor to be present that causes a sign inversion of the defect signal under certain measurement conditions. We think it arises from the presumably existent space charge region at the back contact that comes into play only at lower temperatures. It could be either a Schottky barrier at the molybdenum back contact of the device or an addi-

tional p-n junction located between the Cu(In,Ga)Se₂ and a MoSe₂ layer that develops during deposition of the absorber on the metal contact [18]. We assumed a model of two capacitors connected in series where each induces a capacitance transient that contributes to the resulting measurement signal. Both transients have the same time constants, but opposite sign. Within such a simple model, the pulse height dependent sign change can only be achieved if both contributions from the front and the back contact diode to the total change in capacitance are of the same order of magnitude. Although the latter consequence is somewhat restrictive to our model, the different temporal developments of the capacitance presented can, in principle, be obtained. To explain the abrupt decrease in conductance shown in Figure 8, transient currents have presumably to be taken into account. However, detailed time dependent simulations are necessary to verify our model in detail, but this would exceed the scope of this article. Within the two diode model, the correct sign of the trap has to be negative, i. e., the defect is a majority carrier trap.

5. Conclusions

We disclose in our DLTS measurements either a minority carrier or a majority carrier signal, depending on the respective measurement parameters applied, like height or length of the voltage pulse. These findings cannot be explained by a defect concentration profile of two independent deep levels. As possible mechanism, we propose a measurement parameter dependent sign change of a majority carrier trap signal due to the influence of an additional space charge region at the Mo back contact to explain the experimental findings.

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