Compact, low-noise current drivers for Quantum Sensors with Atom Chips

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Zusammenfassung

Quantensensoren auf Basis der Atominterferometrie entwickeln sich zu geschätzen Werkzeugen für Präzisionsmessungen in verschiedenen Forschungsbereichen, wie Metrologie, Geowissenschaften und Inertialsensorik. Die Verifikation ihrer Genauigkeit ist jedoch an die Auflösung und somit die Freifallzeit des Interferometers gekoppelt, welche auf der Erde nur durch Levtiation oder andere Methoden verlängert werden kann. Diese Verfahren bringen aber zumeist einen Verlust an Genauigkeit mit sich. Speziell im Bereich der Grundlagenforschung sind weltraumgestützte Messapparaturen daher eine faszinierende Perspektive, um neue Maßstäbe für fundamentale Tests und Messungen in der Erdbeobachtung zu setzen. Im Weltraum ist es möglich, die Messapparaturen beliebig lang mit ihren Testobjekten mitfallen zu lassen, was eine erhebliche Verlängerung der Interferometriedauer ermöglicht. Eine wichtige Voraussetzung für Interferometrie auf derart langen Zeitskalen ist die Minimierung der Ausbreitungsgeschwindigkeit und initialen Ausdehnung, welche nur mit ultra-kalten atomaren Ensembles, wie einem BOSE-EINSTEIN-Kondensat (BEK), zu erreichen ist. Die Erzeugung eines solchen BEK auf einer kompakten, weltraumgestützten Plattform stellt daher eine zentrale Herausforderung für die Realisierbarkeit von Atominterferometern im Weltraum dar.

Einen wichtigen Schritt für die notwendige Adaption existierender Laborapparaturen hin zu Weltraumplattformen stellt die Höhenforschungsraketenmission MAIUS-1 dar, welche sowohl die Technologie als auch die Methodik für den Einsatz von Quantensensoren im Weltall entwickeln und erproben soll. Das Kernstück der wissenschaftlichen Nutzlast von MAIUS-1 ist eine ultra-kompakte kalte Atomquelle, basierend auf der Atomchip-Technologie zur Erzeugung von BEK in Magnetfallen. Die präzise Magnetfeldkontrolle mit diesen Atomchips, in einer Umgebung wie die einer Höhenforschungsrakete, erfordert spezialisierte Stromtreiber, die Robustheit, Kompaktheit und exzellente Rauschleistung vereinen, welche mit kommerzieller Technologie bisher nicht zu erreichen sind.

In dieser Arbeit werden Design und Charakterisierung einer neuen Generation von kompakten Stromtreibern für diese Aufgabe vorgestellt. Anhand einer typischen Präparation eines BEK werden Kernspezifikationen für Stromtreiber abgeleitet und deren Auswirkungen auf das Experiment erläutert. Anschließend werden diese Spezifikationen durch die technischen Anforderungen einer Höhenforschungsrakete ergänzt.

Die Evaluation des Anforderungskatalogs resultiert in drei Stromtreiber-Designs. Zunächst wird ein analoger, flexibler Prototyp vorgestellt, der neben der Demonstration von Miniaturisierung und hohen Leistungsdichten viele Einstellmöglichkeiten von Regelparametern ermöglicht und in der Evaluierungsphase der MAIUS-1 Atomchipsektion eingesetzt wurde. Die Erfahungen aus dieser Phase flossen in die Designs der MAIUS Flughardware, welche zwei an die technischen Gegebenheiten angepasste Architekturen bieten: Zum einen für den Einsatz an Atomchips und zum anderen für die externen Spulen um den Chip herum.

Der Designprozess wurde durch detaillierte Simulationen der Schaltkreise unterstützt. Sie ermöglichen eine schnelle Optimierung von Kontrollarchitektur und -parametern für beliebige Lasten. Besonders bei den Spulen, die für die magnetischen Fallen von entscheidender Bedeutung sind, stellt die gewonnene Vorhersagequalität für das Schaltverhalten einen großen technologischen Vorteil dar, da Vorgängerexperimente hier bisher auf heuristische Verfahren zur Optimierung angewiesen waren.

Mit einer Verkleinerung des Volumens von mehr als einer Größenordnung gegenüber Laborelektronik, und Ausgangsströmen von bis zu 10 A, sind die aktuellen Treibermodule von MAIUS unter harten Temperaturbedingungen von 10 bis 70 °C einsetzbar. Hierbei weisen sie einen Temperaturdrift von 100 ppm/K (Chip) bzw. 32 ppm/K (Spulen) auf. Im thermischen Gleichgewicht arbeiten die Treiber mit einer relativen Stromstabilität von $3\cdot10^{-5}$ (Chip) und $5\cdot10^{-6}$ (Spulen).

Technisches Stromrauschen stellt eine entscheidende Limitierung der Lebensdauern in magnetischen Atomchipfallen dar. Die Rauscheigenschaften der erstellten Designs werden daher in einer Spektralanalyse evaluiert und mit kommerziellen Laborgeräten von Vorgängerexperimenten verglichen. Die hierbei ermittelten Werte für integriertes Stromrauschen von $108\,\mu A_{RMS}$ (Chip) und $64\,\mu A_{RMS}$ (Spulen) (1Hz-99.8 kHz), stellen eine Verbesserung um Faktor 3.8, bzw. 6.4 im Vergleich zur kommerziellen Referenz dar.

Zum Abschluss der ersten Charakterisierung der entwickelten Designs vor dem Raketenstart von MAIUS werden erste Betriebsmessungen der integrieten Quelle kalter Atome vorgestellt und in Hinsicht auf die Temperaturdrift der Stromtreibermodule im Experiment ausgewertet.

Die erreichten Leistungswerte setzen einen neue Referenz im Bereich der Kompaktifizierung und Rauschleistung und liefern somit eine Schlüsseltechnologie für kompakte, auf Atomchips basierende Quantensensoren. Die vorgestellten Designs operierten erfolgreich auf der MAIUS-1 Mission, welche am 23. Januar 2017 u.a. die erste Erzeugung eines BEK im Weltraum demonstrieren konnte.

Schlüsselwörter: Stromregelung, Atomchips, Bose-Einstein Kondensat

Abstract

Quantum sensors based on atomic interferometry are becoming valued tools for precision measurements in various research areas such as metrology, Earth sciences and inertial sensors. However, the verification of their accuracy is linked to the resolution and thus the free-fall time of the interferometer, which can only be extended on Earth by levitation or other methods, which themselves usually result in a loss of accuracy. Especially in the field of basic research, space-based measurement apparatuses are therefore fascinating prospects to set new standards for fundamental tests and measurements in Earth observation. In space, it is possible to drop the measuring devices alongside their test objects as long as desired, which allows a considerable extension of interferometry time. An important prerequisite for interferometry on such long time scales is the minimization of propagation velocity and initial expansion, which can only be achieved with ultra-cold atomic ensembles such as a BOSE-EINSTEIN condensate (BEC). Therefore, the creation of such a BEC on a compact, space-based platform represents a central challenge for the feasibility of atom interferometers in space.

An important step for the necessary adaptation of existing laboratory equipment to space platforms is the sounding rocket mission MAIUS-1, which is to develop and test both technology and methodology for the use of quantum sensors in space. The core of the scientific payload of MAIUS-1 is an ultra-compact cold atomic source, based on the atom chip technology, employed to generate BEC in magnetic traps. The precise magnetic field control with atomic chips, in an environment like that of a sounding rocket, requires specialized current drivers that combine ruggedness, compactness and excellent noise performance that is yet unattainable with commercial technology.

This thesis presents design and characterization of a new generation of compact current drivers for this purpose. Based on a typical preparation of a BEC, core specifications for current drivers are derived and their effects on the experiment are discussed. These specifications are then supplemented by the technical requirements of a sounding rocket.

The evaluation of the requirements catalogue results in three current driver designs. First of all, an analog, flexible prototype is presented, which, in addition to the demonstration of miniaturization and high power densities, allows many possible settings of control parameters and has been used in the evaluation phase of the MAIUS-1 atomic chip section. The experiences from this phase flowed into the designs of the MAIUS flight hardware, which offer two architectures, adapted to the given technical conditions: one model for the employment at atom chips and one model to drive the external coils around the atom chip.

The design process was supported by detailed circuit simulation. They enable fast optimization of control architecture and parameters for any load. Particularly in the case of coils, which are of crucial importance for magnetic traps, the prediction quality obtained represents a major technological advantage in terms of optimizing switching behavior, since predecessor experiments previously depended on heuristic methods for this task.

With a volume reduction of more than one order of magnitude compared to laboratory electronics, and output currents of up to 10 A, the current driver modules of MAIUS can be used under harsh temperature conditions from 10 to 70 °C. They show a temperature drift of 100 ppm/K (chip) or 32 ppm/K (coils). In thermal equilibrium, the drivers work with a relative current stability of $3 \cdot 10^{-5}$ (chip) and $5 \cdot 10^{-6}$ (coils).

Technical current noise is a decisive limitation of the lifetimes in magnetic atom traps. Thus, the noise characteristics of the designs are evaluated in a spectral analysis and compared with commercial laboratory equipment from previous experiments. The thereby obtained values for the integrated current noise of $108\,\mu A_{RMS}$ (Chip) and $64\,\mu A_{RMS}$ (Coils) (1Hz-99.8 kHz), represent an improvement by a factor of 3.8, or 6.4 in comparison to the commercial reference.

To conclude the first characterization of the developed designs before the launch of MAIUS the first operational measurements of the integrated source of cold atoms are presented and evaluated in view of temperature drift of the current driver modules in the experiment.

The achieved performance values set a new benchmark in the field of compactification and noise performance and thus provide a key technology for compact, atomic chip-based quantum sensors. The presented designs operated successfully on the MAIUS-1 mission which on January 23rd, 2017, among other things, could demonstrate the first creation of a BEC in space.

Keywords: current control, atom chips, BOSE-EINSTEIN condensate

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Acronyms

AC	alternating current.
ADC	analog-digital converter.
AlN	Aluminum nitride.
ARP	Adiabatic Rapid Passage.
AWG	American Wire Gauge.
BCCD	bipolar coil current driver.
BEC	BOSE-EINSTEIN condensate.
BECCAL	BOSE-EINSTEIN condensate cold atom laboratory.
BJT	bipolar junction transistors.
BLT	bridge-tied load.
CPLD	complex programmable logic device.
DAC	digital-analog converter.
DC	direct current.
DFT	discrete FOURIER-transform.
DKC	delta-kick collimation. *see also* DKC
DLL	dynamic link library.
DLR	germ.: *Deutsches Zentrum für Luft- und Raumfahrt* (German Aerospace Center).
DLR-SC	germ.: *Deutsches Zentrum für Luft-und Raumfahrt, Einrichtung Simulations- und Softwaretechnik*, German Aerospace Center, Division Simulation and Software Technology.
FPGA	field-programmable gate-array.
FSM	finite state machine.
GPE	GROSS-PITAEVSKII-equation.
GRT	the theory of General Relativity.
GUI	graphical user interface.
IC	integrated circuit.
IPOL	isolated point-of-load.
IPT	IOFFE-PRITCHARD-trap.
LASUS	germ.: *Lasersysteme unter Schwerelosigkeit* (laser systems in microgravity). *see also* LASUS
$LiFePO_4$	Lithium ferrophosphate.
LSD	linear spectral density.
MAIUS	germ: *Materiewelleninterferometer unter Schwerelosigkeit* matter-wave interferometer in weightlessness. *see also* MAIUS
MLCD	MAIUS lab-based current driver.

MOPA	master oscillator power amplifier.
MOSFET	metal-oxide-semiconductor field-effect transistor.
MOT	magneto-optical trap.
NASA	National Aeronautics and Space Administration.
NTC	negative thermal coefficient thermistor.
PCB	printed circuit board.
PID	proportional integral differential controller.
ppm	part-per-million.
PSD	power spectral density.
PWM	pulse-width modulation.
QUANTUS	germ.:*Quantengase unter Schwerelosigkeit* (quantum gases in microgravity). *see also* QUANTUS
QUANTUS-1	The QUANTUS-1 experimental apparatus. *see also* QUANTUS-1
QUANTUS-2	The QUANTUS-2 experimental apparatus. *see also* QUANTUS-2
RF	radio frequency.
SMD	surface mount device.
SPICE	*simulation program with integrated circuit emphasis. see also* SPICE
SSR	solid-state relay.
TBUS	*Thijs' Binary Unit System.* 96, *see also* TBUS
UCCD	unipolar chip current driver.
UFF	universality of free fall.
WLAN	wireless local area network.
ZARM	center of applied space technology and microgravity (germ.: *Zentrum für angewandte Raumfahrttechnologie und Mikrogravitation*).

Glossary

DKC

Delta-kick collimation, often misleadingly referred to as *delta-kick cooling* is a technique of magnetic manipulation of an atomic cloud in order to reduce residual expansion velocity. By using an analogy to the focus effect of a lens in optics, sometimes the term *magnetic lensing* is used, although the technique does not necessarily rely exclusively on magnetic fields. With DKC, the expansion velocity of a ^{87}Rb BOSE-EINSTEIN condensate can be reduced down to a corresponding temperature of roughly 50 pK in three dimensions. The efficiency and application of DKC is an ongoing topic in BOSE-EINSTEIN condensate research, as the most beneficial schematics are expected to be only possible in microgravity.

integral windup

Integral windup describes the behavior of an output-limited controller to saturate, if the change of error signal is too high or remains too long at a certain value. This results in an accumulated integrated error signal which then causes the controlled signal to overshoot.

LASUS

The collaboration LASUS is a german acronym, translated to »laser systems under microgravity« and is funded as a collaboration project of several Universities by the german space agency DLR with funds of the Ministry of Commerce and Energy.

MAIUS

The term MAIUS is a German acronym, translated to »matter-wave interferometry in migrogravity«, a sounding rocket mission consisting of the apparatuses MAIUS-A and MAIUS-B, executing three consecutive missions (MAIUS-1, MAIUS-2, MAIUS-3) investigating BEC in space and dual species interferometry.

MAIUS-1

The mission MAIUS-1 was a sounding rocket mission to create and investigate BOSE-EINSTEIN-condensates in space. Simultaneously it was the testbed of the current driver designs introduced in this work. With its successful launch on January, 23$^{\mathrm{rd}}$ of 2017, the experiment could create the first man-made BOSE-EINSTEIN condensate in space, using ^{87}Rb atoms.

mu-metal

mu-metal, or µ-metal is a nickel/iron/molybdenum alloy which has a very high magnetic permeability. Along with additional features like low anisotropy and fast saturation, it is the ideal choice as a shield material against static magnetic fields. Its use is essential to create distortion free environments for magnetic manipulation of cold atoms.

QUANTUS

The collaboration QUANTUS is a german acronym, translated to »quantum gases in microgravity«. It unifies national and international efforts of scientific research on quantum optics in microgravity and space, and is funded by the german space agency DLR with funds of the Ministry of Commerce and Energy.

QUANTUS-1

The droptower apparatus QUANTUS-1. It is a hybrid experiment of one-layer atom chip and classical MOT. It has been employed to achieve the first BOSE-EINSTEIN-condensate and atom interferometry in microgravity.

QUANTUS-2

The droptower apparatus QUANTUS-2. It can employ catapult and drop mode of the droptower. Its long-term mission goal: dual-species atom interferometry with ^{87}Rb and ^{41}K to test the weak equivalence principle.

SPICE

The software SPICE (*simulation program with integrated circuit emphasis*) is a software suite to model the behavior of integrated circuits using simple means of numeric mathematics. It has been introduced in 1973 and is, with several graphical user interfaces and additions by circuit distributors, the quasi standard for simple circuit simulation and thus a crucial part of the design phase.

TBUS

The TBUS, named after it's developer Thijs Wendrich, is employed for the electronic communication in all LASUS-related experiments, and as such especially in QUANTUS-2 and MAIUS.

Symbols

β	parameter to represent the relation of NTC resistance and temperature.
$\delta(\lvert\omega\rvert)$	skin depth of a substrate with specific resistance ρ, explictly: $\delta\lvert\omega\rvert = \sqrt{\frac{\rho}{\mu_0\omega}}$.
ε	energy.
η	the EÖTVÖS ratio of the acceleration of two test masses m_1 and m_2: $\eta = 2 \cdot \left\lvert\frac{a_1 - a_2}{a_1 + a_2}\right\rvert$.
$\mathcal{G}$	gain curve of the magnetic coils.
Γ	inverse lifetime of an atomic or trap state.
h	PLANCK's constant.
$\hbar$	reduced PLANCK's constant, $\hbar = \frac{h}{2\pi}$.
$\mathcal{I}$	current noise spectral density function.
$\vec{j}$	electrical current density.
k_B	BOLTZMANN's constant.
Λ	phase-space density.
Δ	the LAPLACE-operator.
m_e	mass of the electron.
μ	chemical potential.
μ_B	BOHR's magneton, $\mu_b = \hbar \cdot \frac{q}{2m_e}$.
μ_0	the magnetic constant, represents the permeability of free space.
μ_r	magnetic constant of a medium.
ν	frequency.
ω	angular frequency ($\omega = 2\pi\nu$).
ρ	specific resistance of a medium.
$\varsigma^2(N, T, \tau)$	N-Sample variance.
ω_B	trap bottom frequency, $V_\mathrm{trap}(\vec{r}_d)/\hbar$.
ω_D	trap depth.
ω_L	LARMOR-frequency.
ω_T	trap frequency; either individual frequencies for each dimension or their geometrical mean.
π	ARCHIMED's constant. The relation of circumference and diameter of a circle.
q	elementary charge.
$\mathfrak{F}(x)$	substitution function for biasing ALLAN-Variances.
$\mathcal{R}(t)$	controller signal in a PID.
R_0	resistance of a NTC at it's reference temperature.
$\vec{r}_d$	position vector of the trap minimum, $\lvert\vec{r}_d\rvert = d$.
$S(\omega)$	power spectral density.
ϑ	absolute temperature.
ϑ_0	temperature of a NTC at it's reference resistance.
U_S	supply voltage of current driver.
ζ	RIEMANN's zeta-function $\zeta(s) := \sum_{n=1}^{\infty} \frac{1}{n^s}$, $s = \sigma + it \in \mathbb{C}$, $\Re(\sigma) > 1$.

CHAPTER 1

Introduction

Measurements are the very foundation of our physical model of the world. They rely on a well-devised measurement setup, meticulous execution and, most imperatively, sophisticated and precise sensors. In applied sciences, optical interferometers are one of the most versatile, yet highly sensitive devices to perform precision measurements. Among many other applications, they are utilized in fundamental research [1], Earth Science [2] and many industrial applications as a gold standard for measurements of length, rotation and acceleration in various fields of interest.

In recent years, quantum sensors based on atom interferometry [3] have treaded their path into a variety of applications in numerous fields of scientific research. Merging light and matter-wave optics, they utilize the quantum wave nature of solid particles [4], manipulated with suitable matter-wave optical elements, e.g. laser pulses [5]. Although quantum sensors are yet in their early stages of development, they already prove to be worthy alternatives or even successors for classical sensors, for example in the fields of metrology [6] and as inertial sensors [7, 8].

The sensitivity and contrast of atom interferometers depend predominantly on the possible free evolution of the coherently split atomic ensemble, which is coupled to the available free falling time. Although it is possible to extend the free evolution through techniques like e.g. levitation, the accuracy of the interferometric measurements is usually limited by uncertainties of these methods. Optimal properties of atomic ensembles for interferometry include controlled, very low momentum width to allow a long coherence length of the wave packets [9], and a high atom number for good contrast in measurements. However, achieving these properties simultaneously with a satisfactory repetition rate usually demands for large, complicated experimental apparatuses. Additionally, the gravitational potential on Earth does not only impair the preparation quality, but also bends the core trajectories of the interferometer paths. Since atom interferometry has to be performed under high vacuum conditions, in order to suppress decoherence due to collisions with background gases, the achievable free-falling time and hence the sensitivity of interferometers is constrained by the technical and financial availability of large-scale vacuum vessels.

As a logical development, applications of quantum sensors in space have become an appealing goal, with possible benefit for geodesy [10] and tests of fundamental physical concepts [11]. There, the complete measurement apparatus can be kept in free-fall alongside with the test objects, thus not impairing the achievable precision. The sensitivity of measurements on a long-term satellite mission is expected to be at least one order of magnitude better than the current measurements [12, 13]. However, the way to space is paved with harsh technical requirements, such as mass budgets, volume restrictions, and power limitations [14]. Hence, the realization of very compact, high-yield and high-flux sources of cold atoms presents a technological bottleneck, not only to space, but also to many other applications, such as portable and affordable measurement devices.

Atom chips [15] offer an excellent approach to overcome these challenges: Micro-structures in close proximity to the atomic ensembles are able to create strong, highly customizable, magnetic confinement fields which lead to efficient atomic sources with very small power consumption. The close proximity of the chip to the atomic ensemble, alongside with technical noise limits the lifetime in the magnetic trap [16]. Thus, current sources for these chips underly very strict requirements for noise and switching performance, which cannot be easily met by standard laboratory equipment. Today, there are a few commercial solutions [17, 18], which perform satisfactorily in laboratory experiments. Unfortunately, there are yet no commercial products complying with the unique requirements of compact, robust and portable atom chip setups, which are needed for precision atom interferometry in space.

Especially in the context of sounding rocket missions, the overall current output, volume restrictions, and interface requirements cannot be jointly met by any of the commercially available solutions. Thus, customized current driver designs are an imperative task to realize an atom interferometer in space. In this work, we will focus on function, design, development, and characterization of these current drivers, especially suitable for sounding rocket microgravity missions, which are exposed to one of the roughest environments for quantum sensors in the field.

Before introducing the structure of this thesis, we will shortly glance at some of the basic scientific concepts this work orchestrates, along with a brief historical wrap-up of the *Quantum Gases in Microgravity* (QUANTUS) project, which is the overall endeavor giving the whole thesis its higher purpose.

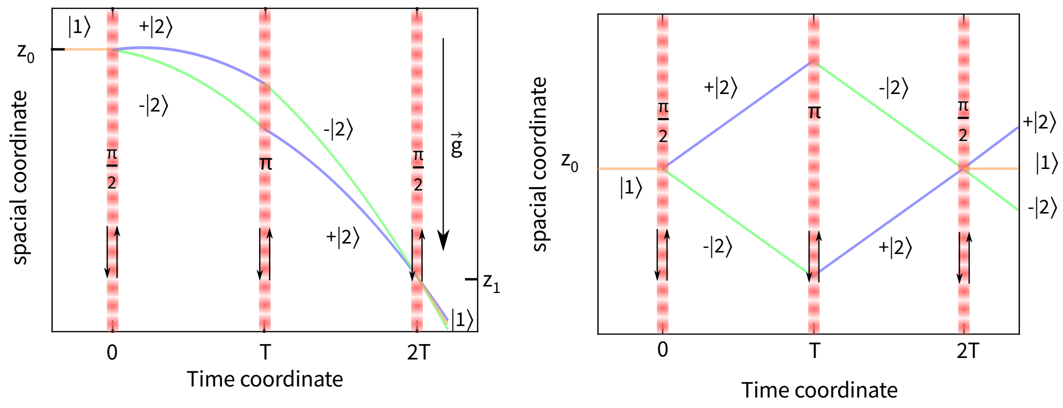
Atom interferometry

Without exception, the atom interferometers which are considered in this thesis use the interaction between matter-waves and light pulses to achieve a coherent manipulation of the interferometry states. Hereby, the incoming wave packet of the interferometer is considered to be a three-level quantum system ($|1\rangle$,$+|2\rangle$,$-|2\rangle$), which can experience RABI-oscillations driven by the laser pulses of the light gratings. As an example of the application of these pulses, we will consider a geometry which is planned to be used in the MAIUS missions, the symmetrical MACH-ZEHNDER-type configuration (figure 1.1). It features a scheme of three interaction pulses with separation time T. The duration of the pulses can be modulated to control the population transfer into the two states. In our case, the mechanism of BRAGG-scattering on standing light waves is used to drive the RABI-transitions between momentum states of the atoms. For the symmetrical MACH-ZEHNDER-configuration, two pairs of counter-propagating laser beams are employed to transfer the incoming state $|1\rangle$ into a superposition of two opposite non-zero momentum ($\pm|2\rangle$) states [19].

In (figure 1.1a), the atomic ensemble, described by a wave packet $|1\rangle$, is interacting with laser light, which changes the external momentum state of the input. By varying the duration of the interaction, one can create a $\pi/2$ pulse, projecting the input into a $50:50$ superposition of the $|+2\rangle$ and $|-2\rangle$ state, similar to an optical beam-splitter. Additionally, a π pulse provides a momentum inversion in each arm of the interferometer, resembling the function of a mirror in an optical setup. The evaluation of the state population after the paths are overlapped again in a second $\pi/2$ pulse, gives rise to a phase difference $\Delta\Phi$, yielding a first order relation of [20]:

$$\Delta\Phi = \vec{k}_{\mathrm{eff}}\,\vec{g}\,T^2\,, \tag{1.1}$$

depending on the gravitational acceleration $\vec{g}$, the pulse separation time T and the relative kinetic momentum between the interferometer arms $\vec{k}_{\mathrm{eff}}$. It is evident from equation 1.1, that longer separation times T between pulses are increasing the phase shift, thus allowing for



a) symmetrical MACH-ZEHNDER interferometer with gravity. The transferred momentum is not to scale with the gravitational acceleration.

b) symmetrical MACH-ZEHNDER interferometer in µ-gravity

FIGURE 1.1.: Comparison of Mach-Zehnder Interferometry schemes with and without gravity, which is denoted by $\vec{g}$. If gravity is present, the interferometer output is displaced to the coordinate z_1, thus the separation time is limited by the size of the apparatus. Furthermore, the enclosed interferometer area is small, due to the perturbation of the state trajectories. In microgravity. The interferometer output is constant at z_0, thus a higher sensitivity can be obtained in a smaller volume.

more precise measurement of g. However, for a large continuous acceleration in one direction, as on Earth's surface, the interferometric paths overlap with a relatively large displacement z_1 in relation to the opening point z_0 of the interferometer. Assuming an atom initially at rest, the baseline of the atom interferometer scales quadratically with the free falling time ($L \sim \frac{1}{2}|\vec{g}|T^2$), which is a serious impairment for the realization to those apparatuses. Even in a fountain scheme, with launched atoms, $T = 1\,\mathrm{s}$ demands for several meters of vacuum tubes which are very cost intensive and far from portable [21].

In microgravity, in absence of a relative acceleration between experiment and test object, an easier implementation of a symmetric BRAGG-diffraction scheme is possible (figure 1.1 b). The function of the $\pi/2$ and π pulses remains the same, but the core trajectories after the $\pi/2$ pulses are symmetrical in relation to the opening point. Moreover, the output coordinate remains the same for all separation times. Thus, given sufficient coherence, the interrogation time of the interferometer can be extended significantly. However, for macroscopic T, one has to account for sufficient volume to allow for a separation width $L \sim \frac{\hbar k_{\mathrm{eff}}}{M} \cdot T$, with the mass M of the atomic species employed.

Usually, interferometers with pulse separations of more than several tens of milliseconds are suffering from a fast loss of signal contrast, even with optimal optical cooling, since the residual momentum spread of an ensemble leads to fast expansion of the atomic cloud during interferometric interrogation. On the other hand, if this is circumvented with velocity sensitive beam splitter pulses, only a fraction of the initial cloud participate in the interferometry, again leading to contrast loss. Hence, the optimization of the momentum spread control of the interferometry input as well as the increase of the input particle number are paramount tasks for precision measurements.

Ultra cold atoms

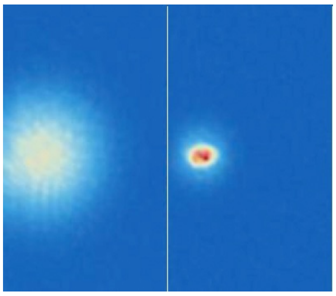


FIGURE 1.2.: Comparison of thermal and condensed ensemble. Both pictures are taken after 18 ms of free propagation, with only a slightly different evaporation sequence. After condensation, the BEC features a significantly denser cloud with much smaller momentum spread (adapted from [22]).

In classical thermodynamics, momentum spread is associated with temperature. Therefore, lowering the temperature of an atomic cloud to be probed equals reducing the momentum spread of the thermal ensemble, according to classical MAXWELL-BOLTZMANN statistics. However, for integer spin particles at lower temperatures, the BOSE-EINSTEIN statistic has to be employed. Inspired by a letter from BOSE, regarding the PLANCK-formula [23], EINSTEIN derived this relation for the energy-dependent occupation probability $n(\varepsilon)$, for particles trapped in a box potential [24]:

$$\langle n(\varepsilon)\rangle = \frac{1}{e^{(\varepsilon-\mu)/k_B\vartheta} - 1} . \tag{1.2}$$

Here, ϑ is the absolute temperature, and μ the chemical potential. Approaching $\vartheta \longrightarrow 0$, the evaluation of equation 1.2 yields a macroscopic occupation of the lowest energy state, the BOSE-EINSTEIN condensate (BEC). This transition marks a change of the state of matter, which makes the whole ensemble treatable as one single, collective quantum state.

If neutral atoms have an integer total spin, they can be considered as Bosons. For the experiments in MAIUS, for example, the bosonic isotopes of ^{87}Rb or ^{41}K have been chosen to create BECs. With the technique of laser cooling and trapping [25], it is possible to prepare samples of these atoms with temperatures as low as several µK. After employing evaporative cooling [26], the critical temperatures to achieve BOSE-EINSTEIN-condensation can be reached experimentally [27].

Similar to the laser, a freely propagating BEC can be understood as an extremely coherent matter-wave packet, ideally suited for atom interferometry [28]. Additionally, the method of *delta-kick collimation* (DKC) [29], allows to reduce the residual momentum spread of a released BEC, by conversion of mean-field energy. In Earth-based microgravity platforms, such collimated wave-packets prolonged possible pulse separation times to the order of seconds [30], limited by the available microgravity time. Although the technique can be utilized for both thermal and condensed atoms, its efficiency largely benefits from the point-source character of the BEC (figure 1.2), which is thus favorable for this technique.

Despite their ideal properties for atom interferometers, the preparation of collimated BECs is, compared with thermal atom sources, a more complex and time consuming procedure which presents a challenge for quantum sensors, which rely on high measurement repetition rates. Thus, the development of high-speed, high-yield BEC sources presents a key technology for modern quantum sensors, in order to benefit from the sensitivity increase a BEC atom interferometer promises.

Atom Chips

The first BECs have been created in room-filling apparatuses, comprising huge vacuum vessels, surrounded by large coils, and having a high power consumption during operation. Naturally, a way to reduce space, power consumption, as well as the detailed control of the just µm-sized atomic ensembles, would be the convergence of the field creating structures in close proximity of the atomic ensemble to be trapped. Here, strong, precisely shaped gradient potentials can be created, which allow for high efficiency of evaporation with much lower energy consumption than with conventional laboratory apparatuses. This can be achieved with the concept of atom chips: Conducting micro structures on a flat substrate, which is either introduced into the vacuum or placed close to the vacuum cell. With controlled currents, flowing through the micro structures, precisely tailored magnetic fields can be employed to trap atoms. Furthermore, the chips provide easy implementation of radio frequency (RF) antennas for evaporation towards a BEC.

The first atom chips have been introduced as elegant tools to create BECs in a simple manner. Shortly thereafter, a miniaturization of the overall vacuum setup could be demonstrated [32], which enabled the use of BECs in a wider range of integrated and portable scientific topics. With improved techniques of atom chip fabrication and more sophisticated engineering of the wire structures, the chips could even be used for atom interferometric measurements [33].

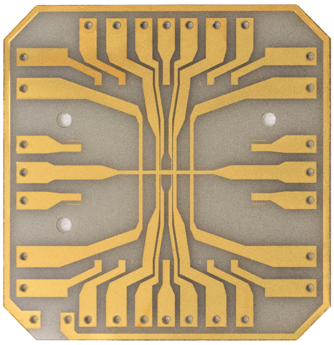


FIGURE 1.3.: Photograph of a MAIUS atom chip layer (adapted from [31]). The structures are made of gold on an aluminum nitride substrate.

After these achievements, the development of atom chips expanded into various fields of scientific topics [34]. An important milestone towards an increase of the flux of a chip-based cold atom source has been the introduction of mesoscopic structures in combination with small bias coils [35], which led to a significant increase in particle number and repetition rate [36]. State-of-the-art atom chip experiments are capable of producing DKC-collimated condensates of 10^5 in 1 s preparation time [22]. These achievements marked the necessary milestones to implement atom-chip-based matter-wave sources for compact quantum sensors.

Atom chip operation requires fast and low-noise current control, since the atoms are highly sensitive to the near field noise of the atom chip wires, which can convey several loss processes, such as spin-flips and heating to the trapped ensemble [16]. For the first proof-of-principle experiments, the necessary currents could be provided by already established laser diode current drivers [37–39]. However, the application of atom chips as a source of interferometry requires a drastic increase of the trap size and surface distance, which rely on magnetic field shapes only realizable with current values beyond the reach of standard laser current controllers [35]. Furthermore, external bias coils cannot be omitted in portable experiments, since the demands on amperage of suitable hexapole-compensated chips cannot yet be met by available compact batteries [40]. Thus, new regimes for current output values and dynamic switching performance become necessary, resulting in the demand for specialized current sources for atom chips.

Today, only very few specialized companies are able to fulfill these demands with suitable circuitry [17, 18]. However, the existing solutions are yet still designed for laboratories with ample lab-space. They are mostly driven with analog voltage signals, do not provide diagnostic data and are far too large and heavy to be operated in a portable setup. Therefore, a compact design of a chip-based matter wave source imperatively includes the creation of suitable current sources to satisfy the specific needs of portability and power economy of portable quantum sensors.

Universality of free fall

A most alluring application of quantum sensors in space are tests of General Relativity (GRT) [41], specifically one of its cornerstones, the universality of free fall (UFF). In a very simple formulation, it states, that in absence of any additional forces, the gravitational acceleration of two bodies is independent of their compositional properties. Experimentally, this statement is usually evaluated for two test bodies (1, 2) and their normalized differential acceleration in the EÖTVÖS-ratio

$$\eta = 2\frac{|a_1 - a_2|}{|a_1 + a_2|}\,. \tag{1.3}$$

If the UFF holds true, η should be zero at all times. However, in search of a grand unified theory of all forces, there are several enhanced gravitational theories, which propose a violation of the UFF in the quantum regime, which is not covered by the GRT. Especially a possible coupling of the non-classical property of spin is discussed [42, 43]. Today, the validation of the UFF in earth-bound classical tests has been performed down to the level of $\eta \leq 10^{-13}$ [13, 44]. A classical test on a satellite is currently in operation [45], which could demonstrate a measurement of $\eta \leq 1.4{\cdot}10^{-14}$ in the first experimental period [46].

Nonetheless, quantum tests with spin-polarizable atomic test bodies deliver a complimentary insight into the mechanisms of gravity, which are not necessary accessible with classical test methods, as they usually do not offer access to the quantum mechanical composition of the test bodies. The current earth-bound tests have reached a level of $\eta = 10^{-8}$ sensitivity [47, 48]. With the prospect of space-borne quantum sensors, new levels of sensitivity are proposed, which promise a significant progress toward an evidence-based standard model extension [11, 49].

Quantum Sensors in microgravity

As one of the first approaches to transfer cold atom research from the lab into field application, the QUANTUS project aims at the research and demonstration of technology and methodology suitable for a space-borne test of EINSTEIN’S GRT [50]. Using the drop tower in Bremen[1], the way from the laboratory to a portable test device for an UFF test in a space-like microgravity environment was the task for the project. Here, the whole experimental apparatus is dropped alongside the test bodies to emulate microgravity conditions during free fall. Furthermore, the demonstration of the controlled manipulation of ultra-cold matter waves in a space-like environment has been a driving factor for the QUANTUS collaboration.

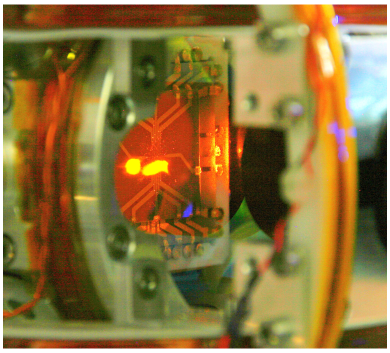


FIGURE 1.4.: Photograph of a magneto-optical trap employing an atom chip. The glowing cloud has a reflection on the optical coating of the chip. It consists of roughly 10^9 atoms with temperatures in the millikelvin regime.

In the pathfinder experiment QUANTUS-1, combining the compact atom chip source with a classical magneto-optical trap, it was possible to create a cold atom experiment suitable for a free falling capsule. With this apparatus, the first creation of a BEC in microgravity could be achieved, with the first long-term observation of 1 s [51]. Moreover, demonstration of advanced manipulation of the created BEC, such as DKC [52] could be achieved, resulting in first atom interferometric measurements in microgravity of

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[1] `https://www.zarm.uni-bremen.de/en/drop-tower/general-information.html`

up to $2T = 0.7$ s of total separation time [30]. With the help of higher order BRAGG-diffraction [53], the investigated technology could be applied as a quantum sensor: the first atom-chip based quantum gravimeter [54].

The next step in the development is QUANTUS-2, designed to be fully equipped for a quantum UFF test with ^{87}Rb and ^{41}K. With an enhanced sophisticated multi-layer atom chip (figure 1.4) and a two-stage magneto-optical cooling scheme, the efficiency and yield of the BEC source was improved significantly. After optimization, the chip setup achieved unprecedented flux rates, routinely yielding more than 10^5 condensed particles at a 1 Hz repetition rate [55]. Due to the intended use of the catapult mode in the drop tower, QUANTUS-2 has additionally been compacted to an easily transportable device. In order to achieve that, significant effort in technology development in the field of lasers and measurement electronics has been undertaken, funded in a supportive project called *Laser Systems in Microgravity* (LASUS). Nonetheless, the atom chip itself, being the most delicate part of the experiment, is still being operated with commercial, but substantially mechanically altered, current drivers [17], since they have been proven to be essential for the performance of the chip source.

Albeit the successes of the drop tower missions, they are not suitable for the investigation of long-term quantitative interferometry, given the short available free fall time of below 9.4 seconds in the tower, which only allow a few measurements per drop. So far, microgravity periods of significant duration and quality are only accessible in space. Thus, consequently following the goal of a space borne-apparatus, the QUANTUS sub-project MAIUS has been initiated, to establish atom interferometry on a sounding rocket platform on a high parabola flight. Three consecutive missions, MAIUS-1 to MAIUS-3, have been projected to successively establish the technology and the methods for a quantum test of the UFF in space, with up to 360 seconds of microgravity per mission.

Operating an experiment on a sounding rocket requires significant engineering efforts for its components to withstand the power handling and mechanical stress induced during a whole rocket mission, including pre-launch and re-entry phase. Moreover, volume and mass of the experimental apparatus have to be reduced drastically, combined with a system design which can be operated autonomously. As a consequence, the atom chip source requires compatible current sources which can replace the existing commercial solutions, while maintaining or improving their performance value. In this work, we will focus on the specific requirements and the construction and evaluation of such chip current sources, by the example of the MAIUS-1 sounding rocket mission.

The scope of this thesis

Basically, three central questions need to be addressed in order to construct current sources for high-flux, high-yield atom chip BEC sources:

- Which specifications are imposed on current sources by the experimental methods of a state-of-the-art atomic source, such as QUANTUS-2?
- What are the additional technical requirements given by the environment of the MAIUS-1 mission?
- Can the performance of the resulting designs match the estimated values?

Following this questionnaire, the two experiments, which formed the research platform for these issues will be introduced. Chapter 2 gives an overall introduction into the facilities and contents of the drop tower experiment QUANTUS-2 and the sounding rocket MAIUS-1.

Accessing the first question, in chapter 3, we will discuss the specifics of matter-wave optics on atom chips. Following a typical experimental sequence from initial cooling to a collimated BEC, a collection of key performance values for the new designs are derived (section 3.1). Moreover, a theoretical introduction of atom chips and trapped BOSE-EINSTEIN condensates (section 3.2) will be given. Section 3.3 reviews some limitations, which are inherently connected with atom chip traps. Especially the impact of technical noise will be reviewed and estimated with concrete values from the QUANTUS-2 apparatus. The specific atom chip configuration of the experiments QUANTUS-2 and MAIUS-1 will be introduced in section 3.4. The chapter concludes with a collection of specification values for the MAIUS-1 current drivers in section 3.5.

Moving on with the second question, the technical specifications of the electronic module of MAIUS-1 are reviewed in chapter 4. Initially, the common module specification and protocol for all functional electronics is introduced in section 4.1. The existing pre-conditions of the support hardware and their impact on the new designs are discussed in section 4.2. Additionally, the already fixed values of several key elements, such as battery voltages, are evaluated for some key performance aspects. In section 4.3, the additional safety measures are discussed, which have been stipulated additionally by the experimentalists, to protect the valuable atom chip assembly. In conclusion of the chapter, a complete, threefold list of design requirements is formulated, which is the guideline for the designs in the following chapter.

Chapter 5 familiarizes the reader with three designs which have been derived from the requirements. Initially, common design decisions are discussed (section 5.1). Afterwards, the designs of the three specific hardware modules are presented: A ground based test current driver (section 5.2), the MAIUS atom chip (section 5.3), and coil current driver (section 5.4). As the design requirements of the latter current driver involved several stipulations on the switching performance, some key problems for inductive loads have been simulated. The results and their consequences for the driver operation are presented in section 5.5. Finally, the functional concept of the chip safety circuit is explained in section 5.6, which is employed in combination with the current driver modules in MAIUS-1.

Our last question, the performance of the designs, is being investigated in chapter 6. Obviously, the characterization of components, especially in a complex environment, can hardly ever be considered to be »complete«, without performing every intended experiment of the mission. Hence, the measurements focus on the key values identified before. In section 6.1, basic functionalities will be demonstrated qualitatively, such as galvanic isolation and comparison of measurement and simulation. One key aspect of the performance, current noise, is evaluated extensively in section 6.2, in comparison with the state-of-the-art current drivers of QUANTUS-2. Several pitfalls of driver operation and their impacts on noise performance will also be discussed. Afterwards, a detailed noise spectrum analysis of the MAIUS-1 flight hardware is performed, with an attribution of the remaining noise contributions to specific sources in the circuitry.

Section 6.3 focuses on the stability of the current output of the MAIUS-1 current drivers. After detailed analysis of thermal drift, the stability of the thermally equalized circuits is characterized. Finally, the reproducibility of BEC in the integrated MAIUS-1 payload is investigated. Due to simultaneous temperature observation, a simplified model for temperature drift impact on particle number, condensate fraction and position of the released cloud is derived, giving hints on the dependence of several experimental stages from certain atom chip structures and coils (section 6.4).

Chapter 7 concludes the thesis with a review of the performance and limitations of the circuitry and possible improvement levers for future microgravity and portable application of chip-based atom sources.

CHAPTER 2

Experimental apparatus

This brief section introduces the two atom-chip experiments the miniaturized current sources have been developed for and which served as a testbed for their performance. The development is set in the wider context of the QUANTUS-collaboration, whose long term-goal is to perform comparative free-fall measurements on two atomic species, Rb and K, ultimately aiming at a quantum test of the UFF. By using atom interferometry, the residual acceleration on degenerate quantum objects should be compared in order to test the validity of the universality of the free fall as a cornerstone of EINSTEIN's General Relativity. Naturally, such an enormous endeavor has to be broken down to several milestones.

Based on the first microgravity experiences in the field of cold atoms, gained with QUANTUS-1 in the Drop Tower Bremen, the experiment QUANTUS-2 paved the way towards precision measurements in space. With a novel chip, rootedly designed for efficient BEC creation, and an innovative two-chamber design for experiments, the apparatus sets the benchmark for all following experiments in the context of QUANTUS.

After successful evaluation of the QUANTUS-2 design, its key elements allowed to integrate a BEC interferometer on a sounding rocket, in the mission MAIUS-1, allowing to increase the available microgravity duration significantly for BEC interferometry studies. Both experiments shall be briefly described, as they set the framework for design work on low-noise current drivers in the context of this thesis.

Detailed descriptions of the apparatuses can be found in [22] for QUANTUS-2 and [31] for MAIUS-1.

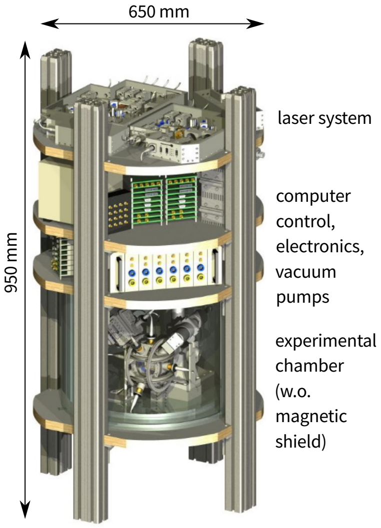

FIGURE 2.1.: QUANTUS-2 capsule drawing. (without hull and magnetic shield) Adapted from [22]

2.1. QUANTUS-2 - drop tower mission

QUANTUS-2 is designed to be a compact experiment operating in the Drop Tower Bremen, locater at the center of applied space technology and microgravity (ZARM). Its form factor is determined by the specifications of the capsules suitable for catapult operation [56], ultimately allowing for a microgravity time of up to 9.4 s. While in case of drops the start is comparable smooth, the payload experiences mechanical shocks of up to $300\,\mathrm{m\,s^{-2}}$ during catapult launch and $500\,\mathrm{m\,s^{-2}}$ at recapture. Whereas the latter criterion just poses a challenge regarding the ruggedness of components, the first one is affecting the whole experimental operation, stipulating that laser locks and other volatile operational parameters be maintained stable, even during these strong accelerations. Additionally, a significant part of the experiment's design has been the necessary reduction of component size in order to fit a lab-size experiment into the volume of a catapult capsule. As a result, the payload, comprising all components necessary to create and observe ultra-cold gases of rubidium and potassium, is housed in a cylindrical capsule with dimensions 950 mm × 650 mm, a volume of 320 L and a weight of 146.8 kg.

The focus of experiments in QUANTUS-2 has been the enhancement of the flux of BEC-creation with ^{87}Rb [55], necessary for atom-interferometric experiments as well as the development of methods to achieve unprecedented low kinetic (expansion) energies. [22]. Creation and manipulation ob BEC at these energy scales is extremely susceptible to tiny magnetic imperfections and perturbations. Hence, these experiments were mandatory to prepare the intended studies and tests with MAIUS-1, which itself could not be tested in the drop tower or other µg-conditions prior to its launch. So far, QUANTUS-2 performed more than 200 successful drops.

2.1.1. Overview

The functional subgroups of QUANTUS-2 are stacked onto each other, such that the connection pathway length is minimized. On the uppermost level of the capsule resides the laser system, the two intermediate sections are filled with a real-time capable computer system, laser controls, analog and digital I/O as well as commercial chip and coil current drivers. On the lowermost section of the payload, the vacuum chamber rests in a two-fold mu-metal shielding, which keeps external magnetic distortions to a minimum.

Starting on the second floor from the top, a vacuum tube leads from the ion-getter pump to the experimental chamber, penetrating all floors below. The scientific payload is powered by another module, not shown in figure 2.1, which houses the batteries and drop tower specific diagnosis systems.

2.1.2. Experimental chamber

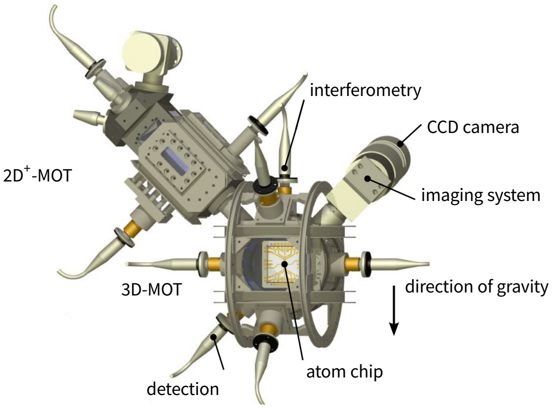

FIGURE 2.2.: QUANTUS-2 vacuum chamber (CAD drawing). The fluorescence detection in the central window is not shown. (Adapted from [22])

The central element of the experiment is a two-fold mu-metal shielded vacuum system consisting of a two-stage magneto-optical cooling system (figure 2.2). The first cooling stage employs atomic vapor, generated by an Rubidium oven, to create a high flux, low velocity atom beam with a 2D$^+$-magneto-optical trap (MOT). This beam is then fed through a differential pumping stage into the main vacuum chamber, which maintains ultra-high vacuum conditions ($p \leq 10^{-10}$ mbar). This part houses the atom chip assembly[1], capturing the atom beam of the first cooling stage in a 3D-MOT. The optical access for interferometry lasers is aligned on an axis parallel to the direction of Earth's gravity. The atoms can be observed with absorption imaging, with a magnification of about 1.8. Furthermore, a fluorescence photo diode and a second absorption detection axis can be employed in order to gain additional information on the atomic cloud's properties. The latter two detection systems are not shown in the figure, as they block the view on the atom chip.

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[1] Details on the chip design are introduced in section 3.4.

2.1.3. Laser system

The QUANTUS-2 laser system, developed and manufactured by the HUMBOLDT-university of Berlin, is especially designed to suit the needs of a drop tower mission. Due to customization of almost every part of the system, from the breadboard, over optical components such as couplers and mirror mounts, to special master oscillator power amplifier (MOPA) designs, the shock durability and miniaturization is significantly increased in respect to commercial or other laboratory systems. The system is capable to deliver cooling light for Rb and K. Additionally, two Raman interferometry modules will be added in a later stage to allow for interferometric manipulation of the two species. Details on performance and system design are documented in [57].

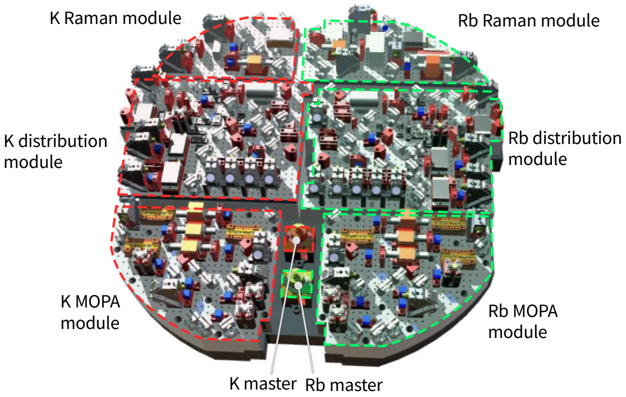

FIGURE 2.3.: QUANTUS-2 laser system (CAD drawing of the 2nd generation). The red parts of the potassium system are not yet integrated. Adapted from [22]

2.1.4. Experimental control

QUANTUS-2 is controlled by a commercial, real-time capable computer system[2] running a LabView® instance, which is accessible over Ethernet connection with any Windows computer running a LabView® graphical user interface (GUI). In the drop tower, this connection is realized via wireless local area network (WLAN) for data transfer.

The experimental sequence is executed by a central field-programmable gate-array (FPGA) card[3] which provides timed output for analog and digital channels. Based on this timing, additional modules in the PXI system generate RF signals for evaporation as well as the data communication with the absorption camera (figure 2.4)[58].

The FPGA digital bus is connected via an interface card to self-built electronic modules (ref: section 4.1), which communicate with the central computer via an unique, sophisticated protocol.

Additional to the digital connector, analog control voltages are delivered by the FPGA to the chip current driver section and laser system electronics. The FPGA analog output offers a refresh rate of 1 µs with 16 Bit resolution, resulting in a total range of ± 10 V, with step size of about 305 µV. The currents for the chip structures and the compensation coils are controlled by this card, using a 1 A/V calibration of the current drivers.

To provide sufficient channels for experimental operation, an additional analog voltage card[4] is used. Having only a refresh rate of 10 µs and a 13 Bit resolution, the ± 10 V output is reduced to a step size accuracy of 2.4 mV, which is sufficient for most components of the experiment, which do not rely on high precision control, such as e.g. RF attenuators or the 2D-MOT coil current driver.

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[2] `[National Instruments PXI 8183 RT]`

[3] `[National Instruments PXI-7054R]`

[4] `[National Instruments PXI-6723]`

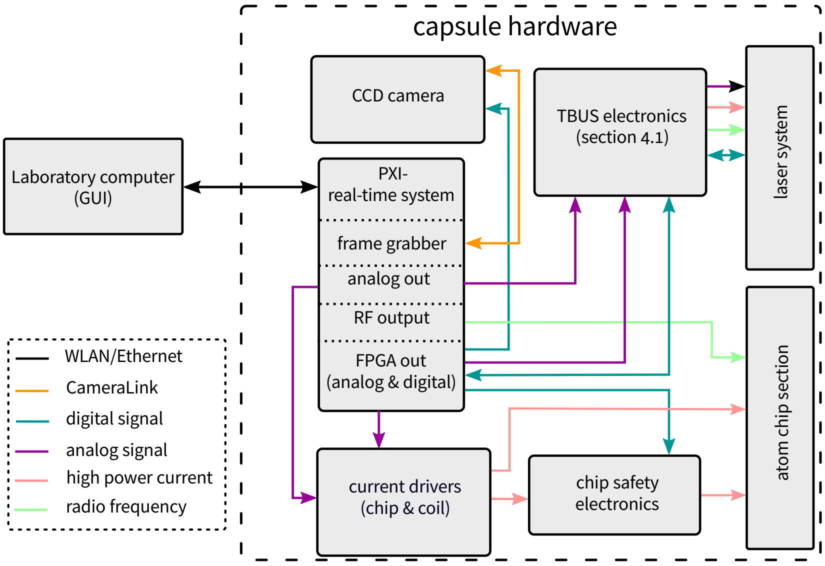

FIGURE 2.4.: QUANTUS-2 control diagram. Actualized version of the first description in [58]

2.1.5. Batteries

QUANTUS-2 is powered by a battery module, featuring state-of-the-art Lithium ferrophosphate ($LiFePO_4$)-battery cells of 3.2 V nominal voltage, which present the best compromise between energy density and operational safety. With the combination of these cells, eight voltages are delivered: +3.2 V (±1S), ±6.4 V (±2S), ±12.8 V (±4S) and ±19.2 V (±6S). Here the »S« refers to the number of cell entities in series. The battery packs are connected to a common ground. As the actual output voltage of batteries usually differs from the nominal voltage during charge and discharge, we will describe the battery configuration by the number of cells, not their output voltage.

The whole electronic layout of QUANTUS-2, which has to incorporate the laser electronics and experimental components, is prone to ground loops, due to several analog interconnections. Because of the significant current flow through the common bus system of the self-built electronics, the local ground reference level for each module can be shifted, depending on the overall power consumption. For precise operation of the analog current drivers, this has to be taken into account in the layout of the current driver power supply, since their operation demands for galvanically isolated batteries, in order not to cause cross-talk between different drivers[5].

Hence, the current driver rack employs five additional, galvanically isolated cell packages of ±2S, each to supply the current drivers for the chips and coils. For the loads of higher resistance (2D-MOT and Y-Coil), only one additional ±4S battery pack is necessary, since these structures are not galvanically connected. Details on the battery section can be found in [59].

2.1.6. Current driver setup

Precise magnetic field control for the atom chip is provided by six commercial current drivers[6], driven by the analog voltages available from the FPGA analog output. The housing and the

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[5] Details on correct grounding of atom chip current drivers are discussed in sections 5.3 and 5.4.

[6] `[High Finesse BCSP-10]`, designated HF1-6

modules themselves have been mechanically altered, to fit a single, 3-HU[7], 19-inch rack.

This already amounts to about one third of the available volume for electronics. To leave room for the remaining components of the electronic system, some structures, which do not demand for very high performance of their current sources, are controlled by self-built, much more compact current drivers[8].

The atom chip structures »Base-Z«, »Science-Z« and mesoscopic »U«[9] are operated with three commercial drivers, each powered with two separate batteries of ±2S. The mesoscopic »H« structure is soldered in a »racetrack« configuration, hence ensuring the exact same amount of current through all segments of the »H«. It is controlled by a custom-built current driver, which has been changed in calibration in order to allow for currents up to 15 A maximum range.

The compensation coils are connected to the other three commercial drivers, but powered with a shared ±4S battery pack to ensure sufficient current flow through the high resistive segments of the coils. The same battery powers the 2D-MOT coils, which are controlled by another self-built circuit, only differing from the Meso-H controller by a calibration change to 5 A maximum output current (figure 2.5).

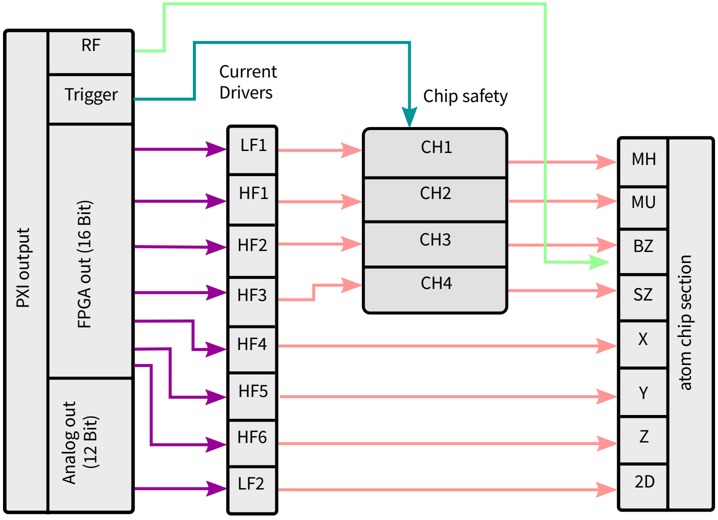

FIGURE 2.5.: QUANTUS-2 current driver connection diagram. Color of signals according to figure 2.4

The

2.2. MAIUS 1 - sounding rocket

The mission MAIUS-1 made the step from earth based microgravity experiments to measurements in an actual space environment. It is designed to study BEC interferometry for high precision experiments in space application. Based on the experience with QUANTUS-2, the mission lasted roughly 15 minutes, with up to 6 minutes of operation in space. Two following missions within the MAIUS project aim at the successive establishment of two species atom interferometry in space. Further details on the mission and on ground qualification are contained in [31], the mechanical design is covered in [60].

2.2.1. Misson goals and achievements

MAIUS-1 served to develop the methods necessary for BEC interferometry with high precision. This covers foremost the study of the phase transition of the space-borne BOSE-EINSTEIN

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[7] 3 height units (HU) correspond to 13.35 mm

[8] The drivers are custom-built, and in their functionality fully compatible to their successor design, which has been used for the MAIUS-1 pre-testing (ref: section 5.2). They are designated LF1 and LF2.

[9] ref. section 3.4 for further details

condensation in comparison to the ground performance. Furthermore, experiments related to the DKC and BRAGG-interferometry have been performed.

The experience with QUANTUS-2 showed, that apart from fast condensation and high atom numbers, the transport of the BEC away from the chip, as well as the disturbance-free release to free propagation are additional challenges for a successful atom interferometer. Thus, the following aspects of interferometric methods have been investigated in particular:

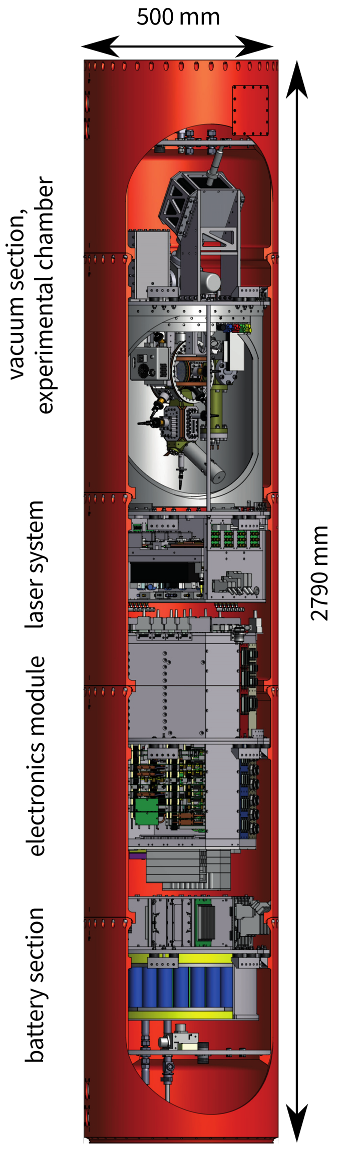

FIGURE 2.6.: MAIUS-1 scientific payload (CAD drawing). Adapted from [60]

- Transport, release and reproducibility of ^{87}Rb BECs in space – comparison with theory on transport schemes
- Experiments on DKC, exploring corresponding temperatures in the pK regime
- Interferometry-related experiments, including the adiabatic rapid passage into an non-magnetic state as well as BRAGG beam-splitter processes for a MACH-ZEHNDER-like interferometer

Soon after the successful launch on the 23rd of January, 2017, it became obvious, that the first goal of the experiment has been achieved. The creation of a BEC in space was the most important demonstration for the feasibility of atom chip technology for space application. In addition, the phase transition could be observed in detail. Furthermore, the evolution of the condensed atomic ensemble in chip traps and after the release into free propagation has been studied. Although interferometry tests have been performed, a spacial intensity modulation across the beam-splitter lasers has been observed during these measurements, which demands for a more elaborate analysis. Thus, a complete comment on these findings will be made in separate publications.

2.2.2. Overview

When transferring laboratory-proven technology to a new environment, the qualification of components plays a principal role, especially for space application of atom optics. Particularly, the vacuum module and the laser system have been subject to a great deal of modifications compared to ground systems. In contrast to drop tower capsules, which only experience a short shock of acceleration during impact or launch, the boost phase of a sounding rocket lasts for up to 60 s, with accelerations of varying frequency and amplitude of up to $120\,\mathrm{m\,s^{-2}}$. Additionally, the rotation of up to 3.2 Hz around the cylindrical axis conveys a strong strain to the mechanical hardware.

For the intended carrier system, a VSB-30 sounding rocket, the scientific payload has to be integrated into a cylinder of only 50 cm diameter. This results in an elongated payload of 279 cm height. The experiment itself consists of stackable modules, which can be connected on designated patch panels in order to operate the specific modules independently. For instance, the vacuum section has been tested with designated ground support modules during the evaluation phase. With a weight of 275 kg, the experiment is substantial heavier than QUANTUS-2, despite of the drastic saving in size and considerate optimization of materials. This is basically due to the necessary implementation of a thermal sink, since the experiment is operated for several minutes without the possibility to actively transport the excess heat away from the heat-creating elements. Additionally, the whole system was placed on shock mounts in order to dampen vibrations during launch, re-entry and landing to a tolerable minimum.

2.2.3. Vacuum setup

The vacuum section features the same basic components as the QUANTUS-2 experiment. The selection of the vacuum pumps[10] and the spacial orientation of the assembly differs, in order to withstand the strong perturbations during the rocket launch and to provide the required vacuum quality for the experiments in space. The ion-getter pump, which is run continuously, is additionally supported by the Titan-sublimation pump, which is used periodically to reach a residual pressure in 10^{-11} mbar regime in the chamber of the atom chip.

The atom chip is loaded by a cold atomic beam, generated in a separate, small chamber, using a 2D$^+$-MOT configuration.

Three layers of mu-metal are employed to strongly reduce the disturbing external magnetic fields during the rocket flight. As a result, the measured magnetic shield factor for the experiment is roughly 10^4 in the polar plane, and $2{\cdot}10^3$ in the cylindrical axis [61].

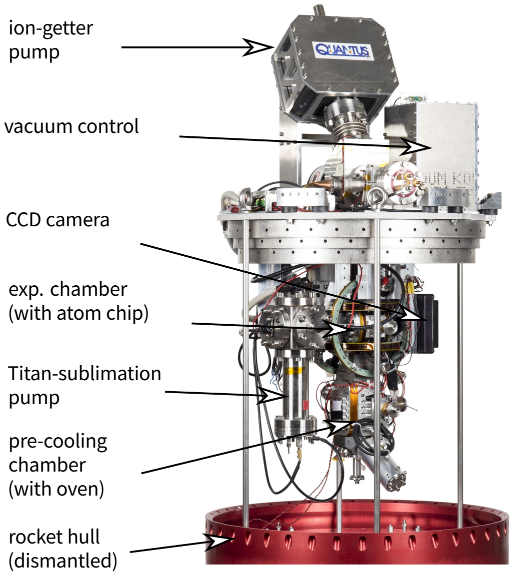

FIGURE 2.7.: MAIUS-1 vacuum section, with the atom chip setup in the experimental chamber. The magnetic shield and the rocket hull have been removed for cosmetic reasons.

2.2.4. Laser system

The MAIUS-1 laser system provides the cooling light for a 2D$^+$-MOT and a 3D-MOT as well as for BRAGG-interferometry. It is based on a sophisticated MOPA design, developed for ultra compact application [63]. In a joint effort of several project partners, combinations of ZERODUR®-based micro-benches with these miniaturized lasers have been constructed, which are able to withstand high temperature drifts without significant mechanical expansion. Despite the active cooling of the laser modules during the flight, such drifts are expected due to the high package density in the payload, combined with impaired heat dissipation of air in microgravity.

Mixing and distribution of the laser light is realized via fiber-integrated splitters, which provide the most compact realization of optical mixing. Moreover, with fiber splitters, repeated alignment procedures are no longer necessary, since fiber coupling is fixed with glued couplers, hence the laser system requires no regular maintenance.

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[10] Ion-getter: `[Varian/Agilent VacIon 20Plus]`, Titan-sublimation: `[VG Sienta ST22]`

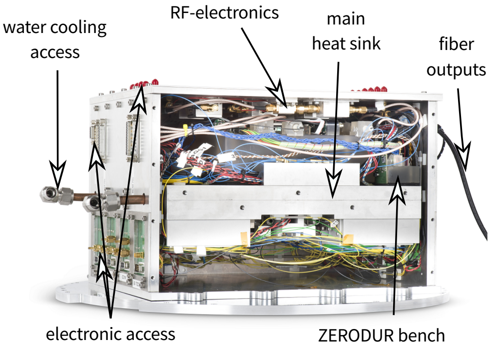

FIGURE 2.8.: MAIUS-1 laser system. One side wall has been removed (adapted from [62]).

While RF electronics, such as amplifiers and photodiodes are integrated into the module, current supply and frequency stabilization of the lasers relies on external circuitry, which is situated in the electronics module. To ensure continuous operation in the laboratory, the laser system has been equipped with a water cooling interface to keep the excess heat at bay. During flight operation, the water supply is disconnected and the remaining liquid serves as an additional heat sink contributor, resulting in only about 3 K temperature gradient during the flight.

With a size of 340 mm × 274 mm × 227 mm and a total mass of 27 kg, the laser system is sustainable at vibration tests of up to $81\,\mathrm{m\,s^{-2}}_{\mathrm{RMS}}$. Further detail on the laser system is described in [64].

2.2.5. Electronics module

The electronics module houses the experimental control of MAIUS-1, as well as the executing devices, like current drivers for lasers and atom chip, measurement interfaces, safety measures, temperature controllers, RF source and laser stabilization electronics. The main computer control is an off-the-shelf component. A large part of the other electronics consists of the modules developed and tested in LASUS, supplemented by some special designs especially designed for the MAIUS-1 mission.

The electronic circuits are located on printed circuit boards (*cards*), which can be combined in functional sub-groups (*stacks*). In these stacks, the cards are individually addressable via an Ethernet-like protocol using standard network cables. The data communication is routed via a central network switch and distributed by the control computer.

The whole electronic module is designed to be operable autonomously to the highest extend possible, as, in contrast to drop tower experiments, the data communication between payload and ground control is not only delayed, but can also easily be interrupted. Based on a Linux operating system, the flight control software has been developed by the DLR Center for Software Technology (DLR-SC) to fit the needs of a highly complex control system such as MAIUS-1.

As an example of advanced control methods employed in MAIUS-1, the laser control includes not only a self-built digital frequency controller card, but also a novel algorithm to enable self-sustained spectroscopy locking (figure 2.9). This technique allows for automated frequency locks in the case of control failure due to vibrations during the launch phase and is therefore crucial to the success of laser-based experiments on sounding rockets.

Since the integration of the electronic module is very delicate and time consuming, the MAIUS-1 experiment contains a unprecedentedly large number of diagnostic measurement data to evaluate erratic behavior prior to de-integration for troubleshooting. Thus, albeit the substantial additional complexity, MAIUS-1 greatly benefits from the flexibility and stability of the control software, which makes the electronics module an outstanding milestone towards reliable, low-maintenance atom optic experiments in field application.

2.2.6. Battery section

The battery section is very similar to that of QUANTUS-2. With $LiFePO_4$ accumulators, the same backbone and cell voltages are used to create the voltages necessary to operate the custom-built electronics[11]: +3.2 V (±1S), ±6.4 V (±2S), ±12.8 V (±4S) and ±19.2 V (±6S).

Additionally, the module envisages six galvanically isolated batteries (2S, 6.4 V) for chip current drivers, to enable full operability on all chip structures. In contrast to QUANTUS-2, only one battery per driver is necessary, hence the setup is of half the size as in the drop tower.

The compensation coils are to be powered by one high capacity battery (3S, 9.6 V), which needs to be galvanically isolated from the main experiment, to be independent from local ground shifts for the respective modules (ref.: section 5.4.2)[12].

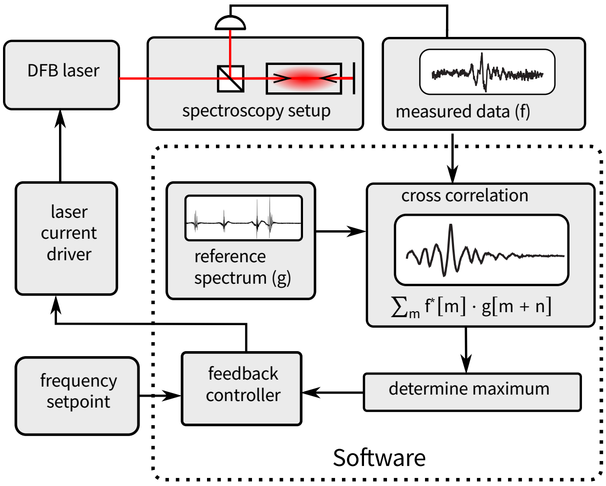

FIGURE 2.9.: MAIUS-1 auto-lock schematic. The frequency controller software samples the spectroscopy data. Afterwards, a cross correlation with prerecorded spectra delivers a feedback. The digital controller then generates a setpoint for the laser current driver. Details are described in [65]. (graphics adapted from same source)

2.3. Summary

This section introduced the two apparatuses on which the main research of this thesis has been conducted and which set the design goals for the development and operation of the electronics. Their application environments demand for extremely compact, powerful and precise current drivers, which are able to operate on variable loads. These requirements hold true also for most space experiments and portable gravity sensors. While QUANTUS-2 is able to fulfill these demands with mechanically altered commercial solutions, the even further restricted volume of MAIUS-1 is requiring a customized solution for current control.

The common electronic environment of the customized electronics represents a guideline for data communication and battery connection. It has been developed and tested in the technology support project LASUS with a strong focus on application in space. Modules with comparable parts as the current drivers to be designed have been qualified in shock and vibration tests as suitable for sounding rockets. Thus, it is fair to assume, that novel designs obeying the general design rules of the LASUS modules will also be qualified.

In the following chapters, we will now evaluate the physical processes and technical requirements, which influence the design of the MAIUS-1 current drivers.

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[11] The modules have the same architecture as in QUANTUS-2, further details on the interface are given in section 4.1

[12] As it turned out during pre-launch testing, this has not been realized during assembly, due to the lack of electronic access pins, therefore minor curtailments in stability of the coil currents are to be expected.

CHAPTER 3

Matter-wave optics with chip-based magnetic traps

Advancing on the task of developing suitable current driver concepts for MAIUS-1, we will review the necessary cooling and manipulation methods as they are performed in atom chip based cold atom sources and determine scientific requirements on the current sources to be employed. Apart from laser cooling and trapping of large atomic ensembles, the atom chip enables functions like magnetic trapping and efficient evaporation towards a BEC. Moreover, the chip allows the collimation of BECs with magnetic lenses in order do reduce the atomic expansion for extended observation times.

The main focus of our discussion will be an optimized atom chip operation for fast, high-yield sources of BOSE-EINSTEIN-condensates, with additional momentum spread manipulation for ultra low cloud expansion after release from the trap. By reviewing the performance of a benchmark example, in this case the source concept of QUANTUS-2 [55], we will derive the stipulations on the current drivers employed in the setup, which will guide the following design process for the MAIUS-1 mission.

In order to be suitable for the atom interferometric measurements intended in the QUANTUS experiments, a atomic source hat to possess three essential properties:

ultra-low temperature: In order to achieve maximum sensitivity in an atom interferometer, the momentum spread of the input state is to be minimized [9]. This corresponds to temperatures[1] much lower that it is achievable with laser cooling alone. For thermal ensembles, this can be realized with velocity selective blow-away pulses. However, for a three dimensional preparation, this results is high particle loss and does not improve the precision in the determination of the center of mass motion of the cloud. A BEC, in contrast, possesses much smaller momentum spread than a thermal cloud, with a more qualified center of mass determination. Thus, photon induced momentum changes can be used to spatially separate interferometer states to be employed in a measurement scheme, with most of the initial atomic cloud participating in the measurement. Nonetheless, the particle loss during of BEC preparation, the infeasibility of state preparation through optical pumping and the possible impact of inter-particle interactions on the overall kinetic energy remain issues that keep BECs from being a general purpose atom source for atom interferometers.

high repetition rate: In the intended interferometric use of quantum sensors, frequent measurements are necessary. Firstly, it is feasible to average a measurement over a number of measurements in order to enhance the sensitivity of the apparatus. Secondly, some changes of a measured quantity, e.g. the Earth's gravity, are of great interest in the Earth sciences. Therefore, to access a certain frequency resolution, the measurements have to be repeated fast enough in order to fulfill the SHANNON-NYQUIST theorem, with resolution bandwidth ν_b and repetition rate τ_s:

$$\nu_b \leq \frac{1}{2} \cdot \frac{1}{\tau_s} \,. \tag{3.1}$$

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[1] Depending on the underlying theory, describing the state of the atoms, the residual momentum spread is sometimes expressed in units ~ $k_B T$ which is then referred to as temperature for a thermal gas, or, in the case of a BEC, since it has no thermodynamical temperature definition, as »effective temperature«, corresponding to an ideal thermal gas.

Thus, a high repetition rate of measurements increases both long-term sensitivity and frequency resolution of an interferometer.

high particle number: Atom interferometry usually relies on single particle effects, hence can be improved by statistics in the order of $N/\sqrt{\tau_c}$. Here, N is the number of particles per measurement and τ_c the cycle time. Thus, the increase in particle number for the interferometry is highly beneficial in order to gain single shot sensitivity.

Unfortunately, these three properties are closely connected with each other. In the QUANTUS interferometry sources, a BEC is created to obtain a low initial temperature spread. However, in the cooling process towards BEC, a high loss of atoms, compared to thermal clouds has to be anticipated. Furthermore, the preparation procedure usually is lengthier and complicated than with thermal clouds, which can negatively affect the cycle time. Thus, a suitable source concept for BEC interferometers has to take these connections into close consideration.

Atom chips provide excellent means of achieving these properties simultaneously, while maintaining a small experiment size. By reviewing a typical experimental sequence of an atom chip experiment, we will collect key values and parameters to be fulfilled by the atom chip and current drivers. Afterwards, we will discuss the elemental theory of atom chips, followed by a more detailed description of the chip setups of QUANTUS-2 and MAIUS-1. Adverse mechanisms, such as particle loss and heating of atom chip traps, which are reducing their BEC flux, will be discussed in the following section. Moreover, the impact of these effects will be evaluated for a given chip trap, as it is expected to occur in the MAIUS-1 experimental sequence. Finally, we can formulate preliminary design guidelines for current sources suitable for atom chip operation.

3.1. Cooling of ^{87}Rb to quantum degeneracy

In this section, we discuss the cooling processes and preparation steps necessary for BEC interferometry, which have to be taken into account in the design phase of the current drivers. From the typical performance of the experiment QUANTUS-2 [55], we will derive key requirements on the current drivers, which have to be fulfilled for the upcoming design phases.

3.1.1. Magneto-optical trapping

The first step of cooling of the Rb particles is the magneto-optical trap (MOT). It provides the first slowing of thermal atomic vapor into a confined space close to the atom chip. In the setup of QUANTUS-2, the trapping is twofold. The states participating in the cooling of ^{87}Rb are of the $5^2S_{1/2} \longrightarrow 5^2P_{3/2}$ transition. The transition of hyperfine states $|F = 1, 2\rangle \longrightarrow |F' = 0, 1, 2, 3\rangle$ can be addressed with a laser of 780 nm. in the case of QUANTUS-2, the cooling transition is chosen to be $|F = 2\rangle \longrightarrow |F' = 3\rangle$, being a usually closed transition according to selection rules. Due to the detuning of lasers, ZEEMAN-splitting and a finite line width of the laser, the additional $|F = 2\rangle \longrightarrow |F' = 2\rangle$ transition can be exited, which itself decays by a fraction into the »dark state« $|F = 1\rangle$, which is not accessible by the cooling laser. Therefore, a second frequency of laser light is necessary to drive the $|F = 1\rangle \longrightarrow |F' = 2\rangle$ transition, thus reintroducing the atom into the cooling circle.

2D$^+$ magneto-optical trap

As an atom chip trap is only capable of creating high gradients between the »U« wires of the planar circuit, the volume and therefore the capture velocity of a chip-MOT is very small, compared to conventional setups. An additional hurdle in providing enough damping of the particle movement is the limited diameter of the laser beams[2]. To achieve a high flux of laser cooled atoms, it is beneficial to load the chip-MOT with a cold atomic beam rather than from the thermal Rb vapor in the chamber. This beam is formed in a 2D$^+$-MOT [66] in a compact, but conventional setup.

With this source, a directed beam of pre-cooled atoms with a flux of $\Phi \approx 10^{10}$ atoms/second, a velocity of $v = 20\,\mathrm{m\,s^{-1}}$, and a spread of $\sigma_v = 22\,\mathrm{m\,s^{-1}}$ is directed to the center of the chip trap. The flux is linearly dependent on the power of the transversal cooling light and is limited in the current setup by the available laser power.

The magnetic necessary fields are generated with two HELMHOLTZ-coil pairs in a series connection, whose current flow is optimized with bypass resistors . This results in a relatively high resistance of the whole load, with medium inductance. In this setup, the current driver has to provide 2.5 A in ≤ 5 ms in order not to impair the overall performance.

3D magneto-optical trap

For the next cooling step, a three-dimensional enclosure is achieved by employing magnetic fields and laser light. Due to a state separating ZEEMAN-splitting and a detuning δ of the laser frequency towards the atomic cooling transition, atoms leaving the trap center hit resonance at a certain velocity due to DOPPLER-shift of the laser light. Caused by the following stimulated emission, the atom experiences a force, pushing it back towards the trap center in all directions.

The theoretical boundary for this cooling scheme depends on the detuning δ of the laser towards the atomic resonance and the inverse lifetime Γ of the upper cooling state, referred to as the DOPPLER-temperature [25]

$$\vartheta_\mathrm{D} = \frac{\hbar\Gamma}{4\,k_\mathrm{B}}\left(\frac{\Gamma}{2\delta} + \frac{2\delta}{\Gamma}\right). \tag{3.2}$$

This relation minimizes for $\delta = -\Gamma/2$, yielding the DOPPLER-limit

$$\vartheta_\mathrm{DL} = \frac{\hbar\Gamma}{2k_\mathrm{B}} \tag{3.3}$$

which is in the case of the employed cooling transition 146 µK [67].

The 3D-MOT of QUANTUS-2 employs a mirror-MOT reflection scheme. Instead of six laser beams and external coils, the atom chip delivers the magnetic fields and acts as a mirror for the incoming light fields, reducing the number of necessary light beams to four. Figure 3.1 depicts the schematic of the irradiated light beams, and the magnetic field created by the chip.

The current setup employs a quadrupole field with the gradient of $20\,\mathrm{G\,m^{-1}}$, resulting in a capture velocity of $30\,\mathrm{m\,s^{-1}}$. In combination with the 2D$^+$-MOT, an initial loading rate of 10^9 atoms/second can be achieved, saturating with $2.5{\cdot}10^9$ atoms after 4 seconds. The MOT achieves temperatures of down to 200 µK. This is a good trade-off between low temperatures

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[2] 18 mm [58, pp. 21–23]

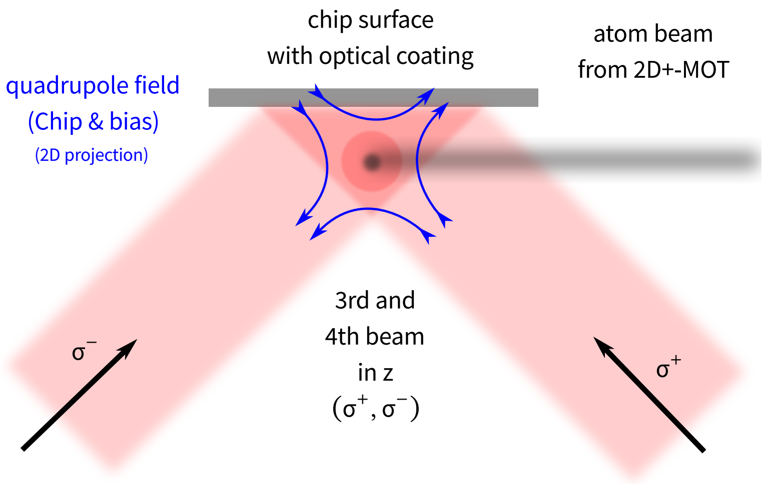

FIGURE 3.1.: Schematic of the mirror MOT. Two laser beams of opposite helicity hit the reflective surface of the chip in an angle close to 45 °, therefore providing all necessary light polarizations on the point of the magnetic field minimum, which itself is generated by the chip structures with the help of an external bias field. The light field parallel to the chip surface (circle, resembling a beam in z direction) completes the enclosure of the atoms to a MOT. In comparison to a conventional setup, only 4 optical access paths are used and the reflection reduces necessary laser power by 33 %.

and high spacial enclosure close to the chip surface, which is equally important to yield a high efficiency while transferring the atoms into the next cooling step.

Compression MOT

With the size of some mm in diameter, the atomic cloud after the MOT stage is not yet suitable to be efficiently loaded in the pure magnetic trap. In order to achieve further compression, the detuning is changed to −40 MHz while ramping down the quadrupole gradients to a few $\mathrm{G\,cm^{-1}}$. While relaxing the radiation pressure from within the dense atomic ensemble, the trap minimum is slowly moved towards the chip in order to create an optimal overlap of magnetic trap and center of mass. With this experimentally derived procedure, the efficiency of the transfer from the MOT to the pure magnetic trap has been optimized, although a perfect overlap is physically impossible without colliding a part of the atoms with the chip surface, thus loosing this fraction in the transfer. The atoms close to the trap center, with sufficiently low kinetic energy, can be transferred in the next trapping stage.

When it comes to current sources, above cooling steps are not very demanding in terms of sensitivity to noise, but pose the highest demands power-wise. For an intermediate loading time of 1 s, 2D and 3D-MOT current drivers are subject significant excess heat[3]. For a high repetition rate, it has to be ensured that the circuits have a sufficient thermal stability to operate these powers in a repeatedly pulsed measurement scheme.

3.1.2. Sub-Doppler cooling

After the compression of the MOT, which usually leads to a higher temperature of the compressed cloud, the atoms are cooled in an optical molasses [68] with a detuning of −116 MHz within 2 ms to a temperature of 20 µK [55]. This value, although well below the DOPPLER limit temperature, is much higher than already demonstrated values in the laboratory. This

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[3] ref.: section 4.2

is a typical trade-off for reflection schemes on atom chips: Due to the unavoidable reflection losses, there persists an imperfect power balance between incoming and reflected beams, thus molasses temperatures on chips are usually higher as those of classical setups. Furthermore, scattered light from the chip surface and particle collisions in a dense cloud leads to the deviation from the much lower minimum photon recoil temperature [69].

$$\vartheta_r = \frac{h^2}{m k_\mathrm{B} \lambda^2} \overset{\left(^{87}\mathrm{Rb}\,,\,D_2\right)}{\approx} 361\,\mathrm{nK}$$

Here, λ is the wavelength of the cooling laser, m the mass of a Rb atom.

Ideally, there are no magnetic fields present during optimal molasses cooling. Nonetheless, during optimization of the performance, current sources of the bias coils are employed to compensate for any remaining external offsets which are not damped by the magnetic shield. Therefore, a precise calibration of the current drivers close to zero current is necessary to generate small fields precisely enough to minimize the residual magnetic field close to the atoms. Furthermore, as the disturbance field direction cannot be estimated, the polarity of the current through the compensation coils must be variable in both directions as well. This is crucial for the design of the coil current driver, as the battery configuration of MAIUS-1 does only provide a single polarity of current supply.

3.1.3. Optical state transfer

The shape of the magnetic potential is determined by the ZEEMAN-effect and hence ultimately depending on the hyperfine sub-state, represented by the quantum number m_F. Thus, for rubidium, only atoms with positive quantum numbers experience an attractive potential with a confining minimum. In order to trap all atoms in the harmonic potential, the initially randomly populated magnetic sub-state has to be prepared. To achieve that, a magnetic field of approximately 4.3 G in direction of the laser beam is built up by the external bias coils, in order to ensure proper state selectivity. Additionally, a directed, σ^+-polarized, far detuned laser beam is directed towards the atoms to drive transitions from $|F = 2, m_F = k\rangle \longrightarrow |F' = 2, m_F = k + 1\rangle\ k \in [-2, +1]$. Ultimately, this procedure leaves every atom of the ensemble in the dark state of this transition, $|F = 2, m_F = 2\rangle$.

The state transfer is crucial in an efficient cooling cycle towards the BEC. In order not to heat the carefully cooled atoms, it has to be as fast as possible to ensure a minimal diffusion from the point of molasses cooling. This is only possible, if the magnetic field is built up quickly and without overshoot, as this would disturb the state selectivity. In the setup of QUANTUS-2, the light is guided towards the detection axis.

3.1.4. Transfer into magnetic trap

With the atoms sufficiently cooled and prepared in a magnetically trappable state, the laser light is turned off and the cloud is transferred into the a purely magnetic trap of IOFFE-PRITCHARD-configuration[4]. This procedure suffers from the largest uncontrolled losses in the cooling sequence. To ensure an optimal mode matching from the freely expanding gas after the molasses and the magnetic trap, magnetic potential with a minimum at the location of the atomic cloud has to be created very quickly, while not exciting any additional motion.

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[4] section 3.2.5

The transfer into the magnetic trap is limited for several reasons. Firstly, the trap volume of the biggest possible magnetic trap is still relatively small compared to the spacial atom distribution after the optical state transfer. This leads to a loss of particles that cannot be confined in the trap center. Furthermore, the center of mass after the molasses is determined by the diameter of the laser beams, thus the confining trap needs to be generated in a relatively great distance to the chip, which demands for high currents through the structures, ultimately resulting in a limitation of confinement. Due to this limitations, the MOT loading time for QUANTUS-2 is usually reduced to several hundreds of ms, since larger particle accumulation in the initial MOT bears no improvement for the transfer into the magnetic trap.

With an optimized procedure, the QUANTUS-2 apparatus is able to transfer up to 25 % of the initial MOT into the magnetic trap, ending up with approximately $2{\cdot}10^8$ particles. After successful transfer to the magnetic trap, the particles are moved closer to the chip, where the trap geometries are more suitable for high efficiency in further cooling steps.

3.1.5. Evaporative cooling to degeneracy

After the transfer of optically cooled atoms into a first magnetic trap, further cooling steps require for tighter traps close to the atom chip's surface. Now confined in a harmonic trap, the ensemble's high energy particles are removed from it. The following re-thermalization of the remaining particles leads to an overall reduction of the ensemble temperature.

This technique of evaporative cooling [26] is realized with RF coupling particles of higher kinetic energy to un-trapped states, thus selectively reducing the trap depth ω_D.

As a result, the remaining trapped atomic cloud features a significantly lower temperature than before. Thus, the *phase-space density* Λ of the ensemble is increased. This process is conducted with several frequency ramp durations and slopes, until the RF reaches a value slightly above the trap bottom ω_B. For a value of $\Lambda = \zeta(3/2) \approx 2.6124$, the phase transition to a BEC occurs.

The detailed procedure and efficiency is described in [55] and does not rely on any special functional features of the current drivers. Nonetheless, precision and stability, as well as low current noise are a necessity for the success of the evaporation towards a BEC. The stability of the offset field is to be maintained, as the value of the trap bottom determines the end value of the evaporation, which is very sensitive[5]. Furthermore, the low noise of the current has to be ensured to inhibit heating or loss processes that would counteract the controlled evaporation and impair the continuous re-thermalization to lower temperatures.

The concept of evaporation and the phase transition involves a high loss of atoms, to achieve a high phase space density, even, when close to the optimum efficiency [55]. Thus, albeit starting with 10^8 particles in the beginning, the evaporation sequence ends up with condensates of up to $2{\cdot}10^5$ particles, which is already considered a macroscopic BEC with atom chip traps.

3.1.6. Trap transfer and release

After condensation, the main goal of the experimental cycle is the release of the BEC into the untrapped continuum in order to perform the cloud preparation for interferometry. In order to manage this accordingly, the internal dynamics of the condensate[6] have to be taken into account, as well as the oscillations of the center of mass within the traps. As another

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[5] ref.: section 6.4

[6] ref.: section 3.2.2

complication, the time between condensation and trap release is of the essence as well, since loss mechanisms due to the proximity to the chip limit the lifetime of the condensate[7].

Currently, significant effort is put into research of non-adiabatic trap transformations that decrease the time of trap transfer without imprinting too much residual motion or oscillation [70], [22]. As of now, it is possible to transfer atoms with strongly suppressed center of mass motion and some controllable internal oscillation modes, which are – since we are working with anharmonic trap geometries[8] – coupled. This is an improvement to a simple switch-off of the evaporation trap, but still has room for optimization.

Especially the release to the continuum and the residual momentum plays an important role to the efficiency of the next topic, the delta-kick collimation.

To achieve optimal control of the trap shape, it is mandatory to have sufficient possibility to shape arbitrary waveform ramps, to synchronize switching of cooperating structures. While in QUANTUS-2 this is ensured with the computer control system, for MAIUS-1 this is a requirement on the current driver modules themselves.

3.1.7. Delta-kick collimation

For precision interferometry, the initial momentum spread of the atomic cloud is very important, which is why BECs are beneficial for such measurements. However, the momentum spread of a condensed cloud can be even further reduced by precisely shaped magnetic field interaction.

After the release of the formerly trapped BEC, a timed and precisely shaped magnetic pulse is applied, narrowing the momentum spread and thus significantly slowing down the expansion in the free evolution. With this technique, a reduction of kinetic energy, corresponding to pK ranges in ideal gases can be achieved. This technique was introduced as »delta-kick cooling« [52], but this term is misleading. During the magnetic manipulation, the phase space volume is preserved. Therefore the whole process is not a reduction of temperature. Instead, the momentum spread of the atoms is collimated by the magnetic field like light beams in an optical lens. Thus, we will refer to it as *delta-kick collimation* (DKC).

Apart from experimental circumstances, such as switching of coupled structures, materials, inductances etc., the form of the pulses and timescales vary, depending on the initial release trap shape and its position relative to the chip. The actual considerations for the QUANTUS-2 experiment are still under investigation and promising preliminary results are discussed in [22]. With this not fully optimized sequence, the record of $9.3{\cdot}10^4$ condensed atoms with a three-dimensional effective temperature of ~47 pK could be obtained.

Nonetheless, the possibilities of realization rely on a good quality of magnetic field control. As most schemes will probably include shaped pulse forms, a current control with ideally no overshoot is beneficial. If only using chip structures, the timescales of $\leq$ 100 µs are sufficient for all kinds of DKC schemes. However, if using bias coils as well, the possibilities are somewhat limited by the finite settling time of the magnetic coils, which can be up to 2 ms and even longer for higher currents than currently used. Hence, the optimization of settling time, while maintaining a reduction of overshoot, presents a key task in the implementation of current control[9].

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[7] ref.: section 3.3

[8] ref.:section 3.2.3

[9] ref.: section 5.5

3.1.8. Adiabatic Rapid Passage

After the preparation of the atomic ensemble, it is necessarily in the magnetically trappable $|m_F = +2\rangle$-sub-state of the ground state manifold. Being sensitive to external magnetic fields, this state is not suitable for precision interferometry, as long as magnetic disturbance can not be excluded during the measurement process. Therefore, a state transfer in to the $|m_F = 0\rangle$ state, which is magnetically insensitive in the first order, is performed.

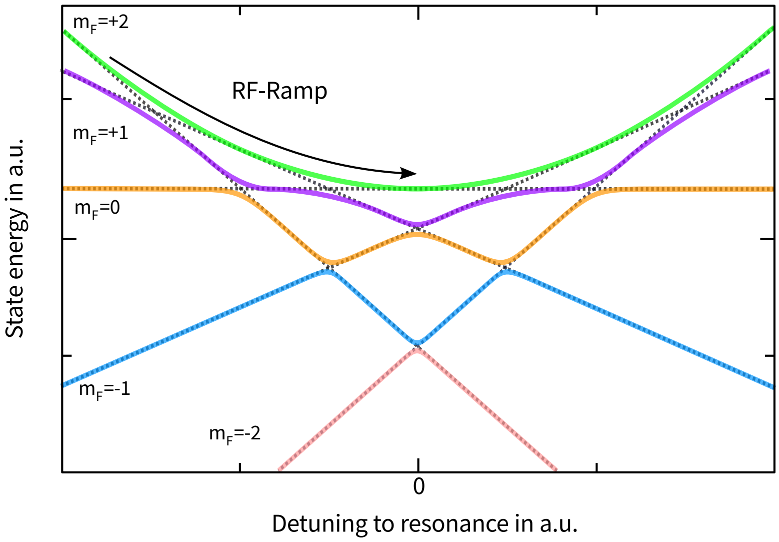

FIGURE 3.2.: State transfer in the Adiabatic Rapid Passage. Solid lines depict the dressed states, which can be expressed as a superposition of eigenvectors of the uncoupled atom states. Dashed lines of equal slopes represent these undisturbed states. Starting with high detuning in the $m_F = +2$ state, the detuning is ramped to $\Delta = 0$, leaving the majority of particles after back projection into the atom eigenstates in the $|m_F = 0\rangle$ sub-state (transfer depicted with arrow trajectory). (adapted from [58])

The technique employed is the Adiabatic Rapid Passage (ARP) [71]. This transfer is rapid in relation to the relaxation of states, which can be neglected since the BEC is in the ground state, and adiabatic enough for the system to follow the changes to achieve state transfer. In the given experiments, a strong magnetic bias field is employed to generate a large ZEEMAN-splitting of the m_F manifold. Afterwards, a detuned RF field is introduced and ramped in frequency over the atomic resonances.

Depending on the amplitude and the detuning of the RF field, the system can be described in the *dressed state picture*, with states that are a coherent superposition of the initial atomic sub-states, but with avoided crossings between them (figure 3.2). With the right change of detuning, the initial $|m_F = +2\rangle$ state can be transferred to the $|m_F = 0\rangle$ within this dressed states and maintains this state, after the RF field is switched off, thus »undressing« the states again. The quantization field can now be lowered and the atoms remain in the $|m_F = 0\rangle$ state.

While this procedure is surely not the bottleneck of the atomic source[10], it requires a delicate interplay of RF electronics and current sources. The magnetic field providing sufficient state separation requires usually for relatively high currents that have to be provided with a well defined switching, in order not to disturb the atoms. The absolute value of the magnetic field does not only shift the energy splitting, but also influences the resonance. Therefore, especially during switch-off, an overshoot in the current, alongside with a finite line width of the RF

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[10] usually, transfer efficiencies of ≥ 95 % are achieved

field, can lead to a false projection, e.g. in the $|m_F = \pm 1\rangle$ states. This is another argument for precise current control in the magnetic coils.

In addition to these preparation steps, it is possible to exploit several interferometric schemes. Their assets and drawbacks are not the subject of this work and will therefore not be treated. For the first demonstration of coherent manipulation, MAIUS-1 will employ an asymmetric BRAGG-based interferometry scheme [30]. For future missions, a symmetrical BRAGG-scheme is intended [53], as well as a symmetrical RAMAN configuration.

3.2. Elementary Atom Chip theory

The concept of trapping of neutral atoms, such as Rubidium, relies on the non-vanishing magnetic moment which can be used to convey external potentials to the atom via the ZEEMAN-effect, which couples a magnetic field to the magnetic moment of the atom, depending on its hyperfine state ($|F, m_F\rangle$, $m_F \in [+F, -F]$).

With precise tailoring of an external magnetic field, one can create potential minima to trap atoms, depending on their internal state. Furthermore, the combination of magnetic fields with atom-light interaction allows for cooling thermal atoms to several µK within fractions of seconds.

Suitable arrangements of magnetic fields usually operate with a classical setup of coils outside of a vacuum cell, but demand for high electrical power for strong magnetic fields as their field amplitude decays $\sim r^{-1}$. While this is not an issue in a stationary lab-based environment, it is indeed problematic when portable setups are employed or power consumption is restricted. Both cases apply to the QUANTUS experiments, which rely on energy efficient, portable apparatuses.

A useful approach to reduce the power consumption is to use integrated planar circuits in vacuum, which are able to generate strong magnetic fields in the immediate vicinity of the atoms. This concept of »atom chips« led to atom trapping and cooling with relatively low currents of about 10 A while still being able to create extremely deep traps to enable for evaporation cooling close to the optimum. Additionally, atom chips can be coated to function as optical elements, thus reducing complexity of the optical setup. In the following, we will review some of the elemental theory regarding the creation and description of atomic chip traps.

3.2.1. Key parameters for harmonic chip traps

An atom with a magnetic moment $\vec{\mu}$ is affected by magnetic fields due to the ZEEMAN-effect. For a static confining potential B, the LARMOR-frequency ω_L describes the time scale of the atomic reaction to magnetic field changes:

$$\omega_L = \frac{\vec{\mu} \cdot \vec{B}(\vec{r}_d)}{\hbar} \quad , \tag{3.4}$$

with the position vector $\vec{r}_d$ of the trap minimum. All interactions of atoms and magnetic field, which occur in a bandwidth below this frequency can be considered adiabatic.

To describe the quantum evolution of the particles in a confinement provided by the atom chip, a simplification is helpful. Therefore, in order to describe energy and behavior of the atoms, an approximation to the harmonic potential is often assumed. Close to the minimum of the chip, the effective potential can be well described by a paraboloid, resulting in the Hamiltonian

$$\mathcal{H} = -\frac{\hbar^2}{2m}\Delta + V(\vec{r}) \quad \text{, with} \tag{3.5}$$

$$V(\vec{r}) = \frac{m}{2}(\omega_x^2 x^2 + \omega_y^2 y^2 + \omega_z^2 z^2) - mgx \tag{3.6}$$

The quantities ω_i are referred to as *trap frequencies.*

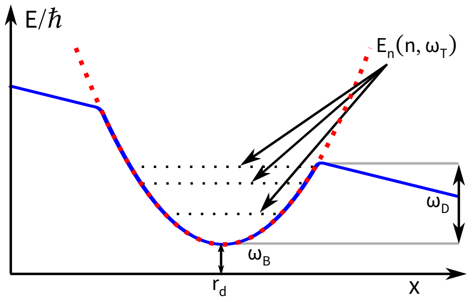

FIGURE 3.3.: 1D Harmonic approximation of a magnetic chip trap with gravity in x direction and bias and offset fields. Close to the trap minimum, the potential is assumed to be a parabola proportional to the squared trap frequency ω_T. The position of the minimum, r_d, is determined by the strength of the magnetic bias field. The trap bottom ω_B is proportional to the minimal energy of the trapping potential, the trap depth ω_D corresponds to the maximal energy of a trappable particle.

In the configurations employed in this work, two of these frequencies are usually of almost the same value, while the third is significantly smaller. The Eigenstates E_n of the harmonic trap allow for dipole oscillations with multiples of the respective trap frequencies.

Due to the conductor configuration, there exists an upper limit of the harmonic approximation (figure 3.3), as to the deviation of the real potential from the parabolic form. This energy is usually referred to as *trap depth* and expressed with a corresponding frequency ω_D.

The position vector of the trap minimum is $\vec{r}_d$. It depends normally on the magnetic field shape and the external gravity potential. In terms of frequency, the potential minimum is referred to as the *trap bottom* $\omega_B = V(\vec{r}_d)/\hbar$. Its value can be estimated via numerical simulations.

With the same simulations, one obtains the trap frequencies ω_i, for convenience, their geometric mean $\omega_T = \left(\omega_x\,\omega_y\,\omega_z\right)^{1/3}$ can be used to calculate with a single number.

As good rule of thumb, the harmonic approximation for a single particle is valid, as long as its energy does not exceed a state with a quantum number n, satisfying [72]

$$n \leq \frac{\omega_L}{\omega_T} \quad . \tag{3.7}$$

Likewise, the validity of the harmonic approximation can be considered to be good, if the fraction of LARMOR-frequency and trap frequency is large, therefore showing adiabatic behavior in the trap.

In microgravity, ω_B and ω_L have the same value. Due to gravitational distortion of the potential on ground, however, the energy level of the trap bottom differs from the magnetic field minimum. Therefore, ω_B is the better value to determine adiabaticity for the given trap. However, the calculation of ω_L is much easier, and usually a good orientation value to estimate adiabaticity criteria and chip loss mechanisms[11].

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[11] ref.: section 3.3

3.2.2. Trapped BOSE-EINSTEIN condensates

With bosonic atom gases, it is possible to achieve a macroscopic occupation of the ground state of a trapped ensemble. This macroscopic population results in the formation of a BOSE-EINSTEIN condensate (BEC). In this state, the inter-particle interactions become important and the standard SCHRÖDINGER-Hamiltonian is corrected by an interaction term:

$$\mathcal{H}_{\mathrm{GPE}} = -\frac{\hbar^2}{2m}\Delta + V(\vec{r}) + g\left|\psi(\vec{r})\right|^2 \quad \text{with} \quad g = \frac{4\pi\hbar^2 a_s}{m}, \tag{3.8}$$

with the particle mass m and the inter-particle scattering length a_s. The resulting operator leads to the GROSS-PITAEVSKII-equation (GPE) [73]:

$$i\hbar\frac{\partial\psi(\vec{r},t)}{\partial t} = \left(-\frac{\hbar^2}{2m}\Delta + V(\vec{r}) + g\left|\psi(\vec{r},t)\right|^2\right)\psi(\vec{r},t), \tag{3.9}$$

which is suitable to describe the energy states of the condensate with a common wave function for all participating particles. While the full evaluation of equation 3.9 is usually to be obtained numerically, it is possible to approximate the cloud behavior in static traps by neglecting the kinetic energy, if the other two terms are much bigger in their contribution. This is the case for confined BEC, like in the chip traps considered here. In the resulting time independent GPE, the chemical potential μ then replaces the energy eigenvalue of the SCHRÖDINGER case. This is called the *Thomas-Fermi-approximation*, yielding [74, sec. 6.2]

$$\Psi(\vec{r},0) = \sqrt{\frac{\mu - V(\vec{r})}{g}} \quad \text{with} \quad \mu = \left(\frac{15\cdot N\cdot a_s}{\bar{a}}\right)^{2/5}\frac{\hbar\omega_T}{2} \quad , \quad \bar{a} = \sqrt{\frac{\hbar}{m\omega_T}} \tag{3.10}$$

Given this initial conditions, one can employ a formalism called *scaling approach* [75], which yields easily calculable cloud radii and a good approximation of the isotropic time evolution of a released BEC, modeled by the trapping frequencies and a center of mass, which behaves like a newtonian particle. Following its formalism, it is possible to obtain an analytical expression of the time evolution of a trapped BEC after an adiabatic release from a harmonic trap.

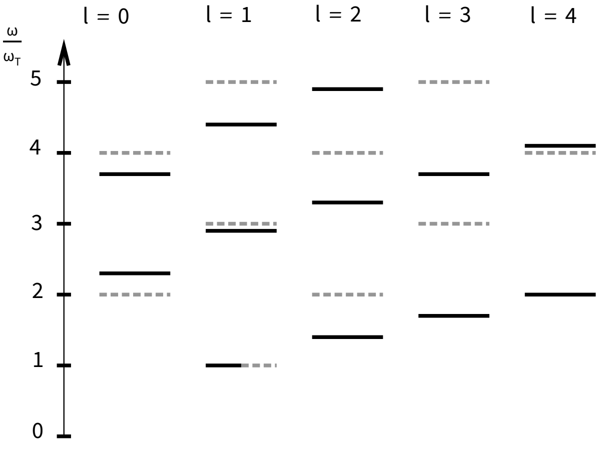

FIGURE 3.4.: Eigenenergies of a BEC in an isotropic harmonic trap for the first few iterations of n and l (solid lines). One can clearly see the deviation from energy levels for ideal gases without interaction (dashed lines). Especially the newly occurring energy modes between ω_T and $2\omega_T$ are to be considered in order to avoid excitation of the BEC. (Adapted from [74, p. 200])

Furthermore, the reduced GPE of equation 3.10, paired with the scaling approach gives rise to the description of inner dynamics of the BEC. Due to the interaction of the condensate, there are new energy states, which differ from a classical harmonic oscillator scaling. They can be described figuratively as internal vibrational energy states based on the BEC features resembling those of a super-fluid. They have been introduced as *collective excitations* [76]. Depending on trap geometry and shape, different dispersion relations apply.

For example, assuming an isotropic harmonic trap with frequency ω_T, the dispersion relation of the BEC yields [76]:

$$\omega = \omega_T \sqrt{2n^2 + 2nl + 3n + l} \tag{3.11}$$

with integer quantum numbers (n, l).

The spectrum of possible trap Eigenenergies therefore differs for a BEC in comparison to a thermal cloud, as depicted in figure 3.4. The additional states between the trap frequency ω_T and its second harmonic illustrate the heightened sensitivity of BECs to excitation in comparison to thermal clouds. This is, apart from the obvious sensitivity of ultra-cold atomic clouds, one of the reasons why BECs are considered an ideal test body for measurements for disturbance effects from the current sources of this work.

3.2.3. Anharmonic traps

While it is relatively easy to obtain harmonic traps in macroscopic laboratory experiments, the structures of the chip intrinsically result in deviations from the perfect harmonic trap shape, especially close to the chips surface. These deviations can be modeled with higher order polynomials, with characteristic parameters L_3 and L_4, which are usually sufficient to model the trap shape.

$$V(x) = \frac{m}{2}\omega^2 x^2 + \frac{m}{3 \cdot L_3}\omega^3 x^3 + \frac{m}{4 \cdot L_4}\omega^4 x^4 \tag{3.12}$$

The anharmonicities, if not negligible in their size, have drastic consequences for the calculation of the BEC dynamics. The scaling approach fails to include for non-harmonic distortions and can therefore not be applied. Hence, a full numerical treatment of the GPE is necessary, which is much more demanding in terms of calculation time and preparation.

Furthermore, the cloud dynamics differ from the separable case of dipole oscillations and can be problematic when releasing the BEC at a certain time of the oscillation period. Due to the deviation from the harmonic trap, the center of mass motion, which used to be a classical trajectory, is coupled to the collective excitations, thereby complicating the evaluation of the dynamics after release. The current model for the QUANTUS experiments is still a topic of intense theoretical research [59].

3.2.4. Creation of magnetic fields with wire tracks and coils

A magnetic field in a closed loop conductor is created according to the BIOT-SAVART-law [77, sec. 3.2.5]

$$\vec{B}(\vec{r}) = \frac{\mu_0}{4\pi} \int_V \vec{j}(\vec{r}') \times \frac{\vec{r} - \vec{r}'}{\left|\vec{r} - \vec{r}'\right|^3} . \tag{3.13}$$

This simplifies for an infinitesimal thin wire in vacuum to [78]

$$B(z) = \frac{\mu_0}{2\pi}\frac{I}{z} \qquad \frac{\partial B(z)}{\partial z} = -\frac{\mu_0}{2\pi}\frac{I}{z^2} \qquad \frac{\partial^2 B(z)}{\partial z^2} = \frac{\mu_0}{\pi}\frac{I}{z^3} . \tag{3.14}$$

If one now superimposes a homogeneous constant magnetic bias field B_0, one will find that this field vanishes on a line parallel to the wire, with the distance [78]

$$d = \frac{\mu_0}{2\pi}\frac{I}{B_0} \tag{3.15}$$

Using these simple equations in the first approach and detailed numerical calculations with equation 3.13, a lot of possible trap configurations and even interferometry schemes have been derived and present an own field of scientific research. A more detailed treatment of the derivation and trap configurations is given in [79, chap. 3].

In general, the fields of chip traps can be subject to perturbations, e.g. by magnetizable materials in the vacuum chamber or eddy currents due to temporal varying fields. Thus, the combined magnetic field is not necessarily always directly proportional to the current flow. When constructing chip mounts and chambers, this has to be considered. However, for the sake of simplicity and with the experience of a working QUANTUS-2 setup, where these complications are suppressed to a high degree, we will neglect this fact in the following, as it is not a subject of consideration in the current driver design, which focuses on current control only.

While there are atom chips capable of creating a whole cooling sequence with wire structures alone [40], the employed currents[12] are not yet feasible for battery driven, compact electronics, since the current output of the batteries is limited. Therefore, the QUANTUS-apparatuses need three external coil pairs in HELMHOLTZ-configuration, to add homogeneous magnetic fields to the chip, forming trapping potentials with tunable minima.

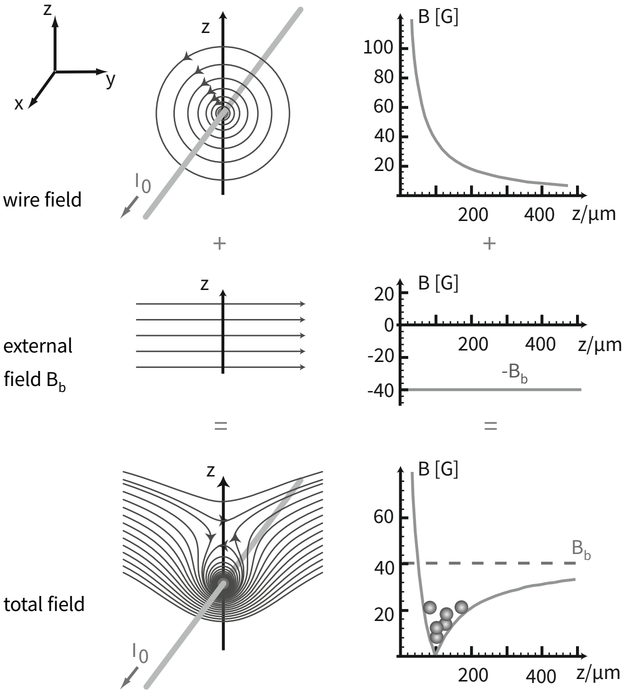

FIGURE 3.5.: Creation of a 2D magnetic trap with a wire and an external field. The left column shows magnetic field lines, while the right column presents magnetic field amplitudes. The overlay of the two fields creates a confining magnetic potential. (Adapted from [78].)

3.2.5. Common chip structures for trapping of neutral atoms

To complete all cooling steps to achieve BECs, three geometries on the Chip are employed. They originate in from a simple double crossing on a chip, forming a letter »H«. Depending on the directions of the current flow and the configuration of offset fields, it can provide two elementary magnetic field configurations – a quadrupole and a harmonic trap potential (figure 3.6).

Generally, for the functionality of atom chip structures, it is not important if they consist of separate wires or a galvanically connected structure. However, the latter option does have certain advantages. First of all, the manufacturing of a single layer of connected conductors is much easier than several separated wires. Moreover, a connected double crossing can be used for a multitude of trap geometries with a single current driver only by changing external connections (figure 3.6, right column), which reduces the amount of necessary hardware, thus is more feasible for compact apparatuses like MAIUS-1.

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[12] The offset and bias fields demand for currents, which easily exceed 100 A

Despite the convenience of the production, a galvanic connection of wires poses an important restriction to the current sources. As the current flow must be distinct from one point of the chip to the other, it has to be ensured, that the employed current sources have no galvanic connection whatsoever outside of the chip structures. Especially the grounding of the chip has to be sophisticated in order to prevent ground loops that would disturb the current flow.

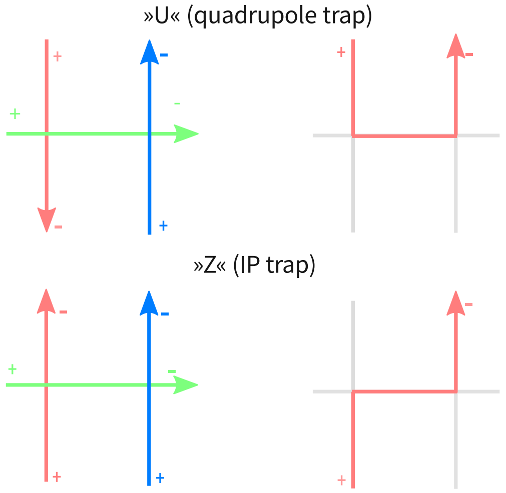

FIGURE 3.6.: Current flow through a »H« structure. Each color stands for a galvanically isolated current source. For galvanically connected wires, the three current sources in the left double crossing structure can be replaced by a single one, to form a current flow of a »U« shape for quadrupole fields, or a »Z« shape for Ioffe-Pritchard traps. Both trap types are defined by the direction of current through the »H« and configuration of external fields.

For all QUANTUS experiments, the usage of several galvanically connected structures for each chip layer had been intended. However, since until now only one structure per chip layer has been used in QUANTUS-2, this scheme has been inherited by the MAIUS-1 mission to ensure comparable trap setups. The circuitry presented in this work, however, allows for the full account of the possible trap combinations, even with several galvanically connected structures.

Quadrupole field - laser cooling

If one chooses the current flow directions in the »H« double crossing to be antisymmetric, with the additional condition of $|I_2| = |I_3| = |I_1/2|$ [79], the magnetic field around the trap minimum can be linearly approximated via it's gradient, forming a quadrupole shape, with vanishing field in the origin [58] (figure 3.7):

$$\vec{B}(\vec{r}) = \left(x \cdot \frac{\partial B}{\partial x}, \; y \cdot \frac{\partial B}{\partial y}, \; -2z \cdot \frac{\partial B}{\partial z} \right) \qquad (3.16)$$

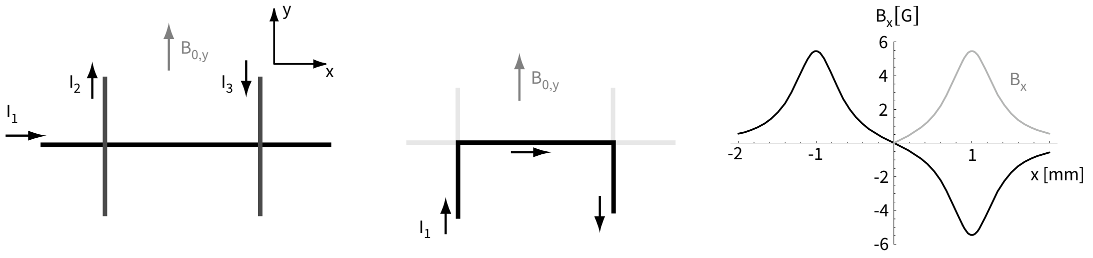

FIGURE 3.7.: Magnetic fields created by an »U« shape. The anti-symmetrical current flow results in a trap center with a vanishing field in the center, and approximated quadrupole field surrounding. The gray curve progression is proportional to the experienced potential for an atom inside a magneto-optical trap. I_1=2 A, B_0=1 mT (adapted from [79])

The resulting high gradients close to the minimum are ideally suited to be employed in a magneto-optical trapping scheme (section 3.1.1). Alternatively, one can employ a »U« shaped connection, when using only one current source.

It is also possible to trap atoms only magnetically in the quadrupole trap, but due to the degeneracy of states in the trap minimum, where the magnetic field vanishes, the trapped particles can undergo spin-flip transitions into magnetically untrapped states, therefore would be lost for further manipulation. Although this is negligible for sufficiently high ensemble temperatures, the trapping close to the chip surface leads quickly into regimes, where losses are occurring [58], which makes it unsuitable for BEC experiments. However, it is a very useful tool to lower temperatures of magnetically trapped ensembles in a different experimental setup, e.g. prior to optical evaporation [80].

Ioffe-Pritchard type - magnetic trapping

Starting again from a »H« double crossing, a symmetrical current flow enables a magnetic field configuration that resembles an IOFFE-PRITCHARD-type potential [69]. It has a non-vanishing trap minimum in the center (figure 3.8), if an additional offset field $B_{0,x}$ is applied. The potential is formulated as following [78]:

$$\vec{B}(\vec{r}) = B_{0,x}\begin{pmatrix}1\\0\\0\end{pmatrix} + B'\begin{pmatrix}0\\-y\\z\end{pmatrix} + \frac{B''}{2}\begin{pmatrix}x^2-\frac{1}{2}(y^2+z^2)\\-xy\\-xz\end{pmatrix} \quad . \tag{3.17}$$

It can also be well approximated by a harmonic trap formalism (subsection 3.2.1) if treated close to the trap center. It is ideally suited for pure magnetic trapping and both evaporation and BEC-confinement after condensation. Because the potential value does not vanish in contrast to the quadrupole trap of the »U«, spin-flip losses can be avoided.

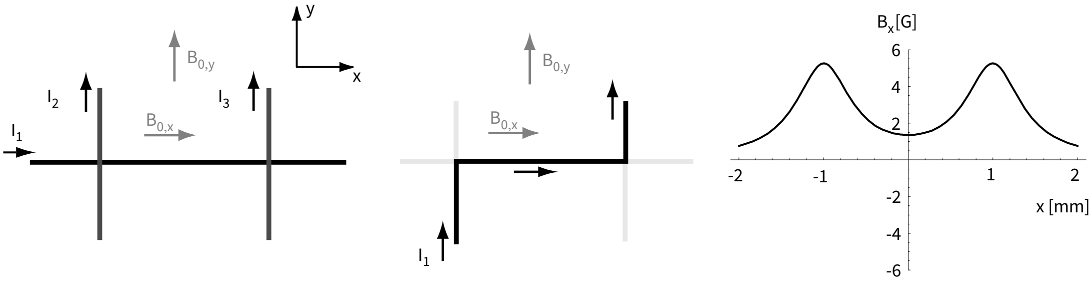

FIGURE 3.8.: magnetic fields created by a Z shape. The trap has a non-zero minimum in the center between the vertical wires. This can be achieved, as well as a linearization of the potential, if an additional bias field is used. I_1=2 A, B_0=1 mT. (adapted from [79])

The IOFFE-PRITCHARD-trap is used to confine and evaporatively cool atomic ensembles until BEC formation. Furthermore, it is suited to confine, transport and release already condensed ensembles.

3.3. Fundamental and technical limitations of atom chip traps

Completing the theoretical treatment of atom-chip-based BEC sources, a short glance at the specific difficulties regarding chips as a source of magnetic fields should be thrown. The proximity of the atomic ensembles to the chip surface, which itself is not only heterogeneous of material, but also has a relatively high temperature while conducting high amounts of current, gives rise for unique effects regarding magnetic trapping. From the several disturbance effects described in the literature (e.g.[72] and [81]), most depend on the distance d to the chip surface.

For a typical sequence used in the QUANTUS-missions, the atoms are located in the intermediate distance to the chip ($100\,\mu\text{m} \le d \le 1\,\text{mm}$)[22], so that near-field influences, such as CASIMIR-

POLDER-interaction, black body radiation[13], or spin-flips induced by shot-noise of the chip currents can be neglected. We will refer to [83] as a reference for these effects.

For the MAIUS-1 chip trap, there are three basic mechanisms, which mediate negative influence on trapped atomic ensembles in intermediate distance to the chip: spin-flips, heating and decoherence. They play an important role for the quality and sustainability of BEC ensembles. The physical effects causing the disturbances can be divided in fundamental limits, such as the thermal noise in the conductor, or resonant heating at specific frequencies caused by technical current noise. We will briefly introduce the most dominant effects relevant for the work in QUANTUS. They are described in more detail in [72] and [84].

3.3.1. Spin-flips

Generally, only a subset of an atom's hyperfine states are low-field seekers, and thus trappable in magnetic traps. Hence, if a change between states occurs, atoms can leave a former confining potential and leave the trap (figure 3.9). Typical processes leading to such losses are spin-flips, which in our case can occur spontaneously or can be driven by current noise.

Spontaneous spin-flip losses

A general phenomenon of magnetic traps are non-adiabatic MAJORANA-spin-flips [85]. These statistical changes in the spin value occur if neighboring hyperfine energy substates are degenerate or very close to each other and can change an atom from a low-field seeker to a high-field seeker which can not be trapped by magnetic traps. In first order, these flips are circumvented by employing a field with a non-zero minimum, such as the IOFFE-PRITCHARD-trap (IPT). Secondly, the adiabaticity criterion $\omega_L \gg \omega_T$ has to be fulfilled.

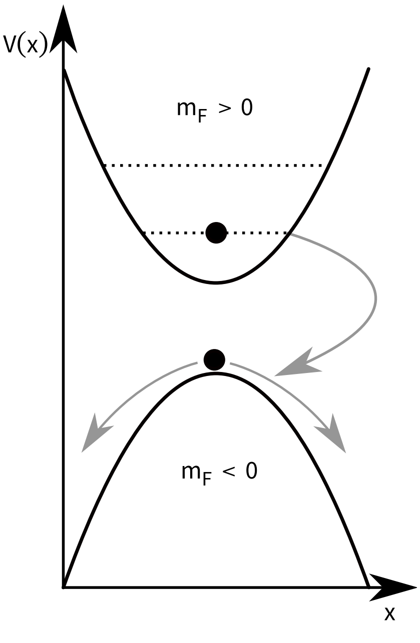

FIGURE 3.9.: Spin-flips in harmonic traps. Due to the induced or spontaneous change in an untrappable magnetic sub-state, formerly trapped atoms are lost.

For an experimental setup such as MAIUS-1, the LARMOR-frequency in a magnetic trap is simply determined by the offset field of the IPT, which can be estimated with the ZEEMAN-splitting energy of the magnetic sub-states of 87Rb (0.7 MHz/G) [67] and the offset-coil gauge factor 2.5 G/A, for a current of I_x:

$$\omega_L \approx 2 \cdot I_x \cdot 0.7\,\mathrm{MHz\,G^{-1}} \cdot 2.5\,\mathrm{G\,A^{-1}} \quad , \tag{3.18}$$

In a typical sequence as in section 3.1, the value of ω_L exceeds typical trap frequencies by three orders of magnitude, therefore the amount of MAJORANA losses can be neglected, as long as an offset field is present.

JOHNSON-NYQUIST-noise

In addition to the omnipresent, but negligible black body electromagnetic radiation due to the temperature of the chip substrate, the thermal motion of the charged particles within the

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[13] For precision atom interferometry, however, there is strong indication, that black body radiation from a chip surface can in fact cause phase distortions in the interferometer even at higher distances [82].

conducting chip circuits, which are usually at room temperature (ϑ=300 K), cause current flow, and, hence, magnetic field fluctuations. This effect is known as JOHNSON-NYQUIST-noise [86]. For a uniform conductor of resistance R and Temperature ϑ, the current noise spectral density, in a given bandwidth $\Delta\nu$ is

$$\mathcal{I}(\vartheta, \Delta\nu) = \sqrt{\frac{4k_\mathrm{B}\vartheta\Delta\nu}{R}} \quad . \tag{3.19}$$

The power spectral density of the magnetic JOHNSON-NYQUIST-noise for an atom of distance d to an atom chip conductor of temperature T, assuming a specific resistance ρ of the circuits material, can be calculated as follows, given the case that the radiation wavelength $\lambda = \omega/c \ll d$ [72, eq. 8]:

$$S_{\alpha\beta}(\omega) = \frac{{\mu_0}^2 k_\mathrm{B}\vartheta}{16\pi\rho}\frac{\mathfrak{s}_{\alpha\beta}}{d}\left[1 + \frac{2d^3}{3\delta(|\omega|)^3}\right]^{-1} \quad , \tag{3.20}$$

with the skin depth $\delta(|\omega|) = \sqrt{\rho/\mu_0\omega}$ and a geometric tensor $\mathfrak{s}_{\alpha\beta} = \mathrm{diag}(1/2, 1/2, 1)$, having a distinguished axis in direction of the normal of the surface. The term in the brackets is variable, depending on the chip's geometry, but not always obtainable analytically. It is given here for a planar surface. Details to the derivation of this formula can be found in [16].

With the additional simplification of a non degenerate cloud[14] and $d \ll \delta(\omega_L)$[15] the JOHNSON-NYQUIST-noise is causing spin-flips of an atomic cloud, with a loss rate of the order [72]:

$$\Gamma_{i \to f} \sim 100\,\mathrm{s}^{-1}\frac{(\mu/\mu_B)^2(\vartheta/300\,\mathrm{K})}{(\rho/\rho_c)(d/1\,\mu\mathrm{m})} \quad . \tag{3.21}$$

Here, ρ_c is the specific resistance of copper and μ_B is BOHR's magneton.

Although not explicitly visible in the upper estimation, the loss rates do vary with the LARMOR-frequency, as well as they depend on the substrate material and geometrical structure [87]. In the typical distances of $d \sim 500\,\mu\mathrm{m}$, this effect decreases below $1\,\mathrm{s}^{-1}$, but remains the predominant limitation of the distance to the atom chip, especially if one deals with BECs, which, due to their energy splitting[16], should show slightly increasing loss rates compared to thermal clouds.

In detailed analysis, it has been found that the magnetic noise increases with the amount of conducting material on the chip surface. Therefore, diameter reduction and economic use of conducting structures is advisable for chip designs. Another way to minimize JOHNSON-NYQUIST noise is to lower the temperature of the chip or employ superconducting chips [88]. Furthermore, the use of silicon as both substrate and conductor seems to be favorable in comparison to gold [87].

Technical current noise

The most variable and usually dominating source causing magnetic field noise of atom chip traps is the noise introduced by the current sources for magnetic field creation.

In order to quantify the impact of this technical noise, it is necessary to obtain a spectral noise density $S_I(\omega)$ for the specific current source and structure, usually through measurements (ref. appendix A.3).

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[14] For a BEC, the transition $k_\mathrm{B}\vartheta \longrightarrow \hbar\omega(1 - \exp[-\hbar\omega_L/k_\mathrm{B}\vartheta])^{-1}$ has to be used. Additional quantum effects, s.a. spin wave scattering and collective excitations can decrease the lifetime even further.

[15] $\delta(\omega_L)$ is of the order 10^4 for our experimental values

[16] ref.: section 3.2.2

The magnetic field fluctuations drive spin-flips into magnetically untrapped states, analog to the thermal near-field noise. The noise spectrum is then normalized with the shot noise limit: $S_{SH} = 2qI$. If we now consider a simple wire, the upper estimate for spin-flips is evaluated at the LARMOR-frequency, scaled with the shot noise. The noise spectrum of the magnetic field of the wire is estimated to be [72]:

$$S_{\mathrm{B}}(\omega_L) = \frac{q\,\mu_0\,I}{4\pi\,d^2}\frac{S_{\mathrm{I}}(\omega_L)}{S_{\mathrm{SH}}} \quad , \tag{3.22}$$

resulting in a spin-flip rate of the order

$$\Gamma_{i\rightarrow f} \sim 1\,\mathrm{s}^{-1}\frac{(\mu/\mu_B)^2}{(d/1\,\mu\mathrm{m})^2}\frac{S_{\mathrm{I}}(\omega_L)}{S_{\mathrm{SH}}}\frac{I}{1\,\mathrm{A}} \quad . \tag{3.23}$$

In an experimental situation, with various values for ω_L, S_I is not always accessible for direct measurement (section 3.3.5). Thus, it is useful to equip the current drivers with a low pass-filter outside of the measurement bandwidth of noise, if compatible with the experimental sequence intended[17].

3.3.2. Heating

The effect of heating in atomic traps, with trap states of lower energy difference than substates of the atom, does not usually result in particle loss. However, by transferring energy to the ensemble, one can excite higher trap eigenstates, which contributes to either increased ensemble temperature, or even a transformation of a BEC back to a thermal cloud. For a finite trap depth, this also might mitigate losses from high energy particles.

Heating is usually the predominant source of disturbance in an experimental sequence such as described in section 3.1. The heating introduced by the technical current noise in harmonic traps can be described as a force fluctuation due to the displacement of the trap minimum (figure 3.10) or the trap's curvature, which corresponds to the »spring constant« of the harmonic oscillator model (figure 3.11).

Generally, higher trap frequencies with strong confinement give rise to stronger heating, so that these effects become important in close proximity to the chip, which makes a fast transfer into distant, shallow traps generally favorable for long trap lifetimes.

Technical current noise

If we again consider an atomic ensemble trapped with a single wire and a displacement of the minimum with the bias field B_b, the force spectrum of the heating rate is [81]

$$S_{\mathrm{F}}(\omega) = \left(\frac{\mu_0 M\omega^2}{2\pi B_b}\right)^2 S_{\mathrm{I}}(\omega) \quad . \tag{3.24}$$

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[17] In fact, the use of ferrite cores and chokes between the current drivers and the atom chips has been a necessity in the QUANTUS experiments using commercial current drivers, as they did suffer from additional losses from this effect.

The resulting approximation for the loss rate from the displacement of the trap minimum is considerably high [81]:

$$\Gamma_{0\rightarrow1} \sim 2.7\,\mathrm{s}^{-1}\cdot\left(M/1\,\mathrm{amu}\right)\left(\omega_T/2\pi\cdot100\,\mathrm{kHz}\right)^3\,\frac{S_\mathrm{I}(\omega_T)}{S_\mathrm{SH}\cdot\left(B_b/1\,\mathrm{G}\right)^2}\,. \tag{3.25}$$

Usually, the fluctuations of the trap minimum results from the current noise of the trapping wire and the coils generating the Bias field B_b. It is possible to reduce these fluctuations to a minimum, if the noise of the currents I through the wire and the bias coils is common, e.g. by employing a series connection with a single current driver.

However, even for common mode fluctuations, the curvature of the potential might still be disturbed, thereby altering the trap frequency. This enables for a parametric resonance on the second harmonic [72]:

$$\Gamma_{0\rightarrow2} \sim 3\cdot10^{-8}\,\mathrm{s}^{-1}\frac{\left(\omega_T/(2\pi\,100\,\mathrm{kHz})\right)^2}{(I/1\,\mathrm{A})^2}\,\frac{S_\mathrm{I}(2\omega_T)}{S_\mathrm{SH}}\,. \tag{3.26}$$

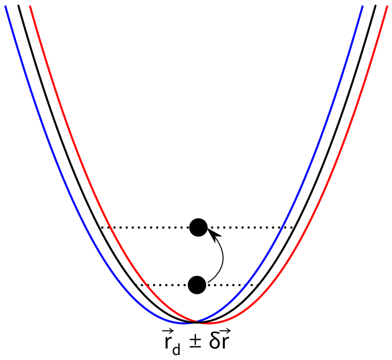

FIGURE 3.10.: Schematic of the heating due to fluctuation of the trap minimum. The displacement adds potential energy to the ensemble that can excite higher trap eigenstates.

JOHNSON-NYQUIST-noise

For trapped ensembles, it is also possible to derive a heating influence due to the JOHNSON-NYQUIST noise, resulting from the displacement of the trap minimum. It is a resonant process, depending on the trap frequency and the confinement in the trap [81]:

$$\Gamma_{0\rightarrow1} \sim 0.7\,\mathrm{s}^{-1}\cdot\frac{\left(\mu/\mu_B\right)^2\left(\vartheta_\mathrm{Chip}/300\,\mathrm{K}\right)}{\left(M/1\,\mathrm{amu}\right)\left(\omega_T/2\pi\,100\,\mathrm{kHz}\right)\left(\rho/\rho_c\right)\left(d/1\,\mu\mathrm{m}\right)^3}\,. \tag{3.27}$$

The contribution of the latter two loss rates is, however, very small, thus not problematic for traps with $d \gg 100\,\mu\mathrm{m}$.

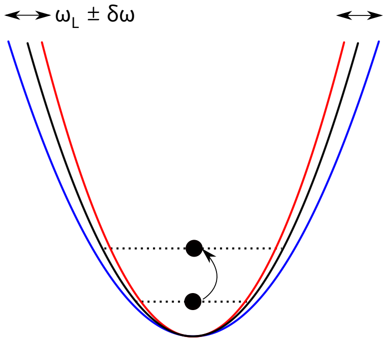

FIGURE 3.11.: Schematic of the Heating due to fluctuation of the trap frequency. The fluctuation of the trap shape adds kinetic energy to the atomic ensemble which can change the eigenstate to higher quantum numbers.

3.3.3. Decoherence

If the shape of the trap potential is locally disturbed, this can affect the phase relation of several parts of the cloud, as well as lead to distortion of cloud shape and velocity distribution. As these properties may cause problems in operation and evaluation of atom interferometers, we will briefly cover two typical atom chip related decoherence effects.

Fragmentation due to conductor imperfections

As one can directly see from the BIOT-SAVART-law (equation 3.13), not just the value of I, but the charge distribution of $\vec{j}$ determines the magnetic field value and shape. Hence, not only the current control, but the quality and shape of wires has to be as precise as possible as variation of conductivity, width or height would change the charge density and thus directly influence the spacial shape and strength of the magnetic field.

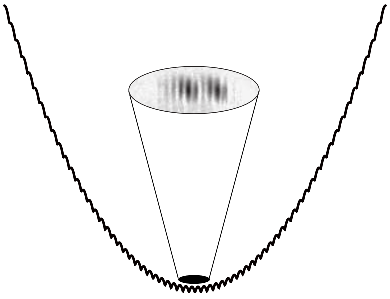

FIGURE 3.12.: BEC fragmentation by conductor imperfections. Due to changes in current density, the magnetic field close to the chip is distorted, thus fragmenting the trapped condensate. (Atom Picture extracted from [89])

In standard industrial processes of circuit board manufacturing, the material of the conductor, mostly gold or copper, is sputtered on the surface or grown in very fast galvanization steps. Therefore the conductor material is technically not bound in a homogeneous crystal structure, but forms microscopic drops, which function as accumulation centers for charges. This leads to small, local variances in the magnetic field value and thus the trap shape. Although relatively negligible in large distances to the conducting wire, these imperfections lead to displacement or fragmentation of atomic clouds [89], depending on the amount of roughness (figure 3.12).

Unfortunately, standard chip production techniques, which are commercially available, have not been proven suitable to achieve the smoothness and precision of manufactured chips according to the scientific needs of atom optics. Therefore, all chips for the QUANTUS missions have been fabricated by physicists[18] in special clean-room facilities, obeying a controlled production recipe extensively described in [90].

By optimizing this technique, a structure height of up to 13 μm with local roughness of not more than a few hundred nm can be achieved. Thus, by carefully observing the outcome of the fabrication process, irregularities due to structure of the conducting wires can be inhibited.

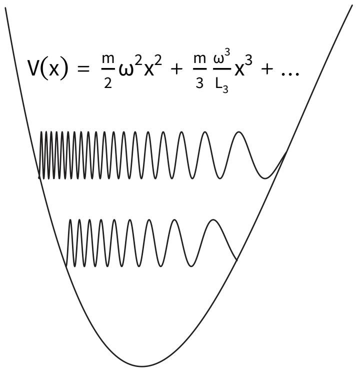

FIGURE 3.13.: Distortion of trap geometry by anharmonicities. The L_3 term in the potential couples internal states of the condensate with the expansion, thus distorting the cloud evolution after release.

Anharmonicities

Chip traps are usually not able to form perfect harmonic traps. Thus, trapped atomic ensembles can experience a disturbance due to anharmonicities, especially during transfer of a BEC from one trap position to another. These disturbances especially affect condensed ensembles, as they are susceptible even for very small potential changes. Energy transfers, e.g. heating, give rise to collective excitations, which are additionally altered in their frequencies due to the L_3 and L_4 contributions of the potential[19].

Depending on the value of the quantum numbers, the dynamics of the condensate cloud takes the shape of monopole, dipole and quadrupole oscillations. In contrast to the harmonic trap, the dynamics of the center of mass motion and the shape oscillations in an anharmonic trap are no longer decoupled, resulting in a non-isotropic expansion after trap release. Especially after a DKC procedure, the distortion a non-harmonic trap imprints on the BEC become immanent. While the residual kinetic energy can be minimized, it still has a great impact on the spacial distribution of the atoms and the velocity distribution that cause a change of shape in free time evolution [22, chap.6].

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[18] QUANTUS-1: Team of T. Hänsch at LMU Munich, QUANTUS-2: experimentalists in cooperation with J. Reichel at ENS Paris, MAIUS-1,2: experimentalists in facilities in Hanover and Brunswick.

[19] ref.:equation 3.12

The switching time and waveform of the structures participating in the DKC have a great impact on the efficiency of the collimation process. Thus, their optimization are an important task in suppressing distortions in the cloud shape and velocity distribution prior to interferometry measurements.

3.3.4. Comparison of disturbance rates

To give a direct comparison of the important disturbances of the specific atom chip, we will compare the presented equations for a model close to experimental parameters from QUANTUS-2. We consider a ^{87}Rb cloud in the final stages of evaporation ($|m_F = 2\rangle$) in a closely confined trap with $\omega_T = 2\pi \cdot 600\,\mathrm{Hz}$, $d = 250\,\mu\mathrm{m}$. The trap is consisting of a wire-structure on a non-conducting substrate of $\vartheta = 300\,\mathrm{K}$ with a current of $I = 2\,\mathrm{A}$, and a bias field of $B_b = 20\,\mathrm{G}$, with an offset field of $2\,\mathrm{G} \longrightarrow \omega_L = 1.4\,\mathrm{MHz}$. A uniform technical current noise level is assumed to be at a level of $\sqrt{S_I} = 1\,\mu\mathrm{A}/\sqrt{\mathrm{Hz}}$ for all frequencies, according to the datasheet of the QUANTUS-2 current drivers [17].

effect	equation	loss rate	scaling	improvement method
Technical current noise (spin-flips)	(3.23)	$6.2\,\mathrm{s}^{-1}$	$S_I(\omega_L)/d^2$	low-noise driver, distance to chip, low-pass choke
Technical current noise (heating, trap displacement)	(3.25)	$1.9\cdot10^{-1}\,\mathrm{s}^{-1}$	$\omega_T\cdot S_I(\omega_T)/d^2$	low-noise driver, correlation
Johnson-Nyquist noise (spin-flips)	(3.21)	$1.5\cdot10^{-1}\,\mathrm{s}^{-1}$	$\vartheta_{Chip}/\rho d^3$	little metal, distance to chip
Technical current noise (heating, curvature change)	(3.26)	$4.2\cdot10^{-7}\,\mathrm{s}^{-1}$	$\omega_T^2\cdot S_I(2\omega_T)/I^2$	low-noise driver
Johnson-Nyquist noise (heating, trap displacement)	(3.27)	$1.7\cdot10^{-8}\,\mathrm{s}^{-1}$	$\vartheta_{Chip}/\omega_T\rho d^3$	negligible

TABLE 3.1.: Estimation of loss and heating mechanisms, sorted by their impact in loss rate. Scaling formulas from [81]

The evaluation of the given loss rates clearly shows a dominant impact of technical noise as a source of disturbance for trapped atoms. Therefore it is mandatory to focus on a further reduction of technical noise for newly designed current sources. It is important to state, that these estimations are valid for thermal clouds and do not consider effects that a BEC would be prone to. However, to assess the impact of technical noise, the numbers are a good starting point. Furthermore, additional low pass chokes and the damping effect of the cables[20] are not considered, although they can damp higher frequency noise components. For a more accurate estimation, we shall review these equations later on, after obtaining more realistic values of the noise spectra from the new designs[21].

3.3.5. Frequency domains of technical noise impact

In order to evaluate the impact of a noise source on a measurement, one has to consider the spectral noise density at the characteristic frequencies of the experiment. Hence, we will shortly glance at the relevant frequency domains for the current driver designs for an experiment such as MAIUS-1.

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[20] see following section

[21] ref.: section 6.2.6

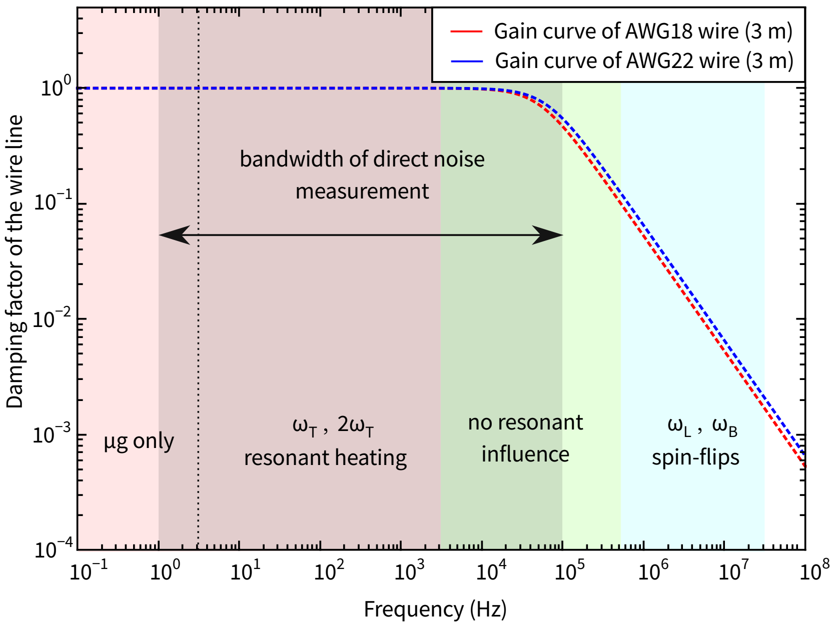

FIGURE 3.14.: Relevant frequency domains of current noise. The described loss mechanisms have distinct frequency ranges which leave a window of non-resonant influence of noise. Currently, only frequencies ≤ 100 kHz are accessible by direct measurement. However, the necessary long cable connections between current driver and atom chip cause additional noise damping, depending on their diameter, which reduces the expected impact of current noise at frequencies ≥ 100 kHz. The two dashed curves depict the gain figure of two standard cables used in MAIUS-1.

Figure 3.14 depicts the frequency spectrum from 0.1 Hz to 100 MHz. Derived from the experimental sequences of QUANTUS-2, the colored areas highlight the frequency span of important experimental quantities for noise analysis, whereas the grey area shows the frequency span which could be accessed in this thesis for direct noise measurement[22].

As the current sources of MAIUS-1 are connected to the experiment with high-current capable cables of significant length, the impedance of this structures, and the resulting damping for higher frequency noise components are also of importance in order to quantify the effective noise density reaching the chip structures[23]. Hence, the gain figures of a 1.5 m two wire cable are depicted in the graph as well (dashed curves). It is observable, that at this cable length, the current noise in the range of the LARMOR-frequency is already suppressed significantly.

The trap frequency of the magnetic traps reaches from sub-Hz up to 5 kHz (red area), while all frequencies ≤3 Hz are only employed in weightlessness due to the gravitational trap distortion. Within this frequency span, trapped ensembles are subject to (parametric) heating, which is determined almost exclusively by technical current noise. Therefore, the noise spectral density in this frequency span is of high interest for control and optimization and can be directly measured with high precision.

The current noise in the span from 5 to 500 kHz (green area) is usually not completely controlled by the current driver due to bandwidth limitation, but can be passively reduced by additional filtering, in order to suppress possible excessive noise peaks to a tolerable level[24]. The noise spectrum can be measured directly up to 100 kHz[25], and is damped above that frequency by

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[22] ref.: section 6.2

[23] ref.: appendix A.1

[24] Although there are no resonant loss processes, excessive noise can mitigate energy transfer to the atomic cloud which can be problematic at some point.

[25] ref.:section 6.2.1

the impedance of the cables.

In the frequency range from 500 kHz to 20 MHz (blue area), the trapped atoms are prone to spin-flip losses, which are caused by technical noise as well as by thermal effects. Unfortunately, the current noise in this frequency range is neither controllable by current drivers nor accessible for a precise direct noise measurement. However, as shown in figure 3.14, the impedance of the apparatus with the connecting wires delivers a damping for current noise of up to a factor 1000. By introducing additional filter elements in the conductor line, such as ferrite chokes, the damping can even be increased without impairing the current control, so that noise influence at this frequencies can usually be suppressed to a satisfactory amount.

3.4. Chip designs of the microgravity missions QUANTUS-2 and MAIUS-1

In this section, we will cover the essential chip properties of the QUANTUS-2 and MAIUS-1 missions, as both apparatuses share the same functional chip design. To realize an atom source with a chip-MOT directly loaded from a 2D$^+$-MOT, three different planar wire configurations have been stacked to create a multi-layer atom chip. The lowest layer uses a large number of copper wires of 0.7 mm diameter, and is integrated in the chip mount, while the other two layers are electroplated on AlN substrates, which are glued on top of each other.

This approach allows a very versatile shaping of magnetic fields for all purposes of the cooling process, as described in section 3.1.

The production process of these type of chips is described in [90]. The chips are manufactured of aluminum nitride (AlN) with gold wires on a layer of several nm of titanium. The subsequent chip layers and their function shall now be introduced as they have been characterized in QUANTUS-2, and differences to MAIUS will be mentioned, if necessary.

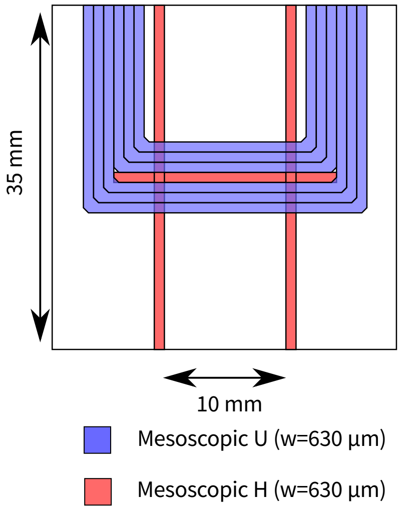

FIGURE 3.15.: Schematic of mesoscopic structures in QUANTUS-2. The blue wires show the sixfold U shape creating the quadrupole field. The »H« shape is used to transfer into the first magnetic trap after optical cooling and to transport the BEC into very shallow traps in microgravity. The numbers in the legend describe the width of the structures.

3.4.1. Mesoscopic Chip

The first layer of the atom chip consists of so-called mesoscopic structures [35] that present an ideal intermediate stage between macroscopic coil-based and microscopic chip traps (figure 3.15). They consist of 0.63 mm[26] thick, polymide-isolated wires, that are directly wound into the copper mount that carries the actual chips. With only 10 A of current flow trough the sixfold wound »U«, gradients of up to 20 G cm^{-1} can be achieved in the quadrupole trap. They are used to capture the cold atom beam loading the magneto-optical trap. The harmonic magnetic trap, which is formed by a single-wire »H«, which is used in a series chain of the three wires, employs currents up to 15 A. The mesoscopic »H« allows to create large traps of intermediate depth at a great distance to the chip, in order to allow for efficient transfer from optically cooled ensembles into pure magnetic traps.

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[26] This corresponds to AWG 22

Design alterations in MAIUS

The atom-chip design of QUANTUS-2 showed significant atom-loss during the transfer of the optical cooled atoms into the magnetic trap generated by the mesoscopic structures, as the magnetic field strength was not sufficiently high at the atoms' position. In order to enhance the trapping confinement in a farther distance to the surface, the MAIUS-chip doubled the windings of the »H« structures to surpass this limitation.

However, further improvement in the initial trapping in terms of transfer efficiency could not be demonstrated yet. Nevertheless, the employed currents could be reduced to a level below 10 A, therefore reducing the maximum current requirements to a more manageable value.

3.4.2. Base Chip

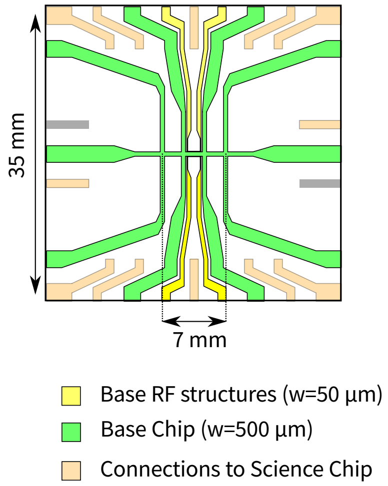

FIGURE 3.16.: Schematic of the Base Chip. The numbers in the legend show the minimum width of the specific structure. With currents up to 6 A, the Base Chip wires provide the baseline of magnetic fields for trapping and evaporation. The yellow RF structures are galvanically isolated and directly connected to RF sources, providing evaporation frequencies from 0.5 to MHz with an input power of up to 20W.

After the transfer into the mesoscopic trap, the atomic particles are transferred into a deeper, narrower trap potential and transported closer to the chip's surface, in order to allow for efficient evaporation. This task is provided by the base chip.

The Base Chip of QUANTUS-2 consists of two »H« gold structures of 500 µm width and 8 µm height [58], which are electroplated onto a titanium seed layer on a AlN substrate. The structures are all galvanically connected and bonded to the chip mount. Estimated by the quality of the bonds, maximum currents of 6 A are employed to create deep magnetic traps.

In order to have a controlled interaction between RF fields and atoms, the Base Chip harbors a waveguide structure to deliver the RF energy to the atoms in a near-field environment. This structure is employed for the evaporation and the adiabatic rapid passage and may be used in later applications for coherent splitting in possible trapped interferometer schemes [33].

However, as the impedance matching for the structures in vacuum is not optimized for any specific frequency, the efficiency is poor, thus relying on an input RF power of up to 2 W. The Base Chip rests in a Teflon® mount with ball pins that are bonded to the chip with wire bonds. Additionally to the employed structures, connection pads for the Science Chip on top of the base structure are added to this atom chip layer (figure 3.16).

Chip alterations in MAIUS

As a test for future developments in the next generation of chip experiments, several minor changes have been made in the MAIUS Base Chip design.

- A slightly thinner AlN substrate[27] has been used, therefore the relative distances of the chip layers have been altered.

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[27] Q-2: 800 µm, M-1: 635 µm

- The AlN substrates have been enlarged in order to incorporate a new method for connecting the circuits with the vacuum feedthrough: Instead of the Teflon® mount with ball pins, the chip was connected directly to the UHV throughput with wires that are glued to the chip, employing a conducting glue.[28]
- The connection between Base Chip and the Science Chip has been replaced by gold wires, which are attached via gap-welding. They support up to 10 A of current before deteriorating.
- The height of the chip's micro-structures could be increased from 8 to 10 µm[29], therefore enabling higher power handling due to the lower current densities.
- The positioning of the chips has been enhanced by introducing locating pins in the chip mount, as well as corresponding holes in the Base Chip.
- A simpler structure to deliver RF-magnetic fields has been introduced at the edge of the chip structures[30] to have the possibility of testing different evaporation schemes. However, its performance is not yet evaluated and is thus of no more concern for this thesis.

All of these modifications do not affect the basic operation principles of the Base Chip. To predict comparable performance of the chip configurations of QUANTUS-2 and MAIUS-1, numeric magnetic field simulations have been employed. While the theoretical circuit model of QUANTUS-2 has been verified with the help of calibration measurements in microgravity, the model of the MAIUS-1 multilayer chip does not yet contain this desired level of detail.

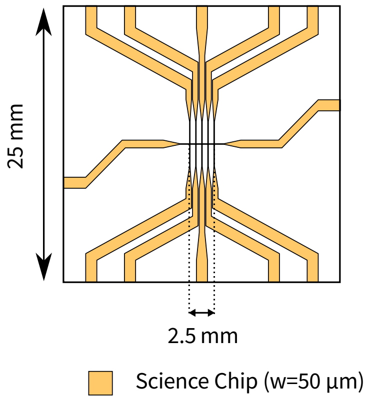

FIGURE 3.17.: Schematic of the Science Chip. All wires are galvanically connected at their intersections. The connection to the current drivers is realized via wire bonds to the Base Chip.

3.4.3. Science Chip

In order to achieve very close confinement in the magnetic traps, the last layer of the atom chip, the Science Chip, provides the smallest wire structures of only 50 µm minimum width (figure 3.17). Using up to 2 A of current, combined with the close proximity of the conducting structures to the atomic ensemble, very steep and deep traps can be created, as well as additional trap manipulation for coherent splitting and other potential techniques. For our purposes, only the feature of very steep traps has been employed and will be therefore treated.

The Science Chip is directly glued on the Base Chip and the conducting structures are connected to it with wire bonding. As an additional property, the Science Chip is coated with a transfer coating, which is glued on top of the wire structures with a vacuum capable glue. This enables for light reflection on the chip surface which can be utilized for a simplified *mirror-MOT* [31] trapping scheme.

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[28] `[Epotek H21D]`

[29] compare [58, pp. 51–52] with [31, p. 37]

[30] see figure 1.3

[31] ref.: section 3.1.1

Chip alterations in MAIUS

Apart from the bonding technique already mentioned in 3.4.2, there are no changes between both experiments as far as the Science Chip is concerned.

3.4.4. Employed chip structures

Due to the limitation of space in the experimental setup, not every chip structure could be equipped with a designated current driver. Although efforts have been made to increase the number of usable structures with only a few current drivers[32], the design proved to be insufficient to enable useful combination of chip structures. Therefore in the first approach of MAIUS-1, only a simplified combination of structures, each one galvanically isolated from the other, has been chosen to realize atomic source. In order to have comparable measurements, to transfer from QUANTUS-2 to MAIUS-1, both experiments use the same configuration (figure 3.18).

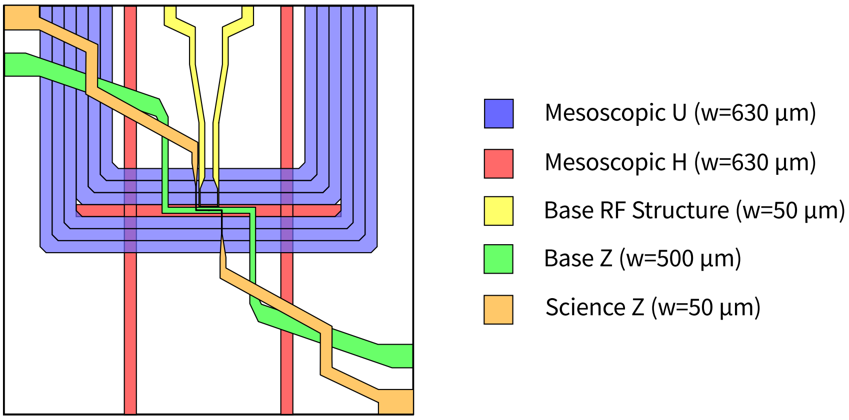

FIGURE 3.18.: Chip structures employed the QUANTUS-2 apparatus. The schematic only shows the wires in a 2D projection. In reality, the z-coordinates of the subsequent structures expand for about 4 mm from top to bottom, therefore the change of chip layers yields high efficiency as the atomic ensemble grows smaller. The width values in the legends refer to the narrowest parts of the structures.

The only difference between the two experiments is the capability of MAIUS to operate each of the mesoscopic »H« wires independently, while in QUANTUS-2, each wire carries the exact same current due to a racetrack configuration. Measured values of the MAIUS-1 structures, which have been used for design purposes, are documented in appendix B.4.

3.5. Scientific requirements on current drivers

After the discussion of the experimental steps and the atom chip operation, we will now review a typical experimental sequence[33] of QUANTUS-2, related to the requirements the current drivers of the apparatus have to fulfill.

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[32] ref: [58, p. 32]

[33] The sequence chosen has been performed in the QUANTUS-2 drop # 198 a, in order to create the effective 3D BEC temperature of 47 pK.

3.5.1. Current driver control sequence

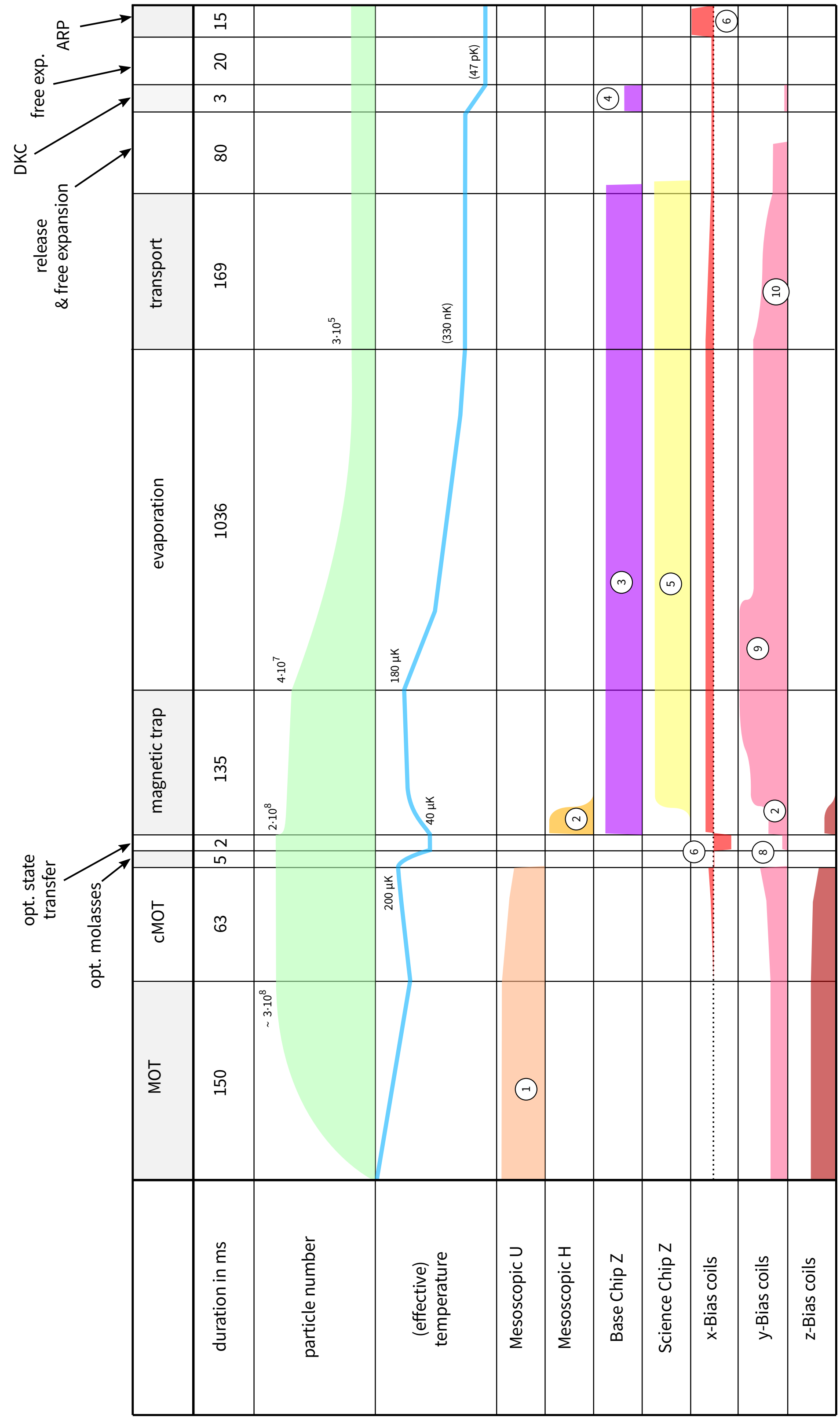

FIGURE 3.19.: Experimental sequence schematic of QUANTUS-2. Timing and amplitudes not to scale. The markings ①-⑨ show key performance areas for current drivers, which are elaborated in section 3.5 (performance data taken from [55] and [22], combined with timings from drop # 198a)

Figure 3.19 depicts a timeline of the experimental procedure with the particle number, the (effective) temperatures an the specific operational current drivers, with the current amplitude and ramp shape. The markings ①-⑨ indicate important procedures, which define scientific requirements as guidelines for the design process of the MAIUS-1 current drivers. They are divided for chip and coil structures, which each will obtain a designated current driver design.

3.5.2. Chip current drivers

① To realize magnetic field gradients of $20\,\mathrm{G\,m^{-1}}$, the mesoscopic U is driven with up to 10 A during the MOT phase of the experiment. Although this phase is relatively short in the shown optimized sequence, a significant amount of current flow needs to be maintained for several seconds during the initial characterization, thus the circuitry has to provide proper heat management and stability over this time period.

② The transfer into the magnetic trap is a critical part in the cooling procedure, which requires a quick buildup of a strong magnetic confinement field.

The magnetic field amplitudes for effective transfer demand for high currents in the mesoscopic H structures, which defines a minimum requirement of 10 A output current to the chip current sources.

③ During magnetic trapping, the Base Chip creates the basic potential to shape the trap.

With a current of 6 A and roughly 1.3 seconds of operation (which corresponds to 80 % cycle time), the Base Chip current driver sets the upper limit of the output power. A detailed calculation for MAIUS-1 will follow in section 4.2.3

④ The process of *delta-kick collimation* (DKC) is performed with current ramps through the chip structures, which allow for precise shaping of the employed magnetic field. Thus, the chip current driver requires the feature of arbitrary waveform shaping, which can be achieved, like in QUANTUS-2, with linear ramp approximation.

⑤ As described in section 3.3, magnetically confined atoms interact with disturbance effects of the trap potentials, whose impact decays with the distance of atoms to the conducting circuit.

The Science Chip, which is situated the closest to the atomic cloud requires the lowest current noise of all structures in the experiment, thus defining a requirement for the maximum current noise. For QUANTUS-2, the employed current driver noise level, according to the datasheet [17], is estimated to be $\leq 10^{-5} \cdot I_{\mathrm{max}} = 1\,\mu\mathrm{A}/\sqrt{\mathrm{Hz}}$, which defines the preliminary design goal[34] for MAIUS-1.

3.5.3. Coil current drivers

② The transfer into the magnetic trap is performed very far away from the chip, which requires a quickly buildup of a strong magnetic bias field.

As a result, the Y-coils have to be jumped to a high current amplitude in a relatively short amount of time, usually with a slope of roughly $1\,\mathrm{A\,ms^{-1}}$, which requires optimized current control, since the switching time for the Y-coils is limited by their inductance[35].

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[34] Detailed noise measurements with frequency decomposition are performed in section 3.3.4,

[35] ref.: section 4.2.5

⑥ The X-coils fulfill various functions, such as offset fields for the IPT, ZEEMAN-splitting for optical transfer and ARP. In the given laser configuration of the experiment, this demands for bipolar current driver operation for the experimental coils. The behavior of the current driver during polarity changes has to be observed carefully, if they feature crossover distortion.

During the optical state transfer, the bias coils have to provide a strong magnetic field with a significant current ramp slope of approximately 1.6 A in 1 ms to leave sufficient time for several transfer cycles. This defines the minimum ramp slope for the coil current drivers.

⑦ The ARP demands for a large ZEEMAN-splitting in order to allow for sufficient state separation in the avoided crossings. For this, currents up to 5 A are necessary. This puts the mimimal output current for the bias coils to this value.

⑧ During molasses, possible residual offset fields might occur. In order to compensate these static disturbances, small compensations must be reliably created by the coil drivers. Thus, a precise calibration of small currents close to zero, as well as bipolar operation are mandatory.

⑨ The Y-coils have the highest number of windings, thus also the highest inductivity. With their maximum current of 2.1 A, they set the benchmark for coil switching time. For M-1, this value needs to be achievable within 2 ms. Detailed analysis of this requirement will be conducted in section 4.2.5.

⑩ The trap transport and release is under large time constraints, as linear, adiabatic trap transport often exceeds available time scales under microgravity. With non-adiabatic transport schemes [70], trap transfers of much shorter timescales are possible. However, since the trap ramps have complex shapes, an arbitrary waveform of currents is a necessity. If linear approximated, a real-time capable current driver needs sufficient memory to store the ramp information.

The coils in QUANTUS-2 have been operated with the same current drivers as the atom chip circuits. Thus, to ensure consistency with the results presented here, the current noise stipulations for the chip current drivers also apply for the coil current drivers.

3.6. Summary

Atom Chips provide an excellent source concept for atom interferometry: They allow for small volumes for the experimental apparatus, yet very versatile trap configurations with a few simple wire structures. With additional bias coils and a RF-source, BECs of 10^5 atoms can be created with a 1 Hz cycle rate, which is a standing record for ^{87}Rb atom sources. Additionally, quickly switchable trap configurations allow for a delta kick collimation of atomic ensembles to a very low residual expansion velocity which makes them the ideal source for precision measurements.

Nevertheless, due to the proximity of the chip's surface and conducting structures to the atomic ensembles, atom chips can convey disturbance effects, such as spin-flips and heating towards trapped atoms. For a BOSE-EINSTEIN condensate (BEC), these effects can result in collective excitations or even a destruction of the condensed state.

For a setup such as QUANTUS-2, technical current noise in the bandwidth of the trap frequency is considered the dominant source that limits the lifetime of atomic traps, even if it is as low

Structure / Parameter	Atom Chip	Bias Coils
max. current output	10 A	± 5 A
direction	unipolar	bipolar
ramp capability	yes	yes
wave form	arbitrary wave form (linear approximation)	arbitrary wave form (linear approximation)
switching time	≤ 100 µs	≤ 2 ms
minimal slope (ramps)	$> 1\,\mathrm{A\,ms^{-1}}$	$\geq 1.6\,\mathrm{A\,ms^{-1}}$
current noise LSD	lower as in Q2 Driver ($1\,\mu\mathrm{A}/\sqrt{\mathrm{Hz}}$)	lower as in Q2 Driver ($1\,\mu\mathrm{A}/\sqrt{\mathrm{Hz}}$)
precision of current output	≤ 50 ppm	≤ 50 ppm

TABLE 3.2.: Specification sheet for new current driver designs, derived from the experimental sequence of QUANTUS-2 and the estimations of current noise loss rates.

as $1\,\mu\mathrm{A}/\sqrt{\mathrm{Hz}}$, as in previous experiments. Thus, the continuing reduction of current noise is a central task for the design of atom chip current drivers.

To allow for experimental sequences like performed in QUANTUS-2, several key parameters have to be met by the new current driver design. They are summarized in table 3.2.

CHAPTER 4

Technical requirements on current drivers in the MAIUS-1 mission

In the last chapter, we ended up with necessary scientific specifications for current drivers operating in cold atom sources. They were derived from the drop tower experiments performed in QUANTUS-2. These specifications can obviously be met already by existing technology, e.g. commercial current drivers. However, these devices do not comply with the specific technical requirements of the rocket integration in several respects. Firstly, the available space is much smaller than in laboratories, which makes the use of commercial current driver modules of a 19 inch rack size not feasible.

Moreover, the integration of current drivers into the infrastructure of the MAIUS-1 electronics module and the already finalized battery module, as well as the implementation into the software environment poses a challenge that no commercial current driver could meet. Although these aspects seem to be mere technical details, their combined impact on the design process is significant, as it demands for current driver designs, whose requirements are augmented by payload-specific items.

Initially, we will review some basic aspects of the module and interface system that is common to all MAIUS-1 electronic modules. Afterwards, specifics on the hardware requirements are discussed, to obtain key target values for the design process. Finally, the safety constraints are introduced, which are necessary to prevent accidental damage of the atom chip assembly. The inclusion of all these facts results in a complete design requirements list for the intended current driver designs.

4.1. Basic system infrastructure

At the beginning of the design process of the current drivers of the MAIUS-1 mission, most hardware interfaces and properties of the electronics had already been laid-out and had to be considered as design baseline for the circuit design phase.

The electronics platform » *Thijs' Binary Unit System*« (TBUS) responded to the demand of compact atom-optic experiments, which can be autonomously operated, without sacrificing the precision and versatility of standard, mostly analog, lab electronics. The drop-tower experiments already showed that full computer-based control of all experimental parameters is necessary in an environment, where direct interaction of operators and experiment is highly limited. Although several commercially available solutions for these demands had been already existing on the market, the combination of very small volume and high robustness without any curtailment in capability had not yet been achieved.

Fortunately, with funding of the German Aerospace Center (DLR), the project LASUS has been initialized. In this project, among other things, a highly integrated microelectronics framework, especially suited for microgravity, have been designed. Moreover, LASUS, does not only deliver hardware modules, but also aims on a complete, yet modular setup of devices with an easily operable software implementation on standard lab PCs.

Within LASUS, a variety of TBUS electronic modules for the control of BEC experiments have been created, except of the current controller for atom chips and bias coils. This section will mark out the necessary interface structures between modules and experimental control, as well as the structure of the current driver stack.

4.1.1. Module specifications

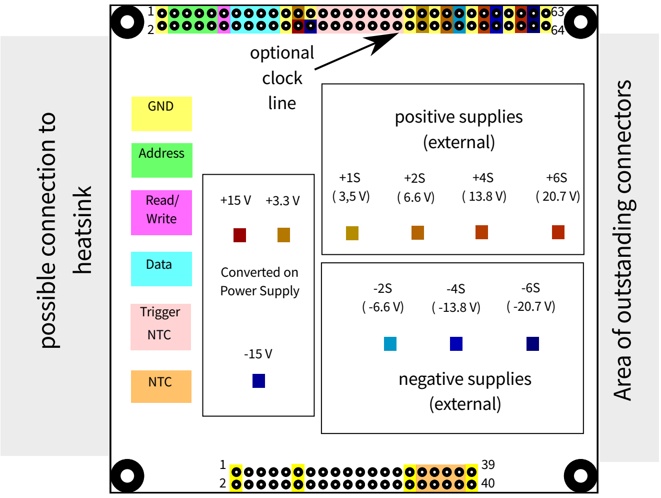

FIGURE 4.1.: Schematic of the TBUS modules (cards). Communication pins deliver a 8 bit data BUS, 13+1 real-time trigger lines, several supplies and temperature monitoring. Pin lines left white are distributed depending on the specific stack hardware. The number of battery cells (»S«) is attributed with a prefix (+,-) due to their connection to the common ground.

A uniform size of hardware boards (*cards*) ensures their compact structures and modularity. Their design is inspired by the industrial standard PC104 [91], but is not directly compatible with it. A standard TBUS card consists of a 100 × 100 mm sized PCB board, with maximum thickness of 2 mm, separated with 15 mm distance bolts, effectively creating a »height unit« of 17 mm (figure 4.1).

Two opposite edges of the boards harbor two double-row, stackable connectors. The 2×20 pin connector is used for diagnostics and (optional) inter-card analog connections, the 2×32 pin connector provides power supply and digital communication. To allow for a certain flexibility, most analog pins of the smaller connectors can be assigned freely by the user. However, there are 8 fixed allocated pins for analog negative thermal coefficient thermistor (NTC) signals, measuring the temperature of key components on the cards as well as the environment temperature in integrated systems.

Cards operating in these specifications can be combined and connected with each other forming a *stack*, when equipped with a joint power supply and interface.

4.1.2. General power supply

The TBUS power supply is designed for LiFePO$_4$-battery cells of nominal cell voltage of 3.2 V. With series connections of such cells, various supply voltages can be obtained. The name of each power line is assigned according to by the number of cells (S) in series and their potential relative to GND. In this way, MAIUS operates with +3.2 V (±1S), ±6.4 V (±2S), ±12.8 V (±4S) and ±19.2 V (±6S) voltages for the electronics module.

In order to connect the batteries to the TBUS, each stack unit possesses a power supply board, which distributes the different batteries to their specific pins. Furthermore, the supply boards generates and distributes stabilized voltages of +15, +3.3 and -15 V to operate the most common analog and digital electronics under regulated supply conditions. The current consumption of each stack can be monitored via internal shunt sensors and software readout. To keep the current drain within the specifications of the pin connectors and stabilization integrated circuits (ICs), it should not exceed 1 A for the stabilized lines and 3 A per pin on the directly connected battery lines.

4.1.3. Interfacing

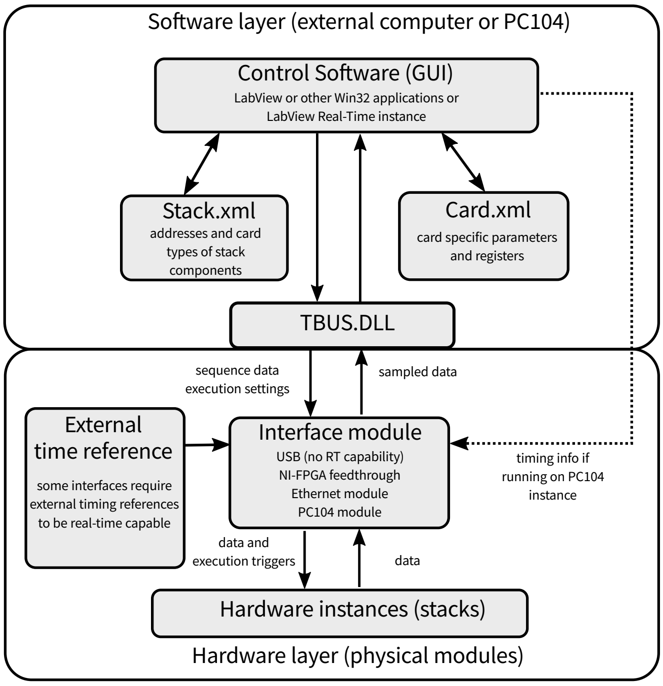

FIGURE 4.2.: Schematic of a typical TBUS implementation on a Win32 or LabView RT System. The software layer only allows for communication with one stack at a time. The USB module relies on external trigger inputs to be real-time capable. On a PC104 module, the software layer runs on the interface hardware itself in a LabView RT environment.

Depending on the demand of the actual application, there are several possibilities to access a TBUS stack via software. For MAIUS, real-time capability and reliable data distribution have been key elements of the interface requirements.

For the usage on Windows PCs, a dynamic link library (DLL), designated as *TBUS.dll*, has been programmed to interface the hardware. This driver instance can be employed with a LabView® based software on a Windows®-32 bit environment (figure 4.2), as was done in QUANTUS-2.

In order to specify communication addresses in the Bus, two more instances of software description are needed: The *Stack.xml* and the *Card.xml*.

The *Stack.xml* describes the address distribution and card types for all modules in the stack which are accessed by the controller unit. It is invoked initially by the *TBUS.dll* and provides unique user defined names that can be addressed in the GUI in order to simplify interaction on a higher logic level. Additionally, it contains the Interface ID in order to map the corresponding hardware address to the software. To customize a generic stack of identical cards, some parameters can be defined for each hardware unit in order to provide calibration parameters or other varying properties for each individual card. Due to restrictions in the Windows operating system in combination with LabView, it is so far only possible to access one stack at a time.

Depending on the card entries in the *Stack.xml*, the individual card description files are loaded in form of the *Card.xml*. This file contains card specific parameters (numeric and boolean) as well as data write and readout commands (*registers*) for their operational modes. It maps TBUS higher software operation directly to the low-level hardware commands, and functions as a reference of available basic operations for the high-level GUI programmer. Further detail on syntax and function of the XML format, as well as the implementation of the TBUS in LabView can be found in appendix C.1.

The electronic system of MAIUS-1 is subdivided into several functional stacks, which are each controlled via an Ethernet interface card. The data for a sequence is calculated and compiled on the main experimental control computer, afterwards distributed by an Ethernet switch to the according stacks. Each interface card is synchronized via a central external oscillator. Based on timing data provided to the interface module, it generates real-time triggers to control the behavior of the cards in the stack which it controls. A common trigger line for all stacks initializes the sequence execution.

During the rocket flight, MAIUS used self-developed, UNIX-based software for the experiments. However, the measurements of this thesis have been conducted exclusively with the Windows software.

4.1.4. Bus structure

The TBUS uses a parallel structure to enable simple real-time communication. To distribute the 8 bit wide data words, each element of a stack is attributed to an exclusive address out of a 8 bit space, allowing theoretically for 255 modules in each stack.

In order to enhance the data width for more complex modules, most stacks use only the first quad-bit exclusively to address modules, while the least significant quad-bit is used to enhance the data word length per module to 128 bit[1]. This method has also been used in the design of the circuitry described in this work. A detailed description of the data mapping for circuits designed in this thesis can be found in appendix C.

The assignment of the data lines and their interpretation depends on the direction of communication, which is determined by the state of a separate read/write bit, common for all modules. Depending on the corresponding address and the programming of the receiving modules, the data lines are written according to figures 4.4 and 4.3.

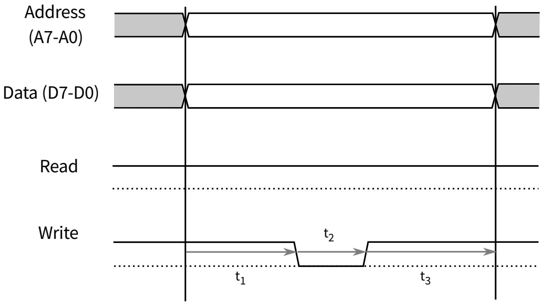

FIGURE 4.3.: A standard write cycle of the TBUS. Address and data byte are set by the interface card. After t_1, the write bit is pulled low by the interface card. The receiving module recognizes the address during t_1 and evaluates the corresponding data lines, triggered by the rising edge during the time t_3.

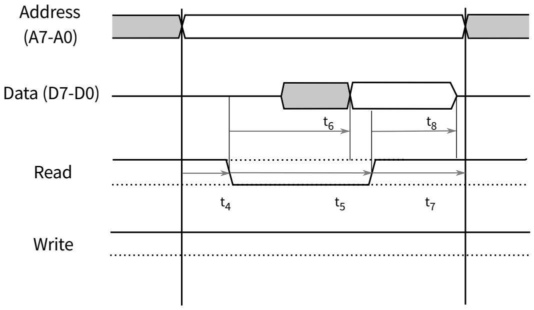

FIGURE 4.4.: A standard read cycle of the TBUS. The interface sets the address to read and triggers pulls the read bit to »low« after t_4 for the duration of t_5. Triggered by the falling edge, the module to be read out controls the data lines and distributes the data in the time $t_6 < t_5$, which is specified for each stack and must be shorter than t_5. After pulling the read bit »up«, the interface card evaluates the data and waits for t_7, while the module, which was read out releases the data lines in the time $t_8 < t_7$ before the next address change.

4.1.5. Interface requirements for the current driver designs

The TBUS presents an excellent protocol for data in-/and output for the current driver designs. Due to the timing features, it is even possible to integrate a ramp feature as a native capability, just by specifying a slope.

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[1] least significant quad-bit × data bus width: $2^4 \cdot 8\,\text{bit} = 128\,\text{bit}$

The implementation of a FPGA, along with a memory chip, enables for sufficient communication and data storage. The data for a sequence can thus be saved on the current driver card itself, only to be triggered by real-time events.

Since the communication of the TBUS is digital only, AD/DA converters are necessary to operate the analog circuitry. The resolution of the digital-analog converter (DAC) limits the precision of the current source and should not under-run the 16 Bit precision employed in QUANTUS-2, to have compatible performance.

In order to design a robust and efficient firmware, which satisfies all the demands of the data processing, the software development has been performed in the Architecture and Systems Group of the Institute of Microelectronic Systems (IMS) at the Leibniz University. Details of the function of this firmware shall not be discussed here, however, its application is described in appendix C.

4.2. Hardware and performance

As we determined in chapter 3, the functions of the intended current drivers can be divided in subgroups of chip and coil drivers[2]. Therefore, two separate designs are envisaged to be built for the MAIUS flight module: the unipolar chip current driver (UCCD) and the bipolar coil current driver (BCCD). Additionally, as the design phase of the latter two promised to be a lengthy endeavor, a intermediate solution for the ground testing was devised: the MAIUS lab-based current driver (MLCD). Its design is supposed to be very close to the function of the analog commercial current drivers of QUANTUS-2, with the focus on the initial task of compactification of the existing commercial parts, to allow for a cheap and smaller ground system in the MAIUS-1 pretesting phase.

This section will collect the hardware and power requirements that are to be expected with the experimental structures of the MAIUS-1 apparatus, which are documented in appendix B.4. Furthermore, technical limitations due to the available power supply will be discussed.

4.2.1. Hardware dimensions

The already specified electronics module of MAIUS-1 allocates a volume of 7 modules[3] of the size of standard TBUS cards[4] for the whole current driver stack, operating 4 coil pairs and 6 chip structures. While the BCCD is laid out to one standard TBUS card per driver, the UCCD has to fit two drivers on the volume of one card to supply all necessary chip structures. To achieve a such a drastic space reduction while maintaining a large design overlap between the three models, almost every IC and part is being used in its surface mount device (SMD) variant.

The MLCD, with basically no initial restrictions in dimension, has been built in a module size of two stackable cards of TBUS dimensions, but with a different interconnection system[5].

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[2] ref. table 3.2

[3] a stack of 10 height units, with 2 HU reserved for the Ethernet interface and one HU power supply card

[4] ref.: section 4.1

[5] ref: figure 5.1

4.2.2. High power supply

The current supply to drive the atom chip and coil structures is not possible to obtain via the usual standard voltage stabilization circuits, due to their limiting specifications. Additionally, the standard connections of the electronic modules of the TBUS[6] are not rated for these high currents. Hence, the current drivers employ a separate external supply line to drive their loads.

In MAIUS-1, high power battery packs are foreseen for this purpose in the electronic module. The chip driver units are each equipped with 2S `[A123 26650M1B]` 6.4 V, 2.5 A h battery packs, while the coil driver units share a common 3S `[Headway 40152SE]` 9.6 V, 15 A h pack.

As several connected circuits have been intended to use per chip layer, a galvanic separation of the current supplies for each structure is required, which results in the large number of batteries for the chip drivers.

Moreover, the complete galvanic isolation of the chip structures requires independent power supply of the employed ICs of the circuitry. This can be achieved by isolated point-of-load (IPOL) DC/DC converters. By means of switched transformators, supply voltages for the controller electronics are generated. These converters have to fulfill two additional requirements. While not exceeding 15 mm in height, they have to provide sufficient power to sustain a whole controller circuit, which is in our case below 2 W. Additionally, the current ripple of the output has to be damped, and the switching frequency of the circuit has to be chosen to be between typical trap and LARMOR-frequencies[7] in order not to cause resonant loss effects over the common ground of power supply and load.

The requirements to be derived from the already finalized power supply setup are quite restrictive, especially for the design of the BCCD.

The fact of a common unipolar battery has two consequences. First of all, although there is no galvanic connection of the coils, it is realized on the common battery ground, thus, IPOL converters are also necessary for the coil current drivers to enable operation. Furthermore, the necessity of bipolar current flow combined with only a positive supply requires a much more sophisticated amplifier architecture. The curtailment from the necessary polarity switch is to be assessed and minimized.

Finally, the limitation of power from the IPOL DC/DC converters require power efficient ICs in the overall design plan, which is another restriction on the selection of parts.

More details and schematics regarding grounding and galvanic isolation can be found in chapter 5.

4.2.3. Output power

Atom chips easily use up to 10 A of current in one circuit, e.g. the mesoscopic U, while compensation coils are driven by up to 5 A of DC current. Therefore all designs necessarily need a high power amplification stage, as conventional IC-stabilized power amplifiers cannot handle these currents.

The maximum achievable current for a load of resistance R is determined by the available supply voltage supply voltage:

$$I_{\max} = \frac{U_S}{R} \quad . \tag{4.1}$$

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[6] ref: section 4.1

[7] ref: section 3.3.5

Accordingly, the maximum available power is

$$P_{\max} = R \cdot I_{\max}^2 = \frac{{U_S}^2}{R} . \tag{4.2}$$

Furthermore, in case of the inductive loads, the switching times are limited by the battery voltage (section 4.2.5). To estimate the necessary power handling capability and the expectable excess heat, the equations above are evaluated in the following for the structures of MAIUS-1.

Chip and mesoscopic structures

The power consumption of the specific atom chip circuits[8] to be driven by the UCCD have been computed as a function of the desired currents. The curves are drawn within the maximum current output or safety margin, respectively. Their maximum power consumptions are marked with a black dots (figure 4.5).

With a maximum resistance of about 0.386 Ω and an employed current of 6.9 A, the Base Chip outer Z has the highest DC Power consumption of

$$P = R \cdot I^2 = 0.386\,\Omega \cdot (6.9\,\mathrm{A})^2 \approx 18.38\,\mathrm{W}. \tag{4.3}$$

To leave a margin for a slight extension of maximal currents, the design goal output for the UCCD was then stipulated to be 30 W.

Compensation coils

The compensation coils have been calculated in the same way (figure 4.6). It is notable, that 2D-coils and Y-coils are limited in their performance not by safety constraints as the chip structures, but by their relatively high ohmic resistance.

Here, the power consumption is much higher, with theoretical values of up to 37 W (2D-Coils). This leads to a higher stipulation for the BCCDs maximal power output of 50 W.

Although seemingly large, those assumptions are a worst case scenario, as they are calculated in a stationary state of maximum power output. However, it is already clear, that the power amplifier structure demands for high power parts to handle the estimated values, which is to be considered in the part selection.

4.2.4. Excess heat

The active control element, for simplicity assumed to be a single transistor, is has to handle the excess energy, which is not used on the chip circuits. As a result of KIRCHOFF's laws, the excess heat power P_{eh}, with the load's resistance R_L and the circuit's internal resistance R_S[9] follows this simple relation, if evaluated for $P_{\mathrm{eh}} \geq 0$:

$$P_{\mathrm{eh}}(I) = U_{\mathrm{S}} \cdot I - (R_L + R_S) \cdot I^2 \quad . \tag{4.4}$$

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[8] for detailed values, please refer to table B.3

[9] As we will see later in this section, this R_S is dominated by a shunt resistor in the current path, to measure the amplitude of the current flow. For our ideal calculations, we anticipate the value of the employed resistors in the later design.

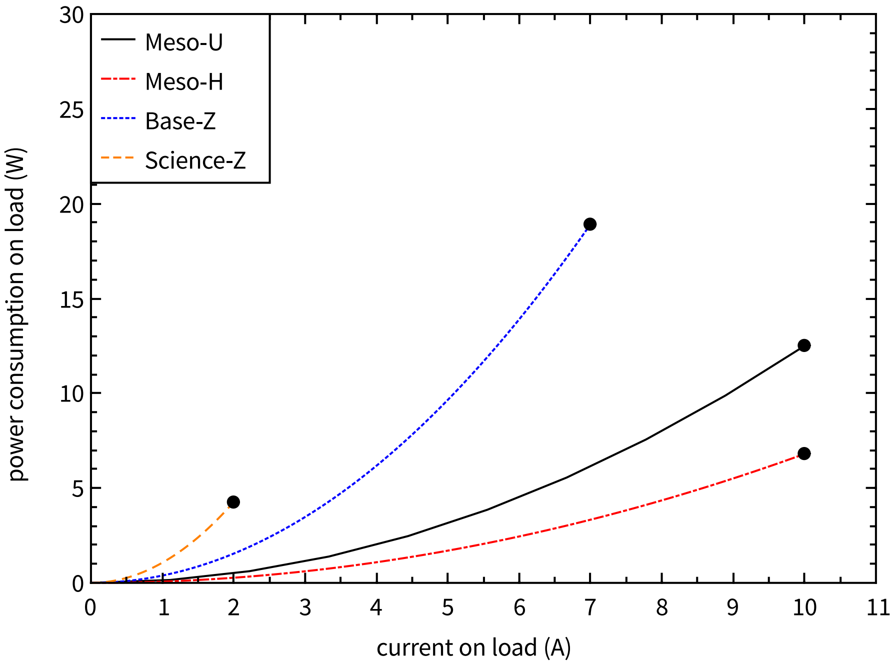

FIGURE 4.5.: Power consumption of the chip structures, within their (safe) maximum current limits. The peaks of output are marked with black dots. The Base-Z marks the maximum output of 18.38 W. With additional margin, the design goal for the chip current driver (UCCD) is thus set to 30 W.

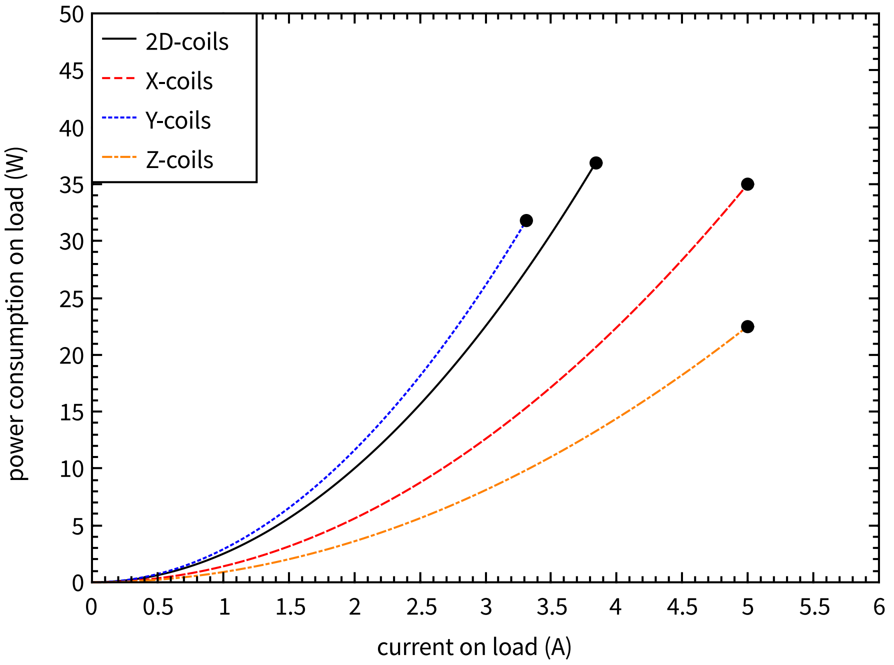

FIGURE 4.6.: Power consumption of the coil structures, within the physically useful range. The peak power requirements are marked with black dots. While the X- and Z-coils are only calculated within the range of the intended coil driver, the Y- and 2D -coils are limited by their resistance, given the supply voltage of MAIUS-1. However, the power consumption in the coil assemblies is significantly higher as in the atom chip, therefore leading to a design goal for the maximum power output of 50 W for the coil driver unit (BCCD).

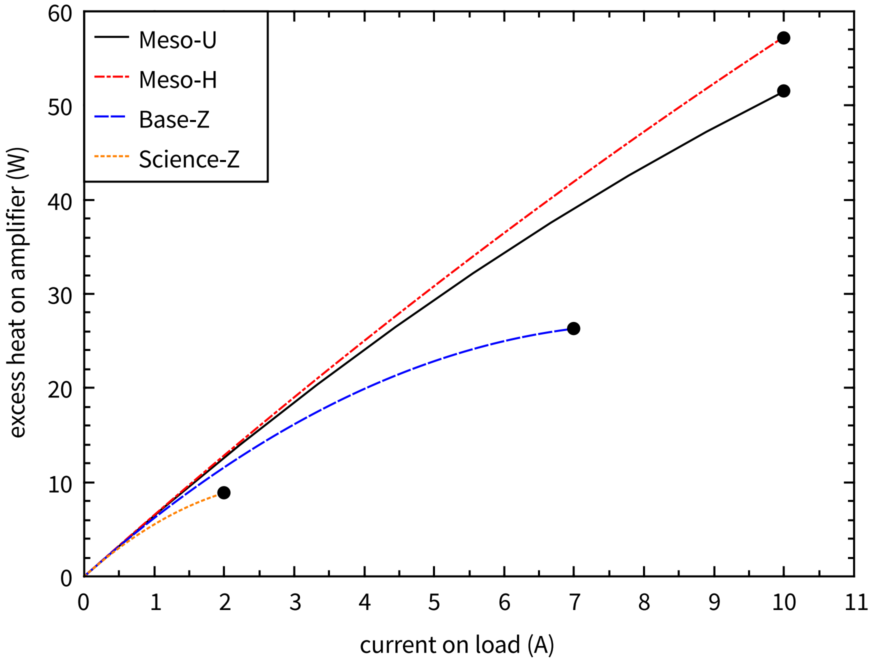

FIGURE 4.7.: Excess heat on the amplifier stages (simplified as one linear transistor) employed on the atom chip structures of MAIUS-1. Power peaks are designated with black dots. The mesoscopic structures, however only shortly in use, produce heat surges of up to 58 W of equivalent power.

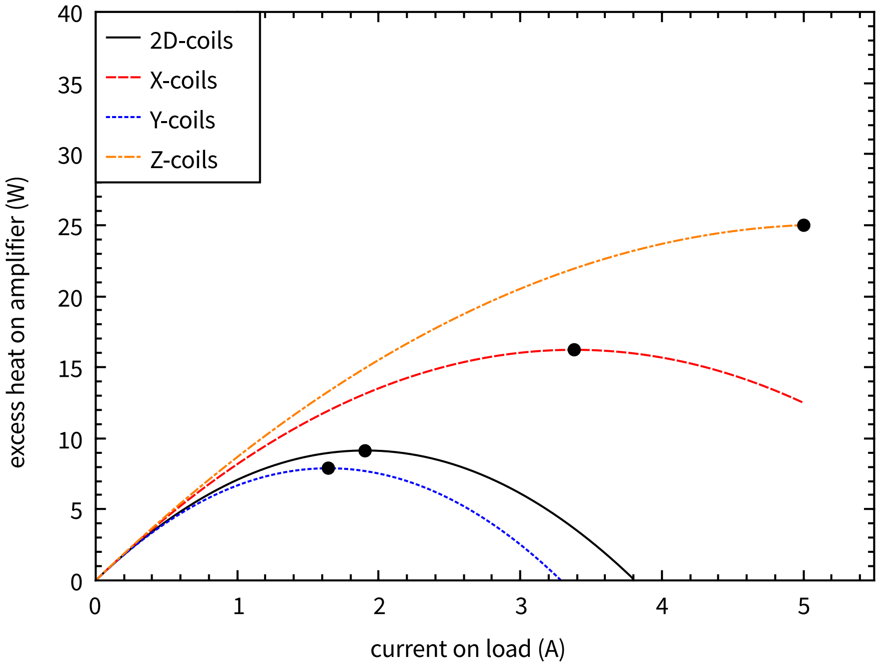

FIGURE 4.8.: Excess heat on the amplifier stages (simplified as one linear transistor) employed on the compensation coils of MAIUS-1. Power peaks are designated with black dots. The largest heat production is possible on the Z-coils, with approximately 25 W.

This function forms an inverse parabola and is minimized at high and small currents, respectively. For MAIUS-1, if one estimates all possible currents on several structures in the experiment with the already existing battery concept, one finds very high static power losses on the amplifier parts (figures 4.7 and 4.8), which thus require suitable cooling to prevent self-harm of the circuit.

The mean power output to be considered for static heat projections, however, varies drastically depending on the duty cycle, which is often short for most structures, compared to the downtime in a whole experimental sequence. Furthermore, the high power phases of a typical experimental sequences usually only cover some fractions of seconds, if not completely avoided by employing current values more favorable to power efficiency.

structure	average excess heat (W)
Meso-H	0.37
Meso-U	3.73
Base-Z	13.96
Science-Z	4.85
X-coils	3.46
Y-coils	4.60
Z-coils	0.94
2D-coils	0.80

TABLE 4.1.: Average power values of excess heat. After integration over a usual experimental sequence of QUANTUS-2, the values for a steady state estimation are much lower than the peak power outputs and allow for a more conservative approach of cooling of the planned current driver designs.

In order to estimate the average excess heat equivalent power $\tilde{P}$, it is useful to integrate over a typical experimental cycle[10]:

$$\tilde{P} = \frac{1}{\tau} \int_{0}^{\tau} U_{\mathrm{S}} \cdot |I(t)| - (R_L + R_S) \cdot I(t)^2 \mathrm{d}t \tag{4.5}$$

Following the equation, we obtain averages which are reasonable estimates for a steady state experimental operation (table 4.1).

Accordingly, it has to be assured that parts are chosen, which are not only capable of handling the high power output, but also can withstand high temperatures while delivering a good thermal coupling to possible cooling structures. The original QUANTUS-2 current driver hardware employed through-hole bipolar junction transistors (BJT) for their power output, with good performance, but not optimal in terms of cooling and ruggedness.

Therefore, replacement complementary transistors have to be selected, which have the potential to replace the BJT parts, with suitable packaging for miniaturized layout.

As one could expect some parts to be producing excessive heat due to high power handling, a cooling concept is to be devised during the design of the electronics board. Since convectional cooling is not applicable in microgravity, due to the lack of heat diffusion, the design requires a directed heat transport to the main electronic board heat sink. The electronics system housing envisages a connection of plug-in aluminum intermediate boards in 7.5 mm height to the main experimental heatsink, therefore this design proposition is the logical way to pursue.

4.2.5. Limitations on coil switching times

As discussed in section 3.5, several procedures of the experiment rely on rapid magnetic field switching. As for the chip, typical switching times of 100 µs for currents of up to 10 A are achievable, which is sufficient for all experimental purposes. The bias coils, however, with their non-negligible inductance, are limited physically in their switch response. For the coil current drivers a design goal of maximum switching times below 2 ms has been set, derived from the performance of QUANTUS-2. For the properties of the MAIUS-1 chip and coil circuits, in combination with the finalized current supply, the feasibility of this design goal will now be discussed.

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[10] In lack of complete experimental data from MAIUS-1, a drop sequence from QUANTUS-2 has been used, with a complete lens sequence and 300 ms evolution, without magnetic interaction.

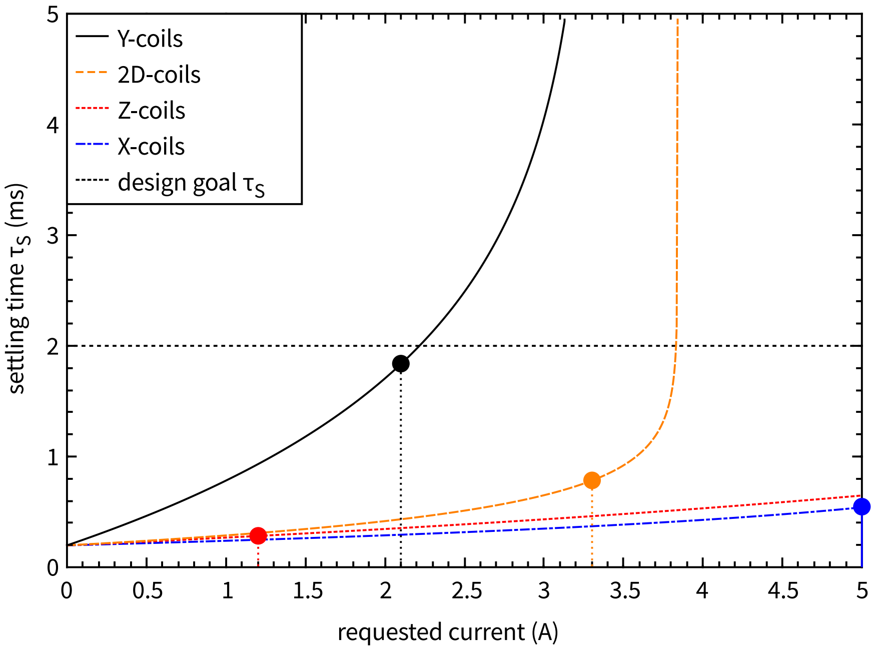

FIGURE 4.9.: Estimation of settling times for the MAIUS-1 coils. Using equation 4.8 with measured values for R and L and the estimated controller response time of τ_{PID} =200 µs, the estimations of minimal switching time can be plotted. Additionally, the maximum values of a typical QUANTUS-2 sequence are plotted for each curve (drop-lines). When approaching $I_x = U_S/R$, equation 4.8 diverges. One can see, that only the Y-coils are problematic in achieving proper switching below 2 ms which is why they have been chosen for the in-depth simulations in section 5.5.

An inductive coil with inductance L and resistance R responds to a voltage step from 0 to U_S with the current [77, eq. 4.7]:

$$I(t) = \frac{U_S}{R} \cdot \left(1 - e^{-\frac{R}{L}\cdot t}\right) . \tag{4.6}$$

This function, based on simple inductor physics, sets the upper limit for the minimal step response time τ_{min} in the case of full voltage applied to the coil.

$$\tau_{\text{min}} = \frac{L}{R} \ln\left(\frac{U_S/R}{U_S/R - I_x}\right) \quad , \quad I_x \in \mathbb{R}^+ \quad , \quad I_x < U_S/R \tag{4.7}$$

In the case of a current control, equation 4.7 would ideally determine the time until a first overshoot is detected by the controller. In order to determine the minimum settling time, it is favorable to use this function as a first estimate, and add the regulation time of the controller, containing the initial response delay and the phase of regulation after the first overshoot. Ultimately, the settling time τ_S is then calculated by the approach of the regulated output parameter into a tolerance interval around the setpoint. Depending on the width of this interval, the duration of the switching may differ. These aspects are represented by the constant τ_{PID}. The estimated settling time is therefore:

$$\tau_S(I_x) = \frac{L}{R} \ln\left(\frac{U_S/R}{U_S/R - I_x}\right) + \tau_{\text{PID}} , \tag{4.8}$$

depending on I_x as independent variable.

Evaluating equation 4.8 with $U_S = 9.6\,\text{V}$, $\tau_{\text{PID}} = 200\,\mu\text{s}$ and the values for MAIUS-1 from appendix B.4, one finds, that the design target of $\tau_{\text{switch}} \le 2\,\text{ms}$ is not achievable for all currents (figure 4.9). However, for typical maximal performance values from QUANTUS-2, as depicted for each coil, an optimized proportional integral differential (PID) controller can achieve the desired settling time.

In terms of requirements, the assumed regulation time of $\tau_{\text{PID}} \le 200\,\mu\text{s}$ is already very demanding, given the low voltage of the MAIUS-1 battery configuration. Hence, an optimization of the control parameters close to the optimum is anticipated to be of great importance to achieve the design goals.

Detailed simulations regarding the optimization of switching performance will be presented in section 5.5.

4.2.6. Technical limitations of precision

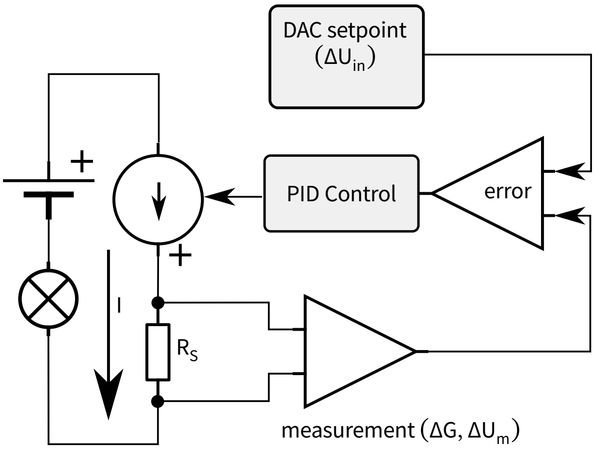

FIGURE 4.10.: Schematic of the current regulation scheme. The imperfections of the current measurement and the DAC setpoint are the biggest influences on the precision of the current output.

In order to achieve precise magnetic field control, the output of the current drivers has to be *true*, that means predictable in its absolute value and *stable*, meaning reproducible outputs for the same input value. While the determination of trueness of the magnetic field can only be performed in the actual apparatus of application with an external reference, we will focus on the given precision of the current output values, which is depending on the circuitry. For the MAIUS-1 current drivers, the measurement of the current flow is performed by a direct a voltage measurement along a stable, precision shunt resistor (figure 4.10).

The shunt resistor has to have a value R_S that allows for measurements across the whole output range of the current driver in question, ideally fitting the input range of the measurement amplifier quantifying the voltage drop $U = R_S \cdot I$. Simultaneously, it must be ensured, that the power $P = R_S \cdot I^2$ across the resistor is reasonably small to inhibit destruction of the part as well as unnecessary temperature drifts of R_S. Furthermore, the voltage drop across the shunt must not be too high, as it adds tho the total load resistance, possibly reducing the maximum output current. The best choice of material in this case are mangan-copper-nickel-chrome alloys with temperature coefficients of down to 20 ppm/K [92].

The measurement should be performed via a four-point terminal measurement, either through layout or terminals on the resistor itself, to compensate for wire resistance. Obviously, the overall precision of the resistor value has to be as good as possible, 0.1 % is usually the best available for commercial parts.

Keeping these constraints in mind, a value of $R_S = 20\,\text{m}\Omega$ is useful for the current range of 0-10 A. The measurable voltages thus have a span of 200 mV. Hence, an amplification factor of 50 can map the current measurement to 0-10 V, the same scale as a standard DAC can deliver as a setpoint. Assuming that the PID control has negligible offsets[11], only the initial current measurement and DAC errors are involved in affecting the current driver precision.

The real current output of a current driver with the digital setpoint I_{sp} can be expressed in first order as:

$$I = I_{\mathrm{sp}} + \delta I_0\left[\delta R, \delta G, \delta U_{in}, \delta U_m\right] + \delta I_\vartheta\left[\Delta R(\vartheta), \Delta U_m(\vartheta), \vartheta\right] + \delta I_R\left[t\right] \ , \tag{4.9}$$

Here, the error model consists of the initial offset δI_0, a thermal drift term δI_ϑ and random noise contributions δI_R. The initial offset δI_0 has contributions from value deviations of the shunt resistor δR, the deviation of the amplifier Gain δG, usually given in percent of the original value, as well as input offset voltages of the measurement amplifier U_m. Furthermore, the DAC can have a few bits offset deviation, which can add an initial offset to the zero current value. Especially for low current values, with only some µV of voltage drop on the shunt, input offsets of the amplifiers can lead to significant relative deviation from the desired output value. These deviations, however, are constant in their amplitude, hence can be compensated by careful calibration measurements in the experiment.

The thermal component of the current deviation, δI_ϑ consists of the thermal coefficients of the shunt resistor($\Delta R(\vartheta)$), and the measurement amplifier[12] ($\Delta U_m(\vartheta)$). These curves can have a complex shape, but are usually given as worst-case linear dependence.

Finally, the output current has contributions of random noise (δI_R), which can be e.g. the input noise of the current measurement or other parts of the regulation. It has minor influence in actual circuits, but determines the lower limit for technical current noise[13]. These contribution will affect the stability of the output, so it has to be suppressed until the value of the desired stability is ensured.

Summarizing the requirement for the current driver precision, it is necessary to choose amplifiers and resistors with low thermal drifts, as well as input offsets. For the current driver designs, an analog feedback controller promises the greatest precision in current driver output, as the measurement of actuated current is not impaired by digitalization errors or sampling speed. Hence, the selection of participating ICs is restricted to analog operational amplifiers for the controller.

4.2.7. Real-time capability

The discrete system infrastructure of the MAIUS-1 experiment requires centralized timing for all stacks. Among other circuits, especially the current drivers need to switch synchronously between several current output levels and ramp slopes with the same precise timing the whole experiment.

For this, the interface modules of each stack are synchronized by a common clock reference, and deliver pre-compiled timing triggers and a phase-locked clock for the stack of cards they control. The cards receive the timing triggers and execute saved states in their memory, thus providing real-time capability.

To allow for this, the designed MAIUS-1 modules must provide sufficient data storage to accommodate all output values which have to be carried out during an experimental sequence.

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[11] This can be assumed, as offsets are usually in the µV range, compared to several volts of internal PID voltages.

[12] This amplifier is ideally situated relatively close to the shunt resistor, hence undergoes the biggest temperature fluctuations.

[13] In the comparison of section 6.2.6, the measured spectra of the current driver designs feature a noise floor which is very close to the added input noise values for the current measurement setup in the circuitry.

Obviously, since the operation of the MAIUS lab-based current driver (MLCD) is supposed to be controlled by an analog voltage signal, these requirements are only valid for the unipolar chip current driver (UCCD) and the bipolar coil current driver (BCCD).

As we have already determined in section 4.1, a digital communication device is required anyway. With the selection of a versatile FPGA, a memory chip and suitable software development, all of the above requirements can be fulfilled without additional hardware.

4.2.8. Diagnostic data

The MAIUS-1 apparatus has to be equipped with a number of diagnostics to provide the most necessary information during and after the flight for control and post-flight analysis. During operation, the UCCD and BCCD are highly integrated, without external access and thus required to deliver the following data output via the TBUS:

- **Temperature information**: Since the drivers handle large amounts of power, the temperature of the parts exposed to excess heat has to be monitored, and if too high, operation of the current driver needs to be suspended in order not to damage circuitry or the atom chips.
- **Battery voltages**: The charging scheme of the batteries for the UCCD did not stipulate a monitoring of the battery charge status (usually done via the output voltage). In order to monitor functionality of the power supply, the value of the battery voltage has therefore to be measured by the current drivers themselves. Although provided for the BCCD by the battery module, this function is stipulated for these modules as well to have comparable measurements for all driver modules in the same stack.
- **Output current**: In the case of malfunctions, the operation of each current driver has to be revisable. Therefore, a coarse signal proportional to the output current is needed.

To achieve these data measurements, the requirements for suitable measurement and rescaling of the data have to be taken into account, as well as a conversion analog-digital converter (ADC) to digitize the analog measurements to be added into the data stream. As the FPGA has no dedicated A/D converter, an external IC has to be employed in the designs.

4.3. Atom chip safety

Atom chips – convenient as they are to use in compact apparatuses – undergo a very elaborated and lengthy production process that demands vast resources of personnel, equipment and clean-room facilities. Therefore, it is mandatory for the experiments to provide a sophisticated failsafe mechanism to prevent the atom chip from being harmed by extensive deployed energy, either due to technical or human failure. The energy can be formulated as product of power P and cycle time τ_C

$$E = P \cdot \tau = I^2 \cdot R \cdot \tau_C \tag{4.10}$$

On conventional printet circuit boards in the laboratory, strip lines of gold can withstand reasonable amounts of energy. In high vacuum, however, the situation of an atom chip is different. Due to the lack of ambient cooling, the only way to transport heat from the structures is the thermal connection to the chip. Although the employed AlN substrates offer a good value in that manner, already moderate energy amounts can cause notable heating in loads as narrow as e.g. the Science Chip structures, with a conductor cross-section of only $50\,\mu\text{m}^2$.

As the whole load consists of vacuum feedthroughs, cables, wire bonds and gold wires, the weakest link of each structure has to be identified to determine proper limits for the protection. For example, the wire of a Science-Z can electrically sustain a current of 6 A without deterioration, but gives rise to temperatures above 50 °C, which causes irreparable damage to the optical coating on top of the chip substrate[14].

To protect all employed chip structures from excess energy, an electronic safety layer is required, providing the following functions:

- Possibility to sever the connections to the load. Inhibition of current flow, even in case of power supply failure.
- Measurement of direct current (DC) amplitude. Inhibition, if value exceeds given maximal values.
- Independent timing measurement of current flow duration. Inhibition, if value exceeds given maximal values.
- Allowance of cool-down period to avoid non-stop current flow.
- Data communication of error messages and external trigger control to synchronize with experimental sequence.

To keep modularity of functions, as well as independence of the security layer, these functions are stipulated to be realized on a separate printed circuit board (PCB) outside of the TBUS environment, which will be introduced in section 5.6, and is described in more detail in appendix D.

4.4. Summary

The parameters of the three MAIUS-1 design models complying with the technical and scientific requirements of the different applications are summarized in table 4.2. These values form the landmarks of the design process, whose outcome will be discussed in chapter 5.

A central part in the overall design is to ensure the compatibility of precision current drivers with a high demand in power output in a very compact environment. The additional requirements on the battery supply for the BCCD demand for creative solutions, as standard approaches do not apply without modification. Furthermore, the required switching times, especially in the y-coils of MAIUS-1, demand for an optimized controller model and a detailed prediction of the switching behavior to determine control values for generic inductive loads. Hence, the coil driver is the most complex design project, and will be accompanied with detailed simulation of performance.

As already mentioned, the firmware design of the circuits has been assigned to the IMS in an early stage of the development, hence the workload and coverage of the design studies will be focused on hardware development and performance evaluation.

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[14] Actually, this damage occurred in the first drop tower experiment, QUANTUS-1 in April of 2009, causing a cease of operation for several weeks, until replacement of the chip and re-evacuation.

apparatus quantity	MAIUS lab-based current driver (MLCD)	MAIUS unipolar chip current driver (UCCD)	MAIUS bipolar coil current driver (BCCD)
max. current output	± 10 A	10 A	± 5 A
direction	bipolar	unipolar	bipolar
ramp capability	yes, if input suitable	yes	yes
wave form	arbitrary input form	arbitrary wave form (linear approximation)	arbitrary wave form (linear approximation)
switching time	variable	≤ 100 µs	≤ 2 ms
minimal slope (ramps)	not specified	$> 1\,\mathrm{A\,ms}^{-1}$	$\geq 1.6\,\mathrm{A\,ms}^{-1}$
current noise LSD	lower as in Q2 Driver ($1\,\mu\mathrm{A}/\sqrt{\mathrm{Hz}}$)	lower as in Q2 Driver ($1\,\mu\mathrm{A}/\sqrt{\mathrm{Hz}}$)	lower as in Q2 Driver ($1\,\mu\mathrm{A}/\sqrt{\mathrm{Hz}}$)
output stability	≤ 50 ppm	≤ 50 ppm	≤ 50 ppm
real-time capable	yes, if input suitable	yes	yes
dimensions	not specified, smaller as commercial modules	100 mm×100 mm×17 mm	100 mm×100 mm×17 mm
cooling	passive/fan	passive	passive
input resolution	± 10 V analog voltage limited by input source	16-bit ($3.05 \cdot 10^{-4}$ V, same as PXI FPGA)	16-bit ($3.05 \cdot 10^{-4}$ V, same as PXI FPGA)
max. inductance	5 mH	200 µH	5 mH
max. resistance	variable	1.2 Ω	3 Ω
max. power (consumption)	not specified	100 W	100 W
max. power (delivery)	not specified	30 W	50 W
max. supply voltage	±4S (12.8 V)	2S (6.4 V)	3S (9.6 V)
monitoring	not available	battery, temperature , current	battery, temperature, current
control mode	analog	TBUS, digital, FPGA real-time trigger	TBUS, digital, FPGA real-time trigger

TABLE 4.2.: Summary of stipulated performance data for different designs of current sources. The maximum power of the MLCD was not specified in the beginning. Note: These values can be surpassed by the actual designs, but formed the baseline of intended performance values.

CHAPTER 5

Design portfolio of current drivers

Facing the unique challenges posed by the derived specifications of portable atom chip sources for sounding rocket missions, several circuit designs have been devised. The following chapter describes their engineering concept and application possibilities, as well as their mode of operation in the experiments of the QUANTUS-collaboration. In the prospect of further commercial exploitation, only the basic design concepts and selected solutions to the problems posed in the context of the MAIUS-1-mission are presented here.

The performance of the circuitry introduced in this section will be characterized in chapter 6.

5.1. Overall design guidelines

When presented with the various requirements on current drivers for chips, one quickly finds that it is not feasible to create an all-in-one solution without succumbing to improper curtailment. However, it is possible to summarize some common cornerstones, which guide the further design process for all current drivers.

All current drivers in this work are self-regulating circuits with analog, active feedback control, to provide for the necessary precision and current control, without digitalization losses. The main controller architecture is a discrete proportional integral differential (PID) scheme, realized with operational amplifiers, effectively controlling the voltage over reference resistors in the current path of the output. With the correct calibration of the feedback path, one can realize different fixed voltage/current gain factors.

While modern current drivers usually employ digital pulse-width modulation (PWM) in combination with low pass filters in order to achieve higher energy efficiency, it has been decided to use well established analog circuits in order to reduce noise introduced by modulation and mixing frequencies, as well as reference oscillators to a minimum. Furthermore, the speed of current switching is most crucial, so that conventional PWM circuits would not be able to deliver ripple free waveforms to an ohmic load, while still maintaining the necessary fast step response.

To realize the lowest current noise possible, a current supply with external batteries has been chosen in all concepts presented. Only this approach combines the favorable properties of compactness, high pulse current rating and absence of ripple noise. Additionally, batteries are very robust in field application and therefore suitable for all kinds of situations encountered in the QUANTUS missions.

Since all experiments of the QUANTUS project are highly integrated, proper measures of safety, especially against failure of the high power circuits had to be implemented. Therefore, all elements of amplification utilize fast melting fuses in order to protect the sensitive loads in case of accidental failure of current driver or control computers.

To enable the operation on galvanically connected atom chips on one hand and to eliminate the possibility of ground loops, all circuits employ the concept of the ground lift, largely known from the area of audio and recording. Utilizing IPOL-DC/DC converters, a new reference potential relatively to the load is created, which has no connection to the input side of the current driver. Thus, the grounds are virtually disconnected. In order to inhibit distortion due to high frequency noise between the both ground potentials, a capacitive coupling via a high pass is then introduced to generate a high frequency short circuit, effectively creating a common ground for alternating current (AC). Furthermore, a high-resistance ohmic coupling ensures the ground-lift to be within safe voltage parameters. The implementation of this coupling differs from circuit to circuit, while the basic idea is the same for all designs.

DC-DC converters of the employed type inevitably introduce ripple noise into the supply line, mostly at the frequency of their switching frequency, which has to be closely observed and reduced as good as possible. To suppress negative influence due to the noise effects discussed in section 3.3, only parts performing way above the estimated trap frequencies have been chosen[1] and equipped with filter circuits to minimize their impact on the current noise.

Apart from their ease of operation, DC-DC converters are limited in their output power, which requires energy-efficient parts in the overall circuit design. The chosen operational amplifiers[2] combine low noise, low power consumption and temperature stability on a level that makes them perfectly suitable to the task at hand. As a result, the whole circuitry of the driver modules can be operated with less than 2 W total supply power.

5.2. MAIUS Laboratory Current Driver (MLCD)

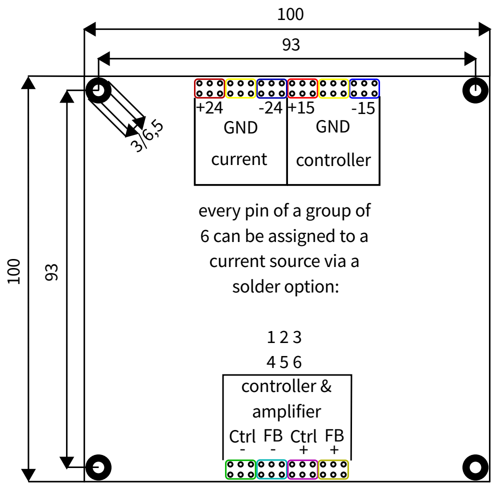

FIGURE 5.1.: Pin assignment of the stackable bus system for the MLCD. Dimensions in mm.

Given the challenging time frame of the MAIUS-1 mission, along with the demand for radical miniaturization of the circuit, an intermediary solution has been created, which should reproduce the performance and functionality of the commercial QUANTUS-2 current drivers, with comparable size to the final flight hardware. Additionally, the yet unclear specifications of the final vacuum system demanded for a preferably versatile configuration of the current drivers in order to enable quick changes of their operation.

Thus, a two-fold concept of a PID-controller and amplifier unit has been developed, based on the modules employed in the drop-tower projects[3]. It was referred to as *MAIUS Laboratory Current Driver* (MLCD). In order to evaluate varying controller setups with different amplifier concepts and cooling methods, the controller module, equipped with a number of switches and adjustable PID control stages was separated from the amplifier board, only connected by a common signal ground and feedback/control signals. The concept employs a stackable connection, combining the positive properties of modularity and compactness of a stackable bus similar to the TBUS.

Based on the experience of LASUS, the same physical dimensions of 100 × 100 × 17 mm^3 have been chosen to have the same mechanical properties such as weight, shock durability, etc.,

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[1] `[XPPOWER IM Series], ref: [93]`

[2] `[TI INA 128, OPA 277]` and derivatives

[3] `[High Finesse BCSP-10]`

but pattern and number of the bus pins have been altered to prevent unintended connection of the analog current drivers to the digital TBUS. Each current driver module consists of a PID-controller and an amplifier board. Communication and power supply is established via the stackable bus (figure 5.1).

Replacing a full 3 HU[4] 19 inch rack unit of the commercial current drivers, a stack system of 6 driver modules per stack has been constructed, with dimensions of 100 × 100 × 195 mm^3. Two of these stacks have been employed to characterize the MAIUS-1 physics package. The configuration devised in the evaluation phase has been a PI-controlled class AB amplifier for the ohmic atom chips, and a PID-controlled class AB amplifier for the inductive bias coils. The amplifiers have been actively cooled with standard computer fans, which is sufficient as long as the experiment is not run continuously, but with 1-5 seconds of cool-down time between sequences.

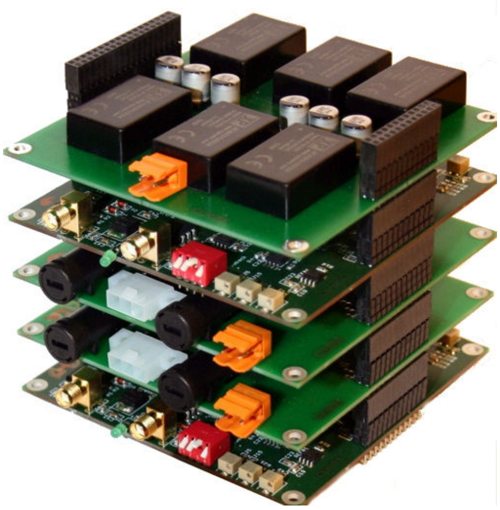

FIGURE 5.2.: Photograph of an example stack with 2 current drivers and power supply.

The PID controller board relies on an external power supply which can either be realized by conventional lab supplies or batteries. For compact operation just from one positive power supply, an optional external power supply has been designed, which enables a galvanic isolation of the current drivers via six isolated point-of-load (IPOL) DC/DC converters and thus enables the operation on a short-circuited atom chip. To prevent influence of the ripple generated by the switching of these parts, as well as enabling operation on batteries without DC/DC conversion, another step of voltage conversion with linear voltage controllers has been introduced on each controller board. Through solder options with logically arranged pads on the PCB, the same board layout enables up to six self-sufficient current drivers in one stack (figure 5.2).

5.2.1. Controller board

The commercial current drivers used in QUANTUS-2 were designed to operate on an ohmic load, thus making them not very suitable to be applied with inductive loads such as compensating bias coils. Their concept of a simple PI-type controller and a noise suppressing capacitor parallel to the load were found to cause oscillations when operated on inductive loads such as the bias coils of QUANTUS-2, where they effectively formed resonant RCL circuits in the current path[5]. Therefore a primary design goal was to deliver a more versatile version of current drivers, offering a more general application on both inductive and pure ohmic loads while maintaining suitable current switching times. To achieve this goal without lengthy simulations that would delay the atom chip ground operation, the controller was designed with as many tuning possibility as possible, including the introduction of a differentiator control path to suppress oscillations.

Furthermore, the circuit features external potentiometers to tune PID, offset and current scaling, adaptable to the features of the respective inductive, capacitive or ohmic load. In the designated application in the lab, the design allows to tune these parameters during operation,

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[4] 3 height units accord to 133.35 mm

[5] For further details on the treatment of this problem in QUANTUS-2, refer to section 5.5.2.

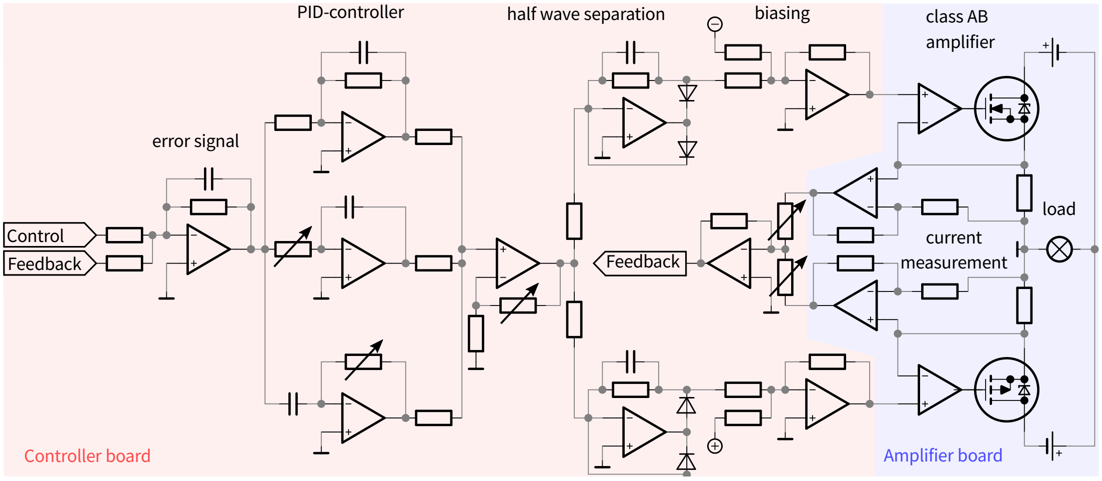

FIGURE 5.3.: Simplified schematic of the MLCD. The two colors indicate the localization of the respective parts of the layout. The control signal can be offset corrected before inserted into this scheme. Potentiometers provide in-situ PID-tuning and feedback calibration. Biasing voltages (+ and -) have to be determined carefully in order not to cause high idle-state current flow.

so an optimization of switching characteristics on every load would be applicable for the experimentalist without in-depth analysis of its impedance. A simplified schematic is shown in figure 5.3. Due to the usual variation of component values, the necessary calibration of high precision current drivers is very time consuming, as it has to be done anew for every module. For convenient operation in the lab, there are solder options to tune the calibration via one potentiometer for each direction of current flow. In addition, the offset to zero of the current output can be tuned to match even very slight output offsets of the analog input stage. If the proper calibration parameters have been found, it is possible to match the potentiometer value with two resistors of high precision, thus permanently establishing the calibration per driver. Afterwards, it is then mandatory to maintain the combination of two successfully calibrated modules, as significant parts for the calibration are situated on both boards.

The current flow is controlled via an analog control voltage (± 10 V) which is then scaled to the full current output (usually $1\,\mathrm{A}\,\mathrm{V}^{-1}$). Inhibiting a common reference via the input, which would in our case be the ground potential of the experimental control computer, a pseudo-galvanic isolation[6] via an instrumental amplifier[7] has been used to separate the control signal from the controller ground. In order to prevent the separated reference voltages to drift further apart as the absolute maximum ratings of the input amplifier, a weak ohmic connection of 1 MΩ was established.

Each controller receives it's setpoint via an external voltage source and can optionally be enabled and disabled via a TTL-trigger input.

5.2.2. Amplifier board

While the miniaturization of an analog logic board is basically a question of part selection and efficient routing, the demand for compact amplifiers is much higher, especially with expected constraints in power delivery and possible excess heat.

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[6] pseudo-galvanic means, that the potentials are separated by a high resistance, but current flow is still possible. Therefore only isolation voltages of ~ 40 V can be achieved, which suffice for our purposes.

[7] `[Texas Instruments INA 128]`

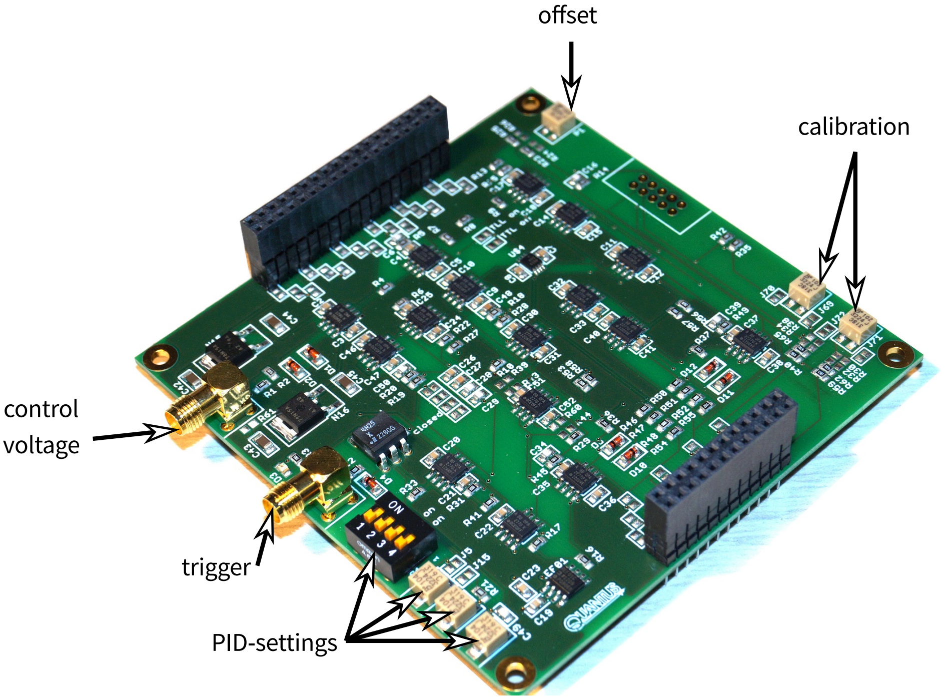

FIGURE 5.4.: PID controller board of the MLCD: in front the SMA-sockets for analog control voltage and TTL-trigger are placed. The front potentiometers change PID parameters and switches. In the back on the left there is the offset control and on the right the calibration potentiometers.

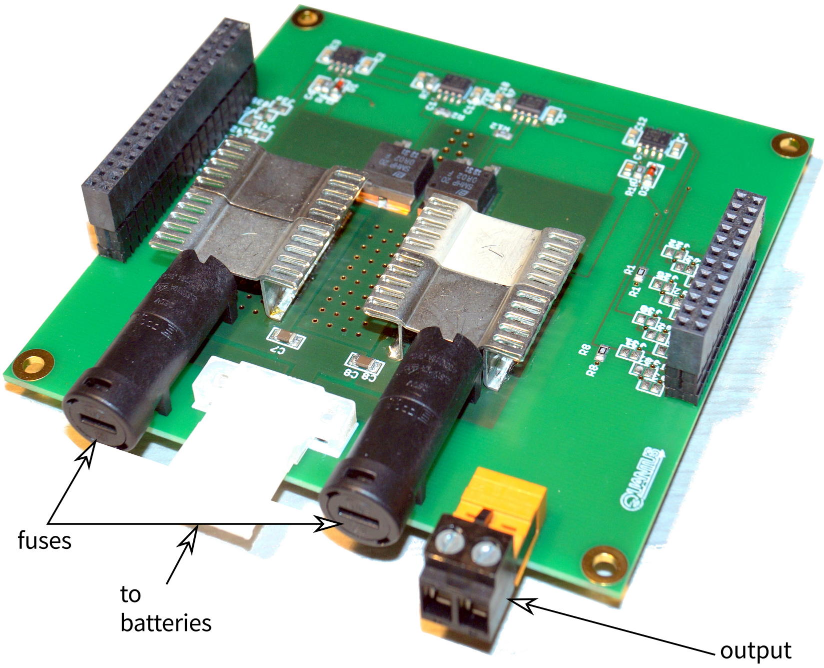

FIGURE 5.5.: Amplifier board of the MLCD current driver: The front harbors the white battery connector and the orange load connector. The black tubes carry two melting fuses. The cooling bodies ensure the proper heat dissipation of the TO- 263 power transistors below.

To ensure a maximum of flexibility while maintaining a comparable performance in precision and noise reduction of the commercial drivers, a class-AB bipolar amplifier has been constructed, allowing two directions of current flow with up to 10 A. The key parts in the amplifier stage are the two power transistors that conduct and regulate the full current flow through the load attached to the driver.

The commercial drivers of QUANTUS-2 use matched pnp-npn DARLINGTON-pair BJT[8] to have a very high current output via current-based control of the transistors. As the flow of the base-emitter current is very precisely tunable, this enables for excellent controlled output current of the amplifier stage. However, the precision of high currents is paid dearly with high thermal losses due to the unfavorable TO-3 case of the DARLINGTON-pair that demands for heat sinks that themselves would exceed the size of our whole current driver module. The reduction of the heat sink mass, while maintaining the decision to use BJT would bear the crucial risk of thermal runaway, as the amplifier gain decreases with rising temperature so a self-destruction of the amplifier, even at idle current flow would be possible.

As metal-oxide-semiconductor field-effect transistors (MOSFETs) are usually self limiting in the regard of thermal runaway, the design of the amplifier stage was altered to use a P- and N-Type MOSFET pair[9] that are controlled by voltage. Due to the variety of packaging with much better thermal connection, this also enabled for a drastic reduction of heat-sink size while maintaining the safety constraints for the case of high excess heat.

In order to keep the heat manageable and to allow for large areas of copper to be used as heat sink, the power transistors and shunt resistors have been placed on a separate PCB to be stacked on top of its PID controller. Using two large layers of copper and additional four TO-263 SMD-heatsinks in combination with convectional cooling fans, steady state operation with part temperatures less than 70 °C[10]can be achieved, which is satisfactory for lab-based operation with a small cool-down period, and short time duty during drop tower experiments.

5.2.3. Limitations of the circuitry

The MLCD has proven to be suitable for its initially intended design goal of high compactness while maintaining the reference circuits performance values and tolerable excess heat. Meanwhile, the design found application in currently four experiments[11] inside the lab and even in the drop tower or for experiments designed for field application. Due to the rich experience with their operation, they have revealed certain constraints that limit their field of application, and are important to keep in mind as these modules, although quite versatile, are no all-in one solution.

- The MLCD operates in class-AB mode, thus a constant current flow out of two batteries is necessary for precise operation, even in idle mode. This causes a significant drain of power out of batteries, even with no output current. Thus, they must be recharged periodically in order to maintain operational (figure 5.6).
- The temperature of the amplifier stage can not be measured by the module itself. An undetected failure of cooling could result in damage of the current drivers[12]. Therefore, external observation of temperature or active cooling is necessary.

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[8] `[ON Semiconductor MJ11*]` series

[9] [STB80NF/PF]

[10] A scenario for relatively high continuous excess heat has been chosen ($P_{\mathrm{Load}} = 9\,\mathrm{W}$, $P_{\mathrm{heat}} \approx 30\,\mathrm{W}$), which is twice the estimated average from table 4.1.

[11] Ref:appendix B.2

[12] not the load, as it is protected with fuses and other safeties (ref.: section 5.6).

- The shunt resistors used to determine the current measurement heat up with the copper on the PCB amplifier stage. Therefore, drifts in the output value occur, which can impair the trueness of the calibration.
- The interface for the control signal is analog, which makes the driver operation easily implementable to an existing setup. The long cables to deliver the control voltages bear the complication, that RF noise of the environment can couple into the signal line and cause disturbance in the current driver operation. Due to the poor common mode noise reduction for frequencies above 1 MHz in the input instrumentation amplifier, strong DC offsets have been observed, caused by RF radiation of the preamplifier, used for evaporation and situated close to the current driver stack (figure 5.7). This makes proper signal filtering and short, shielded signal cables a necessity.
- Designed as a low-cost replacement of the commercial parts, the thermal design of the MLCD limits the overall power the device can handle, since it is completely manufactured on standard pcb boards. The additional cooling elements provide a certain improvement of the cooling capacity, but require a lengthy, delicate manufacturing process that is not suitable for mass production.
- The design uses potentiometers for convenient operation in the lab. However, mechanical drifts can influence the driver operation. In addition, a potentiometer introduces an inductance (typical ~ 100 µH) into the feedback line, which could lead to resonances for certain loads, which have to be excluded thoroughly.

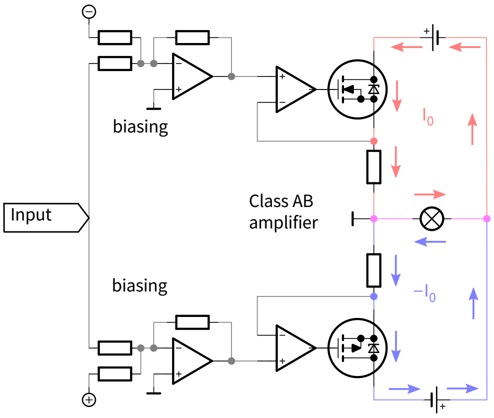
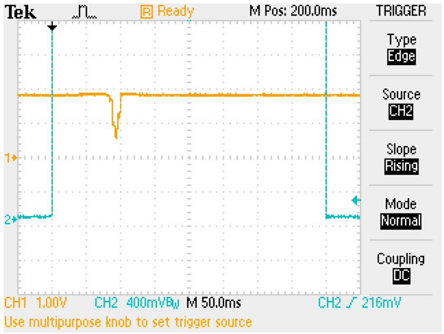


FIGURE 5.6.: Class AB amplifier in idle mode. For a »0« control input, the two idle currents (I_0, $-I_0$) through the transistors compensate each other on the load.



Type Edge
Source CH2
Slope Rising
Mode Normal
Coupling DC
CH1 1.00V CH2 400mVBw M 50.0ms CH2 ∕ 216mV
Use multipurpose knob to set trigger source

FIGURE 5.7.: Radio Frequency Interference on the MLCD. The yellow curve shows the output current measurement of a MLCD during an evaporation sequence. The high-power RF cable is guided close to the current driver board. During the tigger pulse event (cyan), the radio frequency is linearly ramped from 40 to 0 MHz. Between 30-32 MHz, a parasitic resonance of the input opamp occurs, in this case resuling in a current jump of approximately 1.5 A.

If these limitations are acceptable, the MLCD provide a reliable, versatile current driver for preliminary testing in a controlled lab environment. Therefore these current drivers have been used in the context of MAIUS for functional evaluation of the physics package until completion of the electronic module. However, as comparative measurements of noise levels between the different designs of current drivers have revealed (figure 6.10), the current noise performance of the MLCD is surpassed by the later designs, which is why it has been discontinued in favor of the new sophisticated current drivers of MAIUS. Nonetheless, their further development in the direction of larger scaled lab-sized modules could deliver a low-cost, tunable alternative on par with the current state-of-the-art commercial current drivers [94].

5.3. Unipolar Chip Current Driver (UCCD)

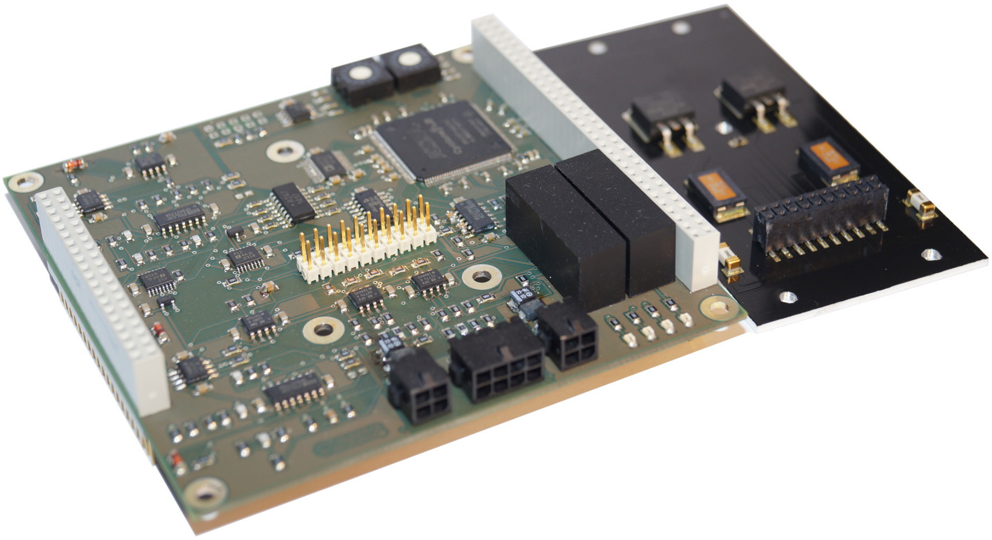


FIGURE 5.8.: Logic and power board of a UCCD module. The amplifier part is on an aluminum board of 1 mm thickness to be stacked on the central pin header during operation. The board houses two independent, galvanically isolated, unipolar driver units with an amperage of up to 10 A for each unit.

As discussed in chapter 4, the operational platform of the MAIUS-1 mission, adds several technical requirements to the flight model of the chip current driver, due to the finalized battery concept, the necessary interface compatibility and compactification demands.

These design constraints require a drastic reduction of the amount of active parts, as well as a change of the amplifier structure towards a single ended current driver. Its design designation is *Unipolar Chip Current Driver* (UCCD).

5.3.1. Current driver architecture

As simple alterations of the MLCD design would hardly fulfill all the requirements at once, a complete new concept for the current drivers has been developed. Due to the missing negative supply voltage for the power stage, an amplifier stage for a single supply has been designed.

A very convenient choice, a class A amplifier, would have excellent performance in linearity and response time, but the steady current flow through the amplifier stage is problematic in the situation of limited battery capacity and high power applications.

Another approach, employing a biased, single ended class AB amplifier, relying on a certain bias voltage to maintain in linear operation, is a poor choice of amplifier for the application on atom chips, which cannot tolerate any idle current due to slight mismatch in the threshold and bias voltages, which themselves also vary with the MOSFET's temperature.

Therefore, the novel design employs an amplifier in form of a single ended class B stage, only amplifying the positive half-cycle of current (figure 5.9). If operated without any bias voltage on the input, a single MOSFET in this configuration has a strongly nonlinear gain curve. While this would be unfavorable in a non-controlled amplifier stage, the feedback control in the design can compensate for these problems by adapting the input voltage to the amplifier. However, the nonlinearities are still notable during the regulation process. Thus, the switching waveforms do not correspond with classic PID behavior due to the variable loop gain.

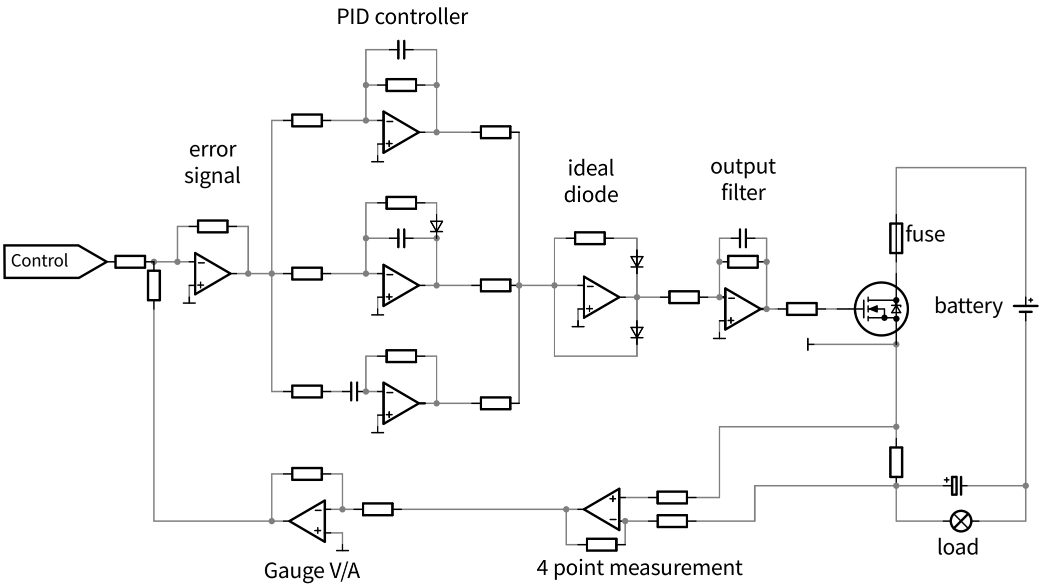


FIGURE 5.9.: Simplified schematic of the analog current driver architecture of the UCCD. The PID controller is modified in the integrator to suppress negative saturation, and afterwards half-wave filtered. Finally, the low-pass filtered controller signal drives the unbiased Class B amplifier.

The PID controller design is basically adopted from a textbook [95, pp. 1279–1280]. In addition to this circuit, the introduction of three diodes in the circuit ensures proper half-cycle separation. The diode in the integrator part inhibits a negative saturation for small negative input offsets, while still enabling the amplification of a positive control signal. With the half-wave separation of the »ideal diode«, it is now possible to enable unipolar operation of the transistor with linear voltage input. The output filter limits the response time of the transistor to frequencies controlled by the PID-controller, thus enabling a noise reduction of high frequency components of the output current. In order to damp excess gain for disturbance or current jumps, a large capacitor is added to the output stage. This leads to additional noise reduction and smoothing of switching waveforms.

The high-power parts are placed on a plug-in aluminum board, which is mounted on top of the controller PCB and contains only the shunt resistors, power transistors and temperature sensors for diagnostics. The power board is attachable to the main heat sink, thus providing enhanced heat transport and temperature stability. With these alterations, the resulting driver modules house now two unipolar drivers which can either be used for different chip structures or combined to drive one structure in different directions[13]

5.3.2. Grounding concept

As the current drivers are used on galvanically connected atom chip structures, it is mandatory to ensure galvanic isolation of all batteries and the ground references of each analog driver, resulting in one exclusive galvanic connection via the chip. With all input and output signals joined on a common digital interface via the TBUS, another step of isolation is necessary, requiring a total of five reference voltages[14] per driver board, with isolation in respect to each other. Apart from the common ground potential of the TBUS, these are two IPOL analog

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[13] Ref.: section 6.1

[14] TBUS GND, GND1, GND2, Battery1 -, Battery2-

reference voltages, generated by DC/DC converters[15] and the two cathodes of the power batteries.

Figure 5.10 gives a schematic review of the grounding concept on an atom chip and two current drivers, including the measurement of the currents via a shunt resistor.

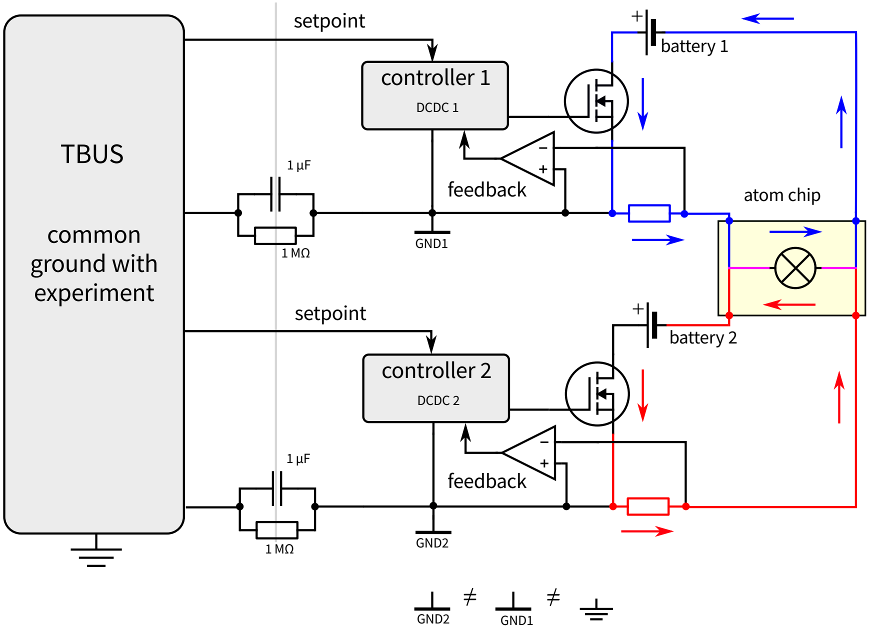

FIGURE 5.10.: Schematic of grounding for the atom chip with exemplary current drivers and a dummy load. The pseudo-galvanic isolation is well defined with a weak ohmic coupling to the common TBUS ground. For higher frequencies, the capacitive AC-coupling of the potentials provides high frequency noise suppression at the output of the drivers. The two separate batteries allow for two independent currents though the galvanically connected chip structures. The reference potentials GND1 and GND2 are provided by two IPOL DC/DC converters in the controllers.

5.3.3. Data input

The digital communication is realized with a field-programmable gate-array (FPGA) module with 128 kb of external configuration memory[16]. The data distribution is realized with a 16 bit digital-analog converter (DAC)[17], diagnostic data is collected with a 10-bit, eight channel analog-digital converter (ADC)[18].

The voltages to control the two analog current drivers are generated via the DAC, driven by the FPGA with reference to the real-time clock of the TBUS. The FPGA control is trigger-based and provides voltage jumps to a designated value or ramps within a certain range of slopes, until the next trigger event occurs. With the typical parameters of the firmware and the clock frequency employed in MAIUS-1, the DAC-connection features the performance conditions summarized in table 5.1, which are all in compliance with the requirements formulated in table 4.2.

As each entity of the UCCD consists of two current drivers, the input data matrix is split into the two-fold of input values. The data type of the input is a one-dimensional array of clusters,

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[15] `[XP Power IM2415S]`, Ref:[93]

[16] `[Intel/Altera Cyclone II]`

[17] `[Analog Devices AD 5752R]`

[18] `[Microchip MCP3008]`

Item	Value
voltage settle time	10.4 µs
full range	± 10 V
minimum step size	± 305.18 µV (≙ 30 ppm)
minimum slope (internal calculation)	$\pm 18.05 \cdot 10^{-3}\,\mathrm{V\,s^{-1}}$
maximum slope (internal calculation)	$\pm 1.95 \cdot 10^{3}\,\mathrm{V\,s^{-1}}$

TABLE 5.1.: Typical values for DAC performance in the unipolar current driver, only voltage values of 0-10 V have effects on the current. For the BCCD, the same performance data are valid for bipolar operation. (Ref: [96])

each cluster representing a state of ramp/jump and a designated value of slope/value to jump to. While the first value of the array represents the standby values, which are executed without timing limitation, the other items of the array are called via trigger commands of the TBUS. Details on the implementation of the data transfer can be found in appendix C.

5.3.4. Diagnostic measurements

The MAIUS-1 mission, being an autonomously operating sounding rocket experiment, is subject to a vast demand for diagnostics, as there are not entry points for additional measurement devices intended in the design. Therefore, the ADC measures battery voltages, actual feedback signals proportional to measured current, and the temperature of the aluminum board close to the power transistors. Read out by the experimental control computer with up to 10 Hz sample rate, these measurements enable for simple diagnostic and intervention by the experimental software, if necessary. The battery voltages are measured after the safety fuse, so that a zero measurement would indicate a melted fuse for additional diagnostic information. Voltages, currents and the temperature values are sampled by the FPGA very quickly, so that a tenfold gliding mean can be executed by the firmware to improve the precision of the measurement. The mean temperature value, measured with a NTC, is then checked by an internal finite state machine (FSM) with hysteresis, to prevent the circuit from overheating. Above the critical board temperature of 80 °C, the current driver shuts down and is re-enabled after a cool down to 60 °C.

The NTC measurement was originally intended for safety purposes only, but has also been of use to characterize the stability of the current output (section 6.3.2).

5.3.5. Layout

As the precise function of the current driver is inherently dependent on temperature stability of key system parts, their arrangement in the layout is a very important aspect of the design. With estimated currents of about 10 A, a suitable thermal connection and width of certain layout parts has to be ensured in order not to generate too much excess heat, while still maintaining a very compact layout. With the separation of high power parts on a plug-in aluminum board, this compromise can be achieved.

The parts relying on good temperature control and conductivity (transistors and reference resistors) have been placed on a separate aluminum board of 1mm thickness and a NTC temperature sensor. The aluminum board is connected with high power connectors on top of the standard 4-layer FR4 PCB. Since it stands out of the usual 10 × 10 cm stack format, it can easily be connected to the main heat sink of the electronic module, therefore providing an efficient heat transport during the flight.

The PCB carries the circuitry for diagnostics, interface and the PID controller, as well as load and battery connectors. To reduce the ohmic resistance of the high current path and thus the excess heat, the PCB-wires have been freed from any solder resist in the design, and have been enhanced in their conductivity with soldered-on solid silver wire.

5.4. Bipolar Coil Current Driver (BCCD)

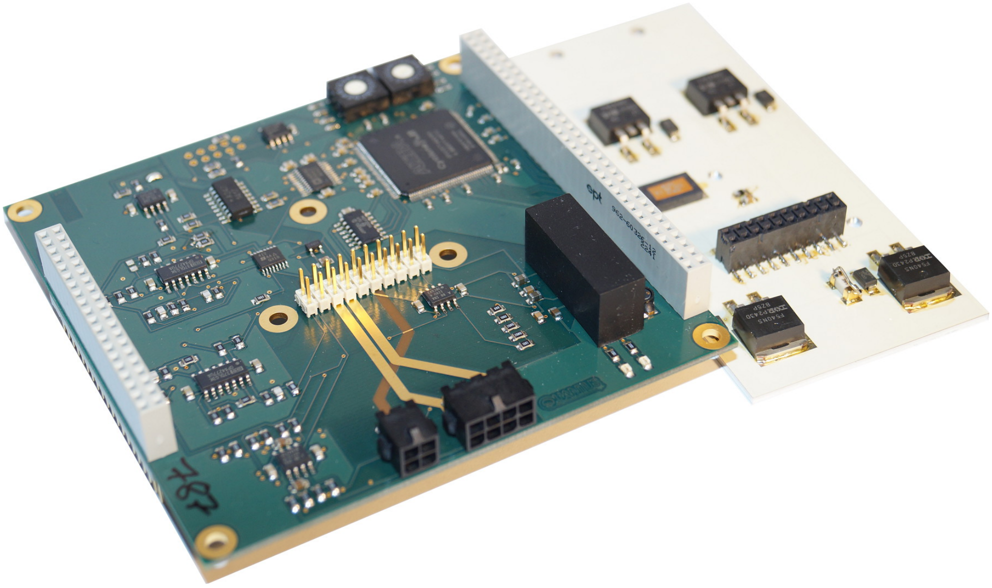

FIGURE 5.11.: Controller and power board of the coil current driver. The four power transistors form the bridge amplifier, resulting in one bipolar output.

The concept of the UCCD provides high current rates in several galvanically connected loads with low, almost completely ohmic impedance. For inductive compensation coils, which usually complete an atomic chip trap, the application parameters differ. These coils, although relatively close to the chip itself, hence not very demanding current-wise ($I < 5$ A), feature a high number of windings to create the necessary offset fields without excessive power requirements. Therefore, both resistance and inductance vary significantly compared to an atom chip[19]. Additionally, compensation coils are not galvanically connected, hence the experimental design stipulates only one 3-cell battery for all coils[20]. Eventually, these circumstances favor a different design approach for the current drivers employed, as the bipolar operation of the coils, although in principle possible with two galvanically separated chip driver instances, is not realizable with the given single battery configuration.

5.4.1. Amplifier design

The design for current driver circuitry needs to account for several constraints. First of all, the fast switching with minimal overshoot due to the inductance of the coils has to be realized. Therefore, the differentiating part of the PID controller has to be used more extensively to create a phase reserve, inhibiting overshooting behavior of the current driver. To create a bipolar current flow through the load, an amplifier in form of a class-B bridge-tied load (BLT) was chosen.

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[19] Detailed values can be found in appendix B.4

[20] ref.: section 5.4.2

Although contemporary applications, e.g. modern audio amplifiers, use the H-bridge in a pulse-width modulated configuration [97, 367f.], an analog approach for the bridge is used. Otherwise, the employed digital modulation of a PWM system would rely on frequencies which typically lie close to anticipated LARMOR-frequencies, which would increase the probability of noise induced losses. Depending on the polarity of the analog control signal, a corresponding diagonal N-P pair of transistors becomes conductive, thus enabling bipolar current flow through the load (figure 5.12).

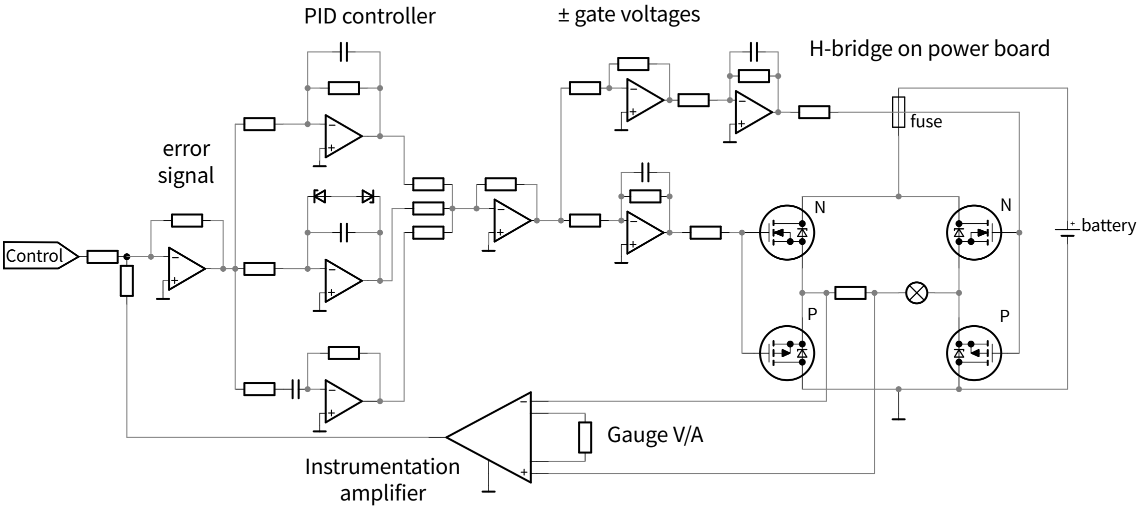

FIGURE 5.12.: Simplified schematic of the BCCD architecture. The ZENER-Diodes in the integrator provide a simple, however non-ideal suppression of the integral windup while maintaining a high integrator gain for small error signals.

The actual current flow is determined by a ground-free measurement on a shunt resistor in line with the load via an instrumental amplifier[21]. With this approach, the required currents for all estimated trapping situations of ^{87}Rb could be realized[22].

5.4.2. Grounding concept

In the case of QUANTUS-2 and MAIUS-1, the current drivers were to be used on galvanically isolated compensation coils, which is why only one battery is envisaged for the whole coil driver unit.

Figure 5.13 shows a schematic, which features two driver modules on separate loads (1,2) powered by the same battery. Due to the galvanic isolation of the controllers, current flow is separately controllable for each load. The 1 µF capacitor provides an AC coupling of the grounds. However, it is crucial to maintain the isolation of the battery all the time in order to inhibt cross-talk between several instances. Particularly when charging the battery, it must be ensured to maintain isolation from the TBUS ground.

5.4.3. Data input

The firmware structure is just marginally different from the one described in section 5.3. The circuit features, as a concession to number of transistors used for one amplifiers, only one

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[21] [TI INA 128]

[22] For details on the sequence, refer to section 3.1

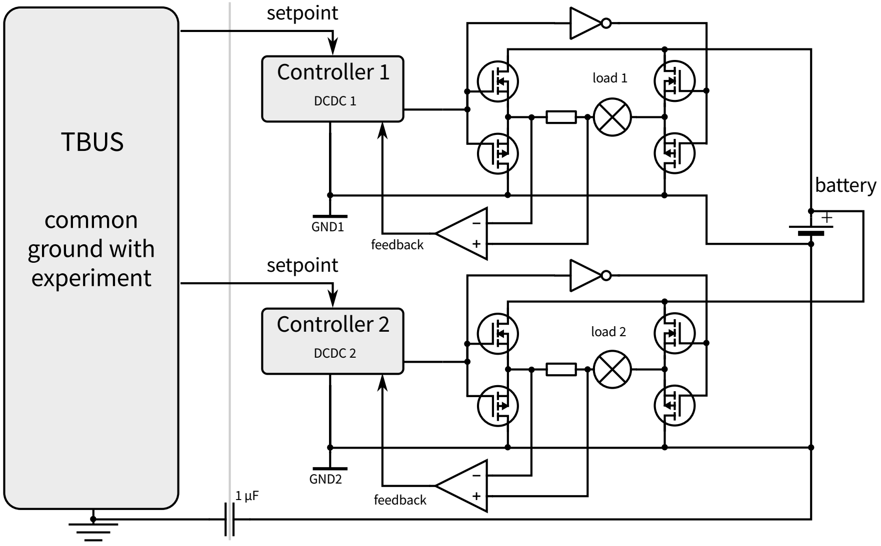

FIGURE 5.13.: Schematic of grounding for the bias coils with their respective driver architecture. The common battery ground has to be isolated from the TBUS in order to inhibit cross-talk between two driver instances. The differential current measurement is performed by an instrumental amplifier on a shunt in series with each load, afterwards referenced to the corresponding controller ground.

driver, hence it is only using one DAC channel. Due to the lack of information by a second battery, the ADC is replaced by a 4-channel version with the same interface. The current flow is bipolar, so the diagnostic measurement of the current is offset via a voltage divider on the differential amplifier to enable digitalization with an unipolar ADC. The conversion differences are denoted in further detail in appendix C.

5.4.4. Limitations on the use of the circuit

With the design of the BCCD, it has not been intended to provide an all-purpose solution to drive compensation coils. Therefore, as useful as they may be in the context of MAIUS-1, it is mandatory to discuss their limitations in a wider context of possible application.

The bridge-tied-load architecture places the source potentials of the power transistors on the two sides of the load itself. Hence, an imbalance of potential occurs, which results in a raise of the high-end transistor's source potential by the voltage $U_L = R_L \cdot I$. Temporarily, the transistors gate-source voltage becomes smaller, resulting in smaller conductivity. This must be compensated by a rise in the control voltage U_control on the gate. In order to keep the current driver operable, the maximum output voltage U_max of the controller must thus not be exceeded by the maximum load voltage on the current, combined with the threshold voltage U_th of the transistor, to enable conductance. This leads to the restriction on the maximum battery voltage U_Bat:

$$U_\text{Bat} \leq U_\text{max} - U_\text{th} - U_\text{control} \tag{5.1}$$

This inequality holds true in the case of MAIUS-1 with a battery voltage of roughly 10 V and a maximum current of ≤3 A in the most resistive coil, which makes this curtailment acceptable.

However, one could think of situations, where higher supply voltages might be necessary for additional experiments. Given sufficient number of module slots, this could be provided by using two UCCD of different polarity on one coil, which would in total only need extra space for one additional battery in comparison with the BCCD[23]. Anyway, this is probably not the best solution, as the UCCD are not been optimized to handle inductive loads. Hence, an improved amplifier stage is a design goal in successor versions of the BCCD.

5.5. Simulations of performance on inductive loads

The introduced hardware provides an important cornerstone of the current control in the experiment. Moreover, the determination and calibration of control parameters, especially for the feedback controlled PID modules, is a key feature to provide a complete design portfolio for current drivers in the context of atom chip experiments. Hence, for all designed modules, simulation software has been employed to create realistic models of loads and circuitry, enabling the experimentalist to evaluate certain PID settings in their validity for the designated purpose of the current driver under investigation. The development of these simulation models has mainly been driven by various motivations.

Firstly, it is imperative to determine whether certain amplifier models are efficient and functional to deliver high currents fast enough while maintaining distortion free switching performance. Therefore, using the program `TINA-TI`,[24] a large quantity of possible PID settings can be evaluated in transient analysis, in order to determine the waveform of the step response functions on several virtual loads.

Especially in the case of inductive coils, these numerical calculations are of great value, since the damping of the current driver due to inductive currents is much harder to incorporate in simple calculations of switching response. Moreover, as we have seen in section 4.2.5, the design goal of switching times below two milliseconds is only achievable with optimized PID settings. Since the minaturized design of UCCD and BCCD have fixed controller parameters, which can only be modified by cumbersome part replacement, the determination of these constants without heuristic iteration is of the essence to keep the time constraints to a minimum. A a result of these investigations, given the measured experimental parameters during manufacturing of the experimental chamber[25], initial factory settings for the MAIUS-1 current drivers have been determined, which are already close to the optimum of those in the final experimental configuration.

Finally, the bandwidth of circuits and possible resonances of the amplifier, especially when operated on inductive loads, are of great interest during the design phase. Using the AC transfer characteristic simulation of the software, it is possible to obtain BODE-plots of the circuit as a whole, enabling to predict the behavior of current flow depending on switching times. This gives not only insight in the possible resonant behavior but also illustrates the bandwidth of the current control as well as possible noise sources in the output spectrum.

The following section will introduce some useful insights that have been determined during simulative evaluation of the circuits. Although there are models for all circuits, most simulation effort has been invested in the model for the BCCD, since inductive loads pose the most complex load for current drivers in chip based traps. The rather trivial behavior of ohmic loads on the UCCD will therefore not be covered.

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[23] Figure 5.10 shows two UCCD in exact this configuration.

[24] short for *Texas Instruments* SPICE. A derivative of the *simulation program with integrated circuit emphasis (SPICE)* software with additional simulation files for ICs developed by Texas Instruments.

[25] ref.: appendix B.4

Step response of the Y-coils

Most experimental processes, like the optical state transfer or magnetic lensing, rely greatly on optimal switching of the magnetic compensation coils. In experiments described in this work, those coils are oriented in all three axes in HELMHOLTZ-configuration, relative to the atom chip surface. The X- and Z-coils have a medium number of windings, therefore their switching is easily controllable. The Y-coils, however, differ widely from these features, and will therefore be presented as the most complex example of simulation.

The Y-coils provide the bias field for trapping in the MOT and the purely magnetic, IOFFE-PRITCHARD-type traps. Their relatively high resistance of 2.9 Ω, due to the mere length of wire, in combination with the high inductance of 4.72 mH, due to the large number of windings, result in a unfavorable impedance when it comes to switching. The design goal for step response time was stipulated to be 2 ms, matching the values achieved in QUANTUS-2. In the same manner, the maximum current was determined to be ± 2.1 A. However, these values prove to be very close to the physical limit, provided that only 9.6 V of battery voltage are available in MAIUS-1, compared to ample 20.6 V in QUANTUS-2.

For the application in atom optic experiments, not only a fast step response curve is desired, but also a smooth one, with minimal overshoot and fast settling. With proper optimization, an ideal PID-controller can achieve such a curve easily, given the right control parameters and infinite voltage reserve. In our case, a PID controller with limited control range (battery voltage), a non-linear output stage (class-B BLT), additional delay (inductance of the coil), and cumbersome variation of parameters (solder options on integrated modules), the optimization of switching waveforms does not underly simple textbook behavior and can't be evaluated empirically. Thus, a substantial effort was spent on simulated optimization switching performance. Furthermore, the passive impedance matching of a coil on a fixed controller setting will be treated, as it is still the method of choice for commercial current driver as in QUANTUS-2.

5.5.1. Integral windup

One of the first results of the simulations, is a common problem in analog PID controllers with a nonlinear gain curve. The BCCD process value, the output current flow, depends nonlinearly from the inductance of the load. Thus, for the limited output voltage, to counteract the inductive countervoltage, the controller output rises, without influencing the process value further, resulting in an overdrive, after reaching the moment of current control again. This results in a massive overshooting, commonly described as *integral windup*. As this effect depends on the change of the current amplitude, $\mathrm{d}I/\mathrm{d}t$, a linear controller, such as a simple PID cannot compensate this behavior.

The impact of the integral windup is characteristic for the analog circuits employed as amplifiers, but also occurs in almost every controller to some extend. Integral windup is considered one of the biggest disadvantages of analog PID regulations, especially in the case of a nonlinear control path, as it is the case with inductive loads. There are several methods to limit the negative influence of integral windup [98]. Most of them are easily implementable with digital controller concepts, which are unfortunately not accessible in the existing designs, which rely on analog feedback controllers. The remaining concept of compensation is the adaption of the controller output curve to the limitations posed by the load itself, hence in this case introduce a nonlinearity into the regulation, which mimics the behavior of the process value.

By scaling the output gain of the integrator empirically, suitable to the load and its current control behavior, it was possible to mimic the saturation of the inductive coil by introducing

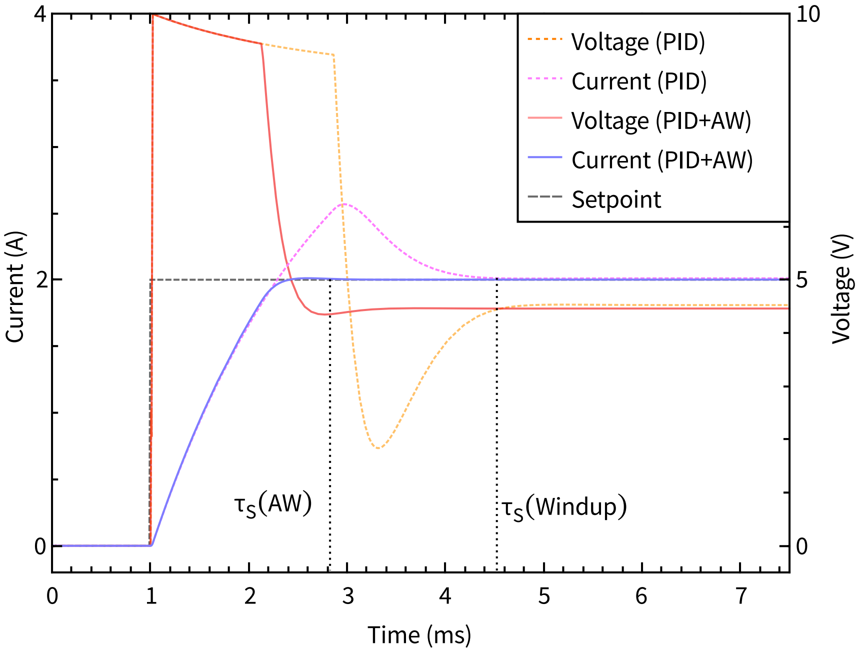

FIGURE 5.14.: Integral windup of a current driver. The figure shows a direct comparison of the standard PID controlled current driver (dotted) with the modified anti-windup solution (solid line). The settling time τ_S is not only strongly reduced, but also the switching overshoot is smoothed out, enabling an operation with almost optimum parameters. For smaller current steps and small impedances, the two controller designs show almost identical perfomance.

ZENER-diodes as bypass in the feedback of the integrator. This allowed for fast integration for smaller differential current jumps while suppressing overshoot during large setpoint changes. Figure 5.14 shows a direct comparison of the cases with a simple PID and the applied anti-windup solution.

Despite the improvements, this approach is far from an optimal solution, as it has to be carefully adapted to each load and varies slightly in efficiency due to temperature dependency[26] of the ZENER-voltages.

Additionally, the unavoidable nonlinearity of the current- voltage-characteristic of the ZENER-diodes again distorts the linearity of the current driver, as there are slight potential shifts in the integrator due to the minimal leakage currents. Since this occurs within the controller path, it is not mitigated by feedback control. Figure 5.15 gives an estimate of the residual deviation from the linear gain for several configurations. If exaggerated, the anti-windup solution can lead to distortions in the linearity of the output (blue). This can be more extreme, if the controller output approaches the breakdown voltage of the ZENER-diodes. The deviations of the currents can be easily compensated with software calibration of the drivers against a reference multimeter, if one would focus on the switching performance. However, with careful adaption, one can achieve a combination of improved windup suppression without sacrificing the linearity in the relevant application band (green curve).

The parameters for MAIUS-1, finally, were chosen to deliver optimal switching curve shapes in the current range up to 2 A, leaving residual windup for higher jumps, which do not occur in the experiments performed in this mission. Although not very sophisticated and added to the existing hardware design, the anti-windup solution of the BCCD, after implemented lead to a

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[26] Depending on the parts, it is possible to achieve almost vanishing temperature coefficient for diodes with ZENER-voltages close to 5.1 V. However, in the case of MAIUS-1, the cutoff voltage lies slightly higher, so one would expect a small temperature drift.

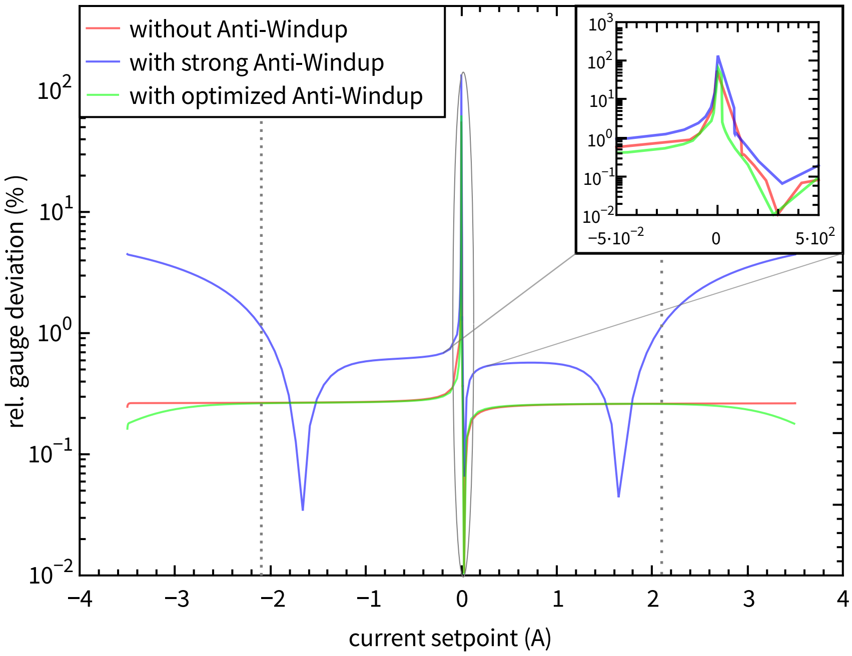

FIGURE 5.15.: Deviation from a linear current gauge of the BCCD on the Y-coils with and without anti-windup measures. Although generally improving switching behavior, a strong windup suppression introduces a nonlinear distortion in the output current values, in contrast to the non-improved controller, which performs close to the expected value with the given part precision. An optimized anti-windup manages to have competitive performance in the designated MAIUS-1 current range, while maintaining the improved switching curve. (Note: The singularity close to zero, which is shown zoomed in the upper right corner, is an effect of the limits in current measurement and the numerical simulation, which leads to high calculated deviations for currents below 10 mA. The offset is a calibration deviation resulting from the limited precision in part values of the simulation.)

significant improvement of switching behavior in comparison to commercial current drivers[27], which will be further exploited in future design iterations of the coil current driver design.

5.5.2. Resonance behavior of inductive loads

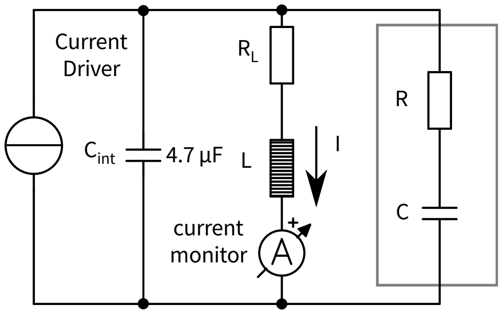

FIGURE 5.16.: Simulation setup of the Y-coils. The added RC circuit in the dotted frame changes the switching behavior of the coil drastically.

It has been already determined in QUANTUS-2, that inductive coils can have a negative resonant influence on the current output of a feedback controlled current driver [22, sec. 2.8.3]. The phase shift introduced by the impedance of the bias coils thus slows down the switching performance of the whole trap setup significantly.

QUANTUS-2 was equipped with the commercial current drivers `[BCS-10P]`, which are optimized for ohmic loads, and filtered internally with a capacitor C_{int}. For an inductive load with a inductance L and a resistance R, this leads to a resonant RCL circuit. Thus, the operation of the `[BCS-10P]` atom chip drivers[28] on the bias coils of QUANTUS-2 resulted in massive overshooting when currents are switched, which is not controllable by the

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[27] see comparison in figure 5.21

[28] These current drivers only allow for very coarse changes in the PI-only controller parameters, which did not enable precise optimization of switching performance for atomic chip traps.

current driver, as it only measures the output current, not the current trough the coil itself, while the oscillations within the RCL circuit create a disturbance in the resulting magnetic field.

In QUANTUS-2, a parasitic RC-circuit (figure 5.16) has been introduced in parallel to the coil, in order to dump excess current in a chargeable, damped depot to inhibit oscillation. While good working values for R and C have initially been obtained empirically for QUANTUS-2, the new current driver design for MAIUS-1 made it mandatory to gain a more detailed comprehension of the impedance for different coils in combination with the BCCD, since this method has been initially proposed for MAIUS-1 as well.

The load itself, with the internal capacitor of the current driver, forms a third-order lag element in control theory. The third order in this case describes the number of independent energy storages within the system (C_{int}, L, C) . With the numeric simulation software SPICE, the transfer functions of this system have been calculated numerically for the values of the MAIUS-1 y-coil. To analyze the current flow, an ideal current source is assumed, driving current through the load network. The AC current response function I_L/I_{in} is then calculated and plotted in a BODE-diagram. The values of R and C are varied to show their influence on the transfer function. Additionally, the corresponding step response of the coil current to an ideal switching of 0 A to 1 A on the input is shown for the different cases around the previously identified optimum (figures 5.17 to 5.20).

Variation of C

The initial RCL system shows a strong resonance close to

$$\nu_R = \frac{1}{2\pi\sqrt{LC_{\text{int}}}} \approx 1068\,\text{Hz}, \tag{5.2}$$

as shown in figure 5.17. When adding a parallel capacitor, the resonance is shifted towards the DC and the damping is increased (orange). The sharp phase jump is washed out. The ideal position is the critically damped case (red) where the gain figure is ideally flat without a phase lag in the DC. The overdamped case (blue) instead does not much differ from the ideal case on a first glance. It is however notable, that the gain is slightly deviating from 0 already at 10 Hz, observable from the phase being < 0. The time-domain (figure 5.18) shows the differences of these cases in a more intuitive manner. Only the critically damped case reaches the desired setpoint in a sufficiently short time period. We find that $C = 100\,\mu\text{F}$ is a good choice for the capacitor value.

Variation of R

Given the rather coarse variational degree of freedom in the capacitor value, an additional resistor is put in line of the capacitor, in order to fine tune the current flow, thus varying the damping constant. For small values of R, the time-domain step response approaches the loading curve of a capacitor, thus creating a different resonance with an additional pole in the transfer function, as observable in the additional turning point in the phase relation diagram (orange). Large values of R become negligible in comparison with the uncompensated case, therefore have not a great enough impact (blue). With an optimum value of R, the damping becomes critical and the parasitic influence of the RCL circuit is neutralized, enabling almost perfect switching curves (red) (figures 5.19 and 5.20).

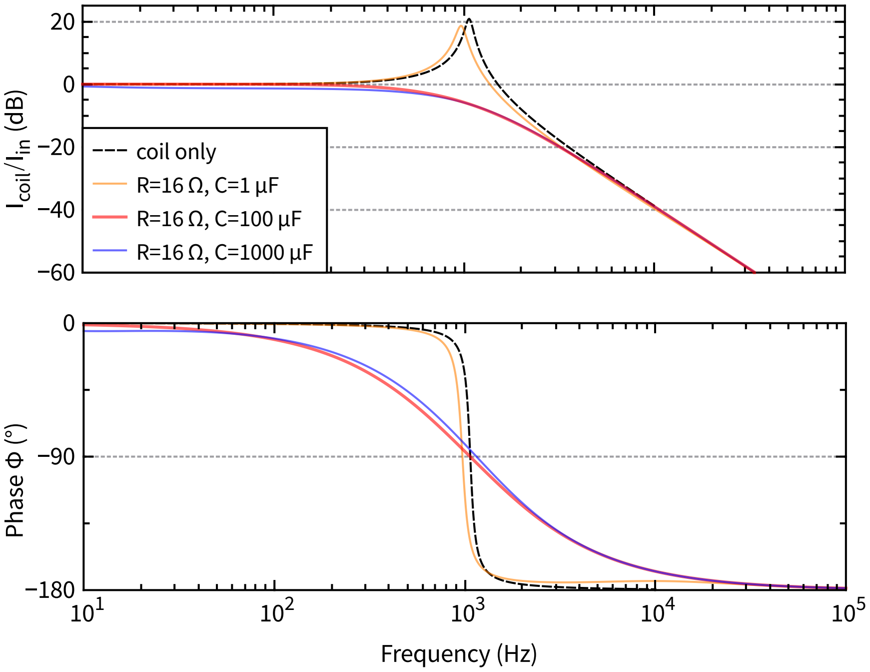

FIGURE 5.17.: Simulation of the Y-coils' frequency response (C-Scaling). Small values of C lead to a resonance shift with a phase jump(orange), higher values of C limit the bandwidth too far to the DC, therefore turn to overdamping(blue). An ideal gain figure is reached for the critically damped case (red).

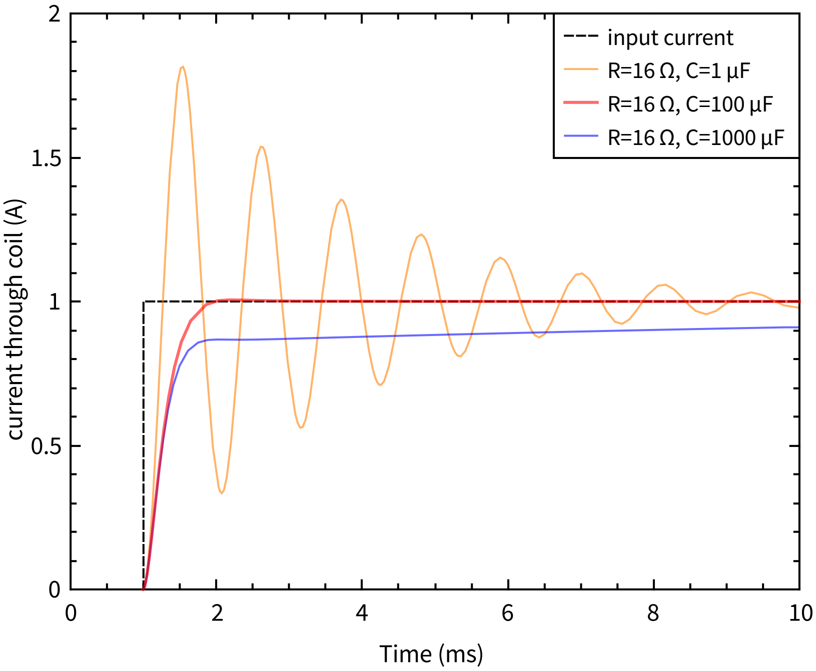

FIGURE 5.18.: Simulation of the Y-coils' frequency response (C-Scaling) in the time domain.

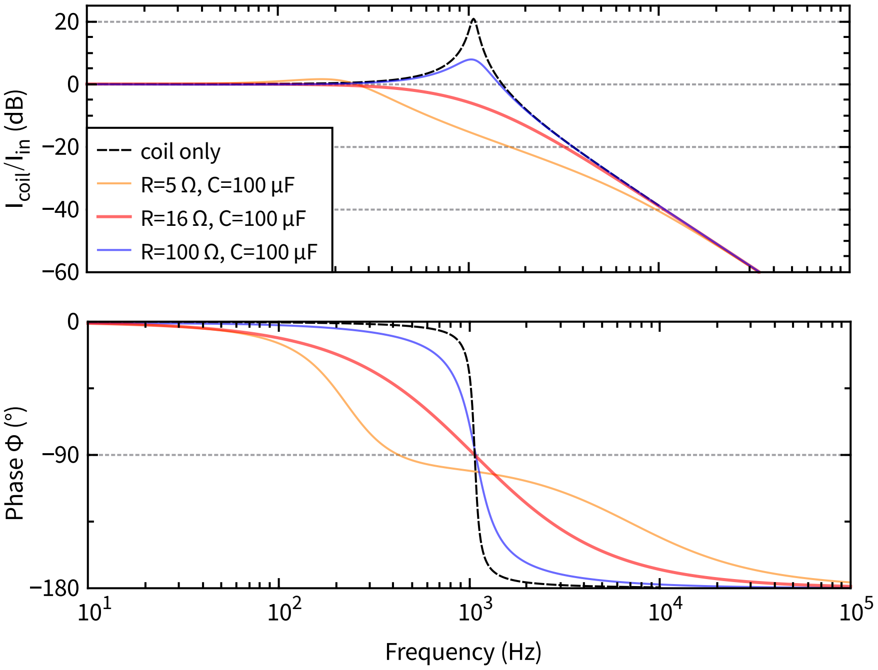

FIGURE 5.19.: Simulation of the Y-coils' frequency response (R-Scaling). Small values of R lead to a resonance shift with a phase jump, higher values of R do not deliver necessary damping to move away from the undamped resonant case.

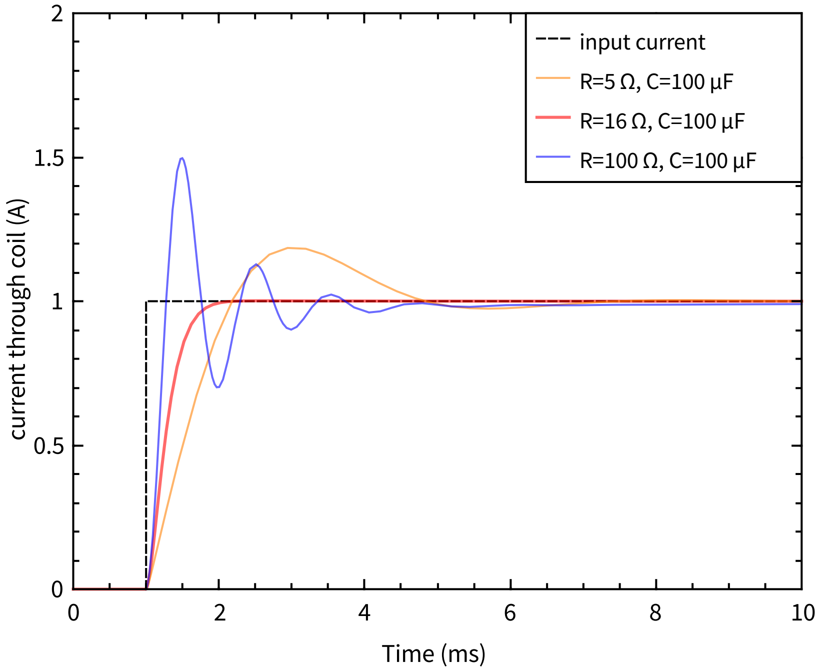

FIGURE 5.20.: Simulation of the Y-coils' frequency response (R-Scaling) in the time domain. The impact of the C variation is much easier to observe than in the BODE-plot.

Optimizing the BCCD switching for MAIUS-1

The findings above help to improve the BCCD switching as well, as the already mentioned integral windup also introduces the same type of current delay as a capacitor, leading to similar oscillation. Therefore we investigate, if a RC circuit, as evaluated before, can improve switching performance of a BCCD in PI-mode as well.

As a first step, the ideal current source in the simulation of the load is replaced by the full model of the BCCD, with controller settings comparable to the `BCS-10P`[29]. The values of L and R_L are taken from a measurement at the MAIUS-1 hardware. Afterwards, the current step response and the voltage drop on the load are shown (figure 5.21, upper graph).

In the next step, the introduction of the RC circuit with the values determined in the impedance analysis enables the user to improve switching performance without changes in the parameter settings of the controller. Figure 5.21 illustrates the difference of initial oscillating situation and impedance matched load (middle graph).

As a complementary method, the RC circuit is again removed, and the full PID setting of the BCCD is optimized using heuristic value alteration and step response analysis. The performance with such optimal settings, along with an anti-windup solution, is shown in the lowest graph of figure 5.21. With the optimized PID settings, not only the switching time is faster, but also the current control through the load is directly controlled by the current driver again. This shows the superiority of the PID controller design of the BCCD compared to their predecessor electronics, which is why it was the method of choice for MAIUS-1.

Remarks on the RC-method

Although omitted in MAIUS-1, the RC circuits of QUANTUS-2 are still in operation. This is only the case, because their commercial current drivers are incapable of delivering a control level comparable to the MAIUS-1 circuitry. Although it might seem appealing to use the simple method of adapting a resonant circuit to a »standard« regulator configuration with the BCCD, instead of careful determination of the optimal PID performance, it is under no circumstances advisable, for the following reasons:

- The values of R and C are temperature-dependent. In the case of MAIUS-1 this could lead to shifts in the resonance, which are hard to track with the expected temperature gradients during the flight, and possibly worsen the quality of the impedance matching.
- The parallel damping element completes a resonance circuit. Therefore it is possible, that current oscillations remain, which are not visible in the coarse analysis of the switching curves by standard oscilloscopes, but introduce a current noise which has negative influence on experiments with atoms. Therefore, an oscillatory load has to be avoided.
- The level of control and damping can also be achieved with a customizable design and suitably modeled control parameters such as in the BCCD. In fact, a differentiating controller increases controller stability further, thus enabling for even faster settling times (figure 5.21, lowest graph)
- The RC-method defies control theory. The purpose of the current driver, to measure and control the current flow through the coil, is inhibited by introducing parasitic currents from a parallel circuit, which cannot be controlled by the current driver itself.

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[29] weak P, strong & fast Integrator, PI regulation only, no anti-windup modifications

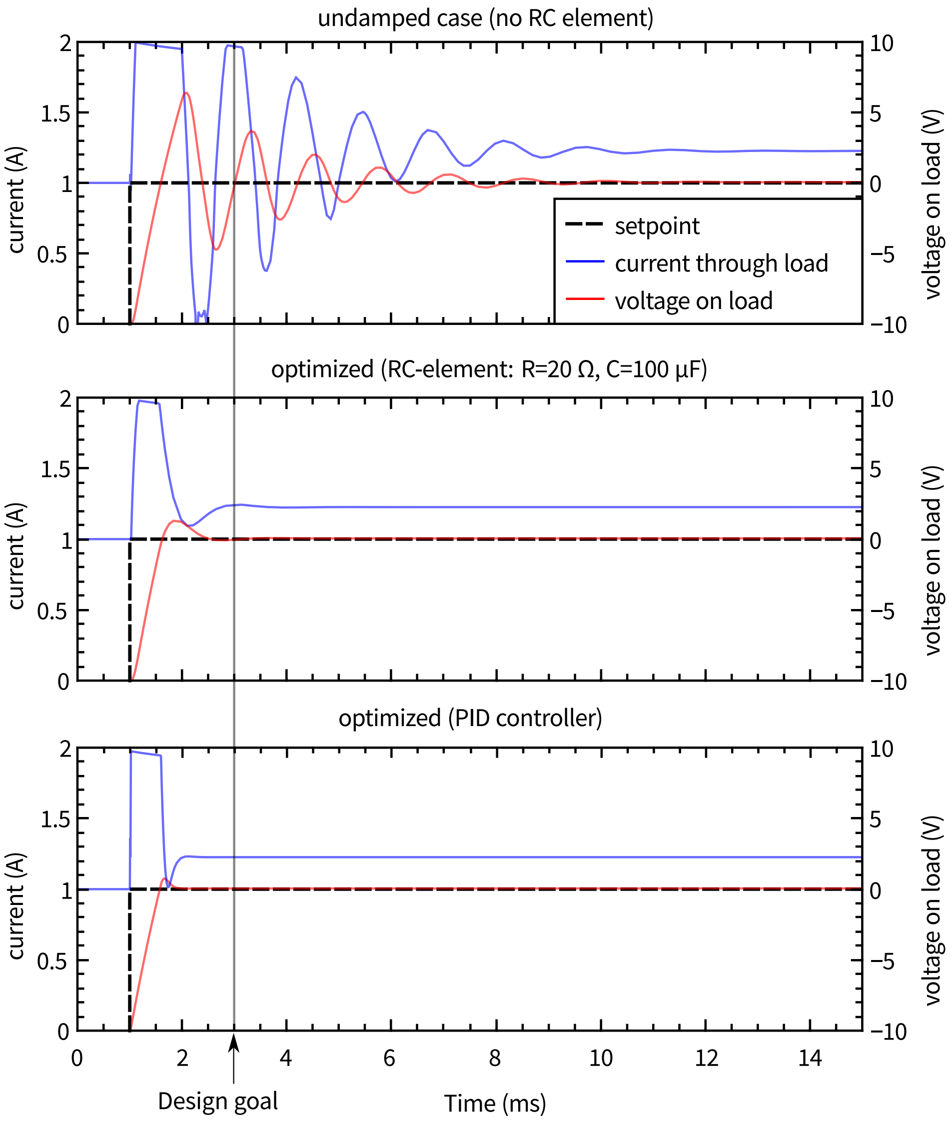

FIGURE 5.21.: Comparison of step response functions of the Y-coils. The voltage drop on the load illustrates the impairment of the switching due to the coils' impedance (upper graph). The introduced damping element (middle graph) circuit improves the switching drastically due to damping of the overshooting inductive current. However, an a full-featured PID controller (lower graph) is able to surpass the RC-circuit's performance without the need for additional parts in the current path of the load.

> Therefore the control of the magnetic field is only as good as the RC matching allows, independently of the current driver.

After careful evaluation of these problematics, an exchange of the existing coil current controllers for QUANTUS-2 is to be investigated in the near future.

5.5.3. Scaling behavior

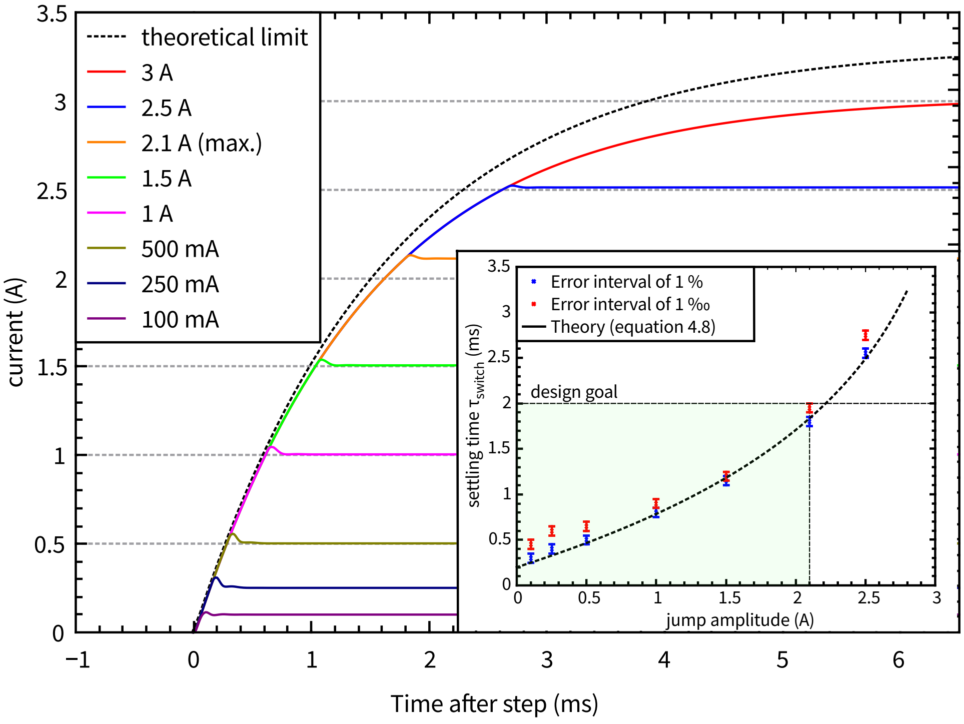

FIGURE 5.22.: Switching waveforms of the Y-coils for variable setpoint jumps. The theoretical limit given by equation 4.6 is a good estimation for the step response time between 0.5 A and 2 A. In the other regions, deviation effects of the amplifier architecture become visible.
INLAY: Simulated settling times for the Y-coils. Depending on the tolerable error interval, the settling times vary slightly. It is notable, that for 1% deviation (blue dots), the estimated PID switching time of 200 µs from chapter 4 has been a good approximation of the controller behavior, since the simulated settling times are close to the theory curve. For the 1 ‰ (red dots) interval, however, the settling times are slightly worse, but are still within the initial design goal range (green area).

Since the gain of the controller output is nonlinear, it is necessary to test the found optimum of PID settings for the full scale of available current jump amplitudes. As figure 5.22 illustrates, the transient figures are depending additionally on the requested current, which is a result of the nonlinearity of the BLT-amplifier. The height of the overshoot is depending on the level of voltage that is available for the current control. For small current jumps, almost no overshoot is experienced. For intermediate amplitudes, the overshoot is the highest ($\approx 15\%$), whereas for large current jumps, the overshoot level decreases, due to the limit of available voltage.

Another limitation of the amplifier is its deviation from the theoretical limit of an ideal coil (equation 4.6). This is explainable by the rising resistance of the MOSFET employed in the bridge-tied load (BLT). As the maximum voltage is applied to the load, the gate source-voltage available to open the bridge is closer to the threshold, therefore the resistance of the MOSFET rises, effectively reducing the available maximum voltage available in (figure 5.22). Unfortunately there is no way to circumvent this problem in the current layout of the circuit, but on the other hand it is not limiting the operation of MAIUS-1, as the time-critical experimental parameters for the Y-coil are well below 2.1 A.

As a better insight into the switching performance, the step-response waveforms of figure 5.22 have been evaluated in relation to their deviation from their steady state value. With a step size of 50 µs, the entry points into error intervals of 1% and 1 ‰ around the setpoint have been identified and are shown in the inlay of figure 5.22, for several jump amplitudes.

5.5.4. Reduction of the overshoot

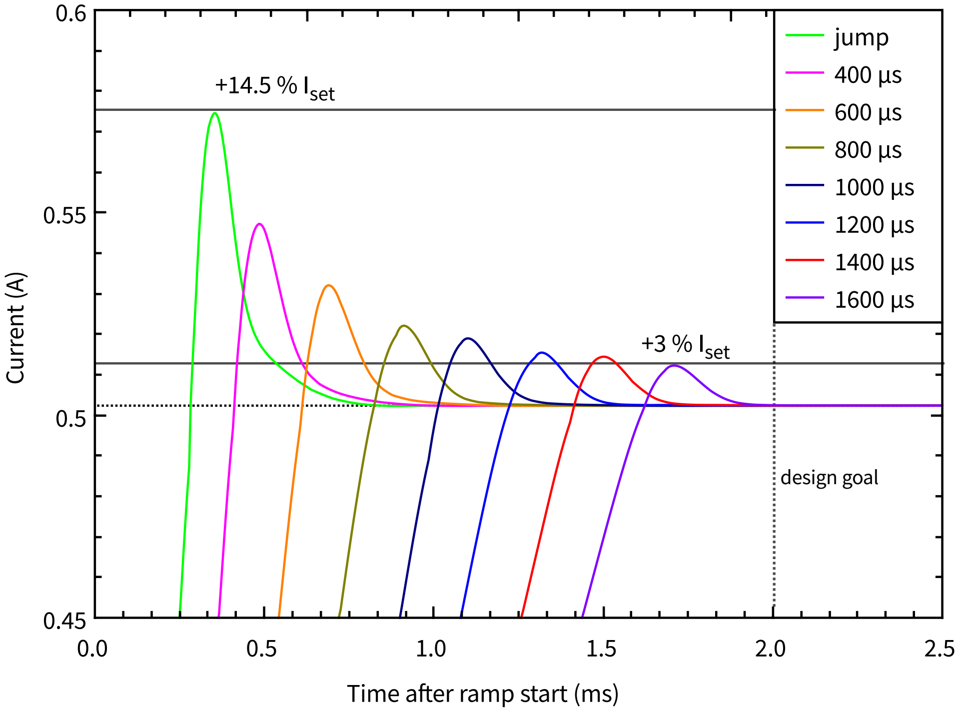

FIGURE 5.23.: Influence of input ramps on the step response. In comparison to a jump, with an overshoot of 14.5 %, a slower, linear increase of input voltage can reduce the overshoot to 3 %, while still maintaining the design goal of 2 ms settling time.

As initially remarked, the ultimate purpose of the BCCD is the control of the magnetic field delivered by the coils. In order to suppress any reaction to overshooting of the current due to PID behavior, it is helpful to further enhance the switching with adaption of the rise time of the analog input, if the application makes it necessary. This is very easy with the ramp feature of the firmware. Figure 5.23 illustrates the influence of various ramp times for a current jump of 500 mA, where the overshoot of the step response is largest. With careful reduction of the input voltage slope. The initial overshoot of 14.5 % can be reduced by over 11 percent points, ending up with only 3 % overshoot. While achieving this, the controller is still compliant with the stipulated maximal settling time of 2 ms.

The timing is varying by the amplitude of the jump, therefore it must be evaluated carefully, if the desired effect persists when changing the amplitude. The optimization is, in the case of the Y-coils, most interesting for intermediate currents in between 100 and 1000 mA, since this amplitude interval features the highest relative overshoots of up to 15% with the simulated PID settings. For current jumps with an amplitude above 1.5 A, although they usually do not occur in MAIUS-1, the overshoot is smaller due to the nonlinearity of the transient response.

Ultimately, for every physical aspect, the trade-off between fast settling time and overshoot has to be carefully weighed by the experimentalist.

5.6. Chip Safety Circuit

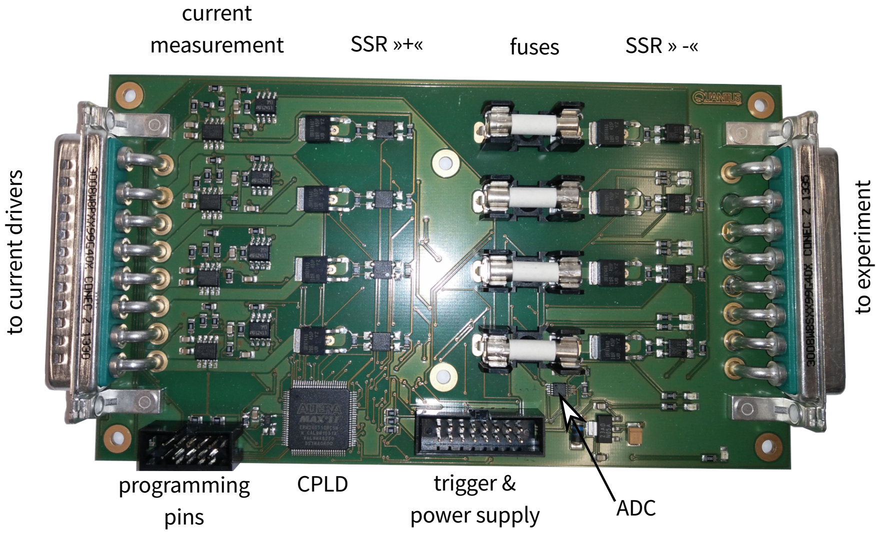

FIGURE 5.24.: Photograph of the Chip Safety Circuit. Each board supports four chip/coil structures with timing and bidirectional excess current protection. The central CPLD is programmed with a firmware to provide timing for additional protection with cool-down periods. A detailed schematic is documented in appendix D.1.

Although the MAIUS-1 current drivers are very reliable, there is always a possibility of circuit failure. The timing of the current jumps and ramps, for example, relies on a functional TBUS infrastructure. A failure or distortion of the global experiment clock could lead to disastrous consequences, e.g. a current-induced melting of the delicate chip structures.

In order to protect each load separately, within their subsequent parameters, another layer of safety has been introduced in form of independent safety circuitry. This circuit, while creating its own timing reference with a quartz oscillator, provides four conductor lines to act as an intermediate control instance of current flow between current driver and load. A conductor line consists of a trigger input stage, a hall-effect current sensor[30], a melting fuse and a discrete solid-state relay (SSR), which can be switched without galvanic connection of Safety Circuit and load.[31]. In this setup, the circuit is designed to provide three basic functions:

- Switching of structures. The SSR effectively inhibits current flow independently of the respective current driver's calibration. On one end, this prevents undesired currents due to an error in the computer control, on the other end, it rules out minor idle current offsets, e.g. due to inaccurate calibration of the zero point for bipolar drivers. The switching occurs on rising edge triggers, in toggle mode.
- Timing limitation. Governed by the internal clock, the first trigger to open the load connection opens a time window with programmable constants (τ_1 »Timeout«, τ_2 »Downtime«). The constant τ_1 defines the timeframe after the first trigger, that allows for current flow. The timing counter is then reset after a time τ_2. Effectively, this leads

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[30] `[Allegro ACS711]`

[31] This is possible with a self-sustaining version of opto-couplers which can provide switching voltages for MOSFET only by the transferred optical energy. The part used in this design is Panasonic's `[APV1121S]`

to a dead time $\tau_2 - \tau_1$ in which triggers are ignored and no switching to »on« is possible. This provides for a »cool-down« period of the respective load to prevent overheating.

- Excess current protection. The current sensor delivers an analog output which is evaluated by a window comparator which basically sets a current range for which an error signal is zero. These error signals are evaluated by the complex programmable logic device (CPLD) which features an asynchronous switch off in case of excess current. Only the absence of errors and a reset trigger allows for further operation of the load.

In the current setup, the oscillator frequency of 1 MHz provides a timing with 1 ms precision and a reaction to overcurrent of ≈ 100 μs, limited by the turn-off time of the relays. Figure 5.25 shows the schematic of the firmware implemented in the CPLD. The detailed schematic is documented in appendix D.1.

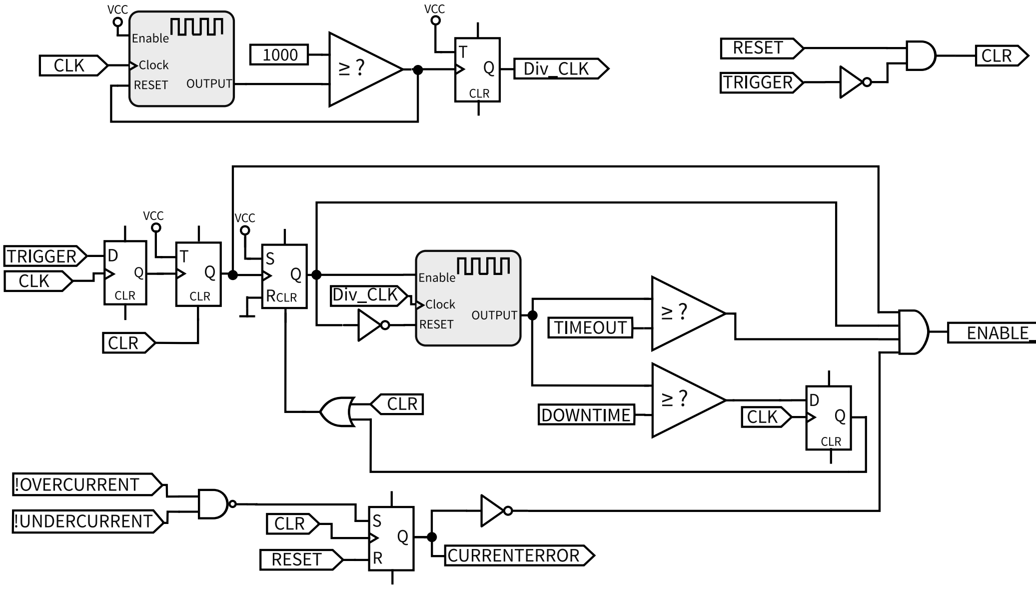

FIGURE 5.25.: Simplified schematic of chip safety firmware. The realization of this circuit has been implemented software-based in the CPLD on the circuit board[32]. The CLK signal is provided by a quartz oscillator, the signals RESET and TRIGGER are delivered by the main computer control of the experiment.

5.7. Summary

Challenged with the complex demands of compact atom chip based experiments, three sophisticated current driver designs have been introduced.

The versatile MAIUS lab-based current driver (MLCD) provides a easily customizable tool to explore experimental sequences for atom chip traps with tunable calibration and regulation parameters. The driver is independent of external support modules and can be operated on batteries or standard power supplies with analog control voltages. However, due to its need for two batteries for power supply and its mechanic delicacy it is not usable on the MAIUS-1 mission.

The unipolar chip current driver (UCCD) is the most miniaturized driver module, especially suited for atom chips. The modules feature two independent, galvanically isolated, unipolar current drivers on one circuit board, with a maximum current delivery of 10 A per driver.

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[32] [ALTERA MAX II]

Their TBUS software implementation allows for monitoring of driver temperature, battery voltage and current flow. Safety parameters inhibit overheating due to active shutdown at high temperatures. Additional to current jumps, the driver is also capable of performing linear ramps.

The bipolar coil current driver (BCCD) represents the most complex circuity developed in this work. It contains adaptions and improvements for current driver operation on inductive coils. Its BLT amplifier output, combined with galvanic isolation, enables for bipolar current flow through separated loads while using only a single battery power supply, hence allowing for a very lightweight setup of the electronics module. The full PID controller offers better control options than the PI stage of the commercial [BCS-10P], enabling the the BCCD to reduce and improve current switching performance compared to the QUANTUS-2 electronic.

The both latter modules can be operated in a completely remote setup in connection with the TBUS environment. In their integrated form, the complete communication for up to 12 modules is realizable via a single Ethernet connection, thus enabling for a very compact setup, comparable in size to just one single driver module of the predecessor experiment (figure 5.26). Aluminum components along with a decisive separation of heat generating parts provide a reasonable temperature stability compared to the overall power density.

The design evaluation with the SPICE models of each circuit delivered a very reliable method of finding the ideal switching parameters for each inductive and resistive load. These thorough investigations are necessary as battery voltages in the electronics module are very low, hence the specified settling time of 2 ms on the Y-coil for all current jumps is technically challenging, if not physically impossible in some cases.

The unfavorable problem of integral windup, occurring with the combination of low battery voltages and high inductances, could be successfully modeled and managed with a controller modification and sophisticated PID settings. Additionally, it has been shown, how a resonant inductance on a fast PI regulator can be managed with additional oscillating circuits, without interfering with the controller parameters. However, a direct comparison showed the BCCDs modified PID-controller to perform even better as the present solution in QUANTUS-2, in terms of shape and speed of current jumps, with very fast response rates, fulfilling all the initial specifications for MAIUS-1, despite the impairment of lower battery voltage.

With the ramp feature of the current drivers, the residual overshooting of the PID controller can be further reduced if the setpoint is ramped with an adapted time constant, reducing overshoot even further. With the sum of all generated improvement, the step response over the relevant current range could be improved close to the physical limit.

Since atom chips and their corresponding structures are usually very fragile, an coarse current surveillance has been developed, which limits current and time for the operation for each structure, independent from the TBUS and current driver operation.

With the usage of the novel designs, it has been possible to assemble the whole MAIUS-1 current driver stack of six atom chip drivers and four coil drivers in the volume of one single commercial current driver module (figure 5.26), which is more than an order of magnitude in size reduction and more than a factor of two in reducing battery weight. This technological advancement is an essential step towards miniaturized setups for chip experiments and presents a key technology for atom optics in space.

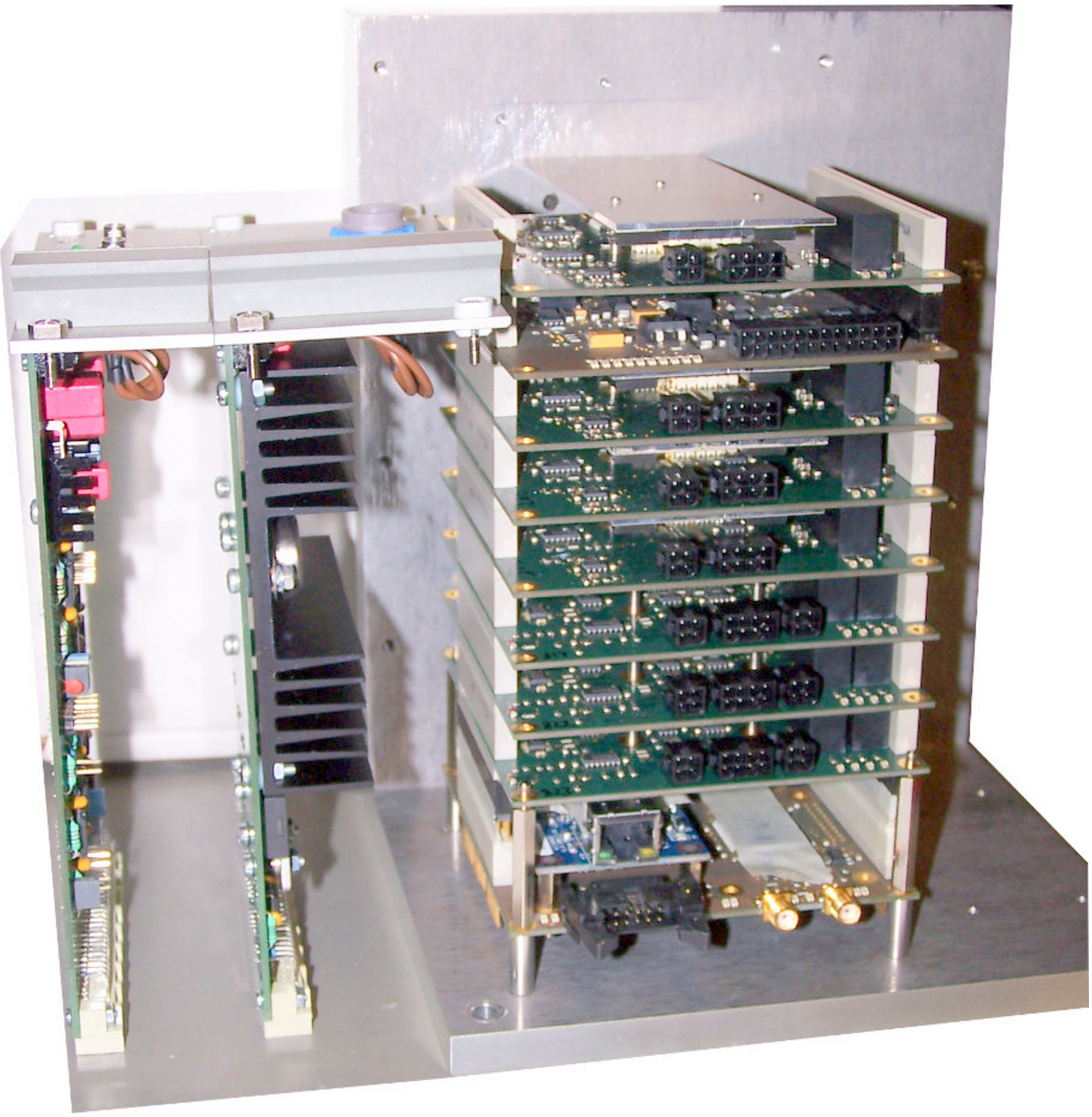

FIGURE 5.26.: Size comparison of one single HighFinesse BCS Driver module (left, without backplane) with the complete MAIUS flight current driver stack of three UCCD and four BCCD , including TBUS power supply and interface module. (right, the metal backplane is for mounting only and not necessary for operation.) Batteries not included.

CHAPTER 6

Characterization of the current drivers

This chapter reports on the characterization of the current driver designs employed in the MAIUS experiment, while focusing on the M-1 flight hardware and compares them with commercial devices. Regarding their operation for a chip based cold atom source, measurements in the following key aspects are presented:

- As discussed in section 5.3, the galvanic isolation of current drivers towards each other is a necessary feature when operating atom chips with galvanically connected circuits, such as in MAIUS-1. Therefore, the separation of current paths and absence of cross-talk between two current drivers on a chip-like structure is investigated.
- The crossover distortion of the bipolar coil current source, which occurs during polarity change due to the amplifier architecture, is quantified in order to assess its impact on the intended experimental sequences.
- The switching behavior, being one of the most important feature of a well adapted current driver, has become very well predictable with the extensive simulation tools available (section 5.5). An example of the agreement with the actual performance on the experiment's Y-coils will be shown to illustrate the excellent predictive value of the software simulation.
- The noise performance of all introduced designs, which is of paramount importance for loss mechanisms (section 3.3) will be compared with the previous state-of-the-art electronics[1], employed in the drop tower experiments. Exemplary sources of noise within the newly designed circuits are identified by comparative spectral analysis. Furthermore, selected cases of user-induced noise sources are illustrated.
- The current stability of the MAIUS flight circuitry is investigated in detail. Initially, the efficiency of the intended cooling provided by the layout is evaluated using thermography of the operating structures on a workbench.
- Both current drivers undergo temperature sweeps with several heating rates in order to characterize thermal drift. Furthermore, the stability of the current drivers in thermal equilibrium will be investigated in long-term measurements and analyzed with the ALLAN-Deviation method.
- Finally, the reproducibility of selected features of the integrated MAIUS-1 atom source are investigated and evaluated regarding thermal drift influences of the current drivers.

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[1] `[HighFinesse BCSP-10]`

6.1. Basic functionality

Apart from the obvious coarse range and calibration tests[2], the current drivers need to demonstrate basic functional tests. These insights are hard to come by with simulation alone, therefore showcase measurements are shown here.

6.1.1. Demonstration of galvanic isolation for the MAIUS Unipolar Chip Current Driver (UCCD)

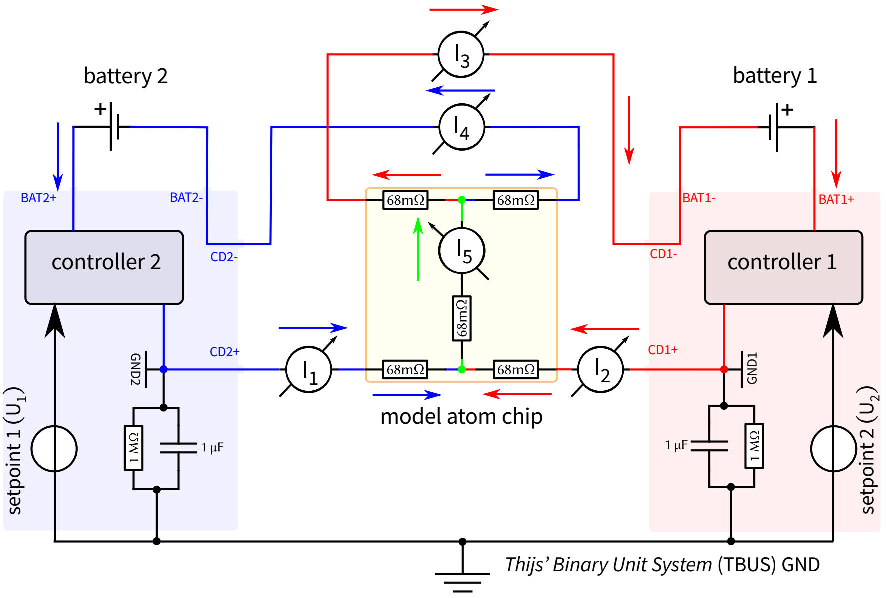

FIGURE 6.1.: Schematic of the atom chip measurement model. The two current drivers (CD1, CD2, in the red and blue frames) are controlled via two setpoint voltages (U_1, U_2), which are referenced to the common ground of the TBUS. The two drivers have high impedance isolation to this ground with their analog reference potentials (GND1, GND2), which are identical with the current driver outputs (CD1,2+). The two drivers are connected to an atom chip model (yellow frame), consisting of resistors. The current measurement points I_1-I_5 are compared to validate galvanic isolation. Note: The connector pins CD- and BAT- are directly connected on the current driver board, thus the currents I_4 and I_3 are identical with the respective battery drain.

An important property of the UCCD is the galvanic isolation, that allows for directed current flow in the connected wire structures of the atom chip. Although the MAIUS-1 mission only used one structure of each chip layer, the full exploitation of all designed chip structures in later experiments requires for independent current control.

The galvanic isolation and simultaneous operation of two current drivers (CD1, CD2) on one board are demonstrated with an artificial chip structure that features all the significant properties of an atom chip (figure 6.1).

Using a closed-loop measurement with a current sensor[3], the currents flowing through the relevant structures have been monitored and compared with the battery drain. Since the negative outputs of the current drivers are directely connected to the battery, the drain measurement and the currents of I_3 and I_4 are trivially identical, due to conservation of charge. Nevertheless, it is of interest to investigate the independence of the regulations. Thus, the switching waveforms of two drivers were tested for possible crosstalk.

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[2] Fine calibration was stipulated to be performed by software adaption by the experimentalists, as this would simplify a change of faulty modules in a field environment like ESRANGE.

[3] `[AiM Iprober 520]`

Current flow and battery drain were consistent all the time which is a good indication for galvanic separation on the board itself. To demonstrate the independence of polarity of the drivers, two examples of the measurement are shown in figure 6.2.

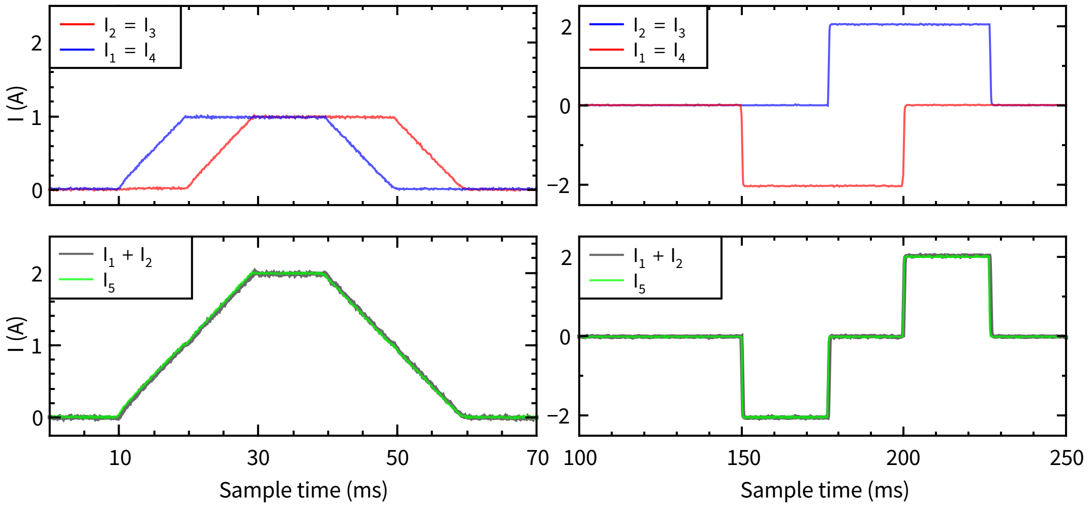

FIGURE 6.2.: Addition & compensation of currents on the model atom chip. UPPER LEFT: Depiction of current flow through the current driver outputs. LOWER LEFT: The middle structure shows the exact sum of the two currents, thus proving exclusive current flow over the chip. UPPER RIGHT: Two current pulses of the amount of ± 2 A are directed to the chip in opposite direction. LOWER RIGHT: The currents compensate each other in the middle wire of the model atom chip, hence proving bipolar isolated operation.

The two graphs show no visible difference from the calculated sum, derived from the two single measurements out of the positive current driver outputs and the measurement of the middle structure's current flow. Furthermore, the two right graphs show the capability of bipolar floating operation, with two currents of opposite polarity compensating each other. With these results, it is shown, that the UCCD provides all necessary functions for floating current delivery, as it was stipulated for the MAIUS-1 atom chip driver.

6.1.2. Crossover distortion of the MAIUS Bipolar Coil Current Driver (BCCD)

The bipolar operation of the BCCD with only one battery bears the inherent disadvantage of a short, but notable dead time while the regulation changes the direction of the current. This time is system-immanent for the circuit design of a »H«-bridge, and depends on the regulation speed of the controller output $\mathcal{R}(t)$, controlling the transistors, which conduct the current. While $\mathcal{R}(t)$ is smaller than the threshold voltage U_{thr} of the regulation transistors, current flow through the load is inhibited. While this can be beneficial to ensure quick turn-off, it can be of negative influence, if the dead zone of regulation signal voltages is not taken into account during switching through or close to zero. In order to validate the expected impact, a current jump typical for the QUANTUS-2-cooling sequence (section 3.5) was evaluated.

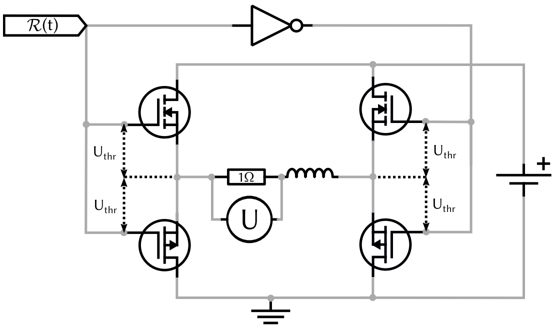

FIGURE 6.3.: Schematic of the crossover measurement. The resistor and the coil are connected to the H-Bridge of the current driver. The internal regulation voltage $\mathcal{R}(t)$ has to cross the » dead zone « of the gate-source threshold voltage ($|\mathcal{R}(t)| \leq U_{thr}$), to change the output current polarity.

The slowest reaction of any driver is to be expected with the PID-settings for the Y-coils due to its inductance and resulting PID settings. Hence, the upper estimate for the zero crossing time is determined with a measurement on a dummy coil with comparable values (figure 6.3).

Starting at 0.5 A, a jump of $\Delta I = -1$ A is performed. The current flow is monitored via direct measurement on the ohmic load (figure 6.4).

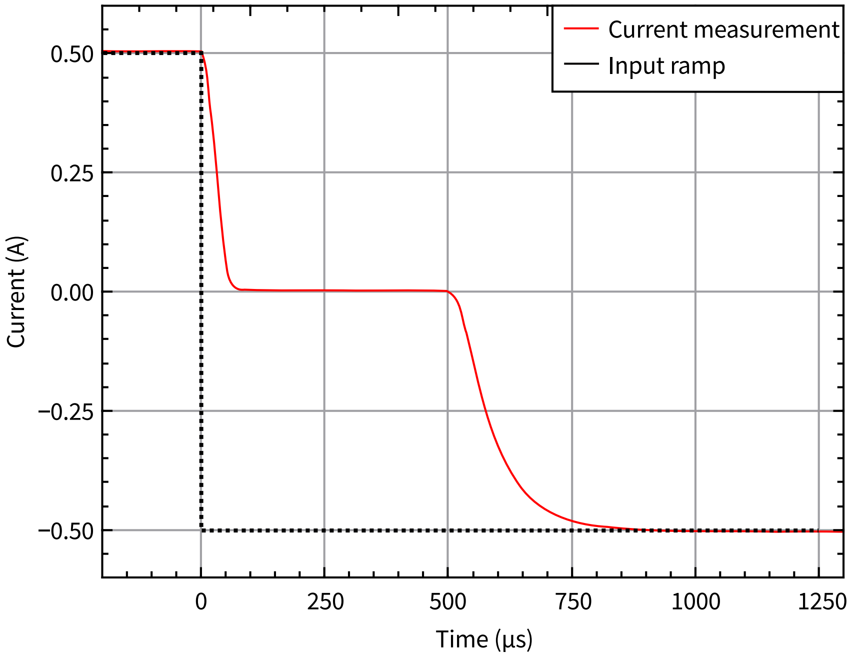

FIGURE 6.4.: Crossover distortion of the BCCD. Measurement of a 1 A-jump through zero on an ohmic load. Although the dead time is clearly notable, the final settling time of 1 ms is well within acceptable parameters.

Evaluating the current flow, it is notable, that turn-off is relatively fast, and the death time is approximately 450 µs. However, with an overall settling time of 1 ms, which is comparable to a normal step response, the switching performance is well within the stipulated settling time of $\tau_s \leq 2$ ms. It is noteworthy, that the value of the dead time is influenced significantly by PID settings and can be minimized by adapted switching ramps and jumps to values ~ 200 µs, which is sufficient for the MAIUS-1 mission.

So far, for the practical purposes of a the MAIUS-1 BEC-source, the currents are just jumped through zero, thus the optimization of continuous ramps with polarity change will be pursued in depth at a later development stage of the BCCD.

6.1.3. Test of Simulation results

For design and layout options of the PID control parameters, simulations of the switching behaviour of the BCCD on inductive loads have been employed. To reduce the computational requirements, some simplifications in the simulations have been necessary, such as reduced computational precision and simplified boundary conditions for numerical integration. To ensure the predictive quality of the simplified simulation, its results have been compared with real measurements on the integrated MAIUS-1 payload.

Hereby, the emphasis was placed on the overlap of measurement and prediction in the regime of switching behavior, since this is the evaluational benchmark of PID settings for the respective loads. While the switching on ohmic loads is relatively trivial to predict, the complex nonlinear waveforms of the inductive loads in connections with the BCCD are of particular interest in the task of achieving optimal current control. As before, the most complex case of the Y-coils has been chosen for the comparison. The showcase measurements, performed on real parts of the integrated MAIUS-1 payload, have been found to be in very good agreement with the simulations (figure 6.5).

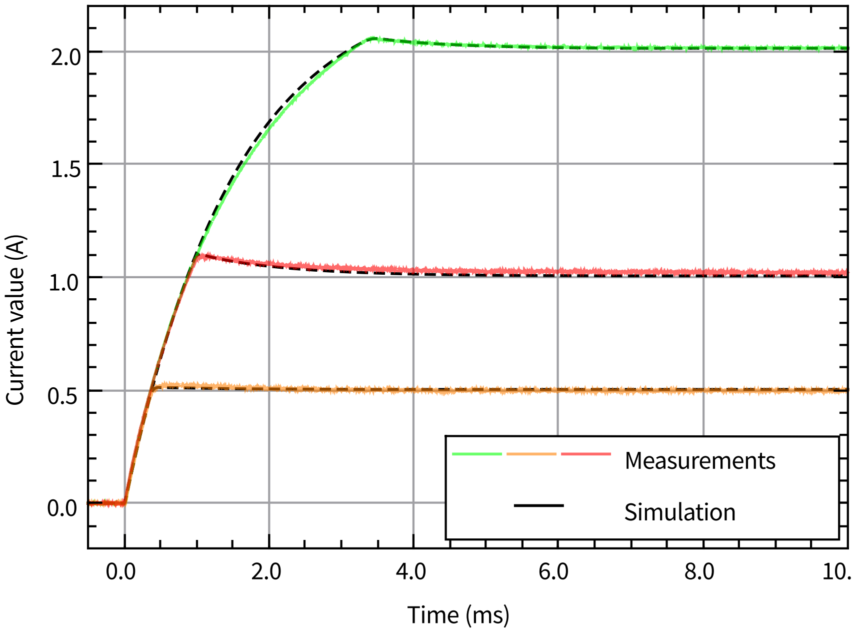

FIGURE 6.5.: Comparision of current simulations with measurements on the integrated MAIUS-1 Y-coils. The dotted curves show an almost perfect correlation for both amplitude and switching waveform. (Note: The lengthy switching times results from the unintentional use of a defective test battery with only two functional cells instead of the usual three.)

Based on these findings, the optimization of current switching can be simulated for the most part prior to implementing them in the flight hardware of MAIUS-1. As the de-integration of the current drivers and change of parameters takes almost a full work day, the simulations proved to be crucial in achieving a working configuration without weeks of experimental PID optimization, especially in the short time frame available for system integration. In fact, it was possible to achieve optimized control parameters for all 10 current drivers of the MAIUS-1-mission within only two iterations of PID settings.

6.2. Current Noise

The focus in this section will be put on the techniques to quantify current noise and to analyze the data obtained by the measurements. Afterwards, the tested current sources are characterized in the context of comparability to commercially available products. The term *noise*, in this context, shall describe variations in the output current in the frequency range larger than 1 Hz. For variations in the Sub-Hz regime, referred to as *drift*, as they are almost exclusively temperature related and not periodical, subsection 6.3.2 shall deliver a separate investigation with a different measurement scheme.

6.2.1. Measurement setup

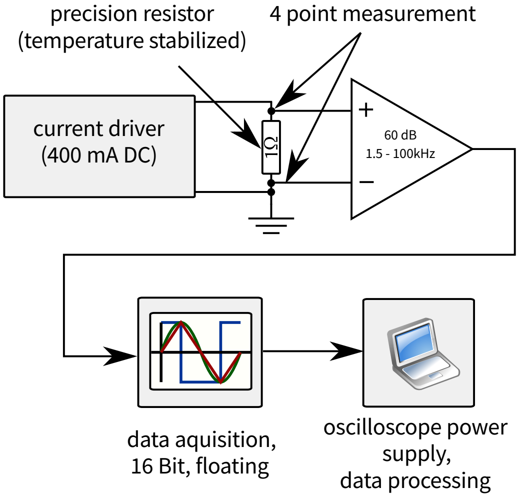

FIGURE 6.6.: Current noise measurement setup (schematic.)

While the measurement of current noise of µA amplitude and below is widely employed for laser power supplies, providing currents in the mA scale, the noise characterization of low noise sources for tens of amperes is more demanding, especially if one aims at a noise level in the µA-range. To achieve accurate estimates of magnetic field fluctuations at performance specifications, one has to measure high DC offset current with ~ part-per-million (ppm) resolution in the AC range. This is achievable with high pass filtered and amplified spectrum analyzers, but not in the low frequency range of 1 Hz up to a few kHz, which in our case contains the most important parts of the noise spectrum for magnetic atom traps. To cover the low frequency noise as well, we employed a discrete FOURIER-transform (DFT), where a time-based sampled signal is decomposed into it's frequency components.

In the measurement setup employed (figure 6.6), the current noise is observed via the voltage drop on a 1 Ω resistor[4], temperature stabilized with a massive heat-sink. The voltage signal is amplified with an ultra low-noise voltage amplifier[5] and AC-filtered with a cutoff of 1.5 Hz. The measurement is executed with the 60 dB gain stage of the amplifier, which has a input voltage noise of 2.4 nV/√Hz. The output was sampled with the 16-Bit resolution of a digital oscilloscope[6], with the coarsest scaling of ± 5 V.

With the input noise of the amplifier and the measured resistor value $\mathcal{R}$, the current measurement is to be expected to have a noise floor of

$$I_n = \frac{U_n}{\mathcal{R}} = \frac{2.4\,\mathrm{nV}/\sqrt{\mathrm{Hz}}}{0.994\,\mathrm{V/A}} = 2.4144\,\mathrm{nA}/\sqrt{\mathrm{Hz}}\,. \tag{6.1}$$

For the spectral analysis, 20 subsequent measurement runs are each weighted with a BLACKMAN-HARRIS function, FOURIER-transformed and averaged. Assuming usual white noise contribution of the pre-amplifier, the sensitivity of the measurement can be increased, by averaging successive time series. Thus, for $n = 20$ averaged measurements, with gain factor $G = 1000$ in the amplifier, while taking into account the resolution of the oscilloscope and rescaling by $\sqrt{2}$ to RMS, we yield the minimum bit resolution of

$$\Delta I_{\mathrm{LSB}} = \frac{2 \cdot 5\,\mathrm{V}}{2^{16} \cdot \mathcal{R} \cdot \sqrt{2} \cdot \sqrt{n} \cdot G} = 24.13\,\mathrm{nA}_{\mathrm{RMS}}\,. \tag{6.2}$$

In order not to cause significant temperature effects in load and current drivers, a current value of 400 mA is chosen for the benchmarks. Details on the data processing method can be found in section A.3 of appendix A.

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[4] [Isabellenhuette WID.RTO 50W 1R0]

[5] [FEMTO DLPNV-100-B-S]

[6] [PICOSCOPE 5000 series]

For the comparative measurement, the analog current driver prototypes[7] have been operated on batteries and obtained their input control voltage over a battery-driven voltage divider in order to ensure no negative influence of signal generators. The digital MAIUS hardware[8] has been powered by a 24V to TBUS external power conversion module. In every measurement, the control stack consists of a power supply, an ethernet control module and the device under testing. The ethernet control module is connected to a laptop operating on batteries.

6.2.2. General remarks on the spectra

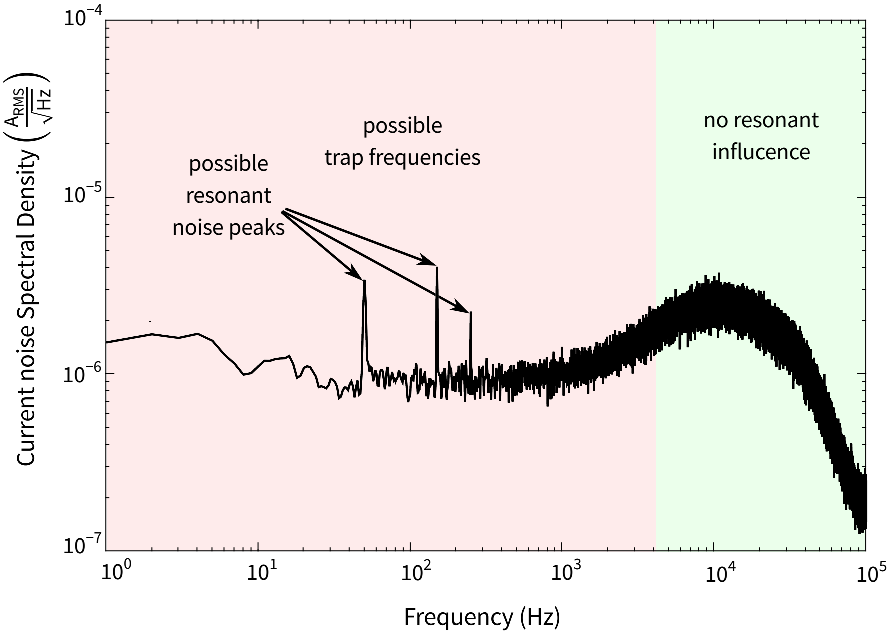

FIGURE 6.7.: A typical noise spectral density. The area in red is of special interest, since exaggerated noise peaks can directly interact with atoms trapped in potentials with similar trap frequencies (section 3.3). The area in green is of lesser interest, since at these frequencies, there are no direct interaction mechanisms with the trapped ensemble.

Before starting detailed spectral analysis, we shall recall the relevant features we derived in section 3.3 which are important in presentation of the obtained data.

Figure 6.7 shows a spectrum of the current noise obtained from the `[BCSP-10]`, which represent a benchmark in terms of noise for the developed circuitry as they have proven to be working satisfactory in the drop tower experiments, achieving trap lifetimes of roughly 3 seconds, over a typical BEC preparation [22].

The spectrum is depicted in a double logarithmic scaling, in order to deliver a good resolution of the lower frequency components, as well as to show all peaks in the spectrum, regardless of their amplitude.

Limited by the bandwidth of the preamplifier, the maximum accessible frequency span is 100 kHz, with a DC cutoff at 1.5 Hz. The most crucial part of the depicted spectrum are the first 3.5 decades, since usual trap frequencies occur in this range and would likely lead to parametric heating[9] of the trapped atomic ensemble. The noise peaks above 4500 Hz, located

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[7] `[HighFinesse BCSP-10]` and MLCD

[8] BCCD and UCCD

[9] Ref:section 3.3

in the green region and beyond could lead to non-resonant heating effects due to magnetic field fluctuations but are generally suppressed in MAIUS-1 either by the self-inductance of the coils or with RF chokes for the atom chip structures. The additional suppression factor for the frequencies above 100 kHz, which are theoretically important for spin-flip losses[10] is expected to be of the order of -20 dB per decade, so that a negative influence of the possible measured peaks would be unlikely.

6.2.3. Optimization of current driver noise performance

With the presented setup, the designed circuits have been characterized by reviewing several current noise spectra of different PID controller settings, as well as laboratory power supplies and batteries, ensuring optimal performance for each circuit for a comparison. As a result of this analysis, we will discuss two typical operation pitfalls, which can cause excessive noise in the experiment, but are easily avoided, as they are usually caused by the user.

Influence of the feedback loop of current control

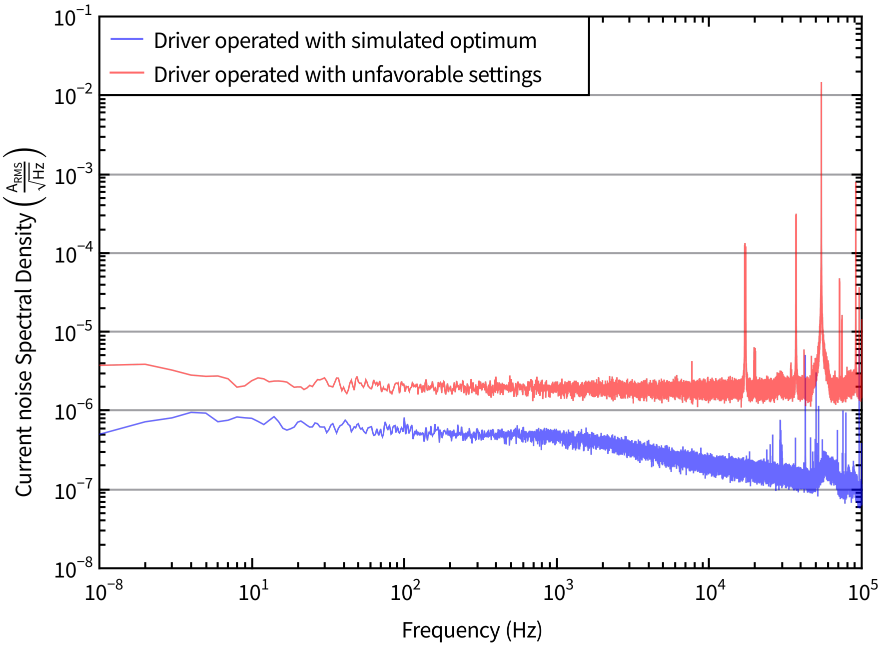

FIGURE 6.8.: Influence of PID settings on the current output noise. The BCCD in this setup has been operated on an ohmic load with factory settings for inductive coils (red) and simulated, optimized settings (blue). The unoptimized case shows deviations of up to three orders of magnitude. After optimization of simulated PID settings, the blue curve is obtained.

When tuning the PID settings of the current control, the user can influence the noise levels negatively to a high extent. Especially in connection with high inductances, the parameters of the current regulation play an important role, and even minimal resonances or slight overdrive can create significant heating which might be hard to come by, especially if the amplitude of oscillation is just below the detection threshold of standard current meters, which might be as coarse as some mA.

Hence, the circuit simulation of section 5.5 is an important tool to estimate the resonances of a certain inductive load and adapt the PID settings accordingly to suppress oscillation. Figure 6.8

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[10] Ref: section 3.3.5

gives an example of the difference between good and bad settings. For this measurement, the same coil current driver was characterized at an ohmic load, firstly with the rather aggressive settings for the X-coils. Afterwards, the PID was adapted to the ohmic load according to the simulation.

One can easily note a strong resonance of the PID controller for the first case, as well as an exaggeration of almost three orders of magnitude in the low frequency noise compared to the optimal settings. These oscillations, although clearly visible in the noise spectra, are very hard to observe with standard current switching waveform measurements in the lab. With these settings, trapping of atoms is possible, but would convey atom loss and heating due to periodic change of trap parameters. Therefore the introduced noise measurement should become the standard tool to investigate possible oscillations in current drivers.

During optimization, it has been found that controller settings determined for the optimum step response as in section 5.5 also minimize noise in the output path. Thus, achieving optimal noise and switching performance is usually possible with optimized control parameters.

Supply of the high power path

The MAIUS-1 experiment is designed to provide currents for the chip and coil drivers from LiFePO$_3$-cells, which are a very good approximation of an ideal current source. However, during laboratory testing, it often is more convenient to employ laboratory current supplies, as they are not prone to maintenance as batteries, which need to be charged and balanced. When doing so, caution is advised for several reasons.

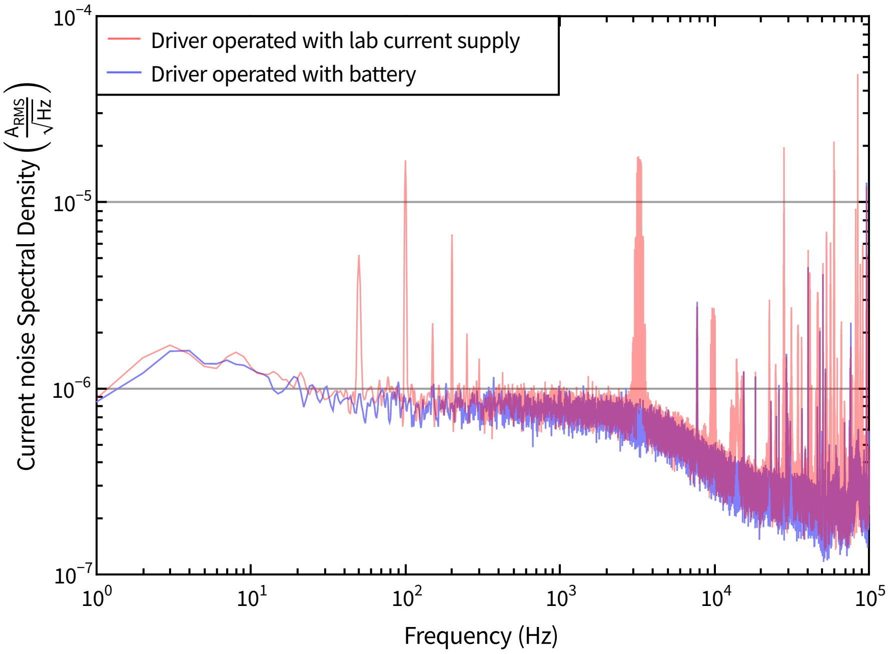

FIGURE 6.9.: Comparison of noise levels of a UCCD, powered with a lab current supply and a battery. The negative influence of the external current supply is clearly visible over the whole spectrum, especially as the 50 Hz peaks and its harmonics are not suppressed and potentially disturbing for magnetic chip traps. The switching regulation introduces additional noise into the higher frequency range around 3 kHz and beyond, giving rise for possible heating with the second harmonic of the trap frequency during evaporation.

Firstly, the regulation of current drivers and the current supply can influence each other and eventually lead to parasitic resonance. Most power supplies have a nonlinear response for high current gradients due to the regulation. This usually results in unfavorable change in the switching waveform of the current driver. Additionally, most lab power supplies are switch-regulated, which usually leaves significant ripple in the critical frequency rage of ≤ 1 kHz, which can inhibit the successful BEC-creation. Figure 6.9 shows a comparative measurement with the same UCCD, powered by battery (blue) and a regulated lab current supply[11] (red).

It is easily notable, that batteries offer a much better noise level than the regulated power source. However, this measurement is hardly sufficient to generally disadvise the use of power sources. Nevertheless, they pose another complication of current source operation which can be easily omitted by the use of batteries. In the context of the autonomous QUANTUS projects, batteries are used exclusively, as usual performance with lab power source operation shows significant impairment of the atomic source.

6.2.4. Comparison of current noise levels

In figure 6.10, the noise spectra of the three developed designs are compared[12] with the performance of the `[BCSP-10]` lab current driver. The drivers have been operated on the same type of batteries as are employed in the MAIUS-1 electronics module, and have been optimized for the load of our measurement setup according to the simulation software introduced in section 5.5. In the case of the `[BCSP-10]`, which does not allow for fine-tuning of control parameters, the factory setting for atom chip operation are used.

At a first glance, one can note that all current drivers show comparable noise results in the area of 1-10 kHz. As discussed in section 4.2.6, a properly designed driver in this frequency span is limited by the resolution of its internal current measurement. The two uppermost circuits share a class-AB amplifier stage in the design and seem to be receptible towards environmental noise like the omnipresent 50 Hz from standard laboratory net support and its harmonics. The slight increase of noise in the BJT-based `[BCSP-10]` model suggests an advantage towards the usage of MOSFET in the MLCD, which otherwise uses almost the same amplifier architecture.

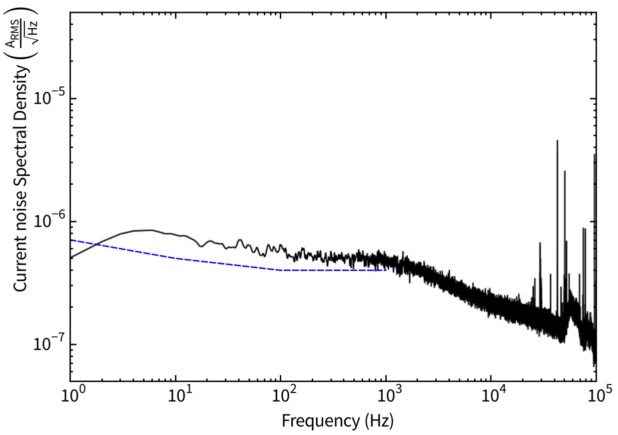

FIGURE 6.11.: The measurement noise spectrum of the BCCD is compared with the theoretical noise spectral density of the internal current measurement amplifier. In the first three frequency decades, the performance is close to the optimum. Afterwards, the bandwidth of the controller is exceeded, thus other noise sources are dominating. (ref: section 6.2.5)

Additional to this advantage on the component level, the MAIUS-1 current drivers benefit from their compact and optimized amplifier stage layout, surpassing the all-purpose BCSP-10 performance in the frequency band up to 1 kHz by a factor from 2 to 10. It is also notable, that the BCCD profits from the slightly reduced input noise in the internal current measurement amplifier for the feedback loop, therefore its performance in the first 1000 Hz span is the better than all the other drivers.

This measured performance is close to the ideal noise floor of the current measurement on the shunt resistor of the circuit (figure 6.11). The blue line in the measure-

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[11] `[Graupner PSU-5]`

[12] Detailed, high-resolution spectra for further reference have been documented in appendix B.1.

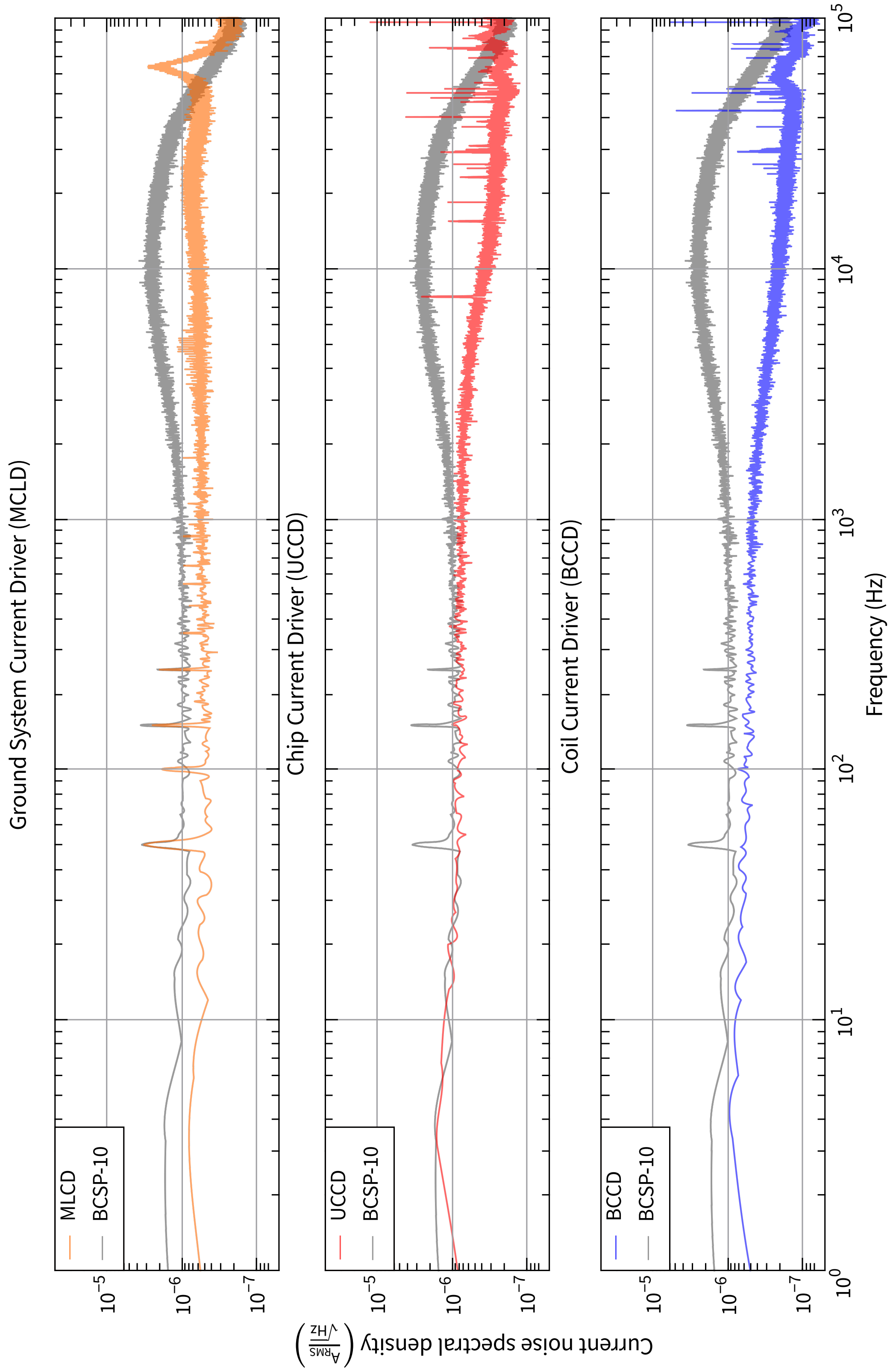

FIGURE 6.10.: Comparison of the current drivers employed in the QUANTUS-projects. In the most relevant frequency span of 1 to 10 kHz, all current sources show comparable performance, with a slight advantage of the MAIUS current sources, as they do not show frequency peaks in the area of possible trap frequencies. Above 10 kHz, all MOSFET-based circuits surpass the benchmark spectrum, but feature distinct noise peaks, which leave the need for further detailed evaluation.

ment's noise spectrum can be easily obtained by using the input voltage noise levels of the corresponding amplifier[13], scaled with the shunt resistor value.

Despite this exellent performance, the compactified MAIUS-1 drivers feature highly damped, but still notable distinct noise peaks from 9-100 kHz. Although very unlikely to cause significant influence on atoms (their amplitude is mostly below the benchmark noise level), their origin will be identified in section 6.2.5, to enable further improvements in the subsequent iterations of designs.

To obtain one single value to compare the performance, it is possible to integrate the power spectral density (PSD)[14] of the current noise over the interesting span and rescale it to μA. The results of these calculations are compared in Table 6.1 for different spectral bands, showing the superiority of the developed circuits in every chosen band. With the absence of resonant noise peaks in the area of possible trap frequencies and superior integrated noise levels in the higher frequencies, the advantage of the new circuits is clearly visible, up to a sixfold improvement between the BCSP-10 and the BCCD over the whole measured spectrum.

Circuit **Freq. Span**	**HighFinesse BCSP-10**	**Ground System Current Driver (MLCD)**	**Chip Current Driver (UCCD)**	**Coil Current Driver (BCCD)**
1 – 99840 Hz	408.788 μA$_{\text{RMS}}$	249.194 μA$_{\text{RMS}}$	107.725 μA$_{\text{RMS}}$	64.4623 μA$_{\text{RMS}}$
1 – 10000 Hz	200.659 μA$_{\text{RMS}}$	64.4252 μA$_{\text{RMS}}$	61.5139 μA$_{\text{RMS}}$	32.9025 μA$_{\text{RMS}}$
1 – 1000 Hz	32.2682 μA$_{\text{RMS}}$	20.1991 μA$_{\text{RMS}}$	25.4349 μA$_{\text{RMS}}$	16.3105 μA$_{\text{RMS}}$
1 – 100 Hz	11.1668 μA$_{\text{RMS}}$	8.1768 μA$_{\text{RMS}}$	9.4720 μA$_{\text{RMS}}$	6.3223 μA$_{\text{RMS}}$

TABLE 6.1.: Overall current noise levels in different frequency ranges.

However, despite the excellent performance of the MAIUS circuits, one should consider possible noise contributions of the DC/DC modules employed. It has to be ensured, that switching frequencies of the employed DC/DC converters are kept well above trap frequencies and below trap bottom energies, or otherwise be filtered rigorously. For MAIUS-1, one can expect noise peaks in the frequency vicinity of ~ 350kHz, which is the switching frequency of the converters. Nevertheless, it is possible to suppress the ripple noise delivered by the switching regulation by filters, so that during the MAIUS-1 mission, no negative influence was registered.

6.2.5. Frequency decomposition of current noise

In order to understand the origin of noise peaks at specific frequencies in the novel amplifier architectures, detailed circuit analysis has been combined with comparative measurements for several components. The differences between spectra allow the identification of distinguished peaks in figure 6.12, that shall be summarized in this section.

For the analysis, only peaks with current noise spectral densities greater $2\,\mu\mathrm{A}_{\mathrm{rms}}/\sqrt{\mathrm{Hz}}$ are taken into consideration. Below this value, the distinction of circuit introduced noise from the environmental noise of the measurement setup is no longer reasonable.

When comparing the two MAIUS flight hardware models, UCCD and BCCD, one notices some peaks which are common for both architectures and can be identified as introduced by certain components of the circuitry. The other peaks, which each occur in one spectrum are most likely

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[13] BCCD: `[TI INA 128]`, all other drivers: `[TI OPA 2277 UA]`

[14] ref: section A.3

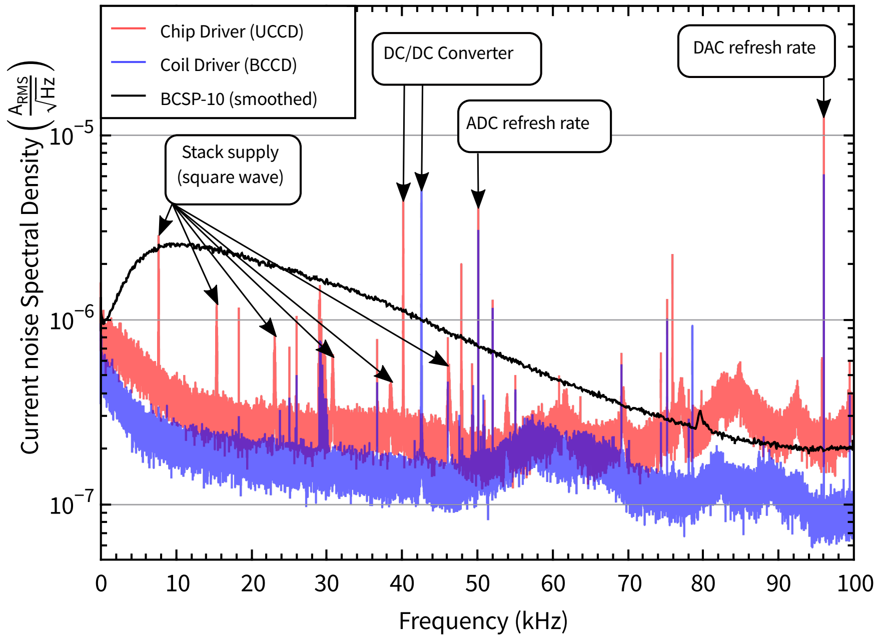

FIGURE 6.12.: Decomposition of MAIUS current driver high frequency current noise. Below 2 µA/$\sqrt{\text{Hz}}$, external noise and circuit noise become hard to distinguish. Major noise sources within the high frequency spectrum are generated by the parts of the current driver itself. However, their influence seems exaggerated due to the high measurement resolution, as their width of few Hz only minimally contributes to the overall noise Integral.

to be attributed to the DAC, as it's datasheet states an overall noise value of 80 μV_{rms} in the 0-100 kHz band, which should be translated directly into current noise within the bandwidth of the regulation, but is apparently damped well enough to not completely impact on the current noise spectrum.

The first notable noise contribution is a consumption-dependent square wave[15], associated with the TBUS power supply module. These noise peaks only occur on the UCCD, but are absent when the circuit is powered by batteries, instead of the power module. However, compared to the benchmark spectrum of the HighFinesse current drivers, the amplitude of these peaks is almost completely masked by the noise floor of the BCSP-10, so that a negative influence on the atomic trap is not very probable. Nevertheless, the width of the peak and it's higher harmonics contribute significantly to the overall noise budget, therefore it is advised to use a battery stack supply for UCCD, as it has been done in MAIUS-1.

frequency (kHz)	contribution	circuits
7.7 + harm.	TBUS supply	UCCD
40.7	DC/DC conv.	UCCD
42.6	DC/DC conv.	BCCD
50	ADC	UCCD, BCCD
96	DAC	UCCD, BCCD

TABLE 6.2.: Significant noise contributions from components.

The next two significant peaks in the spectra differ slightly for the both circuits[16], as they are dependent on the power consumption at the input of the DC/DC converters. Although their influence is expected to be negligible as well, they could be suppressed by additional filter circuits or by replacement of the converters with different models, switching at more suitable frequencies.

The following peak is common for both circuits and is determined by the firmware and the internal clock of the TBUS. For diagnostic purposes, the ADC samples the current measurement

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[15] fundamental at 7.7 kHz, with 8 harmonics

[16] Chip: 40650 Hz, Coil: 42575 Hz

signal with 50 kHz, due to firmware settings. As a result of interference with the controller electronics, the minimal current surge during sampling causes current noise over a slight disturbance in the feedback loop of the controller. This can be suppressed by inhibiting the current monitoring or introducing a separate diagnostic measurement. In any case, it should not be relevant for heating, as the amplitude of the peak is very low and narrow, and the frequency is well above the sensitive part of the spectrum.

Finally, the most dominant contribution to the noise peaks is determined by the firmware as well. It employs a refresh cycle of ~ 10.4 µs for the DAC setpoint output, which corresponds to 96 kHz. At the far end of the visible frequency spectrum, even this contribution can be considered harmless in terms of heating. However, with more aggressive low pass filtering of the input voltage, the amplitude of the peak can be reduced.

These noise contributions of discrete frequencies, with amplitudes well below 1 ppm of the maximum current output and a very narrow width of just a few Hz, is not found to disturb the experiment in any measurable way. If this somehow occurs in the future, this analysis should be a good starting point of countermeasures.

6.2.6. Estimation of chip loss rates based on the obtained noise spectra

In section 3.3.4, we calculated estimations for the loss rates of several malignant effects in atom-chip-based traps, for an experimental situation like in QUANTUS-2. With the measured noise spectra, we can now review these values, based on the available measurements of the chip current driver (UCCD). Assuming the proximity of the chip surface as the dominant source of disturbance, we analyzse the impact of the spectral noise of the UCCD. However, since the noise spectrum at the LARMOR-frequency of the experiment cannot be measured directly in our setup, we can only assume the power spectral density of 99.8 kHz to be valid at ω_L as well. For our consideration, we will also assume a noise suppression of the wire structures[17], as they are employed in MAIUS-1. For an estimation without any unduly optimism, we assume a damping factor of only 10^{-1}.

effect	equation	loss rate	scaling
Johnson-Nyquist noise (spin flips)	(3.21)	$1.5 \cdot 10^{-1}\,s^{-1}$	$\vartheta_{Chip}/\rho d^3$
Technical current noise (heating, trap displacement)	(3.25)	$1.1 \cdot 10^{-1}\,s^{-1}$	$\omega_T \cdot S_I(\omega_T)/d^2$
Technical current noise (spin-flips)	(3.23)	$3.9 \cdot 10^{-2}\,s^{-1}$	$S_I(\omega_L)/d^2$
Technical current noise (heating, curvature change)	(3.26)	$2.6 \cdot 10^{-7}\,s^{-1}$	$\omega_T^2 \cdot S_I(2\omega_T)/I^2$
Johnson-Nyquist noise (heating, trap displacement)	(3.27)	$1.7 \cdot 10^{-8}\,s^{-1}$	$\vartheta_{Chip}/\omega_T \rho d^3$

TABLE 6.3.: Estimation of loss and heating mechanisms with a UCCD driven chip structure. Scaling formulas from [81]

Again, we consider a trap of ^{87}Rb cloud in the final stages of evaporation ($|m_F = 2\rangle$), with $\omega_T = 2\pi \cdot 600\,\text{Hz}$, $d = 250\,\mu\text{m}$. The trap is consisting of a single wire-structure on a non-conducting substrate of $\vartheta = 300\,\text{K}$ with a current of $I = 2\,\text{A}$, and a bias field of $B_b = 20\,\text{G}$, with an offset field of $2\,\text{G} \longrightarrow \omega_L = 1.4\,\text{MHz}$. From our measurements, we can now determine $\sqrt{S_I(\omega_T)} = 7.4 \cdot 10^{-7}\,\text{A}/\sqrt{\text{Hz}}$, $\sqrt{S_I(2\omega_T)} = 7.8 \cdot 10^{-7}\,\text{A}/\sqrt{\text{Hz}}$ and estimate $\sqrt{S_I(\omega_L)} = 2.5 \cdot 10^{-7}\,\text{A}/\sqrt{\text{Hz}} \cdot 10^{-1}$.

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[17] Ref.: figure 3.14

Reviewing table 6.3, we find the technical current noise not longer to be the dominant loss source. However, its contribution is on par with the thermal noise, introduced by the chip structures. Unfortunately, these findings could not be verified experimentally in the time frame for the MAIUS-1 mission. Detailed experimental studies of the significance and the impact of particle loss in several trap configurations thus remain a future task.

6.3. Current Stability

While the higher frequency noise in a current driver determines the disturbance-free operation of a single experiment in terms of losses and heating, the measurement reproducibility plays an equally important role for repeated measurements. Depending on the function of the current drivers, their drifts and inaccuracies can lead to trap deformation, particle number fluctuations and center of mass scatter. This section will focus on the characterization of these instabilities and illustrate some of their impact on the integrated MAIUS payload.

6.3.1. Thermal conductance of power parts

One of the biggest negative influences on stability are temperature fluctuations, which we will investigate in the beginning. To obtain information about the temperature of each current driver, the measurement of the NTC sensor for the high power segment is used, as it is the only accessible temperature sensing unit during the operation of the driver. However, these sensors have the purpose to help protect the circuit from overheating, not for precision calibration measurements. Hence, it is necessary to evaluate the temperature distribution on the power boards during operation to verify the validity of the NTC value for further conclusions. For the MAIUS-1 prototypes, this has been done with infrared thermography. Here, the false color images of the operating circuitry give an impression on the heat distribution of the layout.

To obtain a good resolution of interesting areas of the circuits, the drivers have been disassembled on a workbench and connected via cables, instead of direct plug in of the power module. As the significant areas of heating and the reference resistor are situated on the aluminum boards alone, only pictures of this area are included in this analysis.

Unipolar Chip Current Driver (UCCD)

In the UCCD, the hot spot for each driving stage is situated at the power transistor. The design of the pad area enables heat transport to the heat sink (right hand side of the picture), hence an efficient cooling mechanism. The sense resistors are slightly heated by the excess heat. However, there is a temperature gradient between NTC (crosshair) and sense resistor due to the distance between the two. Hence, the correllation between temperature measurement and actual thermal drift might be distorted. However, for it's original purpose of overheat protection, the placement of the NTC is ideal, as the sensor delivers a relatively well temperature estimate of the transistor.

Bipolar Coil Current Driver (BCCD)

The thermography of the BCCD came up with a rather unexpected result. In the layout of the aluminum board, assuming satisfactory heat transport throughout the substrate, the placement of the MOSFET has been put in a convenient way for routing. As only one MOSFET of a type is

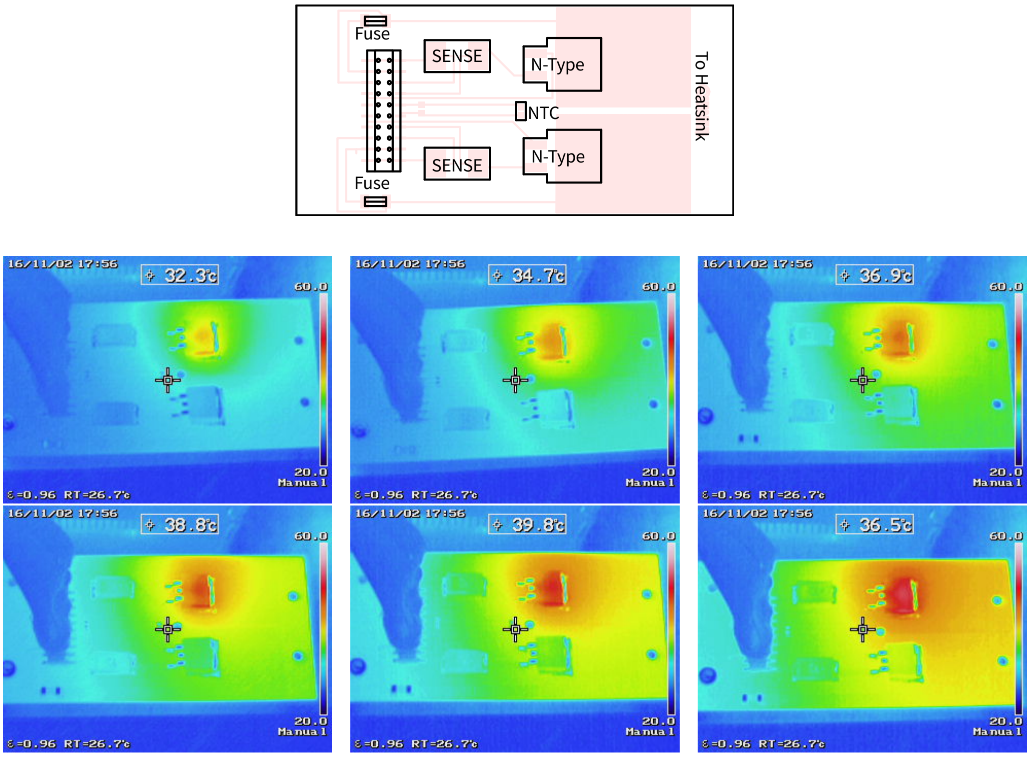

FIGURE 6.13.: Thermography of the UCCD. To simplify identification in the photos, the upper schematic shows the placement of the power parts of the two amplifier stages. The photos below show a time series (10 s between pictures) of a driver that is turned on, delivering 1 A of current into a short circuit. Only the upper driver stage is used.

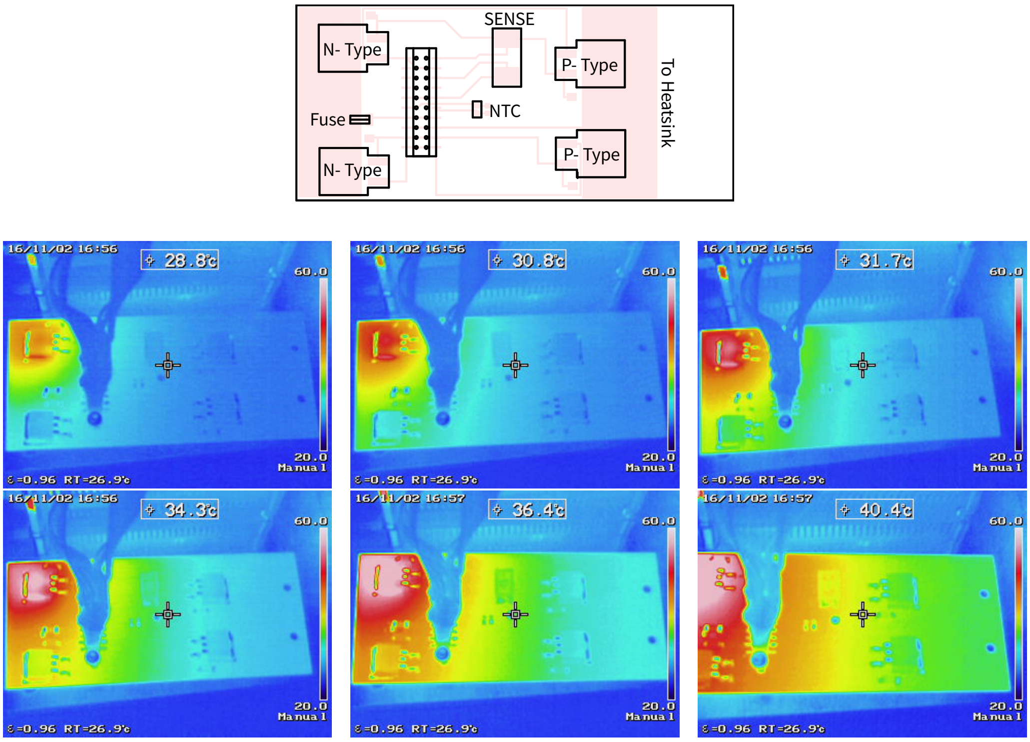

FIGURE 6.14.: Thermography of the BCCD. The amplifier stage consist of four MOSFET, with only one of each type active, depending on the current flow direction. The time series of the board is done with the same configuration as above, revealing a much higher heat concentration at the N-Type MOSFET. The heat transport is sufficient to keep the IC intact. The placement of the NTC delivers a good measurement of the sense resistor temperature.

operating simultaneously, the size of the copper ground plane was considered to be sufficient to ensure heat transport. While this is true in terms of preventing a temperature breakdown of the circuit, the gradients throughout the board have been underestimated. During operation, a strong temperature rise in the N-Type MOSFET is notable, whereas the P-Type MOSFET are basically not experiencing any excess heat, effectively just rinsing in temperature with the aluminum substrate. From the images, the following conclusions rise:

- The temperature measurement of the hot spot of the board is inaccurate during heating, as the sensor is too far away from the actual heat source. Thus, the placement of the NTC is not optimal for safety purposes.
- In the significant range for the temperature safety, the gradient becomes smaller, therefore ensuring still a reliably working safety fuse.
- The heat transport is not optimal, as placement pads and heat sink connection for the N-Type transistors is not optimized for the actual amounts of excess heat .
- Fortunately, NTC and current sense resistor are very close to each other, therefore the temperature data of the coil driver layout can be used to estimate resistance drifts due to temperature.

6.3.2. Temperature coefficient

The MAIUS-current drivers are equipped with analog feedback electronics, which are subject to drift in their output and input offsets, for example due to temperature changes of the environment or caused by the heat due to the power density in the current output amplifier stages. The MAIUS-1 drivers operate in a highly integrated system with vast temperature variations of up to 30 °C during the mission, which cannot be compensated by external control elements. For these drastic temperature changes, the MAIUS-1 current drivers exhibit output drifts, as their passive reference and active semiconductor parts in the change their performance values over temperature, eventually offsetting the feedback value of the control loop.

To ascertain these instabilities, each driver was employed to deliver 0.5 A of current, with changes in the voltage of the supply in order to introduce different values of excess heat on the power transistors[18]. To determine a temperature value of the current drivers, which can be obtained without external measurement devices, thus possibly employed for diagnostics during operation, the internal NTC measurement was used, delivering coarse values. Simultaneously, a high precision multimeter[19] monitored the current output with up to 1 µA resolution. The data was then correlated and characterized by a fit model for temperature drift.

Unipolar Chip Current Driver (UCCD)

Figure 6.15 shows an unexpected nonlinear behavior of the current drift. In the area of our measurement, the internal shunt resistor of the circuit should increase its resistance with rising temperature thus cause a higher feedback value, resulting in a negative drift of the output current. Although this is the case, one can notice a dependence of the drift amplitude from the excess heat power which is applied to the transistors.

With the specification of the reference resistor, one would expect a temperature drift of ± 75 ppm/K, which should theoretically be the limit of the current measurement precision,

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[18] Ref: section 4.2

[19] `[Agilent 64461A]`

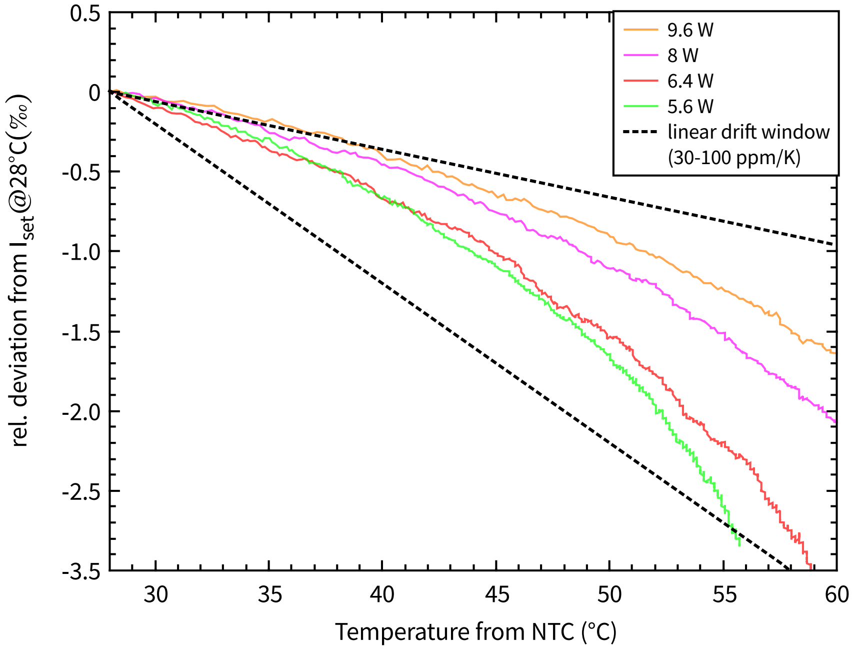

FIGURE 6.15.: Temperature drift coefficient(s) of the UCCD. A correlation of heating powers and temperature drift is clearly recognizable, hence an all-purpose fit is not feasible. However, the temperature drift can be estimated in a window from 30-100 ppm/K. If the temperature can be stabilized below 50 °C, the drift is almost linear with a slope of maximal 60 ppm/K.

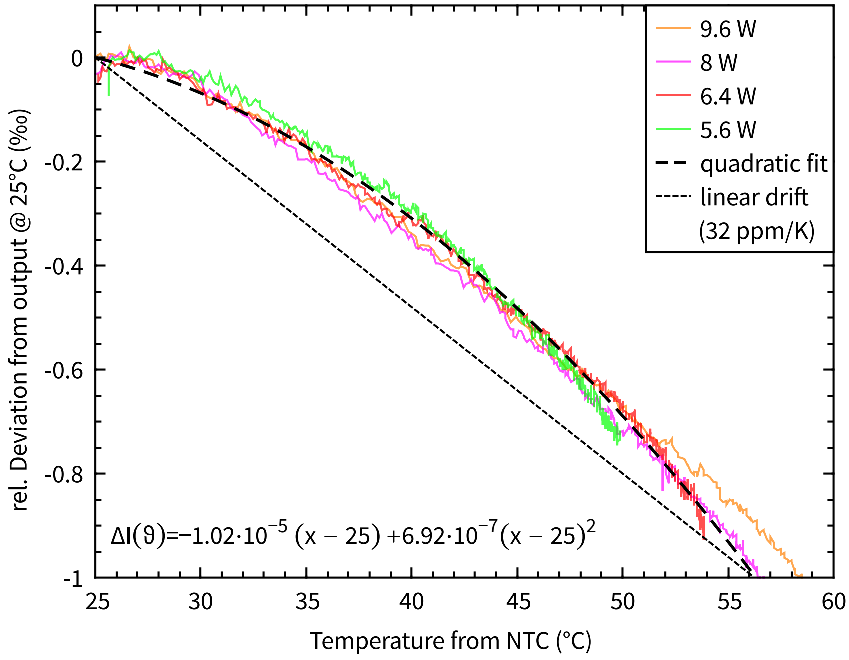

FIGURE 6.16.: Temperature drift coefficient of the BCCD. The temperature drift of the circuit is comparable for different heating powers, therefore it is possible to fit it with a quadratic function. For a linear drift model, a an approximation of 32 ppm/K is obtained.

independent of the heating power. However, if we consider the thermographical analysis of the NTC placement[20], the deviation of the measurement becomes clearer. The distance between the thermal sensor and the shunt resistor is large enough to enable for power-dependent temperature difference from the measurement point and the region of interest. Thus, for higher heating powers, the measured temperature at the NTC rises faster as at the shunt resistor, which leads to a measurement corruption and an underestimation of the temperature drift slope.

Unfortunately, with the given impairment of the temperature measurement, the drift data of the UCCD does not allow an exact calculation curve for the output correction. However, within the limits of 30-100 ppm/K output stability, one can estimate the expected maximum temperature drift during the MAIUS-1 mission. Within this estimated drift window, the UCCD drift is slightly higher than of laboratory devices[21], but still at a competitive level for lower temperatures lesser than 50 °C. For the expected conditions in MAIUS-1, we can assume drifts closer to the 5.6 W heating curve, as the drivers on most chip structures experience relatively low excess heat powers[22], and we can assume a neglible temperature gradient between NTC and shunt resistor. As the electronic module will provide a heat sink connected to the power boards, unlike as in our mesurements, temperatures above 50 ℃ are not to be expected during the rocket flight[23].

Bipolar Coil Current Driver (BCCD)

The temperature drift of the BCCD, as depicted in figure 6.16, shows a different behavior as for the UCCD. Independent from the heating rate, the temperature drift can be approximated by a excellent linear drift of 32 ppm/K, which is much smaller than expected by the shunt resistor's specifications. Moreover, it is almost perfectly fitted by a quadratic polynomial, which makes the drift easily predictable.

The explanation of this result includes the role of the current measurement amplifier in the feedback loop[24]. As this amplifier experiences temperature changes as well, its input offset drifts, which, in the case of the BCCD, is compensating the much higher drift of the shunt resistor.

FIGURE 6.17.: Thermography of sympathetic heating in the BCCD. The excess heat of the transistor heats the current measurement amplifier below, thereby causing a additional drift in the current output.

This effect has an especially large impact, in the dense packaging layout of the BCCD, with the power board stacked ontop of the logic controller board. As observed with thermal imaging (figure 6.17), the energy of the power transistors is not only depleted onto the aluminum substrate, but also dissipates through the surrounding air, thereby additionally heating the underlying operational amplifier in the vicinity .

With the fitted function for the temperature drift of the BCCD, its thermal stability can be improved in future firmware versions, in form of a feed-forward correction of the controller setpoint. However, for the actual hardware, the stepsize of this setpoint amounts to a drift of more than 10 ° C, thus an

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[20] ref.: section 6.3.1

[21] `BCSP-10: 25 ppm/K [94]`

[22] ref.:table 4.1

[23] In fact, during subsequent 200 measurements within the integrated payload on ground (section 6.4), the maximum temperature of 51 ℃, observed on the Base-Z chip driver, has not been exceeded.

[24] ref.: figure 4.10

implementation in the current development stage would provide very little benefit. However, with improved setpoint precision, e.g. with additional scaling of a second DAC channel, a feed-forward stabilization of the current output could significantly improve the thermal stability of the BCCD.

6.3.3. Output stability in thermal equilibrium

After identification of temperature drift as the dominant limitation in stability, the two MAIUS current drivers have been characterized under stable temperature conditions in order to determine the long-term stability in a stationary experimental mode. Maintaining the original measurement setup from section 6.3.2 with the precision multimeter, a time series was obtained with night-time measurements of 30000 s with 2 Hz samplerate. To allow for continous measurement, both circuits have been supplied by a stabilized laboratory current supply instead of batteries. For the analysis, data points during the initial heating processes have been disregarded and only values with stable temperature conditions[25] have been used. The stability is characterized with an ALLAN-Deviation plot[26] as well as with the total mapping of the normalized time series of current measurement.

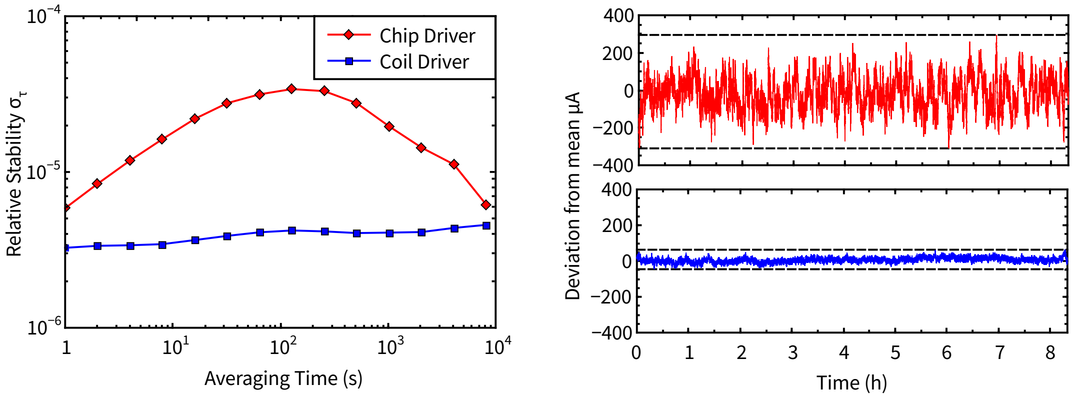

FIGURE 6.18.: Stability measurements in thermal equillibrium. Left: ALLAN-Deviation plots of the relative stability. Right: Corresponding plots of the time series with indicated absolute maximum and minimum deviation of mean. Both measurements have been taken at 500 mA current output level.

In the ALLAN-Deviation plot, both circuits start with an already excellent short time stability of $\sigma < 10^{-5}$ at 1 s. However, their noise picture deviates due to their architecture. The UCCD features a random-walk type noise contribution up to 100 s of averaging. This can be explained by the flicker-type noise of the semiconductor diodes in the integrator part of its regulation. Flicker noise is usually the predominant noise source in electronics. As the noise signal would be integrated in the regulation, this would result in a random walk ($\sim \sqrt{\tau}$).

This influence, however, is averaged out after longer integration, resulting in a falling slope proportional to white noise. The stability performance of the UCCD is still satisfactory, with a roughly 35 ppm maximum drift over the whole anticipated mission time of MAIUS-1 (~15 min).

The BCCD features an almost constant level of relative stability on a level that is expected to be close to the noise floor of the measurement device, suggesting a flicker type noise, as expected in an electronically stabilized circuit.

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[25] $\Delta\vartheta \leq 1\,\mathrm{K}$

[26] Details on the calculation can be found in section A.4

Compared with the specified value of $2.5{\cdot}10^{-5}$ relative stability in thermal stabilized conditions of the commercial `[BCSP-10]` [94], the UCCD performs comparably, even at the maximum of the ALLAN-curve, while the BCCD operates in the lower 10^{-6} regime, therefore outperforming the commercial device.

The superior performance of the BCCD is illustrated in the time series, which has the same scaling for comparison. The amplitude of absolute deviations in contrast to the UCCD is much smaller. The maximum deviation from mean of less than $\pm\, 3.1{\cdot}10^{-4}$ A (UCCD) and $\pm\, 6.3{\cdot}10^{-5}$ A (BCCD), respectively.

These values are of the order or below the value of bit errors occurring in a 16 Bit DAC[27], which deliver the highest analog precision available in all QUANTUS-projects. This means that given temperature stability, drifts of the analog circuitry does not influence the overall precision expected due to digitalization errors. It is also important to note that there is no significant rise in instability over long timescales, therefore it is appropriate to assume that long-term operation is possible within the measured parameters.

6.4. Performance of the current drivers in the MAIUS-1 BEC source

While the model of temperature influence has been determined and described in the section above, the time frame prior to the MAIUS-1 launch did not yet allow for the implementation of a temperature stabilization of the current drivers in this mission. However, with the logging of temperature data, it is possible to investigate the impact of temperature gradients in the integrated payload.

The following measurement has been performed in the completely integrated payload, prior to the final transfer for environmental testing and launch. As the whole system shows strong temperature drift in the first few shots, the experimental procedure includes a pre-heat phase before the shown measurement in order to suppress this effect during the experimental phase, and separating drifts of the optical components from the measurement. During this pre-heat, laser components and current drivers deliver current for several seconds in order to reach a relatively steady temperature. While this is sufficient for the laser system, which reaches an almost steady state power consumption, the current drivers show strong variations in their power consumption, depending on their experimental use. Furthermore, their power density is much higher than on the laser current drivers. As a result, the temperature during flight phase is expected to change significantly for each driver, depending on the sequences performed.

For a performance benchmark, a BEC was created and released from the trap, and detected with absorption detection after a short time-of-flight of 20 ms, without performing a DKC or ARP. This sequence has been repeated 200 times and the reproducibility has been evaluated.

For our analysis, important performance values of the BEC creation have been observed, such as the condensed and thermal particle number, as well as the center of mass position of the detected BEC. Simultaneously, the temperatures of the thermal sensors on the relevant current drivers[28] have been logged during the whole benchmark measurement, which was carried out in 20 min, which is roughly twice of the expected MAIUS-1 flight time (figure 6.19).

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[27] $\delta I = 3.05{\cdot}10^{-4}$

[28] For this analysis, mesoscopic structures will be neglected, as they are of no essential influence in the phases of the experiment that determine these values predominantly, like evaporation and trap transfers. Obviously, the mesoscopic H is important for the trap transfer, as it determines the quality of mode-matching. However, as we see in figure 6.19, the outcome of the BEC number, which is only a fraction of the initially transferred atoms, is relatively stable, thus a significant negative influcence of the mesoscopic H prior to evaporation can be excluded.

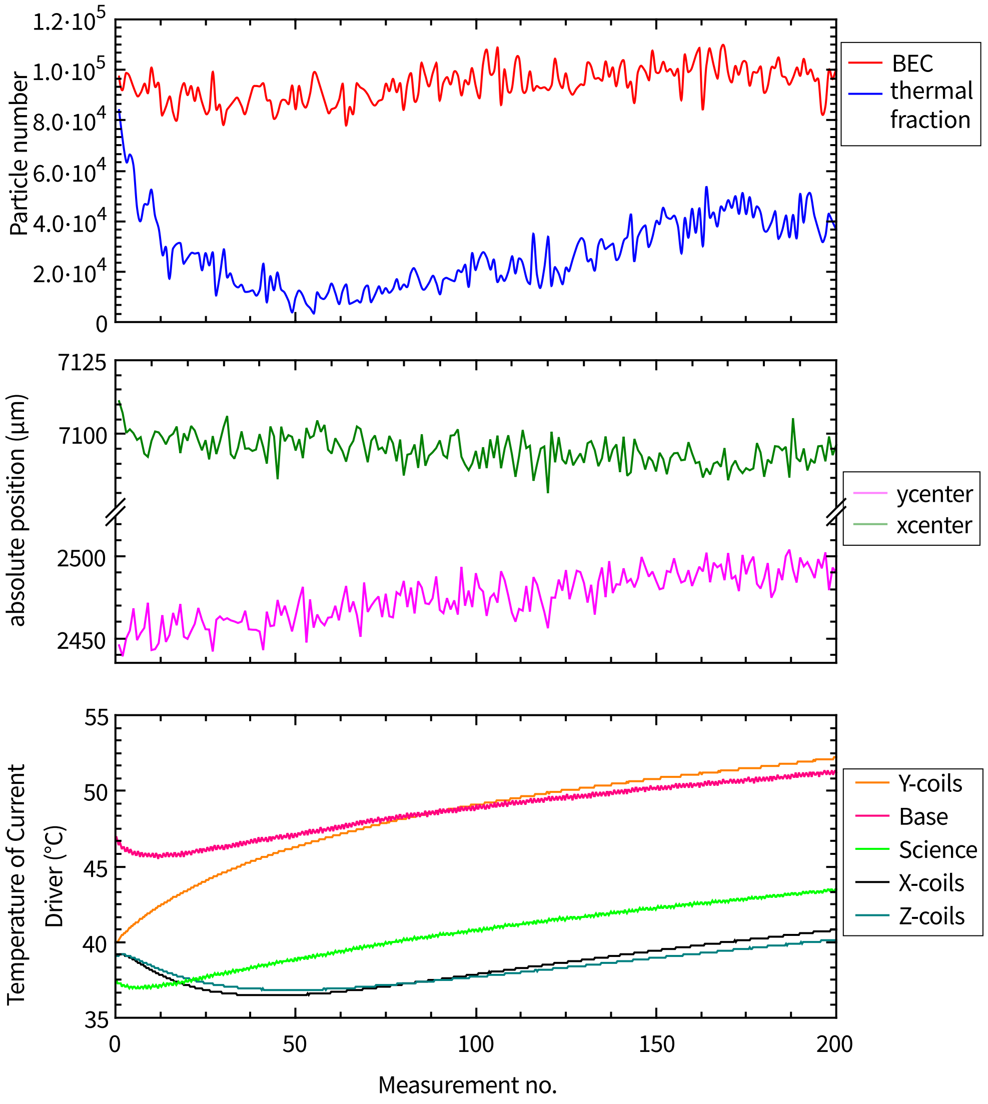

FIGURE 6.19.: Reproducibility of particle number and BEC fraction of the integrated MAIUS-payload. The graph above shows the particle numbers of condensate and thermal background, the middle graph the absolute position of the center of mass in the detection plane, and the lower graph the temperatures of the power boards in the current driver stack, assigned to their specific loads.

While the BEC particle number is relatively constant close to 10^5, the thermal fraction of the atomic ensemble exhibits a drift throughout the experiment, which shows similarities to the temperature drift of the x and z coils. Likewise, the x and y center position of the detected cloud experience a slight shift during the experimental time.

Regarding the temperatures of the current drivers, it is notable, that both employed UCCD (Base and Science Chip) have almost linear temperature increase with relatively moderate slope. The BCCD (all coils) on the other hand have nonlinear temperature curves as a result of the imperfect pre-flight heating. For the Y-coils, the pre-heating was too weak, hence the fast temperature increase, whereas the X- and Z-coils have been heated a too strongly, resulting in an unnecessary temperature decrease within the first 50 measurements.

6.4.1. A simple model of temperature influence

Following the graphs of the temperature and the particle number, a certain degree of correlations with thermal drifts seem likely. For the measurements, which have been obtained with a complex preparation sequence with contributions of several current drivers with their specific drifts, it is obviously not simply possible to derive a predictive model including the temperature drifts of all hardware. However, for the specific data values, we can show with a number of simplifications, that the measured temperature drifts show an impact on the performance stability of the MAIUS-1 BEC source.

① The current drivers do not influence each other within the stack (e.g. by temperature transfer of neighboring parts). Therefore their contribution can be treated decoupled.

② The impact of temperature in the benchmark measurement can be described by a first order linear combination of several contributions around the starting measurement.

③ The magnetic field generated by the Science Chip will is predominantely influenced by temperature drift, as it features the highest temperature gradient of the chip structures and the ratio between anticipated drift and overall current is probable to cause effects.

④ The magnetic field of the X-coils have the most critical influence on particle numbers, since they define the trap bottom. For a fixed digital evaporation frequency, this results in a variation in the evaporable energy levels.

⑤ The magnetic field of the Y-coils influence the trap position the most, as they are used for transport and confinement of the atomic ensemble throughout most of the experimental steps. With the high temperature difference, an impact on the overall particle number, e.g. through a slight shift of the trap minimum is also expectable.

⑥ The influence of temperature to the Base Chip magnetic field is negligible in first order. The relatively high currents throughout the whole sequence have only a small percentage of drift due to temperature, therefore will be assumed constant. Due to the very similar shape of drift curves, a seperate treatment of the structures is not useful.

⑦ The magnetic field drift of the Z-coils does not affect the measured quantities, as these coils are not employed during the evaporation and transfer.

According to the assumptions above, we can define a linear approximation of the change in key features $\mathcal{F}$ of the measurement. It consists of linear combinations of the Science Chip, the x and y coil temperature (T_i), scaled with factors (α, β, γ) and the initial starting value of the measurement $\mathcal{F}_0$:

$$\mathcal{F}[T_{SC}, T_X, T_Y] = \mathcal{F}_0\Big(1 + \alpha \cdot \left(T_{SC} - T_{SC_0}\right) + \beta \cdot \left(T_X - T_{X_0}\right) + \gamma \cdot \left(T_Y - T_{Y_0}\right)\Big) \tag{6.3}$$

Indeed, with this simple approach, a variation of the pre-factors (α, β, γ) yields curves for all analyzed experimental quantities, which fit the measured data points (figures 6.20 and 6.21). This gives an strong argument to assume corellation between temperature drift and performance of the BEC creation. The values of parameters are collected in table 6.4.

parameter **fitted quantity**	$\mathcal{F}_0$	**α (Science-Z)**	**β (X-coils)**	**γ (Y-coils)**
BEC particle number	93 750	$2.6\cdot10^{-2}$	$1.4\cdot10^{-2}$	$-8.5\cdot10^{-3}$
Thermal background	77 500	$9.0\cdot10^{-2}$	$1.4\cdot10^{-1}$	$-9.7\cdot10^{-2}$
Condensate fraction	56 %	$5\cdot10^{-2}$	$-1.6\cdot10^{-1}$	$1.4\cdot10^{-2}$
x-center pos.	7100 µm	$-2.1\cdot10^{-5}$	$2.8\cdot10^{-5}$	$-8.5\cdot10^{-5}$
y-center pos.	2445 µm	$7.2\cdot10^{-4}$	$1.0\cdot10^{-4}$	$1.2\cdot10^{-3}$

TABLE 6.4.: Fit Parameters for equation 6.3 of several quantities in the MAIUS stability measurement. The curves are valid in the regime of temperatures of the measurement. The offset temperatures are taken at the beginning of measurement. Re-scaling to laboratory conditions is probably not simply possible, as linear perturbation theory for these vast temperature difference would fail.

6.4.2. Particle number

In order to correlate the driver temperature with the BEC particle number, it is useful to look at the renormalized condensate fraction of condensed and total atom number:

$$\mathcal{F}_{\mathcal{N}} = \frac{N_{\mathrm{BEC}}}{N_{\mathrm{BEC}} + N_{\mathrm{THERM}}}. \tag{6.4}$$

Figure 6.20 depicts the benchmark measurements, along with the calculated condensate fraction. With the fit model and the values from table 6.4, the temperature changes of the three considered current drivers can be mapped onto the drifts observed in the particle number measurements. As was assumed in ④, the coefficent for the X-coils driver temperature is the largest contribution of the linear combinations, especially for the ratio of condensed and thermal particles. This accomodates the high sensitivity of the evaporation efficiency to changes of the trap bottom, which is defined by the offset-field generated by the X-coils.

6.4.3. Center of mass position

Apart from pure particle number, which is interesting to predict contrast of interferometry, the exact reproducibility of the condensate position after the creation is important in order to estimate a trajectory, internal modes and input state for the DKC.

Again, a fit model of the form of equation 6.3 can be employed to mimic the changes of the position of the released BEC (figure 6.21)

In contrast to the particle number measurements, here the drift of the Y-coils' bias field could be identified as the strongest influence, determining the trap minimum position to a high degree, thus influencing transport and release processes. As the detection axis is orientated in an 45°angle to the xy-axis plane of the bias coils, it is not possible to seperate the influence of the coils by the evaluation of the x and y position in the picture.

Remarks on the validity of the fit model

Unfortunately, in a complex system, simple models that show good correlation with the data are very rare and have to be treated with the necessary doubt. Since our model of equation 6.3 was

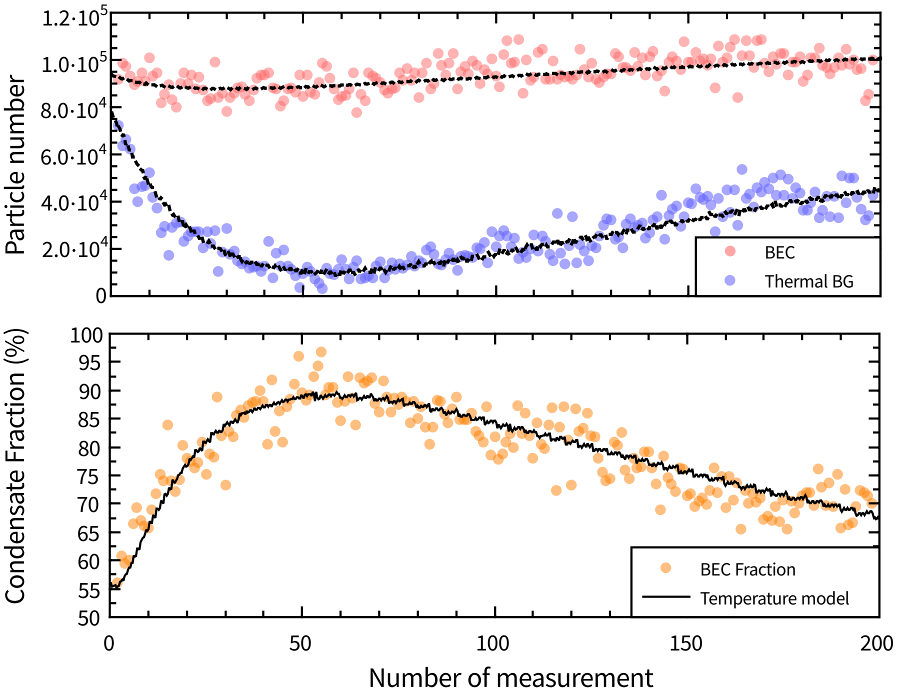

FIGURE 6.20.: Condensate fraction and particle number drifts as a function of temperature. The temperature model of equation 6.3 is able to deliver a good corellation of drift and temperature measured in the specific drivers, revealing a predomindant influence of the X-coils driver temperature, which has been expected.

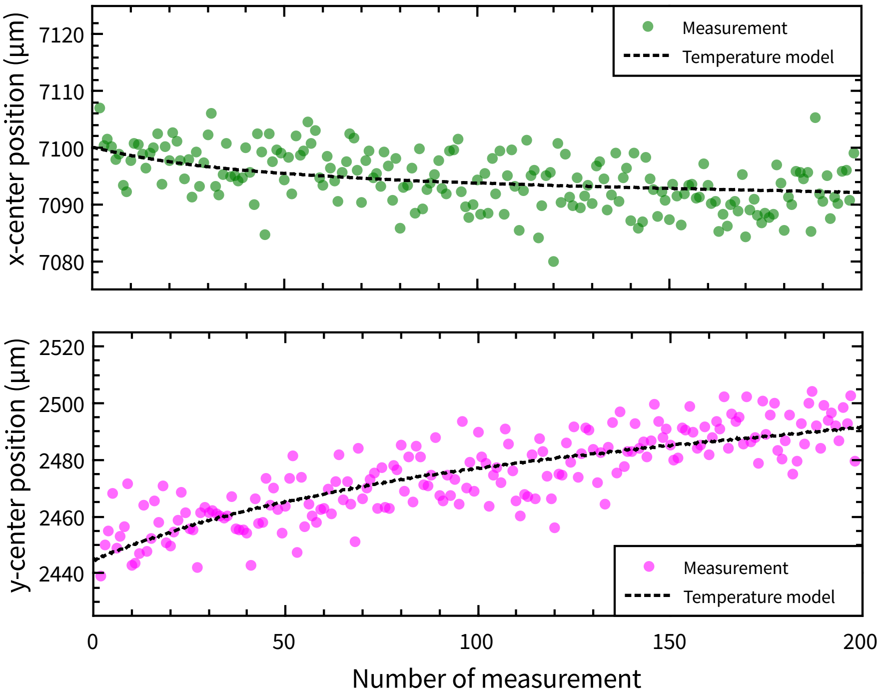

FIGURE 6.21.: Drifts of the center of mass position. The influence of the temperature drifts in the y-axis is much bigger, as it has been initially presumed when constructing the fit model.

derived with several strong assumptions, which are only valid in a very restricted experimental parameter set, it is not very useful to predict future data. For example, with different heating rates, we have seen, that current output drift of the UCCD varies in magnitude, thus different experimental sequences will possibly have different values for the parameters.

Furthermore, the assumption ①, which implies no sympathetic heating between the drivers, is not easy to verify in the integrated payload. Unfortunately, the power board of the Y-coils' driver, featuring the biggest temperature gradient and overall temperature, is very close to the analog feedback measurement of the X-coils driver. Therefore, it might as well lead to a influence on the X-coils, which can not be attributed to the detected temperature on the X-coils' driver sensor. With performance data only and no precision measurement of the actual current flowing, it is not definetly possible to separate the influence of a single driver.

The analysis reveals the relevance of the current drivers for the magnetic traps and their temperature drifts in the integrated payload on general source features such as particle number in the BEC an the position of the released ensemble. For the MAIUS-1 mission, this fact is not optimal but tolerable. With a mission duration of just a fraction of the presented data acquisition time[29], much smaller temperature drift as observed in the pre-testing can be achieved, given an optimized pre-heating procedure, especially for the coils. Overall, although the slight drifts of temperature and particle number had impact on the achievements of the MAIUS-1 mission, these were within tolerable limits. However, for optimal magnetic lensing and precision interferometry, they need to be addressed. This will be done by improving the heat sink construction in the new electronics module, and possibly with additional stabilization measures in the design of the next current driver generation for the successing sounding rocket missions.

6.5. Summary

This chapter, summarizing the results of the characterization of the designed electronics, proved the circuitry as capable to perform the key tasks for the MAIUS-1 mission and beyond.

The reduction of module space and battery number resulted in very compact chip drivers with complete galvanic isolation, enabling the use of more structures on a single chip without changes in the atom chip hardware. The step response waveforms of the driver, however nonlinear, have been shown to be very well predictable with simulation, hence enabling the same level of current control as in commercially available driver structures, with the additional possibility of promptly adaptation switching settings to more complex loads, than possible for the commercial current drivers.

With the more complex bipolar driver structure, the direction of current in the coils can be reversed, while maintaining the single battery configuration with the minor trade-off of nonlinearity in the crossing and the zero current point. These effects have been found to be in acceptable parameters and can be reduced even further by employing intelligent ramps and jumping schemes of the setpoint voltage.

Current noise, being the defining performance feature of specialized atom chip current drivers has been measured comparatively in a standardized manner with all developed circuits and a state-of-the-art commercial current source. The MAIUS-designs proved to be superior to the commercial circuits in all frequency ranges of interest. Noise peaks in the spectrum have been investigated and distributed to their supposed origins, mostly the stack and on-board power

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[29] 200 measurements take approximately 20 min to obtain in the laboratory

supply as well as hardware clocks. None of these peaks have been identified as critical for the MAIUS-1 atom source. Should they be problematic in the future, Software changes and IC replacement provide solutions easily realizable.

The calculation of loss rates on the chip for a realistic trap scenario showed, that the improved current driver designs feature a noise level which lowers the impact of technical noise significantly. With the unipolar chip current driver (UCCD) the disturbances caused by the current driver are reduced to a level, where they cease to be the dominant disturbance source. This is a very important achievement, as the current drivers have always been considered the limiting factor for the lifetimes of atomic ensembles in prior experiments.

Additionally to the noise spectra comparisons, the analysis confirmed the benefit of employing batteries as current sources and the importance of PID tuning for each load.

Focusing towards long term stability and overall precision, thermal drifts have been identified as a major disturbance in the overall reproducibility of currents. While the UCCD features a nonlinear thermal drift below 100 ppm/K, the deviation of the bipolar coil current driver (BCCD) could be modeled with a polynomial model and can be characterized as being below 32 ppm/K, which is comparable with the coefficient of the BCSP-10 reference (25ppm/K)[94]. Additionally, thermal photography has been employed to gather information on heat distribution on critical parts, impairing the stability of the circuits. By optimizing the power board layouts, and implementing thermal stabilization of critical ICs, a further reduction of thermal drift appears to be achievable.

When in thermal equilibrium, both MAIUS circuits show a relative instability which is on par with the commercial benchmark. The UCCD still shows a random-walk type noise influence due to its architecture, while the BCCD performs constantly within the 10^{-6} regime, surpassing the commercial drivers' stability by almost an order of magnitude.

Based on these findings, we conclude that the BCCD excels in all aspects of performance investigated in this chapter. By overcoming its curtailments in operation[30] and improving its thermal design, it will become the design standard for future improved current drivers.

The UCCD, however, with a volume decrease of more than an order of magnitude[31], has pushed the limit on compactness possible, while still being competitive with the former standard atom chip electronics. It's application is still preferable in cases where volume restrictions and maximum current output are given priority before peak performance. Nonetheless, in terms of noise performance, it sets the new standard for atom chip drivers in the QUANTUS cooperation, as its integrated spectral noise density is already a factor four below the predecessor of QUANTUS-2.

Concluding the characterization, the integrated payload with the complete current driver stack has been operated repetitively. During 200 shots, slight drifts in particle number and position of the atomic cloud after time of flight could be observed. With a simple correlation model of driver temperatures, these drifts could be attributed to a part to the temperature drift of the current drivers. Although these drifts are not considered critical towards the achievement of the MAIUS-1 goals, the reduction of the temperature drift of the drivers of great interest for future applications.

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[30] e.g. voltage limitation of current supply and maximum current (ref. section 5.4)

[31] QUANTUS-2 with mechanical alteration: six drivers per 19" rack, 3 U height, 160 mm depth 8.04 cm×13.35 cm ×16 cm, compared to two drivers per module of 10 cm×10 cm×1.7 cm, yields a reduction factor of 20.2 per driver instance.

CHAPTER 7

Discussion & Outlook

The results of this work have been essential for the successful implementation of ultra-compact chip experiments in space. The presented design efforts lead to a vast reduction of the size of the electronics, while simultaneously improving the noise performance in comparison to the state-of-the-art commercial modules formerly in use in the QUANTUS experiments. Moreover, an interface has been created that allows for digital data communication with additional diagnostic information obtained from the drivers.

With the developed simulation models, the prediction and optimization of switching behavior has become much easier, allowing for quick adaption of a current driver regulation to its respective load. Especially in an environment of highly integrated electronics, this is a valuable advantage.

The PI feedback-controlled current drivers, which had been used in QUANTUS-2, suffered from switching distortion due to the integral windup, especially when applied on coils. Supported by the obtained simulation models, the novel designed current drivers have been adapted to this problem. The windup has been compensated with nonlinear elements in the feedback loop of the current controller, which keep the integrator in its operating range. Furthermore, an additional derivative instance enhanced the stability of the controller, thus enabling for more faster switching. The combination of these measures improved the current control in comparison to predecessor experiments significantly, with additional stability due to the elimination of formerly necessary RC elements.

Employing the designed current drivers, the MAIUS-1-mission has been able to perform the first BEC creation in space and gathered substantial information on interferometric techniques on a sounding rocket mission [99]. However, the constructed circuits still have room for improvements, as was determined in the detailed performance analysis. To conclude this thesis, we will discuss the mitigation of the identified imperfections and throw a glance at the possibilities for future application of the current driver technology in projects in the years to come.

In-depth characterization

In chapter 3 and chapter 6, we discussed and estimated the influence of technical current noise on BECs in an atom chip source such as the one of MAIUS-1. However, the experimental characterization of the actual losses, especially in dependence of trap frequency and distance to the chip, has not been possible yet, because the involved experiments have not been available for these extensive measurements. Hence, it remains to be investigated, if the achieved current noise levels pose a dominant loss mechanism in the sequences employed, and if these losses can be mitigated by choosing uninfluenced trap frequencies while maintaining experimental performance. Anyhow, a thorough validation of the current driver noise has to separate the noise-induced particles losses in a static trap from the losses caused of their non-static switching operation, such as the site-to-site atomic transport, which is still ongoing research.

Furthermore, the identified noise peaks in chapter 6 need to be closely monitored for potential parasitic influence in the experiments, especially for interaction with the surrounding electronics. The parts and software settings responsible for their occurrence need to be replaced or damped in order to reduce the overall noise level even further. Depending on the findings of these measurements, additional measures can be taken.

Moreover, the actual integrated setup should be observed during typical experimental sequences, in order to identify and mitigate possible interference with the other electronic components, such as RF amplifiers and sources.

To gather additional information, an increase of the measurable frequency span in current noise measurements would be useful, to include direct measurement of noise in the possible range of the LARMOR-frequencies. While excess noise peaks can be observed with spectrum analyzers, the interesting amplitude range of current noise can only be probed with high-end amplifiers, which require additional financial investment. Until investigations in this area of the frequency range seem necessary, low-passing the output by introducing high-power RF chokes in the current path of the drivers is warranted, inhibiting possible noise influences in the frequency range above 100 kHz.

Improvements on the existing concepts

The laboratory evaluation of the three designs, especially the MAIUS-1 flight hardware, showed the performance of all modules at a level comparable or even superior to the commercial modules of the initial QUANTUS-2 apparatus. Nevertheless, the results indicate a slight advantage for the bipolar coil current driver (BCCD), especially in the key aspects of noise and stability while adding the functionality of bipolar operation with a single battery.

However, even the thermal drift of the best evaluated circuits is clearly notable in the performance of the BEC source of MAIUS-1, which is not problematic, but should be suppressed for future precision measurements. Since the drift of the circuits is almost exclusively attributed to the temperature drifts of the reference current measurement, temperature monitoring of the two participating parts, shunt resistor and measurement amplifier, is advisable for future designs.

Additionally, these parts should be placed separated from the power transistors and ideally thermally shielded. After a characterization of the remaining temperature drift, a feed-forward correction of the setpoint could be enabled via a firmware upgrade. However, for the necessary precision in the µV range, the 16-bit DAC of the current designs would have to be replaced by at least 18-bit models.

Another approach would be the active temperature control of the current measurement ICs. Although this method is simple to implement, the additional heat production from the temperature regulator adds to the already high excess heat of the current drivers.

Both improvement measures require a re-arrangement or even addition of parts, which would reduce the possibility of additional reduction of controller dimensions.

Since the bipolar coil current driver (BCCD) features both superior performance and functionality, it would naturally be a candidate to replace the unipolar chip current driver (UCCD) on the atom chip structures. However, this would require to fit two driver instances to one board, according to the chip driver requirements. This again requires a reduction of the size of the power amplifier stages and controller electronics, which is conflicting with the proposed measures of enhancing the thermal stability. The solution of this problem can only be found by a compromise of high-performance and miniaturization. However, the use of miniaturized packaging for ICs and resistors can help to achieve this solution more easily.

In any case, a general applicability of the BCCD requires to overcome the restrictions in maximum battery voltage, as well as the realization of a more linear operation curve. In order to achieve that, it is important to create an improved version of the bridge amplifier stage, ideally in a biased operation mode to allow for continuous control of the current, without the cross-over distortion, which is occurring due to the non-operability of the output stage for small controller signals.

The integration of all the proposed improvements into the current driver modules will be a central task of the electronic development for the upcoming applications of mobile quantum sensors.

Future projects

For the future evolution of mobile and miniaturized quantum sensors, atom chips will form the backbone of their atomic source. With the possibility of miniaturized current drivers, an atom-chip based BEC source is ideal to rapidly create large condensates, enabling measurements with high contrast and repetition rate, while maintaining a low-power profile during operation.

The quantum gravimeter QG-1 [100], assembled and evaluated in the collaborative research center »geo-Q«[1], is the first compact chip gravimeter aiming to surpass the state-of-the-art solutions for absolute gravimetry. The technology of this thesis will be a key element of the chip-based atom source, delivering more insight on its long-term performance in precision measurements.

In the field of fundamental research, the second sounding rocket mission, MAIUS-2, will enable studies of freely falling atomic ensembles of Rubidium and Potassium. Furthermore, cooling and preparation schemes of atom chip traps with optical dipole traps will be probed, possibly increasing atom number and thus, interferometer sensitivity. In MAIUS-3, the combined two-species cooling scheme plans for the use of FESHBACH-resonances with magnetic field strength of $B \geq 100\,\mathrm{G}$, which requires currents above 5 A in structures comparable to the MAIUS-1 y-coils. As we have seen, these current values are not possible with the BCCD, due to its amplifier architecture. Therefore, the proposed improvements will pose a crucial challenge in order to continue the research in the MAIUS project. As an alternative, the galvanic isolation of the current drivers also allows for the in-line operation of two UCCD of opposite polarity. However, it is yet unclear, if the performance of this solution is suitable for a high precision measurement and is thus only intended for ground pre-testing prior to the MAIUS-2 launch.

In 2018, first long-term measurements on condensed matter will be possible thanks to the Cold Atom Laboratory (CAL) on the International Space Station (ISS)[99], an atom chip experiment operated by the National Aeronautics and Space Administration (NASA). However, the apparatus is not yet able to perform atom-interferometric measurements, but a hardware update is expected in the later stage of the mission, which may be able to add this function. Furthermore, the apparatus employs customized rack electronics for the atom chip operation ([18]), which are, although not compatible with MAIUS, subject to similar requirements for the atom chip application. Their performance will be of interest for direct comparison with the designs developed in this work.

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[1] collaborative research center (SFB) 1128 - »Relativistic Geodesy and Gravimetry with Quantum Sensors« , funded by the Deutsche Forschungsgemeinschaft (DFG) `https://www.geoq.uni-hannover.de`

In any case, interferometry, along with a possible long-term test of the UFF, is proposed to be one of the main objectives for CAL's successor, the joint NASA/DLR project BOSE-EINSTEIN condensate cold atom laboratory (BECCAL), which is also designed to operate on the ISS. Here, an atom-chip apparatus, capable of atom interferometry will be fit into the rack format of the ISS, demanding for even smaller, yet precise current sources to enable long-term, interaction-free, precision measurements. With even greater constraints on power consumption, another architechture change from linear amplifier stages to a sophisticated, adapted pulse-width modulation scheme will be necessary. Along with these improvements, the complete omission of analog controller parts is a logical step, leading to a completely digital, software-based controller. With this architecture, additional functions of the current driver can be implemented simply by software upgrades. A first example of such a function enhancement would be PID auto-tune algorithms, adapting the control parameters to any given inductive and capacitive load without the need for prior simulation. Additionally, digital anti-windup solutions can easily be integrated in these algorithms, in order to make the encountered non-linear overshoot obsolete.

Ultimately, when tests of an ISS experiment are successfully completed, a long-term quantum test of the equivalence principle on a satellite would be the next milestone of space-borne atom interferometry, as it has been proposed in the STE-QUEST mission [49]. Miniaturized, highly effective atom chip sources, tuned for high particle numbers, will be necessary. With sophisticated interferometry schemes, not only the precise survey of gravity will be possible, but also the investigation of another scientific challenge of this century - gravitational waves [101, 102]. Hopefully, countless other opportunities of applications of atom-chip-based quantum sensors will enrich the scientific community — maybe this work will even be a small contribution to that end.

Methods and theoretical additions

A.1. Calculation of damping in a two wire transmission line

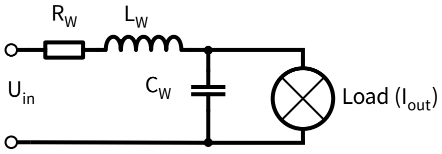

FIGURE A.1.: Schematic of the wire model. The ratio U_{in}/I_{out} is the measure for the damping of the transmission line.

To estimate the impact of the current driver noise on the atoms close to the chip, the transmission line has to be taken into account. While the inductance of the bias coils themselves delivers a low pass filtering, the almost pure ohmic load of the atom chip does not intrinsically set a frequency boundary for transmission of noise.

However, due to finite conductance, cross section, and self inductance and capacitance, the wire transmission line, which has significant length due to the experimental construction, has to be taken into account to determine the spectrum of noise transmission of the current drivers. To achieve a relatively simple description of the system, we take the assumption, that measured current noise above the control bandwidth of the current controller (typ. 2-5 kHz) is not originating from the current source controller itself, therefore to be treated as voltage noise at the position of the transistor gate. In order to estimate its impact on the current flow, we simply calculate the ratio of input voltage to current through an ideal ohmic load with the modeled transmission line in between. The simple model of a discrete RCL-circuit (figure A.1) is valid, since the wavelength of the transmitted current wave is much longer as the length of the transmission line ($c/\omega \gg l$).

To determine the values of the components of figure A.1, we consider a standard, twisted wire pair of length l (total wire length $2l$), separated by the insulation distance d between the current driver (in our treatment the source of noise) and the load, we can calculate the resistance and inductance of this line. From the American Wire Gauge (AWG) standard [103], we obtain the cross-section[1] A and with the specific resistance ρ of copper yield

$$R_W = \rho \frac{2l}{A} . \tag{A.1}$$

The inductance of two parallel wires is basically their self-inductance, considering a different polarity of the signals, as it is given in our case. Therefore, we obtain [104, p.53]

$$L_W = \frac{\mu_0 \mu_r l}{\pi} \cdot \ln\left(\frac{d}{2\sqrt{A/\pi}} + \sqrt{\frac{d}{2\sqrt{A/\pi}} - 1} \right) . \tag{A.2}$$

---

[1] Usually, it is easier to determine the diameter, but in the case of standard wires, the wire itself is not solid, but consists of several smaller wire lines, therefore leading to deviation from a pure circle shaped cross-section, which in our case can be approximated by calculating an effective radius from the given area.

In the same manner as the inductance, the two wires have a capacitance, due to their geometry next to each other. It yields [104, p.53]

$$C_W = \frac{\pi \varepsilon_0 \varepsilon_r}{\ln\left(\frac{d}{2\sqrt{A/\pi}} + \sqrt{\frac{d}{2\sqrt{A/\pi}} - 1}\right)} . \tag{A.3}$$

With these values, a SPICE-based computation of the damping of the employed cables has been performed.

A.2. Derivation of NTC temperature measurement

The temperature of the power parts, especially the high precision current sensor, is crucial to characterize the long-term drift and stability of the current output. It is measured, with a NTC SMD sensor on top of the power aluminum board. Its temperature-resistance correlation is not linear, but follows the STEINHART-HART equation for semiconductors[105]:

$$\frac{1}{\vartheta} = A + B\ln(R) + C\ln(R)^3 \tag{A.4}$$

With fitting parameters A, B and C. As the NTC datasheet features a table of measurement values [106], one can determine the parameters approximately:

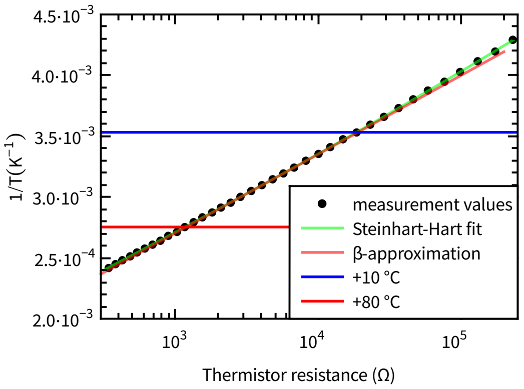

FIGURE A.2.: Fitting curves and the area of interest for our application. The β-approximation offers a more physical approach to the determination of the Temperature with the possibility to replace the NTC without measuring the actual resistance over the whole temperature range.

A	B	C
$9.08 \cdot 10^{-4}$	$2.554 \cdot 10^{-4}$	$1.201 \cdot 10^{-7}$

TABLE A.1.: Fit-parameters for the Steinhart-Hart equation with the NTC dataset.

This equation is very accurate over the whole temperature range. However, as long as R would be sufficiently small, the $\mathcal{O}\left(\ln(R)^3\right)$ term could be neglected, effectively leading to a $R \sim e^{1/\vartheta}$ model for moderate temperatures and drastically reducing computation efforts to determine the temperature in the FPGA. As we are only using temperatures in the 10 to 80 °C, we are approximating the temperature-resistance relation with the β-approximation, effectively assuming $C = 0$, and substituting initial conditions (ϑ_0, R_0) at a specific temperature with one free parameter β, given in the datasheet (figure A.2). Therefore we obtain:

$$\frac{1}{\vartheta} = \frac{1}{\vartheta_0} + \frac{1}{\beta}\ln\left(\frac{R}{R_0}\right) \tag{A.5}$$

In both circuits employing the thermistor to determine the board temperature, we use it in a voltage divider configuration, depicted in figure A.3. With some minor calculations, using the 10 Bit Range of the ADC over U_0, we obtain, with θ being the numerical value of the digitalization:

$$\frac{\theta}{2^{10}-1} = \frac{U_2}{U_0} = \frac{R_2}{R_1 + R_2} \tag{A.6}$$

$$\Longleftrightarrow \quad R_2 = R_1 \cdot \left(\frac{2^{10}-1}{\theta} - 1 \right)^{-1} \tag{A.7}$$

As R_2 is our independent variable in equation A.5, and we used the design constraint $R_0 = R_1$, we insert, solving equation A.5 for ϑ:

$$\vartheta = \frac{\beta}{\frac{\beta}{\vartheta_0} - \ln\left(\frac{2^{10}-1}{\theta} - 1 \right)} \tag{A.8}$$

With this assumption, the precision of the temperature measurement is better than 0.5 °C.

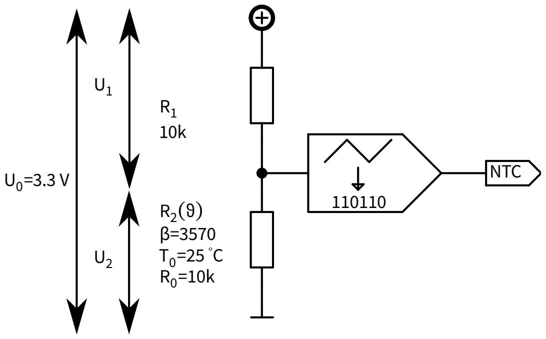

FIGURE A.3.: Schematic of the NTC wiring and readout

A.3. Calculation method of the current noise spectral density

In order to obtain illustrative data for comparison of current noise spectra, an elaborate method of data treatment was used, which is presented in general in [107]. The specific method used in this work shall be described here for reference in later comparison.

A.3.1. Data aquisition

The signal in question is sampled as an oscilloscope time series, in N measurements, with a constant frequency ν_s, yielding datasets with N Tuples (τ_k, u_k), representing the time index and a corresponding voltage peak value. After the measurements, a frequency resolution ν_{res} is chosen, effectively setting the bandwidth $\mathcal{B}$ of the measurement by applying the SHANNON-NYQUIST-theorem. In order to avoid unnecessary oversampled calculation, all items with u_k with $k > n$ are omitted for further evaluation.

$$n := \frac{\nu_{\text{s}}}{\nu_{\text{res}}} \quad , \quad n \leq N \quad , \quad \mathcal{B} = \frac{n}{2} \cdot \nu_{\text{res}} \tag{A.9}$$

As the time series contains only redundant information in the τ_k these values are omitted as well, assuming constant sampling. This leaves n measurement sets of u_k values.

A.3.2. Weighting and scaling

In order to avoid leakage effects in the FOURIER-transform due to the finite length of the sample, a weighting function is usually employed in order to suppress additions in the noise spectrum due to the mathematical treatment of the data. In order to obtain precise frequency resolution without much curtailment in amplitude trueness, a Blackman-Harris-window function was chosen, defined as series of factors

$$w_k = a_0 - a_1 \cos\left(\frac{2\pi k}{n-1}\right) + a_2 \cos\left(\frac{4\pi k}{n-1}\right) - a_3 \cos\left(\frac{6\pi k}{n-1}\right) \quad , \quad (k \leq n-1) \tag{A.10}$$

with

$$a_0 = 0.35875; \quad a_1 = 0.48829; \quad a_2 = 0.14128; \quad a_3 = 0.01168\,. \tag{A.11}$$

The convolution of the weighting and the original data, additionally scaled from the unit V_{pk} to V_{rms} yields

$$d_k = \frac{u_k}{\sqrt{2}} \cdot w_k\,. \tag{A.12}$$

A.3.3. Discrete Fourier transform

In order to obtain a frequency decomposition of the noise signal, the d_i now undergo a discrete fourier transform of the form that yields a new complex-valued vector of y_k

$$y_k = \sum_{j=1}^{n} d_j \cdot e^{\imath 2\pi \frac{(j-1)(k-1)}{n}}\,. \tag{A.13}$$

To prevent DC offsets to influence the low Hz-band, it is useful to normalize the time series before the transformation by subtracting the arithmetic mean:

$$d'_k = d_k - \frac{\sum_{j=0}^{n} d_j}{n}\,. \tag{A.14}$$

It is often useful to use this arithmetic mean as the DC component at 0 Hz, if necessary. In our case, due to the AC coupling of the amplifier, this value is of no physical meaning.

A.3.4. Power Spectral Density

In order to obtain a power spectrum out of the Fourier-transformed data, several rescaling processes are necessary.

The application of a weighting window suppresses the noise of undesired frequency contributions in order to increase frequency accuracy of mesurements by introducing a shift in amplitude values and vice versa. Therefore it is useful to calculate factors necessary to normalize obtained spectra in the later process. They are defined as

$$\mathcal{S}_1 := \sum_{j=0}^{n-1} w_k \quad , \quad \mathcal{S}_2 := \sum_{j=0}^{n-1} w_k^2 \tag{A.15}$$

With these sums, one can define the *normalized equivalent noise bandwith* $\mathcal{N}$, which depends on the form of the window, the number of samples and the resolution frequency

$$\mathcal{N} = n \cdot \frac{\mathcal{S}_2}{(\mathcal{S}_1)^2} \tag{A.16}$$

Similarly, we obtain the effective noise equivalent bandwidth $\mathcal{K}$:

$$\mathcal{K} = \mathcal{N} \cdot \nu_{\text{res}} = \nu_s \cdot \frac{\mathcal{S}_2}{(\mathcal{S}_1)^2}. \tag{A.17}$$

Now the *power spectrum* $\mathfrak{S}_k$ can be calculated:

$$\mathfrak{S}_k = \frac{2 \cdot |y_k|^2}{\mathcal{S}_1^2} \tag{A.18}$$

The factor »2« takes into account, that only $n/2$ elements are used, with the other half containing redundant data. The elements at $\nu = 0$ and $\nu = n/2$ must not be multiplied by 2, as they are singular in the spectrum. Since they are not regarded in our measurements, as the DC value is substracted by the AC filter and the cutoff frequency is below $n/2$, this simple calculation is valid.

However, the power spectrum is of the unit V, but we are interested in the *power spectral density* which can be integrated over the frequency window of interest. It is calculated by

$$S_k = \frac{\mathfrak{S}_k}{\mathcal{K}} = \frac{2 \cdot |y_k|^2}{\nu_s \cdot \mathcal{S}_2} \tag{A.19}$$

The results are now attributed to frequencies in tuples $S(k \cdot \nu_{\text{res}}\,, S_k)$ with $\left(k = 0 \ldots \frac{n}{2}\right)$. As there were n datasets in the beginning, there are also n power spectra to be averaged in each bin. To be done correctly, this averaging has to be done before rescaling.

A.3.5. Rescaling and calibration

The resulting power spectral density has the unit $\text{V}_{\text{RMS}}^2/\sqrt{\text{Hz}}$. To have an illustrative figure of current noise, this power spectrum has to be scaled with the calibration factor due to the resistance $\mathcal{R}$ of the shunt resistor. Afterwards, the linear power spectrum can be obtained by taking the square root of the power spectrum, therefore depicting the RMS equivalent current noise level in the resulting plot.

As a preamplifier has been used, its gain figure has to be taken into account, which is not exactly disclosed by the manufacturer, but can, based on the graphs in the data sheet [108], be well approximated for the 60 dB-stage with the function

$$g(\nu) = 60\text{dB}\left(\frac{1}{1 + \left(\frac{\nu}{250\,\text{kHz}}\right)^3}\right) \tag{A.20}$$

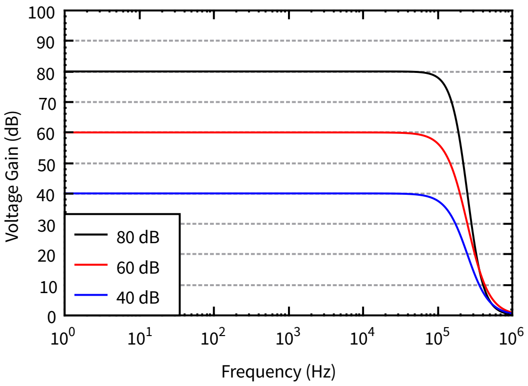

FIGURE A.4.: Gain Figure models for the FEMTO amplifier. The 60 dB-setting was used exclusively in the noise comparison.

The final transformation yields then the final y-values for our presentation, the *linear current spectral density*, pairing the (unscaled) frequencies of the DFT, with the new y-values I_k:

$$\mathcal{I}_k = \frac{1}{\mathcal{R}}\sqrt{S_k} \cdot 10^{-\frac{1}{20} \cdot g(k \cdot \nu_{\text{res}})}. \tag{A.21}$$

The resulting spectrum has now the unit $A_{\text{RMS}}/\sqrt{\text{Hz}}$. However, to get a proper estimate of the current noise equivalent, it is necessary to integrate over the power spectral density and scale the result accordingly afterwards.

$$\tilde{\mathcal{I}} = \frac{1}{\mathcal{R}}\sqrt{\sum_{k=1}^{\nu_1/\nu_{\text{res}}} S_k \cdot \nu_{\text{res}} \cdot 10^{-\frac{1}{10}\cdot g(k\cdot \nu_{\text{res}})}} \tag{A.22}$$

A.4. Allan variance with considerable dead time

In subsection 6.3.3, the relative instability of the current drivers have been calculated. Usually, the plot and the calculation is widely referred to as the »ALLAN-variance method«. However, the classical ALLAN-variance differs from the calculation employed. In order to circumvent disambiguities, I will give a short wrap-up of the calculation method.

The samples y_i, obtained in the measurement have been sampled with a samplerate of 2 Hz, thus have a sample distance of $T_0 = 500\,\text{ms}$. The measurement device, when probed, delivers a current value over 10 cycles of power supply AC cycles, yielding a measurement window of $\tau_0 = \frac{10}{50\,\text{Hz}} = 200\,\text{ms}$.

With these values, a significant dead time between measurements is obtained, as sampling frequency could not be increased due to software limitation. As a result, it is not valid to use the standard ALLAN variance as it assumes $T_0 = \tau_0$. Furthermore, the total values of the currents do not account for all fluctuations between measurements. Hence, it is useful to take a look at the generalized N-Sample variance[109, Eq.(11)]

$$\varsigma^2(N, T, \tau) = \frac{1}{N-1}\left(\sum_{n=0}^{N-1}\left[\frac{\Phi(nT+\tau)-\Phi(nT)}{\tau}\right]^2 - \frac{1}{N}\left[\sum_{n=0}^{N-1}\frac{\Phi(nT+\tau)-\Phi(nT)}{\tau}\right]^2\right). \tag{A.23}$$

In order to follow the evaluational value of a two-sample variance, we choose N=2 for all further calculations. Equation A.23 considers a continous function Φ, which measurements are averaged over the measurement time τ. In our case, these averages have already been performed in the measurement device, yielding the values $\overline{y}_i$, each averaged over τ_0. If $N = 2$ and $\tau_0 = T_0$, Equation A.23 becomes the standard ALLAN-variance [110]:

$$\sigma^2(\tau) = \frac{1}{2}\left\langle(\overline{y}_{i+1} - \overline{y}_i)\right\rangle . \tag{A.24}$$

The pointy brackets denote for the expectation value operator, which includes the explicit mean denoted in equation A.23. Although the simplicity of the ALLAN-variance is compelling, it is not accurate to fit our measurement. Since $\tau_0 \neq T_0$, the dead time of the measurement has to be taken into account. As we want to employ a variance analysis over several values of the integration time $\tau = M \cdot t_0$. Therefore, usually neighboring values in the dataset are averaged into bins, which are then evaluated with the sample variance. We define

$$\tilde{y}_i(M, \tau = M\cdot\tau_0, T = M\cdot T_0) = \frac{1}{M}\sum_{n=1}^{i+M-1}\overline{y}_n\,, \tag{A.25}$$

implicitly keeping in mind, that the data points are sampled with T_0, but have been averaged over τ_0, thereby including a deviation from equation A.24. Therefore we can generalize equation A.24 for dead time measurements as

$$\varsigma_y^2(N=2,M,T,\tau) = \frac{1}{2}\left\langle(\tilde{y}_{i+1}-\tilde{y}_i)\right\rangle . \tag{A.26}$$

Since we have a considerable death time ($r := T/\tau > 1$), a standard approach to calculate the ALLAN-variance would be a significant distortion, introduced by dead time between measurements. To obtain values comparable to σ^2, it is therefore mandatory to introduce certain bias functions that take the mismatch of the timings into account.

Their derivation are explained in detail in [111] and [112]. In the case of a two-sample variance (N=2), only the two functions B_2 and B_3 are necessary. Both rely on the the parameter μ, determined by the power law of the PSD of the raw data, which can be computed and fitted.

Assuming the PSD of the data follows a ν^α power law, the exponent of the frequency determines μ in the following mapping:

$$\mu = \begin{cases} -2 & \text{if} \quad \alpha \geq 1 \\ -(\alpha+1) & \text{if} \quad -3 < \alpha \leq 1 \\ & \text{not defined otherwise} \end{cases} \tag{A.27}$$

With this nomenclature, one can define the bias functions according to [112]

$$B_2(r,\mu) = \frac{\varsigma^2(N,T,\tau)}{\varsigma^2(N,\tau,\tau)} = \frac{1+\frac{1}{2}\left(2|r|^{\mu+2}-|r+1|^{\mu+2}-|r-1|^{\mu+2}\right)}{2\left(1-2^{\mu}\right)} \tag{A.28}$$

and [111]

$$\begin{aligned} B_3(N=2,M,r,\mu) &= \frac{\varsigma_y^2(2,M,T,\tau)}{\varsigma^2(2,T,\tau)} \\ &= \frac{2M + M\cdot\mathfrak{F}[Mr] - \sum\limits_{i=1}^{M-1}(M-i)\left(2\mathfrak{F}[ir]-\mathfrak{F}[(M+i)r]-\mathfrak{F}[(M-i)r]\right)}{\left(\mathfrak{F}[r]+2\right)\cdot M^{\mu+2}} \end{aligned} \tag{A.29}$$

with

$$\mathfrak{F}(x) = 2x^{\mu+2} - (x+1)^{\mu+2} - |(x-1)|^{\mu+2} \tag{A.30}$$

The bias function B_1 exists, hence the nomenclature, but has unity value for our case of N=2, therefore is not defined here.

While usually the ALLAN-variance is investigated in a plot with varying integration times, B_3 has a function that can even influence the shape of the plot, e.g. to find a minimum of instability. The complete estimate for a two-sample variance of the ALLAN-type yields to a function that can be compared with a standard type ALLAN-variance:

$$\sigma^2(M,T,\tau,\mu) = \frac{\varsigma_y^2(N=2,M,T,\tau)}{B_2(r,\mu)\cdot B_3(N=2,M,r,\mu)} \tag{A.31}$$

The square root of this function is the ALLAN-deviation used in this work.

APPENDIX B

Supplementary data and graphs

This appendix shall provide useful, but not necessary information obtained during the evaluation process of this work. Hopefully, future researchers will find a baseline for further improvements of the circuitry. The pure scientifically interested reader may relievedly close this chapter. You will probably not miss anything if you do.

B.1. Detailed current noise spectra of the MAIUS current drivers

While the work at hand has demonstrated the adequate performance of the designed current sources in their particular field of application, there is always room for further improvement. Therefore, this section includes the graphical representation of the recorded current noise spectra for further reference in data analysis or future design studies (figures B.1 to B.4).

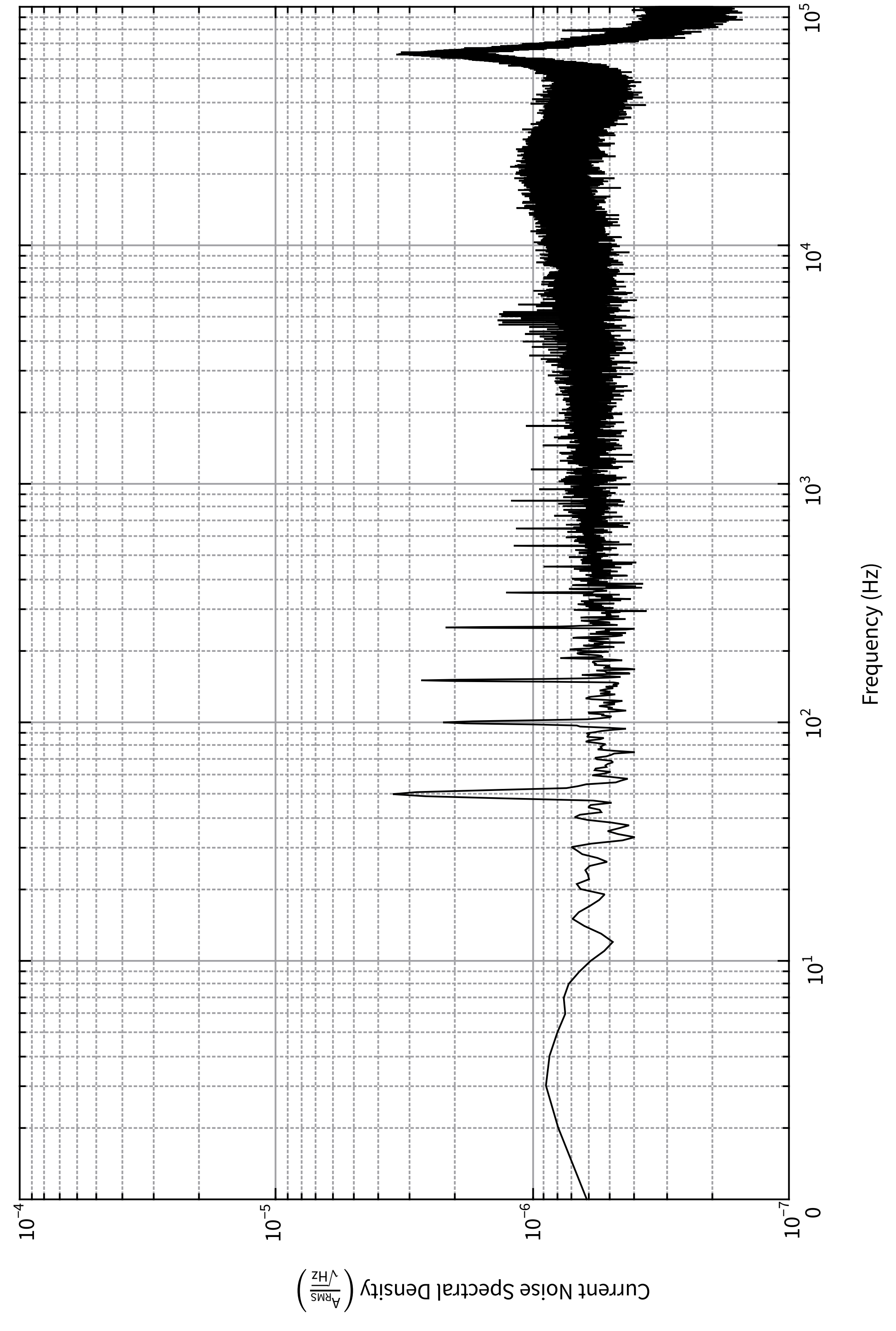

FIGURE B.1.: Detailed noise spectrum of the MAIUS lab-based current driver.

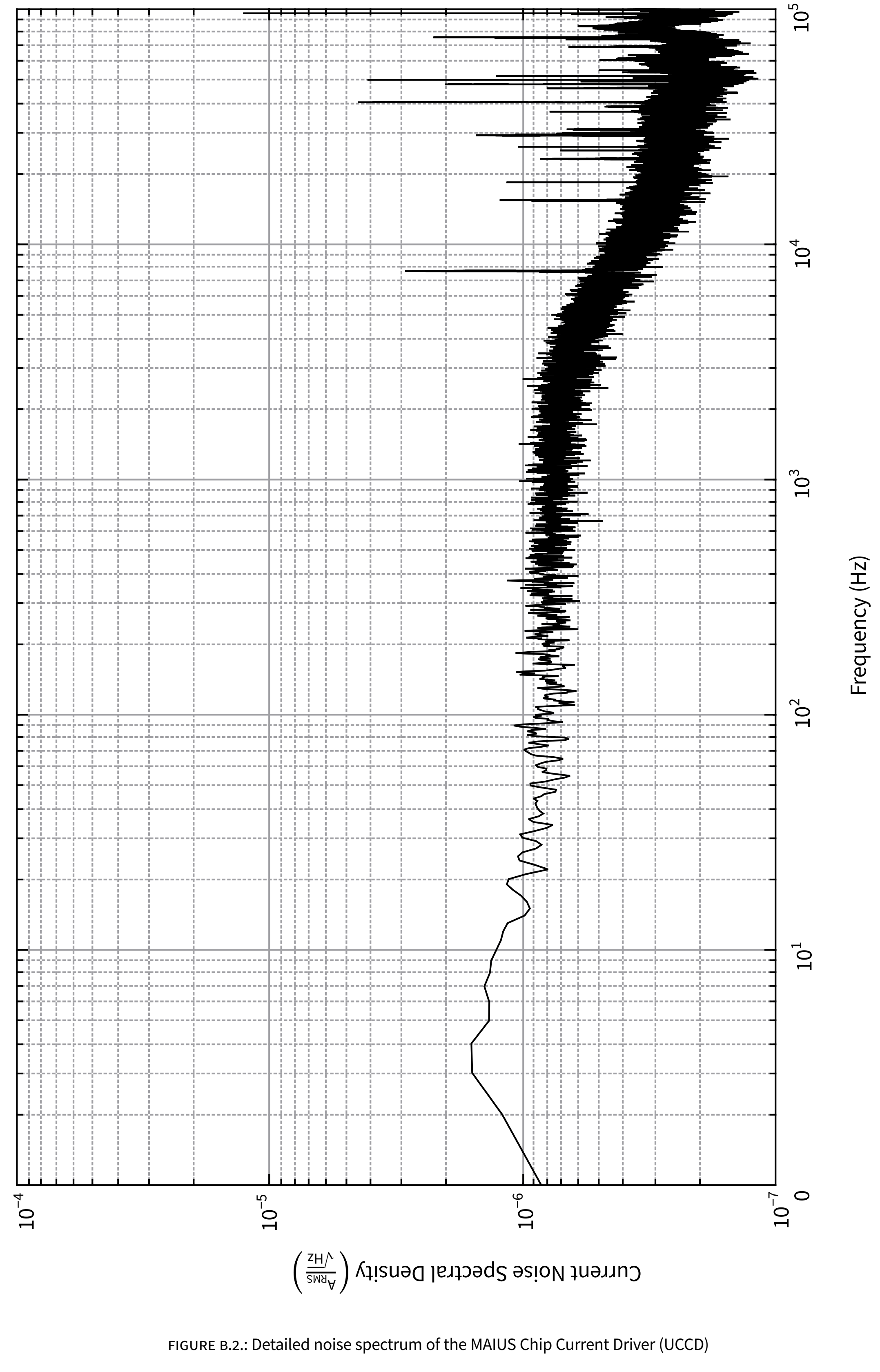

FIGURE B.2.: Detailed noise spectrum of the MAIUS Chip Current Driver (UCCD)

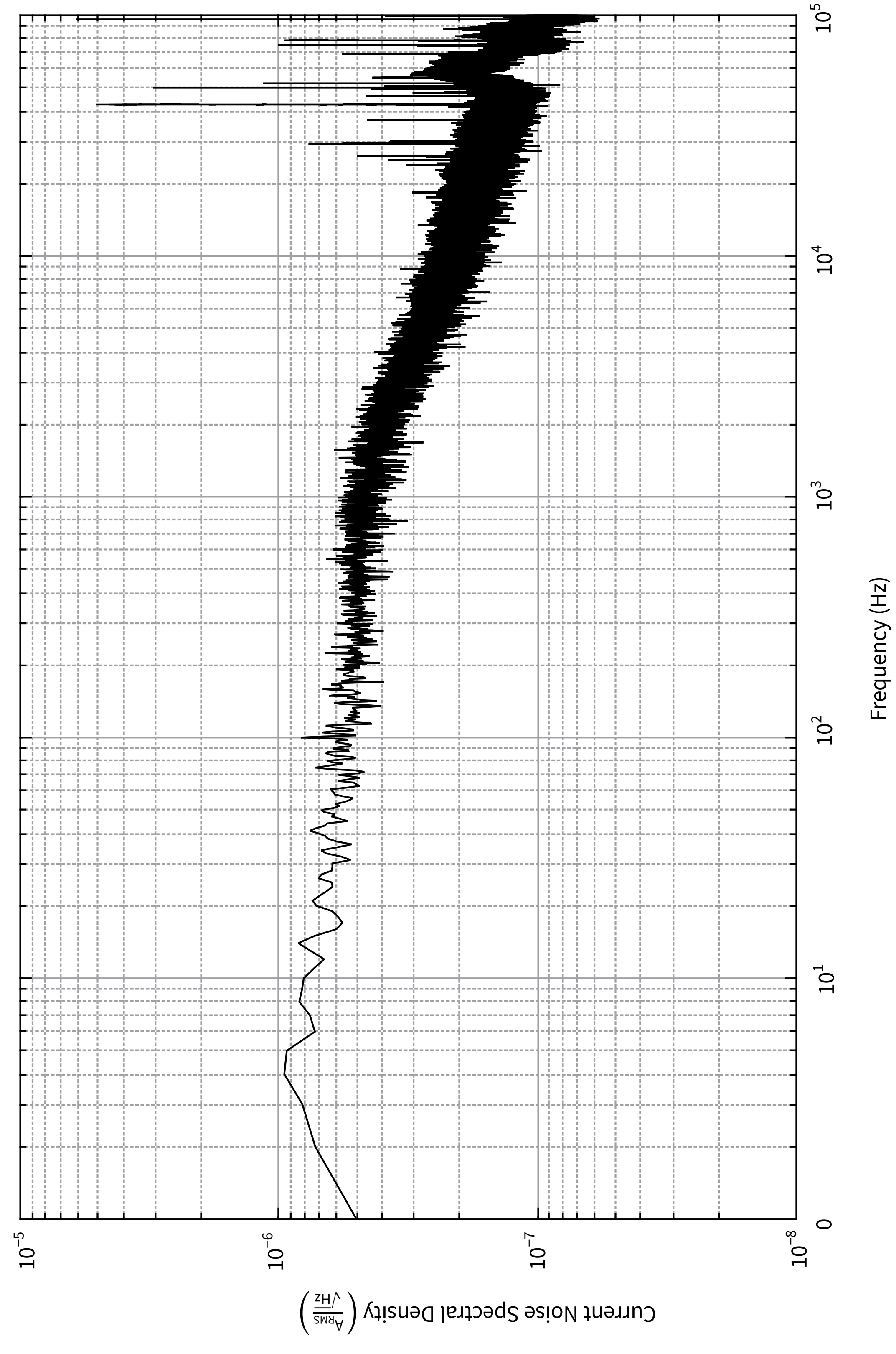

FIGURE B.3.: Detailed noise spectrum of the MAIUS Coil Current Driver (BCCD). Note the different scaling on the Y axis.

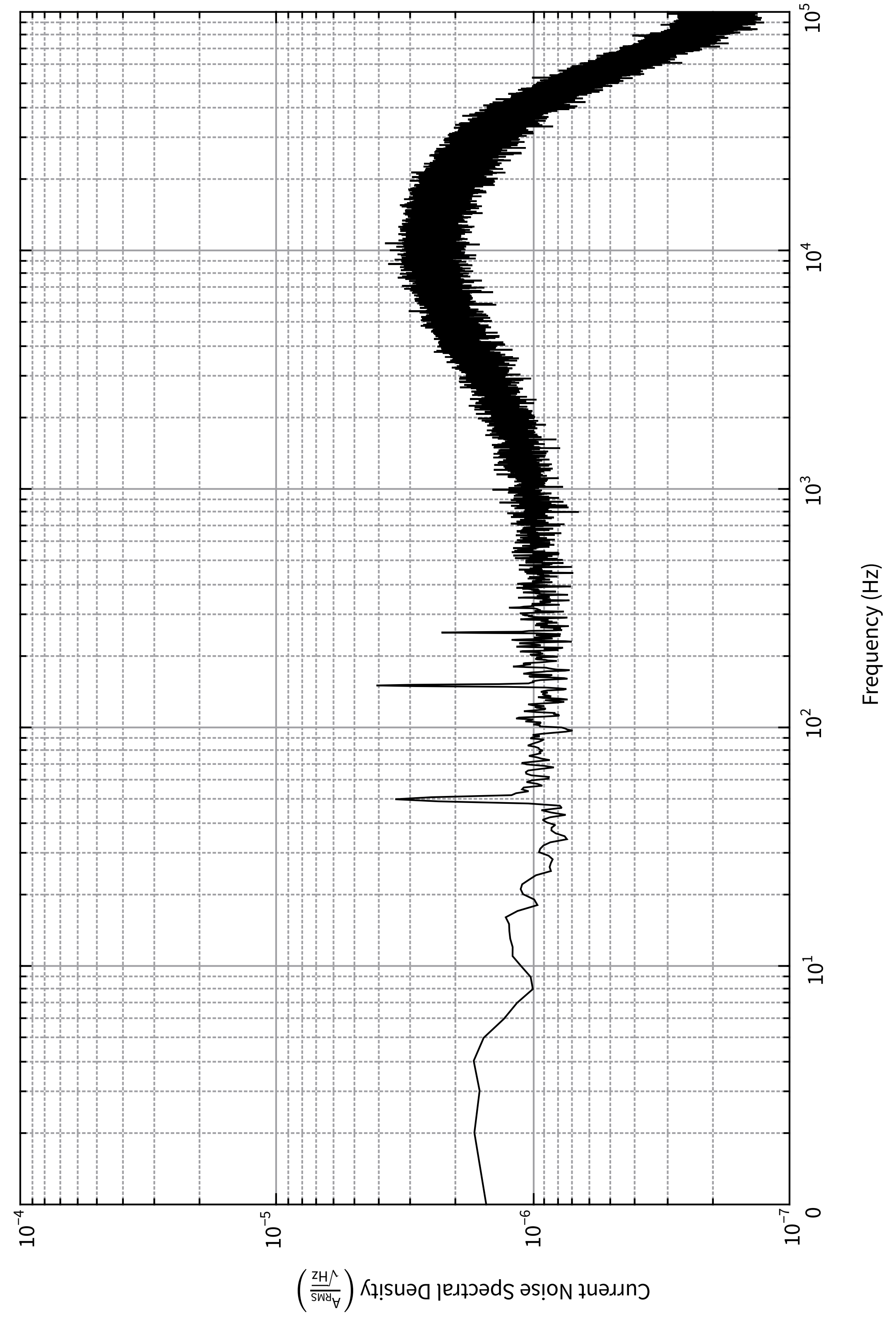

FIGURE B.4.: Detailed noise spectrum of the HighFinesse BCSP-10

B.2. Overview of missions utilizing the designed hardware

While the majority of efforts in design and adaption of the circuitry involved in this work has been done in the QUANTUS consortium, quite a few other projects could benefit from the results achieved. The author was not involved in operations of the lab experiments PRIMUS, QG-1 and iSense, therefore these three shall only be mentioned here in the appendix.

experiment / project	employed units	platform	application
PRIMUS 2	MLCD	drop tower	bias coils
iSense	MLCD	portable gravimeter Rb clock	atom chip
QUANTUS-2	MLCD chip safety	drop tower	2D MOT & mesoscopic structures
MAIUS-A	MLCD	lab (ground pretesting)	2D MOT atom chips, bias coils
MAIUS-A	UCCD, BCCD, chip safety	VSB 30 sounding rocket (flight configuration)	2D MOT atom chips, mesoscopic structures, bias coils
QG-1*	UCCD, BCCD, chip safety	portable gravimeter	lab evaluation: atom chip, bias coils
MAIUS-B*	UCCD, BCCD, chip safety	ground pretest & flight configuration	2D MOT atom chips, mesoscopic structures, bias coils

TABLE B.1.: Summary of experiments employing circuitry of this work. Experiments marked with »*« are not yet fully operational, but have been supplied with hardware.

B.3. Numerical values of physical constants

symbol	physical quantity	value	unit
c	speed of light in vacuum	299 792 458	$\mathrm{m\,s^{-1}}$
ε_0	dielectric constant	$8.854\,187\,817 \cdot 10^{-12}$	$\mathrm{F\,m^{-1}}$
$\hbar$	reduced Planck's constant	$1.054\,571\,726(47) \cdot 10^{-34}$	J s
k_B	Boltzmann's constant	$1.380\,648\,8(13) \cdot 10^{-23}$	$\mathrm{J\,K^{-1}}$
μ_0	magnetic constant	$12.566\,370\,614 \cdot 10^{-7}$	$\mathrm{N/A^2}$
q	charge of the electron	$1.602\,176\,565(35) \cdot 10^{-19}$	C
ρ_c	electrical resistivity of copper @ 20 °C	$16.78 \cdot 10^{-9}$ Source:[113]	Ω m
μ_B	Bohr magneton	$927.400\,968(20) \cdot 10^{-26}$	$\mathrm{J\,T^{-1}}$

TABLE B.2.: Numerical values of physical constants. If not indicated otherwise, source is [114]

B.4. Values of MAIUS-1 experimental structures

structure	phys. quantity	value
Meso U	resistance	125 mΩ
Meso I	resistance	67 mΩ
Meso H_1	resistance	68 mΩ
Meso H_2	resistance	64 mΩ
Base Z	resistance	386 mΩ
Science Z	resistance	1066 mΩ
2D MOT coils	resistance	2.5 Ω
2D MOT coils	inductance	745 µH
x-bias coil	resistance	1.4 Ω
x-bias coil	inductance	368 µH
x-bias coil	mag. field gain	$2.47\,\mathrm{G\,A^{-1}}$
y-bias coil	resistance	2.9 Ω
y-bias coil	inductance	4.72 mH
y-bias coil	mag. field gain	$13.92\,\mathrm{G\,A^{-1}}$
z-bias coil	resistance	900 mΩ
z-bias coil	inductance	341 µH
z-bias coil	mag. field gain	$5.31\,\mathrm{G\,A^{-1}}$

TABLE B.3.: Values of experimental data used for calculations and numerical simulation. [MAIUS: Measurement, 9.08.16]

B.5. Calculated magnetic field noise spectra for MAIUS-1

This section contains detailed magnetic noise spectra, which are calculated with the measured current noise spectrum $\mathcal{I}$ multiplied by the normalized standard impedance of an idealized coil. Afterwards the measured magnetic field gain $\mathcal{G}$ is multiplied with the result:

$$B_k(\nu) = \mathcal{I}_k(\nu)\cdot\frac{R}{\sqrt{R^2+(2\pi L\nu)^2}}\cdot\mathcal{G}_k\,. \tag{B.1}$$

B.5.1. Anticipated Magnetic field noise in MAIUS-1

Additionally, the overall magnetic noise can be calculated from the PSD $P(\nu)$ analog to the current spectral noise level, according to the equation

$$\Delta B(\nu_{\text{stop}}) = \mathcal{G}\cdot\int_0^{\nu_{\text{stop}}} d\nu\,P(\nu)\cdot\frac{R^2}{R^2+4\pi^2L^2\nu^2}\,, \tag{B.2}$$

with the results in summarized table B.4. The combined magnetic noise level of the coils lies close or below 100 µG and thus is very well within the desired level of magnetic field quality of $\Delta B \leq 1\,\mathrm{mG}$.

structure Freq. Span	x-coil	y-coil	z-coil
1 – 99840 Hz	$3.591\cdot10^{-5}\,\mathrm{G_{RMS}}$	$1.002\cdot10^{-4}\,\mathrm{G_{RMS}}$	$6.835\cdot10^{-5}\,\mathrm{G_{RMS}}$
1 – 10000 Hz	$3.581\cdot10^{-5}\,\mathrm{G_{RMS}}$	$1.002\cdot10^{-4}\,\mathrm{G_{RMS}}$	$6.835\cdot10^{-5}\,\mathrm{G_{RMS}}$
1 – 1000 Hz	$3.188\cdot10^{-5}\,\mathrm{G_{RMS}}$	$9.884\cdot10^{-5}\,\mathrm{G_{RMS}}$	$6.319\cdot10^{-5}\,\mathrm{G_{RMS}}$
1 – 100 Hz	$1.519\cdot10^{-5}\,\mathrm{G_{RMS}}$	$7.897\cdot10^{-5}\,\mathrm{G_{RMS}}$	$3.321\cdot10^{-5}\,\mathrm{G_{RMS}}$

TABLE B.4.: Overall magnetic noise levels in different frequency ranges. The noise levels are obtained for the BCCD.

B.5.2. Magnetic field noise of the X-coils

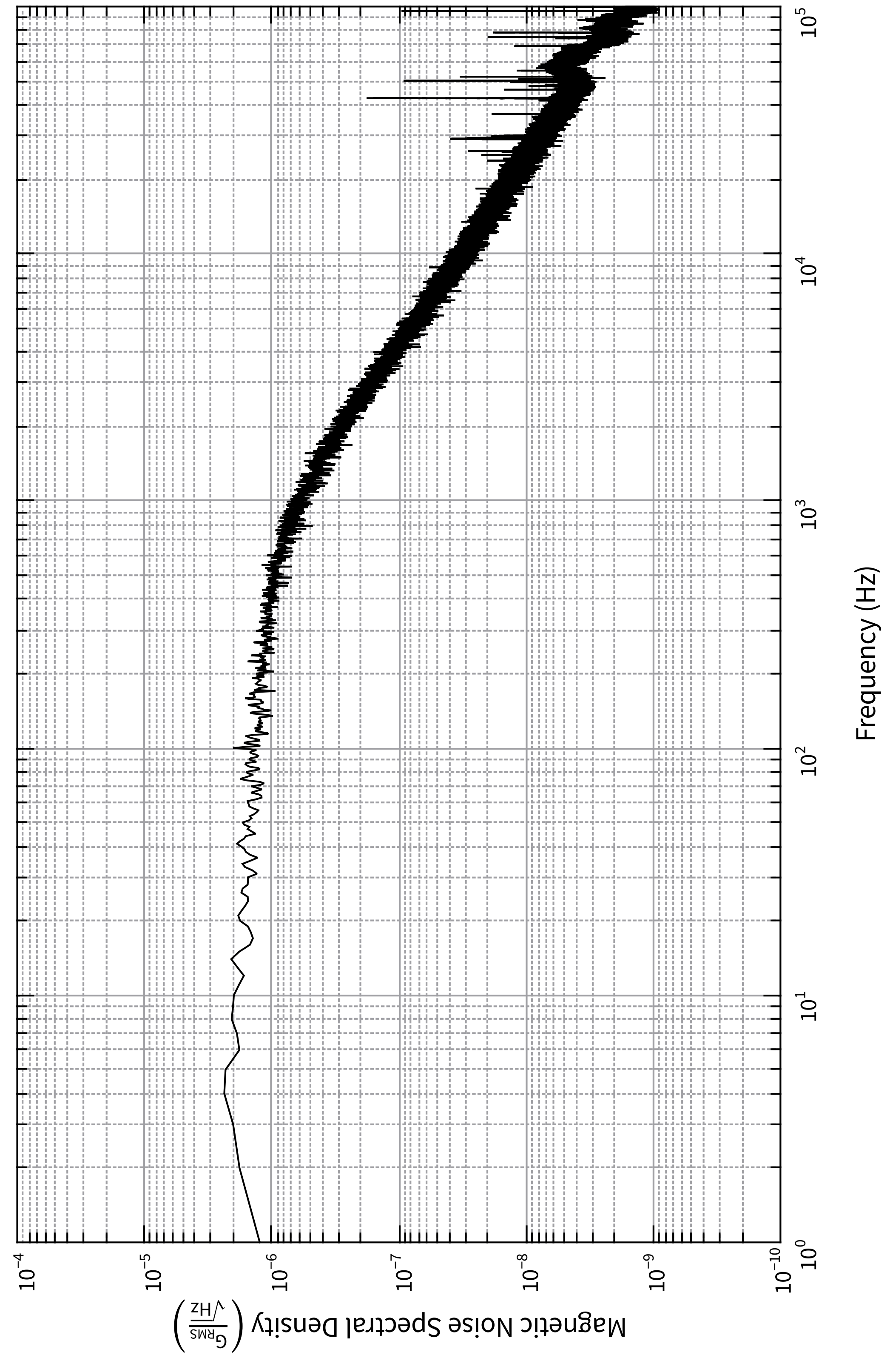

FIGURE B.5.: Magnetic field noise of the X-coils

B.5.3. Magnetic field noise of the Y-coils

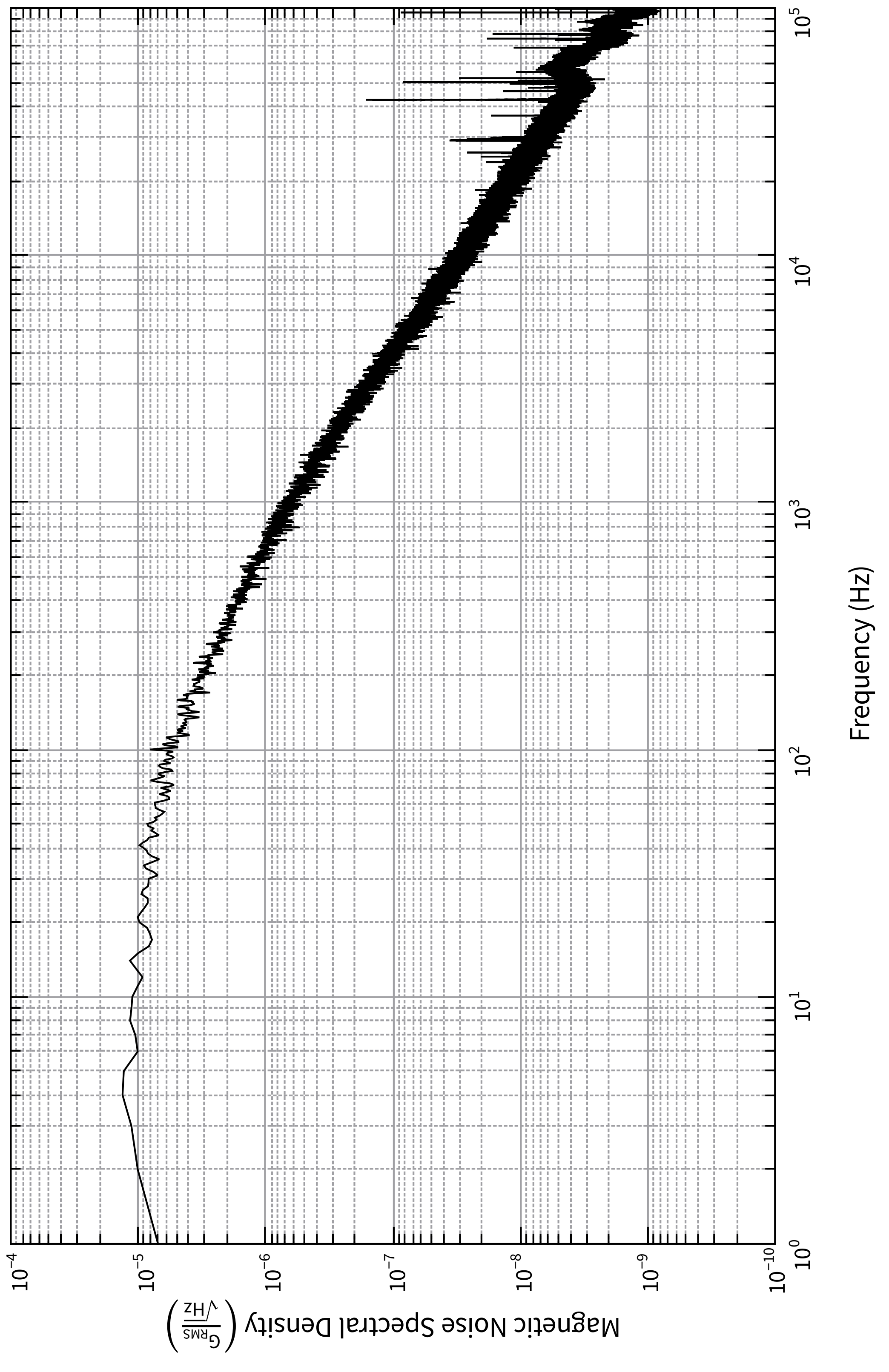

FIGURE B.6.: Magnetic field noise of the Y-coils

B.5.4. Magnetic field noise of the Z-coils

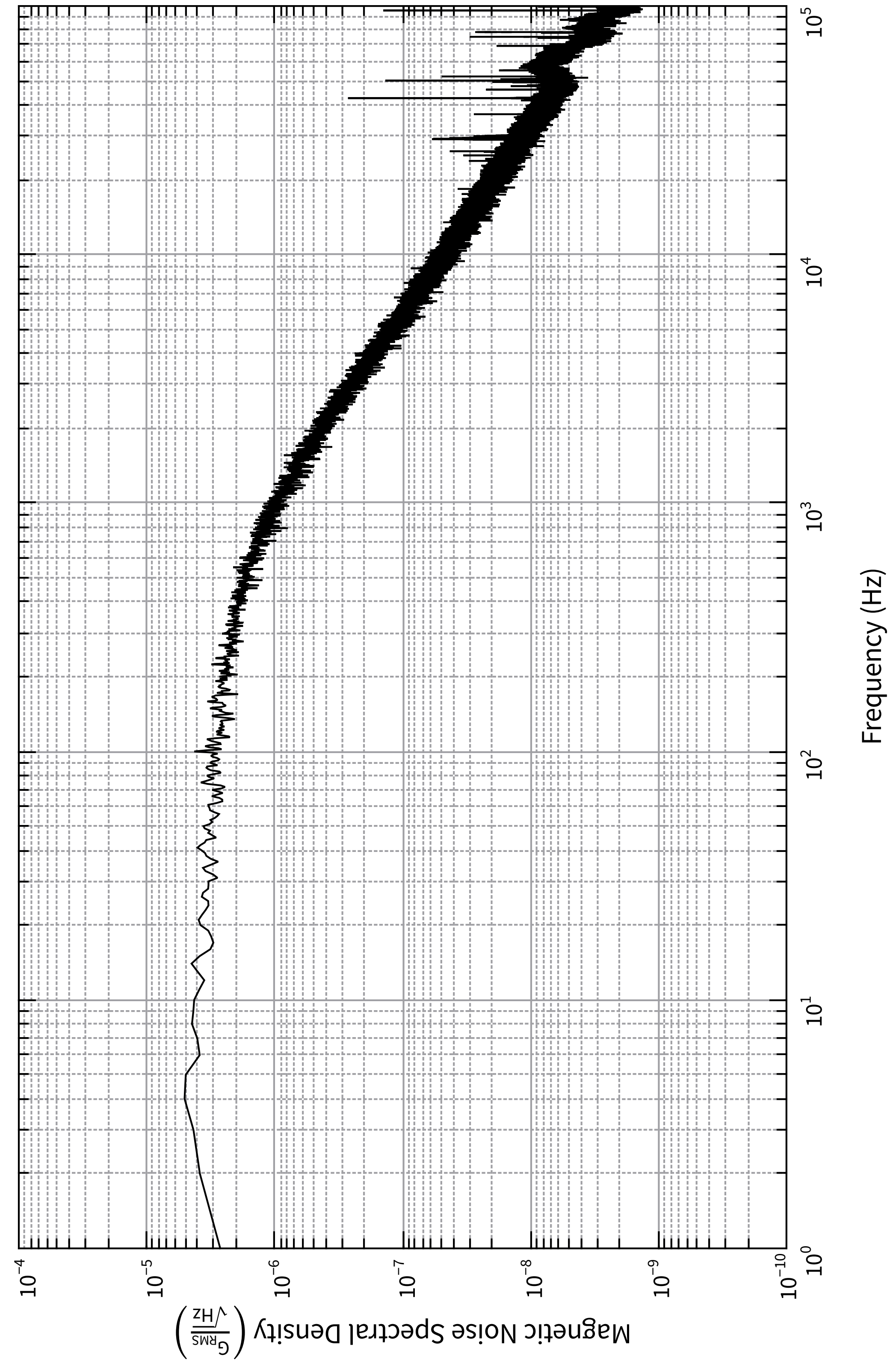

FIGURE B.7.: Magnetic field noise of the Z-coils

APPENDIX C

Software

The software of the MAIUS-1 has been developed in two stages. A LabView®-based Windows software, that is described in section 4.1, and a sophisticated self-programmed solution based on Linux. Because all tests in this thesis have been performed in the first stage, only the Windows-based software will be treated here.

C.1. Basic description of employed XML formats

The backbone of the TBUS software implementation is the `TBUS.DLL`. It is a dynamic link library programmed in `PASCAL`, providing basic functions for read/write communication with the stacks as well as with single modules. For the purpose of this chapter, only the functions `Set*Param` and `Get*Param` are of importance, where »*« can stand for a boolean, a float or an integer number of 32 Bit depth.

The next instance of Software implementation is the `Card.xml` file. It defines parameters that are callable for the specific card type and is the same for every TBUS module of the same type.

The preamble defines an `UTF-8` encoded XML file, as well as the card module name which can be later called by the Software.

```xml
<?xml version="1.0" encoding="utf-8"?>
<Card name="DayCounter">
```

Initially, the *parameters* of the card and their data type are defined. It is possible to give a standard value, minimum and maximum range, although the TBUS in its current development stage usually ignores these settings. The names given in the `name` category can be comma separated with a short or a long name for convenience.

A standard definition of an integer parameter in the XML syntax would be:

```xml
<IntegerParameter name="Day of month,DOM" defaultvalue="1" min="1" max="31" />
```

The definition of float and boolean parameters is analog to this scheme.

While the parameters can now be read individually from a data stream, the readout/write cycles are defined in *registers*, which map the pre-defined parameters to the TBUS datastream. The stream provides a 8 Bit wide 16x16 Bit address space. The MSB is usually used for the inter-stack address distribution while the LSB is used for the BUS write pattern. Therefore, a 8x16 Bit datastream for upload and download is accessible. The address can be given in decimal or hex code. A simple example, for example to write the 8 most significant bits of the defined parameter:

```
<Register name="Set Day of Month" PreferedMethod="Default" DefaultDuration="100ns">
<BusPattern address="+3" direction="w" pattern="DOM[7],DOM[6],DOM[5],DOM[4],DOM[3],
    DOM[2],DOM[1],DOM[0]" />
</Register>
```

The direction »r« is defining a readout. It is possible to write and readout several parameters in on register. While this XML-format provides easy communication definitions, it lacks the features of easy conversion or basic mathematical operations. Therefore, a higher lever computer software is always necessary to convert integers and floats to meaningful quantities. Therefore, the SI conversion equations are given in the following subsections.

The software employed on the MAIUS-1 mission did include basic mathematics, therefore allowed to integrate the definitions in the hardware description files, thus allowing for a reduction of necessary documentation for the future missions.

C.2. MAIUS Chip Driver (UCCD)

C.2.1. Firmware description

Parameters - Write

`Memory Address:` 14 Bit Integer. The address of the memory element to write. The employed firmware enables 4095 memory blocks to store ramp command and Amplitude in each block. In case of the Chip Driver, odd addresses are used for channel B, even addresses for channel A. The first pair of addresses are executed after first upload for an indefinite time.

`Amplitude:` 26 Bit signed Integer. The interpretation of this value depends on the logical value of the associated `ramp command.`

`Ramp Command:` Boolean. It triggers the ramp function of the current drivers. If true, the corresponding value of `amplitude` is interpreted as a slope or a designated value to jump to.

`Tick-Trigger:` 4 Bit Integer. Determines the TBUS trigger line the circuit interprets as next command trigger. This trigger increments the addresses executed is incremented by 1.

`Reset-Trigger:` 4 Bit Integer. Determines the TBUS trigger line the circuit interprets as reset trigger. This trigger sets the addresses executed to 0 and 1.

`Safety-Trigger:` 4 Bit Integer. Determines the TBUS trigger line the circuit interprets as safety trigger. When high, this trigger disables the hardware output and resets the current addresses.

`Mode:` 8 Bit data word: Sets the execution mode of the current driver. Only two values are accepted:

- »`L=$4C`«: LOAD mode. Write commands to the memory are accepted. Tick Trigger is ignored. The first column of the address space is executed.
- »`R=$52`«: RUN mode. Write commands to the memory are ignored. Triggers are executed.

`Enable A/B:` 2 Booleans. Must be set high by bus command to enable hardware output. Can be disabled by bus command or by safety trigger.

Parameters - Read

`NTC:` 10 Bit Integer. The numerical value ϑ, representing the thermistor voltage measured by the ADC, to determine the temperature of the power board.

`Current A/B:` 10 Bit Integer. Numerical value γ, representing the current measured by the feedback loop, measured by the ADC.

`Battery A/B:` 10 Bit Integer: Numerical value ι, representing the battery voltage measured by the feedback loop, measured by the ADC.

SI conversion

`Amplitude:`

- `jump (ramp=false):`

$$A(I \in [-10\text{A}..10\text{A}]) = I \cdot \frac{2^{15}-1}{10} \tag{C.1}$$

- `ramp (ramp=true):` With the Gauge $G = 10\,\text{V}\,\text{A}^{-1}$ and the internal update frequency $\nu = 80\,\text{kHz}$, the slope is scaled to 16 Bit bipolar resolution and then shifted to a 8.17 Bit fixed point integer.

$$\mathcal{A}(\Delta I \in [-3875\text{A}\,\text{s}^{-1}..3875\text{A}\,\text{s}^{-1}]) = \frac{\Delta I}{G} \cdot \frac{2^{15}-1}{\nu} \cdot 2^{17} = \frac{\Delta I}{10} \cdot \frac{2^{15}-1}{10^5} \cdot 2^{17} \approx \Delta I \cdot 4294 \tag{C.2}$$

`NTC`: Assuming the Thermistor is chosen to be 10k at 25 °C, conversion to °C follows, using the parametrized equation A.8, with θ as numeric value of NTC.

$$\vartheta(\theta, \beta = 3570\text{K}, \vartheta_0 = 298.15\text{K}) = \frac{\beta}{\frac{\beta}{\vartheta_0} - \ln\left(\frac{2^{10}-1}{\theta} - 1\right)} - 273.15^\circ\text{C} \tag{C.3}$$

`Battery A/B`:

$$I(\gamma) = \frac{10 \cdot \gamma}{2^{10}-1} \cdot 3.3\text{A} \tag{C.4}$$

`Current A/B`:

$$V(\iota) = \frac{10 \cdot \iota}{2^{10}-1} \cdot 3.3\text{V} \tag{C.5}$$

TBUS communication mapping

Address (Hex) \ Bit no.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Memory Address[07..00]							
01	XX	XX	XX	XX	Memory Address[0B..08]			
02	Amplitude[07..00]							
03	Amplitude[0F..08]							
04	Amplitude[17..10]							
05	XX	XX	XX	XX	XX	XX	Ramp command	Amplitude[18]
06	Reset - Trigger[03..00]				Tick - Trigger[03..00]			
07	XX	XX	XX	XX	Safety - Trigger[03..00]			
08	Mode[07..00]							
09	XX	XX	XX	XX	XX	XX	Enable A	Enable B
0A	XX	XX	XX	XX	XX	XX	XX	Initialize DAC

TABLE C.1.: Input

Address (Hex) \ Bit no.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	NTC[00..07]							
01	XX	XX	XX	XX	XX	XX	NTC[09..08]	
02	Current A[00..07]							
03	XX	XX	XX	XX	XX	XX	Current A[09..08]	
04	Current B[00..07]							
05	XX	XX	XX	XX	XX	XX	Current B[09..08]	
06	Battery A[00..07]							
07	XX	XX	XX	XX	XX	XX	Battery A[09..08]	
08	Battery B[00..07]							
09	XX	XX	XX	XX	XX	XX	Battery B[09..08]	
FF	XX	XX	XX	Temperature OK	Status A	Status B	Read-Mode[1]	Read-Mode[0]

TABLE C.2.: Output

C.2.2. Chipcurrent2x10.card.xml

```xml
<?xml version="1.0" encoding="utf-8"?>
<Card name="ChipCurrent2x10">
    <!-- name should match filename, in case of conflict follow filename -->

    <IntegerParameter name="Next Command TRG,Trg_Nxt" defaultvalue="11" min="0" max="
        12" OnUnderflow="clip" OnOverflow="clip" abs="on" />
    <!-- Define trigger line for the Next command state. -->

    <IntegerParameter name="Command Reset TRG,Trg_Rst" defaultvalue="12" min="0" max="
        12" OnUnderflow="clip" OnOverflow="clip" abs="on" />
    <!-- Define trigger line for memory reset. Sets all output to zero after reset.-->

    <IntegerParameter name="Safety TRG, STRG" defaultvalue="10" min="0" max="12"
        OnWunderflow="clip" OnOverflow="clip" abs="on" />
    <IntegerParameter name="DRV_MODE,mode" defaultvalue="$4C" />
    <BooleanParameter name="EnableA" defaultvalue="0" />
```

```xml
    <BooleanParameter name="EnableB" defaultvalue="0" />

    <!-- Set Enable Bits for the analogue current drivers. If 'false', the drivers are not operational. -->

    <IntegerParameter name="Address, Addr" defaultvalue="0" min="0" max="4095" OnUnderflow="clip" OnOverflow="clip" abs="on" />
    <!-- Memory adress of the current state. For Integer n which is the column of the sequence, 2n represents the address of Channel A, (2n+1) the address of Channel B. -->


    <BooleanParameter name="Command" defaultvalue="false" />
    <!--  False=0=Jump
        True=1=Linear Ramp
        This parameter changes the interpretation of the Amplitude Parameter. Software should include a case seperation. -->

    <IntegerParameter name="Amplitude,Ampl" defaultvalue="16384" min="0" max="33554431"  OnUnderflow="clip" OnOverflow="clip" abs="on" />
        <!-- 2^25-1 = 33554431
        If Command=false then Amplitude is the amplitude to jump to. Only 16 bit unsigned integer.
        Bit conversion from SI: Ampl(I)=(I/10)*2**15   ; I=-10 to 10 A is accepted, current output only for I=0 to 10 A

        If Command=true then Amplitude is the ramp rate for a sweep. with 8.17 bit signed fixed point.
        Bit conversion from SI: Ampl(DeltaI)=(DeltaI/10)*2**52/(1e12)  , DeltaI=-4503 to 4503 A/s
        (the conversion could probably be done more elegantly with a bit shift.) -->

     <!--   Read-only parameters:
       (conversion to SI units is in software, not in XML) -->
    <IntegerParameter name="NTC"       defaultvalue="0" min="0" max="1023" OnUnderflow="clip" OnOverflow="clip" abs="on" />
    <!-- Read NTC Value, 10 Bit Int. unsigned.
    SI (°C) conversion: T(NTC)=3570*298,15/(3570+LN(((3,3/1024)*NTC*10000)/(3,3-(3,3/1024*NTC))/10000)*298,15)-273,15 -->

    <IntegerParameter name="Current A" defaultvalue="0" min="0" max="1023" OnUnderflow="clip" OnOverflow="clip" abs="on" />
    <IntegerParameter name="Current B" defaultvalue="0" min="0" max="1023" OnUnderflow="clip" OnOverflow="clip" abs="on" />

    <!-- Current Values, 10 Bit Int. unsigned.
    SI (A) conversion: I(CURRENT)=10*G*CURRENT/(1024)*3,3 (with gauge parameter G=1A/V by default if not stated otherwise in Stack.xml) -->

    <IntegerParameter name="Battery A" defaultvalue="0" min="0" max="1023" OnUnderflow="clip" OnOverflow="clip" abs="on" />
    <IntegerParameter name="Battery B" defaultvalue="0" min="0" max="1023" OnUnderflow="clip" OnOverflow="clip" abs="on" />
    <!-- Battery Voltages after fuse, 0 if fuse broken.
    SI (V) conversion: V(BATTERY)=10*BATTERY/(1024)-->

    <BooleanParameter name="StatA" defaultvalue="false" />
    <BooleanParameter name="StatB" defaultvalue="false" />
    <BooleanParameter name="TempOk" defaultvalue="false" />
    <IntegerParameter name="ReadMode" defaultvalue="0" min="0" max="3" OnUnderflow="clip" OnOverflow="clip" abs="on"  />


```

```
    <Register name="Set DAC Mem" PreferedMethod="Default" DefaultDuration="100ns">
        <BusPattern address="+0" direction="w" pattern="Addr[7],Addr[6],Addr[5],Addr[4],Addr[3],Addr[2],Addr[1],Addr[0]" />
        <BusPattern address="+1" direction="w" pattern="0,0,0,0,Addr[11],Addr[10],Addr[9],Addr[8]" />
        <BusPattern address="+2" direction="w" pattern="Ampl[7],Ampl[6],Ampl[5],Ampl[4],Ampl[3],Ampl[2],Ampl[1],Ampl[0]" />
        <BusPattern address="+3" direction="w" pattern="Ampl[15],Ampl[14],Ampl[13],Ampl[12],Ampl[11],Ampl[10],Ampl[9],Ampl[8]" />
        <BusPattern address="+4" direction="w" pattern="Ampl[23],Ampl[22],Ampl[21],Ampl[20],Ampl[19],Ampl[18],Ampl[17],Ampl[16]" />
        <BusPattern address="+5" direction="w" pattern="0,0,0,0,0,0,Command,Ampl[24]" />
    </Register>
    <!-- Set the States for the Sequence. Even addresses are for Channel A, odd addresses are Channel B. -->

    <Register name="Set TRG lines" PreferedMethod="Default" DefaultDuration="100ns">
        <BusPattern address="+6" direction="w" pattern="Trg_Rst[3],Trg_Rst[2],Trg_Rst[1],Trg_Rst[0],Trg_Nxt[3],Trg_Nxt[2],Trg_Nxt[1],Trg_Nxt[0]" />
        <BusPattern address="+7" direction="w" pattern="0,0,0,0,STRG[3],STRG[2],STRG[1],STRG[0]" />
    </Register>
    <!-- Set the TRG line addresses.-->

    <Register name="Set mode" DefaultDuration="100ns">
    <BusPattern address="+8" direction="w" pattern="mode[7],mode[6],mode[5],mode[4],mode[3],mode[2],mode[1],mode[0]" />
    </Register>
    <!-- Two interpreted modes: Load=L=$4C=01001100
                                Run=R=$52=01010010-->


    <Register name="Initialize" DefaultDuration="100ns">
    <BusPattern address="+9" direction="w" pattern="0,0,0,0,0,0,EnableA,EnableB" />
    <BusPattern address="+10" direction="w" pattern="0,0,0,0,0,0,0,1" />
    </Register>


    <!-- Enable/Disable the analogue outputs.-->

    <Register name="Get data" PreferedMethod="Default" DefaultDuration="100ns">
        <BusPattern address="+0" direction="r" pattern="NTC[7],NTC[6],NTC[5],NTC[4],NTC[3],NTC[2],NTC[1],NTC[0]" />
        <BusPattern address="+1" direction="r" pattern="0,0,0,0,0,0,NTC[9],NTC[8]" />
        <BusPattern address="+2" direction="r" pattern="Current A[7],Current A[6],Current A[5],Current A[4],Current A[3],Current A[2],Current A[1],Current A[0]" />
        <BusPattern address="+3" direction="r" pattern="0,0,0,0,0,0,Current A[9],Current A[8]" />
        <BusPattern address="+4" direction="r" pattern="Current B[7],Current B[6],Current B[5],Current B[4],Current B[3],Current B[2],Current B[1],Current B[0]" />
        <BusPattern address="+5" direction="r" pattern="0,0,0,0,0,0,Current B[9],Current B[8]"  />
        <BusPattern address="+6" direction="r" pattern="Battery A[7],Battery A[6],Battery A[5],Battery A[4],Battery A[3],Battery A[2],Battery A[1],Battery A[0]" />
        <BusPattern address="+7" direction="r" pattern="0,0,0,0,0,0,Battery A[9],Battery A[8]" />
        <BusPattern address="+8" direction="r" pattern="Battery B[7],Battery B[6],Battery B[5],Battery B[4],Battery B[3],Battery B[2],Battery B[1],Battery B[0]" />
```

```
        <BusPattern address="+9" direction="r" pattern="0,0,0,0,0,0,Battery B[9],
            Battery B[8]" />
        <BusPattern address="+15" direction="r" pattern="0,0,0,TempOk,StatA,StatB,
            ReadMode[1],ReadMode[0]" />
    </Register>
    <!-- Readout command for the Data.-->

</Card>
```

text/Chipcurrent2x10.card.xml

C.3. MAIUS Coil Driver

C.3.1. Firmware description

TBUS communication mapping

Bit no. Address (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Memory Address[00..07]							
01	XX	XX	XX	XX	Memory Address[0B..08]			
02	Amplitude[00..07]							
03	Amplitude[0F..08]							
04	Amplitude[17..10]							
05	XX	XX	XX	XX	XX	XX	Ramp-Command	Amplitude[18]
06	Reset - Trigger[03..00]				Tick - Trigger[03..00]			
07	XX	XX	XX	XX	Safety - Trigger[03..00]			
08	Mode[07..00]							
09	XX	XX	XX	XX	XX	XX	XX	Enable
0A	XX	XX	XX	XX	XX	XX	XX	Initialize DAC

TABLE C.3.: Input

Bit no. Address (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	NTC[00..07]							
01	XX	XX	XX	XX	XX	XX	NTC[09..08]	
02	Current[00..07]							
03	XX	XX	XX	XX	XX	XX	Current[09..08]	
04	Battery[00..07]							
05	XX	XX	XX	XX	XX	XX	Battery[09..08]	
FF	XX	XX	XX	Temperature OK	Status A	Status B	Read-Mode[1]	Read-Mode[0]

TABLE C.4.: Output

C.3.2. CoilCurrent1x5.card.xml

```
<?xml version="1.0" encoding="utf-8"?>
<Card name="CoilCurrent1x5">
    <!-- name should match filename, in case of conflict follow filename -->

    <IntegerParameter name="Next Command TRG,Trg_Nxt" defaultvalue="11" min="0" max="
        12" OnUnderflow="clip" OnOverflow="clip" abs="on" />
    <IntegerParameter name="Command Reset TRG,Trg_Rst" defaultvalue="12" min="0" max="
        12" OnUnderflow="clip" OnOverflow="clip" abs="on" />
    <IntegerParameter name="Safety TRG, STRG" defaultvalue="10" min="0" max="12"
        OnUnderflow="clip" OnOverflow="clip" abs="on" />
    <IntegerParameter name="Address, Addr" defaultvalue="0" min="0" max="4095"
        OnUnderflow="clip" OnOverflow="clip" abs="on" />
    <BooleanParameter name="Command" defaultvalue="false" />
     <!--    False=0=Jump
              True=1=Ramp  -->
    <IntegerParameter name="Amplitude,Ampl" defaultvalue="16383" min="0" max="33554431
        "  OnUnderflow="clip" OnOverflow="clip" abs="on" />
     <!--   2^25-1 = 33554431
    If Command=false then Amplitude is the amplitude to jump to. Only 16 bit unsigned
        integer.
    If Command=true then Amplitude is the ramp rate for a sweep. with 8.17 bit signed
        fixed point.-->

    <IntegerParameter name="DRV_MODE,mode" defaultvalue="$4C" />
    <BooleanParameter name="Enable" defaultvalue="0" />

    <!-- Read-only parameters:
    (convertion to SI units is in software, not in XML) -->
    <IntegerParameter name="NTC"       defaultvalue="0" min="0" max="1023"
        OnUnderflow="clip" OnOverflow="clip" abs="on" />
    <!--
    Read NTC Value, 10 Bit Int. unsigned.
    SI (°C) conversion: T(NTC)=3570*298,15/(3570+LN(((3,3/1024)*NTC*10000)
        /(3,3-(3,3/1024*NTC))/10000)*298,15)-273,15 -->

    <IntegerParameter name="Current" defaultvalue="0" min="0" max="1023"  OnUnderflow=
        "clip" OnOverflow="clip" abs="on" />


    <!-- Current Values, 10 Bit Int. unsigned.
    SI (A) conversion: I(CURRENT)=10*G*CURRENT/(1024)*3,3 (with gauge factor G=1A/V by
         default) -->

    <IntegerParameter name="Battery" defaultvalue="0" min="0" max="1023"  OnUnderflow=
        "clip" OnOverflow="clip" abs="on" />

    <!-- Battery Voltages after fuse, 0 if fuse broken.
    SI (V) conversion: V(BATTERY)=10*BATTERY/(1024)*3,3 -->

    <BooleanParameter name="StatA" defaultvalue="false" />
    <BooleanParameter name="StatB" defaultvalue="false" />
    <BooleanParameter name="TempOk" defaultvalue="false" />
    <IntegerParameter name="ReadMode" defaultvalue="0" min="0" max="3" OnUnderflow="
        clip" OnOverflow="clip" abs="on"  />
------------------------------------------------------

    <Register name="Set DAC Mem" PreferedMethod="Default" DefaultDuration="100ns">
        <BusPattern address="+0" direction="w" pattern="Addr[7],Addr[6],Addr[5],Addr
            [4],Addr[3],Addr[2],Addr[1],Addr[0]" />
        <BusPattern address="+1" direction="w" pattern="0,0,0,0,Addr[11],Addr[10],Addr
            [9],Addr[8]" />
```

```xml
        <BusPattern address="+2" direction="w" pattern="Ampl[7],Ampl[6],Ampl[5],Ampl[4],Ampl[3],Ampl[2],Ampl[1],Ampl[0]" />
        <BusPattern address="+3" direction="w" pattern="Ampl[15],Ampl[14],Ampl[13],Ampl[12],Ampl[11],Ampl[10],Ampl[9],Ampl[8]" />
        <BusPattern address="+4" direction="w" pattern="Ampl[23],Ampl[22],Ampl[21],Ampl[20],Ampl[19],Ampl[18],Ampl[17],Ampl[16]" />
        <BusPattern address="+5" direction="w" pattern="0,0,0,0,0,0,Command,Ampl[24]" />
    </Register>

    <Register name="Set TRG lines" PreferedMethod="Default" DefaultDuration="100ns">
        <BusPattern address="+6" direction="w" pattern="Trg_Rst[3],Trg_Rst[2],Trg_Rst[1],Trg_Rst[0],Trg_Nxt[3],Trg_Nxt[2],Trg_Nxt[1],Trg_Nxt[0]" />
        <BusPattern address="+7" direction="w" pattern="0,0,0,0,STRG[3],STRG[2],STRG[1],STRG[0]" />
    </Register>

    <Register name="Initialize" DefaultDuration="100ns">
        <BusPattern address="+9" direction="w" pattern="0,0,0,0,0,0,Enable" />
        <BusPattern address="+10" direction="w" pattern="0,0,0,0,0,0,0,1" />
    </Register>


    <Register name="Set mode" DefaultDuration="100ns">
        <BusPattern address="+8" direction="w" pattern="mode[7],mode[6],mode[5],mode[4],mode[3],mode[2],mode[1],mode[0]" />
    </Register>

    <Register name="Get data" PreferedMethod="Default" DefaultDuration="100ns">
        <BusPattern address="+0" direction="r" pattern="NTC[7],NTC[6],NTC[5],NTC[4],NTC[3],NTC[2],NTC[1],NTC[0]" />
        <BusPattern address="+1" direction="r" pattern="0,0,0,0,0,0,NTC[9],NTC[8]" />
        <BusPattern address="+2" direction="r" pattern="Current[7],Current[6],Current[5],Current[4],Current[3],Current[2],Current[1],Current[0]" />
        <BusPattern address="+3" direction="r" pattern="0,0,0,0,0,0,Current[9],Current[8]" />
        <BusPattern address="+4" direction="r" pattern="Battery[7],Battery[6],Battery[5],Battery[4],Battery[3],Battery[2],Battery[1],Battery[0]" />
        <BusPattern address="+5" direction="r" pattern="0,0,0,0,0,0,Battery[9],Battery[8]" />
        <BusPattern address="+15" direction="r" pattern="0,0,0,TempOk,StatA,StatB,ReadMode[1],ReadMode[0]" />
    </Register>

</Card>
```

text/CoilCurrent1x5.card.xml

Schematics

The actual schematics of the developed hard- and software on the MAIUS current sources are still in the evaluation phase of commercial exploitation. Therefore, it has been decided not to publish them in full detail in this thesis. However, for documentation purposes, the remaining electronics shall be included as a reference for further development.

D.1. MAIUS CHIP SAFETY

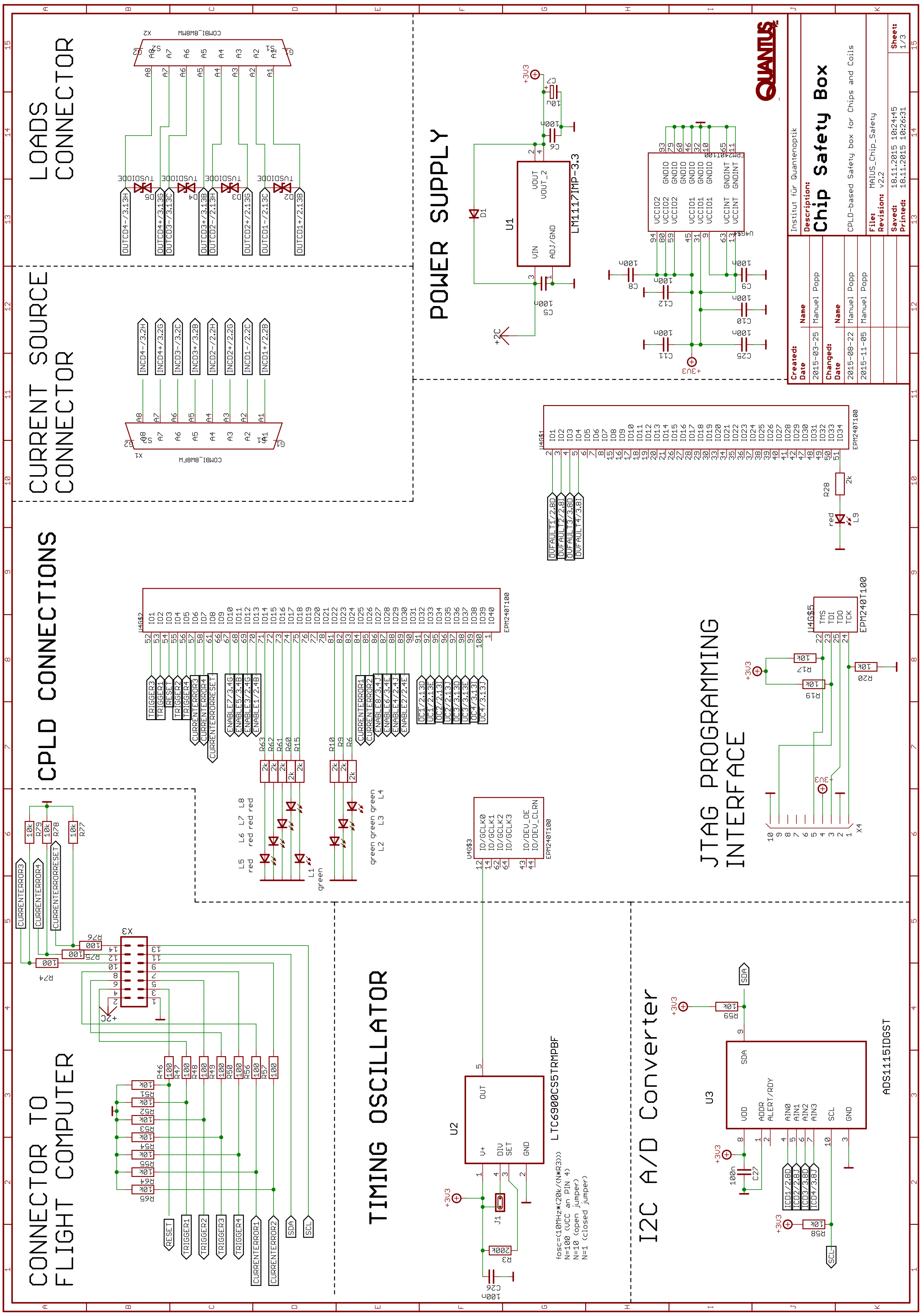

FIGURE D.1.: Schematic of the MAIUS-1 Chip Safety (1/3)

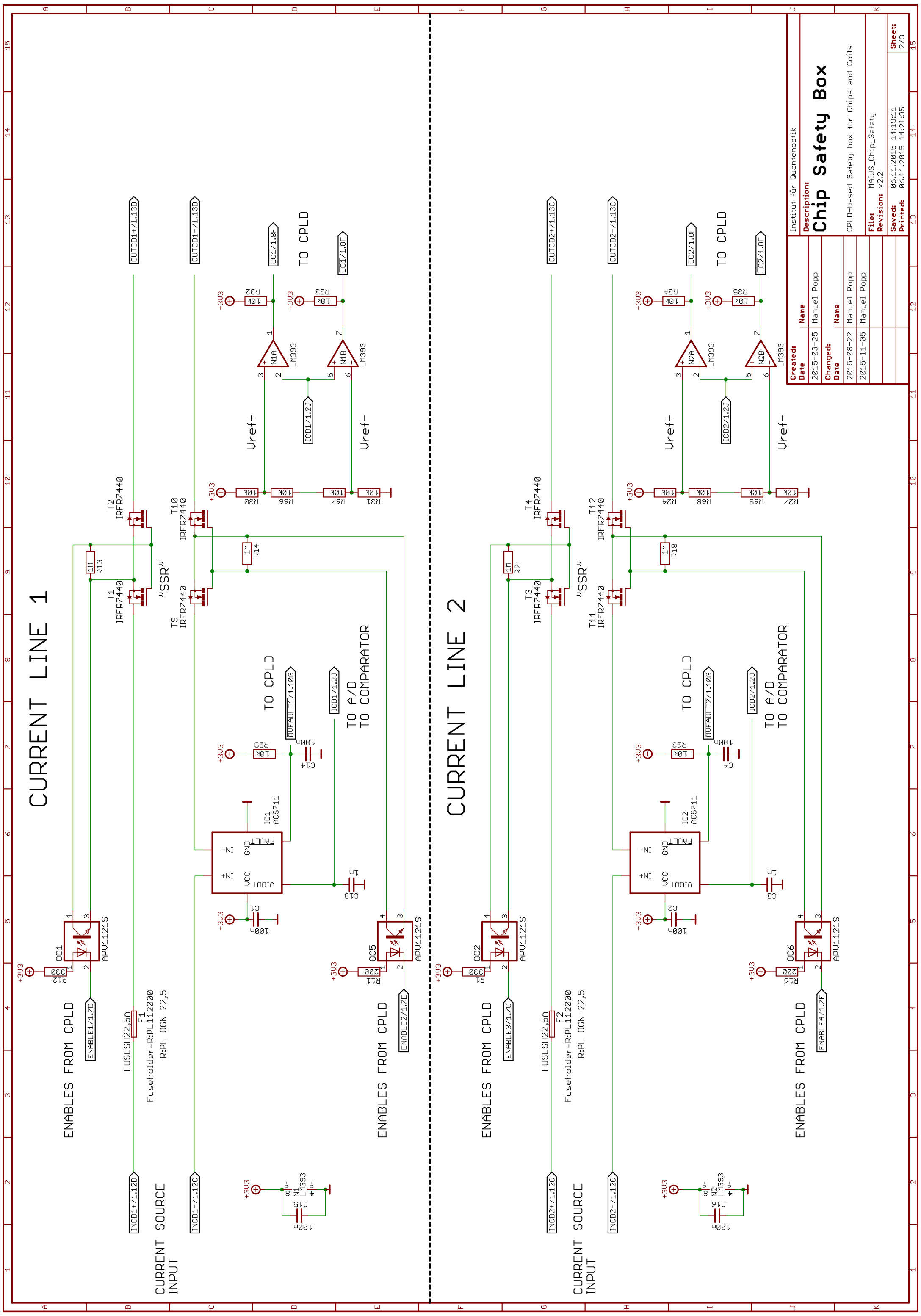

FIGURE D.2.: Schematic of the MAIUS-1 Chip Safety (2/3)

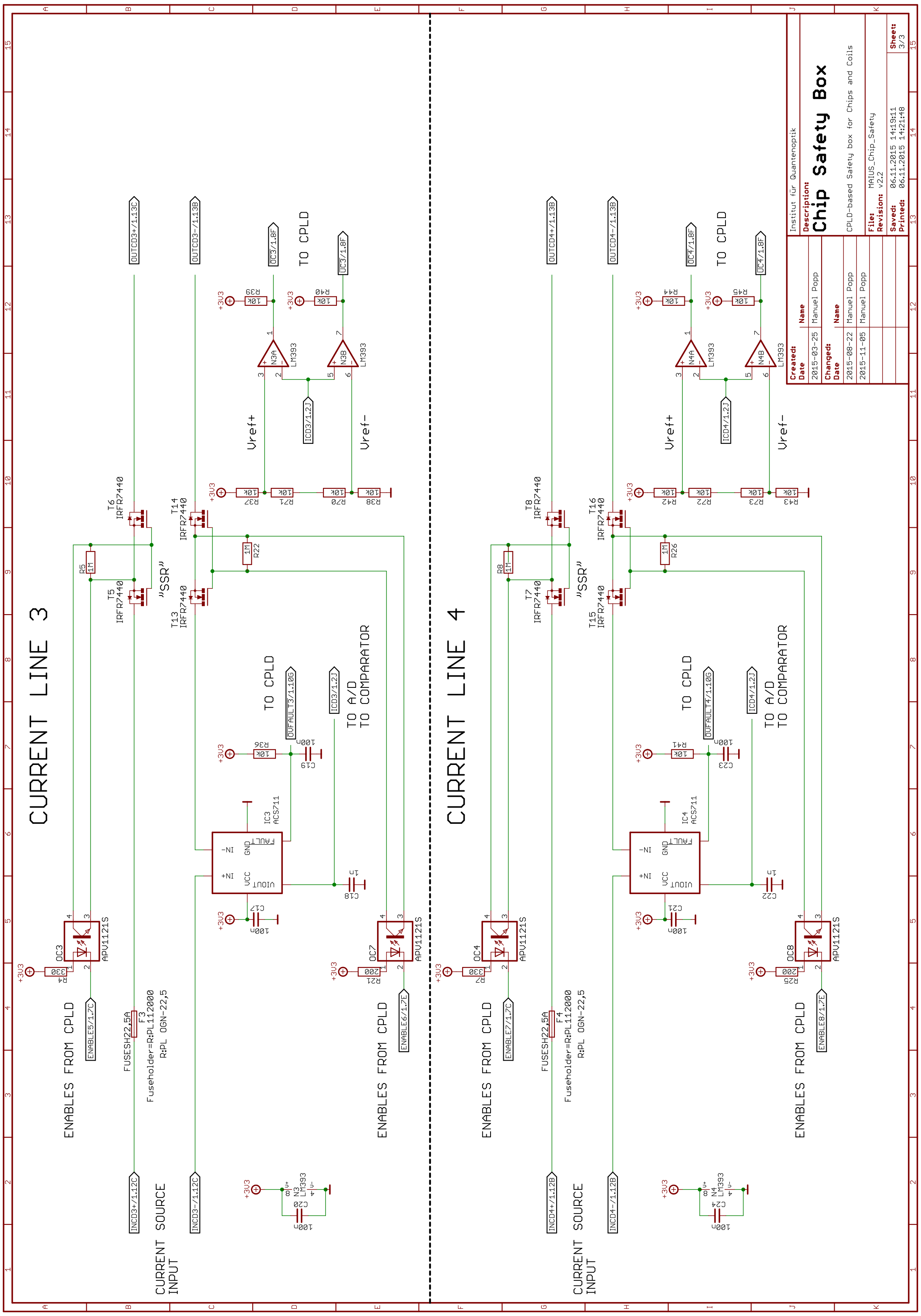

FIGURE D.3.: Schematic of the MAIUS-1 Chip Safety (3/3)

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