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Citation: Appl. Phys. Lett. **84**, 350 (2004);
View online: https://doi.org/10.1063/1.1641181
View Table of Contents: http://aip.scitation.org/toc/apl/84/3
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Roughness and stability of silicon on insulator surfaces

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(Received 13 August 2003; accepted 19 November 2003)

The feasibility of low temperature processes (below 800 °C) to obtain *in situ* atomically clean and smooth surfaces on (100) oriented silicon on insulator material (SOI) with negligible variation of the top Si film thickness was tested. These steps were characterized using low-energy electron diffraction and atomic force microscopy supplemented by conductivity measurements. The most promising method for obtaining atomically smooth and continuous SOI films is the evaporation of Si at 750 °C at a flux of 0.15 ML/min. For lower rates [113]-oriented pits are formed within the SOI layer. It turned out that mobile and volatile oxide formation at the Si/SiO_2 interface in these materials can occur already at temperatures below 1000° C, leading to the destruction of the buried oxide layer. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1641181]

The ongoing miniaturization of electronic devices not only makes the structures in electronic circuits smaller and smaller, it also has increased the influence of the properties of interfaces more and more. It has reached a level that enforces the geometric, chemical, and electronic definition and control of surfaces and interfaces on the atomic scale.

Most circuits today are based on Si technology. The use of silicon-on-insulator (SOI) material has become attractive in recent years, since a thin single crystalline film of Si is directly bonded to insulating SiO_2. It not only facilitates technology by reducing the number of necessary steps of processing, it also allows minimization of parasitic capacitance effects. From a physical point of view, ultrathin SOI surfaces are interesting because of their electronic structure. As investigated in detail with scanning tunneling microscopy,[1] already the lowest concentrations of missing surface Si atoms form characteristic metallic defect states, which lead to pinning of the Fermi level, i.e., for p-doped silicon ($\rho \approx 10\ \Omega$ cm) a Schottky barrier at the vacuum interface occurs. Therefore, thin topmost Si films (<100 nm, depending on the level of doping) are charge depleted.

As a general rule, a heterostructure like SOI with atomically sharp interfaces is metastable, both for entropical and for energetic reasons. Therefore, it is susceptible to high temperature treatment. As a consequence, it is difficult or even impossible to use the standard procedures in UHV for *in situ* removal of oxides and other contaminations by heating samples above 1000 °C. However, steps like these are necessary to obtain atomically smooth and clean Si surfaces of single crystalline Si, since successful processing of surfaces, e.g., in molecular beam epitaxy, depends on roughness on the atomic scale and on traces of contaminations. Therefore, *ex situ* cleaning steps are generally not sufficient. Inevitably, a process that desorbs SiO_2 at the vacuum interface must also make this species mobile at the inner interfaces, thus deteriorating or even destroying them.[2,3] Therefore, alternatives have to be tested.

A further problem seems to be the different degree of metastability from the various production schemes of SOI. Whereas the separation by implantated oxygen (SIMOX) technology forms the SOI structure by implantaion of high-energetic oxygen ions, the UNIBOND® flow process takes advantage of the special bonding of two adequately prepared Si wafers. Prior to bonding, both wafers are thermally oxidized. As judged from the published literature,[1,4] the interfaces obtained with the former process seem to be more stable.

In view of these problems, we tried to optimize *in situ* preparation methods for atomically smooth, contiguous, and clean Si films on SOI under UHV conditions and at temperatures below 800 °C. Characterization of surface morphology and of surface chemistry has been carried out using a combination of low-energy electron diffraction (LEED), Auger electron spectroscopy (AES), and *ex situ* atomic force microscopy (AFM). We show that the removal of SiO_2 by evaporation of silicon at elevated substrate temperatures[5–7] is a viable method also for extremely thin SOI films. It can be carried out at temperatures as low as 750 °C and at extremely small evaporation rates without producing etch pits. Thus, the thickness of the topmost Si layers changes only very little. As a second method, a combination of sputtering with Ar ions, annealing, and smoothing the surface by adsorption of molecular oxygen has been performed, which seems to be an alternative to the former method. Finally, the instability of the insulating film of the sandwich structure is demonstrated by high temperature treatments. For our samples produced with the UNIBOND® process we observed thermal stability of the buried oxide layer (BOX) only for substrate temperatures lower than 900 °C. This finding will be discussed in terms of suboxides (SiO_x, $0<x<2$) located at the Si/SiO_2 interface.

Our SOI samples had a 200-nm-thick Si film on top of the 400-nm-thick BOX film. Macroscopic conductivity measurements have been carried out *in situ* both along the SOI film and between film and bulk Si in order to check qualitatively the insulating properties of the BOX. Different preparation techniques have been tested using always SOI samples from the same wafer. After a high temperature treatment they were replaced in order to make the indiviual steps comparable.

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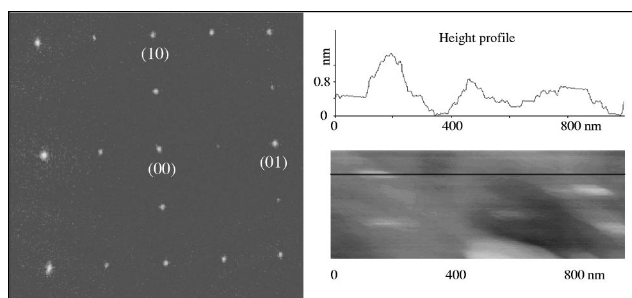

FIG. 1. LEED pattern (left) and AFM image (right, together with a height profile) of a SOI surface cleaned by Si evaporation at $T=750\,^\circ$C. Evaporation rate was 0.15 ML/min. The electron energy was 111 eV.

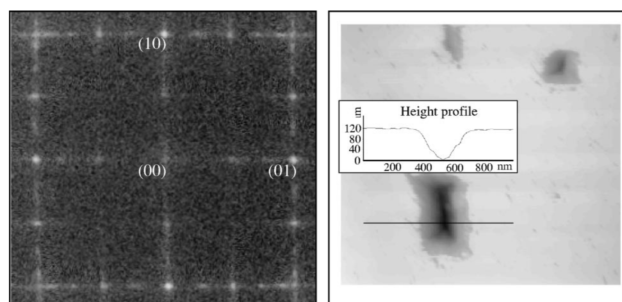

FIG. 2. Left: LEED pattern a SOI surface cleaned by Si evaporation at $T=750\,^\circ$C taken at an electron energy of 111 eV. Evaporation rate reduced to one half of that of Fig. 1. Right: AFM picture ($1.7\times1.7\ \mu$m^2) of a SOI surface with pits after sputtering/oxygen treatment. The depth is around 100 nm as can be seen in the line profile.

All manipulation steps of the SOI sample like evaporation, sputtering, heating, etc., were performed in an UHV chamber at a base pressure of 10^{-8} Pa. The UHV system was equipped with LEED, AES, and a quadrupole mass analyzer (QMA). Silicon was evaporated out of a graphite crucible heated by electron bombardment. The evaporation rate was monitored with a quarz microbalance. It was calibrated by calculating the change of frequency of the quarz microbalance with increasing film thickness assuming an ideal layer-by-layer growth. The cleanness of silicon and also of oxygen and argon for the purpose of smoothing and sputtering was checked by AES and with the QMA, respectively. The SOI sample was heated by direct current through the bulk material and the temperature was controlled by an infrared pyrometer. The sample temperature was carefully calibrated in advance using a Ni/NiCr thermocouple, which was directly attached to a dummy Si sample of the same size in place of the SOI samples on the sample holder. Thus, the uncertainty of the temperature reading could be reduced to $\pm5\,^\circ$C. The AFM (Park M5) and additional conductivity measurements have been done *ex situ*.

In a first step, we tried to remove the thin cap oxide, grown under ambient conditions, by evaporation of Si at temperatures below $800\,^\circ$C using the reaction: $SiO_2(ad)+Si(ad)\rightarrow SiO(gas)$, at a temperature and at evaporation rates as low as possible. According to a generally accepted model,[8] this process at the surface competes with the formation of Si monomers at the SiO_2/Si interface, which may be produced by Si diffusing through the oxide. This leads to an etching process also at the inner interface and formation of etch pits[5,9] with (111)- or (113)-oriented facets that turn out to be the most stable facets under this reaction. A smooth surface bare of oxygen can therefore only be achieved when the reaction of evaporated Si with SiO_2 at the vacuum interface is much faster than the reaction at the inner surface. This depends on evaporation rate and temperature, which controls diffusivities and rates of desorption. However, the Si evaporation rate of 1–1.5 Å/s at a temperature of $780\,^\circ$C suggested as an optimum in Ref. 6 would be much too high to control the Si layer thickness for ultrathin Si layers. We therefore lowered the temperature further. Best results with respect to an atomically smooth SOI film and a still intact BOX film were obtained for a substrate temperature of $750\,^\circ$C with a silicon flux of 0.15 ± 0.05 ML/min (0.003 Å/s). The surface morphology obtained after evaporation for 30 min is shown in Fig. 1 by corresponding LEED and AFM images. LEED shows the expected (2×1) reconstructed pattern of a clean Si(100) surface. From a quantitative LEED spot profile analysis at several scattering conditions we found an average terrace length of perfect (100)-oriented terraces larger than 400 Å. In addition, the vertical rms roughness, Δ, was determined to be around 1.5 Å, as concluded from a G(S)-analysis of the specular beam.[10] As seen from the right part of Fig. 1, AFM clearly shows a smooth and most notably continuous film of silicon. The native oxide layers have been removed completely, since AES shows only Si specific emission lines. The average rms roughness obtained by AFM (calculated from a $3.3\times3.3\ \mu$m^2 scan area) is 2.1 Å, in good agreement with LEED. After this treatment, the BOX layer turned out to be still intact, i.e., the resistance between Si layer and bulk silicon was still unmeasurably large ($\geqslant 50\ M\Omega$).

Indeed, the evaporation rate used in Fig. 1 turned out to be close to the lowest possible at the temperature of $750\,^\circ$C. The result of the same experiment with the evaporation rate only lowered by a factor of 2 at the same temperature is shown in Fig. 2. The LEED pattern shows, apart from the typical integer and half order diffraction spots also satellite spots, which shift their position as a function of electron energy. Plotting the positions of the satellite spots as a function of energy shows that they originate from (113)-facets on the surface, which form the side walls of etch pits, as shown by the AFM image.

As an alternative method for obtaining smooth SOI surfaces, also a combination of sputtering with Ar ions and smoothing the surface by subsequent dosing of molecular oxygen in the same elevated temperature range has been tested. In this case the native oxide was removed first by cycles of sputtering the SOI crystal ($E_{Ar^+}=600$ eV, $I=0.5\ \mu$A) and annealing at $750\,^\circ$C until no traces of oxygen were visible with AES. Right after the sputtering/annealing cycles only a broad (1×1) LEED structure with a typical half width [full width at half maximum (FWHM)] of 10% Brillouin Zone of the specular beam at an out-of-phase condition was observed. Nevertheless, heating the surface up to $750\,^\circ$C in an O_2 atmosphere of 2×10^{-6} Pa results also in a high quality Si(100) surface almost comparable to that shown in Fig. 1. However, pit formation with (113) orientation as a consequence of the smoothing effect by preferential oxidation and desorption of Si atoms at step sites cannot be avoided, as tested with AFM.

The experiments described earlier show how a Si surplus at the surface can be used to remove oxide layers from SOI

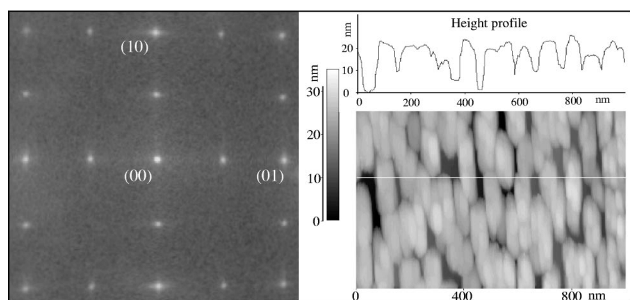

FIG. 3. LEED pattern (left, electron energy 82 eV) and AFM image (right) with a representative line scan of a SOI surface annealed to 1030 °C. The electron energy of 82 eV corresponds to an in-phase scattering condition.

surfaces leaving atomically smooth Si surfaces. The same reaction, however, must also take place at the Si/SiO_2 interface, where the bulk Si material provides a huge reservoir of Si atoms. Nevertheless, it seems that SOI in some cases can stand at least temperatures up to 1000 °C.[1] Even more, flash cycles have been used to remove the native oxide like for silicon. The findings on our samples are clearly at variance with these statements.

After heating SOI samples, that have first been carefully degassed at 800 °C, to temperatures between 1000 and 1030 °C for only 5 s at pressures below 10^{-7} Pa, LEED sees a brilliant (2×1) structure [see Fig. 3(a)] with both reconstruction domains, indicating complete removal of the surface oxide layer and a perfect SOI film, in agreement with Ref. 1. The average terrace length of (100)-oriented terraces is around 260 Å, as determined from the FWHM of the (00)-spot at an out-of-phase condition. Nevertheless, streaks around the diffraction spots are visible, indicating already a nonuniform surface. The finite resistance measured after this treatment between bulk and surface Si layer, however, shows that the BOX layer is obviously destroyed.

Ex situ AFM in contact mode shows that clusters 200 nm long and 40 nm wide have been formed (see right part of Fig. 3), most likely silicon clusters, that are consistent both with the measured terrace widths in LEED and with AES results. The finite size of the silicon clusters can be seen in the LEED pattern by the streaks around all diffraction spots. The elongated structure of the Si islands is most likely an electromigration effect, a consequence of heating the surface with direct current.

These experiments show that also at the inner Si/SiO_2 interface the formation of volatile SiO is a fast process at temperatures around 1000 °C, leading to complete destruction of the SOI structure. However, even at 900 K this process was observed. At this temperature only a broad (1×1) structure was found after several minutes of annealing that could not be improved by further annealing steps, indicating only a poor crystalline quality, most likely because of intermixing of Si and nonstoichiometric oxide species. More important, the resistance across the buried oxide film, measured at room temperature, decreased significantly already after the first few minutes of annealing from >50 to 0.6 MΩ, indicating the onset of the destructive etching process. In contrast, annealing at a temperature of 800 °C over many hours caused no measurable changes. Even after 15 h of heating the sample the resistance measured between the bulk Si and the SOI film was unmeasurably large $(\geqslant 50\ \mathrm{M}\Omega)$, i.e., temperatures of 800 °C should not be exceeded in long time annealing steps. Similiar etching processes below 1000 °C have been observed also by Ishikawa *et al.*[4] Interestingly, they used UNIBOND® SOI material, too.

The authors would like to thank Professor Dr. Latychev for many fruitful discussions during his stay in Hannover.

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