Analysis of ESD induced field coupling due to improper contact between PCB ground and metal housing.

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1 Abstract

Electrostatic Discharge (ESD) poses a significant challenge to the reliability of Devices Under Test (DUTs) within the automotive industry. ESD Power-On Tests are essential to assess how well DUTs can withstand real world ESD events. When designing a DUT for ESD immunity, designer must take care of 1. Direct Conduction: This involves ESD discharges flowing through DUT circuitry, which can potentially lead to permanent damage or performance deterioration. 2. Induced Field Coupling: ESD discharges generate electric and magnetic fields that can couple with nearby sensitive circuits, causing soft errors [1] by inducing voltage or current in these circuits[2]. This paper discusses the influence of Transient Electromagnetic (TEM) coupling on sensitive circuits, which can occur due to high-impulse surface currents generated by ESD events, resulting from improper contact between the Printed Circuit Board (PCB) ground and metal housing.

2 Introduction

ESD events produce high impulse currents through a series of intricate processes. When two materials come into contact and then separate, the triboelectric effect induces the transfer of electrons, leading to a build-up of static charge. This accumulated charge creates an electrostatic potential, seeking discharge to achieve equilibrium. As the potential difference reaches a critical level, it triggers the breakdown of air insulation, causing ionization and the formation of a conductive path. The subsequent arc discharge allows for the rapid flow of electrons, generating high impulse currents. These currents can propagate through electronic components, circuits, and other paths of least resistance, posing a significant threat to the integrity of sensitive devices.

The generation of electromagnetic fields during ESD events is a consequence of the rapid change in current associated with the discharge process. The intense and sudden flow of electrons creates time-varying electric and magnetic fields in the surrounding space. Maxwell's equations describe how the changing electric field induces a magnetic field, and vice versa, resulting in the emission of electromagnetic radiation. The emitted electromagnetic fields from ESD events contribute to electromagnetic interference (EMI), potentially affecting nearby electronic devices and systems. The strength and frequency spectrum of these fields depend on various factors, including the characteristics of the discharge, the geometry of the conductive paths, and the surrounding environment.

Understanding the mechanisms of high impulse current generation from ESD and its subsequent EMF effects is crucial for developing effective strategies to mitigate ESD-related risks. To mitigate the impact of high impulse currents from ESD, grounding the PCB with a casing is a crucial strategy. Grounding provides a low-resistance path for the discharge current to flow safely into the ground, preventing potential damage to sensitive electronic components.

By establishing a solid grounding system and employing protective casings, the mitigation strategy not only dissipates the high impulse currents effectively but also minimizes the associated EMI. However, improper or no contact between the PCB ground and the chassis, can create larger loops as the current returns to the source, increasing the potential for induced field coupling between the discharge path and adjacent conductors or components. This heightened inductive

coupling may result in undesirable effects, such as increased transient electromagnetic interference and signal integrity issues in the sensitive circuits.

This paper delves into the analysis of the root cause of EMI resulting from ESD impacting Serialized-Deserializer (SerDes) circuit. SerDes technology plays a crucial role in seamlessly integrating satellite cameras into Advanced Driver Assistance Systems (ADAS) alongside Power-over-Coax (PoC), which enables the transmission of both data and power through a single coaxial cable. However, the effectiveness of this integration is vulnerable to induced field coupling, given that it incorporates circuitry containing passive components like ferrites and inductors. These components, selected for their high permeability characteristics, are designed to reduce noise within the system. Paradoxically, their susceptibility to TEM fields raises potential concerns. During ESD events, these passive components, intended to mitigate noise, may inadvertently generate currents due to the influence of TEM fields. As a result, this interference can compromise the signal-to-noise ratio, leading to communication disruptions and triggering resets in satellite cameras. The integration of satellite cameras into ADAS, involving SerDes, PoC, and passive components, underscores the importance of addressing induced field coupling to ensure optimal system performance.

This study employs the Langer P1 mini burst E & H field pulse generator to thoroughly examine and pinpoint the root cause of the problem through the replication of the ESD scenario. The generator can generate a localized magnetic and electric field disturbance(as shown in figure 1 and 2) characterized by high intensity and a rapid rate of rise. This closely simulates the EMF conditions commonly encountered during actual ESD events, facilitating a comprehensive investigation and identification of the underlying issues.

This research explores the intricate interplay between ESD-induced impulse currents, electromagnetic field generation, and the practical application of grounding and casings to safeguard electronic systems from potential damage and performance degradation.

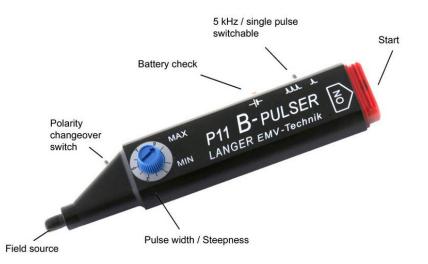


Figure 1: Langer P1 mini burst E & H field pulse generator

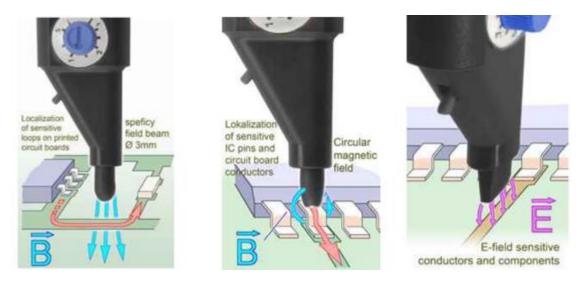


Figure 2: Localized magnetic and electric field genrated by P1 mini burst generator

3 ECU and Test set-up details

The top portion of the PCB is shielded by a die-cast metal housing featuring multiple grooves strategically designed to enhance PCB cooling. Conversely, the underside of the PCB is protected by a sheet metal baseplate. The PCB itself is rectangular in shape and encompasses a continuous PCB ground copper coating along its perimeter, which is connected to all PCB layers via vias. To ensure grounding, both the baseplate and the die-cast housing are affixed to the PCB ground through four metal screws located at the four corners of the PCB. This arrangement effectively sandwiches the PCB ground along its edges between the baseplate and the die-cast housing as shown in figure 1.

While the entire ECU casing maintains physical contact with the PCB ground along its edges, it's important to note that good RF grounding is primarily concentrated within the vicinity of the aforementioned screws.

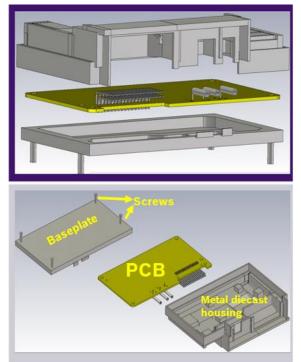


Figure 3: Exploded view of the ECU

The test setup adheres to ISO 10605 standards, wherein a T-shaped Horizontal Coupling Plane (HCP) is positioned atop the ground plane. To ensure isolation, a 50mm high Styrofoam spacer is positioned between the HCP and the ground plane, and the connection between them is established using screws. Notably, the DUT is not directly seated on the HCP but is instead positioned on a 2mm thick fiberglass substrate, providing an insulating layer. The DUT is connected to all requisite peripheral units and is situated on the insulating support. Furthermore, the wiring harness is arranged in a manner such that it parallels the HCP, spanning a length of approximately 1700mm as shown in figure 2.

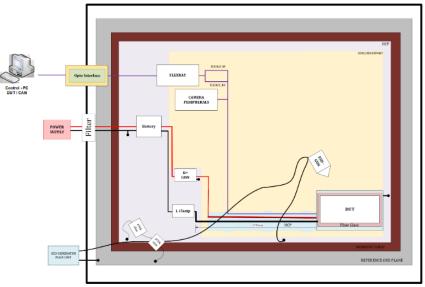


Figure 4: ESD Power-ON test setup.

Establishing a common ground connection for both the ESD gun and HCP is crucial for analyzing the trajectory of ESD current as it returns to the ESD generator. Understanding the effects of induced electric and magnetic fields resulting from ESD surface current is essential for diagnosing failures related to ESD effectively.

Assuming the metal casing acts as perfect shielding for the PCB, during an ESD event on the metal housing of the DUT, the ESD surface current travels along the casing's surface. It actively seeks a low-impedance pathway to ground without penetrating the casing's interior, minimizing the potential for interference with adjacent circuitry.

In this scenario, the surface current exhibits three primary return paths as shown in the figure 3, based on frequency content and their respective low impedance:

- 1. For relatively high-frequency spectrum content, surface currents tend to capacitively couple directly to the HCP beneath the ECU, separated by a fiberglass plate.
- 2. For other spectrum content, surface currents tend to capacitively couple directly to the nearby harness and then to the HCP.
- 3. Metal chassis is conductively connected to the PCB ground, and some surface currents tend to flow to the negative of the ECU, taking the path to ground.

In the third scenario, if there is a chance of inadequate RF connection between the PCB ground and chassis, the path for conducted ESD current becomes higher impedance and exhibits greater inductance. Consequently, the ESD current forms larger loops as it returns to the source, increasing the possibility for induced field coupling.

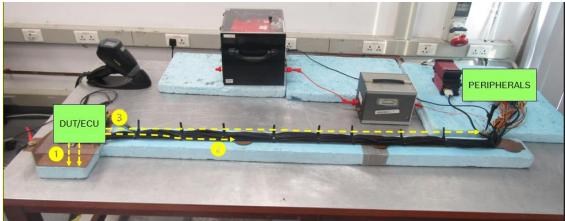


Figure 5: ESD current return paths

4 Failure and investigations

The ESD generator is configured to perform contact and air discharges at specified levels of +/-4kV, +/-8kV, +/-15kV, and +/-24kV, utilizing a 330pF and 330-ohm RC network as shown in figure 4 (a). The ESD discharge takes place on the baseplate, particularly in the vicinity of the camera connector region.

Shortly following the ESD discharge on the baseplate, Diagnostic Trouble Codes (DTCs) related to the camera system appeared in the fault memory as shown in figure 4 (b). Notably, the ECU failed to meet the fundamental discharge requirement of +/- 4kV.

Direct discharge Test	Discharge network	Level	Discharge type	Requirement	Achieved Status	Image: Symbolic Image: Sy		
Discharge on Metal housing of DUT	330pF/330ohm	+/-4 kV	Contact	No deviation allowed	NDTOR Camera Tean Sienal Invalid and Camera left Sienal Invalid DTCs Occurred during Injection of ESD			
		+/-8 kV	Contact	No deviation allowed			Description Status Camera era signal invalid false :: -: true : Camera left signal invalid false :: true : Camera AR signal invalid false :: true : Camera AR signal invalid false :: true : Park ECU no signal true :: true : Camera right calib missing true :: true : Camera rear calib missing true :: -: true : Camera rear calib missing true :: -: true : Camera fanct calib missing true :: -: true : Camera fanct calib missing true :: -: true :	
		+/-15 kV	Air	No deviation allowed				false : : : true : false : true : : false : : : true : false : true : : false : : : true : false : true : :
Discharge on Plastic housing of DUT	330pF/330ohm	+/-4 kV	Air	No deviation allowed	OK, No deviation observed			true : : : true : false : true : : true : : : true : false : true : : true : : : true : false : true : :
		+/-8 kV	Air	No deviation allowed	OK, No deviation observed			true : : -: true : false : true : : true : : -: true : false : true : : true : : -: true : false : true : : true : : : true : false : true : :
		+/-15 kV	Air	No deviation allowed	OK, No deviation observed			

Figure 6: (a) ESD test requirement and achieved status (b) DTCs observed in the fault memory

The appearance of DTCs in the fault memory can be attributed to the ESD discharge, which momentarily disrupted the GMSL (Gigabit Multimedia Serial Link) communication, leading to a temporary distortion in the video signal and causing a momentary freeze in the video feed. Importantly, ECU returned to normal operation once the ESD discharge ceased. The post-test measurements of resistance, inductance, and capacitance on each pin, relative to their respective return paths, fall within the acceptable range of +/-10% of pre-test values. Additionally, the post-test ECU current remains within the range of +/-10% of the pre-test value.

These results suggest that no permanent damage has occurred to the ECU due to ESD. Based on the observed failure pattern, it is evident that the EMF induced by the ESD current is coupling to nearby sensitive circuit, causing soft errors which leads to temporary disruption of the GMSL operation.

To replicate the surface current generated by the ESD discharge on the ECU's baseplate, the baseplate of the ECU was removed. A single strand of wire was positioned near the discharge area, and a controlled +/-2kV ESD was administered at one end of the wire, with the opposite end connected to the ground plane as shown in Fig 5. This procedure successfully reproduced the

observed failure and helped in identifying the specific portion of the circuit affected by the ESD fields.

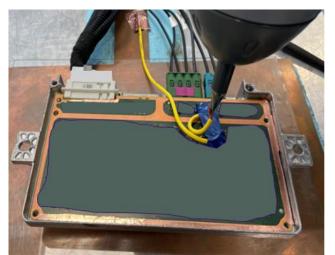


Figure 7: Replicating ESD induced surface currents to identify the specific circuit components affected

Having identified that the GMSL PoC circuit is affected by the ESD field, a subsequent examination delves into the coupling of the ESD field. Additionally, the entire section of the GMSL PoC circuit was shielded using copper tape, and the test was conducted. The implementation of this shielding prevented any occurrences of camera failure.

This outcome suggests that the induced EMF from the ESD current produces eddy currents on the shield's surface. These eddy currents, in response, generate magnetic fields that counteract and alleviate the EMF stemming from the ESD current. As a result, the EM field coupled to the GMSL circuit is significantly diminished[3].

Additionally, the P1 Mini Burst E and H Field Generator was utilized to intentionally apply localized E and H fields onto the GMSL circuit, as illustrated in Figure 6, while simultaneously monitoring the GMSL signal voltage.

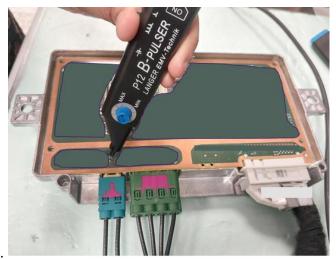
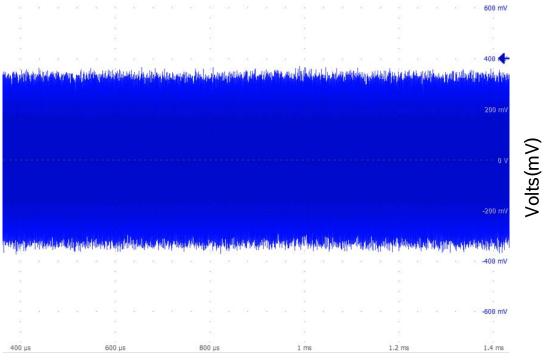


Figure 8: Inducing localized E&H field on GMSL PoC circuit using P1 Mini Burst Field generator.

The voltage plots obtained from these experiments provide clear confirmation that the induced EMF, which arise from the surface current generated by the ESD event, momentarily distort the

high-frequency, low-noise margin GMSL signal during the duration of the ESD event as shown in Figure 7.



Time (ms/us)

Figure 9: (a) GMSL forward channel communication during normal function

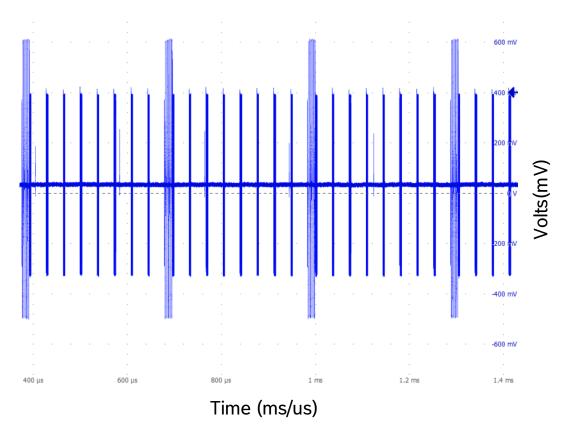


Figure 9: (b) Distorted forward channel when the ESD is discharge onto the PoC circuit.

5 Simulation

Simulation objective: The simulation involve subjecting the DUT to ESD pulses, allowing for an examination of the resultant noise characteristics. This emulation of a realistic ESD event facilitated a comprehensive understanding of the nature and extent of noise induced by such pulses. The findings from this simulation contribute to a deeper comprehension of the device's susceptibility to ESD-induced disturbances, thus informing the development of strategies to mitigate or protect against such effects in real-world applications.

To emulate the ESD pulse generator, the circuit illustrated in the figure 8 was employed. This configuration was chosen as the foundation for simulating ESD pulse characteristic[5]. To validate the fidelity of the simulated ESD pulse characteristics, injected the pulse onto the 2-ohm resistor and it was analyzed to ensure alignment with the anticipated characteristics outlined in the ESD pulse generator verification profile.

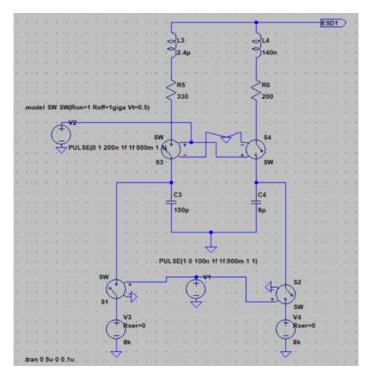


Figure 10: ESD pulse generator circuit

The test case was simulated using 3D electromagnetic software, Computer Simulation Technology (CST), employing a Frequency domain solver. This simulation involved modelling the housing, along with the PCB, with CAD simplifications applied to reduce complexity and solver time. The software employs advanced numerical techniques to model and analyze the transient responses of EMF as well as surface currents, the focus lies in capturing the dynamic behavior of electromagnetic phenomena during an ESD event.

The simulation allows to predict potential weak points in the system, evaluate the efficacy of grounding strategies, and optimize the design to mitigate the impact of ESD.

The spectral content of the ESD surface current on a metal chassis can vary based on the characteristics of the ESD event. However, in general terms, ESD events encompass a broad range of frequencies, spanning from very low frequencies up to radio frequencies. The spectrum of the ESD surface current typically exhibits a fast rise time and can include components in the kilohertz (kHz) to gigahertz (GHz) range. In order to closely mimic real-world conditions, the

simulation scenario was devised wherein the ESD modelled pulse was injected onto the chassis of the DUT as in the figure 9.

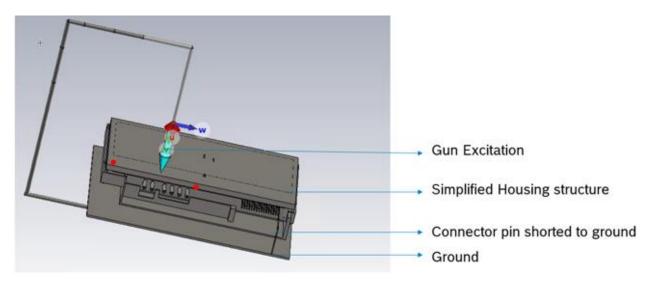


Figure 11: 3D ESD simulation setup

In Figure 10, the spectral content of the ESD discharge onto the DUT casing above the GMSL PoC circuit area is depicted. The plot highlights peak spectral content at 75MHz, 150MHz, 500MHz, and 1GHz. Examining Figure 11, the worst-case surface current is illustrated at the frequency of 75MHz, pinpointing the GMSL PoC circuit precisely within the high-impact zone, rendering it susceptible to EMF.

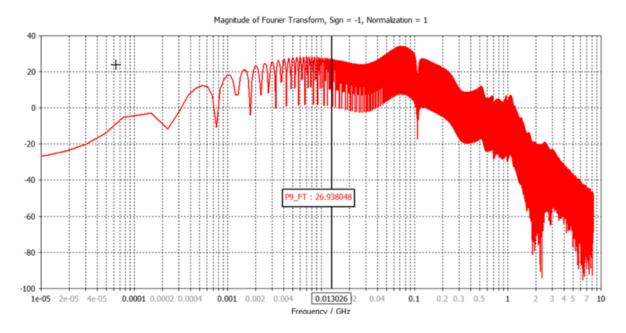


Figure 12: Spectral content of the ESD discharged on DUT chassis

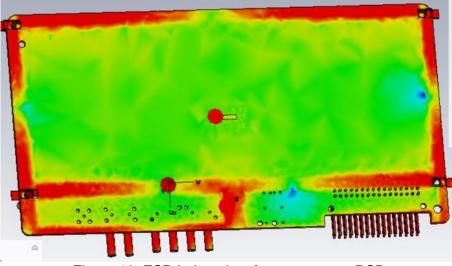


Figure 13: ESD induced surface current on PCB

6 Inference from investigations

The investigation and simulation results reveal that despite the PCB featuring a continuous ground coating along its perimeter, maintaining physical contact with the die-cast housing and baseplate along its edges as shown in Figure 1, effective RF grounding is predominantly concentrated near the screw locations only. Consequently, during an ESD event, the ESD current perceives only the corners of the DUT as low-impedance ground, owing to the maximum contact achieved through screwing. This leads to the formation of high-impulse surface currents in these areas. This results in the generation of magnetic flux, which in turn impacts sensitive nearby circuits. Key takeaways:

- Components incorporating ferrite composites, such as SMD ferrites and inductors, intercept the flux induced by ESD and introduce it into the circuit. To mitigate adverse effects, position these components away from corners of the PCB or regions where contact between the enclosure and PCB ground is poor.
- To prevent ESD-induced field coupling, ensure a solid connection between the PCB ground and the housing. EMC gaskets can be employed to achieve robust contact and enhance protection.

7 Conclusion

This paper analyses the temporary distortion of GMSL signals by induced E&H fields during ESD event, attributed to poor RF ground contact between PCB ground and metal housing. The test case was successfully simulated in the CST 3D solver, and the measurements align closely with the simulation results, confirming the validity and accuracy of the study's findings. To enhance ESD immunity, EMC designers are advised to establish a robust electrical connection between the PCB ground and metal chassis. These findings also offer valuable insights for designing and routing high-frequency sensitive circuits with improved ESD immunity.

8 Future Scope

Response of high-permeability ferrite composite components to magnetic fields induced by ESD.

Literature

- Zelig, P. Mahesgwari und D J. Pommerenke," Measurement Methodology for Field- Coupled Soft Errors Induced By Electrostatic Discharge ", IEEE Transactions on Electromagnetic Compatibility, vol. 58, no. 3, pp. 701-708, June, 2016.
- [2] J-S.Lee, D.Pommerenke, J.Lim und B.Seol ", ESD field coupling study in relation with PCB GND and metal chassis ", International Zurich Symposium on Electromagnetic Compatibility, pp. 153-156, Jan, 2009.
- [3] M.Cui, M.Wei und X.Chen, "Testing of material Shielding effectiveness against electromagnetic pulse", Cross Strait Quad-Regional Radio Science and Wireless Technology Conference, pp. 431-434, Jul, 2013.
- [4] Z.Peng et al., "Characterization and Modeling of Commercial ICs for System-Efficient ESD Design", IEEE Transactions on electromagnetic compatibility, 2022, pp.1802-1811.
- [5] Pavlos K. Katsivelis, Georgios P. Fotis, Ioannis F. Gonos, Tryfon G. Koussiouris and Ioannis A. Stathopulos, "Electrostatic Discharge Current Linear Approach and Circuit Design Method," Energies, vol. 3, no. 11, pp. 1728-1740, 2010.