Design and Evaluation of a Hardware System for Online Signal Processing within Mobile Brain-Computer Interfaces

Von der Fakultät für Elektrotechnik und Informatik
der Gottfried Wilhelm Leibniz Universität Hannover
zur Erlangung des akademischen Grades
Doktor-Ingenieur
Dr.-Ing.
genehmigte Dissertation von

Dipl.-Ing. Marc-Nils Wahalla

geboren am 31.12.1986
in Hannover, Deutschland

2024

Referent: Prof. Dr.-Ing. Holger Blume
Korreferent: Prof. Dr.-Ing. Stefan Zimmermann
Fachgutachter: Prof. Dr. Stefan Debener

Tag der Promotion: 12. Oktober 2023

Acknowledgments

Hannover, 07. Februar 2024   Marc-Nils Wahalla

Kurzfassung

Brain-Computer Interfaces (BCIs) sind innovative Systeme, die eine direkte Kommunikation zwischen dem Gehirn und externen Geräten ermöglichen. Diese Schnittstellen haben sich zu einer transformativen Lösung nicht nur für Menschen mit neurologischen Verletzungen entwickelt, sondern auch für ein breiteres Spektrum von Menschen, das sowohl medizinische als auch nicht-medizinische Anwendungen umfasst. In der Vergangenheit hat die Herausforderung, dass neurologische Verletzungen nach einer anfänglichen Erholungsphase statisch bleiben, die Forscher dazu veranlasst, innovative Wege zu beschreiten. Seit den 1970er Jahren stehen BCIs an vorderster Front dieser Bemühungen. Mit den Fortschritten in der Forschung haben sich die BCI-Anwendungen erweitert und zeigen ein großes Potenzial für eine Vielzahl von Anwendungen, auch für weniger stark eingeschränkte (zum Beispiel im Kontext von Hörelektronik) sowie völlig gesunde Menschen (zum Beispiel in der Unterhaltungsindustrie). Die Zukunft der BCI-Forschung hängt jedoch auch von der Verfügbarkeit zuverlässiger BCI-Hardware ab, die den Einsatz in der realen Welt gewährleistet.

Das im Rahmen dieser Arbeit konzipierte und implementierte CereBridge-System stellt einen bedeutenden Fortschritt in der Brain-Computer-Interface-Technologie dar, da es die gesamte Hardware zur Erfassung und Verarbeitung von EEG-Signalen in ein mobiles System integriert. Die Architektur der Verarbeitungshardware basiert auf einem FPGA mit einem ARM Cortex-M3 innerhalb eines heterogenen ICs, was Flexibilität und Effizienz bei der EEG-Signalverarbeitung gewährleistet. Der modulare Aufbau des Systems, bestehend aus drei einzelnen Boards, gewährleistet die Anpassbarkeit an unterschiedliche Anforderungen. Das komplette System wird an der Kopfhaut befestigt, kann autonom arbeiten, benötigt keine externe Interaktion und wiegt einschließlich der 16-Kanal-EEG-Sensoren nur ca. 56 g. Der Fokus liegt auf voller Mobilität.

Das vorgeschlagene anpassbare Datenflusskonzept erleichtert die Untersuchung und nahtlose Integration von Algorithmen und erhöht die Flexibilität des Systems. Dies wird auch durch die Möglichkeit unterstrichen, verschiedene Algorithmen auf EEG-Daten anzuwenden, um unterschiedliche Anwendungsziele zu erreichen. High-Level Synthesis (HLS) wurde verwendet, um die Algorithmen auf das FPGA zu portieren, was den Algorithmenentwicklungsprozess beschleunigt und eine schnelle Implementierung von Algorithmusvarianten ermöglicht. Evaluierungen haben gezeigt, dass das CereBridge-System in der Lage ist, die gesamte Signalverarbeitungskette zu integrieren, die für verschiedene BCI-Anwendungen erforderlich ist. Darüber hinaus kann es mit einer Batterie von mehr als 31 Stunden Dauerbetrieb betrieben werden, was es zu einer praktikablen Lösung für mobile Langzeit-EEG-Aufzeichnungen und reale BCI-Studien macht.

Im Vergleich zu bestehenden Forschungsplattformen bietet das CereBridge-System eine bisher unerreichte Leistungsfähigkeit und Ausstattung für ein mobiles BCI. Es erfüllt nicht nur die relevanten Anforderungen an ein mobiles BCI-System, sondern ebnet auch den Weg für eine schnelle Übertragung von Algorithmen aus dem Labor in reale Anwendungen. Im Wesentlichen liefert diese Arbeit einen umfassenden Entwurf für die Entwicklung und Implementierung eines hochmodernen mobilen EEG-basierten BCI-Systems und setzt damit einen neuen Standard für BCI-Hardware, die in der Praxis eingesetzt werden kann.

Schlagwörter — Brain-Computer Interface (BCI), Elektroenzephalografie (EEG), Mobiles Hardware System, Digitale Signalverarbeitung, Field-Programmable Gate Array (FPGA)

Abstract

Brain-Computer Interfaces (BCIs) are innovative systems that enable direct communication between the brain and external devices. These interfaces have emerged as a transformative solution not only for individuals with neurological injuries, but also for a broader range of individuals, encompassing both medical and non-medical applications. Historically, the challenge of neurological injury being static after an initial recovery phase has driven researchers to explore innovative avenues. Since the 1970s, BCIs have been at one forefront of these efforts. As research has progressed, BCI applications have expanded, showing potential in a wide range of applications, including those for less severely disabled (e.g. in the context of hearing aids) and completely healthy individuals (e.g. entertainment industry). However, the future of BCI research also depends on the availability of reliable BCI hardware to ensure real-world application.

The CereBridge system designed and implemented in this work represents a significant leap forward in brain-computer interface technology by integrating all EEG signal acquisition and processing hardware into a mobile system. The processing hardware architecture is centered around an FPGA with an ARM Cortex-M3 within a heterogeneous IC, ensuring flexibility and efficiency in EEG signal processing. The modular design of the system, consisting of three individual boards, ensures adaptability to different requirements. With a focus on full mobility, the complete system is mounted on the scalp, can operate autonomously, requires no external interaction, and weighs approximately 56 g, including 16 channel EEG sensors.

The proposed customizable dataflow concept facilitates the exploration and seamless integration of algorithms, increasing the flexibility of the system. This is further underscored by the ability to apply different algorithms to recorded EEG data to meet different application goals. High-Level Synthesis (HLS) was used to port algorithms to the FPGA, accelerating the algorithm development process and facilitating rapid implementation of algorithm variants. Evaluations have shown that the CereBridge system is capable of integrating the complete signal processing chain required for various BCI applications. Furthermore, it can operate continuously for more than 31 hours with a 1800 mA h battery, making it a viable solution for long-term mobile EEG recording and real-world BCI studies.

Compared to existing research platforms, the CereBridge system offers unprecedented performance and features for a mobile BCI. It not only meets the relevant requirements for a mobile BCI system, but also paves the way for the rapid transition of algorithms from the laboratory to real-world applications. In essence, this work provides a comprehensive blueprint for the development and implementation of a state-of-the-art mobile EEG-based BCI system, setting a new benchmark in BCI hardware for real-world applicability.

key words — Brain-Computer Interface (BCI), electroencephalography (EEG), mobile hardware system, digital signal processing, Field-Programmable Gate Array (FPGA)

Contents

List of Acronyms

ADC	Analog-to-Digital-Converter
APB	Advanced Peripheral Bus
ASIC	Application-Specific Integrated Circuit
ASIP	Application-Specific Instruction-Set Processor
BCI	Brain-Computer Interface
BLE	Bluetooth Low Energy
BMI	Brain-Machine Interface
BOM	Bill Of Materials
BSS	Blind Source Separation
CCA	Canonical Correlation Analysis
DAC	Digital-to-Analog-Converter
DIT	Decimation In Time
DDR	Double Data Rate
DSP	Digital Signal Processor
EEG	Electroencephalography
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electromagnetic Interference
EOG	Electrooculography
EP	Evoked Potential
ERP	Event-Related Potential
FF	Flip-Flop
FFT	Fast Fourier Transformation

FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
GPP	General Purpose Processor
GPIO	General-Purpose Input/Output
HDL	Hardware Description Language
HLS	High-Level Synthesis
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
ICA	Independent Component Analysis
JTAG	Joint Test Action Group
LDO	Low-Dropout Regulator
LE	Logic Element
LED	Light-Emitting Diode
LPDDR	Low-Power Double Data Rate
LUT	Lookup Table
MAC	Multiply-Accumulate
MII	Media-Independent Interface
MSE	Mean Square Error
MSS	Microcontroller Subsystem
NN	Neural Network
NVM	Non-Volatile Memory
PC	Personal Computer
PCA	Principal Component Analysis
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PMIC	Power Management Integrated Circuit
PSD	Power Spectral Density
RAM	Random Access Memory
RTC	Real Time Counter
RTL	Register-Transfer Level
SCP	Slow Cortical Potential
SDRAM	Synchronous Dynamic Random-Access Memory
SiP	System-in-Package
SNR	Signal-to-Noise Ratio
SoC	System on a Chip
SPI	Serial Peripheral Interface

SRAM	Static Random-Access Memory
SMR	Sensorimotor Rhythm
SSVEP	Steady State Visually Evoked Potential
THT	Through-Hole Technology
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
VHDL	Very High Speed Integrated Circuit Hardware Description Language
WLAN	Wireless Local Area Network

Introduction

Historically, human neurological injury has been considered static after an initial period of recovery [Kru16]. In this context, the quest to improve the quality of life for people with neurological injuries such as stroke, spinal cord injury or traumatic brain injury has been paramount. Researchers are working on multiple fronts to restore the nervous system and mitigate neurological deficits.

Dating back to the 1970s [Kaw21], neuroengineers have pioneered the development of Brain-Computer Interfaces (BCIs) designed to bypass lesions and restore functionality. These BCIs record and interpret brain activity to communicate with external devices. They can improve physical, mental, and social well-being, in line with the World Health Organization's definition of health [Fry22]. Beyond physical or biological markers, BCIs can have a profound impact on a patient's quality of life, especially when integrated with personal computing.
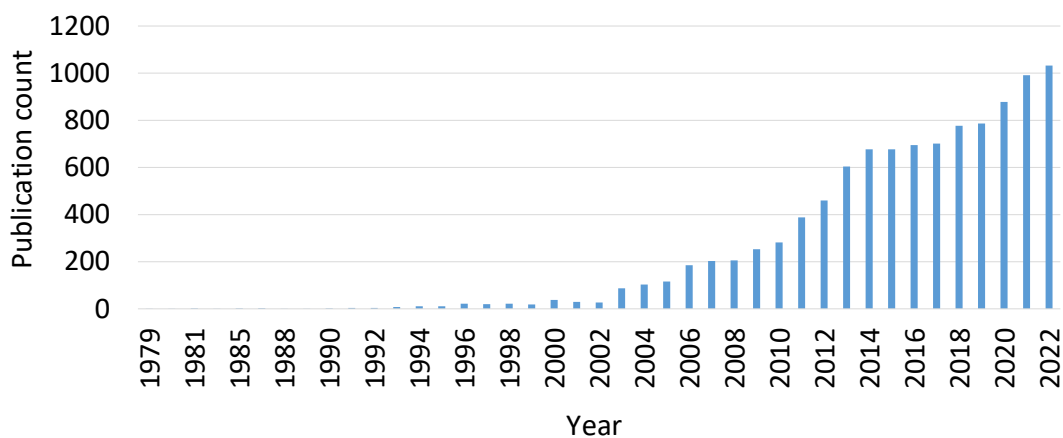
Figure 1.1: *Publications sorted by year until 2022 from results at Pubmed with search term "Brain-Computer Interface"*

Figure 1.2: *The envisioned future BCI system according to [Bel21]. This embedded head-mounted platform is designed to acquire Electroencephalography (EEG) signals, process and analyze brain activity, and send a decision based on the results to an application.*

A major milestone was reached in 1988 with the first experimental demonstration that ensembles of cortical neurons could directly control a robotic manipulator [Boz88] Since then, there has been a surge in BCI research publications, indicating growing interest and progress in the field (see Figure 1.1).

BCIs were originally envisioned as therapeutic tools for patients with severe disabilities, including ALS, spinal cord injury, and cerebral palsy. As the technology advances, BCIs also show promise for amputees and may expand to applications such as prosthetic control, speech restoration, and locomotion [Leb06]. With increasing research interest and results, more ideas for applications have emerged and are no longer limited on people with severe disabilities [Nic12].

The path of BCI research and development is highly interdisciplinary. A major challenge on which the future success of BCI research depends is the development of reliable BCI hardware to ensure real-world applicability, as described in [Shi12]. According to the authors, this hardware must be portable, safe, comfortable, and independent of the environment.

1.1. Objectives

In [Bel21] different approaches for embedded BCI platforms are reviewed. In many cases, although the corresponding brain activity signals are recorded on mobile hardware, the processing is separated and performed on stationary or bulky hardware. For this reason, the authors outline a future desired BCI platform that includes all necessary signal processing steps, from signal acquisition to complete processing and connection of external devices, on a mobile, head-mounted system. The preliminary concept of this envisioned system is shown in Figure 1.2.

To support research on applications and algorithms for BCIs, methods and features for the development of a dedicated mobile BCI platform will be explored. For ease of use and to enable meaningful use in a wide range of applications, this platform will process brain activity based on non-invasive EEG signals. In addition to mobility and sufficient processing capacity, high flexibility should also be in the foreground. The platform should be able to apply a variety of algorithms to the recorded EEG data and support different application goals.

In the context of this thesis, all necessary steps for the realization of such a fully mobile BCI will be discussed. Several research questions arise in this context:

- How should a suitable system concept be designed in order to achieve the best possible performance and at the same time a high degree of flexibility?

- What hardware architecture is suitable for the efficient implementation of different algorithms and what hardware resources are required?

- Which additional features and interfaces are desirable to satisfy most possible applications?

- What are the features, characteristics and limitations of such a system?

The answers to these questions are the main goals of this thesis. On the basis of a developed mobile EEG-based BCI system, the so-called CereBridge system, the individual areas are discussed and evaluated. In the systematic description of the design and implementation of the platform, corresponding trade-offs in the individual development steps are also discussed.

1.2. Structure of this Work

The thesis is structured as follows: Chapter 2 provides an overview of the characteristics of EEG signals, the current state of research on BCIs, and approaches to mobile BCI hardware. Chapter 3 describes the design space of hardware architectures for digital signal processing, with a special focus on Field Programmable Gate Arrays (FPGAs), which are used in the context of this thesis. It also reviews several published implementations of BCI-related algorithms on FPGA platforms. Subsequently, in Chapter 4, a concept for the realization of a fully mobile BCI platform is elaborated. The requirements for such a system are discussed, key components are identified and selected, and a possible implementation is described. Based on this, a suitable concept for data handling and processing on the platform is proposed in Chapter 5, which aims at supporting and extending the flexibility of the hardware. In this context, possible application scenarios of the system are given and some case study implementations of EEG processing algorithms on the platform are presented. These are used in Chapter 6, along with algorithm-independent measurements of power and timing specifications, to evaluate the CereBridge system. A discussion of the results and a classification and comparison with existing BCI hardware implementations conclude this chapter. A summary of this work follows in Chapter 7.

Fundamentals of Current Brain-Computer Interface Research

A BCI, sometimes called Brain-Machine Interface (BMI), establishes a direct communication path between the brain and external devices. The purpose is to bypass the traditional route of brain output through the peripheral nervous system and muscles [Tan10]. This possibility can be exploited in novel methods and applications in a wide range of fields, e.g. neurorehabilitation, treatment of neurological diseases and within the entertainment industry. The emerging field of BCI research is interdisciplinary at the interface of neuroscience, psychology, engineering, and computer science [Wol02].

It should be noted that in general a BCI can theoretically function as a bidirectional interface, i.e. information or stimuli can also be delivered to the brain from the outside. A common application is deep brain stimulation (DBS), which uses implanted electrodes to deliver specific patterns of electrical impulses to the basal ganglia. This method is used, for example, in Parkinson's patients to reduce tremors as much as possible [Wic11]. In the context of this thesis, however, methods that use the brain as the signal source for a BCI will be focused explicitly.

The signal flow of such a typical BCI system can be divided into the following four steps: signal acquisition, feature extraction, classification and application interface (see Figure 2.1).
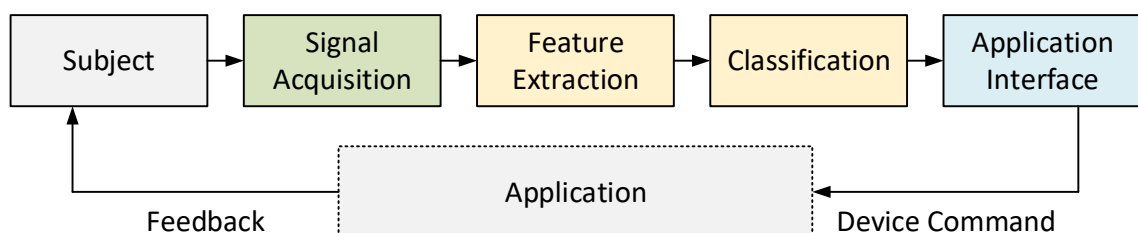
Figure 2.1: *Typical signal flow stages of a BCI system*

In the first step, brain signals are acquired from a subject using either invasive or non-invasive methods. This includes appropriate digitization of the captured signals to enable digital signal processing. Then, noise and artifacts will be removed from the signal and specific features corresponding to particular brain states or tasks can be extracted. Finally, the extracted features are classified to generate a control command for external devices, such as a robotic arm [Bha14]. The subject's perception of the application, e.g., visual or auditory, establishes a feedback path and completes the overall system into a closed loop.

This subdivision of a BCI signal flow is used here to outline the structure of this chapter. The recording of brain signals is covered in 2.1. Available sensing methods are briefly described before focusing explicitly on EEG, its signal characteristics and its sensor variants. In 2.2, different signal processing algorithms in the context of EEG-based BCIs are discussed, as well as some published hardware implementations of these algorithms. Some concrete applications of such a signal processing chain used to control external devices are presented in 2.3. The final Section 2.4 reviews current BCI-related mobile hardware for EEG signal acquisition and processing.

2.1. Brain Activity Signal Acquisition

This section describes signal recording, more specifically the measurement of brain activity. After an overview of possible methods, the EEG signals that are in the focus of this work as well as the required sensor technology will be described in more detail. The methods available for recording brain activity can be divided into two categories: invasive and non-invasive. This distinction is based on whether or not the method requires invasive surgery.

Invasive Brain Sensing Methods

Invasive BCIs involve the implantation of electrodes in or on the brain. These generally provide much higher spatial resolution and less artifactual measurement signals compared to non-invasive methods. However, the neurosurgical procedures required pose several risks and challenges, such as the risk of infection and the long-term stability of the implanted device.

A distinction within this class of brain sensing methods is the depth of implantation, as depicted in Figure 2.2. Electrocorticography (ECoG), for example, is applied to the surface of the brain and measures the electrical activity of the cerebral cortex [Sir14] Because ECoG devices are located inside the skull but still outside the brain, they are sometimes referred to as partially invasive. With intracortical implants however, the electrodes penetrate the brain, allowing a high spatial and fast temporal resolution [Alh23]. The latter method in particular provides a level of detail that cannot be achieved with other methods.

The use of invasive methods in humans is usually reserved for applications where the benefits can outweigh the potential risks. It can be argued that this is the case, for example, in individuals with severe mobility impairments (e.g. due to paraplegia) or severe neurological diseases. On the other hand, for other targeted applications with arguably less impact on quality of life, such as in the entertainment industry, such methods are excluded in contrast to non-invasive methods.
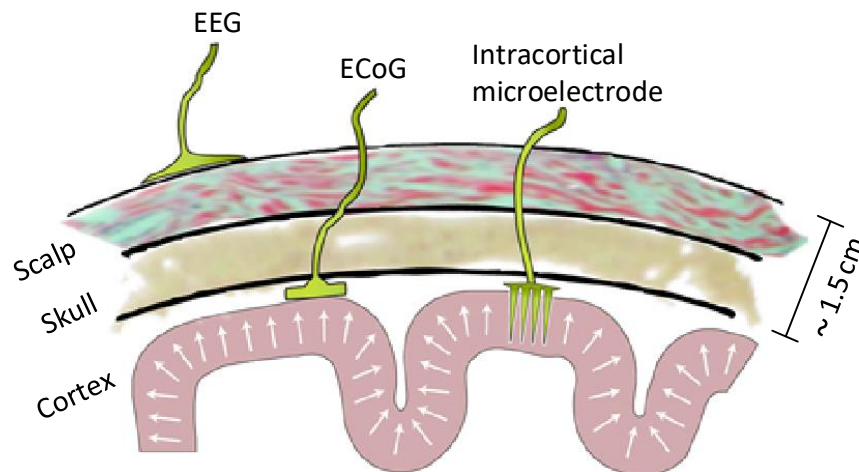
Figure 2.2: *Overview of electrode types for electrical brain activity measurements in the context of BCIs (adapted from [Mil20])*

Table 2.1: *Non-invasive methods for measuring brain activity (adapted from [Alh23])*

Method	Mobility	Approximate Resolution	
		Spatial [mm]	Temporal [s]
Magnetoencephalography (MEG)	static	0.05	0.05
Functional Magnetic Resonance Imaging (fMRI)	static	1	1
Near-Infrared Spectroscopy (fNIRS)	portable	5	1
Electroencephalography (EEG)	portable	10 - 30	0.05

Non-Invasive Brain Sensing Methods

In contrast, non-invasive BCIs record brain activity from the scalp or outside the head. These methods do not require surgery and are therefore safer for the user and easier to apply. The drawback is usually lower signal resolution and higher susceptibility to noise and artifacts.

Table 2.1 summarizes prominent non-invasive methods for sensing brain activity. A distinction is made between methods that can only be used in a stationary environment and those that may allow mobile use. Respective reference values for spatial and temporal resolution are also given.

Magnetoencephalography (MEG) measures changes in the magnetic field on the scalp that are related to the electrical activity of neurons. For this purpose, superconducting quantum interference devices (SQUIDs) are attached to the head. The resulting local and temporal resolution is comparatively good in the class of non-invasive methods. An alternative stationary method is functional Magnetic Resonance Imaging (fMRI). It detects changes in blood oxygen levels in the brain that correlate with various neural activities.

Near-infrared spectroscopy (fNIRS) and Electroencephalography are listed in Table 2.1 as non-invasive methods that can be applied in mobile scenarios. In fNIRS, infrared light is projected through the scalp into the brain to measure a wavelength change related to blood oxygen levels and blood flow in the reflected light. EEG, on the other hand, uses electrodes on the scalp to measure the electrical activity of neurons in the brain. Compared to fNIRS, EEG has a slightly lower spatial resolution, but the temporal resolution is much better.
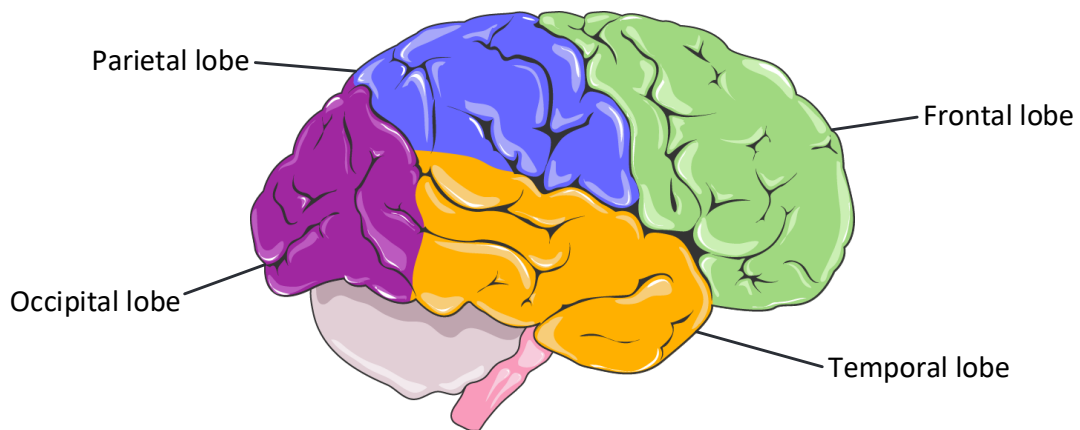
Figure 2.3: *Principal brain fissures and lobes from lateral view; Figure modified with text after adaptation of "Brain" from Servier Medical Art by Servier, licensed under a Creative Commons Attribution 3.0 Unported License*

In the context of this work, only EEG-based methods will be focused on. It should be noted, however, that they can generally be combined with other methods such as fNIRS to enhance the performance of the BCI [Liu21].

2.1.1. Fundamentals and Characteristics of Electroencephalography signals

Electroencephalography (EEG) measures electrical potential differences using electrodes placed on the intact scalp. These potential differences are generated by neurons near the surface of the cerebral cortex. Thus, EEG signals are a superposition of the voltage differences from the activation of nearby neurons that penetrate the scalp. The voltages measured can be correlated with specific brain functions. The correlation with a particular function also depends on the position of the electrode in relation to different areas of the brain.

The cerebral cortex is divided into the left and right hemisphere. Each is typically subdivided into four additional areas called lobes (see Figure 2.3). These are anatomically distinct and are thought to have different functions. The occipital lobe is located at the back of the head and is the smallest of the four main lobes on each side. It is primarily responsible for visual processing. Next to it at the top of the brain lies the parietal lobe. This contains various areas for processing sensory information, such as the sense of touch or spatial sense. Some of its areas are also involved in language processing. Below the parietal lobe, on the side of the head, is the temporal lobe. This is where the centers for processing auditory information, such as understanding speech, are located. This lobe also plays an important role in memory formation. At the front of the head is the frontal lobe, which is responsible for higher cognitive functions. These include reasoning, problem solving, motor functions, and emotion regulation. This area is also involved in memory storage. In general, there are much more detailed subdivisions of the cerebral cortex, such as the 52 Brodmann areas ([Bro05]), but their description is beyond the scope of this paper. Furthermore, the brain is highly interconnected and the different areas work closely together. Therefore, although a particular lobe is often primarily associated for certain functions, different regions across lobes are often used in conjunction.
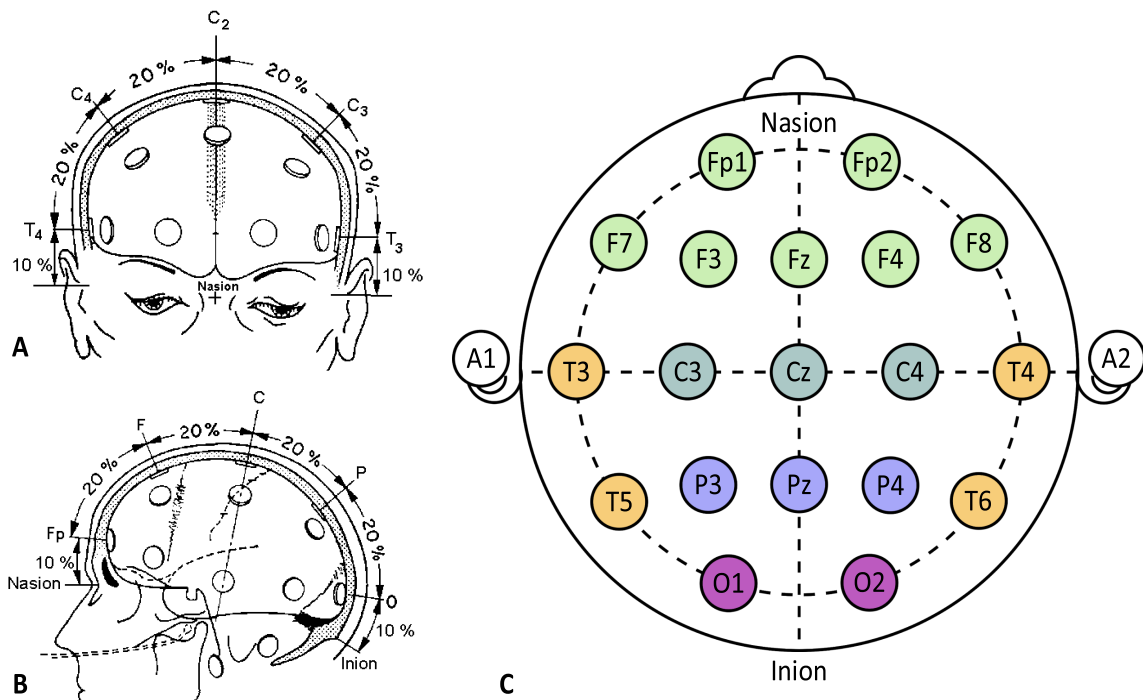
Figure 2.4: *A (lateral view) and B (frontal view) show the 10-20 international system for EEG electrode placement as proposed by Herbert Jasper in 1958 ([Kle99]); C is a schematic representation of this placement from superior view (adapted from `https://commons.wikimedia.org/w/index.php?curid=10489987` accessed on July 20th 2023)*

Because of these local dependencies, electrode positions significantly affect the recorded EEG signals. Generally, the electrical activity of the brain needs to be recorded from multiple locations simultaneously. For this purpose, several electrodes are placed at the same time, and the recorded signals are referred to as EEG channels. To ensure reproducibility and comparability of EEG data, available standardized placements are helpful. These should be adaptable to different head shapes and sizes.

The 10-20 system is one such standardization that allows for reliable and repeatable electrode placement. It was first described by Herbert Jasper in 1958, has been standardized by the American Electroencephalographic Society and is a commonly used method for electrode placement [Nic12]. Figure 2.4 shows on the left (A and B) two figures from the original publication ([Kle99]). Based on these figures, the intended electrode positions are explained. These are based on certain anatomical landmarks on the head, in particular the nasion (the depression between the eyebrows and the nose), the inion (the protruding bone at the back of the head) and the bilateral preauricular points (depression in front of the external auditory canal). The center point on the top of the head between those landmarks is the vertex, the highest point of the head. The distances between these landmarks are divided into 10 % and 20 % increments where the electrodes should be placed. This results in a total of 21 electrode positions. A schematic view from superior perspective is shown on the right side of 2.4. The electrode designators are characterized by the respective head region and are related to the brain lobes (compare color coding of electrodes with Figure 2.3):
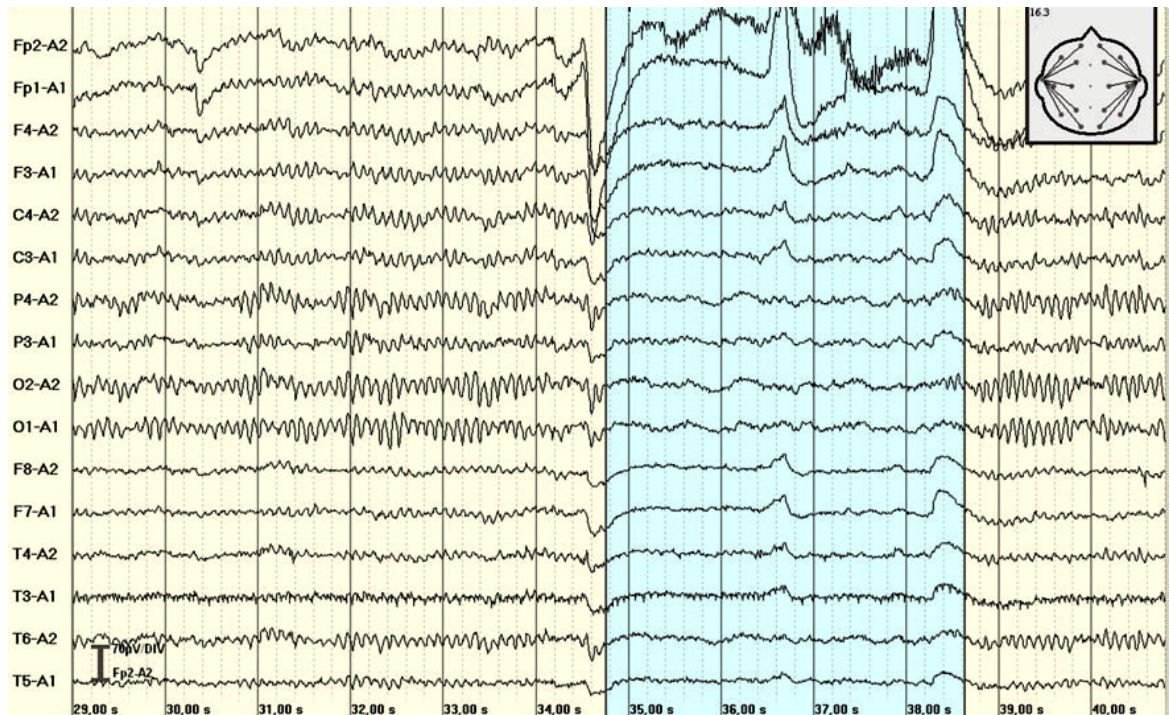
Figure 2.5: *Example EEG with 16 channels adapted from [Hof11]; the yellow area indicates eye closing and the blue area opened eyes; electrode positions and interconnections are given in the top right*

- Fp = frontopolar
- F = frontal
- C = central
- P = parietal
- O = okzipital
- T = temporal
- A = aurical

The corresponding electrode number indicates the distance to the midline, which is the connecting line between the nasion and the inion. The larger the number, the further to the side the electrode is located. Hereby, even numbers are used for the right hemisphere and odd numbers for the left hemisphere. The electrodes that are directly on the midline are labeled with 'z', which represents the zero distance.

This reference placement standard is endorsed by the International Federation of Clinical Neurophysiology and is sometimes refered to as the 20 % system. There are also other methods of electrode placement, such as the 10-10 [Nuw98] and the 10-5 [Oos01] systems, which allow a denser placement of electrodes and thus a higher spatial resolution. Consequently, they are also often referred to in short form, i.e. 10 % and 20 % system. They follow the same landmarks and are based on the same principle, but they subdivide the scalp more finely and thus allow for more electrodes at defined positions (up to 74 and 345). However, this is associated with a significantly higher effort in electrode placement and is therefore only used when needed.

Table 2.2: *Frequency bands in EEG signals as well as their relation to cognitive tasks and states (adapted from [Sai23])*

Rhythm	Frequency [Hz]	Occurrence
Delta (δ)	≤ 4	Deep sleep
Theta (θ)	4 - 8	Drowsiness
Alpha (α)	8 - 13	Relaxed awake state, eyes closing
Beta (β)	13 - 30	Alert state, active thinking/attention/concentration
Gamma (γ)	≥ 31	High-level cognitive function
Mu (μ)	8 - 12	Motor cortex functionalities

An example of a 16-channel EEG recording is shown in Figure 2.5. In order to measure the voltage potential at a position, a second electrode is required as the second pole. In this example, these are the auricular electrodes A1 and A2. The selected configuration is shown in the upper right corner of the figure and is also reflected in the names of the vertical channels on the left. The electrodes have been placed in a 10-20 system, leaving the central electrodes on the midline unused. Typical EEG signals are in the range of $5\,\mu$V to $100\,\mu$V and have analyzable frequency components of $1\,$Hz to $70\,$Hz [Kra17].

Furthermore, the background of the figure is color-coded to indicate the period (abscissa axis) in which the eyes are closed (yellow) or open (blue). It can be seen that the transitions, i.e. the opening and closing of the eyes, have a clear influence on the course of the EEG signals. This effect is stronger the more frontal the corresponding signal electrode is located. Moreover, the two periods differ significantly in terms of amplitude and frequency.

Periodic information in EEG signals is often distinguished by its frequency. Table 2.2 shows the most common frequency ranges, also called rhythms. The 'Occurrence' column indicates to which functions or states a pronounced activity of an EEG signal in this frequency range corresponds. Besides the classical frequency ranges delta (δ), theta (θ), alpha (α), beta (β) and gamma (γ), other more specific rhythms are sometimes described. One example given here is mu (μ), which frequencies overlap with α. It is associated with motor cortex functions and is characterized as non-sinusoidal [McF00].

In general, there are several approaches to the reference electrode in EEG signal recording. The configuration shown in Figure 2.5 is called unipolar measurement. In contrast, in a bipolar measurement, the potential difference is always determined by two other electrodes and there is no uniform reference. This makes the gradient of the signals more comparable, but the amplitudes and respective phases more difficult to compare quantitatively [Hof11]. In addition to the active signal electrodes and the reference electrode, a ground electrode is used for high-quality signal acquisition and assists by reducing common-mode interference. This electrode, also called a bias electrode, is typically placed at a site that is considered electrically neutral and unlikely to be influenced by specific brain activity. Typical locations include the forehead or earlobes. Therefore, for example, to measure 8 EEG signal channels in unipolar configuration, at least 10 physical electrodes would be required, including a dedicated reference and bias electrode.

Classes of Artifacts in EEG signal acquisition

At this point, artifacts in EEG signal acquisition should be explicitly discussed. Due to the low voltage levels of EEG signals in the microvolt range, they are susceptible to interference voltages that superimpose and distort the actual signals in focus.

The artifacts that occur can be divided into the following two categories: Physiological and Technical Artifacts. Some representative and common examples of each category are described below:

- Physiological Artifacts:
  - Eye Artifacts: Eye movements and blinks, typically large amplitude and slow waveforms, particularly prevalent in frontal electrodes
  - Muscle Artifacts: Especially facial and oral movements, generally seen as high-frequency activity
  - Cardiac Artifacts: Electric activity of the heart, usually regular, rhythmic waveforms
- Technical and Environmental Artifacts:
  - Electric Noise: Environmental electromagnetic radiation, especially powerlines, typically appearing as 50 Hz or 60 Hz signal in EEG
  - Movement Artifacts: Caused by moving of the subject, resulting in electrode shift or wire sway, which cause noise in EEG
  - Electrode Pop: Momentarily contact loss of an electrode with the skin, leading to a sudden and large-amplitude signal

In this context, depending on the type of EEG recording, other neurophysiological signals may also be interpreted as interfering signals. For example, if the focus of the recording is solely on auditory processing, signal components from the motor cortex or visual processing will interfere.

Some examples of artifacts and their impact on the EEG signal waveform are shown in Figure 2.6. The time periods highlighted in red indicate the visible occurrence of eye (A), muscle (B), heart (C) and electrode pop (D) artifacts. These can affect individual electrodes as well as the entire EEG recording. It can be observed that the amplitudes of the artifacts can sometimes significantly exceed the levels of the regular EEG signals.

Each of these artifacts and interferences can distort the EEG signal and make it more difficult to interpret. Therefore, it is important to use techniques to minimize these artifacts during data collection and to use signal processing techniques to remove or reduce these artifacts during data analysis. Some methods are discussed in section 2.2.

2.1.2. Sensors for Electroencephalography

Sensors for EEG signal acquisition are designed to sense the electrical signals generated by neuronal activity in the brain. For this purpose, non-invasive surface electrodes can be used that are in direct contact with the scalp via an electrolyte layer. The electrodes must be made of a conductive material. Ag/AgCl is often used as the contact material [Hof11]. The coating with the poorly soluble salt AgCl prevents the electrode from becoming polarized, which would
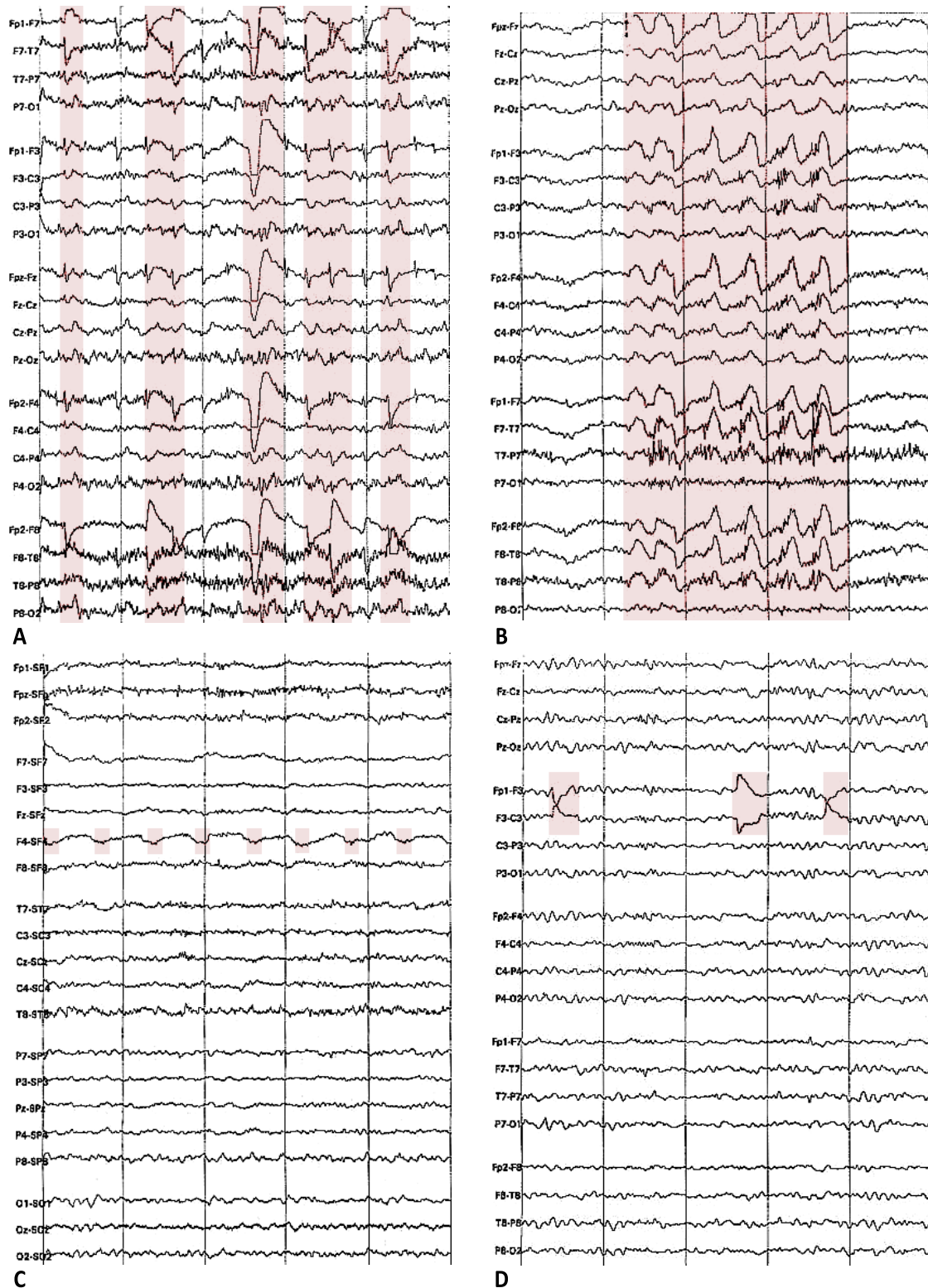
Figure 2.6: *Example artifacts in EEG signals, the periods with the most pronounced artifacts are highlighted in red. A: Rapid eye movements cause spikes especially in frontal electrodes (F7, F3, Fz, F4 and F8). B: Tongue muscle movement by saying "la la". C: Cardiac rhythm visible on electrode F4. D: Electrode pop of electrode F3. (all figures adapted from [May16])*

Table 2.3: *Application specific EEG sensors*

Sensor	Placement	Connectivity	Type	Contact	Mounting	#Electrodes
trEEGrid	Lateral Forehead	Passive	Wet	?	Adhesive	9*
cEEGrid	Circumaural	Passive	Wet	Ag/AgCl	Adhesive	10
Ear-EEG	In-ear	Passive	Wet	Ti/IrO2	Plugged	15
Bittium BrainStatus	Forehead	Passive	?	?	?	16*
fEEGrid	Forehead	Passive	Wet	Ag/AgCl	Adhesive	24*
g.PANGOLIN	Flexible	Active	Wet	Gold plated	Adhesive	16-1024

*Cell values in column #Electrodes marked with * include electrode placement outside classical EEG like Electrooculography (EOG) positions*

distort the measured signals. Moreover, the material has low thermal noise, is biocompatible, and is more DC stable than, for example, pure gold electrodes [Gór19].

In order to record the relatively weak electrical signals well, a good connection and low impedance between the scalp and the electrode contact is desirable. Acceptable impedance values are below $10\,k\Omega$ [Sin16]. For this reason, some EEG sensors are designed with wet electrodes that use a conductive fluid such as gel between the skin and the contact to improve the electrical connection. Another advantage of wet electrodes is that they reduce motion and skin surface artifacts [Sai23]. However, dry electrodes are generally faster to apply and avoid the signal degradation that can occur with wet electrodes as the conductive gel dries.

The electrical output signal from EEG electrodes must then be digitally converted for digital processing. The Analog-to-Digital-Converters (ADCs) required for this are specially designed for this type of signal and its characteristics. In some sensor systems, the conversion from analog to digital takes place directly at the sensor. These are called active (as opposed to passive) electrodes. This has the advantage of a better signal quality, as motion artifacts and interference from the wiring can be reduced. A disadvantage of this approach, however, is that the additional electronics required make active EEG sensors heavier and larger. Therefore, they are less attractive for long-term recordings with many desired EEG channels.

Typically, the individual electrodes are placed and secured on the skull using EEG caps. These caps usually have holes into which the electrodes can be inserted. The position of the holes is based on the well-known 10-20 or 10-10 systems. The caps are available in different sizes to allow correct placement of the electrodes.

For mobile signal recording, especially for long-term BCI applications, the classic EEG caps are not very suitable due to their size. They are uncomfortable to wear for long periods of time and may distract the subject in real-life situations. For this reason, there are smaller EEG sensors that do not cover the entire scalp. Here, however, the correlation between the electrode positions and the focused brain activity can be exploited (compare section 2.1.1). This is particularly useful for mobile BCIs, since their application pursues a clear use case and thus certain brain areas (e.g. auditory cortex) are of particular interest.

An overview of some of these sensors, referred to within this work as application-specific EEG sensors, is given in Table 2.3. All entries except the Bittium BrainStatus are shown in Figure 2.7 (B-F), as well as a classical EEG cap (A) for comparison. The electrodes of the application-specific sensors are centered on specific areas of the head, such as the forehead or
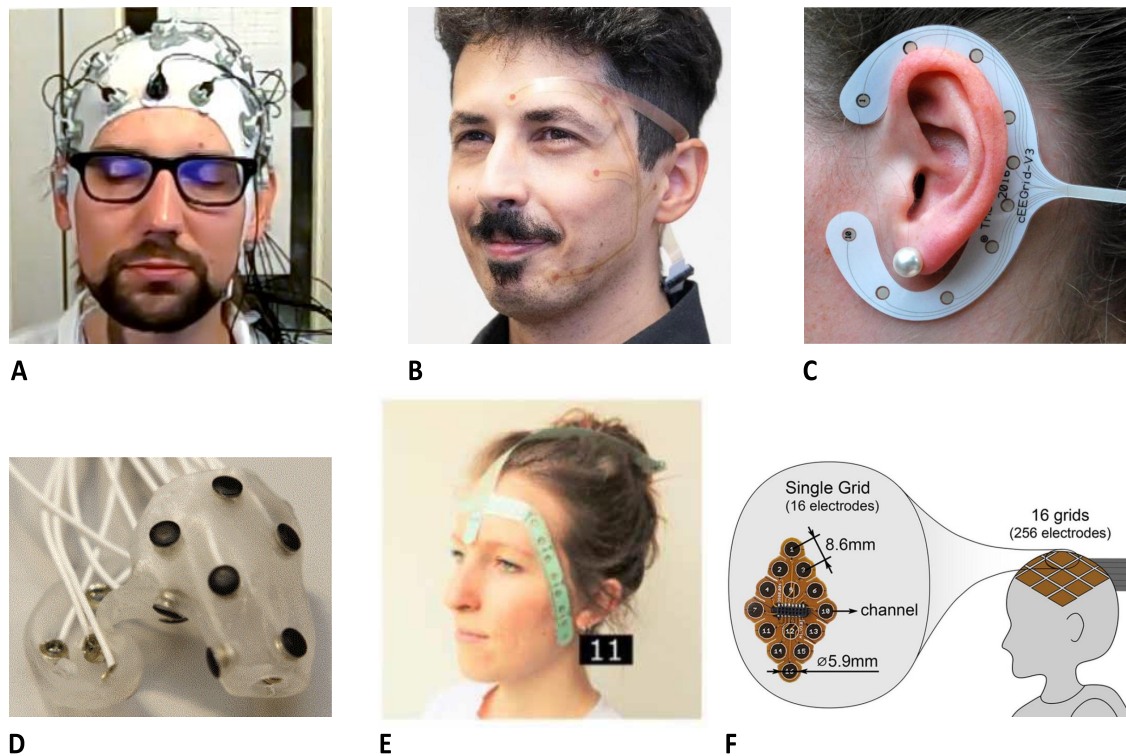
Figure 2.7: *Different types of EEG sensors. A: Classic EEG cap for measurements oriented to the 10-20 system. B: trEEGrid sensor adapted from [Da 22]. C: cEEGrid sensor adapted from [Hol22]. D: In-ear EEG sensor adapted from [Kap17]. E: fEEGrid sensor adapted from [Blu20]. F: g.PANGOLIN sensor adapted from [Lee22].*

the ear. The only exception is the g.PANGOLIN system, which has a very high electrode density and can be placed anywhere on the scalp. It is also the only system that has been deliberately designed for cascading, theoretically allowing signal acquisition over larger areas with up to 1024 electrodes. With this system, it should also be noted that the sensor shown in Figure 2.7 F is theoretically passive. However, because the ADC is located directly on the sensor in the junction box (not shown), the system is advertised as active. All other sensors listed in the table are passive and (as far as known) with wet electrodes. Another interesting feature of these application-specific sensors is the number of EEG electrodes provided, which in almost all cases is less than that of a full configuration of the 10-20 system (21 electrodes). This is primarily due to the localized focus on specific brain areas. Another aspect is that this reduces the dimensionality of the EEG data to be processed. This is particularly useful for a mobile BCI, where computational power is limited.

2.2. Preprocessing and Feature Extraction Algorithms

This section provides an overview of EEG signal processing algorithms in the context of BCIs. The first part focuses on typical preprocessing, which is primarily aimed at minimizing artifacts and irrelevant signal components from the recorded EEG signals. In the second part, exemplary methods for classification of EEG signals are presented.

According to [Lot07], BCI-related EEG signal processing algorithms face the following challenges:

- Artifacts: As described in Section 2.1.1, the brain activity information that is the focus of an application is often obscured by artifacts. This is primarily due to the low voltage levels of EEG signals and the resulting low Signal-to-Noise Ratio (SNR).

- High dimensional: EEG signals often have high dimensionality (e.g. [Rak05]). Individual features are usually extracted from multiple input channels and possibly from different time segments [Lot07]. This increases the computational complexity of the algorithms.

- Non-stationary: The extracted features are non-stationary. This means that EEG signals can vary greatly over time. This effect is amplified when recordings are made in different sessions.

- Small training sets: The available training sets of EEG data for algorithms are relatively small. This is due to the time-consuming and sometimes strenuous nature of data acquisition, including the application of electrodes. This is further complicated by the fact that the characteristics of the recorded signals vary greatly between subjects [Hua23]. Therefore, it makes sense to include the data of the specific BCI user in the training set, or to calibrate it to that person in some other way.

2.2.1. Preprocessing and Artifact Handling Algorithms

Before the actual brain activity information is extracted from the recorded EEG data, the data is preprocessed. Here, artifact handling methods specifically adapted to EEG signals are primarily used to facilitate the evaluation or automatic classification of the data. Nevertheless, there are also some general preprocessing methods that are used regularly. A typical example is resampling, which aims to reduce the amount of data for subsequent processing steps. This can save computing time and hardware resources such as memory. This is especially possible when the frequency range in which features occur is known for a particular application.

However, algorithms to counter the parasitic factors and interferences of EEG recordings are essential and is considered the most important preprocessing step of EEG data [Jia19]. Some artifacts, such as ambient electrical line noise, are outside the frequency range of the desired signals and can be removed by a simple filter [Uri15]. In other cases, especially for physiological artifacts, methods for their detection and, preferably, their correction are required.

Statistical methods, such as the standard deviation, can be used to detect the presence of artifacts. Based on this, time segments with known artifact occurrence can be omitted [Ble16]. This method works well for artifacts with relatively large amplitudes, such as eye artifacts. However, the relevant neural signals are also lost during these epochs. Therefore, if possible, methods with simultaneous artifact correction are preferred.

The main classes of algorithms that can detect and simultaneously correct artifacts in EEG signals are summarized in Table 2.4. These algorithms fall into two main categories: Reference signal-based methods and decomposition methods [Jia19]. The former use additional input electrodes in addition to the EEG signals, such as Electrooculography (EOG) for eye artifacts or Electrocardiography (ECG) for heart rhythm artifacts. Based on these additional inputs, the signal components of the respective artifact class can be estimated and removed from the EEG

Table 2.4: *Common classes of artifact correction algorithms for EEG signals*

Reference-based	Decomposition	Hybrid Methods
Regression	Principal Component Analysis (PCA)	Enhanced EMD + ICA
Adaptive Filtering	Independent Component Analysis (ICA)	Enhanced EMD + CCA
	Canonical Correlation Analysis (CCA)	DWT + ICA
	Discrete Wavelet Transform (DWT)	DWT + PCA
	Empirical Mode Decomposition (EMD)	

EEG Data → Transform → Denoising → Inverse Transform → Cleaned EEG Data
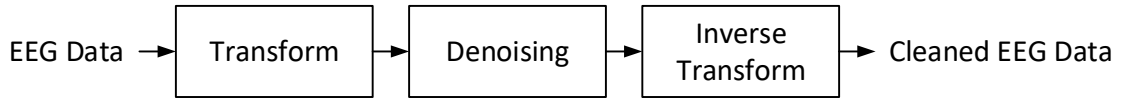
Figure 2.8: *Decomposition algorithm principle for artifact correction of EEG data*

data. Decomposition methods, on the other hand, convert the EEG signals into other domains and do not require any extra inputs. In addition to some typical representatives of each category, Table 2.4 also lists examples of hybrid approaches that combine different methods.

In the first category, additional electrodes are used as a reference for physiological artifacts. Regression methods [Woe83] or, alternatively, adaptive filters [Cor07] are used to clean the recorded EEG signals from the artifacts of the respective reference signals. The regression approach is characterized by low computational cost [Jia19]. However, all reference-based methods are limited to correcting artifacts for which one or more good reference channels are available. This implies that a suitable sensor system must be provided. For instance, to theoretically eliminate eye artifacts, heart rhythm artifacts, and all possible muscle artifacts, a large number of additional electrodes would be required. In addition, the influence of the different signal recordings is bidirectional. For example, parts of the brain activity information are also contained in the EOG, which can be erroneously corrected by these methods [Jer89]. For these reasons, reference-based methods are uncommon in practical applications. Nevertheless, they are used as gold standards for the evaluation of other methods [Kot20].

The second category is based on the decomposition of EEG signals into other domains. Figure 2.8 visualizes the basic idea underlying all methods of this class. In the first step, the EEG signals are transformed. Then, artifact-dominated signal components are separated from the actual brain activity information and can be removed. Finally, the cleaned EEG data can be reconstructed using an inverse transformation. The step of identifying the artifact-dominated signal components is generally not a fixed part of the decomposition algorithms. This can be done either manually (e.g., by visual inspection) or automatically. Automatic identification of artifact-dominated signal components can be based on statistical features, simple thresholding, or additional algorithms such as support vector machines (SVMs) [Sho05; Hal07].

The most widely used decomposition-based algorithms are the so-called Blind Source Separation (BSS) approaches [Jia19]. They include Principal Component Analysis (PCA), Independent Component Analysis (ICA), and Canonical Correlation Analysis (CCA). PCA is one of the simpler BSS approaches and is based on the eigenvalues of the covariance matrix [Uri15]. In [Ber91], PCA was successfully used for the first time to detect and remove ocular artifacts (blinking and eye movements) from EEG data using the variance of the transformed signals. ICA is based

Table 2.5: *Examples of typical features extracted from EEG recordings*

Event-Related Features	Rhythm-Based Features
Event-Related Potentials (ERP)	Sensorimotor Rhythms (SMRs)
Slow Cortical Potentials (SCPs)	Power Spectral Density (PSD)
Steady-State Visual Evoked Potentials (SSVEP)	
Event-Related (De-)Synchronization (ERD/ERS)	

on the assumption that the recorded signal is a linear mixture of cerebral and artificial sources and that the sources are statistically independent [Jia19]. It has also been successfully used to correct for ocular [Vig00] and muscle-related artifacts [Vig97]. A limitation of ICA is that the number of observed signal mixtures must be at least as large as the number of signal sources. This is not always achievable, especially in EEG recordings with few channels. In contrast to ICA, which is based on higher-order statistics, CCA uses only second-order statistics. This has a positive impact on the computational time required [Jia19]. CCA is particularly suitable for removing muscle artifacts as induced through spoken language [Wim06; Vos10].

Other exemplary approaches of decomposition-based methods for artifact correction are Discrete Wavelet Transform (DWT) [Saf12] and Empirical Mode Decomposition (EMD) [Zha17]. All of the decomposition algorithms have their own advantages and disadvantages, which is why many hybrid approaches are being researched. These combine two or more known methods to improve performance in artifact correction. Examples include enhanced EMD with ICA [Soo13], enhanced EMD with CCA [Swe13; Che19], DWT with PCA (also called Multiscale PCA) [Kev14; Kev15], and DWT with ICA [Lin05; Cal14].

It should be noted that this list of methods and examples is not exhaustive. There are many other methods and approaches for detecting and correcting artifacts in EEG recordings. No single artifact correction algorithm works for all applications and artifact types, and therefore this topic is still subject of extensive research [Jia19].

2.2.2. Brain Signal Features and Classification Algorithms

In this section, typical features extracted from EEG signals are discussed and an overview of exemplary classification algorithms is presented. The signal features may be in the time domain, the frequency domain, or both. The most common types of features include amplitudes, latencies, or power spectra of specific frequencies [Mak09]. Of course, for all features it is also important from which region of the scalp, i.e. at which electrode position, they can be detected.

A list of some typical extracted features is given in Table 2.5. As can be seen, the presented methods can be divided into two categories: The event-related features, also called Evoked Potentials (EPs), and the EEG rhythm-based features. EPs can be thought of as the measured neural response of the brain to stimuli. Internal stimuli are usually related to the subject's movement. External stimuli are usually visual, auditory or somatosensory.

Voltage fluctuations that occur in specific time frames after a stimulus are called ERPs. There are a variety of observed ERPs associated with different brain processes after the onset of a stimulus. The most important ERP in research is the P300 [Sur09]. This can be seen in EEG signals as a small positive voltage change (about 10 µV) with a delay of 200 ms to 400 ms relative
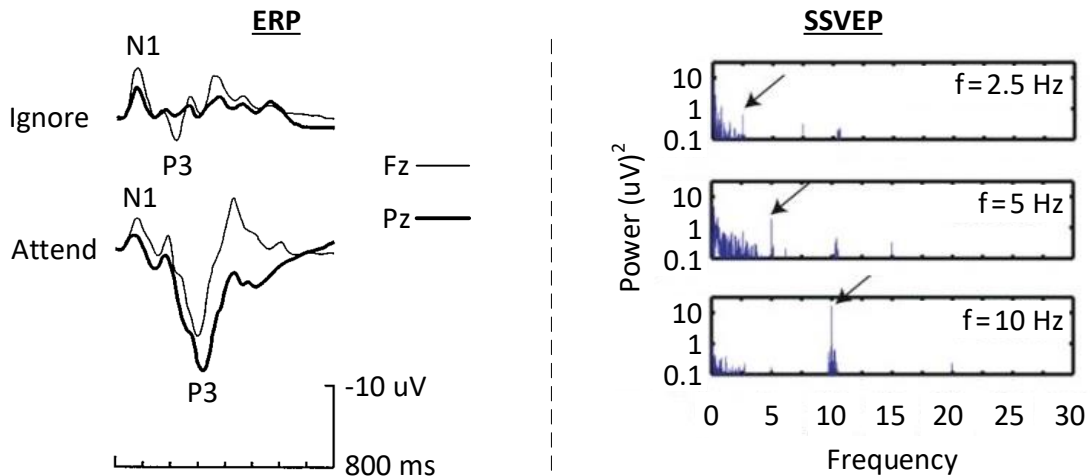
Figure 2.9: *Event-Related Potential (ERP) and Steady State Visually Evoked Potential (SSVEP) event-related features of EEG signals (ERP adapted from [Pic92] and SSVEP adapted from [Din06])*

to the time of the stimulus [Pic92]. The naming of ERPs is based on the observable change in the EEG signal waveform: the letter indicates the direction of the expected voltage change (p=positive, n=negative) and the number indicates the approximate latency in milliseconds. Figure 2.9 (left) shows the progression of the N100 and P300 ERP for illustration.

Another type of time-domain EP is the Slow Cortical Potential (SCP). These are relatively slow voltage changes in the EEG signal with a duration of about 300 ms to several seconds [Bir99]. They are related to the level of excitability of the cerebral cortex and are associated with cognitive processes such as attention [Hin04] or anticipation [Bir81]. With appropriate training, they can also be generated voluntarily, which makes them interesting for BCI applications [Hin04].

There are also EPs in the frequency domain such as SSVEPs or Event-Related Desynchronization/Synchronization (ERD/ERS). The former are responses of the brain to a visual stimulus of constant frequency (e.g. flicker). They are expressed in the EEG signals by the fact that the corresponding frequency is clearly visible especially when the corresponding stimulus source is in focus. SSVEPs are characterized by good SNR and have been used for BCI applications as well [Mid00].

ERD/ERS are stimulus-induced changes in the power of the EEG signal within specific frequency bands or EEG rhythms. For example, they can be utilized at the appropriate scalp position within the β and μ frequency ranges to generate motor control signals within a BCI [Tan16].

Rhythmic features (see Table 2.5) occur independently of stimuli. The first example is the Sensorimotor Rhythm (SMR), which occurs close at the sensorimotor cortex (located at the front of the parietal lobe). It includes the μ frequency range, usually with some β or γ components [Lau16]. They are commonly used in motor-related BCI applications where the imagery of a motor movement is used as a control signal [Kub05]. It should be noted that other EEG rhythms can also be used as the basis in this context to serve other applications.

The second example is the so-called Power Spectral Density (PSD). This is not based on the classical EEG rhythms, but on the mathematical power density of different frequency ranges.

Table 2.6: *Common classification and data analysis algorithms used for EEG-based BCIs*

Machine Learning	Deep Learning
Linear Discriminant Analysis (LDA)	Convolutional Neural Network (CNN)
Support Vector Machine (SVM)	Long Short Term Memory (LSTM)
K-Nearest Neighbor (KNN)	

It is applied to EEG signals to identify dominant frequencies and their respective power. One possible application for BCIs is, to infer the user's intention [Xio22].

In addition to the methods summarized in Table 2.5, spatial features can also be extracted and used as input for subsequent classification. The most popular method is the Common Spatial Patterns (CSP) [Kai14]. It can also be used to reduce the number of EEG electrodes to be considered. Moreover, several related methods exist, such as Separable Common Spatio-Spectral Patterns [Agh16].

2.2.3. Classification Algorithms

Ultimately, the features of the recorded brain activity must be interpreted automatically to generate control signals for other devices in the BCI context. For this purpose, a classification of the EEG data or its features is performed. Possible results are e.g. (non-)attention to a stimulus (Attention Decoding) [Ble16], imagined rehearsal of a movement (Motor Imagery) [Wan17], or decoding the emotional state of the user (Emotion Recognition) [Tor20].

In [Sai23], 84 publications on the Motor Imagery paradigm are reviewed in the context of EEG-based BCIs. Table 2.6 summarizes the classification methods and other data analysis techniques described therein that are frequently applied and researched. These approaches are divided into classical machine learning, and deep learning. The order within the categories is sorted by frequency of publication, with the above entry being the most frequently used among the 84 papers considered.

The classical machine learning seem to be the most used category. Among them, the two methods Linear Discriminant Analysis [Kar22; Du 21] and Support Vector Machine [Kar22; Wan17] dominate. In addition, the K-Nearest Neighbor approach appears regularly in the reviewed publications [Kar22; Api21].

In deep learning approaches, most of the architectures used are based on Convolutional Neural Networks [Zhu21; Mah21]. In some publications they are combined with Long Short Term Memory layers [Gar20; Mwa21].

Most of the classification algorithms considered in [Sai23] are binary, although some publications on multi-class tasks are also included. In most cases, a classification accuracy $> 70\%$ is achieved. However, most publications focus on pure offline analysis and only a few implementations follow the online approach. Online in this context refers to the processing of incoming EEG data at runtime while the data stream is active. The term online processing will also be used in the rest of this work.

Besides the mentioned Machine Learning and Deep Learning models, some statistical analysis has also been applied. For example, methods based on correlation [Ble16], CCA [Byu19],

Table 2.7: *Main categories for BCI applications*

Assistive Technology	Rehabilitation & Augmentation	Recreation
Communication	Attention monitoring	Games
Mobility	Rehabilitation robots	Virtual Reality
Environmental control	Feedback Training	Creative Expression

Mean Square Error (MSE) [Shy13], or Bayesian Networks [He16] have been applied for EEG classification.

Some state-of-the-art FPGA implementations of EEG signal processing in the context of BCIs are presented in Chapter 3.3.

2.3. Applications of Brain-Computer Interfaces

In this section, an overview of the versatile applications of BCIs is given. To date, the predominant motivation for BCI research has been to assist people with severe physical disabilities [Tan10]. However, other areas are increasingly being explored.

The main categories of BCI applications are shown in Table 2.7: Assistive technologies, rehabilitation and augmentation, and recreation. There are several examples for each of these, which are discussed below.

2.3.1. Assistive Technologies

The ability to communicate has been identified as one of the most important needs for people with severe physical disabilities [Tan10]. The simplest BCI applications for communication are based on binary classifiers that allow rudimentary communication via "yes" and "no" responses. For example, the SMR [Bla06], SCP [Küb01] or SSVEP [Yin15] features have been used for this purpose. Building on this, spellers[1] can also be implemented using a decision tree to allow the formulation of free text [Per00]. Another early approach to implement a speller is the so-called "Farwell-Donchin Matrix", which is based on ERPs [Far88]. Here, groups of letters are made to flash, and the group that the user focuses on can be identified. In general, further developments in this area aim at speeding up the spelling process. One possible approach is predictive spelling [Bla07].

The restoration of motor function is also profound for individuals with severe motor impairments. One possible goal may be to perform an independent grasping movement with the help of a BCI. For this purpose, a hand orthosis can be closed or opened using SMR [Pfu00]. Based on SSVEP using four Light-Emitting Diodes (LEDs) mounted on a hand prosthesis, two additional conditions for bilateral rotation of the artificial wrist could also be achieved [Mul08]. Another approach is to control an assistive robot. Using ERPs based on real feedback from the robot itself, it could be controlled to perform discrete tasks such as picking up and moving an object [Bel08].

---

[1]A speller is a type of device that typically selects individual letters of the alphabet one at a time to build words and phrases over time

Finally, the restoration of autonomous locomotion is also an important area of BCI application, improving the quality of life and autonomy of affected individuals [Nic12]. Of particular interest is the control of a wheelchair. One possibility for control is preprogrammed landmarks that can be approached and selected with the help of ERP based on suggested options (e.g., living room) [Bla08]. Alternatively, freely selected movements of the wheelchair can be enabled, as in [Ban21]. Here, an eight-class system is proposed to select bilateral turning, forward and backward movement, and speed adjustment. Based on α rhythm during eye opening and closing, ERD/ERS are binary classified. Finally, the actual command is selected in a three-step procedure. In both examples, special obstacle detection functions of the wheelchair are implemented to avoid collisions with environmental objects.

The same principles can be applied to control devices in the environment. SSVEP classification enabled number dialing for telephoning [Min02], based on SMR, various devices such as lights, TV and front door opener could be controlled [Cin08].

2.3.2. Rehabilitation and Augmentation

BCIs can save lives in safety-critical jobs by automatically monitoring the alertness of those in charge [Tan10]. If drowsiness is detected in air traffic controllers or long-distance truck drivers, appropriate action can be taken. Based on the α and θ frequency spectra, such drowsiness can be detected automatically [Lin10].

In addition, BCIs are being studied for therapeutic use. For example, a stroke can cause a patient's motor control to be limited or partially lost. Rehabilitation robots controlled by neural signals can help to treat this paralysis beyond traditional therapies [Tan10]. In upper limb rehabilitation, for example, patients are asked to move robotic arms connected to their own arms in a two-dimensional plane using their motor cortical brain signals. The associated visual and proprioceptive feedback should help to restore or replace damaged neural pathways and thus improve stroke recovery [Jac10].

The feedback from BCIs can allow selective control of specific brain areas, resulting in behavioral changes in the brain [Nic12]. This effect can be exploited, for example, to improve cognitive performance [Han05]. It can also be used to treat mental disorders such as attention deficit [Str06], depression [Sch92], or alcohol dependence [Sch93].

2.3.3. Recreation

With significant advances in BCI technology, interest in entertainment applications has increased [Nic12]. Interpreted brain activity provides a new level of interaction with video games. Popular video games with simple inputs such as Pacman or Pong have been adapted and a BCI can be used as a controller [Kre07]. In addition, new games have been developed. In the case of the game "BrainBasher" [Pla08], a user satisfaction survey showed that players found the BCI controller more enriching and engaging than traditional input methods.

With Virtual Reality (VR) applications becoming increasingly popular, the BCI is also becoming more interesting as a further communication level for this. In addition to control via the BCI, a passive application that assesses the workload level or attentional state of a user, for example, can also serve as an input for the VR application [Put20].

As a final example in the area of recreation, a BCI can also be used as a means of creative expression. The output of a brain-controlled BCI has been used to generate both music [Mir05] and visual art [Rap08].

2.3.4. Other Applications

In addition to the topics presented here, there are many other possible applications for BCIs. For example, the use of BCI control in military and industrial contexts has been proposed [Tan10]. Furthermore, there are approaches to make brainwave measurements commercially viable, especially in marketing. The field of neuromarketing could provide more accurate information about user preferences than traditional market research studies and could be quantified by measuring brain response [Ari10]. There are already several companies offering neuromarketing services.

2.4. Exemplary mobile Hardware for Brain-Computer Interfaces

This section provides an overview of hardware that can be used for mobile EEG-based BCIs. At the same time, a metric for evaluating mobile EEG devices is presented.

Many mobile EEG recording devices exist today, including commercially available ones. These devices are usually suitable for signal acquisition, but do not provide embedded signal processing capabilities on the mobile platform. Instead, they are designed to send the recorded data via a wireless interface (e.g. Bluetooth Low Energy) to another hardware and rely on the processing there.

Twenty-nine published research studies related to mobile EEG are reviewed in [Bat17]. Based on this review, the authors developed a scoring system to evaluate different parameters and requirements of such a system. Figure 2.10 summarizes the four proposed categories, which are explained below. For all of them, a higher score is considered better.

The "Device Mobility Score" (D) describes the extent to which the use of the system physically restricts the user and includes the location of the device. This score is given on a scale of 0 to 5, with 0 representing no mobility (e.g., cable-based) and 5 representing a fully head-mounted solution with no additional equipment required.

Next, the "Participant Mobility Score" (P) is used to consider the extent to which actual participant mobility was endorsed in the reviewed EEG studies. Also on a scale of 0 to 5, a score of 0 corresponds to a study in which participants were expected to stand, sit, or lie down at complete rest. A value of 5, on the other hand, represents unrestricted running and potentially extensive physical activity. As noted in [Bat17], none of the studies considered achieved a score of 5 in this category, and the maximum score achieved was 4.

The "System Specification Score" (S) evaluates the technical specifications of the EEG recording system used. This includes the resolution and sampling rate of the analog-to-digital conversion, as well as the battery life of the data acquisition module. Additionally, the electrodes used are considered, with active, shielded and gel-based electrodes being rated as the best. Overall, the value for S can reach a maximum of 20.

	Section 1: Device Mobility Score (D)		**Section 2: Participant Mobility Score (P)**
0	All equipment off-body mounted and participant tethered via cabling to EEG acquisition equipment.	**0**	Lying, sitting or standing still.
1	Waist-mounted (or back-mounted) with additional equipment located in a rucksack.	**1**	Lying, sitting or standing with localised movement.
2	All equipment is waist-mounted.	**2**	Constrained walking/cycling.
3	Head-mounted EEG system, with additional equipment located in a rucksack or off-body.	**3**	Unconstrained walking/cycling.
4	Head-mounted and requires smartphone/tablet.	**4**	Walking and carrying, climbing stairs, constrained running.
5	Head-mounted and does not require any additional equipment.	**5**	Unconstrained running, vigorous physical exercise or sport.

Section 3: System Specification Score (S)

	Bit resolution (bits)	Sampling rate (Hz)	Battery Life (Hrs)	Electrode Type			
1	14	125 or 128	Mains, USB or equivalent	Passive (0)		Active (1)	
2	16	250 or 256	1 to 8	Unshielded (0)		Shielded (1)	
3	22	500 or 512	9 to 16	Dry (1)	Wet (2)	Gel (3)	
4	24	1000 or 1024	17 to 24				
5	>24	>1000	>24	**Electrode Score**			
	+	+	+			=	(S)

Section 4: Number of Channels: **(C)**

Figure 2.10: *Scoring system for mobile EEG platforms (adapted from [Bat17])*

Finally, the number of channels of the system provided and used in the study is also taken into account under "Number of Channels" (C). The corresponding value refers to the actual signal channels, and usually two additional electrodes are added for reference and ground.

The values for D, S, and C are primarily related to the hardware system used. The value for P, on the other hand, depends primarily on the study performed. Overall, the scoring system does not take into account the processing capacity of the individual system.

Table 2.8 summarizes the actual scores for each category of publications considered in [Bat17]. The rows are sorted in ascending order according to the device mobility score. It can be seen that most of the studies already rely on wired or off-body solutions. Less than half have a head-mounted recording system that requires additional equipment. And only two studies require only a small additional device such as a smartphone. There is no study reviewed that relies on a completely self-contained mobile device.

Similarly, the value for P is mostly low, meaning that the subjects did little or no movement during the study. However, the values for S and C are more spread out. The values for S range from 6 to 17 out of a maximum of 20 points. The number of channels ranges from 1 to 248.

Table 2.8: *Scores for all categories and all twenty-nine considered research studies, sorted by device mobility score D (adapted from [Bat17])*

EEG system	Considered study	Device mobility score (D)	Participant mobility score (P)	System specification score (S)	Number of channels (C)
ActiveTwo-1	[Dav07]	0	0	16	32
ActiveTwo-2	[Gra10]	0	2	15	248
ActiveTwo-3	[Gwi10]	0	4	15	248
ActiveTwo-4	[Mai14]	0	1	17	32
ANT-1	[Cas11]	0	2	13	32
ANT-2	[Duv13]	0	2	15	128
asalab	[Ehi14]	0	2	16	128
BrainAmp-2	[Wag12]	0	2	17	120
V-Amp	[Zan17]	0	1	13	16
actiCHamp	[Bul14]	1	2	16	64
BrainAmp-1	[Jun16]	1	1	15	156
BrainAmp-3	[Was14]	1	4	16	28
Polymate AP216	[Lot09]	1	3	15	3
Mobita	[Ask14]	2	4	17	32
Penso	[Gar08]	2	1	7	8
Profusion	[Fit13]	2	1	11	32
Varioport	[Dop12]	2	3	13	10
B-Alert	[Rob15]	3	2	10	20
Cognionics	[Lin14b]	3	2	11	10
EPOC-1	[Asp15]	3	3	6	14
EPOC-2	[Klo13]	3	1	6	14
MindWave-1	[Liu13]	3	1	10	1
MindWave-2	[Won14]	3	1	10	1
NuAmp	[Wan14]	3	1	10	32
Oldenburg Hybrid-1	[Deb12]	3	3	8	14
Oldenburg Hybrid-2	[De 14]	3	0	8	14
SMARTING-2	[Zin16]	3	3	12	24
EPOC-3	[Sto14b; Sto14a]	4	0	6	14
SMARTING-1	[Deb15]	4	0	12	16

The two studies with the highest values for D of 4 are discussed below. The computing power available for EEG signal processing is also taken into account. Both studies avoided movement during recording and have a moderate number of EEG channels.

In [Deb15], an indoor EEG study was performed with seated subjects. EEG signal acquisition was performed using the Smarting EEG system, which sent the sampled data via Bluetooth Low Energy (BLE) to a smartphone. Additionally, the smartphone was used to provide an auditory stimulus to determine the resulting ERPs. However, all signal processing did not take place on either the signal acquisition device or the smartphone. Instead, the recorded EEG signals were processed offline on a Personal Computer (PC).

The other study with a score of 4 for category D also uses a mobile EEG recording system that sends data to a smartphone via BLE [Sto14a; Sto14b] . In this case, however, the EEG signals are processed on the smartphone itself. The goal of this processing is to localize the source of the brain activity and to display it on the smartphone's screen. Furthermore, a stimulus can be provided via the smartphone in order to visualize the effects on the brain activity.

Although both studies have the same device mobility score, they differ greatly in the platform for the signal processing described. For a mobile BCI with an equivalent or higher device mobility, all signal processing would have to be embedded. For this reason, some solutions for embedded signal processing in the context of BCIs are discussed below.

In [Bel21], publications on explicitly embedded hardware for BCI-related signal processing are reviewed. A total of 47 papers are considered. The focus is on BCI applications for pathological analysis and functional replacement. Other application areas such as communication or recreation are considered out of scope.

A limitation of this review is that only the hardware platform for signal processing is considered and not the signal acquisition. In addition, the publications do not distinguish whether the processing hardware is truly mobile or, for example, part of a stationary development board that communicates with a PC via a cable. The remaining hardware components required for a BCI implementation (e.g. signal acquisition) are also not described in most of the publications.

For this reason, the 47 papers considered were evaluated with respect to their device mobility. The scoring system shown in Table 2.10 was applied. However, systems consisting of a head-mounted EEG system with additional hardware up to the size of a smartphone were also assigned a value of 4 for the device mobility score (D). The scoring neglected the actual application as well as the application interface, as this is not part of the processing required for the BCI.

Using these criteria, 8 of the 47 publications considered in [Bel21] were identified that describe an EEG-based BCI system with a device mobility score of at least 4. These are summarized in Table 2.9.

The table describes the algorithms implemented on the processing platform of the eight publications considered. Additionally, the used channel number (Chan.), sampling rate (samples/s) and resolution (Res.) of the EEG signal recording are given. The last three columns show the respective power dissipation according to [Bel21] and the two calculated scores for device mobility (D) and system specification (S). Since the values for P could not be determined for all publications and, as already described, they are primarily study-dependent and not hardware-dependent, they were neglected.

In some cases, the publications do not specify whether the full resolution or sample rate of the EEG acquisition module was used for processing. In addition, when battery capacity or runtime

Table 2.9: *Embedded processing hardware for EEG-based BCIs (adapted from [Bel21])*

Work	Algorithm	Proc. Platform	Chan.	samples/s	Res.	Power [W]	D	S
[Kar17]	FFT, PSD, Threshold	ARM Cortex-M4	2	512	24	0.091	5	11
[McC17]	Filters, Threshold	Arduino Due	4	240	12	1	5	9
[Lin14a]	FFT	Tablet	1	512	12	12	4	6
[Lin16]	FFT, Threshold	Tablet	2	512	12	70	4	6
[Tse15]	FFT, Threshold	Tablet	8	512	12	4	4	10
[Jia12]	Threshold	Smartphone	1	512	12	~ 6	4	7
[Ram19]	Filter, DWT, FFNN	Raspberry Pi 3B	1	250	24	5.77	4	9
[Shy10]	Phase Coding, FFT	FPGA (EP2C20Q)	1	8,000	12	~ 27	5	10
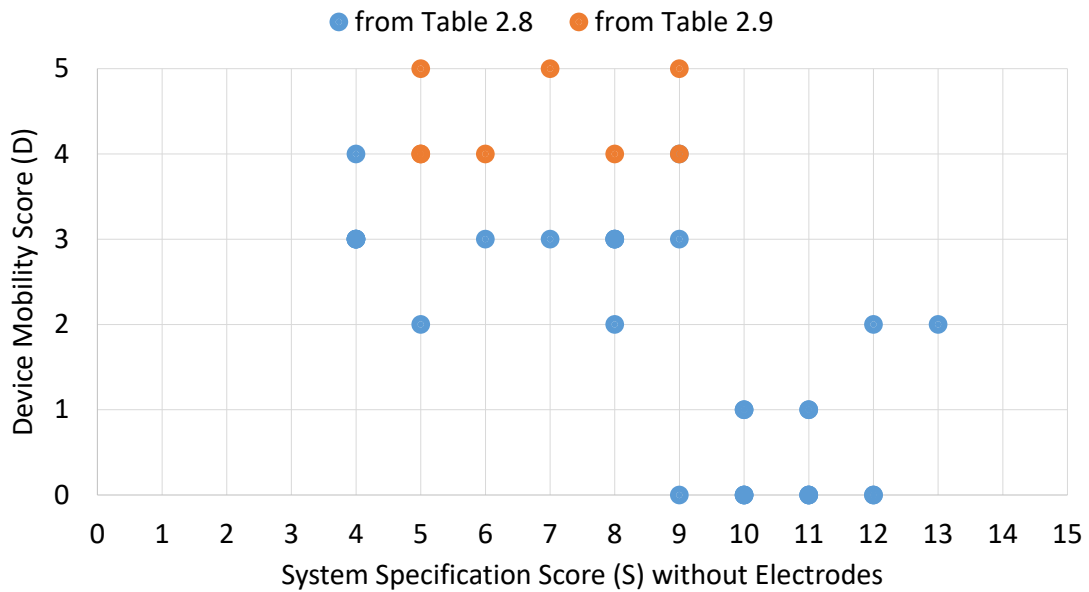
Figure 2.11: *Distribution of the examined systems from the publications with respect to their scores for Device Mobility (D) and System Specification (S)*

was not specified, a 3.7 μV 2000 mA h battery was assumed to be used to determine the value for S.

Table 2.9 is sorted by the type of processing platform used. The first two entries are based on relatively simple microcontroller architectures (ARM Cortex-M4 and Arduino Due). Rows 3-6 use a consumer smartphone or tablet. The penultimate line is based on a four-core microprocessor (Raspberry Pi 3B), and the last entry is the only one to use an FPGA as processing hardware.

Overall, there are significant differences between the publications in terms of processing power. Similarly, the power dissipation of the systems ranges from 91 mW to 70 W.

Compared to Table 2.8, the number of EEG channels used also differs, in some cases very significantly. For the embedded architectures, the largest number of channels supported is 8, and in most cases it is only 1 or 2 signal channels.

Finally, the distribution of values for S and D for all publications from Tables 2.8 and 2.9 is visualized in Figure 2.11.

For this purpose, all values for S were recalculated to remove the influence of the EEG electrodes used. There are two reasons for this. On the one hand, the electrodes used in almost all systems are easily interchangeable, so that their influence on the system specification score could also be interpreted as study-dependent. On the other hand, it is generally not possible to make a clear statement about which sensor version is better. For example, dry signal electrodes (score contribution of 1) also have some advantages over gel-based electrodes (score contribution of 3), such as long-term stability or wearing comfort. Consequently, the new theoretical maximum for S with this change is 15.

The complete revised table with the values used for S and D can be found in Appendix A Table A.1. As can be seen in Figure 2.11, there are a few fully mobile platforms ($D = 5$). However, these are comparatively limited in terms of system specification, i.e. resolution, sampling rate, and battery life (maximum $S = 9$). However, all of the better platforms based on these characteristics ($S > 9$) have low device mobility scores ($D \leq 2$).

Field Programmable Gate Arrays for Mobile EEG Signal Processing

This chapter discusses the target hardware for mobile processing of EEG signals in the context of a BCI. A suitable hardware architecture depends on various parameters and requirements of the respective application. For the mobile BCI system in focus of this thesis, an FPGA is used as the central component of the digital signal processing.

Section 3.1 explores the available design space of suitable hardware architectures. The hardware options are briefly characterized with respect to their features, advantages and limitations. Based on this, Section 3.2 describes some basics of FPGAs in more detail. It also discusses different ways to store the FPGA configuration, i.e. Static Random-Access Memory (SRAM) and Flash memory. Finally, Section 3.3 gives an overview of state-of-the-art FPGA implementations of BCI algorithms.

3.1. Design Space of Architectures for Digital Signal Processing

The design space exploration should identify suitable hardware architectures. In the context of this work, this is an architecture for processing digital EEG signals within a BCI system.

Figure 3.1 summarizes the available options in the design space. It includes categories ranging from processors with operating systems to fully dedicated hardware [Blu08]. The coordinate system visualizes the trade-off between platform flexibility and power efficiency when executing a target algorithm. The more specialized the hardware, the higher the performance, but at the same time, the higher the implementation overhead for integrating an algorithms.

The General Purpose Processor (GPP) is the most flexible platform, but also the most power consuming. It is designed to run arbitrary code and is usually supported by an operating system. The most common GPPs are PC processors from AMD and Intel.
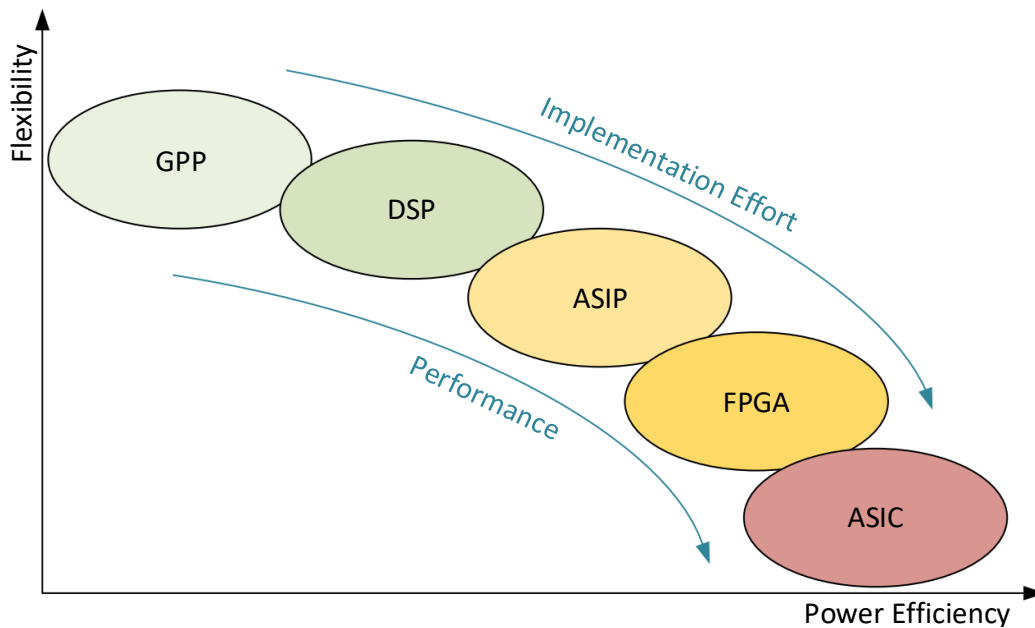
Figure 3.1: *Processing hardware design space with included tradeoffs (adapted from [Blu05; Blu08])*

The Digital Signal Processor (DSP) is a specialized microprocessor with dedicated accelerators for a particular type of digital signal processing. It is optimized for online processing. Examples of applications include audio or video signal processing.

In the case of an Application-Specific Instruction-Set Processor (ASIP), the hardware of a GPP architecture is extended to perform specific applications or calculations in an accelerated manner. One way to do this is to implement a coprocessor with specific instructions that are regularly called by an application and would otherwise take a long time to execute.

An FPGA is a programmable array for hardware emulation. It is based on a regular array of logic blocks. After configuring these blocks, the FPGA can perform a variety of different functions with custom timing characteristics. A more detailed description of FPGAs is given in Section 3.2.

An Application-Specific Integrated Circuit (ASIC) is a dedicated hardware implementation that is specifically tailored to the requirements of a particular application. It is the most powerful and power efficient option for implementing an algorithm, but the hardware is very inflexible. Extending functionality, such as adding a new type of computation, usually requires a costly and time-consuming redesign of the hardware.

In the context of this work, FPGAs are explicitly chosen for online signal processing of digital EEG signals. For the signal processing hardware of a fully mobile BCI, power consumption is of particular importance [Bel21]. At the same time, it is necessary that the performance provided by the hardware is fast enough for online computation of specified algorithms. However, the signal processing supported by the platform should still be adaptable on demand and not be limited to a fixed list of functions. For this reason, the FPGA represents a suitable compromise with good features, including basic adaptability. Since an adaptation of the algorithmic processing steps is not expected on a regular basis, an increased implementation effort of the algorithms is accepted.
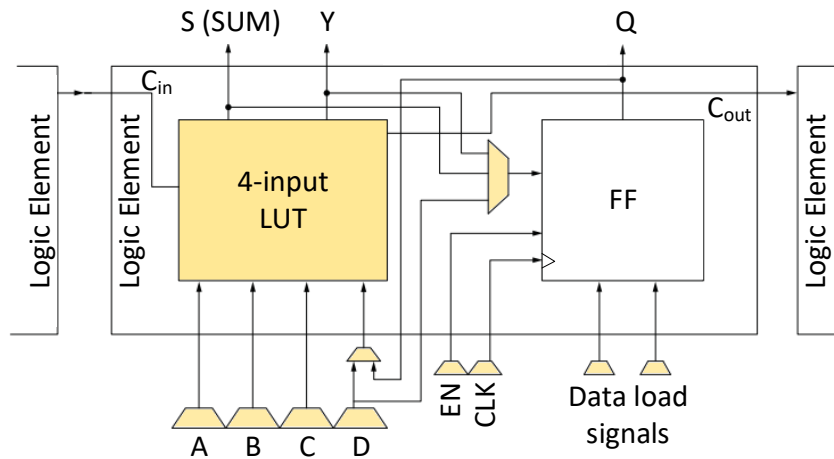
Figure 3.2: *Simplified structure of an FPGA logic element. Components highlighted in yellow are configurable. (adapted from [Mic19])*

It should be noted, that besides pure FPGAs, there are also some Systems on a Chip (SoCs) that combine an FPGA with a microprocessor in one package. These heterogeneous hardware architectures allow for partially high-level language programming in addition to the full functionality and reconfigurability of the integrated FPGA.

3.2. Fundamentals of Field-Programmable Gate Arrays

The FPGA consists primarily of a regular array of many identical logic blocks that can be configured. Depending on the manufacturer, this smallest hardware structure is called differently. In the context of this work, the term logic element is used uniformly.

The structure of an Logic Element (LE) is shown in Figure 3.2. It always contains a Lookup Table (LUT) and a Flip-Flop (FF). The additional multiplexers can be used to connect or bypass the inputs and outputs of the LE in different ways. The LUT is used to convert purely logical connections of its inputs. The LUT shown in the figure can logically link up to four inputs, although the number may vary slightly depending on the particular FPGA. The FF is used to cache individual signals and to map the temporal behavior in the FPGA.

Dedicated functions are also available to implement a hardware adder. The word width of the adder's inputs within an LE depends on the number of inputs of the LUT. In Figure 3.2, a 4-bit adder can be implemented per LE. To increase the word width efficiently, LEs can be cascaded using dedicated signal lines (C_{in} and C_{out} in the figure).

All components highlighted in the figure are configurable. Furthermore, the connections of the many logic elements to each other and to the input and output pins of the Integrated Circuit (IC) are also programmable. To define the desired functionality and timing of an FPGA, it is first described in a hardware description language, such as VHDL or Verilog. This description is then translated into a bitstream using a synthesis tool and loaded into the FPGA. The bitstream defines the function of all the configurable components contained in the FPGA IC, allowing real-time execution of the originally described hardware.
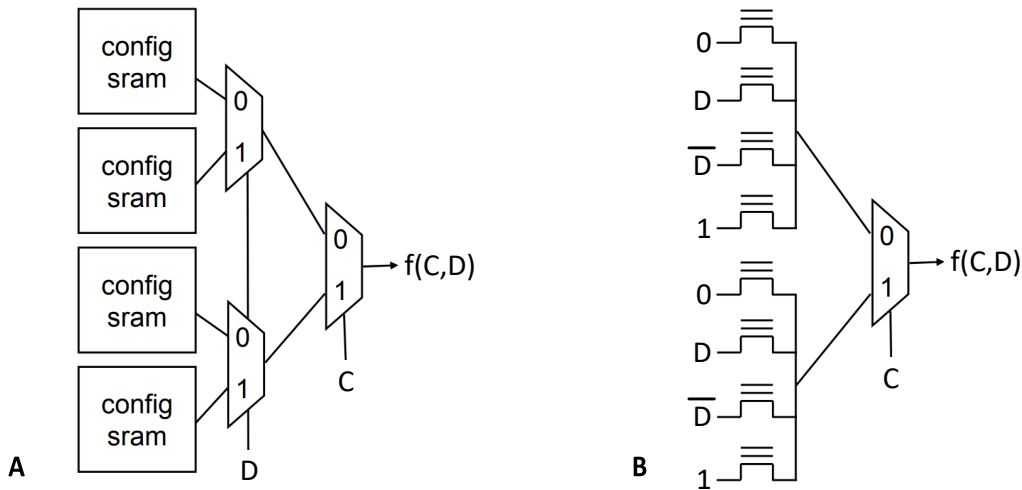
Figure 3.3: *Lookup table implementations based on SRAM (A) and Flash memory (B) (adapted from [Gre11])*

In addition to the described logic elements, modern FPGAs also contain a certain amount of data memory and dedicated hardware modules for efficient implementation of frequently occurring functions. For example, special modules are available to generate different clock rates to supply certain circuit parts on the FPGA. This allows different parts of the FPGA to be used with different clock rates simultaneously. In addition, hardware multipliers are often included that can also multiply signals of higher bit widths within one clock cycle.

As of 2019, according to Gartner (2019, as cited in [HPC19]), the two largest companies in the FPGA market are Xilinx and Intel, followed by Microchip (formerly Microsemi).

3.2.1. Comparison of Configuration Memory

The configuration information of an FPGA, from the LE (see yellow components in Figure 3.2) to the chip-wide signal routing, must be stored. The most common approaches are SRAM-based FPGAs, which use an SRAM cell at the respective location to store the configuration. However, there are also approaches based on Flash memory, with Microchip's products being particularly noteworthy.

Figure 3.3 shows the basic structure of a LUT in both technologies. For clarity, only two inputs (C and D) are considered. On the left side, a configuration of the LUT is stored in four SRAM cells, which can then be passed through the multiplexers controlled by the two inputs to the output ($f(C,D)$). On the right side you can see the realization of such a LUT with eight Flash memory cells. One input D can be routed directly through these cells, so that in the second stage only one multiplexer controlled by the other input C is needed.

A key difference between the two memory technologies is the volatility of the stored information. SRAM is a volatile memory, meaning that the stored information must be rewritten to the memory cells each time the device is powered on. Flash memory, on the other hand, is non-volatile, and therefore the stored data is retained even when the power is turned off.

In terms of the characteristics of FPGAs based on them, this means that Flash FPGAs have the advantage of being immediately usable when powered up [Pan17]. With SRAM, the

complete design must first be reloaded into the FPGA before it is ready for use. For this purpose, such FPGAs often use an additional non-volatile Electrically Erasable Programmable Read-Only Memory (EEPROM), from which the configuration is transferred to the SRAM cells of the FPGA during the power-on process of the IC. Nevertheless, this process takes time and power, so the desired FPGA functionality is not immediately available.

Moreover, Flash memory FPGAs consume less power than SRAM approaches [Pan17]. However, the manufacturing processes for the more widely used SRAM-based FPGAs are more advanced, resulting in higher logic gate densities. As a result, these FPGAs often have more integrated LEs and more embedded memory than flash-based variants.

In general, when choosing a suitable FPGA, a trade-off must always be made between characteristics such as the number of hardware resources required or the power budget.

3.3. Field Programmable Gate Arrays for Brain-Computer Interface Algorithms

In this section, an overview of exemplary FPGA implementations of BCI-related signal processing is given.

Relevant state-of-the-art implementations are summarized in Table 3.1. The entries are sorted by the function or application of the algorithm. These are partially abstracted to facilitate easier overview and comparison. Furthermore, the particular use case is not intended to be determinant for this comparison. The group "Flexible" includes all types of recurrent, feedforward or convolutional Neural Networks (NNs). Although some publications describe a specific use case or the dataset used for evaluation aims at a specific classification, NNs can be generally trained for other cases without affecting the required hardware architecture. Therefore, they are grouped together.

The Algorithm column gives a more detailed description of the algorithm implemented on the FPGA. Entries separated by a "-" indicate multi-level processing. For example, many other entries also include certain preprocessing steps in their signal processing chain. The few entries with brackets are used to distinguish between multiple implementations within one publication.

The columns "Chan." and "Res." refer to the number of electrode channels and their bit width/resolution given in the publications (if specified). For the channels, the reference and ground electrode were uniformly not counted. It can be seen that significantly higher numbers of channels are used for neural network based processing. However, with by far the largest channel counts of 1,059 and 10,0000 respectively, it should be noted that these entries either only consider simulated electrodes [Hee18] or are based on invasive electrodes [OUc22]. Suppressing all flexible function rows results in an average used channel count of 8.83 electrodes. For the used resolution of the processed data, the average value is 15.875 bit. The overall resolution is significantly less spread out and ranges from 10 bit to a maximum of 24 bit.

The exact type of the FPGA used in the publication is shown in column "FPGA". A total of six entries starting with "EP2", "EP4" or "5CE" are Intel FPGAs. The remaining 17 entries are all Xilinx FPGAs and FPGA-based SoCs.

Table 3.1: *FPGA implementations for BCI-related algorithms*

Function	Algorithm	Chan.	Res.	FPGA	#LE	Source
Preproc.	Filter	1	16	EP2C35F	24	[Has19]
Preproc.	Filter - Adaptive filter	14	14	XC6SLX9	324	[Dut18]
Preproc.	Floating Point operations	1	16	Virtex7-690T	417	[Lib18]
ERP	Filter - LDA	7	-	Spartan 3E	11,033	[Khu12]
SSVEP	CCA	4	24	5CEBA4F23C7N	4,544	[Kar20]
SSVEP	Filter - Phase Identification	1	12	EP2C20Q	4,952	[Shy10]
SSVEP	FFT - Butterfly - Maximum	1	-	XC7A15T	10,400	[Lin21]
SSVEP	Filters - MSE	1	12	EP2C20Q	15,606	[Shy13]
SSVEP	Filter - CCA	8	-	EP4CE115	31,800	[Byu19]
ERD/ERS	Filters - CSP - LDA	22	-	EP4SGX230	17,281	[Kai14]
SMR	SCSSP - LDA - SVM	14	20	XC6VLX240T	11,311	[Mal18]
Flexible	CNN	59	16	Zynq7020	1,716	[Ma19]
Flexible	CNN	64	24	XC7K325T	2,724	[Fen22]
Flexible	CNN	64	16	XC7Z010	4,937	[Her21]
Flexible	CNN	-	-	XC6SLX9	≤ 5,720	[Sai22]
Flexible	MLP NN (no DSP)	72	16	XC7VX485T	285,555	[Shr18]
Flexible	MLP NN (DSP)	72	16	XC7VX485T	8,704	[Shr18]
Flexible	LSTM	22	-	XC7A200T	24,064	[Yoo22]
Flexible	LSTM (Zero-weight aware)	22	-	XC7A200T	34,424	[Yoo22]
Flexible	CNN	62	16	XCZU7EV	97,205	[Flo22]
Flexible	LSTM NN	10,000	12	Zynq-ZU15EG	177,286	[Hee18]
Flexible	CNN	1,059	10	XCVU9P	1,002,783	[OUc22]
Supportive	Communication Network	32	14	XC7Z045	≤ 55,940	[Zho21]

It should be noted that not all the information given in the publications is unambiguous throughout and has been extracted and transferred to the table to the best of my knowledge. Here, some values already had to be partially converted for the values given in the table. At the same time, it is to be expected that many of the data on hardware resource utilization can still be significantly optimized, at least under certain boundary conditions. Some publications also explicitly point this out.

The column "#LE" refers to the number of used LEs in the described implementation. If the actual hardware resource usage is not specified, the maximum number of available logic elements of the FPGA is listed and marked with a prefixed "≤". It can be seen that the number of LEs used varies greatly.

"Source" refers to the publication from which data for the corresponding row were extracted. The focus of most of the publications considered here is explicitly on signal processing in the FPGA. Therefore, pre-recorded or publicly available data sets are often transferred to a corresponding FPGA board for processing and usually no actual complete BCI application is described.

The entries in this table, and in particular the specified LE usage, are used in Section 4.2.1 as a basis to estimate the resources required to select a suitable FPGA for a mobile BCI system.

It should be noted that comparing the hardware resources of an FPGA vendor is already non-trivial, and dedicated metrics can be created for this purpose [Hes21]. Therefore, abstractions and simplifications must be accepted when comparing different FPGAs from different vendors.

The CereBridge Hardware System for Mobile Online EEG-Signal Processing

The basic idea of the developed and researched hardware system is to provide a flexible and efficient solution for mobile EEG signal processing in the context of BCIs. The signal flow of such a BCI can be, as described in Chapter 2, roughly divided into the recording and digitization of EEG signals, the subsequent (pre)processing as well as automatic interpretation of the digital EEG data, and finally the handling of the processing results (e.g. generating control signals for other devices). As shown in Figure 4.1, partially mobile approaches exist, in which signal acquisition is implemented on mobile hardware, while the entire processing of these signals takes place on a stationary or at least locally separated platform (compare to 2.4, this applies to all platforms with Device Mobility Score ≤ 5). However, the interface of these two parts is usually based on a wireless connection, which add additional latency to the signal path [Wöh17]. Furthermore, only a fully mobile and autonomous system can meaningfully address all possible application scenarios independent of additional hardware. Therefore, the CereBridge system should include the complete signal flow of a BCI within its dedicated mobile hardware, while still providing high quality system features.

This chapter describes the design process and underlying decision making for the CereBridge system and starts in section 4.1 with the definition of the main requirements and scope of desired functionality. Based on this, the essential components for such a system (e.g. FPGA) will be discussed in section 4.2 and an appropriate one will be selected in each case. Section 4.3 describes how the CereBridge system was partitioned and how its individual layers were designed. Finally, in section 4.4, a summary of functional range, interaction options, interfaces provided and the most important parameters of the complete system hardware-wise is presented.
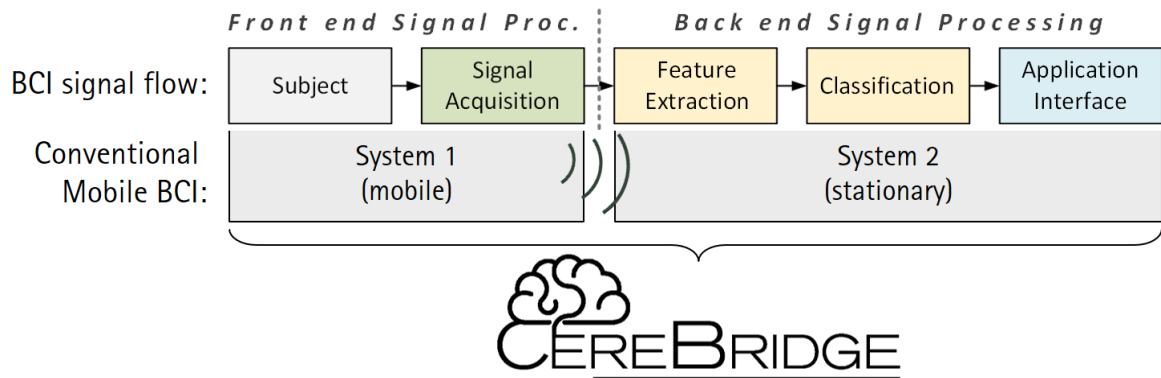
Figure 4.1: *Signal flow for stationary and partially mobile Brain-Computer Interfaces*

4.1. Requirements and Constraints

In order to ensure effectiveness and practicality for the CereBridge system as a mobile online BCI platform it is crucial that the design process is guided by several requirements and constraints. For clarity, these are defined in bullet point terms below, and possible relationships with design decisions are discussed.

- Interchangeable EEG sensors with at least 16 channels:

  As described in 2.1.2, many types of EEG sensors exist. They may differ in number of electrodes, form factor and specific brain areas. The system should allow to be modified for connection of different EEG sensor variants to ensure its flexibility and allow researchers and developers to choose the appropriate sensors for different applications. Based on potential EEG sensors as summarized in Table 2.3, at least 16 channels excluding reference and ground should be supported. This would allow complete connection of all sensors listed in the table except the fEEGrid. Furthermore, this value exceeds the capabilities of all fully mobile reference systems with embedded signal processing from Table 2.9. As all mentioned application-specific EEG sensors are passive, an ADC to enable their use should be provided.

- Configurable processing hardware architecture:

  For the processing of the EEG signals an FPGA will be used. The ability of reconfiguration enables the processing architecture to be adapted and optimized to a wide range of algorithms commonly used in BCI applications. Nevertheless, for estimating a reasonable number of desired hardware resources for the FPGA, existing algorithm implementations and their resource usage needs to be considered and will be discussed in 4.2.1.

- Self-sufficient operation:

  The CereBridge system must be autarkic, meaning that it can operate independently without a host or other external device. As a prerequisite, initialization, parameter setting and configuration of system's components must be carried out within the system. This requirement supports its applicability in various environments and situations, such as during outdoor activities or in remote locations. It is worth noting, that self-sufficiency does not imply that no communication with the outside world is possible. However, this should be entirely optional and chosen based on the application.

- Mobility:

    This requirement ensures the system to be usable in various environments and situations, i.e. for application scenarios outside of laboratory studies. Hence, the overall system should be effortlessly wearable, which presuppose a small form factor and low weight. Besides this being aspects to be considered for the physical design and layout of the system on its own, this also implies a low power consumption, since the size of a battery can significantly impact the dimensions and mass of a mobile hardware system. Regarding the weight of the system, 300 g is targeted as upper limit, because over-ear headphones are in this range as well [Gmba; Gmbb] and can be considered to be worn comfortably on the head.

- Low power consumption:

    As a mobile system, the CereBridge hardware needs to rely on a battery as a power source. Consequently, it should have a low power consumption in order to achieve a long battery life. This also needs to be considered beyond the system hardware design, as algorithms should be implemented with regard to their energy efficiency as well. Without any actual signal processing, the target runtime for continuous EEG signal acquisition and without the necessity to recharge the battery is 16 hours, which can be considered a full day without sleeping. Moreover, the power required by the complete system should not exceed 1 W in average, as this is considered a good value according to [Bel21].

- Throughput and latency considerations:

    Typical sampling rates (f_s) of EEG signals are up to 1 kHz, with continuous sampling for longer periods of time. As the system will be used to process this incoming data in real-time, it must complete all computations for a sample set (samplewidth x channels) within the time frame $1/f_s$. In addition, the latency from input sampling to processing result needs to be considered also, although the tolerable latency is highly dependent on the actual algorithm and application. As some of the information contained in EEG signals can last hundreds of milliseconds, it is not usually the most determining factor for a system design. Nevertheless, the system should be configurable to achieve low-latency implementations if desired and, more importantly, must provide measures to specify the latency for a given algorithm. However, with EEG signals containing most of the information in a frequency range up to 80 Hz (compare [Con05]), the need for a latency lower than 100 ms is improbable and will be taken as a general guideline.

- Unified hardware:

    When developing algorithms for BCIs, pre-recorded EEG data sets are typically processed offline first. Afterwards, potential approaches might be transferred to online processing in order to conduct studies in laboratory environments. Ideally, the investigated and evaluated algorithms can be transferred on the same hardware architecture to other application scenarios, even outside the laboratory. The CereBridge system should provide a unified hardware platform for all the steps during the evolution of an algorithm up to the actual application. In addition to practicality, this approach also supports predictable processing results, when the EEG signals used for the software reference were recorded on the same hardware as the final BCI implementation.

- Extensibility:

  Because applications and their requirements can vary widely, the hardware system should be extensible. This should include options for connecting new modules as well as a variety of supported communication protocols and interfaces used to communicate with them (e.g. Serial Peripheral Interface (SPI), Universal Asynchronous Receiver-Transmitter (UART), Inter-Integrated Circuit (I2C), Media-Independent Interface (MII)). This flexibility also makes it easier to integrate the CereBridge system with other electronic devices whose hardware may be more fixed.

- On-board memory options:

  The system shall include memory ICs. For pure data storing, a non-volatile memory (e.g. flash memory) is required. To support applications that require regular reading from memory, such as larger parameter sets or reference data, an additional memory with faster access time would also be beneficial.

- User interaction:

  Even though an ideal BCI platform should not require any user interaction, having this option might be advantageous in some scenarios. Programmable buttons can help with turning the processing on and off or for mode switching. This can also increase the ease of use, especially during testing and debugging scenarios. Additionally, programmable LEDs shall be included to indicate the current state of the system. In any case, the required user interaction should be kept minimal by default, ensuring that the system can be easily used by researchers and developers with minimal training. Additional options for user interaction should not be part of the core system but could be integrated on an extension module if needed.

- Reproducibility:

  The hardware system should be reproducible, also for other research groups. For this reason, it should be based exclusively on commercially available components.

4.2. Definition of Essential Components

Once the boundary conditions for a mobile BCI system have been clarified, its key components will be defined and selected. Each of the component type discussed below will have a significant impact on the system design and must fulfill the applicable constraints. Their early definition support a holistic understanding of the overall system and also influence some later design decisions due to interdependencies. This section provides a detailed description of each of these essential components, their role in the system, and their design considerations. Possible trade-offs involved are also being discussed. In cases where this process affects the selection of other components, these are briefly described as well.

4.2.1. Field-Programmable Gate Array

An FPGA will be used as the main hardware architecture for the digital signal processing. As the dedicated IC for signal processing, all other components of the signal flow will be connected

Table 4.1: *Normalized resource usage of exemplary FPGA implementations for BCI-related algorithms from Table 3.1*

		Referen	ced FPGA	-based BCI	systems		#LE N	ormalizat	ion
ID	Source	Chan.	Res.	FPGA	IpL	#LE	C	I R	n.#LE
1	[Has19]	1	16	EP2C35F	4	24	x		384
2	[Dut18]	14	14	XC6SLX9	6	324	x	x x	635
3	[Ma19]	59	16	XC7Z020	6	1,716		x	2,574
4	[Fen22]	64	24	XC7K325T	6	2,724		x x	2,724
5	[Kar20]	4	24	5CEBA4	4	4,544		x	3,030
6	[Shy10]	1	12	EP2C20Q	4	4,952		x	6,603
7	[Her21]	64	16	XC7Z010	6	4,937		x	7,406
8	[Sai22]	-	-	XC6SLX9	6	$\leq$5,720		x	$\leq$8,580
9	[Lib18]	1	16	XC7VX690T	6	417	x	x	10,008
10	[Khu12]	7	-	Spartan 3E	4	11,033			11,033
11	[Shr18]	72	16	XC7VX485T	6	8,704		x	13,056
12	[Mal18]	14	20	XC6VLX240T	6	11,311		x x	13,574
13	[Lin21]	1	-	XC7A15T	6	10,400		x	15,600
14	[Kai14]	22	-	EP4SGX230	4	17,281			17,281
15	[Shy13]	1	12	EP2C20Q	4	15,606		x	20,808
16	[Byu19]	8	-	EP4CE115	4	31,800			31,800
17	[Yoo22]	22	-	XC7A200T	6	24,064		x	36,096
18	[Zho21]	32	14	XC7Z045	6	$\leq$55,939	x	x x	$\leq$47,949
19	[Yoo22]	22	-	XC7A200T	6	34,424		x	51,636
20	[Flo22]	62	16	XCZU7EV	6	97,205		x	145,808
21	[Hee18]	10,000	12	XCZU15EG	6	177,286		x x	354,572
22	[Shr18]	72	16	XC7VX485T	6	285,555		x	428,333
23	[OUc22]	1,059	10	XCVU9P	6	1,002,783		x x	2,406,680

to it. In addition, its contribution to the overall power consumption can be expected to be substantial and thus has an impact on the power management, especially the required supply power and the power rails. The selection process starts with an estimation of the desired number of hardware resources for the FPGA, especially its logic elements. Based on this, the ICs to be considered are compared with regard to other constraints such as their physical package size or power consumption.

In order to make a meaningful and informed decision regarding the available resources of the FPGA, i.e. primarily the number of logic elements, the existing FPGA implementations of BCI-related algorithms given in Table 3.1 will be considered. For the comparison, some simplifications and unifications needed to be applied, which will be described as follows. The resulting table with normalized logic element usage (n.#LE) is presented in Table 4.1.

The various FPGAs differ in terms of their internal circuitry, and especially in the content of the individual logic elements or logic cells. The column "IpL" refers to the inputs per LUT of the corresponding FPGA. It is therefore an indication of the level of logic complexity that
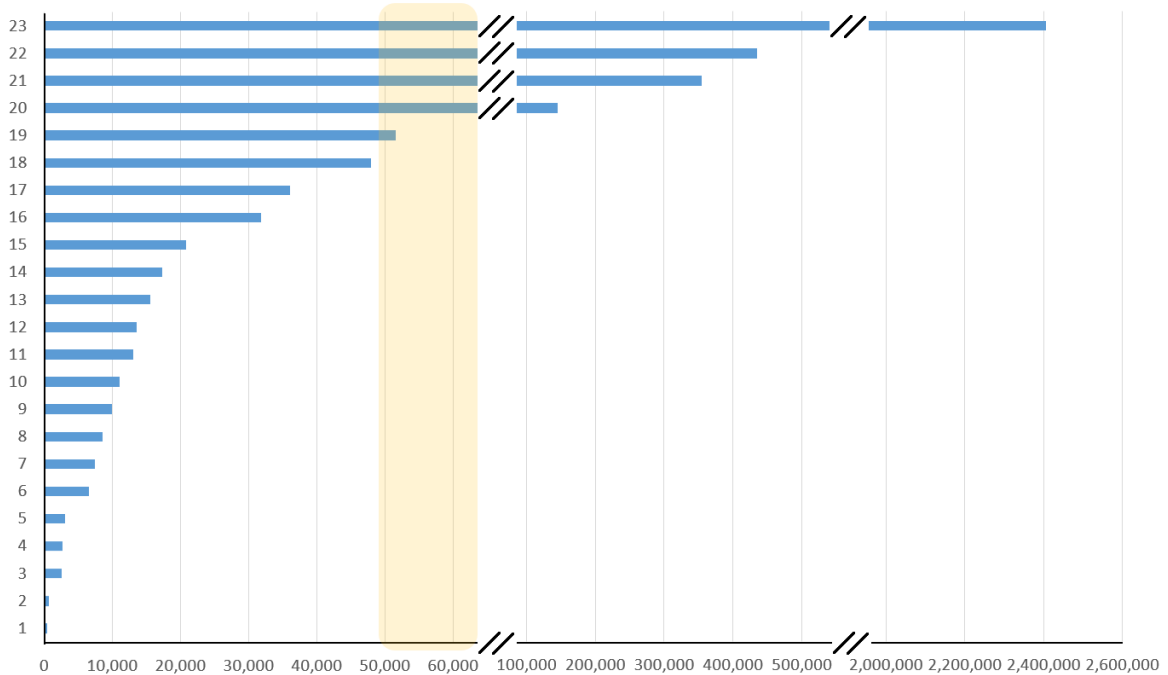
Figure 4.2: *Visualization of LUT-4-equivalent resource usage of considered publications as listed in Table 4.1. Marked area points to region of interest for FPGA selection.*

can be implemented per logic element. To make the results more comparable, they have been partially normalized with respect to the number of channels (C), the inputs per LUT (I), and the resolution of the input data (R). An "x" in the corresponding cell indicates that this normalization was applied to the LUT resource usage of the corresponding row.

Since preprocessing steps are expected to be performed on all available channels, these types of implementation were normalized to 16 channels, which meets the requirements of the CereBridge system (compare to Chapter 4.1). The inputs per LUT were normalized to the value four for all FPGA. Lastly, resolution normalization to 16 bit was applied. The resulting, normalized count of logic elements used is presented in the column "n.#LE". In all three cases, a linear scaling was assumed for the purpose of simplification.

The normalized values of LE usage are visualized in Figure 4.2. As can be seen, the results are quite polarized. For a large part of the implementations between 10,000 to 52,000 logic elements would be sufficient, while some others require hundreds of thousands and more. Hence, a desired range of 55,000 to 80,000 LEs was defined for the FPGAs of the CereBridge system. This range is sufficient for most algorithms, but not for the largest, to help reduce the overall expected power consumption. The four implementations above this marked area of interest are also rather uninteresting as a basis for comparison for the FPGA selection of the CereBridge system. The main reason is that these implementations have a rather high number of EEG channels, ranging from 62 to 10,000. With a lower amount of channels to process, the computational effort for processing them declines. On the other hand, the headroom provided with this range compared to the implementations with less resource demand is beneficial, since the resources of an FPGA can usually never be fully utilized due to the limited routing capacities. In general, if resources are not sufficient for a particular use case, the extensibility of the system could theoretically be used to outsource (partial) computations.

Table 4.2: *Possible FPGAs and FPGA SoCs in the range of 55,000 to 80,000 4-input-equivalent LUTs*

	Device	#LUT	lpL	n.#LUT	#FF	Package	Dim.[mm^2]	Node
Xilinx	Spartan 6 XC6SLX75	46,648	6	69,972	93,296	CSG484	19 × 19	45 nm
	Spartan 7 XC7S75	48,000	6	72,000	96,000	FGGA484	23 × 23	28 nm
	Artix 7 XC7A75T	47,200	6	70,800	94,400	CSG324	15 × 15	28 nm
	Zynq Artix 7 XC7Z014S*	40,600	6	60,900	81,200	CLG400	17 × 17	28 nm
	Artix UltraScale+ AU7P	37,000	6	55,500	75,000	SBVC484	19 × 19	16 nm
	Artix UltraScale+ AU10P	44,000	6	66,000	88,000	UBVA368	11.5 × 9.5	16 nm
Intel	Cyclone IV E EP4CE55	55,856	4	55,856	55,856	U484	19 × 19	60 nm
	Cyclone IV GX EP4CGX75	73,920	4	73,920	73,920	F484	23 × 23	60 nm
	Cyclone IV E EP4CE75	75,408	4	75,408	75,408	U484	19 × 19	60 nm
	Cyclone V GX 5CGXC5	29,080	8	58,160	116,320	M301	11 × 11	28 nm
	Cyclone V E 5CEA5	29,080	8	58,160	116,320	M383	13 × 13	28 nm
	Cyclone V GT 5CGTD5	29,080	8	58,160	116,320	M301	11 × 11	28 nm
	Cyclone 10 LP 10CL055	55,856	4	55,856	55,856	U484	19 × 19	60 nm
Microchip	IGLOO 2 M2GL050	56,340	4	56,340	56,340	FCS325	11 × 11	65 nm
	IGLOO 2 M2GL060	56,520	4	56,520	56,520	FCS325	11 × 11	65 nm
	SmartFusion 2 M2S050*	56,340	4	56,340	56,340	FCS325	11 × 11	65 nm
	SmartFusion 2 M2S060*	56,520	4	56,520	56,520	FCS325	11 × 11	65 nm

*SoC with additional integrated microcontroller or microprocessor

Once the target size of the FPGA has been determined, the available types from different vendors in this range is listed and compared as in Table 4.2. The portfolios of the two largest FPGA manufacturers, Xilinx and Intel (formerly Altera), were taken into account. In addition, the products of Microchip (formerly Microsemi) were also considered, since their FPGAs are flash-based.

Since many modern FPGA family use 6-input LUT instead of 4-input LUT within their logic cells, a linear scaling is assumed and therefore the desired amount of LE for those FPGAs is defined as 36,600 to 53,300. This constant scaling factor of 1.5 is a simplification and its actual value is implementation dependent. If a full logical linkage of more than four input variables is required, more than one and a half times 4-input LUT would be needed compared to an implementation with 6-input LUTs, up to a maximum of four times. This consideration therefore represents rather the best case, which conversely means that the chosen FPGA with normalized number of LUTs should always be sufficient compared to a 4-input LUT implementation. The 8-input LUTs specified for some Intel FPGAs can also be used as two 4-input LUTs according to the data sheets, which is why the search range between 27,500 to 40,000 is selected here. Similar to Table 4.1, the specified number of available LUTs is presented in column #LUT and the linearly normalized values in n.#LUT.

In the further selection process, special attention should now be paid to the power consumption, based on the established requirements. Many manufacturers provide special Excel-based tables for estimating power consumption. A large number of parameters such as the resource utilization, selected clock frequency, toggle rate of the flip-flops, etc. have to be entered into these tables. Thereupon one receives an estimation of the power consumption of this FPGA. This procedure

was applied to all FPGA and FPGA SoC types under consideration (Table 4.2). Since the actual utilization depends on the application or algorithm, the following cases were researched:

I No resource allocation: 0 LUTs and registers used (Static power consumption)

II Medium logic resource usage (based on [Shy13]): 20,808 registers and 4-input equivalent LUTs used

III Extensive logic resource usage (based on [Yoo22]): 51,636 registers and 4-input equivalent LUTs used

For all cases, the following parameters and settings have been used uniformly:

- 25 °C ambient temperature with still air

- Commercial temperature grade with no heatsink applied

- No DSP and no memory usage

- Parametric system clock frequencies of: 1 MHz, 5 MHz, 20 MHz and 50 MHz with 100 % clock enable rate

- Clock fanout set to sum of used LUTs and registers

- Global register toggle rate of 10 %

- Average logic fanout of 3

- 10 input and 10 output pins with a voltage level of 3.3 V, driven with system clock, an output load of 5 pF, output enable rate of 50 % as well as the output current drive as low as possible (2 mA to 4 mA)

- Other settings are left default

- Linear normalization for number of 6-input LUTs with the factor $1/1.5$ for applicable FPGAs

The early power estimation results are visualized in Figure 4.3 for improved comparison. The complete table with all numerical values for all FPGAs and cases studied can be found in Appendix A in Table A.2.

The colors of the curves represent the different FPGAs, while the symbols at the examined logical resource utilization values mark the respective clock frequency used for this curve. For better clarity, the values for all the FPGAs were grayed out here, which exceed dimensions larger than 15×15 mm^2. Since the package sizes of the FPGAs under consideration vary widely, the focus here is on the smaller versions. FPGAs with identical power consumption values have been grouped together, such as M2GL050 and M2S050. Furthermore, the power consumption values for the highlighted FPGAs from Intel (5CGXC5 and 5CEA5, respectively) are almost the same, which is why their representations overlap and thus cannot be visually distinguished.

It can be seen that some of the FPGAs differ significantly in their static, frequency-independent power consumption (seen at 0 MHz). In particular, the values for SmartFusion 2 and IGLOO 2 families from Microchip stand out positively, which is also plausible due to their flash-based hardware architecture. However, their gradient, i.e. the resource-dependent power consumption at a given clock frequency, is higher than the alternatives from Intel and Xilinx. This is due to the coarser technology node (65 nm) of the Microchip variants in contrast to the SRAM-based
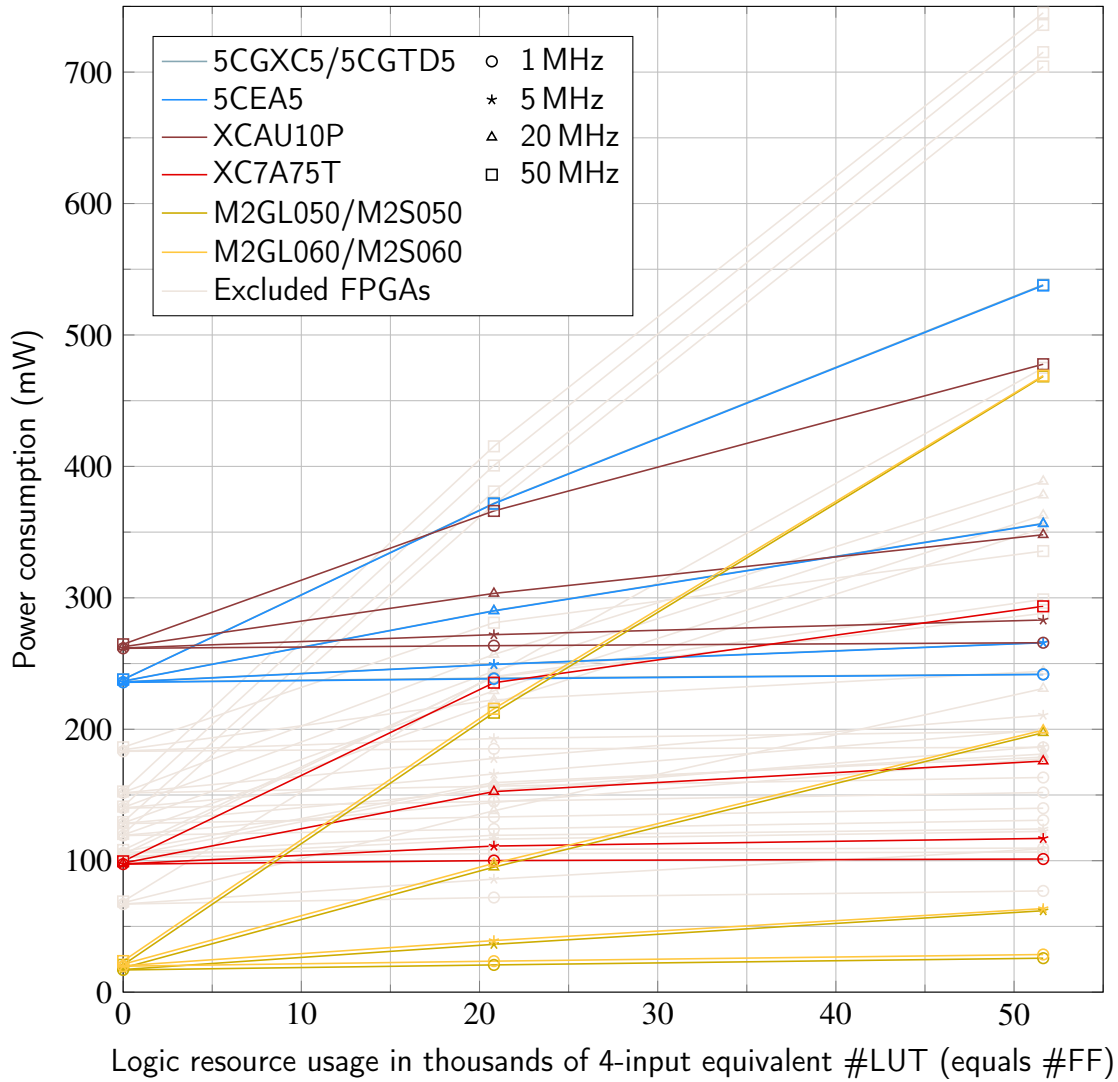
Figure 4.3: *Power consumption of various FPGAs for different logic resource usages and clock frequencies*

FPGAs (16 nm to 28 nm). In general, a smaller structure size in manufacturing leads to a reduced dynamic power dissipation.

Based on these findings, a Microchip FPGA will be used as the digital processing core in the context of a mobile BCI hardware system. They provide the lowest power consumption for lower clock frequencies or logic resource usage scenarios. Due to the comparatively low frequency spectrum of EEG signals of interest for BCI applications, the former is plausible for many use cases and algorithms. In addition, the static power dissipation is less than 20 % of the next best option in this respect, the Xilinx XC7A75T. Assuming that certain scenarios require processing that is not continuous throughout or at least certain parts of the hardware are unused in the meantime, this can have a significant impact on the overall power dissipation.

Table 4.3 summarizes the core aspects and features of the considered ICs from Microchip, according to their datasheet. Since the SoCs, i.e. SmartFusion 2, does not have any significant disadvantages, a SmartFusion 2 is to be used. The features offered are almost identical to the IGLOO 2, and according to the early power estimation with unused microcontroller, the power consumption does not differ between these two options. However, the embedded microcontroller

Table 4.3: *Detailed overview and summary of Microchip's FPGAs and SoCs under consideration*

	Features	IGLOO 2		SmartFusion 2	
		M2GL050	M2GL060	M2S050	M2S060
Logic/DSP	LUTs	56,340	56,520	56,340	56,520
	Registers	56,340	56,520	56,340	56,520
	Multipliers (18 bit x 18 bit)	72			
	Fabric Interface Controllers	2	1	2	1
	PLLs and CCCs	6			
	SPI/HPDMA/PDMA	2	1	-	-
Memory	Total Fabric SRAM [KiB]	1,314			
	eNVM [KiB]	256			
	eSRAM [KiB]	4 x 64			
	eSRAM Non SecDed [KiB]	-	-	80	80
High Speed	DDR Controllers	2	1	2	1
	DDR Bit Width	36	18	36	18
	SerDes Lanes	8	4	8	4
	PCIe End Points	2	2	1	2
Security	AES256, SHA256	1			
	RNG	1			
	ECC, PUF	-	1	-	1
MSS	ARM Cortex-M3	no	no	yes	yes
	CAN, 10/100/1000 Ethernet, HS USB	-	-	1	1
	MMUART, SPI, I2C, Timer	-	-	2	2
Physical & Core	User General-Purpose Input/Output (GPIO)	200			
	Technology Node [nm]	65			
	Core Voltage [V]	1.2			
	Smallest Package	FCS325			
	Dimensions [mm^2]	11 x 11			

ARM Cortex-M3 has a number of advantages, such as simple programming in the high-level C language. This can be exploited with an appropriate firmware design, for example, to implement small coefficient or parameter changes to the signal processing more quickly. In addition, more interfaces such as SPI or UART are already available as a hardware module on the Microcontroller Subsystem (MSS), so that communication with peripheral components is easier and possible without allocating FPGA resources. Between the two considered SmartFusion 2 variants M2S050 and M2S060, the former was chosen. The difference in the available FPGA resources is negligible and well under one percent. The difference in estimated power dissipation, on the other hand, is up to 15 % (compare scenario I-1 in Table A.2).

With the integrated Double Data Rate (DDR) Synchronous Dynamic Random-Access Memory (SDRAM) controller cores within the SmartFusion 2, such a memory will be used for the faster access memory type as described in the previous section. These controllers support the SDRAM memory types Low-Power Double Data Rate (LPDDR)1, DDR2 and DDR3, whereby the data rate is limited to a maximum of 667 Mbps for the regular, non low-power variants. Due to this

restriction, the LPDDR1, which is explicitly adapted to low-power and mobile applications, is to be used, since the possible speed gain compared to the regular DDR memories cannot be fully exploited. In addition, the use of a DDR3 memory would require additional components such as ICs for active termination of the data lines, which can be saved otherwise. The MT46H32M16LFBF-5 IT from Micron is targeted as the corresponding LPDDR1 SDRAM, since this is used on a development board (SF2-STARTER-KIT by Emcraft Systems) of the M2S050, thus ensuring compatibility with the DDR controllers of the SoC.

4.2.2. Analog-to-Digital Converters

For the use of passive EEG sensors the ADC is a pivotal component in a mobile BCI. It is responsible for translating the real-world, analog signals derived from brain electrical signals into digital data that can be processed and interpreted within digital signal processing hardware. Since multiple EEG electrodes are expected to be used, the choice of a multi-channel ADC makes sense. These can guarantee a simultaneously sampling of several channels. In addition, application-specific ICs are adapted to the general conditions as well as characteristics of the corresponding signal recording and sometimes offer specialized functions, which is why a variant with focus on EEG signals is explicitly preferred over a generic ADC. A corresponding component search identified four possible ADCs, the ADS1299 by Texas Instruments as well as the AD7768, AD7177-2 and AD7779 by Analog Devices. All four are based on delta-sigma modulation and use SPI as a serial interface for configuration and data readout, with other related interface options (e.g. MICROWIRE) also available in some cases. Furthermore, all ICs can be cascaded, either via daisy-chaining or via dedicated pins for synchronization and use of a common clock, which also allows a larger number of EEG channels to be provided in synchronization. Finally, all variants include a unit for adjustable signal gain. It should be noted that the ADS1299 is the only one that focuses exclusively on EEG and biopotential measurements. The other ICs have additional applications listed on their datasheets, such as audio test and measurement (AD7768), chromatography (AD7177-2), or power switches (AD7779).

The main features and characteristics of the four possible ADCs are listed in Table 4.4. Except for the AD7177-2, all ADCs provide eight fully differential input channels, which can also be used as eight single-ended inputs. However, the AD7177-2 is the only candidate to have 32 bit resolution instead of 24 bit. As for the sampling rate, all ADCs support at least 10 kHz, which is generally considered sufficient for EEG signal acquisition. The included digital filter options vary. The AD7177-2 offers the most variability, followed by the AD7768. Nevertheless, missing filter options can be provided within the reconfigurable SmartFusion 2 on an application-by-application basis and therefore do not need to be a high priority for the ADC selection.

The AD7177-2 is initially excluded due to its low channel count. Although its package dimensions are slightly smaller, a multi-channel implementation with more than the number of channels provided would require a significantly larger PCB area than the other ADCs. Of the remaining three options, the ADS1299 was selected for the CereBridge system. Its sampling has the best SNR, the second-lowest power consumption for active mode, and the lowest standby power consumption. Moreover, the ADS1299 stands out with special additional functions, which are tailored to EEG signal acquisition specifically. The lead-off detection, indicating the correct connection between the electrode of an EEG channel and the scalp, should be mentioned here in particular. Such a feature is especially useful in a mobile BCI, where the likelihood of

Table 4.4: *Overview of potential ADCs*

Features	ADS1299	AD7768	AD7177-2	AD7779
#Channels (Differential)	8	8	2	8
#Channels (Single-Ended)	8	8	4	8
Resolution [bit]	24	24	32	24
Output samples per second [kHz]	0.25-16	1-256	0.005-10	0.25-16
SNR [dB]	121	111	-	108
Analog Power Supply [V]	5	5	5	3.3
Digital Power Supply [V]	1.8-3.6	1.8-3.6	2.5-5	1.8-3.6
Power Consumption (active) [mW]	49	75	42	44
Power Consumption (standby) [mW]	5.1	18	2.2	-
Power Consumption (Power-Down) [µW]	10	2,500	125	530
Sinc digital filter I	3rd order	5th order	5th+1st order	3rd order
Sinc digital filter II	-	-	3rd order	-
High order brick wall filter	-	yes	-	-
50/60 Hz rejection filter	-	-	yes	-
Reference Voltage	Ext. or int.	External	Ext. or int.	Ext. or int.
Package Dimensions [mm^2]	10×10	10×10	7.8×6.4	9×9
Test signal generator	yes	no	no	no
Lead-off detection	yes	no	no	no

electrode displacement is higher than in a controlled laboratory environment. This mechanism can further be used to measure the impedance of the electrode-scalp contact, assisting in the correct setup of the electrodes and, if necessary, the application of an appropriate amount of contact gel. In addition, an included test signal generator can be used to debug and verify data flow to the surrounding hardware system. The performance and quality of sampled EEG signals with the ADS1299 have been evaluated in [Ras18]. Based on the results, it is concluded that the performance of the ADS1299 using wet Ag/AgCl electrodes is comparable to that of a laboratory-based system for low frequency (< 40 Hz) EEG recordings.

In summary, the ADS1299 IC, with its low noise level and high-resolution multi-channel sampling, sufficient data rate, and built-in lead-off detection mechanism, provides an optimal ADC solution for the CereBridge system. Its integrated features and low power consumption can reduce the complexity of system design and improve the performance of the mobile BCI.

4.2.3. Power Management

This section focuses on all components required for the electrical supply of the overall system. Since the CereBridge system is battery-powered, in-system charging of the necessary battery should also be possible and will be considered here. Two factors are primarily relevant for the planning of power management and the corresponding selection of components: The generally required voltage rails and the required maximum electrical power provided on them.

The chosen ADS1299 requires an analog supply voltage of 5 V. In addition, a core voltage of 1.2 V is required for the SmartFusion 2 (VDD_core), as well as a voltage of 1.8 V to operate the LPDDR1 and the associated GPIO bank of the SmartFusion 2. This voltage can also be used for the digital supply voltage of the ADS1299 (1.8 V to 3.6 V), as this is its nominal supply voltage with the least power consumption for this IC. Since a non-volatile memory is desired (see 4.1), 3.3 V should also be available to power a flash memory such as a microSD card. In addition to the core voltage, the SmartFusion 2 also requires a voltage supply for its charge pump (VPP), embedded Non-Volatile Memory (NVM) (VPPNVM) and various Phase-Locked Loops (PLLs) (VDDA_PLL). These are specified as either 2.5 V or 3.3 V, the former of which would have a positive impact on the resulting power consumption.

The next step is to estimate how much current is required from the individual supply voltage rails. It should be noted that the provided power specified for the voltage converters and voltage regulators should not be exceeded during normal operation for stability reasons, so this will be a worst-case estimate. Since not all components used in the system are known at this point, a corresponding headroom is taken into account. Starting with the SmartFusion 2, the same power estimation tool as in 4.2.1 is utilized, but this time the settings are as follows:

- M2S050 in FCSBGA package with commercial temperature grade and no applied heatsink

- Process is set to „Maximum"

- 25 °C ambient temperature with still air

- All available DSP, LUTs, registers and memory SRAM are fully utilized

- Global clock frequency of 100 MHz (used for FPGA, MSS and LPDDR) with 100 % clock enable rate

- Clock fanout set to 112,680

- Global toggle and enable rate of 25 %

- Average logic fanout of 5

- 15 input and 15 output pins with LVCMOS25 standard as well as 15 input and 15 output pins with LVCMOS33 standard, all driven with system clock, an output load of 5 pF, output enable rate of 50 % and an output current drive of 4 mA

- MSS Cache controller and embedded NVM enabled, also utilization of all available UART, SPI, I2C, Real Time Counter (RTC) and timer peripheral modules

- Usage of an external crystal with a frequency of 32,768 kHz as a clock source

- Other settings are left default

All estimates, including the currents required on each rail and the resulting power values, are summarized in Table 4.5. The resulting power dissipation is about 2953 mW, with more than 96 % attributed to the 1.2 V rail. However, it should be noted that such a load on the FPGA is not only extremely unlikely, but would probably be impossible to achieve due to the complexity of the routing.

In addition to the power consumption of the SmartFusion 2, the power consumption of the ADS1299 ADC, LPDDR1 memory, and microSD card memory was estimated and considered. For the ADC, it was assumed that four ADS1299s are operated in parallel to support a maximum

Table 4.5: *Voltage rails for the CereBridge system with estimated maximum current and power requirements*

Voltage Rail [V]	Max. Current [mA]	Max. Power [mW]	Required by... / Used for...
1.2	2376.8	2852.2	VDD_core
1.8	$2 + 115 + 20.5 = 137.5$	247.6	ADC DVDD, LPDDR1, GPIO
2.5	$5.3 + 2 + 6.6 = 13.9$	34.7	VPP+VPPNVM, AVDD_PLL, GPIO
3.3	$198 + 8.8 = 206.8$	682.6	microSD card, GPIO
5	62.2	310.8	ADC AVDD

channel count of 32. As stated in the data sheet, each ADS1299 requires 0.5 mA current to operate its digital part at a supply voltage of 1.8 V (DVDD) and 15.54 mA via the 5 V rail for the analog supply voltage (AVDD). According to its data sheet, the LPDDR1 MT46H32M16LFBF-5 IT requires a maximum of 115 mA for the two operating modes "Operating Burst Write" and "Operating Burst Read". ATP's AF8GUD4A-EBAXM was used as an example to estimate the power consumption of a microSD card, which specifies a maximum current consumption of 198 mA across the 3.3 V rail.

The values listed are taken as the basis for selecting appropriate voltage regulators for the CereBridge system. Since they already represent extreme cases, and since the components considered can be assumed to be the most power-demanding for the CereBridge system, no additional headroom needs to be applied to the values.

For some FPGA families specialized Power Management Integrated Circuits (PMICs) are available. These usually contain all the necessary voltage regulators in one package. However, for the SmartFusion 2 and the other core components described, no PMIC solution could be found that meets the requirements listed in Table 4.5. Nevertheless, the use of a PMIC is recommended whenever possible to reduce board area for power management, especially when multiple voltage rails are required.

Maxim's MAX8663 PMIC was selected as the central power management component of the CereBridge system. It includes a Li-ion battery charger, two buck regulators with 95 % efficiency as well as maximum output currents of 1200 mA and 900 mA. Four additional linear Low-Dropout Regulators (LDOs) are also provided. The whole system is available in a small 5×5 mm^2 package. This IC can be used to directly implement in-system battery charging, as well as provide several of the required voltage rails. The MAX8663 has a connection option for an external voltage V_{EXT} in addition to the Li-ion battery. If there is a present V_{EXT} in the specified voltage range of 4.1 V to 6.5 V (nominal 5 V), a connected battery will be charged. In addition to the outputs of the integrated voltage regulators, a voltage V_{SYS} is also provided, which corresponds to V_{EXT} if present or V_{BAT} otherwise. This voltage can be used as the supply line for all components that do not depend on one of the included voltage regulator outputs.

Figure 4.4 summarizes the power management implementation for the CereBridge system, including all components discussed here.

The 1.8 V rail is provided by the first switching converter of the MAX8663. Due to the high voltage difference to a lithium-ion battery and the present current requirement, a linear voltage conversion, which consumes the power of the voltage difference multiplied by the current as power dissipation, would be associated with quite high power dissipation overhead. However, one of the supplied linear regulators is used to supply the 2.5 V rail. The higher power dissipation
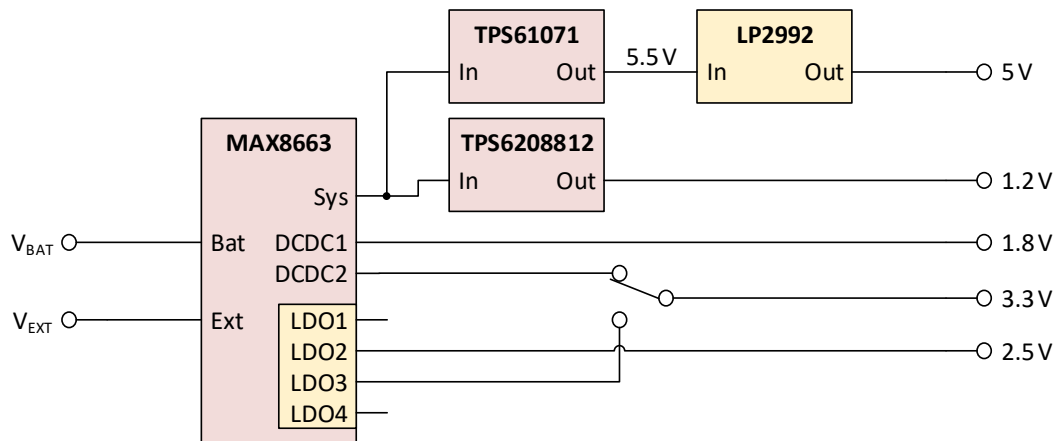
Figure 4.4: *Schematic overview of the power management ICs for the CereBridge system*

due to linear regulation compared to a switching converter is accepted here because the 2.5 V rail has the lowest current requirement of all rails (see Table 4.5) and accounts for less than 1 % of the total power. Since 2.5 V is always below the usable voltage range of about 3 V to 4.2 V of a single cell Li-ion battery, the linear converter can be used without concern. The second switching regulator is used for the 3.3 V rail. Alternatively, an LDO could be used instead, since it is available anyways and does not require any additional components other than a decoupling capacitor at the output to smooth the output voltage. In the default case, the switching regulator is used because it can achieve significantly lower power dissipation during voltage conversion, and this rail may have to supply a comparatively large amount of power, at least when actively using a microSD card memory. It should be noted that the 3.3 V is within the usable voltage range of a Li-ion battery. As soon as the battery voltage is close to or below 3.3 V due to discharge, the full 3.3 V at the output of the used voltage regulator can no longer be guaranteed. Since the components that require a 3.3 V supply are typically specified for 3 V as the lower limit, this is accepted. In addition, the battery is well above 3.3 V for most of its discharge capacity. According to [Tra16], the residual charge of the two investigated batteries is only 11.2 % and 24.2 % at an output voltage of 3.3 V with a simultaneous discharge current of 2.5 A, and 4 % and 14.8 % at an output voltage of 3 V with the same current drain. Thus, it can be assumed that up to a 70 % discharge of the battery, no effects on the 3.3 V output voltage of the converter are to be expected. Only at significantly more than 80 % discharge, a violation of the 3.3 V rail's component specifications with a voltage below 3 V at high current consumption can possibly occur. The other two included LDOs are left unused.

For the voltage rails of 1.2 V and 5 V other solutions were selected, which will be derived from the V_{SYS} output of the MAX8663. The 1.2 V may require more current than the maximum 1200 mA specified by the buck converter included in the MAX8663, as our estimates show. Therefore, the TPS6208812 from Texas Instruments was chosen, which provides up to 3 A output current and is available in a 1.2×0.8 mm^2 package. For the 5 V rail a boost converter is required, which is not provided with the MAX8663. Since the output of a switching regulator is usually somewhat noisy due to its internal operation, the combination of a boost converter, which raises the voltage slightly above the actual desired voltage level, and a subsequent LDO can be used if necessary. This method is a common design practice to supply more sensitive, i.e.
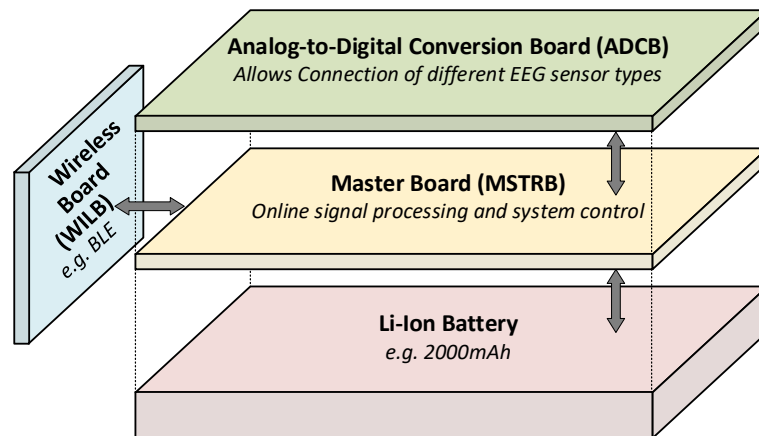
Figure 4.5: *Concept for stackable modules of the mobile CereBridge system (adapted from [Wah20])*

analog, circuit parts with a voltage as stable as possible. In this case, we chose a combination of the Texas Instrument's TPS61071 boost converter, which outputs 5.5 V, and the Texas Instrument's LP2992 low-noise LDO to provide the final 5 V, both from Texas Instruments.

4.3. System Concept and Design

This section describes in detail the structure and features of the CereBridge system. After an initial explanation of the partitioning of the system components into individual modular boards, these are discussed in more detail and their practical implementation is presented.

4.3.1. Partitioning for Modular Structure

The CereBridge system is divided into several individual boards for two reasons. First, it allows to keep the footprint of the system small, making it easier to integrate into a mobile system that is comfortable to carry and to mount close to the subject's head. Second, this approach supports the changing requirements of different application scenarios without having to change the entire system or to keep it overly complex to cover many special cases. Instead, the system design provides many interfaces and connectivity options, which will be used to connect possible extensions as needed. An abstract overview of the partitioning of the system on several modules for the mobile application is shown in Figure 4.5. It consists of the three Printed Circuit Boards (PCBs): Master Board (MSTRB), Analog-to-Digital Conversion Board (ADCB), and Wireless Board (WILB), as well as a lithium-ion battery for power supply.

The MSTRB is the core of the system and is primarily based on the SmartFusion 2 SoC with many interfaces and connectivity options for connecting other hardware components to extend functionality. Since this module is also intended to be always present, it will also include the lithium-ion battery connectivity and all the components of the general power management circuitry. The only exception is the LP2992 LDO, which generates the final analog supply voltage for the ADCs. It is placed as close as possible to its sink, the ADS1299. This also avoids routing this voltage rail close to possibly high frequency signals on the MSTRB.

The ADCB is deliberately kept as a separate module. On the one hand this allows to exchange the connectors for the EEG sensors including the used ADCs if necessary. On the other hand, this approach results in a local separation of the sensitive analog electronics from other digital circuit parts of the system, especially from the high-frequency high-speed signals such as the LPDDR SDRAM connection. The WILB module for wireless data transmission is also separated to allow different (wireless) protocols for the system if required. To prevent this module from significantly increasing the footprint or stacking height of the system, it will be able to be connected to the side of the MSTRB in a T-shape if needed. However, the standards-based and comparatively energy-efficient BLE protocol was chosen as an example and will be considered in the following.

For the use in laboratory environments, during the debugging process of algorithm development, or for programming the SmartFusion 2, a battery-based power supply for the system is not always optimal, and additional wired connection options may be desirable in these scenarios. These requirements are met by the Programming and Debugging Board (PRGDB, not shown in Figure 4.5), which can be connected directly to the MSTRB and/or the ADCB. It provides external powering options, access to all lines of the connectors between the two modules, and Joint Test Action Group (JTAG) as a programming and debugging interface to the SmartFusion 2.

Mezzanine Connectors

The mezzanine connectors in the CereBridge system facilitate system expansion and customization, allowing researchers and developers to add new features and functionality to the system as needed through connection of modules. Even though the connectors do not directly affect signal acquisition or digital processing, they have a significant impact on the board area required for each module and continue to contribute to the mechanical stability and reliability of the system. Thus, a few notes on this topic are provided here.

For stability reasons, two connectors are used for each connection between two of the larger boards. From practical experience with early prototypes, it was known that some connectors with the smallest possible pitch between pins can be very susceptible to mechanical stress, especially shear stress. This effect is amplified in very small connectors with relatively few pins (<50). In some cases, this has manifested itself as individual unconnected lines between two mated connectors, or as momentary disconnects when mechanical force is applied to the corresponding modules of the system. This is particularly unacceptable for a mobile system attached to the body, where vibrations are anticipated.

This effect was explicitly observed with the 0.4 mm pitch DF40C series from Hirose. Two of these connector types are used on the development board for the SmartFusion 2 (SF2-STARTER-KIT from Emcraft Systems) with 80 pins each and showed no connection problems. Nevertheless, the smaller variants from the same product series with 20 and 30 pins were quite unstable on the prototype boards. In addition to motion-induced mechanical stress, even small differences in alignment between the receptacle and the connector during component placement caused enough mechanical stress to cause connection errors on individual lines.

For this reason, a larger pitch was chosen and the associated increase in board area accepted. During the selection process, it was also important to ensure that the connectors were reverse polarity protected and allowed a relatively high number of mating cycles for their size class.
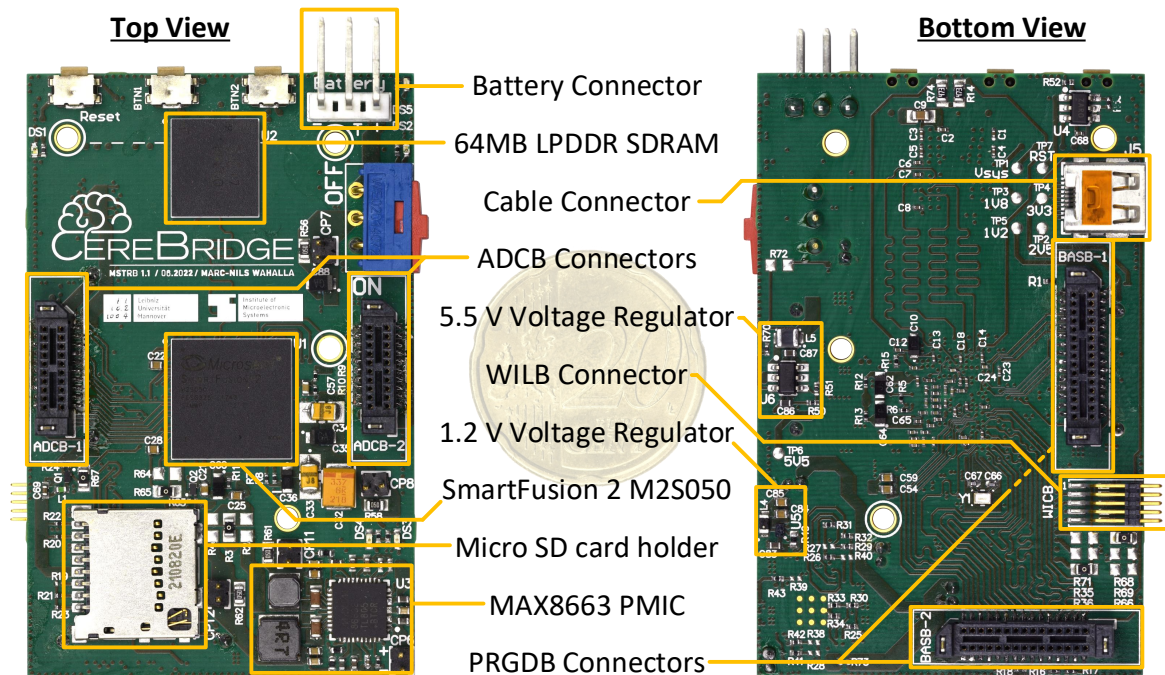
Figure 4.6: *The master- and processing-board v1.1 of the CereBridge system*

The latter is also related to the strength of the connection and thus the robustness against mechanical strain. The next largest pitch with corresponding connector products after 0.4 mm is 0.635 mm, but no variants were found with a suitable number of pins to allow a high number of mating cycles (> 200). Therefore, the 0.8 mm pitch TEM/SEM series from Samtec was chosen, which is explicitly advertised as robust and highly reliable and is specified for at least 2500 mating cycles.

4.3.2. Master- and Processing-Board

As described earlier, the Master Board (MSTRB) is the central module of the CereBridge system. It is essential to the operation of the entire system, since the SmartFusion 2 SoC is responsible for all configuration and control of the remaining, possibly peripheral, electronic components. Figure 4.6 shows two photos of the MSTRB, one from the top and one from the bottom. In addition, the main components are labeled and a full scale 20 euro cent coin is included for size comparison. The dimensions of the PCB area are 36×56 mm^2. It should be noted that the Bills of Materials (BOMs), schematic documents and layout examples for the MSTRB PCBs are provided in the Appendix B for the interested reader, as a complete discussion of all circuit components is beyond the scope of this work.

The SmartFusion 2 SoC was placed in the center of the board during the initial floorplanning phase. It has the most used pins of all components, which can be better routed to other components in a star configuration. Figure 4.7 shows the approximate location of each of the SmartFusion 2's GPIO banks, which dictate the useful placement of other components. Since bank 0 can be used by both the FPGA and the ARM Cortex-M3 (unlike bank 5), it is used to connect the LPDDR memory. In order to simplify routing on this board and to support
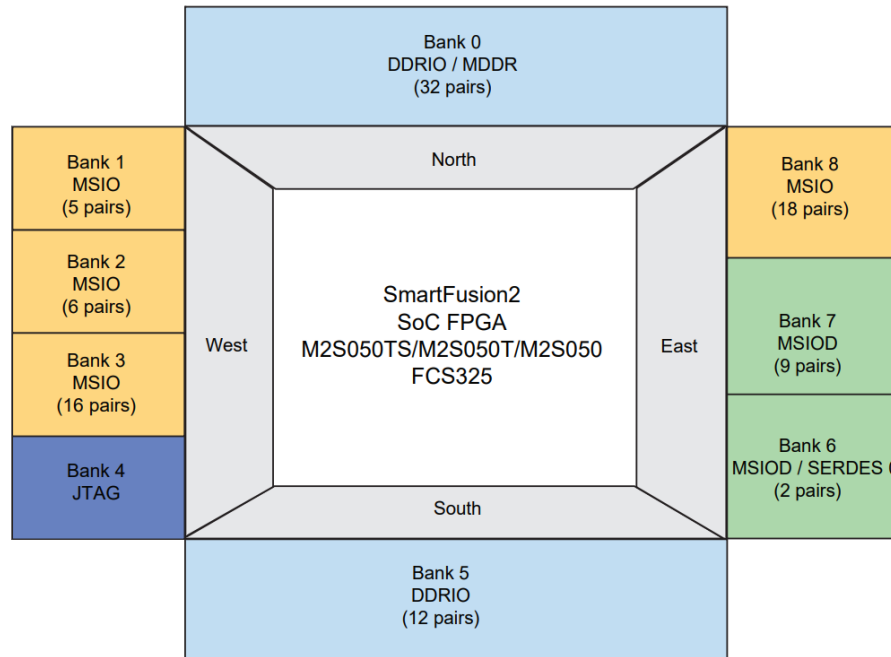
Figure 4.7: *Abstract overview of the SmartFusion 2 GPIO bank locations (adapted from [Mic17])*

separation between fast digital signals and analog areas such as the power supply, the remaining banks of the SmartFusion 2 were selected so that not all sides require digital connections and routing respectively. Since JTAG (bank 4) is needed for programming, banks 1-3 will be used and banks 5-8 will be left unused. For the connection to the ADCB board, the digital signals as well as the corresponding power supply are separated from the analog 5.5 V voltage rail by splitting them between the two mezzanine connectors (ADCB-1 and ADCB-2 on the top side in Figure 4.6). Moreover, these should be placed as far away from each other as possible to improve mechanical stability. In addition, care was taken to place them distant from the LPDDR memory to reduce the likelihood of interference with the sensitive ADCs. This resulted in a sideways placement compared to the SmartFusion 2, with the data lines on the west side and the analog power supply tracks for the ADCs on the east side. In addition, all of the power management components, including the battery connector and power switch, were also placed on the east side, although the two individual voltage regulators on the MSTRB were placed on the bottom side for space reasons.

The connectors for the PRGDB, also on the bottom, were moved to the south and west. The reason for this is that the GPIO banks are easily accessible and the Through-Hole Technology (THT) mechanical stabilization pins, which protrude slightly on the opposite side of the PCB, can be placed there without interfering with other components. The center of the bottom side is dominated by many decoupling capacitors for the SmartFusion 2's power supplies and the northern half consists a high track density, especially in the inner layers, for connecting the LPDDR memory, preventing this area to be used for useful routing of other signals or component placing. All other interface connectors, which consist of tracks for digital signals, were also placed on the bottom side, horizontally opposite to the power supply components.

The multilayer structure of the PCB itself consists of a total of eight signal layers, which are described below from top to bottom, numbered 1-8. Four layers are primarily dedicated to the power supply. Layers 2, 4 and 7 are mostly covered by a ground plane. The various power supply

voltage rails are routed as planes mostly within layer 5 and thus, together with the adjacent ground plane, generate the typically desired built-in capacitance to compensate for voltage fluctuations during electrical load changes. Layers 3 and 6 are used to route digital signals in addition to the outer layers (1 and 8). Due to the layer structure, each signal layer is adjacent to at least one ground layer, which is beneficial for signal integrity. The minimum structure dimensions used are 100 μm with 150 μm diameter holes. Since not all of the SmartFusion 2 SoC's GPIOs are needed, the use of laser-cut microvias or other blind and buried vias is not necessary. However, the plated-through vias were plugged to prevent solder paste from flowing from adjacent pads during soldering. This is particularly important in the SmartFusion 2 SoC area where via-in-pads are used. In addition, the usual solder resist mask clearances around vias have been removed to prevent potential short circuits when handling the board.

Some special component groups, which are either interesting from a routing point of view or can be useful when using the CereBridge system, will be discussed in the following sections.

High-Speed Signal Tracks

On the MSTRB, there are two specific groups of signal tracks which, because of their relatedness combined with a comparably high switching rate, have been routed with special regard to their length and spacing.

The first group of signals includes all data, address, configuration and clock tracks between the LPDDR memory and the SmartFusion 2. Based on various design guidelines, the maximum length of any signal should not exceed 200 mm. In addition, all address, configuration and data tracks (divided into upper and lower bytes) in their respective classes should have a length difference of no more than 1.27 mm between each other. The two differential clock signals should have a length difference of less than 0.508 mm. Moreover, the maximum length difference from the shortest to the longest signal is 8.89 mm. In the practical implementation of the routing, however, these limits were significantly undershot. The actual maximum track length differences are 318 μm for the upper byte of the data tracks and 593 μm for the lower byte. For the control signals the value is 984 μm, for the address tracks 160 μm and for the differential clock track 17 μm. Furthermore, the maximum length difference between all signals of 984 μm is well below the required 8.89 mm. The maximum absolute length of 36.328 mm is also well below 200 mm. The recommendations for trace widths, routing layers and spacing (15 mil[2] for clock and configuration signals, 12 mil for the rest) were taken into account as well. Altogether, these measures, with the corresponding headroom compared to the specifications, should ensure error-free communication with the LPDDR memory IC and also minimize Electromagnetic Interference (EMI). On the other hand, this means that compliance to the length and spacing requirements for the memory connections on all signal layers (1,3,6,8) takes up a considerable amount of board space. This is the main reason why the northern half of the MSTRB is not as densely populated with components as the southern half.

The second group refers to specific tracks routed from SmartFusion 2 to a PRGDB connector. The intended application is to provide an MII interface, so that a total of 15 tracks are routed, taking into account their differences in length. This interface can be used to provide Ethernet with a data rate of 10 Mbps to 100 Mbps on the PRGDB with the help of an appropriate PHY

---

[2]1 mil ≙ 25.4 μm

(first layer of the OSI model), if desired. For MII routing a trace length matching within 10 mm is recommended while the total length should not exceed 150 mm. The tracks are routed with a maximum length of 28.239 mm and a maximum length difference of 445 µm, leaving more than enough margin for the potential second part of the routing on the PRGDB. In addition, the use of vias has been omitted so that no additional major impedance changes occur on the tracks. Depending on the configuration of the PRGDB, these signals can be used alternatively for other high-speed protocols instead of MII, which might also benefit from small length differences between the lines.

External Interfaces

The following describes the interfaces of the MSTRB with other boards and potential peripheral electronics. These are subdivided according to the respective connector type and the number of available data lines are explicitly mentioned. Here it is explicitly stated for certain connections that they can be used as UART or SPI interface directly with the corresponding MSS module of the SmartFusion 2. Note that all GPIOs of the SmartFusion 2 and therefore all described data lines can theoretically be used by the MSS and its modules if they are mapped internally to the corresponding pins via the fabric.

The two connectors to the ADCB are of the Samtec SEM-110-02-03 type and have 20 pins each. As mentioned above, one of them is dedicated to the analog power supply (5 V) and some ground pins. The other one uses two tracks for the digital power supply (1.8 V), four ground pins and 14 data lines. This also includes the corresponding lines for an SPI interface with up to four slaves directly with the MSS of the SmartFusion 2. In total, it is possible to control up to four ADS1299s with these lines, even without daisy-chaining. For each of them, a separate data ready track and a common start signal track are designated. The remaining two data lines can be configured and used as needed and are not required for communicating with the ADS1299 by default.

Two Samtec SEM-115-02-03 connectors with 15 pins each are used to connect the PRGDB. These contain a total of 11 ground and 11 external voltage (V_{EXT}) pins to allow charging of a connected lithium-ion battery even during extensive use of the CereBridge system. In addition, six tracks are designated to JTAG for programming and debugging both the ARM and FPGA of the SmartFusion 2. The associated 2.5 V rail is also provided so that a properly connected programmer can sense the power supply to the target system. Also included are 14 general purpose data pins and the 15 high-speed signal pins intended for the MII. The last two pins provide the signal of one of the MSTRB's user buttons as well as the global reset signal.

The WILB is connected to the right-angle connector FTE-105-01 from Samtec, which has 10 pins. Four of them are used as ground connections and one of the three voltage rails 3.3 V, 2.5 V or 1.8 V can be connected to supply the WILB. The voltage is selected by setting a 0 Ω resistor jumper. A total of four data lines are available, two of which can be configured directly with an MSS UART. For the last connection, either the global reset signal or one of the user buttons of the MSTRB can be selected, also via a resistor jumper.

Finally, a Micro-HDMI connector is included on the MSTRB to enable a robust cable connection to hardware expansions. For this connector, the use of an external power supply should also be supported, even instead of the MSTRB's own battery. The reason for this is that the CereBridge

system can be connected to another battery powered system if needed, avoiding a double battery. The Micro-HDMI form factor was chosen to allow the use of commercially available cables. The comparatively small Micro-USB connector was deliberately not used, as it is more widely available and might increase the chance of the connector on the MSTRB to be misused. A total of 6 power and 7 ground pins are available, allowing the current flow to be distributed to the individual lines in the case of external power supply. There are also 5 data lines, two of which can be connected directly to a UART on the MSS of the SmartFusion 2.

Special Power Measurement and Configuration circuits

In this section, some special circuit parts dedicated to measuring or optimizing power dissipation are discussed.

A power switching circuit based on a p-channel MOSFET is implemented on the MSTRB. The default state can be set by $0\,\Omega$ resistor jumpers and the current value can be controlled from the SmartFusion 2 during operation. The power switching circuit is used to turn off the power to a microSD card when it is inserted into the provided card holder. Especially before the memory card is correctly initialized, e.g. after a reset, it can consume up to $15\,\text{mA}$ current or $49.5\,\text{mW}$ power in an unused state. Therefore, this allows the power supply to the SD card to be controlled without having to mechanically remove it if a contribution to power consumption is unwanted and the memory is currently not needed.

For evaluation and debugging of the CereBridge system, measuring the current and power consumption of individual voltage rails is desirable. This is especially true for the rails that have significant loads inside the MSTRB, as these values could not be determined externally through the connectors. Therefore, a corresponding possibility was provided for the battery voltage V_{BAT} as well as for the $1.2\,\text{V}$, $1.8\,\text{V}$ and $3.3\,\text{V}$ rails. For this purpose, a $50\,\text{m}\Omega$ current sense resistors with a deviation tolerance of $0.5\,\%$ and a high temperature stability are connected in series after the corresponding voltage regulators. A small 2-pin header is connected in parallel to each of these resistors, which can be used to measure the voltage drop and thus the current flow through the resistor. This simple method also allows to bypass the resistor without replacing it. For the $2.5\,\text{V}$ rail, this has been omitted because the load there is the smallest, thus saving board space.

Lastly, test points are provided for the $1.2\,\text{V}$, $1.8\,\text{V}$, $2.5\,\text{V}$, $3.3\,\text{V}$, $5.5\,\text{V}$ and V_{SYS} voltage rails so that the corresponding voltage can be easily measured for debugging or control purposes.

4.3.3. Sensor Connection Board

The Sensor Connection Board or Analog-to-Digital-Conversion Board (ADCB) is the second, always present module of the CereBridge system. It is used to connect EEG sensors and, in the case of passive sensors, to perform the necessary analog-to-digital conversion. In the version shown in Figure 4.8, up to 16 EEG channels can be connected, digitally sampled and forwarded to the MSTRB. The figure again includes a full scale 20 cent coin for size comparison. The actual dimensions of the board are $36.5 \times 48.2\,\text{mm}^2$. This is $500\,\mu\text{m}$ wider than the MSTRB, but significantly shorter vertically.
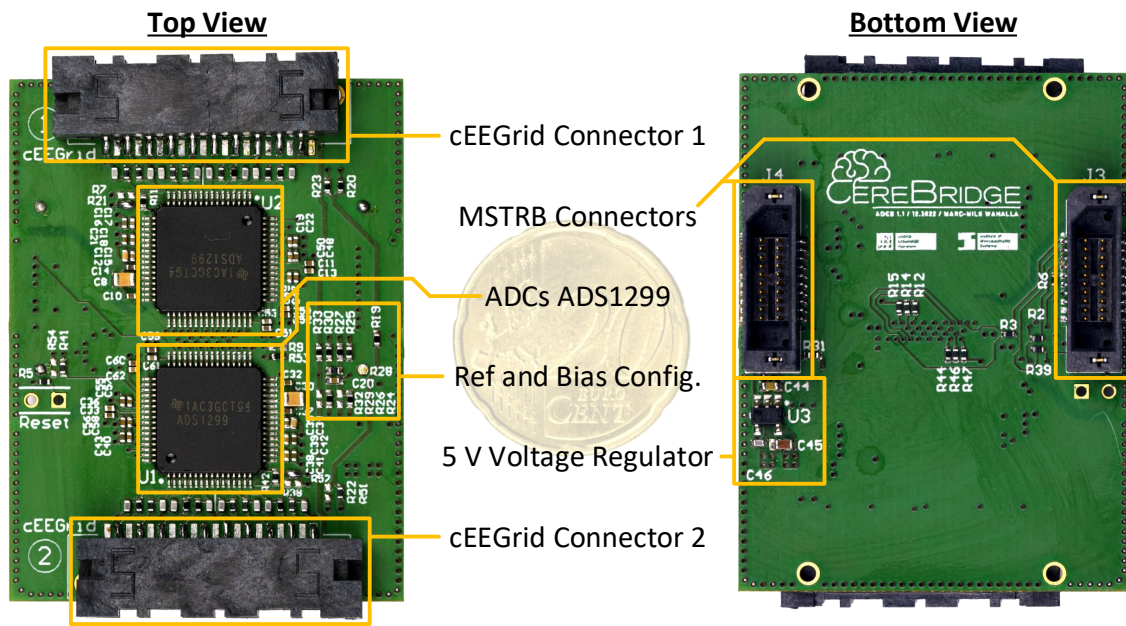
Figure 4.8: *The sensor connection and ADC board v1.1 of the CereBridge system*

The design of the ADCB is centered around the ADS1299s, which are placed on top. The ADCs are not daisy-chained, but can be addressed individually via SPI to allow the use of only one ADS1299 or different configuration of both, e.g. different sampling rates, if required. An example application for this board is the use of two cEEGrid sensors with 10 electrodes each, placed circumaurally around the ears of a human subject. Two adapted connectors are placed opposite to each other on the top side of the board. [Ble16] describes the use of 8 signal channels per cEEGrid, with the two remaining electrodes used as ground and reference signal. Using the "Ref and Bias Config." area marked in the Figure 4.8, the two ADS1299s can be configured using $0\,\Omega$ resistor jumpers to sample each cEEGrid individually or together using the same sampling clock and reference and ground electrodes. On the bottom side there are mainly the two connectors for the MSTRB connection and the LP2992 linear voltage converter to convert the 5.5 V to 5 V for the analog supply of the ADCs. The LP2992 is hereby placed as close as possible to the corresponding connector. All in all, the board has been designed to keep the analog and digital areas and components as separate as possible to minimize interference on the analog electronics and signals.

As mentioned above, the choice of reference and ground electrode is configurable for each ADS1299. It is possible that each ADS1299 receives these two signals from one particular connected cEEGrid, or that each cEEGrid provides these signals for their corresponding ADS1299. Similarly, the internally generated sampling clock can be configured. Both ADS1299s can use their own sampling clock, or alternatively the clock of one ADS1299 can be shared with the other, so that the sampling time of both ADS1299s is nearly identical and drift-free. In contrast to using a reference electrode, both ADS1299s can also use the analog voltage rail as a reference. Generally, up to 4 ADCs or 32 EEG channels are possible on the board. However, a slight deterioration of the noise behavior of the recorded EEG signals is to be expected in that case, since the separation of the analog and digital circuit parts could no longer be achieved as clear. An alternative would be to increase the size of the board to maintain the separation. In any

case, the connectors for the EEG sensors are relatively easy to change, so that other sensor types can be connected. If the sensors use active electrodes, the ADCs could be omitted and the board area could be reduced significantly.

The ADCB is realized with a 6-layer PCB with two dedicated ground layers (2 and 5) and one power layer (4). The digital supply voltage of 1.8 V as well as the analog supply voltage of 5 V are routed as planes on the power layer, whereby this can be implemented well here due to the clear separation of the two domains throughout the board. The minimum feature sizes used are 150 μm with 300 μm diameter holes. Also on this board the copper surfaces of the vias are covered with solder resist to prevent unwanted short circuits.

4.3.4. Additional Extensions

In the following, the two extension PCBs PRGDB and WILB are presented. For each board one implemented variant is described, whereby for both boards an exchange for a different design might be beneficial for applications with other requirements. This is especially true for the WILB, since the favorable wireless communication interface for the CereBridge system strongly depends on external factors as other communication participants.

Wireless Interfacing Board

The Wireless Interfacing board (WILB) is targeted for mobile applications on the CereBridge system with a desired wireless interface. For example, it may still be beneficial to send recorded and processed EEG data to, or receive parameters and commands from, other hardware. BLE was chosen as an example implementation of the WILB. This interface is widely used, especially on commercial devices such as smartphones or PCs. In addition, this protocol is much more energy efficient than, for example, Wireless Local Area Network (WLAN) or classic Bluetooth. A disadvantage of BLE is that the data throughput is more limited.

For this version of the WILB with BLE, the goal was to have a very small and lightweight PCB, which, due to the right-angle connection to the MSTRB, causes only a minimal increase in system area and does not affect its stacking height. Therefore, a search was conducted for a highly integrated Bluetooth System-in-Package (SiP) that includes both the required antenna and the clock crystal. Table 4.6 summarizes the suitable and matching ICs that were available at the time of PCB design. Of these options, the ISP1507 from Insight SiP was preferred as it offers the best trade-off between power characteristics and package dimensions. Additionally, a significant reduction in power consumption can be expected when the supply voltage is lower than the 3 V.

The ISP1507 is available in two variants (-AL and -AX), both based on different versions of a Nordic Semiconductor nRF52 microprocessor. The main difference is that the -AX version has more Flash memory, SRAM and a larger number of GPIOs. Since the smaller number of 13 GPIO is sufficient for the application in the CereBridge system, the WILB could be planned to provide pin compatibility between both versions, so that they can be used as needed. Both are Bluetooth 5.0 capable and support multiple data interfaces, e.g. SPI, I2C and UART.

The implemented version of the WILB is shown in Figure 4.9 and consists of only three main components: The ISP1507, the corresponding connector to the MSTRB, and a programming

Table 4.6: *Possible BLE SiP options for the WILB PCB*

Manufacturer	Type	Vdd [V]	Required Current with Vdd=3 V			Dim.[mm²]
			Tx [mA]	Rx [mA]	Idle [µA]	
Microchip	BM71BLE01FC2	1,9 - 3,6	10	10	2	8 × 6
Insight SiP	ISP1507	1,7 - 3,6	5	6.5	0.3	8 × 8
Insight SiP	ISP1302	1,8 - 3,6	10.5	12.6	0.6	8 × 8
Laird	BT860-SA	3 - 3,6	8	8	< 120	12.85 × 8.5
TDK	SP14808	2,35 - 3,6	5	5	0.9	14 × 12
ACKme	AMS001	1,8 - 3,6	10.8	12.8	1.65	17.6 × 11.4
Seeed	113050012	1,8 - 3,6	10.5	10.5	0.5	18.5 × 13
Espressif	ESP32-WROOM-32D	2,7 - 3,6	130	100	10	25.5 × 18
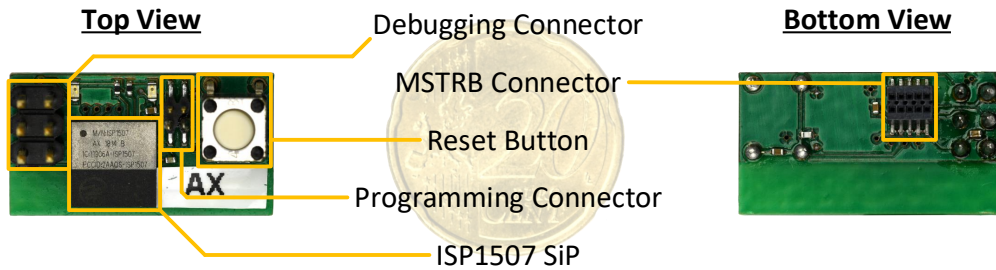
Figure 4.9: *Exemplary Wireless Transceiver Board with Bluetooth LE for the CereBridge system*

connector to program the integrated nRF52 processor. The fully assembled version shown in the figure also includes a reset button and a debugging header, allowing the WILB to be powered separately and used as a stand-alone device for test and evaluation. For the use with the CereBridge system, these are not required and can be removed through desoldering, which would significantly reduce the height of the WILB. The board utilizes a simple two-layer stack with dimensions of $13.2 \times 24.5\,\text{mm}^2$.

Programming and Debugging Board

The PRGDB PCB is primarily used to program the SmartFusion 2 SoC and to debug the whole CereBridge system. It can access all individual connections of the mezzanine connectors with many provided pin headers. In addition, the module is also intended to allow stationary use of the CereBridge system and to provide a suitable wired interface to a PC. In this case, a serial COM port via an Universal Serial Bus (USB) cable is provided.

Figure 4.10 shows the implemented PRGDB with an area of $125 \times 86\,\text{mm}^2$. The MSTRB and/or the ADCB can be stacked onto this board, with many headers in the accessible 2.54 mm pitch format around the respective surfaces of these boards to tap the corresponding connection signals of the connectors. For the ADCB connectors, depending on the assembled pin-compatible connector type on the PRGDB, either the ADCB or the MSTRB from its top side can be plugged in, allowing comprehensive debugging of both boards. As described above, it should be possible to provide a COM port via an USB cable. The FT230 IC, a USB-to-serial-UART interface, is
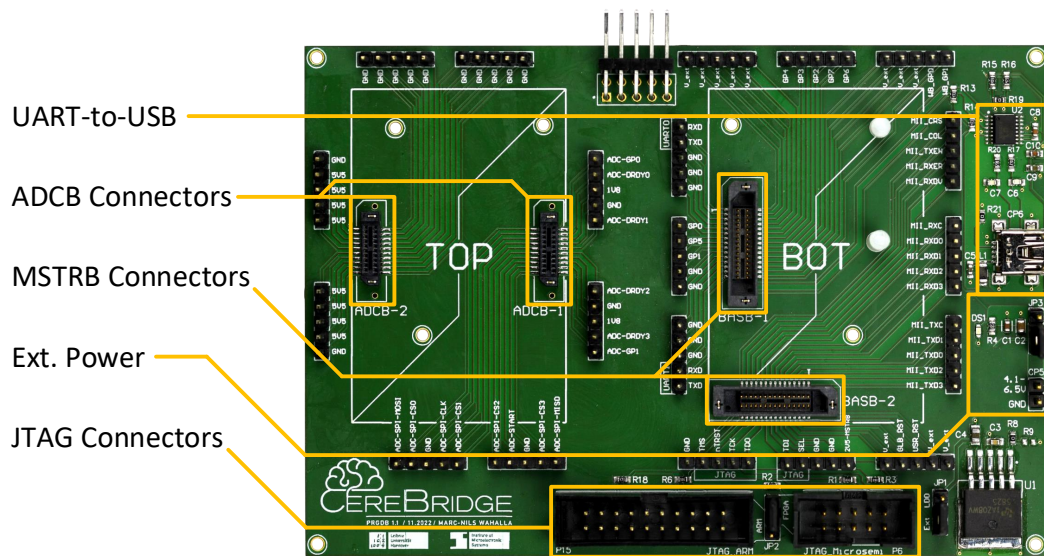
Figure 4.10: *Exemplary Programming and Debugging Board for the CereBridge system*

used to communicate directly with the MSS of the SmartFusion 2. Moreover, the PRGDB can provide the voltage V_{EXT} to power the CereBridge system and/or charge a lithium-ion battery connected to the MSTRB. Either the USB voltage can be selected as the source via a jumper or an external voltage of 4.1 V to 6.5 V can be connected to the provided header. Programming and direct debugging of the SmartFusion 2 is done through one of the two JTAG connectors. Hereby, the 20 pin header is specifically designed for ARM Cortex-M3 JTAG debugging. The PCB itself has a 2-layer stack and is optimized for easy access to the many connectors.

4.4. System Summary

In this chapter the hardware of the CereBridge system has been presented. Its modular design allows high flexibility in applications while having a small footprint. A comprehensive comparison of commercial state-of-the-art FPGAs was performed for the digital signal processing unit. Microsemi's SmartFusion 2 was selected for the CereBridge system because of its very low static power consumption, making it well suited for mobile applications. In combination with the ADS1299 ADC, which is specially tailored for EEG applications, and the integrated memory options such as LPDDR1 and a removable flash memory card, the system is highly versatile. With the implemented versions of the individual modules presented here, up to 16 EEG signal channels can be acquired, digitized and processed. The result of this processing can be communicated via BLE.

The system was designed with a clear focus on stand-alone operation and requires minimal user interaction. However, several programmable buttons have been integrated to allow, for example, changing the current operating mode. Status information can also be displayed directly via several programmable LEDs. Both are especially useful for debugging the hardware as well as new algorithms that will run on it. The debugging capabilities can be greatly enhanced by the stationary PRGDB module. In general, a variety of connectivity options and interfaces are provided so that the CereBridge system can be adapted to new requirements of future
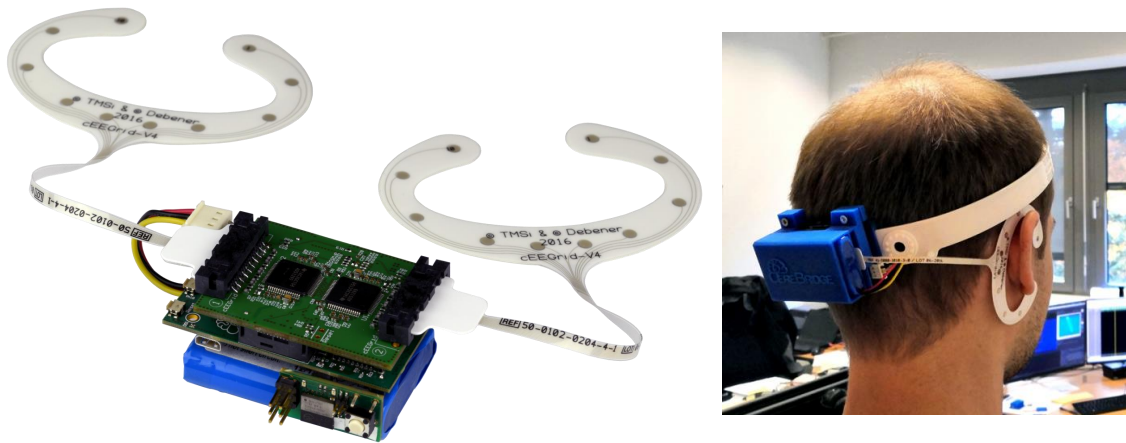
Figure 4.11: *Complete hardware system with cEEGrid electrodes (left) and an exemplary head-mounting with a 3D-printed prototype casing (right)*

applications. In addition to simpler protocols such as UART, SPI or I2C, the possibility of providing high-speed interfaces like MII should also be mentioned here in particular.

The presented complete system with two connected cEEGrid sensors is visualized in Figure 4.11, both with and without a casing. The head-mounted system shown on the right uses a simple 3D-printed prototype casing. The MSTRB and ADCB, with the battery underneath, require a total area of $36.5 \times 56 \, \text{mm}^2$, about the size of half a credit card. The CereBridge system in the configuration shown on the left, weighs about 56 g including all modules, the battery and the two cEEGrid sensors. This is well below the required 300 g. Furthermore, with the 1800 mAh lithium-ion battery, the system can operate for at least two and a half hours under the maximum power dissipation estimate of 2953 mW.

Integration of Data Handling and Processing

This chapter presents methods for the configuration of the CereBridge system and in particular the SmartFusion 2 SoC to handle and process sampled EEG data. Several techniques are proposed to support the hardware system concept and to further extend the already given flexibility.

Section 5.1 first proposes a data flow oriented task distribution of the SoC. It is discussed how signals can enter and be processed in the system. Furthermore, several possibilities are supported to tap signals in order to store them within the system or to communicate them further. The methods used to program and configure the SoC are described in Section 5.2. High-level synthesis is also introduced here, which can speed up the porting of algorithms to the FPGA. Since the CereBridge system is ready for use after the SoC configuration, possible application scenarios of the system are discussed in the subsequent section 5.2.2. The flexible application possibilities due to the modular and configurable design are highlighted. Finally, Section 5.3 describes some case studies in which different implementations of exemplary EEG processing algorithms for the CereBridge system were researched.

5.1. Data Flow Organization

In this section, we discuss the signal flow within the SmartFusion 2 SoC and within the overall CereBridge system. In addition, a concrete task distribution within the SoC is proposed.

The SmartFusion 2 SoC with an FPGA and the integrated microcontroller ARM Cortex-M3 allows a clear separation of their tasks. The main motivation for using an FPGA is to provide an adaptable hardware architecture for parallel data processing. Therefore, the processing of the digital EEG data should be done entirely on the FPGA by default. The microcontroller, on the other hand, is responsible for configuring all other components of the system and providing appropriate interfaces like SPI or UART to them. Thus, the microcontroller controls the entire signal flow of the EEG data to be processed in the CereBridge system.
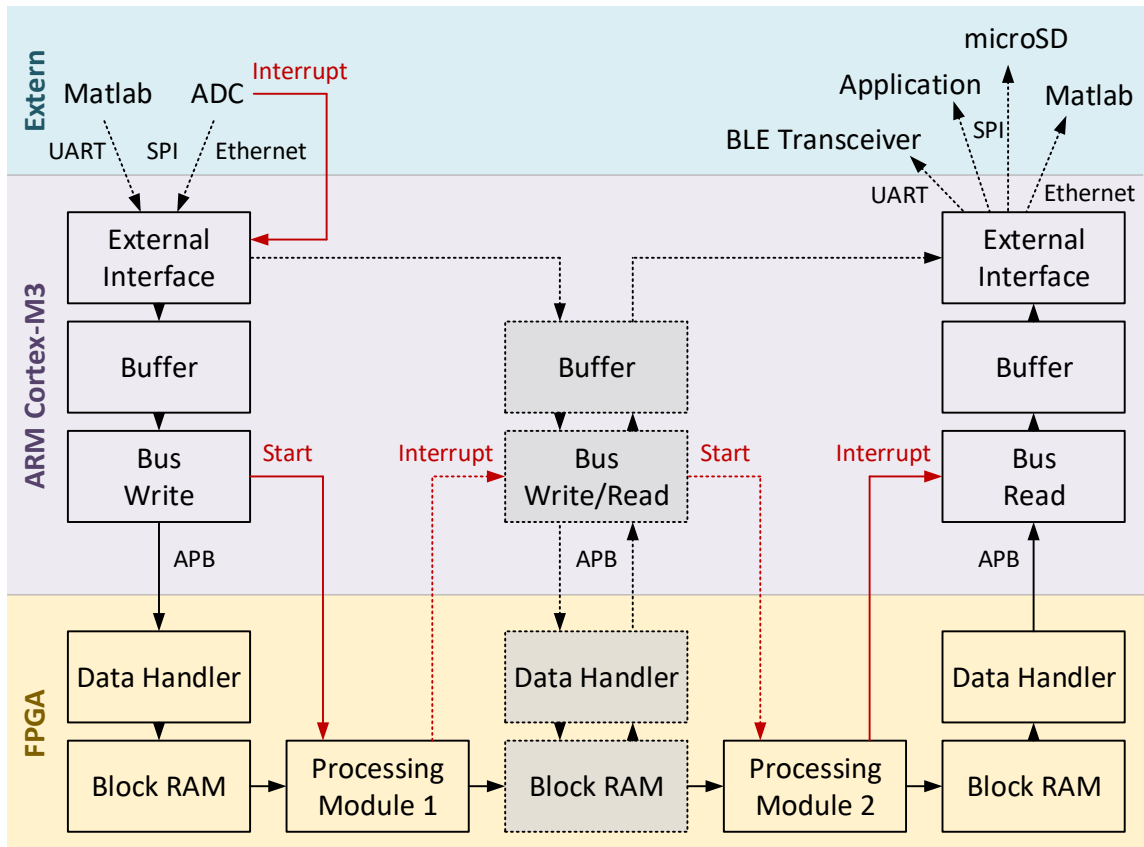
Figure 5.1: *Signal flow within the SmartFusion 2 SoC with task separation on the heterogeneous hardware architecture*

Consequently, the heterogeneous hardware architecture of the SoC should also be an advantage for controlling the signal flow within the SoC. Figure 5.1 shows the proposed partitioning. The figure is divided vertically into three layers. The external layer represents components and tasks outside the SoC, and the other two areas, ARM Cortex-M3 and FPGA, are the respective components of the SoC. All dotted arrows and blocks indicate optional or selectable connections and functions. All connections shown in red are control connections as opposed to black data lines.

The EEG data to be processed enters the SoC from external sources and is received by the microcontroller. Depending on the data source, different interfaces can be selected. During live recording of EEG signals via ADCs, the SPI is used. In addition, a corresponding pin of the ADC, which indicates the presence of a newly sampled data set, is utilized as an interrupt signal for the microcontroller to read out the ADCs. Alternatively, the data for test purposes can be provided by a PC, for example directly from the Matlab software. In this case other interfaces can be used. The incoming EEG data is first buffered before being transferred to the FPGA via a suitable data bus protocol, e.g. Advanced Peripheral Bus (APB).

In the FPGA of the SoC, the data is received and first written to an embedded block Random Access Memory (RAM). This is followed by any number of processing modules before the processed data is stored back into a block RAM at the end of the processing chain. From this block RAM, the processed data can be read back by the microcontroller through a custom data

handler via the data bus. Optionally, intermediate results of an integrated processing chain can be tapped. This is indicated by the gray and dotted blocks of the block RAM and the Data Handler at the center of Figure 5.1. EEG data can also be fed in at this point to verify the back end of the processing chain without the necessity to reconfigure the FPGA. In all cases, the microcontroller signals the FPGA via the start signal when a new data set is available for processing. On the other hand, the FPGA signals the end of processing to the microcontroller via an interrupt, which causes the microcontroller to read out the corresponding block RAM .

On the output side, i.e. the right side in Figure 5.1, the processed data is read out of the FPGA by the microcontroller and temporarily stored in a buffer. Via a selectable output interface, e.g. UART or SPI, this data is communicated to the external layer. The target of this communication can be a microSD card for data storage, Matlab on a PC, or a direct application.

Whether the output data is (processed) EEG data or a classification result is configurable and depends on the application. Both types of data are not mutually exclusive. For exampele, the classification result can be transmitted to an application (e.g. wirelessly) and at the same time the EEG data before classification can be written to a microSD card for later analysis.

Therefore, the figure shows the complete signal flow with some configuration options within the SmartFusion 2 SoC during normal operation. Not shown is the initial configuration of external peripherals or the SoC itself at startup or when changing modes.

5.2. Programming and Configuration of SmartFusion2

Several software tools are required to configure and program the SmartFusion 2 SoC with the task distribution described. In all cases, the FPGA and ARM Cortex-M3 are programmed using the FlashPro5 programmer connected to the MSTRB via the JTAG data lines.

Microchip's Libero SoC version 12.5 is used to configure the FPGA. Typically, a description of the FPGA in an Hardware Description Language (HDL) is also translated into a corresponding bitstream for programming the FPGA using the synthesis tool. Beyond that, Libero SoC is also used to customize and configure the intended interfaces and hardware modules for the MSS. The the physical pin layout for the SoC is also defined here.

After programming the SmartFusion 2 from Libero SoC, the ARM Cortex-M3 has no firmware and therefore no function. For this purpose, the software SoftConosle v6.4 is being used. This software compiles a corresponding firmware from the high-level programming languages C and C++. Subsequently, this firmware can be programmed into the microcontroller. Here, for an application of the CereBridge system, the firmware for the microcontroller is written to the embedded NVM so that it is stored non-volatile within the SoC. Afterwards, the programmed firmware is automatically executed on the microcontroller when the SoC is powered on.

5.2.1. High-Level Synthesis for Processing Modules

The processing blocks for an FPGA are usually described in a HDL, such as VHDL or Verilog. However, this process is comparatively time-consuming and is the main reason for FPGAs to have the disadvantage of increased implementation effort (compare Section 3.1). Therefore,
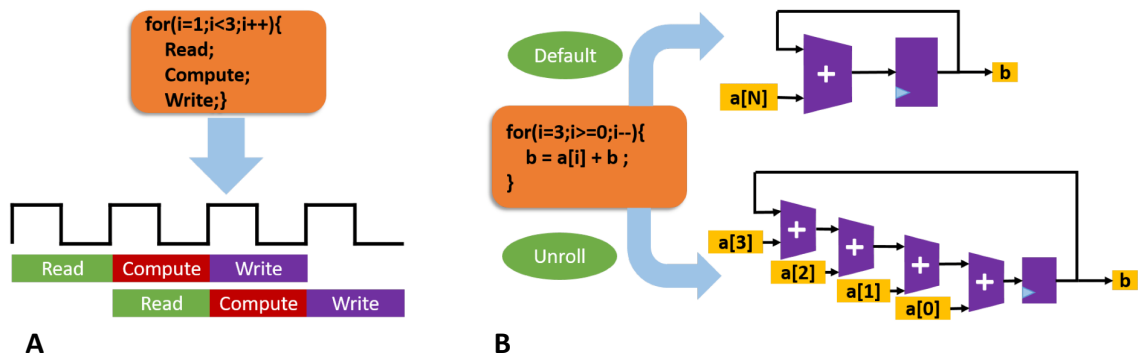
Figure 5.2: *Hardware Optimization techniques for increased throughput. A shows loop pipelining, B shows loop unrolling (adapted from [Man20]).*

special tools for High-Level Synthesis (HLS) can be used to accelerate this process significantly [Mic21]. HLS allows the hardware to be described at a higher level of abstraction and in a high-level programming language. In addition to getting an initial hardware implementation of an algorithm faster, different implementation options and optimizations can be explored and compared more quickly. For the SmartFusion 2 SoC, Microchip's SmartHLS software is available for this purpose and has been used in version 2022.2.1.

SmartHLS was used to describe processing blocks for the FPGA in C and C++. The software first compiles and verifies this code. Subsequently, a corresponding hardware description for the FPGA and a corresponding test bench are generated from this code. All steps for bitstream generation are performed automatically and reports on timing and resource usage of the implementation are provided. The function software-hardware co-simulation can then be used to verify that the results of the implementation are identical to those of the software. Finally, the processing modules generated in this way are integrated into the Libero SoC and can be written to the actual hardware.

During hardware design with HLS, the SmartHLS software takes into account various pragmas and constraints specified by the user. These can instruct the software to apply different optimization techniques during hardware generation. The two main techniques investigated are shown in Figure 5.2. Loop pipeling (A in the figure) allows a new iteration of a loop to be started in parallel with a running loop. This can increase the throughput of that section of hardware. Figure 5.2 B visualizes loop unrolling. Whenever possible, the software parallelizes the hardware for the computations performed in the loop. In the case of data dependencies, the additional hardware is applied as shown. This method also leads to an increase in data throughput. The cost for both optimization techniques is an increased resource requirement of the FPGA.

As an alternative to directly using the increased data throughput, the clock frequency of the processing modules can be lowered by a corresponding amount, since on average more data can be processed per clock cycle. Some case studies integrating processing modules for EEG data described with HLS are presented in Section 5.3 and evaluated in Section 6.2.
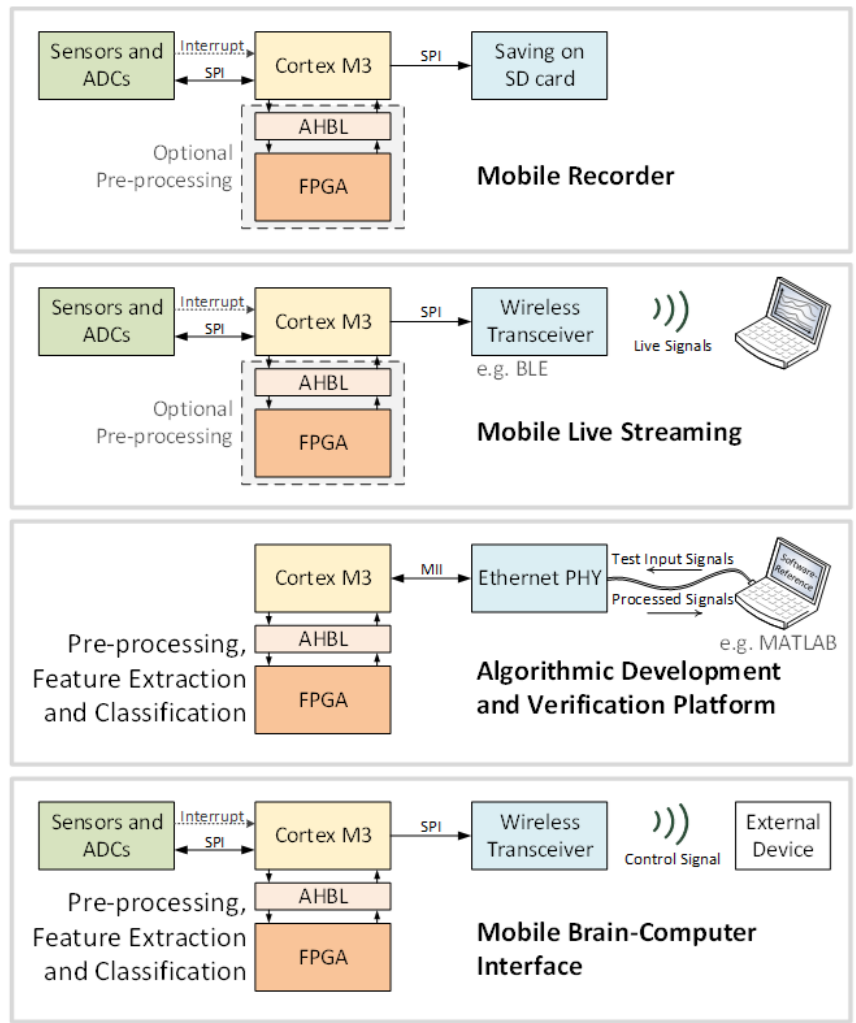
Figure 5.3: *Possible use cases of the CereBridge system (adapted from [Wah21])*

5.2.2. Possible Applications

With the described hardware modules of the CereBridge system and the proposed signal flow concept for the SoC, a flexible overall system for an EEG-based BCI is available. This system can cover a wide range of applications and can be used as a unified platform for the development, optimization and application of algorithms for EEG signal processing. Figure 5.3 summarizes the main applications of the CereBridge system.

On the one hand, it can be used as a mobile recorder of EEG signals (top of the figure). In this case, the potentials at the scalp are sampled from EEG electrodes by the used ADCs and transferred via SPI to the microcontroller of the SmartFusion 2 SoC. The microcontroller stores the data either raw or after preprocessing by the FPGA on the system's integrated microSD card memory.

The mobile live streaming of the recorded data is shown below. The only difference to the first application is the sink of the (possibly preprocessed) data at the end of the signal chain. In this case, the data is streamed wirelessly and can be visualized on the target platform, such as a PC or smartphone.

The next figure shows the use of the CereBridge system as a platform for algorithm development and verification. Typically, the development of algorithms is done first with offline data sets in software, e.g. Matlab. To verify the hardware integration of such an algorithm, it is recommended to use the same data set as input. For this purpose, the CereBridge system can be provided with test data from a PC (e.g. via Ethernet), which is received by the microcontroller. The corresponding hardware implementation of the algorithm is performed on the FPGA and the processing result is then transferred back to the PC through the microcontroller. On the PC, the results of the hardware processing can be directly compared with the results of the software reference.

After testing the algorithms offline and verifying their hardware integration, the algorithms can be used in the context of a mobile BCI (bottom of Figure 5.3), where the data is again obtained from the live-sampled EEG sensors and processed in the FPGA. The classification result can then be used directly as a control signal for external devices. As an exemplary application interface, a wireless connection (e.g. BLE) is shown here.

In summary, the flexibility of the CereBridge system makes it possible to use the same platform for all steps of algorithm development. If the EEG used for the software reference is already data recorded through this system, this guarantees uniform quality and properties of the EEG signals up to the application as a mobile BCI.

5.3. Case-Studies for Online EEG signal processing

This section describes example implementations of algorithms in the FPGA of the SmartFusion 2 SoC. Since the corresponding processing architecture is generated using HLS, the focus of the description is on possible applied optimizations and the corresponding hardware resource utilization of the respective algorithms. At the same time, the mathematical background is only briefly addressed, while references to the relevant literature are given where appropriate.

All values given for FPGA resource utilization are relative to the total hardware resources available within the used SmartFusion 2 SoC. These maximum values are as follows for the hardware components considered:

- LUT: 56,340
- DFF: 56,340
- LSRAM: 69
- uSRAM: 72
- DSP: 72

In order to clarify and standardize the effects of the respective optimization steps on the runtime of the computations within the case studies, the computation considers a sample number of 512 per EEG channel. In addition, a total of 16 EEG channels are processed, with the corresponding processing architecture being reused, i.e. the channels are computed sequentially one after the other. As a consequence, about 22 LSRAM blocks of the FPGA are used to store the complete input and output data of the processing. This value is included in the results, even though the algorithm does not necessarily require it to be that large.
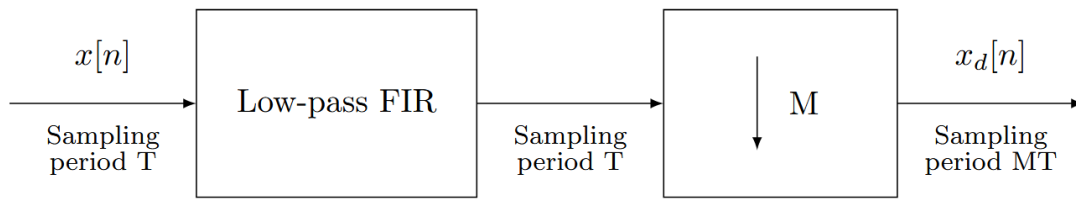
Figure 5.4: *Schematic of the processing associated with the first case study. The incoming signals are low-pass filtered before the sampling rate is reduced. (adapted from [Li23])*

All implementations were simulated with the corresponding HLS tools and verified against the software reference. Exactly two case studies are described here: Case study 1 highlights the HLS optimization using the simple directive to apply loop pipelining. Case study 2 shows how different approaches to implementing the same algorithm can be quickly implemented using HLS. The optimizations applied are loop unrolling and the use of an appropriate fixed-point data format.

Both case studies will be evaluated in Section 6.2 regarding their processing latency and the power consumption in the context of the complete CereBridge system.

5.3.1. Case-study 1: Filtering and Downsampling

This case study describes a simple preprocessing of the acquired EEG signals. Figure 5.4 visualizes the implemented processing steps, which consist of a low-pass filter and a downsampling module. Downsampling is used to reduce the data rate of the recorded EEG signals. This can simplify subsequent processing steps or reduce the amount of data to be transmitted wirelessly or stored within the CereBridge system.

The basis for the implementation of the digital filter is an Finite Impulse Response (FIR) filter, which is a linear, time-invariant system with a finite number of filter coefficients. These coefficients influence how each frequency component of the incoming signal waveform is modified. Since the hardware implementation of an FIR filter is independent of the chosen coefficients, they can be easily replaced if needed.

For filtering the recorded EEG signals in the context of this case study, the filter fulfills two main tasks. On the one hand, high-frequency signal components (e.g. $> 30\,\mathrm{Hz}$), which are uninteresting for the application and may contain artifacts, can be filtered out. On the other hand, this low-pass filter is a necessary processing step before downsampling to avoid aliasing, i.e. distortions in the signal.

With the preceding low-pass filter and a suitable choice of coefficients (i.e. cutoff frequency), the downsampling module can be implemented simply by retaining only one sample of a group of consecutive samples of the original signal. For example, if only every other sample is retained, the sampling frequency would be halved.

68
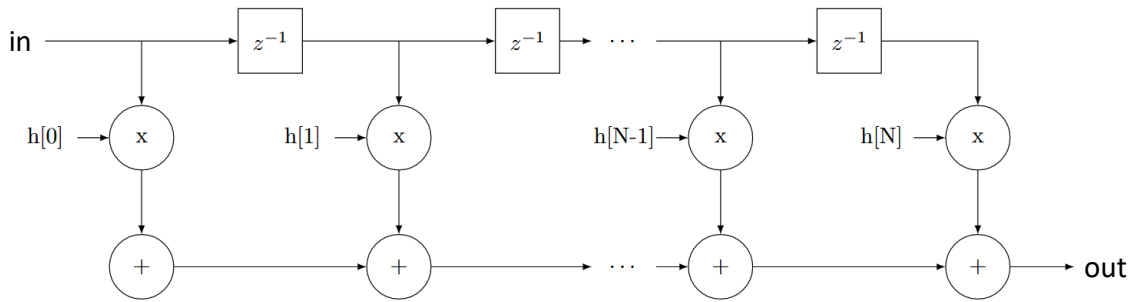
Figure 5.5: *Working principle of an N-coefficient FIR filter (adapted from [Li23])*
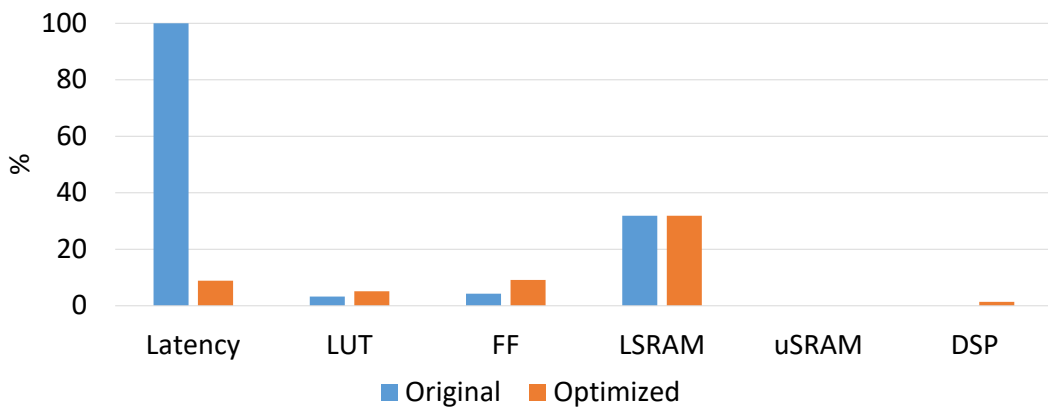
Figure 5.6: *Comparison of latency and resource usage between the original and optimized implementations of the filtering and downsampling module (adapted from [Li23])*

Implementation of FIR and Downsampling Module

The structure of the hardware implementation of a FIR filter is shown in Figure 5.5. The mathematical operations on the input data can be divided into two groups: the delay units (z^{-1}), which are implemented as registers in the FPGA, and the Multiply-Accumulate (MAC) operations with the corresponding filter coefficient $h[x]$. These MAC operations can be efficiently implemented with the built-in DSP units if the data format, especially the data width, is suitable. For this case-study, the number of filter coefficients is set to 11. Downsampling can also be directly integrated into this architecture by storing the outputs of the FIR filter only periodically.

In addition to a comparatively fast implementation of this hardware module, the use of HLS also allows easy and accelerated application of optimization techniques. Figure 5.6 shows a comparison of the processing latency and resource requirements of two implementations of the described FIR filter with downsampling. The latency is relative and normalized to the slower implementation, which requires 475,029 clock cycles. The other values shown in the figure denote the corresponding resource consumption in the FPGA and are given relative to the total number of available resources.

The implementation labeled "Original" in Figure 5.6 refers to a straightforward implementation of the FIR filter with downsampling described above, without applying specific HLS optimization directives. The second implementation, "Optimized", uses the loop pipelining directive to
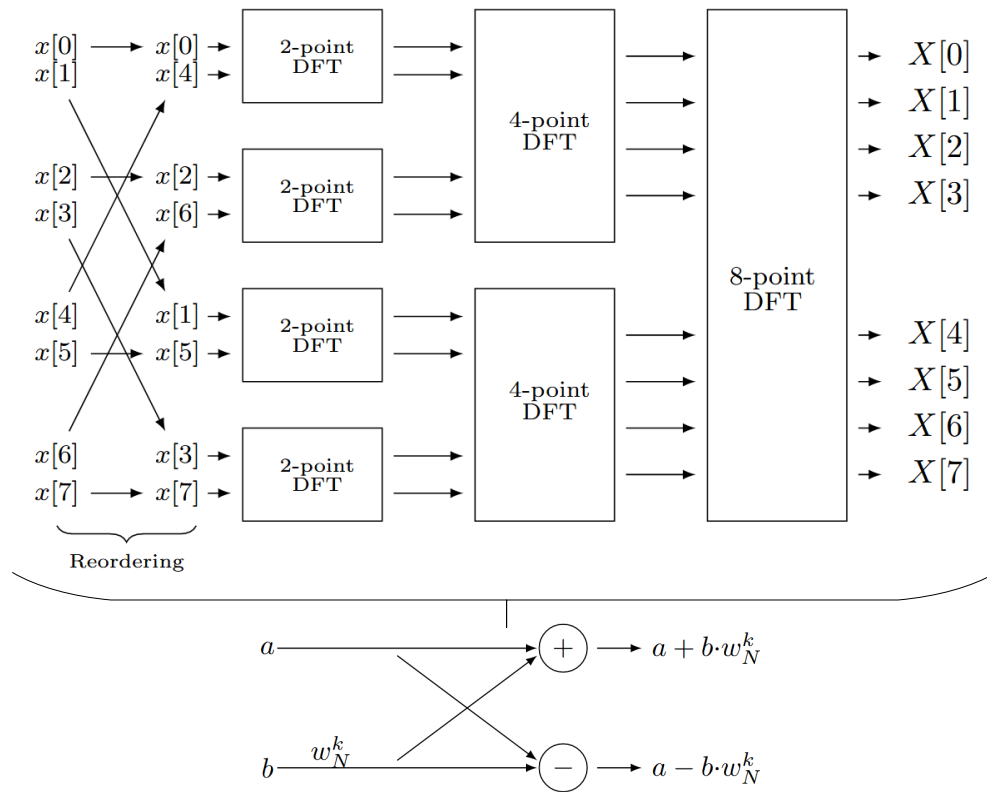
Figure 5.7: *Structure of an examplary 8-point FFT implementation (top), which can be subdivided into the Butterfly units shown below (adapted from [Li23])*

significantly reduce processing latency to 42,135. The tradeoff is a slight increase in resource requirements for LUTs, FFs, and DSPs, as shown in Figure 5.6.

5.3.2. Case-study 2: Fast Fourier Transform

The Fast Fourier Transformation (FFT) transforms incoming data into the frequency domain. As can be seen in Table 2.9, this is regularly applied to EEG data. The FFT is most commonly assigned to the Feature Extraction processing step and, sometimes, a simple subsequent thresholding is sufficient as a classifier for certain applications [Lin16; Tse15].

In the context of this case study, the so-called Decimation In Time (DIT) approach is chosen for the realization of the FFT, which divides the time-domain sequence into subsequences and computes them separately for the most part.

A schematic representation of an 8-point DIT FFT is shown in Figure 5.7. However, the blocks shown can be further subdivided and traced back to a regular processing unit called a "butterfly" [Opp72]. From this basic 2-point FFT component, FFT implementations with a length of the power of two can be built up regularly.
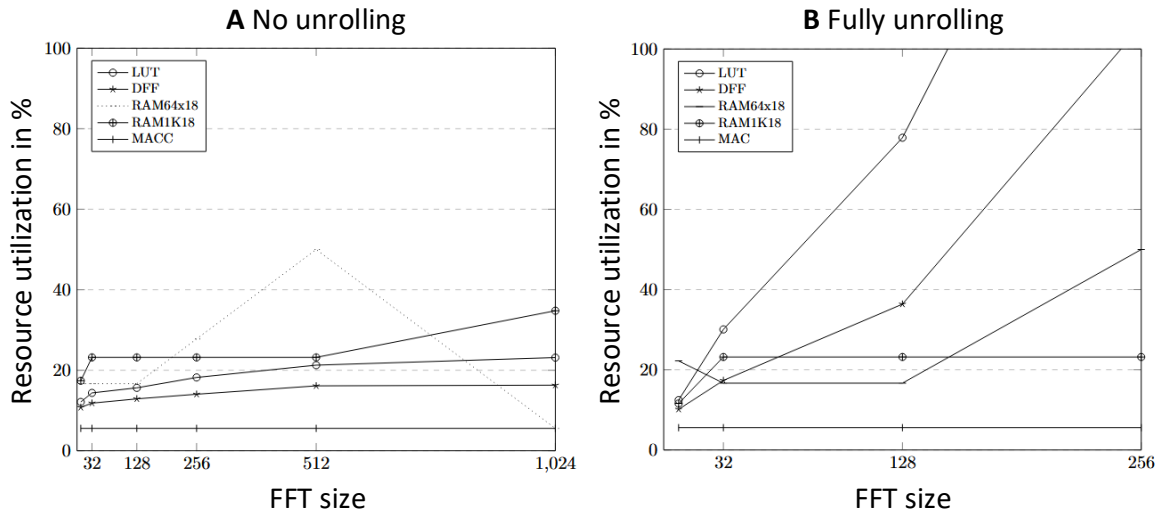
Figure 5.8: *Effect of loop unrolling on the hardware resource utilization for the Radix-2 FFT (adapted from [Li23])*

Implementation of FFT

The so-called radix-2 DIT FFT is one of the most widely used implementations and is therefore chosen as the starting point here. Exactly as shown in Figure 5.7, this method divides a discrete fourier transform into two interleaved ones of half length at each recursive step [9]. Since 512 samples are assumed on the input side, a 512-point FFT implementation is also focused here.

This case study shows the effect of loop unrolling optimization in HLS, which is directly related to the number of butterfly units applied in the implementation. Figure 5.8 shows the impact of full loop unrolling optimization on hardware resources for different FFT sizes. It can be seen that without loop unrolling (A), the required hardware resources are only slightly dependent on the FFT size. With full loop unrolling (B), however, the hardware resources required rise substantially with increasing FFT size, so that only a maximum of 128 of the examined FFT sizes are possible.

One approach to achieving full loop unrolling with a 512-point FFT is to simplify the data format. The implementation described above is based on a FFT that use floating-point number representations. Since fixed-point arithmetic typically requires less hardware resources [Won95], it is considered here. Nevertheless, corresponding conversion and computation errors are to be expected with this approach. Therefore, the error should be estimated in order to find a meaningful fixed-point number representation.

Figure 5.9 shows the error estimate for a 512-point FFT for fixed-point number representations of different word lengths. The ordinate corresponds to the Mean Absolute Percentage Error (MAPE), which supports an intuitive interpretation of the relative error [De 16]. It is calculated as follows:

$$MAPE = \frac{1}{N} \sum_{n=1}^{N} \left| \frac{a_n}{ref_n - a_n} \right| \times 100\%$$

71
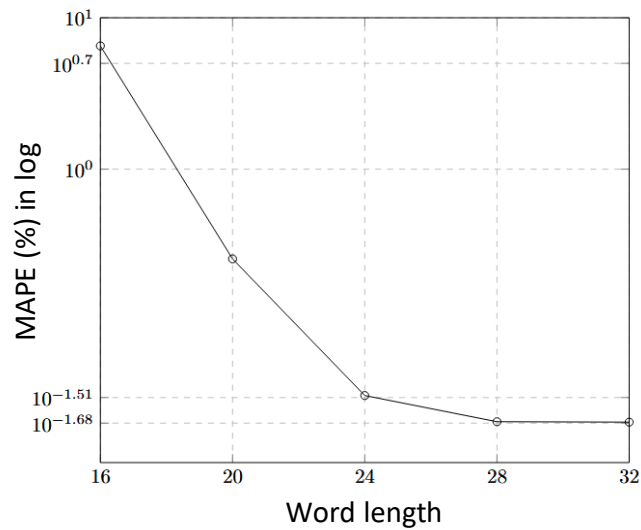
Figure 5.9: *Error estimation for different word lengths of fixed point data representation using a 512-point FFT implementation (adapted from [Li23])*
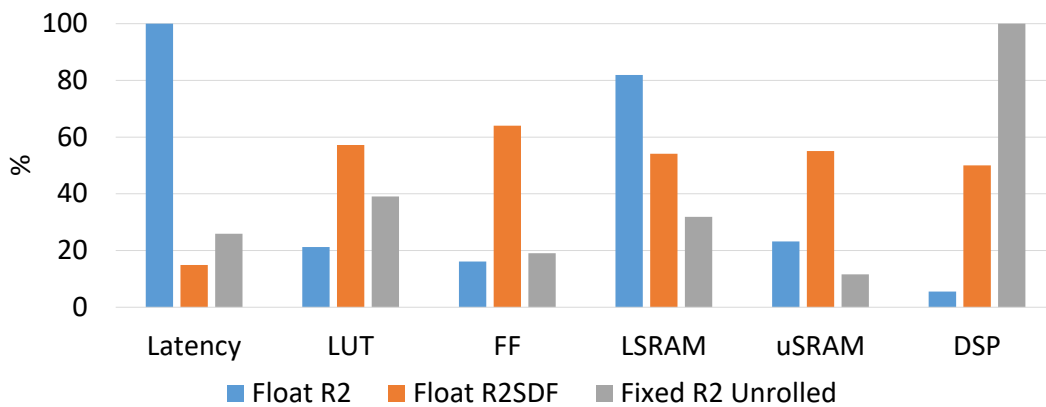
Figure 5.10: *Comparison of latency and resource usage between the original and optimized implementations of FFT module (adapted from [Li23])*

Figure 5.9 illustrates that a larger word length achieves a better accuracy of the fixed-point representation. At the same time, however, the effect diminishes and saturates with increasing word length. For a word length of 24, the average relative error is 0.31 %. However, in the context of this case study, a word length of 32 was chosen with an error measure of 0.21 %.

An alternative approach to mapping a 512-point FFT with loop unrolling optimization is to use a different calculation method. As an example, the so-called radix-2 single delay feedback method is implemented here, which extends the radix-2 algorithm with a feedback loop and is designed as a fast streaming-based FFT architecture [Rao14]. This is implemented using HLS with the floating-point data format and optimized for computational speed with complete loop unrolling.

Figure 5.10 summarizes the resource utilization and processing latency results of the three 512-point FFT algorithms implemented as examples. "Float R2" denotes the first implementation described, the Radix-2 without loop unrolling and floating point data format. It can be seen that this has a low hardware resource requirement, but the processing latency is the highest by far.

This is 1,128,688 clock cycles and was used to provide a normalized relative indication of the latency of the other two implementations. The radix-2 single delay feedback method is shown as "Float R2SDF" and also uses the floating-point data format. This uses significantly more resources than the original radix-2 variant, but also reduces the processing latency by about 85 %. The Radix-2 implementation with full loop unrolling and the 32 bit fixed point format is shown in Figure 5.10 as "Fixed R2 Unrolled". This also has a significantly reduced latency compared to the original radix-2 implementation, although this value is slightly higher than the "Float R2SDF". However, in direct comparison with this method, the fixed-point implementation of the radix-2 algorithm also consumes less hardware resources overall, except for the DSP units.

CHAPTER 6

Evaluation of the CereBridge System

After appropriate verification of all components of the CereBridge system and their functionality, the system components required to operate the system should be characterized and evaluated. Since the characteristics of the FPGA of the SmartFusion 2 SoC depend primarily on the implemented algorithm, it is not adressed here. Instead, the focus is on the hardware and data handling during EEG data acquisition. In addition, the impact of storing the recorded data on the included microSD card memory and transmitting the data via BLE is considered.

In Section 6.1, the power dissipation and timing characteristics are first determined quantitatively based on measurements. Based on this, the case-studies will be evaluated in Section 6.2 in the context of their application within the complete CereBridge system. Finally, the results are discussed in Section 6.3 with respect to the requirements and constraints and compared to other state-of-the-art BCI hardware platforms.

6.1. Quantitative Performance Analysis of Individual Modules

In the following, the hardware of the CereBridge system is evaluated in terms of power consumption and timing behavior during signal acquisition and for the wireless interface. The results of different measurements are discussed, which characterize the CereBridge system independent of application and algorithm.

6.1.1. Power Analysis

This section discusses the power requirements of the CereBridge system. Since the selection of a desired algorithm is intended to be flexible, the focus here is on the power consumption required for EEG signal acquisition and data processing in the SmartFusion 2 SoC. Based on

Table 6.1: *Measured current and calculated power of the two supply voltage rails for the ADCB during continuous sampling of 16 connected EEG electrodes with 250 samples per second*

	Analog power supply	Digital power supply
Voltage [V]	5.5	1.8
Measured Current [mA]	13.08	3.12
Power [mW]	71.95	5.61

this, total power consumption values are given for the two application scenarios Mobile Recorder and Mobile Live Streaming (see Figure 5.3).

In all cases, it is helpful not only to determine the total value, but also to be able to quantify the contribution of each circuit group to the power dissipation. This allows to identify the parts that contribute the most to the power dissipation and, if necessary, discuss trade-offs for optimization.

To determine the power dissipation values, the modules of the CereBridge system can be measured individually during operation. However, the Programming and Debugging Board (PRGDB) was not included in this study because it is intended for stationary use only and therefore does not require a mobile power supply.

Analog-to-Digital Conversion Board (ADCB)

To measure power dissipation, the ADCB was connected to two cEEGrid sensors and plugged onto the PRGDB together with an MSTRB. The data lines between the two modules were connected via the pin headers, and the power supply for each module was provided separately from an external laboratory power supply. This way, the two modules could communicate with each other, while the current draw for the ADCB could be determined individually.

The ADCB was powered by two separate voltages: 5.5 V for the analog supply and 1.8 V for the digital supply. Exactly the same voltages would be provided by the MSTRB if both modules were connected directly. The MSTRB is also initializing the configuration of the two ADS1299 ADCs used on the ADCB and starts a continuous sampling of the 16 EEG channels at 250 samples per second with a resolution of 24 bits. The data is periodically read from the ADCs via SPI when new samples are available.

Table 6.1 summarizes the measured current consumption and the calculated power dissipation on the two voltage rails of the ADCB. The current consumption was averaged over 10 s during operation. The current consumption and power dissipation mainly contains the power of the two ADCs. However, it also includes the small power dissipation of the remaining components on this module, such as the linear voltage converter, which generates the 5 V required by the ADCs from the 5.5 V supply voltage.

Wireless Board (WILB)

For the WILB presented here, two different versions were implemented, which can transmit incoming data wirelessly via BLE. Depending on the version of the module and the SiP used
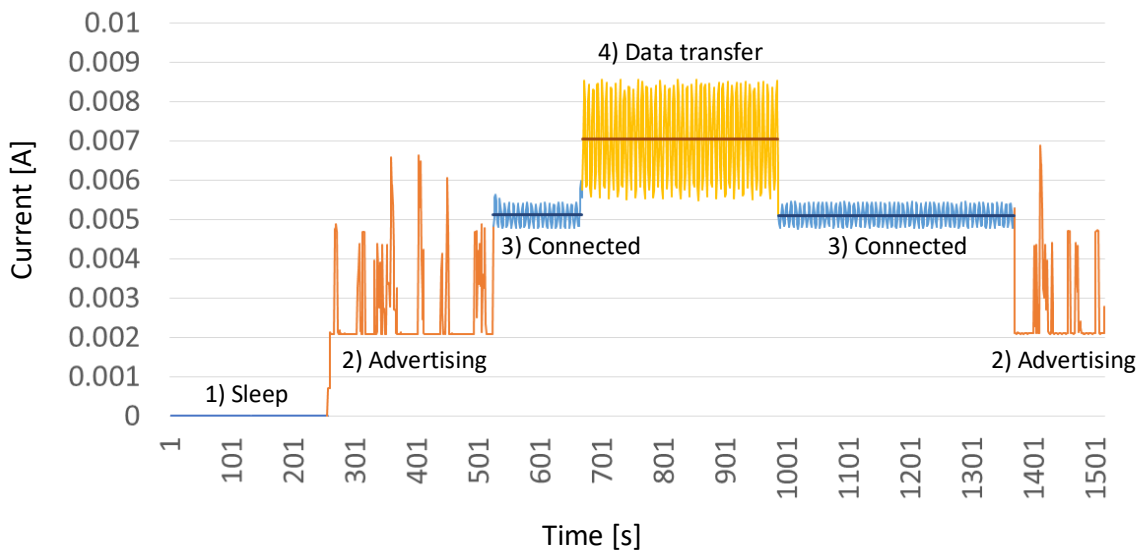
Figure 6.1: *Current consumption for the ISP1507-AX version of the WILB module with a supply voltage of 3 V during several operation modes (adapted from [Mao19])*

(AX or AL), different values could be measured. The AL version is explicitly aimed at low-power applications, while the AX version is expected to provide higher performance.

The two SiPs ISP1507-AL and ISP1507-AX are based on different microcontrollers from Nordic. Corresponding firmware templates with the appropriate Bluetooth stack are already available. The software stacks used are SoftDevice S112 (AL) and SoftDevice S132 (AX). The firmware was configured so that after initialization and connection to a wireless receiver, incoming data to the SiP via UART is sent directly wirelessly. Since the usage of the wireless interface depends on the actual application and the amount of data, continuous transmission with maximum throughput was considered.

The WILB was also individually tested and measured for power dissipation. A suitable laboratory power source and appropriate data transmission lines were connected by cable and the power consumption on the power supply line was measured.

It was observed that the measured power consumption strongly depends on the currently active operating mode of the SiP. The measured current consumption in different operating modes is shown in Figure 6.1 as an example for the AX version with a supply voltage of 3 V. The SiP is in "Sleep" mode at the beginning of the measurement. The "advertising" mode is present when the SiP is brought to a fully active state but with no direct wireless connection to a specific receiver. After a connection to a receiver has been established, the SiP is in "Connected" mode, although no active data transmission is taking place. Active data transmission only takes place in the "Data Transmission" mode. Since the power dissipation is primarily relevant for the ongoing data transfer, the average current draw in this mode is explicitly considered in the following. For longer periods of time when no wireless connection is required, the use of the "Sleep" mode can significantly reduce the power dissipation of the WILB module to about 1.8 µW.

The MSTRB can provide several selectable voltages to supply the WILB, so the influence of this supply voltage could be investigated. Figure 6.2 shows the course of the power dissipation calculated from the measured current consumption for both variants of the WILB. A Bluetooth
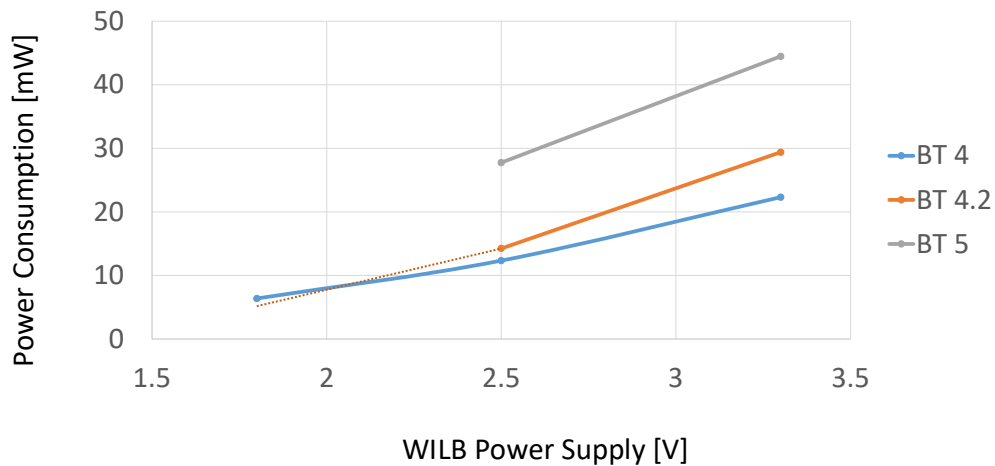
Figure 6.2: *Calculated Power Consumption from measured current draw of the WILB module for different power supply voltages. Different Bluetooth (BT) versions have been considered, with the BT 4 implemented on the AL and BT 4.2 as well as BT 5 used by the AX version. (adapted from [Mao19])*

4 connection was established for the AL variant, while Bluetooth 4.2 and Bluetooth 5 were considered for the AX variant. The reason for this is that the software stack for the AL variant only offers a basic set of configuration options for the BLE connection and therefore cannot benefit from a higher Bluetooth standard. Supply voltages of 1.8 V, 2.5 V and 3.3 V were investigated, as these can be provided by the MSTRB at the corresponding connector for the WILB module. It can be seen that the power dissipation can be significantly reduced with lower supply voltages. In addition to the influence of the voltage on the power dissipation, a reduction of the current consumption can also be seen on the basis of the gradient of the connected measuring points.

For the AL version of the WILB with Bluetooth 4, a supply voltage of 1.8 V is suitable, with a power dissipation of 6.37 mW during continuous data transmission. Surprisingly, the AX version of the WILB with Bluetooth 4.2 connection has an even lower power consumption than the AL version at the same supply voltage. However, it was found that entering and waking up from sleep mode does not work reliably with this supply voltage for the AX version, which regularly gets stuck in a kind of freeze state. For this reason, this supply voltage is no longer considered for the AX version as indicated by the dashed line in Figure 6.2 and a voltage of 2.5V is used by default. The power dissipation for Bluetooth 4.2 is 14.25 mW and for Bluetooth 5 27.75 mW.

Master Board (MSTRB)

For the MSTRB, the power consumption was determined by connecting a laboratory voltage supply with 3.6 V to the battery connector and measuring the current draw. To take into account the overhead of the power management dissipation for the supply of the other modules, they should be connected at the same time. For this purpose, the two modules ADCB and WILB were connected to the MSTRB in the configurations described and the total current consumption was measured. Since the contributions of the other two modules in their respective modes are known, these values could be subtracted from the determined power dissipation. Thus, the

Table 6.2: *Power consumption for the MSTRB determined from the total power dissipation and the known values for the ADCB and WILB*

	Power Consumption [mW]
Total	189.76
ADCB	- 77.56
WILB (AX)	- 14.25
MSTRB	= 112.2
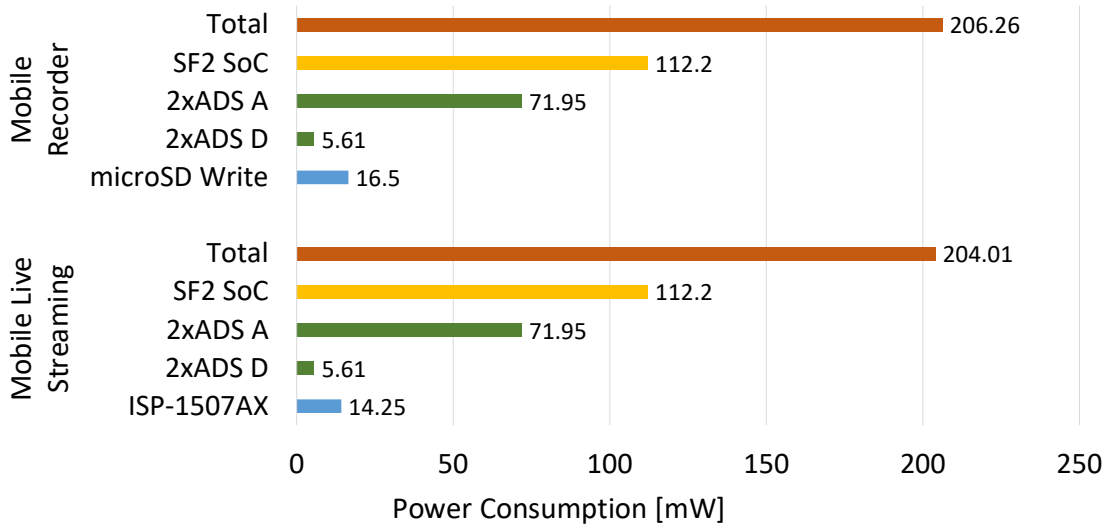
Figure 6.3: *Measurements of power consumption by components for different CereBridge applications*

resulting power dissipation value primarily contains that of the SoC. It also includes the other components of the MSTRB, including the power management.

Table 6.2 shows the determined total power dissipation and the calculated share for the MSTRB after subtracting the known values for the ADCB and WILB modules. As described above, 16 EEG channels are recorded at 250 samples per second and read out by the SmartFusion 2 SoC. These are then transmitted to the WILB in the AX version, which sends them via BLE in Bluetooth version 4.2. It can be seen that the MSTRB is the largest contributor to the total power dissipation with approximately 112.2 mW. However, it should be noted that the ARM Cortex-M3 operates at 40 MHz during this measurement. Depending on the application and other required components, this clock frequency and thus the power dissipation can be reduced. Since 40 MHz was used for the clock frequency in the case studies, this value is highlighted here.

Complete System

Now that the power dissipation of the individual modules has been determined, the power dissipation for the use of the entire system in specific applications can be derived. The two application scenarios Mobile Recorder and Mobile Live Streaming (see Figure 5.3) are particularly relevant, as they do not depend on the use of specific algorithms.

24 bit EEG channel data

Good data	Positive lead off	Negative lead off	GPIO Regs	Channel 1	Channel 2	...	Channel 8
4	8	8	4				

24 status bit
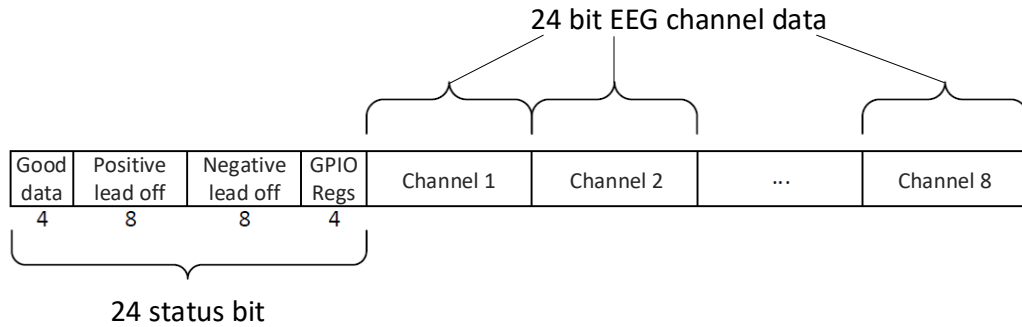
Figure 6.4: *Structure of data to be read out over SPI from each ADS1299 ADC for every sample time (adapted from [Mat17])*

Figure 6.3 summarizes the corresponding measured values for the power dissipation of the CereBridge system in the two scenarios. For the Mobile Recorder, a microSD card was used as a non-volatile data storage device. It was used and written with the recorded EEG signals via SPI. Its power dissipation cannot be measured directly in the system, but its contribution was determined by the difference of the sum from Table 6.2. For the Mobile Live Streaming application, the WILB is listed with the ISP-1507AX and a BLE connection via Bluetooth 4.2.

It can be seen that both application scenarios have similar power consumption values. The battery life can be estimated based on these values, using the 1800 mA lithium-ion battery described above as the power source and considering a nominal voltage of 3.6 V. For the described Mobile Recorder application, the battery life is 31.4 h. For the Mobile Live Streaming application, this value is 31.7 h. Thus, in both cases, the achieved battery runtime is well above the required 16 h.

It should be noted that the power dissipation values and thus the determined battery runtime were determined for continuous operation and without explicit power optimization strategies. If it is of interest in the context of an application to further reduce this value, several approaches would be plausible. First, the clock frequency of the SmartFusion 2 SoC could be reduced to a value that just meets the requirements to handle a set of EEG data before a next set is available at the ADCs. In addition, power saving modes can be used as long as continuous operation is not required or at least there are regular larger time gaps in processing or data handling. Sleep mode could also be used for the WILB, especially if data can be sent in bundles at the cost of increased average latency.

6.1.2. Timing Specifications

In this section, the algorithm-independent timing specifications of the CereBridge system are investigated and determined. Therefore, the corresponding properties of the ADCB and the WILB are characterized in the following.

For the ADCB, the timing mainly depends on the selected serial clock frequency of the used SPI interface. The data to be transmitted by an ADS1299 ADC is shown in Figure 6.4. The first 24 bit correspond to status information of the ADC, including information about the good electrical contact between the electrodes and the scalp (lead off detection). These status bits are followed by the individual digital values for the eight available EEG channels with 24 bit each.
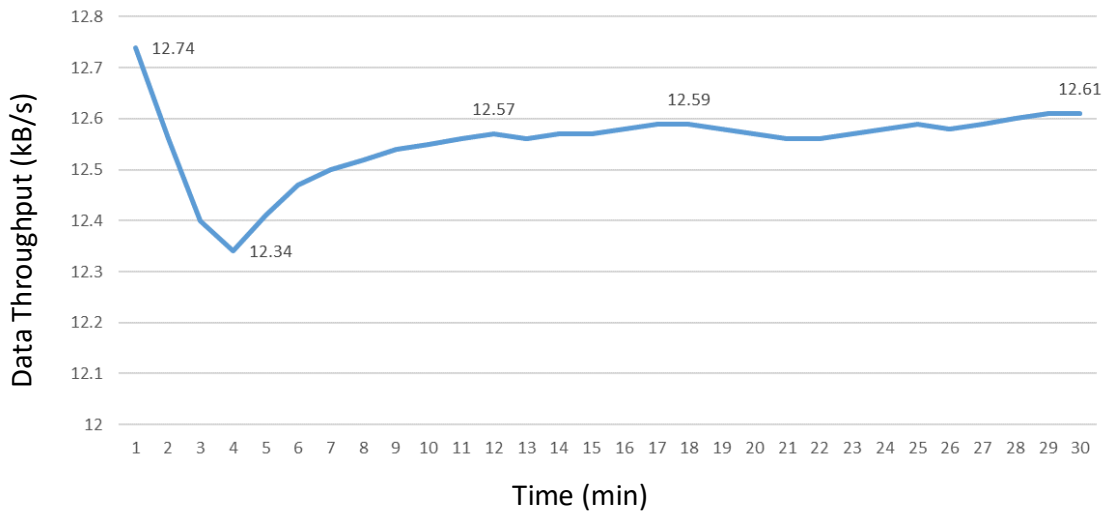
Figure 6.5: *Data throughput stability for the ISP1507-AL version of the WILB module (adapted from [Mao19])*

Consequently, when reading out each ADS1299 ADC that samples 8 EEG channels, a total of $9 * 24\,\text{bit} = 216\,\text{bit}$ must be transferred to the SmartFusion 2 SoC via SPI. Furthermore, it has been investigated that a clock frequency of up to 2 MHz for the SPI ensures a stable and error-free data transfer [Mat17].

In general, if both ADCs are to be used and read out, all 16 channels should be sampled as simultaneously as possible. If the two ADS1299 ADCs each generate and use their own sampling clock, there will be shifts in the sampling time and thus a different number of EEG samples per ADC over a longer period of time. Therefore, the ADS1299s were configured so that both are based on the generated clock of one ADS1299. Measurements have shown that the difference in sampling times is drift-free and below 50 ns, so no difference in the amount of data per ADC can occur. Reading out the data of both ADCs via SPI takes on average about 260 μs.

Furthermore, the properties of the wireless interface provided by the WILB are of particular interest. Primarily, the achievable data throughput of the different versions of the WILB and the associated long-term stability are investigated.

First, the throughput was measured over a period of 30 minutes using the AL version of the WILB and Bluetooth 4. Data is continuously transmitted from the AL version of the WILB and received by a Bluetooth 4 USB dongle on a PC. A dedicated software calculates and outputs the average amount of data received per minute.

The resulting curve is shown in Figure 6.5. It shows that there are slight fluctuations in the average data throughput. However, these fluctuations are within 2 % of the average, so long-term measurements are not required to determine throughput. This also means that a data transfer with higher data volumes from the CereBridge system to external devices can take place with long-term stability.

Moreover, for BLE based on Bluetooth versions 4 (AL), 4.2 (AX) and 5 (AX), different configurations and parameter choices were investigated to maximize the data throughput. The same setup as for the throughput stability measurement was used for the AL version. For AX with Bluetooth 4.2, an appropriate Bluetooth 4.2 USB dongle was used. For Bluetooth 5, no

Table 6.3: *Throughput and power consumption measured at different supply voltage levels for BLE Bluetooth 4 (AL), 4.2 (AX) and 5 (AX) of the WILB*

BLE Version		Supply Voltage [V]	Throughput [kB/s]	Power Consumption [mW]
AL	4	1.8	12.7	6.37
	4	2.5	12.7	12.33
	4	3.3	12.7	22.31
AX	4.2	1.8	21.7	-
	4.2	2.5	21.7	14.25
	4.2	3.3	21.7	29.4
AX	5	1.8	62.38	-
	5	2.5	62.38	27.75
	5	3.3	62.38	44.484

USB dongle was available at the time of the measurements, so a second WILB connected to the PC was used as a receiver.

It could be shown that a connection interval of 7.5 ms achieves the highest data throughput [Mao19]. On the ISP-1507AX, the so-called data length extension for Bluetooth 4.2 and 5 could also be activated, which additionally increases the data throughput.

The average BLE throughput measurements for the different Bluetooth versions and the two WILB variants are summarized in Table 6.3. Only the configurations described above, which result in the maximum data throughput, were listed. In addition to the different Bluetooth versions, different voltages for the power supply were also examined, but these have no effect on the achievable data throughput. It can be seen that the WILB variant and the Bluetooth version used have a significant influence on the data throughput. While the low-power AL version with BLE achieves a throughput of 12.7 kB/s with Bluetooth version 4, this value is almost doubled (Bluetooth 4.2) or almost quintupled (Bluetooth 5) with the AX version. For completeness, the power consumption is also listed in the table.

Assuming 16 EEG channels are sampled with 250 samples per second and 24 bit resolution, the data amount to be transmitted is $16 * 250 * 24\,\text{bit} * 1\,\text{B}/8\,\text{bit} = 12\,\text{kB}$ per second. For data transmission of the CereBridge system via BLE, this means that the data throughput achieved by the AL version of the WILB and Bluetooth 4 is already sufficient. However, the AX version will be needed when data is recorded at a higher sampling rate (up to 1 kHz of uncompressed data with Bluetooth 5) or other additional data (e.g. transmitting all raw data and processed EEG data) is desired to be transmitted.

6.2. Evaluation of FPGA-based processing

The two case studies described in Section 5.3 have shown that implementing algorithms on the FPGA of the SmartFusion 2 SoC is feasible and can be implemented and optimized in a time-efficient manner using HLS. At this point, FIR filtering and downsampling as well as FFT are evaluated in terms of power dissipation and processing latency for the considered implementations of the two case studies. The underlying clock frequency is 40 MHz in all cases.
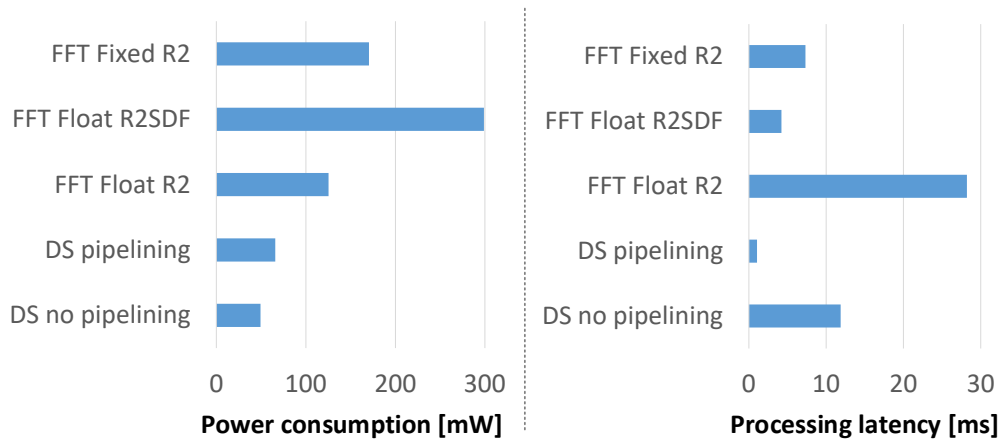
Figure 6.6: *Comparison of Power Consumption and Latency of different algorithmic implementations for the described case-studies Downsampling (DS) and FFT*

Figure 6.6 shows the corresponding values for the five different processing implementations (3× FFT, 2× downsampling). By showing the power dissipation and processing latency next to each other, one tradeoff between the different implementations is also clearly visible. The implementations of a processing type usually show a higher power dissipation when the processing latency is comparatively low.

For the downsampling of all 16 EEG channels, the power dissipation is 49.25 mW and 65.81 mW, respectively. The processing latencies are 1.05 ms and 11.88 ms. This shows on the one hand that the processing is well below the required 100 ms. On the other hand, the determined power consumption in sum with the rest of the system including the wireless unit results in a total power dissipation of 253.26 mW (no loop pipelining) and 269.82 mW (loop pipelining) for low pass filtering and downsampling of live recorded EEG data. This results in a battery life of more than 24 hours in both cases.

The FFT is computationally more complex, which can be seen especially in the power consumption values. The corresponding values are 125.37 mW (floating-point radix-2 FFT), 298.85 mW (floating-point radix-2 single delay feedback FFT) and 170.43 mW (fixed-point radix-2 FFT). This results in battery run times of 19.7 h, 12.9 h and 17.3 h for the entire system. Thus, even with continuous processing of all input channels with the radix-2 implementations, battery run times would still exceed the 16 h demanded for pure EEG signal acquisition. The processing latencies of 18.22 ms, 4.21 ms and 7.31 ms achieved by the different implementations are all below the required 100 ms.

In summary, processing 16 EEG channels on the FPGA is feasible and HLS provides an adequate tool for accelerating the integration of algorithms.

6.3. Discussion and Comparison with Requirements

Based on the measurements presented in this chapter, it could be shown that the CereBridge platform fulfills all requirements for a mobile EEG-based BCI system. Especially for the two algorithm independent application scenarios Mobile Recorder and Mobile Live Streaming, concrete

Table 6.4: *Features of the CereBridge system in comparison to the requirements defined in Section 4.1*

Requirements	CereBridge feature
Interchangeable EEG sensors with at least 16 channels	The components for connecting EEG sensors are integrated on a separate board (the ADCB) within the modular CereBridge hardware, allowing it to be adapted to changing sensor requirements. The ADCB version discussed in this work provides two ADCs for the connection of 16 passive EEG electrodes with state-of-the-art signal quality (24 bit resolution and 250 to 16,000 samples per second). With a different PCB design, up to 32 EEG channels could be supported by one ADCB.
Configurable processing hardware architecture	EEG signal handling and processing is performed on the heterogeneous processing architecture included in the SmartFusion 2 SoC. It consists of a low-power Flash-based FPGA and an ARM Cortex-M3 microcontroller. The number of hardware resources available within the FPGA is chosen based on many state-of-the-art publications describing the implementation of BCI-related processing algorithms on FPGAs. Therefore, it is sufficient to implement a variety of BCI-related signal processing.
Self-sufficient operation	The CereBridge system is completely independent of any additional hardware or connections. It includes all necessary steps from initialization, EEG recording, processing and data handling without the need for external interaction.
Mobility (total weight $< 300\,g$)	All required components are assembled into a small form factor hardware system that can be mounted on the head. The actual weight of the mobile CereBridge system, including an examplary 1800 mA h battery and two cEEGrid sensors, is 56 g, well below the requirement.
Low power consumption ($< 1\,W$)	The components for the CereBridge hardware were selected with emphasis on low power. In addition, the flexible processing hardware allows for power-optimized algorithm integration. During mobile EEG acquisition and either storing the data on an integrated microSD card memory or sending the results via BLE, approximately 205 mW of power is required. This results in a battery life of more than 31 hours.
Throughput and latency considerations	No latency drifts during recording of EEG data. Throughput for wireless BLE interface is capable of transmitting all recorded EEG data with sampling rates up to 1000 Hz. Furthermore, filtering and downsampling processing of 16 EEG channels can be as fast as 1.05 ms and an integrated 512-point FFT implementation for 16 EEG channels can finish computations within 4.21 ms.
Unified hardware	The CereBridge system represents a unified hardware platform for algorithm development and testing. The proposed firmware and data handling framework supports this approach, resulting in application options for the CereBridge system ranging from mobile EEG recording, mobile EEG streaming, stationary algorithm verification, and mobile BCI platform.
Extensibility	Various connection and interfacing options are provided on the hardware of the CereBridge system. A wireless interface as well as pin headers and a cable connector are available. Wired interfaces include UART, SPI, I2C and MII.
On-board memory options	Several types of memory are available on the MSTRB module of the Cerebridge system. A 64 MB LPDDR SDRAM is available as a dedicated IC with comparatively high read and write speeds. In addition, microSD cards of variable capacity can be inserted on the board to provide large non-volatile data storage. The SmartFusion 2 SoC also includes 1314 kB of embedded memory.
User interaction	The MSTRB module provides three configurable user push buttons. A total of five LEDs, two of which are freely programmable, can be used to provide status information to a user. However, no user interaction is required for the basic operation of the system.
Reproducibility	All components used in the CereBridge system are commercially available.

Section 1: Device Mobility Score (D)	
0	Off-body with cable connection
1	Backpack
2	Waist-mounted
3	Head-mounted EEG plus off-body or backpack
4	Head-mounted EEG plus smartphone/tablet
5	Completely head-mounted system

Section 2: System Specification Score (S)			
	Resolution [bit] +	Sampling rate [Hz] +	Battery life [h]
1	14	125 or 128	cable
2	16	250 or 256	1 to 8
3	22	500 or 512	9 to 16
4	24	1000 or 1024	17 to 24
5	>24	>1000	>24

Figure 6.7: *Used scoring system for the comparison of the CereBridge system with its values marked in red*
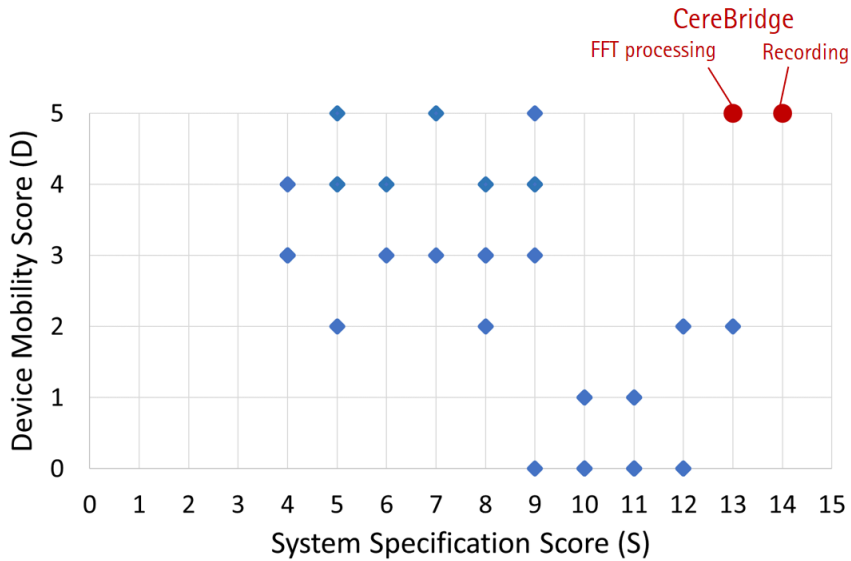
Figure 6.8: *Visualization of selected scores for device mobility (D) and system specification (S). The CereBridge system presented and evaluated within this thesis is marked in red with two configurations.*

values for power dissipation and expected battery life could be determined. For a mobile BCI, which also includes the corresponding data processing and classification of the EEG data, a suitable framework and with HLS a tool for the accelerated integration of algorithms are available.

Table 6.4 compares and discusses all features with the requirements and constraints for a mobile BCI platform mentioned in Section 4.1. When possible, concrete values for the performance of the CereBridge system are also given.

In conclusion, it will be shown that the CereBridge system represents an unprecedented solution for a mobile BCI system. For this purpose, the CereBridge system is compared to the embedded processing platforms considered in Section 2.4, based on the reviews of [Bel21] and [Bat17]. The Figure 2.11 serves as a starting point.

The scoring for the two relevant underlying categories, System Specification (S) and Device Mobility (D), is summarized in 6.7. The marked entries show the characteristics of the CereBridge system as evaluated in this thesis. The given two different numbers for battery life depend on the application of the CereBridge system: For continuous EEG recording and saving or transmitting of the data, the battery life is well over 24 hours. However, with additional FFT processing of all recorded EEG data, the power consumption of the CereBridge system increases, resulting in a reduction of the battery life score from 5 to 4.

With these known features of the CereBridge system, its characteristics can be compared to other hardware platforms for EEG recording and, in part, processing. The result is shown in Figure 6.8. It can be seen that although there are several implementations with the maximum device mobility score, they have so far achieved a maximum value of 10 out of 15 for the device mobility score. With the CereBridge system, this score could be increased up to 14. The only contribution to this score for the CereBridge system that prevents a maximum score of 15 is the resolution of the recorded EEG data. According to [Bat17], a resolution of > 24 bit is required to achieve a maximum score. Nevertheless, the CereBridge system outperforms all other platforms considered.

In addition, most of these other systems have little to no processing capabilities included as part of the mobile hardware. The use of a SoC with heterogeneous hardware architecture for digital signal processing of EEG data, as in the CereBridge system, provides a highly flexible and powerful hardware solution for a mobile BCI system.

CHAPTER 7

Conclusion

A system for online EEG signal processing within a mobile Brain-Computer Interface (BCI) places special demands on the hardware used. A flexible and adaptable hardware concept is required, especially if the use is not limited to a specific application. Furthermore, a fully mobile BCI system including sensors and power supply should be small and light enough to be worn unobtrusively on the head. In addition, a special focus on a low power design is essential so that longer-term operation of the system is possible with a mobile battery power supply. Finally, an appropriate concept for firmware, data handling and hardware configuration should be available to efficiently adapt to changing requirements between different algorithms.

The goal of this work was to discuss and evaluate all necessary steps for the realization of such a fully mobile BCI that can interpret brain activity based on recorded EEG data. For this purpose, several key research questions were defined. The first research question was to find a suitable system concept that allows a high degree of flexibility while still achieving good performance. The second research question explicitly refers to a hardware architecture suitable for digital signal processing in this context. This architecture must allow an efficient implementation of different algorithms and therefore provide sufficient hardware resources. Further desired features and interfaces that support the flexibility of the system and its applicability in different application scenarios are defined as the third research question. Finally, the question of appropriate evaluation methods and their application to the features, characteristics and limitations of such a system is raised. In all steps described, possible trade-offs in the development and optimization of such a system will be considered and discussed. The results of these research questions should provide understanding of the hardware required for mobile BCIs and provide insight into the design of BCI systems.

First, the processing steps within a BCI system were described and an overview of possible methods for measuring brain activity was given. The method used in this thesis is EEG, which is non-invasive, offers high temporal resolution and is suitable for mobile applications. Based on this, an overview of the current state of research on signal processing of brain activity measurements

from preprocessing to feature extraction and classification was given. Furthermore, different application areas of BCIs were described. Finally, existing platforms for mobile EEG measurement were discussed and a method for evaluating these platforms was presented.

In a design space exploration, possible hardware architectures for digital signal processing were first introduced and compared for application in a mobile BCI. An FPGA was identified as the main target hardware architecture for flexible and efficient EEG signal processing, and its fundamentals and differences among available FPGAs were discussed. Subsequently, several state-of-the-art implementations of BCI-related algorithms on FPGAs were reviewed.

Based on the described state of research on BCIs and FPGA architectures, a systematic conceptual design and implementation of a mobile BCI hardware, the CereBridge system, was performed. The requirements and constraints for such a system were discussed before essential components were identified, compared and selected. These are in particular suitable ADCs adapted to the characteristics of EEG signal acquisition as well as the actual FPGA, which provides sufficient hardware resources for the integration of different desired algorithms. Compared to the state of the art, an FPGA with more than 56,000 LEs was found to meet the requirements. The core of the system is the SmartFusion 2 SoC, which integrates a low-power FPGA of appropriate size with an ARM Cortex-M3 within a heterogeneous IC. Appropriate power management of the system was also described, providing the various required supply voltage rails and allowing in-system charging of a connected lithium-ion battery. Based on these selected essential components, a suitable system concept for the realization of the CereBridge platform could be defined. For mobile use, this concept is based on three individual, modular boards. The first one, the MSTRB, represents the core of the system and contains the processing hardware for digital EEG signal processing as well as for initialization and control of other components. It also includes power management and data storage functions. The second module, the ADCB, contains the corresponding ADCs for high-quality recording of 16 EEG channels via passive sensors. The connected sensors are sampled at 24 bit and an adjustable sampling rate of 500 Hz to 16,000 Hz. The last module for mobile use is the WILB, which provides a wireless communication interface for possible external hardware using BLEs. The entire system can be powered by a single lithium-ion battery. If a desired application prefers stationary operation, an additional module can be added to the system to provide wired interfaces and additional power connections. The modular design of the system and the interfaces provided for expandability ensure a high degree of adaptability to changing requirements, such as the use of different sensors for measuring brain activity. Despite several interfaces to peripheral devices, the system is designed to work autonomously and does not require any external interaction for operation. All hardware for mobile use can be integrated with an exemplary 1800 mA h lithium-ion battery on a footprint of $36.5 \times 56 \, \text{mm}^2$ and weighs only about 56 g including two circumaural EEG sensors (cEEGrid).

To support and extend the flexibility of the hardware system, a signal flow concept has been proposed that can also accelerate the deployment and further development of embedded algorithms. The configuration of the SmartFusion 2 SoC is the main focus, since all processing steps as well as the control of the rest of the system are integrated in this SoC. In addition, High-Level Synthesis (HLS) has been introduced to port algorithms to the FPGA, which can significantly accelerate the algorithm development process. It also supports the rapid implementation of different variants of an algorithm to compare trade-offs and optimization goals. Since the entire CereBridge system is available, various applications have been sketched,

which are made possible by the flexible system concept and the appropriate implementation. Although the focus is on the hardware system as such, case-studies have shown how certain signal processing algorithms, i.e. downsampling and FFT, can be integrated on the SoC efficiently using HLS and optimized with respect to freely selectable design goals.

To answer the last research question, the overall system and the case studies presented were evaluated. The individual system modules were characterized with respect to their power dissipation and timing behavior. To answer the last research question, the individual system modules were characterized with respect to their power dissipation and timing behavior. It was shown that the use as a mobile EEG recording device, either with embedded data storage or live transmission via BLE, is possible for more than 31 h continuously with a 1800 mA h battery. The data throughput at the wireless interface is still sufficient to stream the digital signals of all 16 EEG signal channels to external devices without data compression. To evaluate possible integrated signal processing on the FPGA, the power dissipation for several algorithm variants is also investigated based on the case studies. The resulting battery life for continuous data acquisition and processing reaches 24 h to 25.6 h for downsampling and 12.9 h to 19.7 h for the FFT. In conclusion, the CereBridge system, including the integration of the proposed data handling and processing concept, fulfills all requirements for a mobile BCI system. In the context of a comparison with existing research platforms, it could be shown that the CereBridge system offers unprecedented performance and features for a mobile BCI.

With the completion of this work, the development methodology and implementation of a complete system for a mobile EEG-based BCI is available. This system meets the relevant requirements and can be used with different algorithms in different application scenarios. It can also accelerate the porting of algorithms from laboratory applications to the field. The hardware can be attached to a head on a small footprint, has been evaluated in terms of various design parameters, and also extends the current state of research in BCI hardware for real-world applicability.

Bibliography

[Agh16]   Amirhossein S. Aghaei, Mohammad Shahin Mahanta, and Konstantinos N. Plataniotis. "Separable Common Spatio-Spectral Patterns for Motor Imagery BCI Systems". In: *IEEE Transactions on Biomedical Engineering* 63.1 (Jan. 2016), pp. 15–29. ISSN: 0018-9294, 1558-2531. DOI: 10.1109/TBME.2015.2487738. URL: http://ieeexplore.ieee.org/document/7293143/ (visited on 08/07/2023).

[Alh23]   Hadeel Alharbi. "Identifying Thematics in a Brain-Computer Interface Research". In: *Computational Intelligence and Neuroscience* 2023 (Jan. 4, 2023). Ed. by Abdul Rehman Javed, pp. 1–15. ISSN: 1687-5273, 1687-5265. DOI: 10.1155/2023/2793211. URL: https://www.hindawi.com/journals/cin/2023/2793211/ (visited on 07/19/2023).

[Api21]   Andrea Apicella et al. "High-wearable EEG-based distraction detection in motor rehabilitation". In: *Scientific Reports* 11.1 (Mar. 5, 2021), p. 5297. ISSN: 2045-2322. DOI: 10.1038/s41598-021-84447-8. URL: https://www.nature.com/articles/s41598-021-84447-8 (visited on 08/06/2023).

[Ari10]   Dan Ariely and Gregory S. Berns. "Neuromarketing: the hope and hype of neuroimaging in business". In: *Nature Reviews Neuroscience* 11.4 (Apr. 2010), pp. 284–292. ISSN: 1471-003X, 1471-0048. DOI: 10.1038/nrn2795. URL: https://www.nature.com/articles/nrn2795 (visited on 08/09/2023).

[Ask14]   Jessica Askamp and Michel J.A.M. Van Putten. "Mobile EEG in epilepsy". In: *International Journal of Psychophysiology* 91.1 (Jan. 2014), pp. 30–35. ISSN: 01678760. DOI: 10.1016/j.ijpsycho.2013.09.002. URL: https://linkinghub.elsevier.com/retrieve/pii/S0167876013002523 (visited on 08/12/2023).

[Asp15]   Peter Aspinall et al. "The urban brain: analysing outdoor physical activity with mobile EEG". In: *British Journal of Sports Medicine* 49.4 (Feb. 2015), pp. 272–276. ISSN: 0306-3674, 1473-0480. DOI: 10.1136/bjsports-2012-091877. URL: https://bjsm.bmj.com/lookup/doi/10.1136/bjsports-2012-091877 (visited on 08/12/2023).

[Ban21]   Kacper Banach et al. "Brain–computer interface for electric wheelchair based on alpha waves of EEG signal". In: *Bio-Algorithms and Med-Systems* 17.3 (Sept. 29, 2021), pp. 165–172. ISSN: 1896-530X. DOI: 10.1515/bams-2021-0095. URL: https://www.degruyter.com/document/doi/10.1515/bams-2021-0095/html (visited on 08/08/2023).

[Bat17]   Anthony D. Bateson et al. "Categorisation of Mobile EEG: A Researcher's Perspective". In: *BioMed Research International* 2017 (2017), pp. 1–15. ISSN: 2314-6133, 2314-6141. DOI: 10.1155/2017/5496196. URL: https://www.hindawi.com/journals/bmri/2017/5496196/ (visited on 08/09/2023).

[Bel08]   Christian J Bell et al. "Control of a humanoid robot by a noninvasive brain–computer interface in humans". In: *Journal of Neural Engineering* 5.2 (June 15, 2008), pp. 214–220. ISSN: 1741-2560, 1741-2552. DOI: 10.1088/1741-2560/5/2/012. URL: https://iopscience.iop.org/article/10.1088/1741-2560/5/2/012 (visited on 08/08/2023).

[Bel21]   Kais Belwafi, Sofien Gannouni, and Hatim Aboalsamh. "Embedded Brain Computer Interface: State-of-the-Art in Research". In: *Sensors* 21.13 (June 23, 2021), p. 4293. ISSN: 1424-8220. DOI: 10.3390/s21134293. URL: https://www.mdpi.com/1424-8220/21/13/4293 (visited on 08/09/2023).

[Ber91]   P Berg and M Scherg. "Dipole modelling of eye activity and its application to the removal of eye artefacts from the EEG and MEG". In: *Clinical Physics and Physiological Measurement* 12 (A Jan. 1, 1991), pp. 49–54. ISSN: 0143-0815. DOI: 10.1088/0143-0815/12/A/010. URL: https://iopscience.iop.org/article/10.1088/0143-0815/12/A/010 (visited on 08/03/2023).

[Bha14]   Saugat Bhattacharyya, Amit Konar, and D. N. Tibarewala. "Motor imagery, P300 and error-related EEG-based robot arm movement control for rehabilitation purpose". In: *Medical & Biological Engineering & Computing* 52.12 (Dec. 2014), pp. 1007–1017. ISSN: 0140-0118, 1741-0444. DOI: 10.1007/s11517-014-1204-4. URL: http://link.springer.com/10.1007/s11517-014-1204-4 (visited on 07/14/2023).

[Bir81]   N. Birbaumer et al. "EEG and slow cortical potentials in anticipation of mental tasks with different hemispheric involvement". In: *Biological Psychology* 13 (Dec. 1981), pp. 251–260. ISSN: 03010511. DOI: 10.1016/0301-0511(81)90040-5. URL: https://linkinghub.elsevier.com/retrieve/pii/0301051181900405 (visited on 08/04/2023).

[Bir99]   Niels Birbaumer. "slow Cortical Potentials: Plasticity, Operant Control, and Behavioral Effects". In: *The Neuroscientist* 5.2 (Mar. 1999), pp. 74–78. ISSN: 1073-8584, 1089-4098. DOI: 10.1177/107385849900500211. URL: http://journals.sagepub.com/doi/10.1177/107385849900500211 (visited on 08/04/2023).

[Bla06]   Benjamin Blankertz et al. "The Berlin brain-computer interface presents the novel mental typewriter Hex-O-Spell". In: *Clinical Neurophysiology* 113 (Jan. 2006).

[Bla07] Benjamin Blankertz et al. "A Note on Brain Actuated Spelling with the Berlin Brain-Computer Interface". In: *Universal Access in Human-Computer Interaction. Ambient Interaction*. Ed. by Constantine Stephanidis. Red. by David Hutchison et al. Vol. 4555. Series Title: Lecture Notes in Computer Science. Berlin, Heidelberg: Springer Berlin Heidelberg, 2007, pp. 759–768. ISBN: 978-3-540-73280-8. DOI: 10.1007/978-3-540-73281-5_83. URL: http://link.springer.com/10.1007/978-3-540-73281-5_83 (visited on 08/08/2023).

[Bla08] Rossella Blatt et al. "Brain Control of a Smart Wheelchair 1". In: 2008. URL: https://api.semanticscholar.org/CorpusID:42069930.

[Ble16] Martin G Bleichner, Bojana Mirkovic, and Stefan Debener. "Identifying auditory attention with ear-EEG: cEEGrid versus high-density cap-EEG comparison". In: *Journal of Neural Engineering* 13.6 (Dec. 1, 2016), p. 066004. ISSN: 1741-2560, 1741-2552. DOI: 10.1088/1741-2560/13/6/066004. URL: https://iopscience.iop.org/article/10.1088/1741-2560/13/6/066004 (visited on 07/05/2023).

[Blu05] H. Blume, H. T. Feldkaemper, and T. G. Noll. "Model-Based Exploration of the Design Space for Heterogeneous Systems on Chip". In: *Journal of VLSI signal processing systems for signal, image and video technology* 40.1 (May 2005), pp. 19–34. ISSN: 0922-5773. DOI: 10.1007/s11265-005-4936-4. URL: http://link.springer.com/10.1007/s11265-005-4936-4 (visited on 08/21/2023).

[Blu08] Holger Blume. *Exploration des Entwurfsraumes für heterogene Architekturen zur digitalen Videosignalverarbeitung*. Habilitation. RWTH Aachen, Feb. 2008.

[Blu20] Sarah Blum et al. "Flex-printed forehead EEG sensors (fEEGrid) for long-term EEG acquisition". In: *Journal of Neural Engineering* 17.3 (June 1, 2020), p. 034003. ISSN: 1741-2560, 1741-2552. DOI: 10.1088/1741-2552/ab914c. URL: https://iopscience.iop.org/article/10.1088/1741-2552/ab914c (visited on 07/27/2023).

[Boz88] S. Bozinovski, M. Sestakov, and L. Bozinovska. "Using EEG alpha rhythm to control a mobile robot". In: *Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society*. Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society. New Orleans, LA, USA: IEEE, 1988, 1515–1516 vol.3. ISBN: 978-0-7803-0785-8. DOI: 10.1109/IEMBS.1988.95357. URL: http://ieeexplore.ieee.org/document/95357/ (visited on 09/04/2023).

[Bro05] K. Brodmann. *Brodmann's Localisation in the Cerebral Cortex*. Boston, MA: Springer US, 2005. ISBN: 978-0-387-26917-7. DOI: 10.1007/b138298. URL: http://link.springer.com/10.1007/b138298 (visited on 08/15/2023).

[Bul14] Thomas C. Bulea et al. "User-driven control increases cortical activity during treadmill walking: An EEG study". In: *2014 36th Annual International Conference of the IEEE Engineering in Medicine and Biology Society*. 2014 36th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC). Chicago, IL: IEEE, Aug. 2014, pp. 2111–2114. ISBN: 978-1-4244-7929-0. DOI: 10.1109/EMBC.2014.6944033. URL: http://ieeexplore.ieee.org/document/6944033/ (visited on 08/12/2023).

[Byu19]   Wooseok Byun et al. "A 110.3-bits/min 8-Ch SSVEP-based Brain-Computer Interface SoC with 87.9% Accuracy". In: *2019 IEEE Asian Solid-State Circuits Conference (A-SSCC)*. 2019 IEEE Asian Solid-State Circuits Conference (A-SSCC). Macau, Macao: IEEE, Nov. 2019, pp. 201–204. ISBN: 978-1-72815-106-9. DOI: 10.1109/A-SSCC47793.2019.9056983. URL: https://ieeexplore.ieee.org/document/9056983/ (visited on 05/22/2023).

[Cal14]   Calcagno. "INDEPENDENT COMPONENT ANALYSIS AND DISCRETE WAVELET TRANSFORM FOR ARTIFACT REMOVAL IN BIOMEDICAL SIGNAL PROCESSING". In: *American Journal of Applied Sciences* 11.1 (Jan. 1, 2014), pp. 57–68. ISSN: 1546-9239. DOI: 10.3844/ajassp.2014.57.68. URL: http://thescipub.com/abstract/10.3844/ajassp.2014.57.68 (visited on 08/03/2023).

[Cas11]   Thierry Castermans et al. "Optimizing the Performances of a P300-Based Brain–Computer Interface in Ambulatory Conditions". In: *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* 1.4 (Dec. 2011), pp. 566–577. ISSN: 2156-3357, 2156-3365. DOI: 10.1109/JETCAS.2011.2179421. URL: http://ieeexplore.ieee.org/document/6111496/ (visited on 08/12/2023).

[Che19]   Xun Chen et al. "A Novel EEMD-CCA Approach to Removing Muscle Artifacts for Pervasive EEG". In: *IEEE Sensors Journal* 19.19 (Oct. 1, 2019), pp. 8420–8431. ISSN: 1530-437X, 1558-1748, 2379-9153. DOI: 10.1109/JSEN.2018.2872623. URL: https://ieeexplore.ieee.org/document/8476603/ (visited on 08/03/2023).

[Cin08]   Febo Cincotti et al. "Non-invasive brain–computer interface system: Towards its application as assistive technology". In: *Brain Research Bulletin* 75.6 (Apr. 2008), pp. 796–803. ISSN: 03619230. DOI: 10.1016/j.brainresbull.2008.01.007. URL: https://linkinghub.elsevier.com/retrieve/pii/S0361923008000142 (visited on 08/08/2023).

[Con05]   Isabelle Constant, Robert Seeman, and Isabelle Murat. "Sevoflurane and epileptiform EEG changes". In: *Pediatric Anesthesia* 15.4 (Apr. 2005), pp. 266–274. ISSN: 1155-5645, 1460-9592. DOI: 10.1111/j.1460-9592.2004.01538.x. URL: https://onlinelibrary.wiley.com/doi/10.1111/j.1460-9592.2004.01538.x (visited on 08/16/2023).

[Cor07]   A Garcés Correa et al. "Artifact removal from EEG signals using adaptive filters in cascade". In: *Journal of Physics: Conference Series* 90 (Nov. 1, 2007), p. 012081. ISSN: 1742-6596. DOI: 10.1088/1742-6596/90/1/012081. URL: https://iopscience.iop.org/article/10.1088/1742-6596/90/1/012081 (visited on 08/03/2023).

[Da 22]   Carlos F. Da Silva Souto et al. "Pre-gelled Electrode Grid for Self-Applied EEG Sleep Monitoring at Home". In: *Frontiers in Neuroscience* 16 (June 24, 2022), p. 883966. ISSN: 1662-453X. DOI: 10.3389/fnins.2022.883966. URL: https://www.frontiersin.org/articles/10.3389/fnins.2022.883966/full (visited on 07/27/2023).

[Dav07]   Patricia L. Davies and William J. Gavin. "Validating the Diagnosis of Sensory Processing Disorders Using EEG Technology". In: *The American Journal of Occupational Therapy* 61.2 (Mar. 1, 2007), pp. 176–189. ISSN: 0272-9490, 1943-7676. DOI: 10.5014/ajot.61.2.176. URL: https://research.aota.org/ajot/article/61/2/176/5146/Validating-the-Diagnosis-of-Sensory-Processing (visited on 08/12/2023).

[De 14]   Maarten De Vos et al. "P300 speller BCI with a mobile EEG system: comparison to a traditional amplifier". In: *Journal of Neural Engineering* 11.3 (June 1, 2014), p. 036008. ISSN: 1741-2560, 1741-2552. DOI: 10.1088/1741-2560/11/3/036008. URL: https://iopscience.iop.org/article/10.1088/1741-2560/11/3/036008 (visited on 08/12/2023).

[De 16]   Arnaud De Myttenaere et al. "Mean Absolute Percentage Error for regression models". In: *Neurocomputing* 192 (June 2016), pp. 38–48. ISSN: 09252312. DOI: 10.1016/j.neucom.2015.12.114. URL: https://linkinghub.elsevier.com/retrieve/pii/S0925231216003325 (visited on 09/11/2023).

[Deb12]   Stefan Debener et al. "How about taking a low-cost, small, and wireless EEG for a walk?: EEG to go". In: *Psychophysiology* 49.11 (Nov. 2012), pp. 1617–1621. ISSN: 00485772. DOI: 10.1111/j.1469-8986.2012.01471.x. URL: https://onlinelibrary.wiley.com/doi/10.1111/j.1469-8986.2012.01471.x (visited on 08/12/2023).

[Deb15]   Stefan Debener et al. "Unobtrusive ambulatory EEG using a smartphone and flexible printed electrodes around the ear". In: *Scientific Reports* 5.1 (Nov. 17, 2015), p. 16743. ISSN: 2045-2322. DOI: 10.1038/srep16743. URL: https://www.nature.com/articles/srep16743 (visited on 08/12/2023).

[Din06]   Jian Ding, George Sperling, and Ramesh Srinivasan. "Attentional Modulation of SSVEP Power Depends on the Network Tagged by the Flicker Frequency". In: *Cerebral Cortex* 16.7 (July 1, 2006), pp. 1016–1029. ISSN: 1460-2199, 1047-3211. DOI: 10.1093/cercor/bhj044. URL: http://academic.oup.com/cercor/article/16/7/1016/425685/Attentional-Modulation-of-SSVEP-Power-Depends-on (visited on 02/07/2024).

[Dop12]   M. Doppelmayr et al. "Changes in EEG during Ultralong Running". In: *Journal of Human Performance in Extreme Environments* 10.1 (Oct. 18, 2012). ISSN: 2327-2937. DOI: 10.7771/2327-2937.1047. URL: https://docs.lib.purdue.edu/jhpee/vol10/iss1/4 (visited on 08/12/2023).

[Du 21]   N. Du Bois et al. "Neurofeedback with low-cost, wearable electroencephalography (EEG) reduces symptoms in chronic Post-Traumatic Stress Disorder". In: *Journal of Affective Disorders* 295 (Dec. 2021), pp. 1319–1334. ISSN: 01650327. DOI: 10.1016/j.jad.2021.08.071. URL: https://linkinghub.elsevier.com/retrieve/pii/S0165032721008764 (visited on 08/06/2023).

[Dut18]   Prasad Vilas Dutande, Sanjay L. Nalbalwar, and Sanjay V. Khobragade. "FPGA Implementation of Filters for Removing Muscle Artefacts from EEG Signals". In: *2018 Second International Conference on Intelligent Computing and Control Systems (ICICCS)*. 2018 Second International Conference on Intelligent Computing and Control

Systems (ICICCS). Madurai, India: IEEE, June 2018, pp. 728–732. ISBN: 978-1-5386-2842-3. DOI: `10.1109/ICCONS.2018.8662998`. URL: `https://ieeexplore.ieee.org/document/8662998/` (visited on 05/22/2023).

[Duv13] Matthieu Duvinage et al. "Performance of the Emotiv Epoc headset for P300-based applications". In: *BioMedical Engineering OnLine* 12.1 (2013), p. 56. ISSN: 1475-925X. DOI: `10.1186/1475-925X-12-56`. URL: `http://biomedical-engineering-online.biomedcentral.com/articles/10.1186/1475-925X-12-56` (visited on 08/12/2023).

[Ehi14] Benedikt V. Ehinger et al. "Kinesthetic and vestibular information modulate alpha activity during spatial navigation: a mobile EEG study". In: *Frontiers in Human Neuroscience* 8 (2014). ISSN: 1662-5161. DOI: `10.3389/fnhum.2014.00071`. URL: `http://journal.frontiersin.org/article/10.3389/fnhum.2014.00071/abstract` (visited on 08/12/2023).

[Far88] L.A. Farwell and E. Donchin. "Talking off the top of your head: toward a mental prosthesis utilizing event-related brain potentials". In: *Electroencephalography and Clinical Neurophysiology* 70.6 (Dec. 1988), pp. 510–523. ISSN: 00134694. DOI: `10.1016/0013-4694(88)90149-6`. URL: `https://linkinghub.elsevier.com/retrieve/pii/0013469488901496` (visited on 08/08/2023).

[Fen22] Lichen Feng et al. "An Efficient Model-Compressed EEGNet Accelerator for Generalized Brain-Computer Interfaces With Near Sensor Intelligence". In: *IEEE Transactions on Biomedical Circuits and Systems* 16.6 (Dec. 2022), pp. 1239–1249. ISSN: 1932-4545, 1940-9990. DOI: `10.1109/TBCAS.2022.3215962`. URL: `https://ieeexplore.ieee.org/document/9925579/` (visited on 05/22/2023).

[Fit13] Zoë Fitzgerald et al. "Examining factors related to accelerated long-term forgetting in epilepsy using ambulatory EEG monitoring". In: *Epilepsia* 54.5 (May 2013), pp. 819–827. ISSN: 00139580. DOI: `10.1111/epi.12090`. URL: `https://onlinelibrary.wiley.com/doi/10.1111/epi.12090` (visited on 08/12/2023).

[Flo22] Daniel Flood, Neethu Robinson, and Shanker Shreejith. "FPGA-based Deep-Learning Accelerators for Energy Efficient Motor Imagery EEG classification". In: *2022 IEEE International Conference on Omni-layer Intelligent Systems (COINS)*. 2022 IEEE International Conference on Omni-layer Intelligent Systems (COINS). Barcelona, Spain: IEEE, Aug. 1, 2022, pp. 1–6. ISBN: 978-1-66548-356-8. DOI: `10.1109/COINS54846.2022.9854985`. URL: `https://ieeexplore.ieee.org/document/9854985/` (visited on 05/22/2023).

[Fry22] Adam Fry et al. "Evaluating the clinical benefit of brain-computer interfaces for control of a personal computer". In: *Journal of Neural Engineering* 19.2 (Apr. 1, 2022), p. 021001. ISSN: 1741-2560, 1741-2552. DOI: `10.1088/1741-2552/ac60ca`. URL: `https://iopscience.iop.org/article/10.1088/1741-2552/ac60ca` (visited on 09/04/2023).

[Gar08] Gaetano Gargiulo et al. "A mobile EEG system with dry electrodes". In: *2008 IEEE Biomedical Circuits and Systems Conference*. BioCAS 2008. IEEE Biomedical Circuits and Systems Conference - Intelligent Biomedical Systems. Baltimore, MD: IEEE, Nov. 2008, pp. 273–276. ISBN: 978-1-4244-2878-6. DOI: `10.1109/BIOCAS.2008.`

4696927. URL: https://ieeexplore.ieee.org/document/4696927/ (visited on 08/12/2023).

[Gar20] Francisco M. Garcia-Moreno et al. "A CNN-LSTM Deep Learning Classifier for Motor Imagery EEG Detection Using a Low-invasive and Low-Cost BCI Headband". In: *2020 16th International Conference on Intelligent Environments (IE)*. 2020 16th International Conference on Intelligent Environments (IE). Madrid, Spain: IEEE, July 2020, pp. 84–91. ISBN: 978-1-72816-158-7. DOI: 10.1109/IE49459.2020.9155016. URL: https://ieeexplore.ieee.org/document/9155016/ (visited on 08/06/2023).

[Gmba] beyerdynamic GmbH & Co. KG. *DT 1770 PRO*. https://www.beyerdynamic.de/dt-1770-pro.html. Accessed: 2023-08-15.

[Gmbb] beyerdynamic GmbH & Co. KG. *DT 770 PRO*. https://www.beyerdynamic.de/dt-770-pro.html. Accessed: 2023-08-15.

[Gór19] Joanna Górecka and Przemysław Makiewicz. "The Dependence of Electrode Impedance on the Number of Performed EEG Examinations". In: *Sensors* 19.11 (June 8, 2019), p. 2608. ISSN: 1424-8220. DOI: 10.3390/s19112608. URL: https://www.mdpi.com/1424-8220/19/11/2608 (visited on 07/28/2023).

[Gra10] Klaus Gramann et al. "Visual Evoked Responses During Standing and Walking". In: *Frontiers in Human Neuroscience* 4 (2010). ISSN: 1662-5161. DOI: 10.3389/fnhum.2010.00202. URL: http://journal.frontiersin.org/article/10.3389/fnhum.2010.00202/abstract (visited on 08/12/2023).

[Gre11] Jonathan Greene et al. "A 65nm flash-based FPGA fabric optimized for low cost and power". In: *Proceedings of the 19th ACM/SIGDA international symposium on Field programmable gate arrays*. FPGA '11: ACM/SIGDA International Symposium on Field Programmable Gate Arrays. Monterey CA USA: ACM, Feb. 27, 2011, pp. 87–96. ISBN: 978-1-4503-0554-9. DOI: 10.1145/1950413.1950434. URL: https://dl.acm.org/doi/10.1145/1950413.1950434 (visited on 08/18/2023).

[Gwi10] Joseph T. Gwin et al. "Removal of Movement Artifact From High-Density EEG Recorded During Walking and Running". In: *Journal of Neurophysiology* 103.6 (June 2010), pp. 3526–3534. ISSN: 0022-3077, 1522-1598. DOI: 10.1152/jn.00105.2010. URL: https://www.physiology.org/doi/10.1152/jn.00105.2010 (visited on 08/12/2023).

[Hal07] Sebastian Halder et al. "Online Artifact Removal for Brain-Computer Interfaces Using Support Vector Machines and Blind Source Separation". In: *Computational Intelligence and Neuroscience* 2007 (2007), pp. 1–10. ISSN: 1687-5265, 1687-5273. DOI: 10.1155/2007/82069. URL: http://www.hindawi.com/journals/cin/2007/082069/abs/ (visited on 08/03/2023).

[Han05] Simon Hanslmayr et al. "Increasing Individual Upper Alpha Power by Neurofeedback Improves Cognitive Performance in Human Subjects". In: *Applied Psychophysiology and Biofeedback* 30.1 (Mar. 2005), pp. 1–10. ISSN: 1090-0586, 1573-3270. DOI: 10.1007/s10484-005-2169-8. URL: http://link.springer.com/10.1007/s10484-005-2169-8 (visited on 08/09/2023).

[Has19]   Mahamudul Hassan and Sheikh Md. Rabiul Islam. "Design and Implementation of Pre-processing Chip for Brain Computer Interface Machine". In: *2019 International Conference on Robotics,Electrical and Signal Processing Techniques (ICREST)*. 2019 International Conference on Robotics,Electrical and Signal Processing Techniques (ICREST). Dhaka, Bangladesh: IEEE, Jan. 2019, pp. 428–433. ISBN: 978-1-5386-8012-4. DOI: 10.1109/ICREST.2019.8644230. URL: https://ieeexplore.ieee.org/document/8644230/ (visited on 05/22/2023).

[He16]   Lianghua He et al. "Common Bayesian Network for Classification of EEG-Based Multiclass Motor Imagery BCI". In: *IEEE Transactions on Systems, Man, and Cybernetics: Systems* 46.6 (June 2016), pp. 843–854. ISSN: 2168-2216, 2168-2232. DOI: 10.1109/TSMC.2015.2450680. URL: https://ieeexplore.ieee.org/document/7167726/ (visited on 08/06/2023).

[Hee18]   C Heelan, Av Nurmikko, and W Truccolo. "FPGA implementation of deep-learning recurrent neural networks with sub-millisecond real-time latency for BCI-decoding of large-scale neural sensors (104 nodes)". In: *2018 40th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*. 2018 40th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC). Honolulu, HI: IEEE, July 2018, pp. 1070–1073. ISBN: 978-1-5386-3646-6. DOI: 10.1109/EMBC.2018.8512415. URL: https://ieeexplore.ieee.org/document/8512415/ (visited on 05/22/2023).

[Her21]   Ana Caren Hernandez-Ruiz et al. "Motor-Imagery EEGNet-Based Processing on a Low-Spec SoC Hardware". In: *2021 IEEE Sensors*. 2021 IEEE Sensors. Sydney, Australia: IEEE, Oct. 31, 2021, pp. 1–4. ISBN: 978-1-72819-501-8. DOI: 10.1109/SENSORS47087.2021.9639747. URL: https://ieeexplore.ieee.org/document/9639747/ (visited on 05/22/2023).

[Hes21]   Sebastian Hesselbarth, Holger Blume, and Wolfgang Nebel. *Methodik zur FPGA-basierten Analyse und Optimierung der Verlustleistung und des thermischen Verhaltens von eingebetteten Prozessoren*. In collab. with Gottfried Wilhelm Leibniz Universität Hannover. 1. Auflage. Informationstechnik. München: Verlag Dr. Hut, 2021. 177 pp. ISBN: 978-3-8439-4693-3.

[Hin04]   T. Hinterberger et al. "Brain-computer communication and slow cortical potentials". In: *IEEE Transactions on Biomedical Engineering* 51.6 (June 2004), pp. 1011–1018. ISSN: 0018-9294, 1558-2531. DOI: 10.1109/TBME.2004.827067. URL: https://ieeexplore.ieee.org/document/1300796/ (visited on 08/04/2023).

[Hof11]   Klaus-Peter Hoffmann and Ursula Krechel. "Geräte und Methoden der Klinischen Neurophysiologie (EEG, EMG/ENG, EP)". In: *Medizintechnik*. Ed. by Rüdiger Kramme. Berlin, Heidelberg: Springer Berlin Heidelberg, 2011, pp. 155–192. ISBN: 978-3-642-16187-2. DOI: 10.1007/978-3-642-16187-2_12. URL: http://link.springer.com/10.1007/978-3-642-16187-2_12 (visited on 07/21/2023).

[Hol22]   Björn Holtze et al. "Ear-EEG Measures of Auditory Attention to Continuous Speech". In: *Frontiers in Neuroscience* 16 (May 3, 2022), p. 869426. ISSN: 1662-453X. DOI: 10.3389/fnins.2022.869426. URL: https://www.frontiersin.org/articles/10.3389/fnins.2022.869426/full (visited on 07/27/2023).

[HPC19]   HPCwire. *Xilinx Says Its New FPGA is World's Largest*. `https://www.hpcwire.com/2019/08/21/xilinx-says-its-new-fpga-is-worlds-largest/`. Accessed: 2023-08-22. Aug. 21, 2019.

[Hua23]   Gan Huang et al. "Discrepancy between inter- and intra-subject variability in EEG-based motor imagery brain-computer interface: Evidence from multiple perspectives". In: *Frontiers in Neuroscience* 17 (Feb. 13, 2023), p. 1122661. ISSN: 1662-453X. DOI: `10.3389/fnins.2023.1122661`. URL: `https://www.frontiersin.org/articles/10.3389/fnins.2023.1122661/full` (visited on 08/15/2023).

[Jac10]   Melody Jackson. "Direct Brain Interfaces for Healing Games". In: (Jan. 2010).

[Jer89]   B. W. Jervis, M. Coelho, and G. W. Morgan. "Effect on EEG responses of removing ocular artefacts by proportional EOG subtraction". In: *Medical & Biological Engineering & Computing* 27.5 (Sept. 1989), pp. 484–490. ISSN: 0140-0118, 1741-0444. DOI: `10.1007/BF02441466`. URL: `http://link.springer.com/10.1007/BF02441466` (visited on 08/03/2023).

[Jia12]   Lijun Jiang et al. "iPhone-based portable brain control wheelchair". In: *2012 7th IEEE Conference on Industrial Electronics and Applications (ICIEA)*. 2012 7th IEEE Conference on Industrial Electronics and Applications (ICIEA). Singapore, Singapore: IEEE, July 2012, pp. 1592–1594. ISBN: 978-1-4577-2119-9. DOI: `10.1109/ICIEA.2012.6360978`. URL: `http://ieeexplore.ieee.org/document/6360978/` (visited on 08/14/2023).

[Jia19]   Xiao Jiang, Gui-Bin Bian, and Zean Tian. "Removal of Artifacts from EEG Signals: A Review". In: *Sensors* 19.5 (Feb. 26, 2019), p. 987. ISSN: 1424-8220. DOI: `10.3390/s19050987`. URL: `http://www.mdpi.com/1424-8220/19/5/987` (visited on 08/01/2023).

[Jun16]   Evelyn Jungnickel and Klaus Gramann. "Mobile Brain/Body Imaging (MoBI) of Physical Interaction with Dynamically Moving Objects". In: *Frontiers in Human Neuroscience* 10 (June 27, 2016). ISSN: 1662-5161. DOI: `10.3389/fnhum.2016.00306`. URL: `http://journal.frontiersin.org/Article/10.3389/fnhum.2016.00306/abstract` (visited on 08/12/2023).

[Kai14]   Belwafi Kais et al. "An embedded implementation of home devices control system based on brain computer interface". In: *2014 26th International Conference on Microelectronics (ICM)*. 2014 26th International Conference on Microelectronics (ICM). Doha, Qatar: IEEE, Dec. 2014, pp. 140–143. ISBN: 978-1-4799-8153-3. DOI: `10.1109/ICM.2014.7071826`. URL: `http://ieeexplore.ieee.org/document/7071826/` (visited on 05/21/2023).

[Kap17]   Simon L. Kappel and Preben Kidmose. "High-density ear-EEG". In: *2017 39th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*. 2017 39th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC). Seogwipo: IEEE, July 2017, pp. 2394–2397. ISBN: 978-1-5090-2809-2. DOI: `10.1109/EMBC.2017.8037338`. URL: `https://ieeexplore.ieee.org/document/8037338/` (visited on 07/27/2023).

[Kar17] V. Kartsch et al. "A wearable EEG-based drowsiness detection system with blink duration and alpha waves analysis". In: *2017 8th International IEEE/EMBS Conference on Neural Engineering (NER)*. 2017 8th International IEEE/EMBS Conference on Neural Engineering (NER). Shanghai, China: IEEE, May 2017, pp. 251–254. ISBN: 978-1-5090-4603-4. DOI: 10.1109/NER.2017.8008338. URL: http://ieeexplore.ieee.org/document/8008338/ (visited on 08/14/2023).

[Kar20] Reza Karkon, Seyed Mohammad Reza Shahshahani, and Hamid Reza Mahdiani. "A Custom Hardware CCA Engine for Real-time SSVEP-based BCI Applications". In: *2020 20th International Symposium on Computer Architecture and Digital Systems (CADS)*. 2020 20th International Symposium on Computer Architecture and Digital Systems (CADS). Rasht, Iran: IEEE, Aug. 2020, pp. 1–6. ISBN: 978-1-72818-111-0. DOI: 10.1109/CADS50570.2020.9211863. URL: https://ieeexplore.ieee.org/document/9211863/ (visited on 05/22/2023).

[Kar22] Nedime Karakullukcu and Bülent Yilmaz. "Detection of Movement Intention in EEG-Based Brain-Computer Interfaces Using Fourier-Based Synchrosqueezing Transform". In: *International Journal of Neural Systems* 32.1 (Jan. 2022), p. 2150059. ISSN: 0129-0657, 1793-6462. DOI: 10.1142/S0129065721500593. URL: https://www.worldscientific.com/doi/abs/10.1142/S0129065721500593 (visited on 08/06/2023).

[Kaw21] Aleksandra Kawala-Sterniuk et al. "Summary of over Fifty Years with Brain-Computer Interfaces—A Review". In: *Brain Sciences* 11.1 (Jan. 3, 2021), p. 43. ISSN: 2076-3425. DOI: 10.3390/brainsci11010043. URL: https://www.mdpi.com/2076-3425/11/1/43 (visited on 09/04/2023).

[Kev14] Jasmin Kevric and Abdulhamit Subasi. "The Effect of Multiscale PCA De-noising in Epileptic Seizure Detection". In: *Journal of Medical Systems* 38.10 (Oct. 2014), p. 131. ISSN: 0148-5598, 1573-689X. DOI: 10.1007/s10916-014-0131-0. URL: http://link.springer.com/10.1007/s10916-014-0131-0 (visited on 08/03/2023).

[Kev15] Jasmin Kevric and Abdulhamit Subasi. "The Impact of Mspca Signal De-Noising In Real-Time Wireless Brain Computer Interface System". In: *Southeast Europe Journal of Soft Computing* 4.1 (Oct. 1, 2015). ISSN: 2233-1859. DOI: 10.21533/scjournal.v4i1.90. URL: http://scjournal.ius.edu.ba/index.php/scjournal/article/view/90 (visited on 08/03/2023).

[Khu12] Kanav Khurana et al. "Development of an FPGA-based real-time P300 speller". In: *22nd International Conference on Field Programmable Logic and Applications (FPL)*. 2012 22nd International Conference on Field Programmable Logic and Applications (FPL). Oslo, Norway: IEEE, Aug. 2012, pp. 551–554. ISBN: 978-1-4673-2255-3. DOI: 10.1109/FPL.2012.6339377. URL: http://ieeexplore.ieee.org/document/6339377/ (visited on 05/22/2023).

[Kle99] George H. Klem et al. "The ten-twenty electrode system of the International Federation. The International Federation of Clinical Neurophysiology." In: *Electroencephalography and clinical neurophysiology. Supplement* 52 (1999), pp. 3–6.

[Klo13] Juris Klonovs et al. "ID Proof on the Go: Development of a Mobile EEG-Based Biometric Authentication System". In: *IEEE Vehicular Technology Magazine* 8.1 (Mar. 2013), pp. 81–89. ISSN: 1556-6072. DOI: 10.1109/MVT.2012.2234056. URL: http://ieeexplore.ieee.org/document/6449282/ (visited on 08/12/2023).

[Kot20] Shailaja Kotte and J R K Kumar Dabbakuti. "Methods for removal of artifacts from EEG signal: A review". In: *Journal of Physics: Conference Series* 1706.1 (Dec. 1, 2020), p. 012093. ISSN: 1742-6588, 1742-6596. DOI: 10.1088/1742-6596/1706/1/012093. URL: https://iopscience.iop.org/article/10.1088/1742-6596/1706/1/012093 (visited on 08/03/2023).

[Kra17] Rüdiger Kramme, ed. *Medizintechnik: Verfahren - Systeme - Informationsverarbeitung.* 5., vollständig überarbeitete und erweiterte Auflage. Springer Reference Technik. Berlin [Heidelberg]: Springer, 2017. 1074 pp. ISBN: 978-3-662-48771-6. DOI: 10.1007/978-3-662-48771-6.

[Kre07] Roman Krepki et al. "The Berlin Brain-Computer Interface (BBCI) – towards a new communication channel for online control in gaming applications". In: *Multimedia Tools and Applications* 33.1 (Mar. 13, 2007), pp. 73–90. ISSN: 1380-7501, 1573-7721. DOI: 10.1007/s11042-006-0094-3. URL: http://link.springer.com/10.1007/s11042-006-0094-3 (visited on 08/09/2023).

[Kru16] Max O. Krucoff et al. "Enhancing Nervous System Recovery through Neurobiologics, Neural Interface Training, and Neurorehabilitation". In: *Frontiers in Neuroscience* 10 (Dec. 27, 2016). ISSN: 1662-453X. DOI: 10.3389/fnins.2016.00584. URL: http://journal.frontiersin.org/article/10.3389/fnins.2016.00584/full (visited on 09/04/2023).

[Küb01] Andrea Kübler et al. "Brain–computer communication: Unlocking the locked in." In: *Psychological Bulletin* 127.3 (2001), pp. 358–375. ISSN: 1939-1455, 0033-2909. DOI: 10.1037/0033-2909.127.3.358. URL: http://doi.apa.org/getdoi.cfm?doi=10.1037/0033-2909.127.3.358 (visited on 08/08/2023).

[Kub05] A. Kubler et al. "Patients with ALS can use sensorimotor rhythms to operate a brain-computer interface". In: *Neurology* 64.10 (May 24, 2005), pp. 1775–1777. ISSN: 0028-3878, 1526-632X. DOI: 10.1212/01.WNL.0000158616.43002.6D. URL: https://www.neurology.org/lookup/doi/10.1212/01.WNL.0000158616.43002.6D (visited on 08/05/2023).

[Lau16] Steven Laureys, Olivia Gosseries, and Giulio Tononi, eds. *The neurology of consciousness: cognitive neuroscience and neuropathology.* Second edition. Amsterdam ; Boston: Elsevier/AP, Academic Press is an imprint of Elsevier, 2016. 471 pp. ISBN: 978-0-12-800948-2.

[Leb06] Mikhail A. Lebedev and Miguel A.L. Nicolelis. "Brain–machine interfaces: past, present and future". In: *Trends in Neurosciences* 29.9 (Sept. 2006), pp. 536–546. ISSN: 01662236. DOI: 10.1016/j.tins.2006.07.004. URL: https://linkinghub.elsevier.com/retrieve/pii/S0166223606001470 (visited on 09/04/2023).

[Lee22]   Hyemin S. Lee et al. "Individual finger movement decoding using a novel ultra-high-density electroencephalography-based brain-computer interface system". In: *Frontiers in Neuroscience* 16 (Oct. 19, 2022), p. 1009878. ISSN: 1662-453X. DOI: 10.3389/fnins.2022.1009878. URL: https://www.frontiersin.org/articles/10.3389/fnins.2022.1009878/full (visited on 07/27/2023).

[Li23]   Yuning Li. *HLS-Based Implementation in Digital Signal Processing Algorithms for Real-Time EEG Data Analysis*. Master's Thesis. Yuning Li, Institute of Microelectronic System, Leibniz University Hanover. 2023.

[Lib18]   Erwan Libessart et al. "40 Gop/s/mm ^{2} fixed-point operators for Brain Computer Interface in 65 nm CMOS". In: *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2018 IEEE International Symposium on Circuits and Systems (ISCAS). Florence: IEEE, May 2018, pp. 1–4. ISBN: 978-1-5386-4881-0. DOI: 10.1109/ISCAS.2018.8351028. URL: https://ieeexplore.ieee.org/document/8351028/ (visited on 05/22/2023).

[Lin05]   Jing Lin and Aimin Zhang. "Fault feature separation using wavelet-ICA filter". In: *NDT & E International* 38.6 (Sept. 2005), pp. 421–427. ISSN: 09638695. DOI: 10.1016/j.ndteint.2004.11.005. URL: https://linkinghub.elsevier.com/retrieve/pii/S0963869504001525 (visited on 08/03/2023).

[Lin10]   Chin-Teng Lin et al. "A Real-Time Wireless Brain–Computer Interface System for Drowsiness Detection". In: *IEEE Transactions on Biomedical Circuits and Systems* 4.4 (Aug. 2010), pp. 214–222. ISSN: 1932-4545, 1940-9990. DOI: 10.1109/TBCAS.2010.2046415. URL: http://ieeexplore.ieee.org/document/5456232/ (visited on 08/09/2023).

[Lin14a]   Jzau-Sheng Lin and Cheng-Hung Hsieh. "A BCI Control System for TV Channels-Selection". In: *International Journal on Communications (IJC* 3 (2014), pp. 71–75.

[Lin14b]   Yuan-Pin Lin et al. "Assessing the quality of steady-state visual-evoked potentials for moving humans using a mobile electroencephalogram headset". In: *Frontiers in Human Neuroscience* 8 (Mar. 31, 2014). ISSN: 1662-5161. DOI: 10.3389/fnhum.2014.00182. URL: http://journal.frontiersin.org/article/10.3389/fnhum.2014.00182/abstract (visited on 08/12/2023).

[Lin16]   Jzau-Sheng Lin and Cheng-Hung Hsieh. "A Wireless BCI-Controlled Integration System in Smart Living Space for Patients". In: *Wireless Personal Communications* 88.2 (May 2016), pp. 395–412. ISSN: 0929-6212, 1572-834X. DOI: 10.1007/s11277-015-3129-0. URL: http://link.springer.com/10.1007/s11277-015-3129-0 (visited on 08/14/2023).

[Lin21]   Bor-Shing Lin et al. "Design of SSVEP Enhancement-Based Brain Computer Interface". In: *IEEE Sensors Journal* 21.13 (July 1, 2021), pp. 14330–14338. ISSN: 1530-437X, 1558-1748, 2379-9153. DOI: 10.1109/JSEN.2020.3033470. URL: https://ieeexplore.ieee.org/document/9239968/ (visited on 05/22/2023).

[Liu13]   Ning-Han Liu, Cheng-Yu Chiang, and Hsiang-Ming Hsu. "Improving Driver Alertness through Music Selection Using a Mobile EEG to Detect Brainwaves". In: *Sensors* 13.7 (June 26, 2013), pp. 8199–8221. ISSN: 1424-8220. DOI: 10.3390/s130708199. URL: http://www.mdpi.com/1424-8220/13/7/8199 (visited on 08/12/2023).

[Liu21]   Ziming Liu et al. "A systematic review on hybrid EEG/fNIRS in brain-computer inter-face". In: *Biomedical Signal Processing and Control* 68 (July 2021), p. 102595. ISSN: 17468094. DOI: 10.1016/j.bspc.2021.102595. URL: https://linkinghub.elsevier.com/retrieve/pii/S1746809421001920 (visited on 08/15/2023).

[Lot07]   F Lotte et al. "A review of classification algorithms for EEG-based brain–computer interfaces". In: *Journal of Neural Engineering* 4.2 (June 1, 2007), R1–R13. ISSN: 1741-2560, 1741-2552. DOI: 10.1088/1741-2560/4/2/R01. URL: https://iopscience.iop.org/article/10.1088/1741-2560/4/2/R01 (visited on 08/01/2023).

[Lot09]   Fabien Lotte et al. "Towards ambulatory brain-computer interfaces: a pilot study with P300 signals". In: *Proceedings of the International Conference on Advances in Computer Entertainment Technology*. ACE '09: International Conference in Advances in Computer Entertainment Technology. Athens Greece: ACM, Oct. 29, 2009, pp. 336–339. ISBN: 978-1-60558-864-3. DOI: 10.1145/1690388.1690452. URL: https://dl.acm.org/doi/10.1145/1690388.1690452 (visited on 08/12/2023).

[Ma19]   Xunguang Ma et al. "FPGA-Based Rapid Electroencephalography Signal Classification System". In: *2019 IEEE 11th International Conference on Advanced Infocomm Technology (ICAIT)*. 2019 IEEE 11th International Conference on Advanced Infocomm Technology (ICAIT). Jinan, China: IEEE, Oct. 2019, pp. 223–227. ISBN: 978-1-72814-778-9. DOI: 10.1109/ICAIT.2019.8935935. URL: https://ieeexplore.ieee.org/document/8935935/ (visited on 05/22/2023).

[Mah21]   Musa Mahmood et al. "Wireless Soft Scalp Electronics and Virtual Reality System for Motor Imagery-Based Brain–Machine Interfaces". In: *Advanced Science* 8.19 (Oct. 2021), p. 2101129. ISSN: 2198-3844, 2198-3844. DOI: 10.1002/advs.202101129. URL: https://onlinelibrary.wiley.com/doi/10.1002/advs.202101129 (visited on 08/06/2023).

[Mai14]   Clemens Maidhof, Torsten Kästner, and Tommi Makkonen. "Combining EEG, MIDI, and motion capture techniques for investigating musical performance". In: *Behavior Research Methods* 46.1 (Mar. 2014), pp. 185–195. ISSN: 1554-3528. DOI: 10.3758/s13428-013-0363-9. URL: https://link.springer.com/10.3758/s13428-013-0363-9 (visited on 08/12/2023).

[Mak09]   J.N. Mak and J.R. Wolpaw. "Clinical Applications of Brain-Computer Interfaces: Current State and Future Prospects". In: *IEEE Reviews in Biomedical Engineering* 2 (2009), pp. 187–199. ISSN: 1937-3333, 1941-1189. DOI: 10.1109/RBME.2009.2035356. URL: http://ieeexplore.ieee.org/document/5342720/ (visited on 08/04/2023).

[Mal18]   Alireza Malekmohammadi et al. "An Efficient Hardware Implementation for a Motor Imagery Brain Computer Interface System". In: *Scientia Iranica* 0.0 (Aug. 12, 2018), pp. 72–94. ISSN: 2345-3605. DOI: 10.24200/sci.2018.4978.1022. URL: http://scientiairanica.sharif.edu/article_20830.html (visited on 05/21/2023).

[Man20]   Mohammad Amir Mansoori and Mario R. Casu. "High Level Design of a Flexible PCA Hardware Accelerator Using a New Block-Streaming Method". In: *Electronics* 9.3 (Mar. 7, 2020), p. 449. ISSN: 2079-9292. DOI: 10.3390/electronics9030449. URL: https://www.mdpi.com/2079-9292/9/3/449 (visited on 08/28/2023).

[Mao19] Haoran Mao. *Analysis, Implementation and Evaluation of Communication Interfaces for Mobile Brain-Computer Interfaces with Real-Time Constraints*. Master's Thesis. Institute of Microelectronic System, Leibniz University Hanover. 2019.

[Mat17] Petjon Mata. *Implementierung und Evaluation einer mobilen intelligenten EEG-Sensorplattform für Brain-Computer Interfaces*. Master's Thesis. Petjon Mata, Institute of Microelectronic System, Leibniz University Hanover. 2017.

[May16] Mayo Clinic College of Medicine, Rochester, Minnesota et al. *Electroencephalography (EEG): An Introductory Text and Atlas of Normal and Abnormal Findings in Adults, Children, and Infants*. American Epilepsy Society, 2016. ISBN: 978-0-9979756-0-4. DOI: 10.5698/978-0-9979756-0-4. URL: https://www.ncbi.nlm.nih.gov/books/NBK390354/ (visited on 07/25/2023).

[McC17] Colin M. McCrimmon et al. "Performance Assessment of a Custom, Portable, and Low-Cost Brain–Computer Interface Platform". In: *IEEE Transactions on Biomedical Engineering* 64.10 (Oct. 2017), pp. 2313–2320. ISSN: 0018-9294, 1558-2531. DOI: 10.1109/TBME.2017.2667579. URL: http://ieeexplore.ieee.org/document/7851005/ (visited on 08/14/2023).

[McF00] Dennis J. McFarland et al. "Mu and Beta Rhythm Topographies During Motor Imagery and Actual Movements". In: *Brain Topography* 12.3 (Mar. 1, 2000), pp. 177–186. ISSN: 1573-6792. DOI: 10.1023/A:1023437823106. URL: https://doi.org/10.1023/A:1023437823106.

[Mic17] Microchip. *DS0115: SmartFusion2 Pin Descriptions*. Datasheet. Accessed: 2023-08-21. 2017. URL: https://www.microsemi.com/document-portal/doc_view/130718-ds0115-smartfusion2-pin-descriptions-datasheet.

[Mic19] Microchip. *UG0445: SmartFusion2 SoC FPGA and IGLOO2 FPGA Fabric*. User Guide. Accessed: 2023-08-21. 2019. URL: https://www.microsemi.com/document-portal/doc_view/132008-ug0445-smartfusion2-soc-fpga-and-igloo2-fpga-fabric-user-guide.

[Mic21] Microchip. *Benefits of Smart High-Level Synthesis for FPGA Design*. DS50003181A. 2021. URL: https://coredocs.s3.amazonaws.com/smarthls/2021.2/SmartHLS_Benefits_Whitepaper.pdf (visited on 08/28/2023).

[Mid00] M. Middendorf et al. "Brain-computer interfaces based on the steady-state visual-evoked response". In: *IEEE Transactions on Rehabilitation Engineering* 8.2 (June 2000), pp. 211–214. ISSN: 10636528. DOI: 10.1109/86.847819. URL: http://ieeexplore.ieee.org/document/847819/ (visited on 08/04/2023).

[Mil20] Kai J. Miller, Dora Hermes, and Nathan P. Staff. "The current state of electrocorticography-based brain–computer interfaces". In: *Neurosurgical Focus* 49.1 (July 2020), E2. ISSN: 1092-0684. DOI: 10.3171/2020.4.FOCUS20185. URL: https://thejns.org/view/journals/neurosurg-focus/49/1/article-pE2.xml (visited on 09/11/2023).

[Min02] Ming Cheng et al. "Design and implementation of a brain-computer interface with high transfer rates". In: *IEEE Transactions on Biomedical Engineering* 49.10 (Oct. 2002), pp. 1181–1186. ISSN: 0018-9294. DOI: 10.1109/TBME.2002.803536. URL: http://ieeexplore.ieee.org/document/1035968/ (visited on 08/08/2023).

[Mir05]   Eduardo Miranda et al. "Plymouth brain-computer music interface project: Intelligent assistive technology for music-making". In: (Jan. 2005).

[Mul08]   G.R. Muller-Putz and G. Pfurtscheller. "Control of an Electrical Prosthesis With an SSVEP-Based BCI". In: *IEEE Transactions on Biomedical Engineering* 55.1 (Jan. 2008), pp. 361–364. ISSN: 0018-9294, 1558-2531. DOI: 10.1109/TBME.2007.897815. URL: http://ieeexplore.ieee.org/document/4360033/ (visited on 08/08/2023).

[Mwa21]   Tat'y Mwata-Velu et al. "Motor Imagery Classification Based on a Recurrent-Convolutional Architecture to Control a Hexapod Robot". In: *Mathematics* 9.6 (Mar. 12, 2021), p. 606. ISSN: 2227-7390. DOI: 10.3390/math9060606. URL: https://www.mdpi.com/2227-7390/9/6/606 (visited on 08/06/2023).

[Nic12]   Luis Fernando Nicolas-Alonso and Jaime Gomez-Gil. "Brain Computer Interfaces, a Review". In: *Sensors* 12.2 (Jan. 31, 2012), pp. 1211–1279. ISSN: 1424-8220. DOI: 10.3390/s120201211. URL: http://www.mdpi.com/1424-8220/12/2/1211 (visited on 08/08/2023).

[Nuw98]   Marc R. Nuwer et al. "IFCN standards for digital recording of clinical EEG". In: *Electroencephalography and Clinical Neurophysiology* 106.3 (Mar. 1998), pp. 259–261. ISSN: 00134694. DOI: 10.1016/S0013-4694(97)00106-5. URL: https://linkinghub.elsevier.com/retrieve/pii/S0013469497001065 (visited on 07/24/2023).

[Oos01]   Robert Oostenveld and Peter Praamstra. "The five percent electrode system for high-resolution EEG and ERP measurements". In: *Clinical Neurophysiology* 112.4 (Apr. 2001), pp. 713–719. ISSN: 13882457. DOI: 10.1016/S1388-2457(00)00527-7. URL: https://linkinghub.elsevier.com/retrieve/pii/S1388245700005277 (visited on 07/24/2023).

[Opp72]   A.V. Oppenheim and C.J. Weinstein. "Effects of finite register length in digital filtering and the fast Fourier transform". In: *Proceedings of the IEEE* 60.8 (1972), pp. 957–976. ISSN: 0018-9219. DOI: 10.1109/PROC.1972.8820. URL: http://ieeexplore.ieee.org/document/1450750/ (visited on 09/11/2023).

[OUc22]   Shin-Ichi O'Uchi and Ryusuke Hayashi. "Short Floating-Point CNN Accelerator for Brain-Computer Interface to Decode Visual Information". In: *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2022 IEEE International Symposium on Circuits and Systems (ISCAS). Austin, TX, USA: IEEE, May 28, 2022, pp. 2299–2303. ISBN: 978-1-66548-485-5. DOI: 10.1109/ISCAS48785.2022.9937282. URL: https://ieeexplore.ieee.org/document/9937282/ (visited on 05/22/2023).

[Pan17]   Aiken Pang and Peter Membrey. *Beginning FPGA: Programming Metal*. Berkeley, CA: Apress, 2017. ISBN: 978-1-4302-6248-0. DOI: 10.1007/978-1-4302-6248-0. URL: http://link.springer.com/10.1007/978-1-4302-6248-0 (visited on 08/22/2023).

[Per00]   J. Perelmouter and N. Birbaumer. "A binary spelling interface with random errors". In: *IEEE Transactions on Rehabilitation Engineering* 8.2 (June 2000), pp. 227–232. ISSN: 10636528. DOI: 10.1109/86.847824. URL: http://ieeexplore.ieee.org/document/847824/ (visited on 08/08/2023).

[Pfu00] G Pfurtscheller et al. "Brain oscillations control hand orthosis in a tetraplegic". In: *Neuroscience Letters* 292.3 (Oct. 2000), pp. 211–214. ISSN: 03043940. DOI: 10.1016/S0304-3940(00)01471-3. URL: `https://linkinghub.elsevier.com/retrieve/pii/S0304394000014713` (visited on 08/08/2023).

[Pic92] Terence W. Picton. "The P300 Wave of the Human Event-Related Potential:" in: *Journal of Clinical Neurophysiology* 9.4 (Oct. 1992), pp. 456–479. ISSN: 0736-0258. DOI: 10.1097/00004691-199210000-00002. URL: `http://journals.lww.com/00004691-199210000-00002` (visited on 08/04/2023).

[Pla08] Danny Plass-Oude Bos and Boris Reuderink. "BrainBasher: a BCI game". In: *Journal of Vacuum Science & Technology A - J VAC SCI TECHNOL A* 2008 (Jan. 2008).

[Put20] Felix Putze et al. "Editorial: Brain-Computer Interfaces and Augmented/Virtual Reality". In: *Frontiers in Human Neuroscience* 14 (May 12, 2020), p. 144. ISSN: 1662-5161. DOI: 10.3389/fnhum.2020.00144. URL: `https://www.frontiersin.org/article/10.3389/fnhum.2020.00144/full` (visited on 08/09/2023).

[Rak05] A. Rakotomamonjy et al. "Ensemble of SVMs for Improving Brain Computer Interface P300 Speller Performances". In: *Artificial Neural Networks: Biological Inspirations – ICANN 2005*. Ed. by Włodzisław Duch et al. Red. by David Hutchison et al. Vol. 3696. Series Title: Lecture Notes in Computer Science. Berlin, Heidelberg: Springer Berlin Heidelberg, 2005, pp. 45–50. ISBN: 978-3-540-28754-4. DOI: 10.1007/11550822_8. URL: `http://link.springer.com/10.1007/11550822_8` (visited on 08/01/2023).

[Ram19] Juan Ramírez-Quintana et al. "Novel SSVEP Processing Method Based on Correlation and Feedforward Neural Network for Embedded Brain Computer Interface". In: *Pattern Recognition*. Ed. by Jesús Ariel Carrasco-Ochoa et al. Vol. 11524. Series Title: Lecture Notes in Computer Science. Cham: Springer International Publishing, 2019, pp. 248–258. ISBN: 978-3-030-21076-2. DOI: 10.1007/978-3-030-21077-9_23. URL: `https://link.springer.com/10.1007/978-3-030-21077-9_23` (visited on 08/14/2023).

[Rao14] K. Hanumantha Rao and C. Kumar Charlie Paul. "Performance analysis of different radix2 structure". In: *Second International Conference on Current Trends In Engineering and Technology - ICCTET 2014*. 2014 2nd International Conference on Current Trends in Engineering and Technology (ICCTET). Coimbatore, India: IEEE, July 2014, pp. 405–408. ISBN: 978-1-4799-7987-5. DOI: 10.1109/ICCTET.2014.6966326. URL: `https://ieeexplore.ieee.org/document/6966326` (visited on 09/11/2023).

[Rap08] Evan D. Rapoport et al. "Engaging, Non-Invasive Brain-Computer Interfaces (BCIs) for Improving Training Effectiveness & Enabling Creative Expression". In: *Proceedings of the Human Factors and Ergonomics Society Annual Meeting* 52.7 (Sept. 2008), pp. 591–594. ISSN: 2169-5067, 1071-1813. DOI: 10.1177/154193120805200702. URL: `http://journals.sagepub.com/doi/10.1177/154193120805200702` (visited on 08/09/2023).

[Ras18]   Usman Rashid et al. "An EEG Experimental Study Evaluating the Performance of Texas Instruments ADS1299". In: *Sensors* 18.11 (Nov. 1, 2018), p. 3721. ISSN: 1424-8220. DOI: 10.3390/s18113721. URL: http://www.mdpi.com/1424-8220/18/11/3721 (visited on 06/19/2023).

[Rob15]   C. V. Robertson and F. E. Marino. "Prefrontal and motor cortex EEG responses and their relationship to ventilatory thresholds during exhaustive incremental exercise". In: *European Journal of Applied Physiology* 115.9 (Sept. 2015), pp. 1939–1948. ISSN: 1439-6319, 1439-6327. DOI: 10.1007/s00421-015-3177-x. URL: http://link.springer.com/10.1007/s00421-015-3177-x (visited on 08/12/2023).

[Saf12]   Doha Safieddine et al. "Removal of muscle artifact from EEG data: comparison between stochastic (ICA and CCA) and deterministic (EMD and wavelet-based) approaches". In: *EURASIP Journal on Advances in Signal Processing* 2012.1 (Dec. 2012), p. 127. ISSN: 1687-6180. DOI: 10.1186/1687-6180-2012-127. URL: https://asp-eurasipjournals.springeropen.com/articles/10.1186/1687-6180-2012-127 (visited on 08/03/2023).

[Sai22]   Manali Saini, Deepak Kumar, and Udit Satija. "Edge of Medical Things Implementation for Deep Learning-Based Cognitive Task Recognition". In: *IEEE Internet of Things Magazine* 5.3 (Sept. 2022), pp. 56–60. ISSN: 2576-3180, 2576-3199. DOI: 10.1109/IOTM.001.2200038. URL: https://ieeexplore.ieee.org/document/9945855/ (visited on 05/22/2023).

[Sai23]   Aurora Saibene et al. "EEG-Based BCIs on Motor Imagery Paradigm Using Wearable Technologies: A Systematic Review". In: *Sensors* 23.5 (Mar. 3, 2023), p. 2798. ISSN: 1424-8220. DOI: 10.3390/s23052798. URL: https://www.mdpi.com/1424-8220/23/5/2798 (visited on 05/22/2023).

[Sch92]   Frank Schneider et al. "Self-regulation of slow cortical potentials in psychiatric patients: Depression". In: *Biofeedback and Self-Regulation* 17.3 (Sept. 1992), pp. 203–214. ISSN: 0363-3586, 1573-3270. DOI: 10.1007/BF01000403. URL: http://link.springer.com/10.1007/BF01000403 (visited on 08/09/2023).

[Sch93]   Frank Schneider et al. "Self-regulation of slow cortical potentials in psychiatric patients: Alcohol dependency". In: *Biofeedback and Self-Regulation* 18.1 (Mar. 1993), pp. 23–32. ISSN: 0363-3586, 1573-3270. DOI: 10.1007/BF00999511. URL: http://link.springer.com/10.1007/BF00999511 (visited on 08/09/2023).

[Shi12]   Jerry J. Shih, Dean J. Krusienski, and Jonathan R. Wolpaw. "Brain-Computer Interfaces in Medicine". In: *Mayo Clinic Proceedings* 87.3 (Mar. 2012), pp. 268–279. ISSN: 00256196. DOI: 10.1016/j.mayocp.2011.12.008. URL: https://linkinghub.elsevier.com/retrieve/pii/S0025619612001231 (visited on 09/04/2023).

[Sho05]   L. Shoker, S. Sanei, and J. Chambers. "Artifact removal from electroencephalograms using a hybrid BSS-SVM algorithm". In: *IEEE Signal Processing Letters* 12.10 (Oct. 2005), pp. 721–724. ISSN: 1070-9908. DOI: 10.1109/LSP.2005.855539. URL: http://ieeexplore.ieee.org/document/1510668/ (visited on 08/03/2023).

[Shr18]   Ritu Ranjan Shrivastwa, Vikramkumar Pudi, and Anupam Chattopadhyay. "An FPGA-Based Brain Computer Interfacing Using Compressive Sensing and Machine Learning". In: *2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. 2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI). Hong Kong: IEEE, July 2018, pp. 726–731. ISBN: 978-1-5386-7099-6. DOI: 10.1109/ISVLSI.2018.00137. URL: https://ieeexplore.ieee.org/document/8429458/ (visited on 05/22/2023).

[Shy10]   Kuo-Kai Shyu et al. "Development of a Low-Cost FPGA-Based SSVEP BCI Multimedia Control System". In: *IEEE Transactions on Biomedical Circuits and Systems* 4.2 (Apr. 2010), pp. 125–132. ISSN: 1932-4545, 1940-9990. DOI: 10.1109/TBCAS.2010.2042595. URL: http://ieeexplore.ieee.org/document/5437509/ (visited on 05/22/2023).

[Shy13]   Kuo-Kai Shyu et al. "Total Design of an FPGA-Based Brain–Computer Interface Control Hospital Bed Nursing System". In: *IEEE Transactions on Industrial Electronics* 60.7 (July 2013), pp. 2731–2739. ISSN: 0278-0046, 1557-9948. DOI: 10.1109/TIE.2012.2196897. URL: http://ieeexplore.ieee.org/document/6193428/ (visited on 05/21/2023).

[Sin16]   Saurabh R. Sinha et al. "American Clinical Neurophysiology Society Guideline 1: Minimum Technical Requirements for Performing Clinical Electroencephalography". In: *Journal of Clinical Neurophysiology* 33.4 (Aug. 2016), pp. 303–307. ISSN: 0736-0258. DOI: 10.1097/WNP.0000000000000308. URL: http://journals.lww.com/00004691-201608000-00003 (visited on 07/28/2023).

[Sir14]   J.I. Sirven. "Electrocorticogram (ECOG)". In: *Encyclopedia of the Neurological Sciences*. Elsevier, 2014, pp. 1080–1083. ISBN: 978-0-12-385158-1. DOI: 10.1016/B978-0-12-385157-4.00522-4. URL: https://linkinghub.elsevier.com/retrieve/pii/B9780123851574005224 (visited on 08/15/2023).

[Soo13]   M. H. Soomro et al. "A method for automatic removal of eye blink artifacts from EEG based on EMD-ICA". In: *2013 IEEE 9th International Colloquium on Signal Processing and its Applications*. 2013 IEEE 9th International Colloquium on Signal Processing & its Applications (CSPA). Kuala Lumpur: IEEE, Mar. 2013, pp. 129–134. ISBN: 978-1-4673-5609-1. DOI: 10.1109/CSPA.2013.6530028. URL: http://ieeexplore.ieee.org/document/6530028/ (visited on 08/03/2023).

[Sto14a]   Arkadiusz Stopczynski et al. "Smartphones as pocketable labs: Visions for mobile brain imaging and neurofeedback". In: *International Journal of Psychophysiology* 91.1 (Jan. 2014), pp. 54–66. ISSN: 01678760. DOI: 10.1016/j.ijpsycho.2013.08.007. URL: https://linkinghub.elsevier.com/retrieve/pii/S0167876013002407 (visited on 08/12/2023).

[Sto14b]   Arkadiusz Stopczynski et al. "The Smartphone Brain Scanner: A Portable Real-Time Neuroimaging System". In: *PLoS ONE* 9.2 (Feb. 5, 2014). Ed. by Daniele Marinazzo, e86733. ISSN: 1932-6203. DOI: 10.1371/journal.pone.0086733. URL: https://dx.plos.org/10.1371/journal.pone.0086733 (visited on 08/12/2023).

[Str06]   Ute Strehl et al. "Self-regulation of Slow Cortical Potentials: A New Treatment for Children With Attention-Deficit/Hyperactivity Disorder". In: *Pediatrics* 118.5 (Nov. 1, 2006), e1530–e1540. ISSN: 0031-4005, 1098-4275. DOI: 10.1542/peds.2005-2478. URL: https://publications.aap.org/pediatrics/article/118/5/e1530/69860/Self-regulation-of-Slow-Cortical-Potentials-A-New (visited on 08/09/2023).

[Sur09]   Shravani Sur and Vk Sinha. "Event-related potential: An overview". In: *Industrial Psychiatry Journal* 18.1 (2009), p. 70. ISSN: 0972-6748. DOI: 10.4103/0972-6748.57865. URL: https://journals.lww.com/10.4103/0972-6748.57865 (visited on 08/04/2023).

[Swe13]   Kevin T. Sweeney, Seán F. McLoone, and Tomás E. Ward. "The Use of Ensemble Empirical Mode Decomposition With Canonical Correlation Analysis as a Novel Artifact Removal Technique". In: *IEEE Transactions on Biomedical Engineering* 60.1 (Jan. 2013), pp. 97–105. ISSN: 0018-9294, 1558-2531. DOI: 10.1109/TBME.2012.2225427. URL: http://ieeexplore.ieee.org/document/6332491/ (visited on 08/03/2023).

[Tan10]   Desney S. Tan and Anton Nijholt, eds. *Brain-Computer Interfaces: Applying our Minds to Human-Computer Interaction*. Human-Computer Interaction Series. London: Springer London, 2010. ISBN: 978-1-84996-272-8. DOI: 10.1007/978-1-84996-272-8. URL: http://link.springer.com/10.1007/978-1-84996-272-8 (visited on 07/13/2023).

[Tan16]   Zhichuan Tang et al. "A Brain-Machine Interface Based on ERD/ERS for an Upper-Limb Exoskeleton Control". In: *Sensors* 16.12 (Dec. 2, 2016), p. 2050. ISSN: 1424-8220. DOI: 10.3390/s16122050. URL: http://www.mdpi.com/1424-8220/16/12/2050 (visited on 08/04/2023).

[Tor20]   Edgar P. Torres et al. "EEG-Based BCI Emotion Recognition: A Survey". In: *Sensors* 20.18 (Sept. 7, 2020), p. 5083. ISSN: 1424-8220. DOI: 10.3390/s20185083. URL: https://www.mdpi.com/1424-8220/20/18/5083 (visited on 08/06/2023).

[Tra16]   Lance Traub. "Calculation of Constant Power Lithium Battery Discharge Curves". In: *Batteries* 2.2 (June 11, 2016), p. 17. ISSN: 2313-0105. DOI: 10.3390/batteries2020017. URL: http://www.mdpi.com/2313-0105/2/2/17 (visited on 06/26/2023).

[Tse15]   Kevin Tseng et al. "Design of a Mobile Brain Computer Interface-Based Smart Multimedia Controller". In: *Sensors* 15.3 (Mar. 6, 2015), pp. 5518–5530. ISSN: 1424-8220. DOI: 10.3390/s150305518. URL: http://www.mdpi.com/1424-8220/15/3/5518 (visited on 08/14/2023).

[Uri15]   Jose Antonio Urigüen and Begoña Garcia-Zapirain. "EEG artifact removal—state-of-the-art and guidelines". In: *Journal of Neural Engineering* 12.3 (June 1, 2015), p. 031001. ISSN: 1741-2560, 1741-2552. DOI: 10.1088/1741-2560/12/3/031001. URL: https://iopscience.iop.org/article/10.1088/1741-2560/12/3/031001 (visited on 07/25/2023).

[Vig00]   R. Vigario et al. "Independent component approach to the analysis of EEG and MEG recordings". In: *IEEE Transactions on Biomedical Engineering* 47.5 (May 2000), pp. 589–593. ISSN: 00189294. DOI: 10.1109/10.841330. URL: http://ieeexplore.ieee.org/document/841330/ (visited on 08/03/2023).

[Vig97]   Ricardo Nuno Vigário. "Extraction of ocular artefacts from EEG using independent component analysis". In: *Electroencephalography and Clinical Neurophysiology* 103.3 (Sept. 1997), pp. 395–404. ISSN: 00134694. DOI: 10.1016/S0013-4694(97)00042-8. URL: https://linkinghub.elsevier.com/retrieve/pii/S0013469497000428 (visited on 08/03/2023).

[Vos10]   De Maarten Vos et al. "Removal of Muscle Artifacts from EEG Recordings of Spoken Language Production". In: *Neuroinformatics* 8.2 (June 2010), pp. 135–150. ISSN: 1539-2791, 1559-0089. DOI: 10.1007/s12021-010-9071-0. URL: http://link.springer.com/10.1007/s12021-010-9071-0 (visited on 08/03/2023).

[Wag12]   Johanna Wagner et al. "Level of participation in robotic-assisted treadmill walking modulates midline sensorimotor EEG rhythms in able-bodied subjects". In: *NeuroImage* 63.3 (Nov. 2012), pp. 1203–1211. ISSN: 10538119. DOI: 10.1016/j.neuroimage.2012.08.019. URL: https://linkinghub.elsevier.com/retrieve/pii/S1053811912008129 (visited on 08/12/2023).

[Wah20]   Marc-Nils Wahalla, Guillermo Paya Vaya, and Holger Blume. "CereBridge: An Efficient, FPGA-based Real-Time Processing Platform for True Mobile Brain-Computer Interfaces". In: *2020 42nd Annual International Conference of the IEEE Engineering in Medicine & Biology Society (EMBC)*. 2020 42nd Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC) in conjunction with the 43rd Annual Conference of the Canadian Medical and Biological Engineering Society. Montreal, QC, Canada: IEEE, July 2020, pp. 4046–4050. ISBN: 978-1-72811-990-8. DOI: 10.1109/EMBC44109.2020.9175623. URL: https://ieeexplore.ieee.org/document/9175623/ (visited on 05/09/2023).

[Wah21]   Marc-Nils Wahalla and Holger Blume. "Framework for Live Recording and Algorithmic Evaluation of Ear-EEG on an FPGA-based Mobile Brain-Computer Interface Platform". In: 2021 55th DGBMT Annual Conference on Biomedical Engineering 2021. Hanover, Germany, 2021.

[Wan14]   Yu-Te Wang et al. "Developing an EEG-based on-line closed-loop lapse detection and mitigation system". In: *Frontiers in Neuroscience* 8 (Oct. 13, 2014). ISSN: 1662-453X. DOI: 10.3389/fnins.2014.00321. URL: http://journal.frontiersin.org/article/10.3389/fnins.2014.00321/abstract (visited on 08/12/2023).

[Wan17]   Hongtao Wang and Anastasios Bezerianos. "Brain-controlled wheelchair controlled by sustained and brief motor imagery BCIs". In: *Electronics Letters* 53.17 (Aug. 2017), pp. 1178–1180. ISSN: 0013-5194, 1350-911X. DOI: 10.1049/el.2017.1637. URL: https://onlinelibrary.wiley.com/doi/10.1049/el.2017.1637 (visited on 08/06/2023).

[Was14] Edmund Wascher, Holger Heppner, and Sven Hoffmann. "Towards the measurement of event-related EEG activity in real-life working environments". In: *International Journal of Psychophysiology* 91.1 (Jan. 2014), pp. 3–9. ISSN: 01678760. DOI: 10.1016/j.ijpsycho.2013.10.006. URL: https://linkinghub.elsevier.com/retrieve/pii/S0167876013002833 (visited on 08/12/2023).

[Wic11] Thomas Wichmann and Mahlon R. DeLong. "Deep-brain stimulation for basal ganglia disorders". In: *Basal Ganglia* 1.2 (July 2011), pp. 65–77. ISSN: 22105336. DOI: 10.1016/j.baga.2011.05.001. URL: https://linkinghub.elsevier.com/retrieve/pii/S2210533611001067 (visited on 08/15/2023).

[Wim06] Wim De Clercq et al. "Canonical Correlation Analysis Applied to Remove Muscle Artifacts From the Electroencephalogram". In: *IEEE Transactions on Biomedical Engineering* 53.12 (Nov. 2006), pp. 2583–2587. ISSN: 0018-9294, 1558-2531. DOI: 10.1109/TBME.2006.879459. URL: http://ieeexplore.ieee.org/document/4015602/ (visited on 08/03/2023).

[Woe83] J.C. Woestenburg, M.N. Verbaten, and J.L. Slangen. "The removal of the eye-movement artifact from the EEG by regression analysis in the frequency domain". In: *Biological Psychology* 16.1 (Feb. 1983), pp. 127–147. ISSN: 03010511. DOI: 10.1016/0301-0511(83)90059-5. URL: https://linkinghub.elsevier.com/retrieve/pii/0301051183900595 (visited on 08/03/2023).

[Wöh17] Hendrik Wöhrle et al. "A Hybrid FPGA-Based System for EEG- and EMG-Based Online Movement Prediction". In: *Sensors* 17.7 (July 3, 2017), p. 1552. ISSN: 1424-8220. DOI: 10.3390/s17071552. URL: http://www.mdpi.com/1424-8220/17/7/1552 (visited on 08/16/2023).

[Wol02] Jonathan R Wolpaw et al. "Brain–computer interfaces for communication and control". In: *Clinical Neurophysiology* 113.6 (June 2002), pp. 767–791. ISSN: 13882457. DOI: 10.1016/S1388-2457(02)00057-3. URL: https://linkinghub.elsevier.com/retrieve/pii/S1388245702000573 (visited on 07/13/2023).

[Won14] Savio W.H. Wong, Rosa H.M. Chan, and Joseph N. Mak. "Spectral modulation of frontal EEG during motor skill acquisition: A mobile EEG study". In: *International Journal of Psychophysiology* 91.1 (Jan. 2014), pp. 16–21. ISSN: 01678760. DOI: 10.1016/j.ijpsycho.2013.09.004. URL: https://linkinghub.elsevier.com/retrieve/pii/S0167876013002547 (visited on 08/12/2023).

[Won95] Wonyong Sung and Ki-Il Kum. "Simulation-based word-length optimization method for fixed-point digital signal processing systems". In: *IEEE Transactions on Signal Processing* 43.12 (Dec. 1995), pp. 3087–3090. ISSN: 1053587X. DOI: 10.1109/78.476465. URL: http://ieeexplore.ieee.org/document/476465/ (visited on 09/11/2023).

[Xio22] Xingliang Xiong et al. "Power Spectral Density Features for Classifying Action Intention Understanding EEG Signals". In: *2022 7th International Conference on Intelligent Computing and Signal Processing (ICSP)*. 2022 7th International Conference on Intelligent Computing and Signal Processing (ICSP). Xi'an, China: IEEE, Apr. 15, 2022, pp. 2045–2051. ISBN: 978-1-66547-857-1. DOI: 10.1109/ICSP54964.2022.9778810. URL: https://ieeexplore.ieee.org/document/9778810/ (visited on 08/05/2023).

[Yin15] Erwei Yin et al. "A Dynamically Optimized SSVEP Brain–Computer Interface (BCI) Speller". In: *IEEE Transactions on Biomedical Engineering* 62.6 (June 2015), pp. 1447–1456. ISSN: 0018-9294, 1558-2531. DOI: 10.1109/TBME.2014.2320948. URL: http://ieeexplore.ieee.org/document/6807693/ (visited on 08/08/2023).

[Yoo22] Seungjae Yoo et al. "Zero-Weight aware LSTM Architecture for Edge-Level EEG Classification". In: *2022 IEEE Biomedical Circuits and Systems Conference (BioCAS)*. 2022 IEEE Biomedical Circuits and Systems Conference (BioCAS). Taipei, Taiwan: IEEE, Oct. 13, 2022, pp. 472–476. ISBN: 978-1-66546-917-3. DOI: 10.1109/BioCAS54905.2022.9948628. URL: https://ieeexplore.ieee.org/document/9948628/ (visited on 05/22/2023).

[Zan17] Thorsten O. Zander et al. "Evaluation of a Dry EEG System for Application of Passive Brain-Computer Interfaces in Autonomous Driving". In: *Frontiers in Human Neuroscience* 11 (Feb. 28, 2017). ISSN: 1662-5161. DOI: 10.3389/fnhum.2017.00078. URL: http://journal.frontiersin.org/article/10.3389/fnhum.2017.00078/full (visited on 08/12/2023).

[Zha17] Yi Zhang et al. "Noise-assisted multivariate empirical mode decomposition for multichannel EMG signals". In: *BioMedical Engineering OnLine* 16.1 (Dec. 2017), p. 107. ISSN: 1475-925X. DOI: 10.1186/s12938-017-0397-9. URL: http://biomedical-engineering-online.biomedcentral.com/articles/10.1186/s12938-017-0397-9 (visited on 08/03/2023).

[Zho21] Yuxuan Zhou et al. "Heterogeneous Multi-Agent System for Brain-Computer Interaction in Routing and Forwarding with Memristive Neuron Networks". In: *IEEE Transactions on Parallel and Distributed Systems* (2021), pp. 1–1. ISSN: 1045-9219, 1558-2183, 2161-9883. DOI: 10.1109/TPDS.2021.3137837. URL: https://ieeexplore.ieee.org/document/9661451/ (visited on 05/22/2023).

[Zhu21] Jiayu Zhuang, Keke Geng, and Guodong Yin. "Ensemble Learning Based Brain–Computer Interface System for Ground Vehicle Control". In: *IEEE Transactions on Systems, Man, and Cybernetics: Systems* 51.9 (Sept. 2021), pp. 5392–5404. ISSN: 2168-2216, 2168-2232. DOI: 10.1109/TSMC.2019.2955478. URL: https://ieeexplore.ieee.org/document/8930086/ (visited on 08/06/2023).

[Zin16] Rob Zink et al. "Mobile EEG on the bike: disentangling attentional and physical contributions to auditory attention tasks". In: *Journal of Neural Engineering* 13.4 (Aug. 1, 2016), p. 046017. ISSN: 1741-2560, 1741-2552. DOI: 10.1088/1741-2560/13/4/046017. URL: https://iopscience.iop.org/article/10.1088/1741-2560/13/4/046017 (visited on 08/12/2023).

Appendix

APPENDIX A

Supplementary Tables

This section contains supplementary tables. These are referenced within the corresponding section of the main chapters.

Table A.1: *Revised table for System Specification (S) and Device Mobility (D) scores based on Table 2.8 and 2.9. The values in rows "D" and "S New" were used for Figure 2.11.*

	Publication	D	S Old	Electrode Score	S New
Mobile EEG (Table 2.8)	[Dav07]	0	16	5	11
	[Gra10]	0	15	5	10
	[Gwi10]	0	15	5	10
	[Mai14]	0	17	5	12
	[Cas11]	0	13	4	9
	[Duv13]	0	15	4	11
	[Ehi14]	0	16	5	11
	[Wag12]	0	17	5	12
	[Zan17]	0	13	3	10
	[Bul14]	1	16	5	11
	[Jun16]	1	15	5	10
	[Was14]	1	16	5	11
	[Lot09]	1	15	5	10
	[Ask14]	2	17	4	13
	[Gar08]	2	7	2	5
	[Fit13]	2	11	3	8
	[Dop12]	2	13	1	12
	[Rob15]	3	10	4	6
	[Lin14b]	3	11	3	8
	[Asp15]	3	6	2	4
	[Klo13]	3	6	2	4
	[Liu13]	3	10	2	8
	[Won14]	3	10	2	8
	[Wan14]	3	10	3	7
	[Deb12]	3	8	4	4
	[De 14]	3	8	4	4
	[Zin16]	3	12	3	9
	[Sto14b; Sto14a]	4	6	2	4
	[Deb15]	4	12	3	9
Embedded (Table 2.9)	[Kar17]	5	11	2	9
	[McC17]	5	9	4	5
	[Tse15]	4	10	1	9
	[Lin14a]	4	6	1	5
	[Lin16]	4	6	1	5
	[Jia12]	4	7	1	6
	[Ram19]	4	9	1	8
	[Shy10]	5	10	3	7

Table A.2: *Early power estimation results in mW for the FPGAs of Table 4.2 for no (I), medium (II) and heavy (III) logic resource usage and clock frequencies of 1 MHz (-1), 5 MHz (-5), 20 MHz (-20) as well as 50 MHz (-50)*

	Scenario	I-1	I-5	I-20	I-50	II-1	II-5	II-20	II-50	III-1	III-5	III-20	III-50
Xilinx	XCAU7P	183	183	184	186	185	193	222	281	186	198	244	336
	XCAU10P	262	262	263	265	264	272	303	366	266	283	348	478
	XC7Z014S*	106	106	107	108	109	119	159	240	110	124	179	288
	XC7S75	103	103	104	105	105	116	158	240	107	122	181	299
	XC6SLX75	67	67	68	69	72	86	138	242	77	109	231	475
	XC7A75T	97	98	98	100	100	111	153	235	101	117	176	294
Intel	EP4CE55	128	128	129	129	133	153	229	381	140	187	363	715
	EP4CGX75	151	152	152	153	157	178	257	415	163	211	389	745
	EP4CE75	140	140	140	141	145	166	244	401	152	199	378	736
	5CGXC5	236	236	237	238	239	249	290	372	242	266	357	538
	5CEA5	236	236	237	238	238	249	290	372	242	266	356	538
	5CGTD5	236	236	237	238	239	249	290	372	242	266	357	538
	10CL055	119	119	120	120	124	144	220	371	131	178	353	704
Microchip	M2GL050	17	17	18	21	21	36	95	213	26	62	197	468
	M2GL060	20	20	21	24	24	39	98	216	29	64	199	469
	M2S050*	17	17	18	21	21	36	95	213	26	62	197	468
	M2S060*	20	20	21	24	24	39	98	216	29	64	199	469

Microcontroller or microprocessor within SoCs are unused and should not affect the results

APPENDIX B

Circuit Documentation for the CereBridge MSTRB v1.1

This section contains the documentation for the Master and Processing Board (MSTRB) v1.1 module of the CereBridge system. The following information is provided in the appropriate order:

- Bill of Materials
- Schematic
- Component Assembly Plan Top
- Layout Layers 1-8
- Component Assembly Plan Bottom

Bill of Materials (BOM)

MSTRB 1.1 / 10.2022 / MARC-NILS WAHALLA

Legend:
- IC = Integrated Circuits + Quartz
- = LEDs
- EM = Electromechanical
- C = Chip Capacitors
- R = Chip Resistors
- L = Chip Inductors

Line #	Name	Description	Designator TOP	Designator BOT	Quantity	Manufacturer	Manufacturer Part Number	Group	DNP
1	TPS61071	TPS61x 90% Efficient Synchronous Boost Converter With 600-mA Switch, Adjustable Output Voltage Up to 5V5		U6	1	Texas Instruments	TPS61071DDCR	IC	
2	TPS6208812	Tiny 6-pin 3-A Step-Down Converter in 1.2-mm x 0.8-mm WCSP, Fixed 1V2 output voltage		U5	1	Texas Instruments	TPS6208812YFPR	IC	
3	M2S050-FCS325I	SmartFusion2 SoC FPGA, ARM Cortex-M3, 50 k LUTs, 200 User I/O, Design Security, -40 to 100 degC, 325-Ball BGA	U1		1	Microsemi	M2S050-FCS325I	IC	
4	MAX8663	PMIC with integrated Li charger, 2 Buck/Boost Converters and 4 LDOs	U3		1	Maxim	MAX8663ETL+	IC	
5	TPS3702	TPS3702CX10DDCT, Fixed Threshold 1V		U4	1	Texas Instruments	TPS3702CX10DDCT	IC	
6	MT46H32M16LFBF-5 IT	512Mb LPDDR400 SDRAM, 32Mb x16, 1.8V, -40 to 85 degC, 60-Ball VFBGA, Pb-Free	U2		1	Micron Technology	MT46H32M16LFBF-5 IT:C TR	IC	
7	32.768kHz	32.768kHz crystal 1.2mm x 1.6mm		Y1	1	Abracon	ABS05W-32.768KHZ-K-2-T	IC	
8	PMZB3S0UPE,315	Single P-Channel Trench MOSFET, -20 V, -55 to 150 degC, 3-Pin SOT883B, Reel	Q1, Q2		2	Nexperia	PMZB3S0UPE,315	IC	
9	16-219A/T2D-AR2T1QY/3T	Chip LED, White, 5 V, 10 mA, 30 mW, -40 to 85 degC, 2-Pin SMD (0402), RoHS, Tape and Reel	DS5		1	Everlight	LB QH9G-N1OO-35-1	(LED)	
10	LNJ347W83RA	Hight Bright Surface Mounting Chip LED, Green, 55 mW, -30 to 85 degC, 2-Pin SMD, RoHS, Tape and Reel	DS1, DS2		2	ROHM Semiconductor	SML-P13FTT86R	(LED)	
11	APHHS1005SURCK	Red Water Clear Chip LED Lamp, 1.95 V, 20 mA, -40 to 85 degC, 2-Pin SMD (0402), RoHS, Tape and Reel	DS3, DS4		2	Kingbright	APHHS1005SURCK	(LED)	
12	100uF	Polarized Capacitor (Surface Mount), 100uF, 0805(2012)	C35, C88		2	Kyocera AVX	F980G107MSA	C	
13	220uF	Polarized Capacitor (Surface Mount), 220uF, 1206(3216)	C33, C34		2	Kyocera AVX	F95OG227MSAAM1Q2	C	
14	GRM033R61C393KE84D	Chip Multilayer Ceramic Capacitors for General Purpose, 0201, 39000pF, X5R, 15%, 10%, 16V	C78		1	Murata	GRM033R61C393KE84D	C	
15	22uF	Polarized Capacitor (Surface Mount), 22uF, 0603(1608)	C60	C62, C64	3	Kyocera AVX	F380J226MMAAH1	C	
16	47uF	Polarized Capacitor (Surface Mount), 47uF, 0603(1608)	C36	C10	2	Kyocera AVX	F380J476MMAAXEH3	C	
17	CAP 6.8pF 25V 0201(0603)	CAP 6.8pF 25V ±0.1pF 0201 (0603 Metric) Thickness 0.33mm SMD		C66, C67	2	Kyocera AVX	02013A6R8BAT2A	C	
18	CAP 4.7uF 6.3V 0603(1608)	CAP 4.7uF 6.3V ±20% 0603 (1608 Metric) Thickness 1mm SMD			1	KEMET	C0603C475M9PACTU	C	C9
19	CAP 4.7uF 10V 0603(1608)	CAP 4.7uF 10V ±10% 0603 (1608 Metric) Thickness 0.55mm SMD	C81, C82		2	Murata	GRM185R61C475KE11D	C	
20	CAP 2.2uF 6.3V 0402(1005)	CAP 2.2uF 6.3V ±10% 0402 (1005 Metric) Thickness 0.6mm SMD	C77		1	Kyocera AVX	04026D225KAT2A	C	
21	330uF	Polarized Capacitor (Surface Mount), 330uF, 1411(3528)	C32		1	KEMET	T490B337M006ATE800	C	
22	CAP 10nF 10V 0201(0603)	CAP 10nF 10V ±10% 0201 (0603 Metric) Thickness 0.33mm SMD		C15, C16, C17, C18, C19, C24, C27, C31, C44, C45, C46, C47, C48, C49, C50, C51, C55, C58	18	Yageo	CC0201KRX7R6BB103	C	
23	CL05A106MP5NUNC	Chip Capacitor, 10 uF, +/- 20%, 10 V, -55 to 85 degC, 0402 (1005 Metric), RoHS, Tape and Reel	C89, C90, C73, C79, C80, C57, C21, C22, C25, C28	C54, C59, C84, C85	14	Murata	ZRB15XR61A106ME01D	C	
24	CAP 4.7uF 6.3V 0402(1005)	CAP 4.7uF 6.3V ±10% 0402 (1005 Metric) Thickness 0.6mm SMD	C70, C71,	C83, C86, C87	5	TDK	C1005X5R0J475K050BC	C	
25	CAP 1uF 10V 0402(1005)	CAP 1uF 10V ±10% 0402 (1005 Metric) Thickness 0.6mm SMD	C69, C74, C75, C76		4	Kyocera AVX	04022D105KAT2A	C	
26	CAP 100nF 10V 0201(0603)	CAP 100nF 10V ±10% 0201 (0603 Metric) Thickness 0.33mm SMD	C72	C1, C2, C3, C4, C5, C6, C7, C8, C11, C12, C13, C14, C20, C23, C26, C29, C30, C37, C38, C39, C40, C41, C42, C43, C52, C53,	32	Taiyo Yuden	LMK063C6104KP-F	C	

Line #	Name	Description	Designator TOP	Designator BOT	Quantity	Manufacturer	Manufacturer Part Number	Group	DNP
27	RES0603	0603 (1608 Metric) Chip Resistor	R56, R58, R61, R62		4	Mouser	KDV06FR050ET	R	
28	6K2 5% 0201(0603)	6K2 0.05W 5% 0201 (0603 Metric) SMD	R37		1	Vishay Dale	CRCW02016G20JNED	R	
29	91R 5% 0201(0603)	91R 0.05W 5% 0201 (0603 Metric) SMD	R60		1	Yageo	RC0201JR-0791RL	R	
30	82R 1% 0201(0603)	82R 0.05W 1% 0201 (0603 Metric) SMD	R54, R55, R57, R59		4	Yageo	RC0201FR-0782RL	R	
31	3K3 5% 0201(0603)	3K3 0.05W 5% 0201 (0603 Metric) SMD	R44		1	Bourns	CR0201-JW-332GLF	R	
32	1M8 5% 0201(0603)	1M8 0.05W 5% 0201 (0603 Metric) SMD		R50	1	Yageo	RC0201FR-071M8L	R	
33	165K 1% 0402(1005)	165K 0.063W 1% 0402 (1005 Metric) SMD	R45		1	Yageo	RC0402FR-07165KL	R	
34	1R 1% 0201(0603)	1R 0.05W 1% 0201 (0603 Metric) SMD	R11	R12, R13	3	Yageo	RC0201FR-071RL	R	
35	180K 1% 0201(0603)	180K 0.05W 1% 0201 (0603 Metric) SMD		R51	1	Yageo	RC0201FR-07180KL	R	
36	CPF0402B200KE1	Chip Resistor, 200 KOhm, +/- 0.1%, 0.063 W, -55 to 155 degC, 0402 (1005 Metric), RoHS, Tape and Reel	R46, R48		2	TE Connectivity	CPF0402B200KE1	R	
37	47K 5% 0201(0603)	47K 0.05W 5% 0201 (0603 Metric) SMD	R52, R53		2	Yageo	RC0201JR-0747KL	R	
38	47K 1% 0201(0603)	47K 0.05W 1% 0201 (0603 Metric) SMD	R63, R20, R21, R22, R23, R24		7	Yageo	RC0201FR-0747KL	R	R19
39	240R 1% 0201(0603)	240R 0.05W 1% 0201 (0603 Metric) SMD		R15	1	Yageo	RC0201FR-07240RL	R	
40	470K 1% 0402(1005)	470K 0.063W 1% 0402 (1005 Metric) SMD	R47		1	Yageo	RC0402FR-07470KL	R	
41	47K 5% 0603(1608)	47K 0.1W 5% 0603 (1608 Metric) SMD		R14, R74	1	Yageo	RC0603JR-0747KL	R	
42	1K 1% 0201(0603)	1K 0.05W 1% 0201 (0603 Metric) SMD	R9, R10		2	Yageo	RC0201FR-071KL	R	
43	10K 5% 0201(0603)	10K 0.05W 5% 0201 (0603 Metric) SMD	R7, R8	R70, R41, R42, R43, R29, R30, R31, R32, R33, R34, R25, R26, R16, R17, R18, R5, R6	25	Yageo	RC0201JR-0710KL	R	R27, R28, R38, R39, R40, R73
44	100R 1% 0201(0603)	100R 0.05W 1% 0201 (0603 Metric) SMD		R1	1	Yageo	RC0201FR-07100RL	R	
45	Jumper 0603(1608)	Jumper 0603 (1608 Metric)	R65, R67, R3	R36, R68	13	Bourns	CR0603-J/-000ELF	R	R2, R4, R35, R64, R66, R69, R71, R72
46	100K 1% 0402(1005)	100K 0.063W 1% 0402 (1005 Metric) SMD		R49	1	Yageo	RC0402FR-07100KL	R	
47	4.7uH	LQM2MPN4R7NG0L, 0805, 4.7uH +-30%, 1.1A rated Current, 0.140 Ohm DC Resistance		L5	1	Murata	LQM2MPN4R7NG0L	L	
48	74404032033	WE-LQS SMD Power Inductor, L=3.3 µH	L2		1	Wurth Electronics	74404032033	L	
49	74404042047	WE-LQS SMD Power Inductor, L=4.7 µH	L3		1	Wurth Electronics	74404042047	L	
50	240uH	DFE18SANR24MG0L, 0603, 0.24uH +-20%, 3,2A rated Cirremt, 0.036 Ohm DC Resistance		L4	1	Murata	DFE18SANR24MG0L	L	
51	LQG15HN2N02D	Chip Inductor, 22 nH, +/- 5%, 300 mA, -55 to 125 degC, 0402 (1005 Metric), RoHS, Tape and Reel	L1		1	Murata	LQG15HN2N02D	L	
52	SEM-110-02-03.0-H-D-WT-K	Micro Tiger Eye™ Socket Strip, 0.80 mm pitch	J1, J2		2	Samtec	SEM-110-02-03.0-H-D-WT-K	EM	
53	SEM-115-02-03.0-H-D-WT	.8MM TIGER EYE MICRO SOCKET		J3, J4	2	Samtec	SEM-115-02-03.0-H-D-WT	EM	
54	FTE-105-01-G-DH	FTE-105-01-G-DH, 5x2 Pins, 0.8mm pitch, horizontal, header		CP9	1	Samtec	FTE-105-01-G-DH	EM	
55	22-28-4033	Male Header, Pitch 2.54 mm, 1 x 3 Position, Height 8.38 mm, Tail Length 3.18 mm, RoHS, Bulk	CP5		1	TE Connectivity / AMP	3-644457-3	EM	
56	450302014072	WS-SLTU 10mm*2.5mm, SPDT, ON-ON, 2.54mm, right angle type, THT, Mini Slide Switch, 3 pins	SW4		1	Wurth Electronics	450302014072	EM	
57	46765-0001	Connector		J5	1	Molex	46765-0001	EM	
58	0294-0-15-01-06-27-10-0	Pin Receptacle Connector, 0.076' (Min) Mounting Hole, 0.206' Length	MH1, MH2, MH3, MH4		4	Mill-Max	0294-0-15-01-06-27-10-0		
59	KMS231GPLFS	SWITCH TACTILE SPST-NO 0.05A 50V	SW1, SW2, SW3		3	ITT	KMS231GPLFS	EM	
60	1040310811	Micro SD Card, RA, -25 to 85 degC, 8-Pin SMD, RoHS, Tape and Reel	SD1		1	Molex	1040310811	EM	
61	GRP8021VWVN-RC	Male Header, Pitch 1.27 mm, 1 x 2 Position, Height 4 mm, Tail Length 2.3 mm, -40 to 105 degC, RoHS, Bulk	CP6, CP7, CP8, CP11, CP12		5	Harwin	M50-3530242	EM	
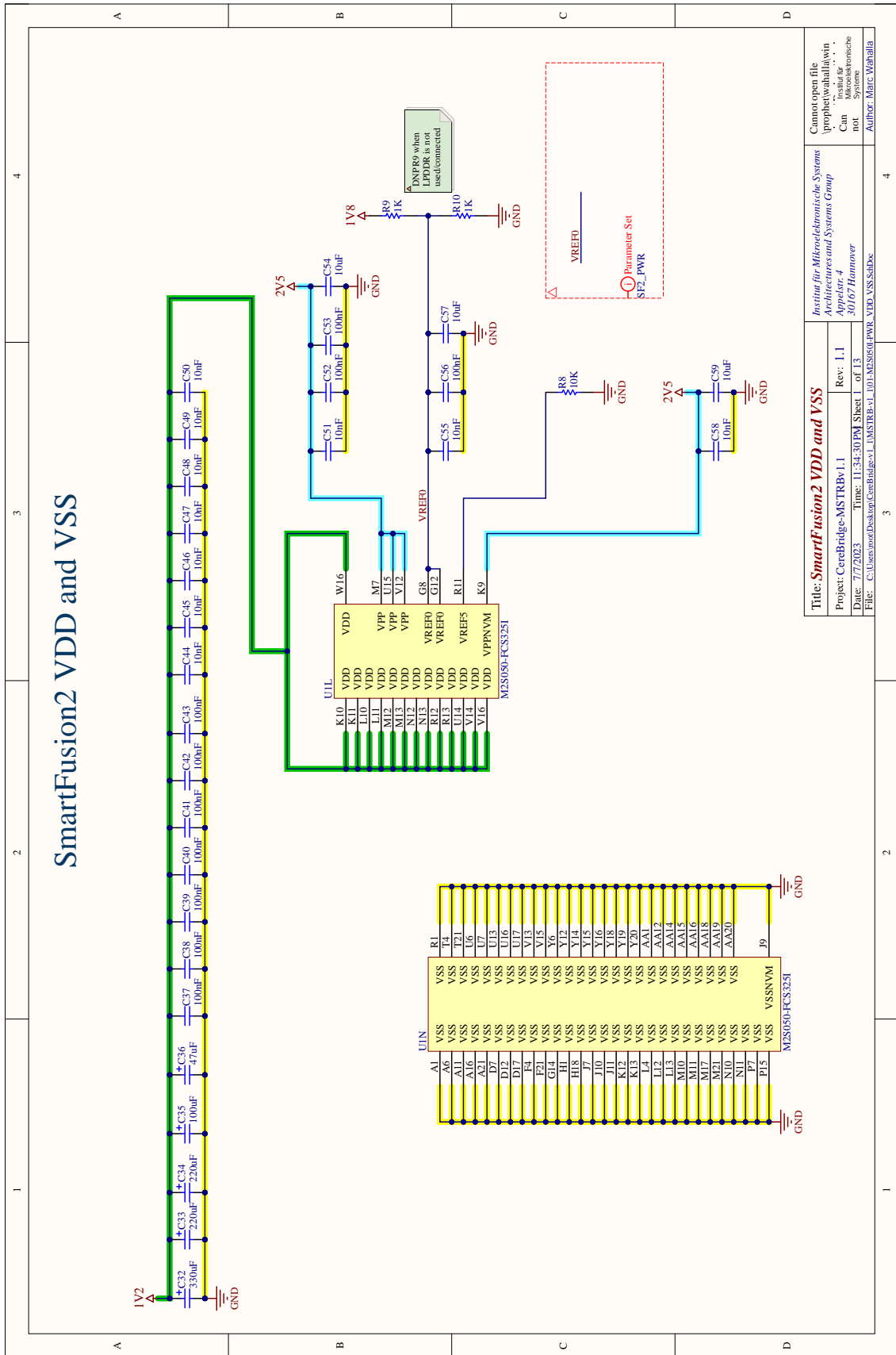
SmartFusion2 VDD and VSS

SmartFusion2 VDDIO (Bank Supply)

SmartFusion2 OSC, PLL and Reset

UserLogicButtonR

UserLogicButtonL

GlobalReset

1V8 R74 47K
1V8 R14 47K

SW3 Right Button
SW2 Left Button
SW1 Reset Button

2V5 R52 47K
2V5 R53 47K

U4 TPS3702
Sense UV
VDD
SET OV
GND
1V2
2V5
C68 100nF
GND

U1J M2S050-FCS325I
M9 DEVRST_N
D18 MDDR_IMP_CALIB
AA4 XTLOSC_MAIN_XTAL
Y4 XTLOSC_MAIN_EXTAL

R15 150R
GND

Y1 32.768kHz
C66 6.8pF
C67 6.8pF
GND

U1K M2S050-FCS325I
CCC_NE0_NE1_MSS_MDDR_PLL_VSSA G7
CCC_NW0_NW1_PLL_VSSA H15
CCC_SW0_SW1_PLL_VSSA R15
GND

CCC_NE0_NE1_MSS_MDDR_PLL_VDDA H7
CCC_NW0_NW1_PLL_VDDA G15
CCC_SW0_SW1_PLL_VDDA R14

PLL_MDDR
C60 22uF C61 100nF R11 1R GND
PLL_NW
C62 22uF C63 100nF R12 1R GND
PLL_SW
C64 22uF C65 100nF R13 1R GND

2V5

Parameter Set
SF2_PWR
PLL_MDDR
PLL_NW
PLL_SW

Title: **SmartFusion2 OSC, PLL and Reset**
Project: CereBridge-MSTRBv1.1   Rev: 1.1
Appelstr. 4
30167 Hannover
Date: 7/7/2023   Time: 11:34:30 PM   Sheet 3 of 13
File: C:\Users\root\Desktop\CereBridge-v1_1\MSTRB-v1_1\03-M2S050-OSC_PLL_Reset.SchDoc

Institut für Mikroelektronische Systeme
Architectures and Systems Group

Cannot open file \prophet\wahalla\win Institut für Mikroelektronische not Systeme

Author: Marc Wahalla

SmartFusion2 JTAG

All resistors on this sheet were described as 1kOhm within to "Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs". Since 10kOhm was used for R18 on the EvalBoard this value will be used to lower static power consumption.

JTAGSEL chooses between
- High: FPGA fabric TAP
- Low: Cortex-M3 JTAG
Default configuration should be High but can be pulled down within the stationary board where the JTAG connector(s) are placed as well.

Title: **SmartFusion2 JTAG**

Project: CereBridge-MSTRBv1.1   Rev: 1.1

Date: 7/7/2023   Time: 11:34:31 PM Sheet 4 of 13

File: C:\Users\root\Desktop\CereBridge-v1_1\MSTRB-v1_1\04-M2S050I-JTAG.SchDoc

Institut für Mikroelektronische Systems
Architectures and Systems Group
Appelstr. 4
30167 Hannover

Cannot open file
\prophet\wahalla\win
Can   Institut für
not   Mikroelektronische
          Systeme

Author: Marc Wahalla

SmartFusion2 DDR-Interface

SmartFusion2 Used IO Banks

SmartFusion2 Unused Banks and Pins

U1O — M2S050-FCS325I

Pin	Net		Pin	Net
V17	DNC	DNC	AA17	
V18	DNC			
Y13	DNC		Y5	
Y17	DNC	NC	AA5	
AA13	DNC	NC		

U1H — BANK 8 — M2S050-FCS325I

MSIO95PB8, MSIO95NB8, MSIO96PB8, MSIO96NB8, MSIO98PB8, MSIO98NB8, MSIO99PB8, MSIO99NB8, MSIO100PB8, MSIO100NB8, MSIO102PB8, MSIO102NB8, MSIO103PB8, MSIO103NB8, MSIO104PB8, MSIO104NB8, MSIO106PB8, MSIO106NB8, MSIO107PB8, MSIO107NB8, MSIO108PB8, MSIO108NB8, MSIO110PB8, MSIO110NB8, MSIO111PB8, MSIO111NB8, MSIO112PB8, MSIO112NB8, MSIO114NB8, MSIO115NB8, MSIO116NB8, MSIO117NB8

MSIO114PB8/GB6/CCC_NW1_CLKI1, MSIO115PB8/GB2/CCC_NW0_CLKI1, MSIO116PB8/CCC_NW1_CLKI0, MSIO117PB8/CCC_NW0_CLKI0

U1G — BANK 7 — M2S050-FCS325I

MSIOD118PB7/GB5/CCC_SW1_CLKI1, MSIOD119PB7/GB1/CCC_SW0_CLKI1, MSIOD119NB7, MSIOD120PB7/CCC_SW1_CLKI0, MSIOD120NB7, MSIOD121PB7/CCC_SW0_CLKI0, MSIOD121NB7, MSIOD135PB7, MSIOD135NB7, MSIOD136PB7, MSIOD136NB7, MSIOD138PB7, MSIOD138NB7, MSIOD140PB7, MSIOD140NB7, MSIOD142PB7, MSIOD142NB7

U1E — BANK 5 — M2S050-FCS325I

DDRIO147PB5, DDRIO147NB5/CCC_SW0_CLKI2, DDRIO148PB5/PROBE_A, DDRIO148NB5/PROBE_B, DDRIO152PB5/GB3/CCC_SW0_CLKI3, DDRIO152NB5/GB7/CCC_SW1_CLKI2, DDRIO159PB5/CCC_SW1_CLKI3, DDRIO159NB5, DDRIO160PB5/VCCC_SE0_CLKI, DDRIO160NB5, DDRIO161PB5/GB11/VCCC_SE0_CLKI, DDRIO161NB5, DDRIO163PB5/GB15/VCCC_SE1_CLKI, DDRIO163NB5, DDRIO164PB5/VCCC_SE1_CLKI, DDRIO164NB5, DDRIO172PB5, DDRIO172NB5, DDRIO177PB5, DDRIO177NB5, DDRIO184PB5, DDRIO184NB5, DDRIO186PB5, DDRIO186NB5

U1F — BANK 6 — M2S050-FCS325I

MSIOD145PB6, MSIOD145NB6, MSIOD146PB6, MSIOD146NB6

LPDDR 512Mb Micron (Optional)

LPDDR_ADDR

LPDDR_BYTELINE0

LPDDR_BYTELINE1

BYTELINE0

BYTELINE1

LPDDR_CTRL_CLK

LPDDR_ADDR

LPDDR_CTRL_CLK

U2A — MT46H32M16LFBF-5 IT

U2B — MT46H32M16LFBF-5 IT

1V8

GND

Decoupling Guidelines (www.micron.com/media/documents/products/technical-note/dram/tn4619.pdf):
- Number and location of capacitors are of greater importance than the exact value of each capacitor
- choose lowest ESL capacitor package, highest capacitance available in that package
- place capacitors as close as possible to each corner of each LPDDR device
- minimum 6 layers, layer 2,3 and 5 for power planes
- signal layer impedance controlled: 50-60 Ohm for a 5 mil wide trace
- Most LPDDR designs reference DQ, strobe, and clock signals to Vss; address, command, and control signals are referenced to Vdd. DQ signals are generally routed on the outer layers of the PCB
- recommended trace width: DQ lines = 4 mil minimum, 6 mil nominal, DQS lines = 4 mil minimum, 6 mil nominal, Address lines = 4 mil minimum, 6 mil nominal, Command/control lines = 4 mil minimum, 6 mil nominal, Clock lines = 4 mil minimum, 610 mil nominal
- recommended trace spacing (all nominal): 12 mil except CAS#, RAS#, WE#, CS# and CKE which should be 15 mil
- place DQS in the midst of related nibbles or bytes
- CK and CK# should have differential characteristic Impedance of 100-120 Ohm, trace length matching with +-20mil, inner plane routing minimizes EMI, Clock lengths to all signals should be within +-400mil
- trace lengths for data group within +-50 mil

Decoupling Calculation For DDR (https://www.micron.com/resource-center/resource-details/2fa515c8-b501-425e-8325-c45d53c718a2):
- Using 0.1µF caps in a 0603 package
should provide sufficient capacitance
- Capacitor Package should provide a low (parasitic) Inductance

DDR Memory and Interface Design Trends (http://jp.tek.com/dl/E2_TIF2012_DDR_trends.pdf):
- Bulk Capacitance only needed if DDR is at a long distance from supply regulator
- one cap per supply bin at minimal distance

place at midpoint
R1
100Ω

C1 100nF   C2 100nF   C3 100nF   C4 100nF   C5 100nF   C6 100nF   C7 100nF   C8 100nF   C9 4.7uF DNP

PRGD Board Connectors

MII Interface:
Trace Length Matching within 10mm
Total Length should not exceed 150mm

Implement parallel termination on receiving ends, SF2 has ODT for receiving signals

BASE-B_MII
Parameter Set
MII_Interface

TXC	MII TXC
TXEN	MII TXEN
TXD0	MII TXD0
TXD1	MII TXD1
TXD2	MII TXD2
TXD3	MII TXD3
RXC	MII RXC
RXDV	MII RXDV
RXD0	MII RXD0
RXD1	MII RXD1
RXD2	MII RXD2
RXD3	MII RXD3
EXER	MII RXER
CRS	MII CRS
COL	MII COL

MII

BASE-B_USB-UART
SoC-TXD | UART0_TXD
SoC-RXD | UART0_RXD

USB-UART

BASE-B_GP
GP0 | GP0
GP1 | GP1
GP2 | GP2
GP3 | GP3
GP4 | GP4
GP5 | GP5
GP6 | GP6
GP7 | GP7

BASE-B_AUX

WiLess-B_UART
SoC-TXD | UART1_TXD
SoC-RXD | UART1_RXD

WiLess-UART

WiLess-B_CTRL
GP0 | WB_GP0
GP1 | WB_GP1

WiLess-CTRL

UserLogicButtonL | UserButton_Left
GlobalReset | GLB_RST

JTAG
JTAG_TDI | TDI
JTAG_TDO | TDO
JTAG_TCK | TCK
JTAG_TMS | TMS
JTAG_nTRST | nTRST
JTAGSEL | Select
JTAG

Pins from the Harnesses
"WiLess-B_UART" and
"WiLess-B_CTRL" are reserved for use
with the WiLess-Board by default.
Nevertheless, those pins can be used on
the BASE-Board if WiLess-Board is not
present or if the CTRL-pins are not used
by the WiLess-Board.

J3 SEM-115-02-03.0-H-D-WT

UART1_TXD 29	29	30	30 WB_GP1
UART1_RXD 27	27	28	28 WB_GP0
25	25	26	26
23	23	24	24
21	21	22	22
19	19	20	20
GP1 17	17	18	18 GP6
GP5 15	15	16	16 GP7
GP0 13	13	14	14 GP2
11	11	12	12 GP3
09	09	10	10 GP4
07	07	08	08
UART0_TXD 03	05	06	06
UART0_RXD 01	03	04	04
	01	02	02

V_ext

GND

J4 SEM-115-02-03.0-H-D-WT

02	02	01	01 MII TXD3
UserButton_L 04	04	03	03 MII TXD2
GLB_RST 06	06	05	05 MII TXD0
08	08	07	07 MII TXD1
10	10	09	09 MII TXC
12	12	11	11 MII RXD3
14	14	13	13 MII RXD2
JTAGSEL 16	16	15	15 MII RXD1
JTAG_TDI 18	18	17	17 MII RXD0
JTAG_TDO 20	20	19	19 MII RXC
JTAG_TCK 22	22	21	21 MII RXDV
JTAG_nTRST 24	24	23	23 MII RXER
JTAG_TMS 26	26	25	25 MII TXEN
28	28	27	27 MII COL
30	30	29	29 MII CRS

V_ext

2V5

GND

MH1
Mounting Hole ME
GND

MH2
Mounting Hole NW
GND

MH3
Mounting Hole NE
GND

MH4
Mounting Hole SE
GND

Title: **PRGD Board Connectors**		
Project: CereBridge-MSTRBv1.1		Rev: 1.1
Date: 7/7/2023	Time: 11:34:31 PM	Sheet 09 of 13
File: C:\Users\root\Desktop\CereBridge-v1_1\MSTRB-v1_1\09-BASE-Board_Connectors.SchDoc		

Institut für Mikroelektronische Systeme
Architectures and Systems Group
Appelstr. 4
30167 Hannover

Cannot open file
\prophet\walhalla\win
Can   Institut für
not   Mikroelektronische
         Systeme
Author: Marc Wahalla

ADC-Board Connectors

Pins with even numbers should show to the inside of the pcb

J1 SEM-1-10-02-03.0-H-D-WT-K

01	ADC-SPI_MOSI	
03	ADC-SPI_CS0	
05	GND	
07	ADC-SPI_CLK	
09	ADC-SPI_CS1	
11	ADC-SPI_CS2	
13	ADC-START	
15	GND	
17	ADC-SPI_CS3	
19	ADC-SPI_MISO	

02	ADC-GP0
04	ADC-DRDY0
06	1V8
08	GND
10	ADC-DRDY1
12	ADC-DRDY2
14	GND
16	1V8
18	ADC-DRDY3
20	ADC-GP1

J2 SEM-1-10-02-03.0-H-D-WT-K

01	GND
03	5V5
05	5V5
07	5V5
09	5V5
11	5V5
13	5V5
15	5V5
17	5V5
19	GND

ADCCNTRL

ADC-B_CNTRLSIG
- ADC-START — START
- ADC-DRDY0 — DRDY0
- ADC-DRDY1 — DRDY1
- ADC-DRDY2 — DRDY2
- ADC-DRDY3 — DRDY3
- ADC-GP0 — GP0
- ADC-GP1 — GP1

ADCSPI

ADC-B_SPI
- ADC-SPI_MOSI — MOSI
- ADC-SPI_MISO — MISO
- ADC-SPI_CLK — SCLK
- ADC-SPI_CS0 — CS0
- ADC-SPI_CS1 — CS1
- ADC-SPI_CS2 — CS2
- ADC-SPI_CS3 — CS3

Additional-Board Connectors

WILB Connector

CP9

VCC-WB	1 2
WB_GP1	3 4 GNDorRST
UART1_TXD	5 6
WB_GP0	7 8
UART1_RXD	9 10

FTE-105-01-G-DH

GND

MicroHDMI Connector

J5

UART0_RXD	1	HOT_PLUG_DETECT TMDS_CLOCK_SHIELD 13
	2	UTILITY TMDS_CLOCK- 14
	3	TMDS_DATA2+ CEC 15
WB_GPI	4	TMDS_DATA2_SHIELD DDC/CEC_GROUND 16
	5	TMDS_DATA2- SCL 17
	6	TMDS_DATA1+ SDA 18
	7	TMDS_DATA1_SHIELD +5V_POWER 19
WB_GP0	8	TMDS_DATA1- MP1
	9	TMDS_DATA0+ MP2
	10	TMDS_DATA0_SHIELD MP3
	11	TMDS_DATA0- MP4
UART0_TXD	12	TMDS_CLOCK+

467651001

V_ext

GND

V_ext

UART1_RXD

GND

The J5 connector (micro HDMI) is intended to connect the CereBridge platform to the SensOhr (Fraunhofer IDMT) through an SPI interface. Hereby, the CereBridge platform is meant to be SPI slave.

The signals are intended as follows:
- V_ext: External 5V power supply to power the CereBridge system (with no separate battery connected)
- WB_GP0: SPI_SS
- UART0_RXD: SPI_MOSI
- UART0_TXD: SPI_Clk
- WB_GP1: SPI_MISO
- UART1_RXD: Optional data line for Interrupt signal or similar

All data signal connections are running with 3V3 by default.

WiLess-B_UART

WiLess-UART

SoC-TXD	UART1_TXD
SoC-RXD	UART1_RXD

WiLess-B_CTRL

WiLess_CTRL

GP0	WB_GP0
GP1	WB_GP1

BASE-B_USB-UART

USB-UART

SoC-TXD	UART0_TXD
SoC-RXD	UART0_RXD

3V3 2V5 1V8

R36 R35 R71
0R   0R DNP 0R DNP

VCC-WB

UserButton_Left UserLogicButtonL

GLB_RST GlobalReset

R66 R69 R68
0R DNP 0R DNP 0R

GNDorRST

GND

SD-Card Socket

SDCSPI

SDC_SPI
CS SDC-SPI_CS
MOSI SDC-SPI_MOSI
SCK SDC-SPI_SCK
MISO SDC-SPI_MISO

SDC-LoadSw

SDC-LoadSw R67 0R

R24 47K

3V3

Q1 PMZB3350UPE,315

The Q1 load switch enables the SF2 to turn-off the (socketed) SD-card in runtime (if Resistor R67 is placed).

L1 22nH

C69 1uF GND

R19 47K DNP

R20 47K
R21 47K

R22 47K
R23 47K

SD CARD

SDI
DAT2
CD/DAT3
CMD
VDD
CLK
VSS
DAT0
DAT1

CD_A SDC-DetectA
CD_B SDC-DetectB
SHLD
SHLD

104031-0811

GND

GND

SDC-DetectA
SDC-DetectB

Informations from mikrocontroller.net:
- Clock frequency during initialization not higher than 400kHz
- After Deselecting the card (CS# -> '1') pulse the clock signal a few more times to ensure the cards outputs is going high-Z
- if p-channel Mosfet is used for powering off the SD-card ensure that all control lines are pulled low to avoid powering the card through them

Power Management

CAMtasticDXP (TM):

Curriculum Vitae

About the Person	Marc-Nils Wahalla born on 31.12.1986 in Hanover (Lower Saxony)

Education

10/2007 - 06/2014	**Electrical Engineering Studies** Leibniz Universität Hannover Microelectronics Track Degree *Diplom-Ingenieur (Dipl.-Ing.)*
1999 - 2006	**St. Ursula-Schule Hannover** Hannover Degree *Abitur*

Work Experience

since 11/2022	**Employee in Technology and Administration** Presidential Staff Leibniz Universität Hannover
07/2014 - 10/2022	**Research Engineer** Institute of Microelectronic Systems Architecture and Systems Group Leibniz Universität Hannover
12/2014 - 04/2015	**Development Engineer** MediTECH Electronic GmbH Wedemark - Bissendorf
07/2012 - 11/2012	**Specialized Internship** Sennheiser electronic GmbH & Co. KG Department of Research and Development San Francisco, USA
01/2010 - 03/2011	**Student Assistant (Research & Teaching)** Institute of Theoretical Electrical Engineering Leibniz Universität Hannover
05/2008 - 12/2009	**Student Assistant (Research)** Institute of Production Engineering and Machine Tools Leibniz Universität Hannover

Conference Papers

CereBridge: An Efficient, FPGA-based Real-Time Processing Platform for True Mobile Brain-Computer Interfaces
M.-N. Wahalla; G. Paya Vaya; H. Blume
42nd Annual International Conference of the IEEE Engineering in Medicine & Biology Society (EMBC) 2020, Montreal, Canada

A real-time monitoring system controller for medical tissue engineering bioreactors
C. Leibold, M. Wahalla, C. Blume, H. Blume and M. Wilhelmi
IEEE International Conference on Consumer Electronics (ICCE) 2015, Las Vegas, USA

Journal Publications

Blue light-induced protein expression of active BDNF in human cells using the optogenetic CRY2/CIB system
S. Christoffers, N. Wichert, E. Wiebe, M. L. Torres-Mapa, M. Goblet, M.-N. Wahalla, H. Blume, A. Heisterkamp, A. Warnecke, C. Blume.
ACS Synthetic Biology 2023, Status: submitted

Mobile SARS-CoV-2 screening facilities for rapid deployment and university-based diagnostic laboratory
N. Stanislawski, F. Lange, C. Fahnemann, C. Riggers, M.-N. Wahalla, M. Porr, F. Cholewa, R. Jonczyk, S. Thoms, M. Witt, F. Stahl, S. Beutel, A. Winkel, P.-C. Pott, M. Stiesch, M. Paulsen, A. Melk, H. Lucas, S. Heiden, H. Blume, C. Blume
Engineering in Life Sciences 2023, Journal volume 23, Issue 2

An intelligent bioreactor system for the cultivation of a bioartificial vascular graft
P. Maschhoff, S. Heene, A. Lavrentieva, T. Hentrop, C. Leibold, M.-N. Wahalla, N. Stanislawski, H. Blume, T. Scheper, C. Blume
Engineering in Life Sciences 2017, Journal volume 17, Issue 5

Other Scientific Contributions

Online EEG-Signal Processing within the CereBridge mobile Brain-Computer Interface system
M.-N. Wahalla
Hearing4all Cluster of Excellence Symposium 2023, Oldenburg, Invitational highlight talk

Framework for Live Recording and Algorithmic Evaluation of Ear-EEG on an FPGA-based Mobile Brain-Computer Interface Platform
M.-N. Wahalla, H. Blume
55th DGBMT Annual Conference on Biomedical Engineering 2021, Hanover, Germany

An Efficient, FPGA-based Real-Time Processing Platform for True Mobile Brain-Computer Interfaces
M.-N. Wahalla
Hearing4all Cluster of Excellence Symposium 2020, Online, Invitational highlight talk