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Efficiency modeling for MHz DCDC converters at 40 V input voltage range

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Abstract. Size and cost of a switched mode power supply can be reduced by increasing the switching frequency. This leads especially at a high input voltage to a decreasing efficiency caused by switching losses. Conventional calculations are not suitable to predict the efficiency as parasitic capacitances have a significant loss contribution. This paper presents an analytical efficiency model which considers parasitic capacitances separately and calculates the power loss contribution of each capacitance to any resistive element. The proposed model is utilized for efficiency optimization of converters with switching frequencies > 10 MHz and input voltages up to 40 V. For experimental evaluation a DCDC converter was manufactured in a 180 nm HV BiCMOS technology. The model matches a transistor level simulation and measurement results with an accuracy better than 3.5 %. The accuracy of the parasitic capacitances of the high voltage transistor determines the overall accuracy of the efficiency model. Experimental capacitor measurements can be fed into the model. Based on the model, different architectures have been studied.

1 Introduction

Switched mode power supplies can achieve high efficiency in power management systems but require passive filter elements like inductors, transformers and capacitors which mainly dominate the system size and thus the costs. Especially at low power, high volume applications up to 10 W a high degree of integration is important. This can be achieved by increasing the switching frequency as this scales down the passive components. In many cases, this also has a positive effect on reliability as it relaxes the requirements on assembly and interconnect technology. Today, power supplies with a switching frequency up to 2 MHz are common, but the passive components remain dominant. With a further increase of the frequency, the switching losses significantly reduce the efficiency of the regulator. For low input voltages of less than 10 V, the efficiency still remains acceptable. However, many applications require an efficient power supply with an input voltage range up to 100 V. Higher input voltages significantly impacts the switching losses. Such high-voltage applications include growth areas like energy conversion from renewables. Moreover, in cars the battery voltage can go up to > 40 V. In e-mobility systems, the medium board net voltage is defined to be 48 V.

To analyze the efficiency of converter architectures for high switching frequencies and high input voltage range, standard efficiency calculations turn out to be insufficient because the influence of parasitic capacitances becomes dominant, but it is modeled poorly and it is not possible to extract the root causes of the losses. As proposed by Wang et al. (2010), Wang and Huang (2011), the losses caused by parasitic capacitances in all current paths need to be considered. This approach is extended in this paper. This way, both critical loss contributions (root causes) and loss elements (locations) in an architecture can be obtained. The losses are calculated for each switching phase separately. There are two main benefits of the proposed model: (1) design parameters, e.g. the on-state resistance, can be optimized for a given architecture, (2) various converter architectures can be studied and compared in terms of efficiency by comparing the particular circuit elements. The focus in this paper is on a supply up to 40 V, 10 MHz and $V_{\text{out}} = 5$ V. The proposed methodology is suitable also for circuits operating at higher input voltages and higher frequencies as long as parameters, such as the parasitic capacitances, can be provided precisely enough.

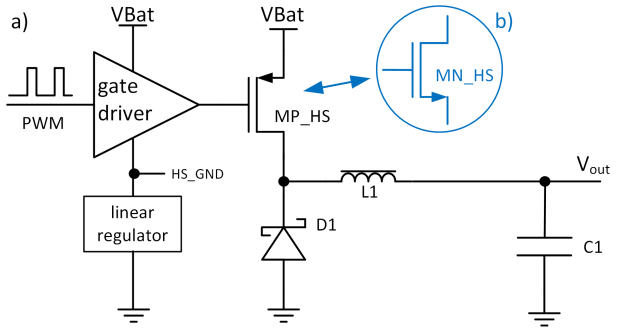

Figure 1. Overview of a buck converter in various architectures. **(a)** with PMOS high side switch; **(b)** with NMOS high side switch.

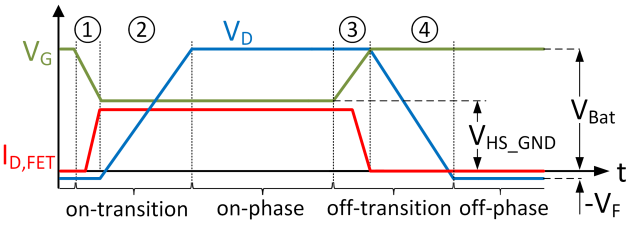

Figure 2. Separation of the switching transients into four phases.

The model has been developed in first place for an asynchronous buck converter architecture with a PMOS high side power FET as shown in Fig. 1a. The regulation circuit of the converter creates a pulse width modulated signal (PWM) which controls the input to output voltage ratio by regulating the duty cycle Wittmann and Wicht (in press). To fully open the PMOS FET MP_HS during the on-phase, the gate driver is connected between the supply voltage V_{Bat} and the HS_GND rail. A linear regulator regulates the HS_GND to $(V_{\mathrm{Bat}} - 5\,\mathrm{V})$.

The PMOS high side switch can be replaced by an NMOS high side switch (Fig. 1b) which requires a boot strapping circuit to generate the gate overdrive. The HS_GND for the NMOS switch is typically connected to the source of the NMOS switch.

The efficiency model for the buck converter is derived in Sect. 2. A discussion of the efficiency results and the loss elements including an architecture comparison is given in Sect. 3.

2 Efficiency model

To allow a separation of the power losses for each element of the converter, all current paths during the switching transients have to be analyzed. The charge or discharge of a parasitic capacitance in a switching phase contributes to the losses in each resistive element along the current path. Figure 2 shows the idealized drain current $I_{\mathrm{D,FET}}$, the gate voltage V_{G} and the drain voltage V_{D} of the PMOS power FET over one switching period. In order to obtain a single charge or discharge event for each capacitance per phase, the switching transitions are separated into four phases. A very fast gate driver is assumed and thus the rise at the drain voltage until the gate is fully charged and discharged, respecively, is not significant Wittmann and Wicht (in press)Wittmann et al. (2012).

Figure 3 shows the current paths which have been derived for each switching phase. In phase 1 and phase 3, the gate is discharged and charged, respectively, to turn on and off the power FET. The capacitances C_{SG} and C_{GD} are charged and discharged by the gate voltage change ΔV_{G}. In phases 2 and 4, the drain voltage sees a swing of approximately V_{Bat}. In these phases, the parasitic capacitances in the power FET C_{GD} and C_{DB} (C_{DS} included in $=$ DB for simplification) and the junction capacitance of the Schottky diode are charged and discharged. The gate driver is designed strong enough such that the miller-plateaus in phases 2 and 4 are not significant.

The modeling approach will be demonstrated below for the discharge of C_{GD} by ΔV_{G} during phase 1 (Fig. 3a). The charge ΔQ_{CGD} on C_{GD} also flows through the gate driver's low side and through the linear regulator to ground on one side and through the Schottky diode (I_{DIO}) on the other terminal of C_{GD}. During discharge, the voltage at the gate driver output falls from 5 V to 0 V while the high side ground voltage is constant at $V_{\mathrm{HS\_GND}} = V_{\mathrm{Bat}} - 5\,\mathrm{V}$. The charge $\Delta Q_{\mathrm{CGD}} = \Delta V_{\mathrm{G}} \cdot C_{\mathrm{GD}}$ thus creates the energy loss $w_{\mathrm{lr}} = \Delta Q_{\mathrm{CGD}} \cdot V_{\mathrm{HS\_GND}}$ in the linear regulator when the charge is discharged to ground. The energy loss in the gate driver is $w_{\mathrm{driver}} = 0.5 \cdot \Delta Q_{\mathrm{CGD}} \cdot \Delta V_{\mathrm{G}}$ and in the Schottky diode $w_{\mathrm{d}} = \Delta Q_{\mathrm{CGD}} \cdot V_{\mathrm{F}}$ with forward voltage V_{F}.

These calculations can be done for all capacitances in all phases to obtain the loss contributions of all parasitic capacitances for each circuit element. This is summarized in Table 1, which shows the root causes and locations of the losses in all phases during a switching period. By summing up the losses per line, the loss contributions to the particular resistive elements (i.e. loss location) can be determined. Respectively, the columns yield the losses caused by each capacitance per phase. If a parasitic capacitance is discharged through the inductor $L1$ (e.g. $C_{\mathrm{J}}, C_{\mathrm{GD}}, C_{\mathrm{DB}}$ in phase 4) to the output, no losses occur, since the energy is stored in the inductor or can be used as output current. The losses caused by the parasitic capacitances are time invariant and occur once in a switching period. The according power dissipation thus increases linearly with the switching frequency.

In the turn-on transition phase (Fig. 2), the transition losses are calculated in the conventional way by $P_{\mathrm{SWon}} = 0.5 \cdot I_{T\mathrm{begin}} \cdot (V_{\mathrm{Bat}} + V_{\mathrm{F}}) \cdot t_{\mathrm{SWon}} \cdot f_{\mathrm{sw}}$ with the assumption that the drain voltage decreases linearly. t_{SWon} is the duration of the transition phase (see phase 2 in Fig. 2) and $I_{T\mathrm{begin}}$ the source-drain current through the transistor at the beginning of phase 2. The analytical calculation of the transition time t_{SWon} is usually not suitable, as it depends on various

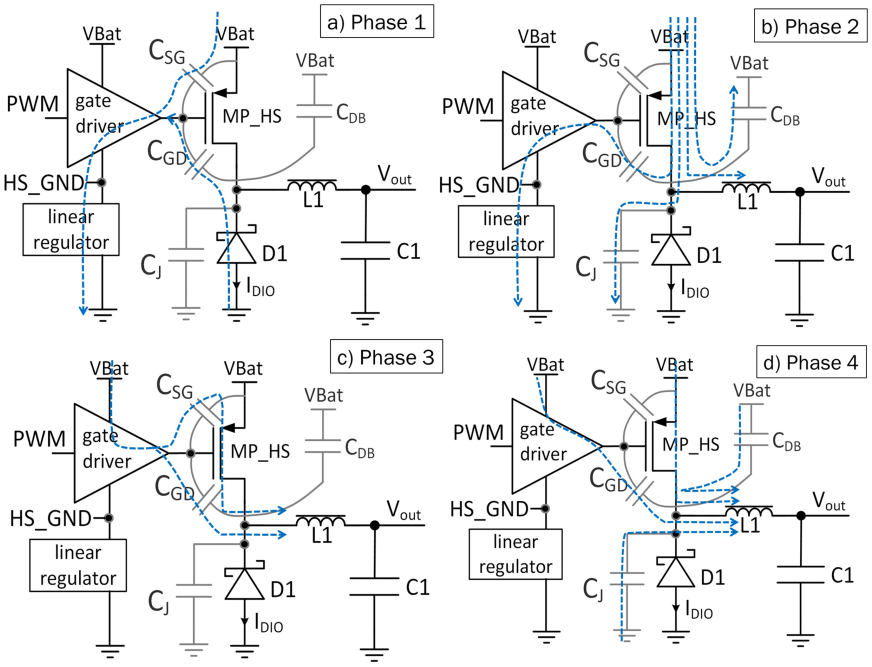

Figure 3. Current paths in a converter with PMOS switch.

Table 1. Location and root causes of losses due to parasitic capacitances in the FET and the Schottky Diode.

Loss location	Loss cause			
	Phase 1	Phase 2	Phase 3	Phase 4
Gate driver pull-down path	C_{GD}, C_{SG}			
Gate driver pull-up path			C_{DG}, C_{SG}	
Linear regulator	C_{GD}, C_{SG}	C_{GD}		
Schottky diode	C_{GD}			
FET R_{DSon}		C_{GD}, C_{DB}, C_J Transition losses, static losses		

parameters including the R_{DSon} transition, the level of the miller plateau and the stability of the HS_GND. Therefore it is appropriate to take t_{SWon} from transistor level simulation or experimental measurement. For the architecture comparison, t_{SWon} was taken from the transistor level simulation. Measurements show that t_{SWon} is roughly independent of the load current I_{out}. Additional losses due to reverse recovery are extracted in a transistor level simulation and scaled with the output current in the efficiency model.

During the turn-off transition phase (see phase 4 in Fig. 2), no losses occur as the load current is fully provided by the discharge current of the parasitic capacitances. The losses caused by the output current in the FET during the charging of the gate in phases 1 and 3 are negligible due to the fast discharge time with a strong gate driver. The static losses in the on-phase and off-phase occur when the power FET is fully turned on during the time t_{on} and fully turned off during the time t_{off}. During the on-phase, the power loss is determined by the average output current I_{out} and the on-state resistance R_{DSon} and thus is $P_{on} = R_{DSon} \cdot I_{out}^2 \cdot t_{on} \cdot f_{sw}$. During t_{off} the current flows through the forward conducting Schottky diode and the power loss is $P_{on} = V_F \cdot I_{out} \cdot t_{off} \cdot f_{sw}$. The losses due to reverse recovery in the Schottky Diode can be neglected.

3 Results and circuit architecture comparison

To verify the efficiency model, an asynchronous buck converter with a DEMOS p-channel HS FET was implemented in a 180 nm high-voltage BiCMOS technology. Figure 4 shows a comparison of the simulated total efficiency at $V_{Bat} = 18\,V$ (traces a) and c) in Fig. 4) and $V_{Bat} = 40\,V$ traces (b) and d) in Fig. 4) over the switching frequency. The traces a) to d) show a very good matching between the transistor level simulation and the efficiency model. Trace e) shows the efficiency from a real measurements at the same operation point as the simulation in a). The deviation between

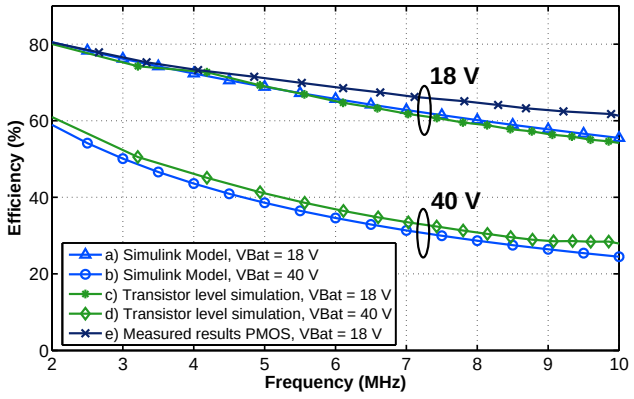

Figure 4. Efficiency comparison of circuit simulation, model and measured results over frequency at $V_{\mathrm{Bat}} = 18\,\mathrm{V}$, $40\,\mathrm{V}$ and $I_{\mathrm{out}} = 200\,\mathrm{mA}$ (right).

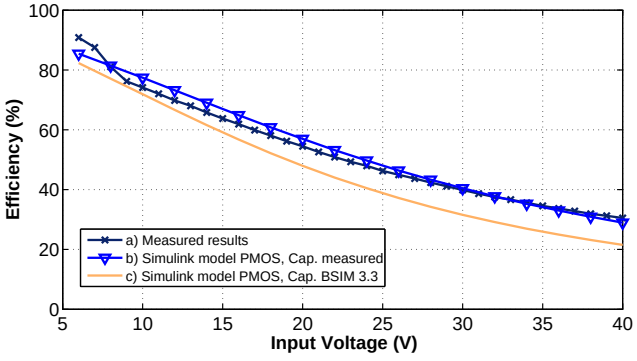

Figure 5. Efficiency comparison of model and measured results with parasitic capacitance extraction from the BSIM 3.3 model and measured capacitance extraction over input voltage at $f = 10\,\mathrm{MHz}$ and $I_{\mathrm{out}} = 200\,\mathrm{mA}$.

the curves appears mostly due to the known limited accuracy in the modeling of parasitic capacitances of high voltage transistors in the BSIM 3.3 model. This will be addressed by more advanced models like HiSIM-HV in future Mattausch et al. (2010). To provide more accurate capacitance values to the efficiency model, the values of the parasitic capacitances were measured in the according operation regions of the FET (saturation, triode and cutoff) with a gate charge and output charge measurement. Figure 5 shows that the measured capacitances improve the accuracy of the efficiency simulation compared to the measured efficiency.

The results of a frequency simulation of the efficiency model of the asynchronous buck converter with a high side PMOS FET are shown in Fig. 6 for operating conditions of $V_{\mathrm{Bat}} = 40\,\mathrm{V}$, $I_{\mathrm{out}} = 200\,\mathrm{mA}$. The power FET was optimized by an efficiency simulation over the on-state resistance. The size of the FET resulted to be optimum at $R_{DSon} = 1.4\Omega$. All relevant loss causes of the particular elements are plotted over the frequency in Fig. 6a while the loss locations, i.e. the resistive elements in which the losses are dissipated,

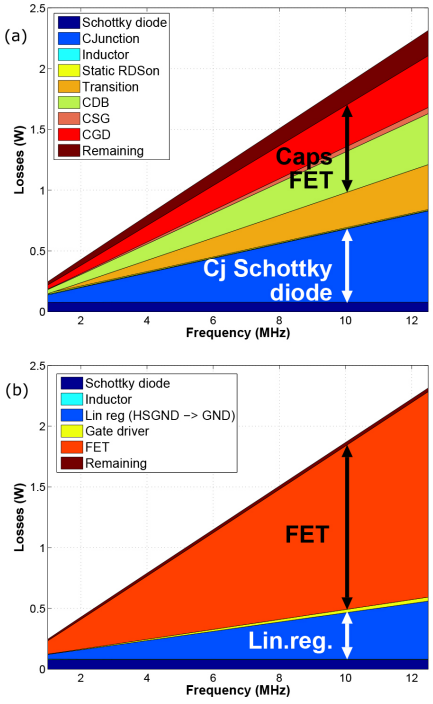

Figure 6. (a) Loss causes and **(b)** loss locations of an asynchronous buck converter with PMOS high side switch ($V_{\mathrm{Bat}} = 40\,\mathrm{V}$, $I_{\mathrm{out}} = 200\,\mathrm{mA}$, $R_{\mathrm{DSon}} = 1.4\Omega$).

are shown in Fig. 6b. The loss causes labeled "Remaining" in Fig. 3 mainly include the losses caused by the first five stages of the six stage gate driver and its current flowing through the HS_GND regulator. The capacitances of the PMOS FET cause losses, which are in the range of the losses caused by the capacitance of the Schottky diode. At higher frequencies, the losses caused by the capacitances C_{GD} and C_{DB} and the transition losses in the FET are becoming dominant, while in the Schottky diode, the losses caused by its junction capacitance become superior compared to the forward losses. Analyzing the loss locations in Fig. 6b, it can be seen that most of the losses caused by parasitic capacitances are occurring in the resistive channel of the FET. These results lead to the assumption that the efficiency can be significantly increased by using an NMOS power FET, which has either a smaller on-resistance compared to a PMOS FET with the same size, or the parasitic capacitance can be reduced with a smaller transistor size keeping the on-resistance equal.

An architecture comparison is done by replacing the PMOS FET by an NMOS FET of half the size (see Fig. 1b) with an on-state resistance of $R_{\mathrm{DSon}} = 0.8\Omega$. For a good model accuracy, the R_{DSon} and the parasitic capacitances of an implemented LDMOS NMOS FET were measured and fed to the model, as described in Sect. 2. The simulation of the loss causes with NMOS FET at $f = 10\,\mathrm{MHz}$ over V_{in} is shown in Fig. 7, in this case as a function of the

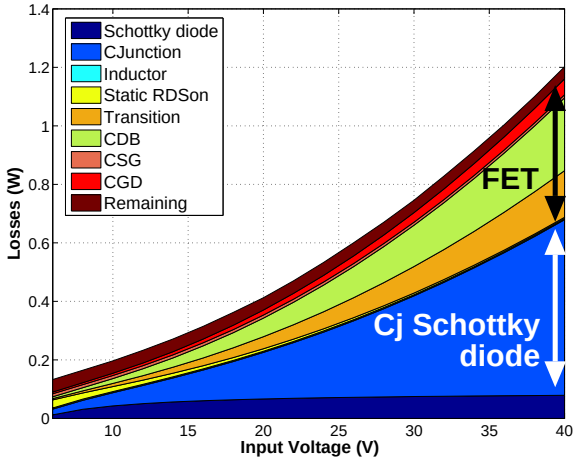

Figure 7. Loss causes of an asynchronous buck converter with NMOS high side switch over the input voltage V_{Bat} ($f_{\mathrm{sw}} = 10\,\mathrm{MHz}$, $I_{\mathrm{out}} = 200\,\mathrm{mA}$, $R_{DSon} = 0.8\Omega$).

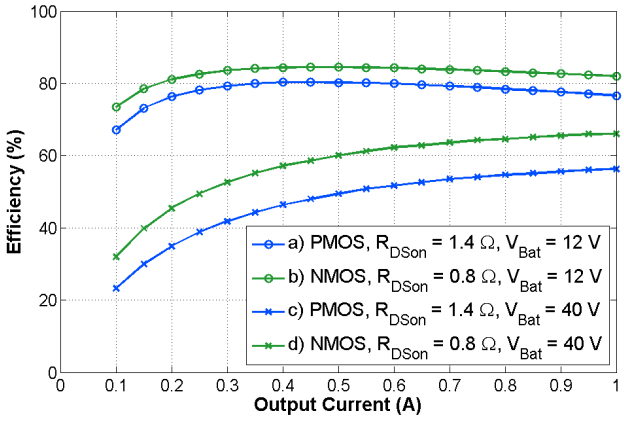

Figure 8. Comparison of the efficiency with PMOS and NMOS power FET over the output current I_{out} ($V_{\mathrm{Bat}} = 12\,\mathrm{V}, 40\,\mathrm{V}$, $f = 10\,\mathrm{MHz}$)

input supply voltage. The losses in the FET are significantly reduced. The current through the HS_GND contributes to the output current and, hence, the corresponding losses through the HS_GND regulator are eliminated. The transition losses are decreased due to lower R_{DSon}. The losses caused by the Schottky diode remain equal. The total losses are reduced by more than 30 % at $V_{\mathrm{Bat}} = 40\,\mathrm{V}$.

Figure 8 shows a comparison of the overall efficiency of the converter with a PMOS to an NMOS FET over the output current at a switching frequency of 10 MHz, $V_{\mathrm{Bat}} = 12\,\mathrm{V}$ and $V_{\mathrm{Bat}} = 40\,\mathrm{V}$. In all architectures, the efficiency first increases, since the output power increases more than the losses. With higher output current, the losses in the R_{DSon} get dominant at low input voltage. Due to the smaller ratio of R_{DSon} to the parasitic capacitances, the NMOS high side FET leads in average to 6% higher efficiency (curves a) vs. b)) at $V_{\mathrm{in}} = 12\,\mathrm{V}$ and to a 10 % higher efficiency (curves c) vs. d)) at $V_{\mathrm{in}} = 40\,\mathrm{V}$ compared to a PMOS FET.

4 Conclusions

By considering all parasitic capacitances and analyzing the current paths in the separate switching phases, the model is suitable to perform different efficiency analysis in a voltage range up to 40 V especially at high switching frequency. The possibility to extract all loss causes and locations separately allows to determine the critical elements. In particular, the model approach allows to (1) optimize design parameters for a given architecture, (2) to study and compare various converter architectures. To verify the model, an asynchronous buck converter with PMOS high side FET was manufactured. A model accuracy of around 3.5 % was achieved up to 10 MHz compared to measurements. It was demonstrated that the limited modeling accuracy of parasitic capacitances of high voltage transistors in the BSIM 3.3 can be circumvented by feeding measured capacitance values into the model.

A comparison based on the efficiency model was presented for an asynchronous buck converter switch resulting in a higher efficiency by using an NMOS high side switch. As a general conclusion, with higher frequency smaller FETs achieve a higher efficiency.

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