

# Analysis and Simulation of Reduced FIR Filters

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**Abstract.** High order FIR filters employ model reduction techniques, in order to decrease power consumption and time delay. During reduction high order FIR filters are converted into low order IIR filters preserving stability and phase linearity as main features. Matlab simulations of an audio system with these reduced filters are presented. Furthermore, the influence of order on power consumption is discussed.

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## 1 Introduction

In problem area like model order reduction several reduction methods have been developed in the last two decades. A classification of these methods can be given by referring to the domain where the high-order and low-order models have to be represented either in frequency or time domain. The most frequently employed model reduction methods for linear, stable, continuous- or discrete-time systems are the Balanced Truncation Model Reduction (Beliczynski et al., 1992) (BMT), Singular Perturbation Model Reduction (SPR) (Aldhaheri, 2000) and Optimal Hankel Norm Approximation (OHN) (Beliczynski et al., 1994). These methods operating in the state-space domain of the original model lead to the derivation of a low-order model with fewer state variables.

Our starting point for applying model reduction methods is a novel binary zero-position coding algorithm (ZePoC) (Streitenberger and Mathis, 2002a). This algorithm is developed to convert audio signals into binary signals eliminating high frequency distortions. Hardware implementation of ZePoC system includes FIR filters as main building blocks (Streitenberger et al., 2001), where phase linearity is essential. It is well known that phase linear FIR filters allow distortion free transmission of signals, and they are widely used due to advanced design tools. However, the main drawback of FIR filters is their high order. Model reduction techniques offer a solution for designing filters with low order preserving phase

linearity and stability (Prenbo and Silverman, 1982).

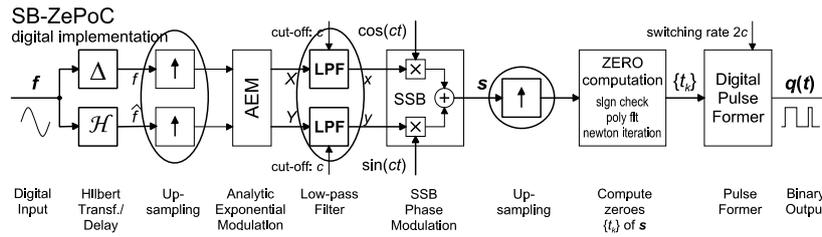
While model reduction techniques give IIR filters with lower order, their implementation may lead to problems of coefficients presentation. We will show that the coefficients of the reduced IIR filters can be represented by second-order sections and implemented with the same digital signal processor (DSP) with two's complement fix point arithmetic as in the case of the original FIR filters.

In addition, we are going to discuss the power consumption of the reduced filters. There are different approaches to this problem. One way is to reduce the amount of switched capacitance during its operation (Chandrakasan and Brodersen, 1995). Another way is to reduce filter hardware decreasing the number of its digital circuits. In this sense we observe correlation between reduction methods and the complexity of the reduced filter.

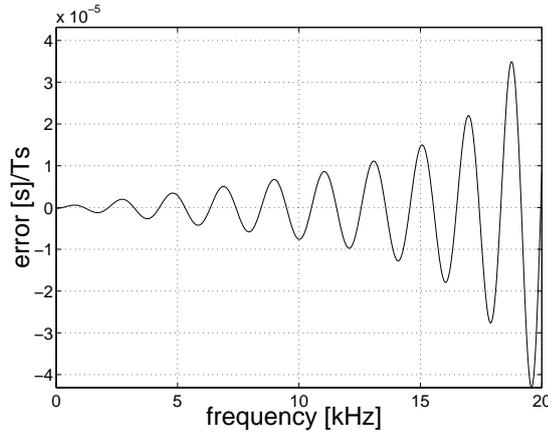
In our paper we will show in an implicit manner the influence of conventional model reduction methods to the power consumption. Furthermore we will show with Matlab simulations that these reduced IIR filters preserve the quality of audio signals of the ZePoC system with the original FIR filters, while power consumption is reduced.

## 2 Application of the model reduction techniques

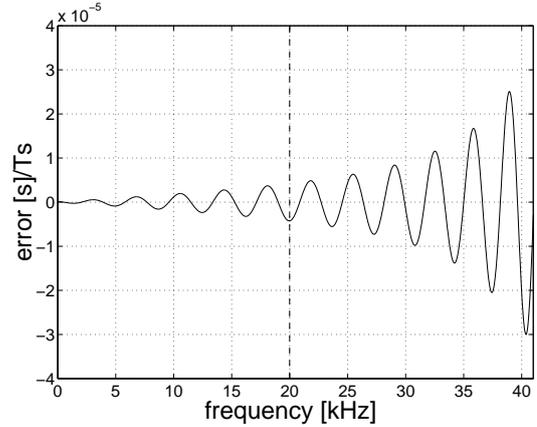
As already mentioned we are going to show applications of the model reduction techniques to a new type of coding algorithm for audio signals (ZePoC). The ZePoC system is presented in Fig. 1. In order to get the audio signal from the intermediate binary carrier signal, low pass digital FIR filters are needed for each channel of the two parts of the analytic signal, (Streitenberger et al., 2002b). Circles in Fig. 1 mark these filters. The stop band suppression and pass band ripple for all filters are  $-100$  dB and  $1.737 \cdot 10^{-4}$  dB respectively. The first two FIR filters, marked as an Up-sampling block, are digital 8-times up sampling filters. The order of each filter is 260. The LPF blocks present low pass FIR filters with the order 170. The sampling frequency  $f_s$  for these four



**Fig. 1.** Symbolic presentation of the ZePoC algorithm. All hardware elements with FIR filter structure are marked with circles.



**Fig. 2.** Group delay error of the 8-times up sampling IIR filters in pass band. Error is scaled by sampling rate  $T_s = 1/f_s$ ,  $f_s = 384$  kHz.



**Fig. 3.** Group delay error of the low pass IIR filters in pass band. Error is scaled by sampling rate  $T_s = 1/f_s$ ,  $f_s = 384$  kHz. The dashed line marks the highest input signal frequency, 20 kHz.

filters is  $f_s = 384$  kHz. The last up-sampling block is 4-times up-sampling FIR filter that carry out the signal processing algorithms including implicit zero-computation to an accuracy of 16 bits. The order of this filter is 34 with the sampling frequency  $f_s = 1536$  kHz.

For audio signals only the frequency range between [0, 20 kHz] is significant in the pass band of the filters.

Analysis of magnitude response error and group delay error in Radić and Mathis (2004a) for described filters showed that the best results were archived by SPR. This method is applicable to systems that can be heuristically decoupled into a slow subsystem and a fast one. Rejection of very fast modes from a model gives a new system consisting of a slow part that can be considered dominant for a description of the full behaviour.

All reduced filters obtained by SPR techniques are IIR filters with quasi-linear phase in pass band. We are going to discuss the size of ripple shape of group delay error of each reduced filter, because it shows the deviation of phase from exact linearity. Indeed, the group delay errors increase with frequency in pass band, as it is shown in Fig. 2, for 8-times up sampling filters that are reduced to order 34. For frequencies larger than 17 kHz this ripple reaches values larger than  $2 \cdot 10^{-5}$ . Therefore, the input signal with frequencies between 17 kHz and 20 kHz can be more interfered.

The LPFs are reduced to order 37 and have very small group delay error up to frequency 20 kHz, see Fig. 3. For the most critical frequencies, around 20 kHz, the ripple of the scaled group delay error is less than  $10^{-5}$  and has small influence on the input signals.

The last 4-times up sampling filter reduced to the order 15 has very small group delay error in pass band, particularly for the input signal range marked by dashed line in Fig. 4.

The magnitude response error for all filters is in the pass band smaller than  $-150$  dB, so that the error is imperceptible for audio signals (Radić and Mathis, 2004b).

### 3 Power consumption of the reduced filter

In the following, we are going to study the connection between the complexity of a filter structure and its power consumption. Since power consumption is proportional to the filter order (Ludwig et al., 1996), our approach achieves power reduction with respect to a filter order reduction. The filter order and the number of key components/operation can be identified from filter transfer functions. If we consider the complete DSP architecture it consist of a multiply accumulator, several forms of memory (RAM, ROM), a storage cell for the filter output value and a control function for scheduling

the different components. The average power consumption,  $P$ , of a digital system may be expressed as

$$P = \sum_i N_i C_i V_{dd}^2 f_s, \quad (1)$$

where  $N_i$  is the number of operations of type  $i$  performed per sample,  $C_i$  is the average capacitance switched per operation of type  $i$ ,  $V_{dd}$  is the operation supply voltage and  $f_s$  is the sample frequency (Erdogan et al., 2001). Therefore, for achieving low-order it has to be minimised one or more of the parameters  $N_i$ ,  $C_i$ ,  $V_{dd}$  and  $f_s$ . In this paper we analyze the power consumption of a reduced filter through the number of operations,  $N_i$ , like multiplying and adding, because they are directly impacted by reduction of filter order.

The number of multipliers and adders is related to the selected filter presentation and each of them needs some energy  $E_M$  and  $E_A$  respectively. Therefore the power consumption can be presented as a function of these two energies

$$P = F(N_M E_M, N_A E_A). \quad (2)$$

$N_M$  and  $N_A$  are numbers of multiplying and adding operations, respectively. We are not going to discuss the nature of the function  $F$  but the influence of the order reduction on  $N_M$  and  $N_A$ .

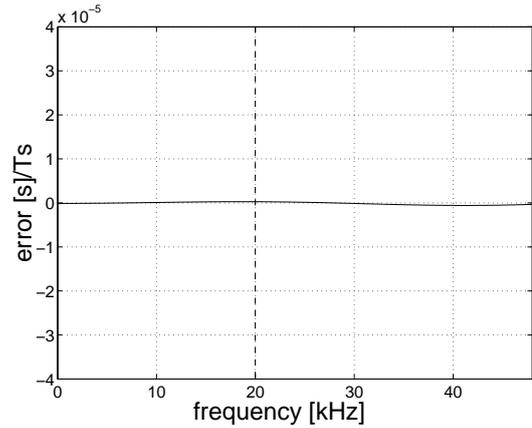
The multipliers are one of the major bottlenecks governing the performance of a DSP algorithm. Indeed, the power dissipated within a multiplier represents a significant proportion of the overall power dissipated by the DSP device (Abu-Khater et al., 1996). Furthermore we will consider and influence of the number of adders because their number depends on size of reduction.

### 3.1 Relations between order reduction and power consumption of the reduced filter

In this section we investigate the influence of model reduction to the complexity of the reduced filters and to compare the power consumption of the reduced IIR filter with the original FIR filters. First we are going to discuss the complexity and power consumption of the original linear phase  $N_{FIR}$ th order FIR filters. These FIR filters have a symmetric or antisymmetric impulse response, so that  $\lfloor N_{FIR}/2 \rfloor$  two-input multipliers are required. “ $\lfloor \cdot \rfloor$ ” stands for odd  $N_{FIR}/2$  rounded to the nearest larger integer. The number of two-input adders is equal to the order of such a filter. Therefore, the power consumption of an FIR filter according to Eq. (2) is

$$P_{FIR} = F\left(\frac{N_{FIR}}{2} |E_M, N_{FIR} E_A\right). \quad (3)$$

It is well known that the parallel structure has problems with finite word length representations (Vaidyanathan, 1993). Due to infinite word length requirements we will not discuss parallel structure as a possible solution for the representation of the reduced filters. Further, a filter represented by DF is implemented such that for each multiplication both inputs of the multiplier receive new data. This causes higher level



**Fig. 4.** Group delay error of the 4-times up sampling IIR filter in pass band. Error is scaled by sampling frequency  $T_s=1/f_s$ ,  $f_s=1536$  kHz. The dashed line marks the highest input signal frequency, 20 kHz.

of switching activity within the multiplier leading to higher power consumption (Arslan and Erdogan, 2002). The other two interesting structures TDF and SOS will be discussed, because of their low complexity (Tietze and Schenk, 1986), which may lead to low power consumption.

The TDF of an  $N_{IIR}$ th order IIR filter is characterized by  $2N_{IIR}-1$  unique coefficients and employs  $2N_{IIR}+1$  two-input multipliers and  $2N_{IIR}$  two-input adders. In this filter representation delay units are placed between adders so that the multipliers can be feed simultaneously. It results in a reduction of the switching activity of the multiplier data inputs since the data input remains unchanged for a significant number of multiplication operations.

Comparing the number of multipliers for a linear phase FIR filter and its associated reduced IIR filter, the degree of reduction for which a number of multipliers for TDF is lower than for original filter, can be calculated using the relation

$$pN_{FIR} = N_{IIR} \quad (4)$$

in the expression where the numbers of multipliers is compared

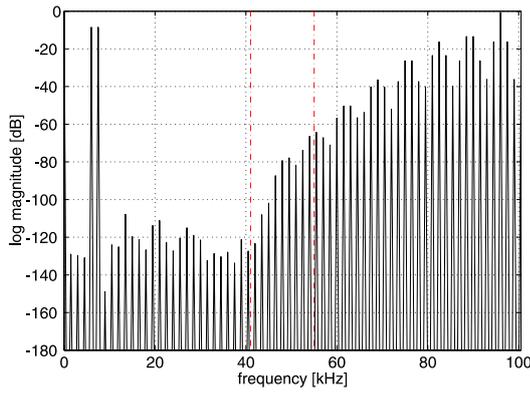
$$2pN_{FIR} + 1 \leq \frac{N_{FIR}}{2}, \quad (5)$$

The coefficient  $p$  indicates the degree of reduction. If we assume that  $1/2N_{FIR} \ll 1/4$  then  $p \approx 25\%$ . The FIR filter has to be reduced by more than 75% to verify a lower number of multipliers for the reduced IIR filter.

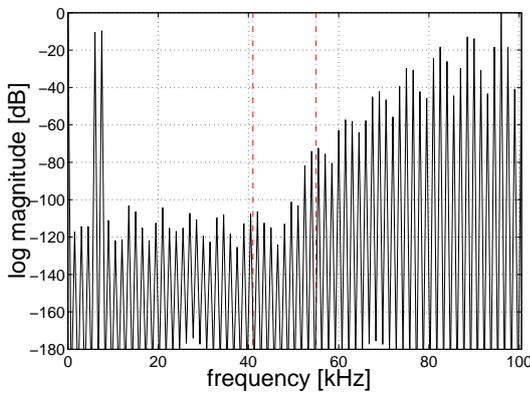
In the following the power consumption of the reduced filter presented by SOS can be presented as

$$P_{IIR}^{SOS} = F\left(\frac{N_{IIR}}{2} |5E_M, \frac{N_{IIR}}{2} |E_{A_5}\right), \quad (6)$$

where  $E_{A_5}$  is energy of five-input adder. The number of adders is lower for second order section than for FIR filter representations because  $N_{IIR} \ll N_{FIR}$ . But the number of



**Fig. 5.** Spectrum of output signal of ZePoC system with FIR filters, where signal contains  $f_1=6$  kHz and  $f_2=7.5$  kHz frequencies.



**Fig. 6.** Spectrum of output signal of ZePoC system with IIR filters, where signal contains  $f_1=6$  kHz and  $f_2=7.5$  kHz frequencies.

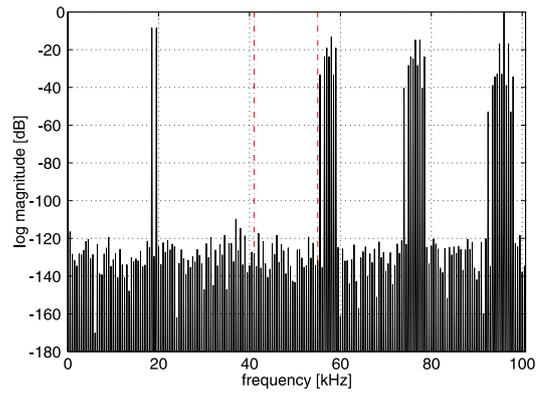
multipliers of SOS is not necessarily lower for each reduced IIR filter than for the original FIR filter. If the order of an IIR filter is presented as percentage  $p$  of the order of an FIR filter we can calculate value of the constant  $p$  as

$$\left| \frac{pN_{FIR}}{2} \right| \leq \left| \frac{N_{FIR}}{2} \right|. \quad (7)$$

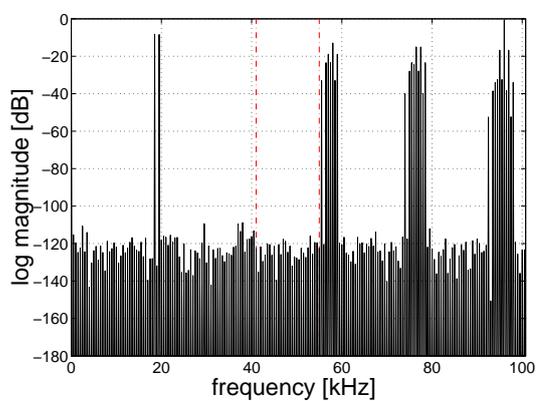
From Eq. (7)  $p$  has to be equal or smaller than 20%. According to Eq. (4) the FIR filters have to be reduced at least by 80%, so that the second order section presentation of reduced IIR filter requires less number of multipliers.

#### 4 Simulation of the ZePoC system with reduced low pass IIR Filters

The representation of data and coefficients in DSPs plays also very important role in reducing power consumption of the filters. There are two common methods of their representation two's complement and sign-magnitude representation (?). We decided to use the same 24 bits DSP and to represent the coefficients of reduced filters in two's complement, because the two's complement was used for representation of the original FIR filters coefficients.



**Fig. 7.** Spectrum of output signal of ZePoC system with FIR filters. The signal contains  $f_1=18.5$  kHz and  $f_2=19.5$  kHz frequencies.



**Fig. 8.** Spectrum of output signal of ZePoC system with the low pass IIR filters instead of the FIR filters. The signal contains  $f_1=18.5$  kHz and  $f_2=19.5$  kHz frequencies.

Here two different output signals from the reduced ZePoC system are presented and compared with output signals of the original ZePoC system. The reduced system contains the reduced IIR filters represented in the SOS because using TDF four of five filters from ZePoC system lost their coefficients during implementation.

We will observe and compare two different input signals. First observed input signal consists of a two-component sinusoidal signal with frequencies 6 kHz and 7.5 kHz. The output signal from the ZePoC system with linear phase FIR filters is presented in Fig. 5. Figure 6 shows the output signal if all filters in the original ZePoC system are replaced by low pass quasi-linear phase IIR filters. As one can see these two output signals are so similar that there is no difference in using quasi-linear phase IIR filters instead of linear phase FIR filters. The reason lays in very small group delay errors in the frequency range where audio signal appears for all reduced IIR filters, Figs. 2, 3 and 4. Furthermore, pass band noise is smaller than  $-100$  dB, and all high frequency distortions are in stop band that extends after second vertical dashed line in Fig. 6.

The second tested input signal is a two-component sinus signal with frequencies 18.5 kHz and 19.5 kHz. In Fig. 7 the

output signal from ZePoC system with FIR filters is given. The linear phase FIR filters allow easily distinguishing of the audio signal from noise and high frequency distortions. However, the output signal from the ZePoC system with quasi-linear phase IIR filters is also clearly divided from all kind of noises, see Fig. 8. Therefore, quasi-linear phase IIR filters can be used instead of linear phase FIR filters.

## 5 Conclusions

In this paper we have demonstrated the implementation of a reduced linear time invariant system from aspect of complexity and the power consumption. First, we presented order reduction of coding algorithm for digital class D audio amplifier (ZePoC) through reduction of its FIR filters as main building blocks. Model reduction techniques applicable to linear systems give reduced IIR filters with quasi-linear phase. Stability and all characteristics of original FIR filters are maintained in the reduced IIR filters.

The main emphasis was the power consumption, which is assumed to be a function of input signals wordlengths and the energy per logical circuit. The discussed reduction techniques decrease the number of logical circuits, while increasing the wordlength for some forms as transposed direct and parallel form. Analyzing power consumption of the reduced filter second order section appeared as the best structure for reduced filters. This structure demands finite wordlength for coefficients presentation and does not lead to numerical problems. Realization of the reduced IIR filters, as SOS needs less number of bits per quantized coefficient than realization of FIR filters. However, SOS of reduced IIR filter requires more multipliers. The number of multipliers in SOS is correlated with the degree of reduction. We showed that for filters, where the filter order can be reduced more than 80% fewer multipliers per section are necessary for SOS.

Simulations of the ZePoC system with reduced filters showed that the original FIR filters are replaceable by IIR filters with quasi-linear phase allowing distortion free transmission of signals.

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