Design and Control of a Multiphase Interleaving DC-DC Converter with Loss Optimizing Operating Strategies for Electric Vehicle

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M.Sc. Rashidreza Karimi

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1. Referent Univ.-Prof. Dr.-Ing. Axel Mertens
2. Referent Univ.-Prof. Dr.-Ing. Volker Staudt
3. Referent Univ.-Prof. Dr.-Ing. Bernd Ponick

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Nomenclature

General Definitions

$\hat{A}$	Peak value
$\hat{a}$	Estimated value
$\overline{a}$	Average value
$\underline{a}$	Complex value
$\vec{a}$	Vector value
$\widetilde{a}$	Amplitude
A	Effective value
a	Time dependent quantity
a'	Reflected value to the primary
a_{n}	n_{th} harmonic

Latin Letters

$\mathcal{F}$	Magnetomotive force (MMF)
A	Area
A_{c}	Area of the magnetic core cross section
A_{L}	Inductance factor
a_{st}	First Steinmetz constant
B	Magnetic flux density
b_{st}	Second Steinmetz constant
C_{d}	Capacitor inherent dielectric absorption
c_{d}	Drag coefficient of the vehicle
C_{R}	Ideal capacitance of the DC-Link
c_{r}	Rolling resistance coefficient
c_{st}	Third Steinmetz constant
$C_{\mathrm{th,x-y}}$	Thermal capacitance between x and y

D	Displacement current density
d	Diameter
D_{inn}	Core inner diameter
d_{L}	Duty cycle of the DC-DC converter phase
D_{out}	Core outer diameter
$e_{\mathrm{ctrl,u}}$	Voltage controller error
f	Frequency
F_{CF}	Frequency correction factor
G_{m}	Gear ratio between the wheel and motor
H	Magnetic field force
h_{core}	Core height
i	Current
I_{RRM}	Peak value of the reverse recovery current
j	Current density
J_{R}	Rotor moment of inertia
K_{N}	Gain of a given controlled plant
K_{P}	Gain (proportional part) of a PI-controller
L	Inductance
l	Length
$L_{\mathrm{C,ES}}$	Capacitor equivalent series inductance
L_{m}	Magnetizing inductance of the induction machine
$L_{\mathrm{s}\sigma}$	Leakage inductance of stator windings
L_{S}	Inductance of the electrodes and supply lines of a capacitor
$L'_{\mathrm{r}\sigma}$	Leakage inductance of rotor windings reflected to stator
L'_{r}	Total inductance of rotor windings reflected to stator
M	Modulation index
m	Mass
N	Number of winding turns
n_{mech}	Motor mechanical rotation speed
N_{ph}	Number of active phases in DC-DC converter
P	Power
p	Number of pole pairs in electric machine
Pv	Power loss per unit volume
Q_{RR}	Reverse recovery charge
$R_{\mathrm{C,ES}}$	Capacitor equivalent series resistance

R_{ch}	Resistance of the MOSFET channel
R_{d}	Dielectric resistance of the capacitor
R_{epi}	Resistance of the MOSFET drift region
R_{G}	Gate resistance
R_{i}	Leakage resistance of the capacitor
R_{n^+}	Resistance of the MOSFET source layer
R_{sub}	Resistance of the MOSFET substrate
R_{S}	Lead and junction resistance of a capacitor
$R_{\mathrm{th,x-y}}$	Thermal resistance between x and y
s	Complex frequency in Laplace transformation
s	Slip in induction machine
t	Time
T_{dead}	Actuator dead-time
T_{e}	Motor electric torque
T_{I}	Integral time constant of a PI-controller
T_{N}	Time constant of a given controlled plant
T_{r}	Electric time constant of rotor
T_{s}	Electric time constant of stator
u	Voltage
$U_{0,\mathrm{CE}}$	Forward voltage drop of the IGBT at no load
U_{block}	Blocking voltage
U_{BR}	Breakdown voltage
u_{c}	Control voltage
u_{F}	Diode forward voltage
$U_{\mathrm{GS,th}}$	Gate-source threshold voltage of transistor
U_{G}	Gate voltage
u_{i}	Voltage difference between phase i and motor star point
U_{ref}	Reference voltage
u'_{i}	Voltage difference between phase i and DC-Link middle point
V	Volume
v	Speed
W	Energy
X	Reactance
$Z_{\mathrm{th,x-y}}$	Thermal impedance between x and y

Greek Letters

α_{cu}	Temperature coefficient of the copper
α_s	Duty cycle of the inverter stator voltage
δ	Skin depth of a conductor
ε_0	Electric field constant
η	Efficiency in percentage
μ_0	Magnetic field constant
μ_{eff}	Effective permeability
μ_r	Relative permeability
ω	Angular frequency
ω_m	Mechanical angular speed of the rotor
ω_{res}	Angular frequency of the DC-Link capacitor at resonance
ω_r	Electrical angular frequency of the rotor magnetic field
ω_s	Electrical angular frequency of the stator magnetic field
ϕ	Magnetic flux
ϕ_{lag}	Carrier signal phase lag of the interleaving pulse generator
Ψ	Magnetic linkage flux
ρ	Density
σ	Specific Conductivity
σ_{cu}	Specific conductivity of the copper
σ_{eq}	Equivalent leakage coefficient of the induction machine
σ_r	The ratio of the rotor leakage inductance to the magnetizing inductance
σ_s	The ratio of the stator leakage inductance to the magnetizing inductance
θ	Temperature
ζ	Winding factor
$tan\delta$	Dissipation factor of the capacitor

Indices

Ab	Ambient
ac	Transient
acc	Acceleration
act	Actuator
ag	Air gap
air	Air

alt	Alternative drivetrain
asm	Asynchronous machine (induction machine)
avg	Average
bd	Breakdown
bs	Bit stream
C	Capacitor
c	Control
Ca	Case of a transistor
CE	Collector to emitter of an IGBT
con	DC-DC converter
cond	Conduction
cont	Continuous
core	Magnetic core
cross	Crossover frequency
cu	Copper
D	Diode
DC	DC-Link
dc	Steady-state
dev	Deviation
diel	Dielectric
DS	Drain to source of a MOSFET
ed	Eddy current
eff	Effective value
eq	Equivalent
est	Estimated
F	Fluid
GD	Gate to drain of a MOSFET
GE	Gate to emitter of an IGBT
GS	Gate to source of a MOSFET
Hs	Heat-sink
inv	DC-AC inverter
iss	Input capacitance of a MOSFET
J	Junction of a transistor
K	Maximum dominant harmonic order
L	Inductor

LL	Line to line
load	Load
loss	Losses
mag	Magnetic core
max	Maximum value
mg	Magnetizing part
MOS	MOSFET
n	Harmonic order
nom	Nominal value
norm	Normalized value
ohm	Ohmic
OP	Operating Point
oss	Output capacitance of a MOSFET
peak	Peak value
r	Rotor
RRM	Reverse Recovery Mode
rss	Reverse capacitance of a MOSFET
s	Stator
sin	Sinusoidal
ss	Small signal
sw	Switching
T	Transistor
V	Vehicle
W	Wheel
win	Winding
x	Arbitrary variable

Abbreviations

Al-Caps	Aluminum Electrolytic Capacitors
BJT	Bipolar junction transistor
COS	Coordinate system
DAB	Data Acquisition Board
DC-AC	DC-AC converter
DC-DC	DC-DC converter

Gm	Gain Margin
HEV	Hybrid Electric Vehicle
IGBT	Insulated Gate Bipolar Transistor
ISR	Interrupt Service Routine
JFET	Junction Field Effect Transistor
MAT	MATLAB
MLC-Caps	Multi-Layer Ceramic Capacitors
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPF-Caps	Metalized Polypropylene Film Capacitors
OL	Open-Loop
OS	Operating Strategy
PM	Passive Mode
Pm	Phase Margin
RMS	Root Mean Square
RRM	Reverse Recovery
Si	Power transistor with silicon technology
SiC	Power transistor with silicon carbide technology
SIM	SIMULINK
SPWM	Sinusoidal pulse width modulation
SSA	State-space average
SVM	Space vector modulation
ZCS	Zero-current switching
ZVS	Zero-voltage switching

Kurzfassung

In den letzten Jahrzehnten wurde die weit verbreitete Einführung von Fahrzeugen mit Verbrennungsmotor durch zwei bedeutende Herausforderungen beeinflusst, nämlich den schwankenden ölpreis, und den Klimawandel, der durch die Emissionen von Fahrzeugen mit fossilen Brennstoffen verursacht wird. Infolgedessen hat die Entwicklung leistungsfähiger Elektro- und Hybridelektrofahrzeuge in den letzten Jahren viel Aufmerksamkeit erregt und sich zu einem Trend entwickelt. Um dieses Ziel zu erreichen, sind Forschungsarbeiten zur Verbesserung der Elektrofahrzeuge in Bezug auf Kosten, Energieverbrauch, Gewicht und Zuverlässigkeit unerlässlich. Eines der wichtigsten Ziele bei der Entwicklung von Elektrofahrzeugen ist die Optimierung des elektrischen Antriebsstrangs auf maximale Effizienz, wobei ein wichtiger Faktor die maximale Reichweite pro Vollladung der Batterie ist (analog zu einer Vollbetankung in einem verbrennungsmotorischen Fahrzeug).

Die Komponenten des Antriebsstrangs von elektrischen Nutzfahrzeugen umfassen das Batteriepaket, den Wechselrichter und die elektrische Maschine. In einer solchen Antriebsstrangkonfiguration ist die Eingangsspannung des Wechselrichters (DC-Link Spanung) jedoch gleich der Batteriespannung, was einige Nachteile mit sich bringt. Erstens sind unterschiedliche Werte erforderlich, um das optimale Spannungsniveau während des Konstruktionsprozesses des Batteriestapels und der elektrischen Maschine zu erreichen. Zweitens wirkt sich der Ladezustand der Batterie negativ auf den Betriebsbereich der elektrischen Maschine aus. Wie in dieser Arbeit gezeigt wird, führt eine Verringerung der Zwischenkreisspannung außerdem zu geringeren Leistungsverlusten des Wechselrichters. In Betriebspunkten, in denen die erforderliche Maschinenspannung niedriger ist als der Nennwert der Batteriespannung, führt eine feste Zwischenkreisspannung in Höhe der Batteriespannung zu zusätzlichen Wechselrichterverlusten.

Der Schwerpunkt dieser Arbeit liegt auf dem Entwurf und der Analyse eines batterieelektrischen Fahrzeugantriebsstrangs mit einer zusätzlichen DC-DC Wandler Erweiterung in diesem. Dementsprechend besteht das Hauptziel darin, die Energieeffizienzvorteile zu untersuchen, die sich aus der Verschiebung der Betriebspunkte der Komponenten des Antriebsstrangs ergeben, indem ein Gleichstromwandler zwischen der Batterie und der umrichtergespeisten Maschine platziert wird. Zu diesem Zweck wird ein mehrphasiger Interleaving-Konverter ausgewählt, und durch eine umfassende Modellierung des Antriebsstrangs wird zum einen das geeignete Kontrollsystem entworfen und bewertet, und zum anderen werden verlustoptimierende Betriebsstrategien entwickelt, um den größten Nutzen aus der Integration eines Gleichstromkonverters in den Antriebsstrang zu ziehen. Im Rahmen der Forschungsarbeiten wird ein Prototyp eines mehrphasigen, interleaving DC-DC Wandlers gebaut, um die entwickelten Modelle und das Steuerungssystem unter verschiedenen Last- und Betriebsbedingungen zu verifizieren. Nach der

Dimensionierung zweier unterschiedlicher Antriebsstränge für ein Prototyp-Elektrofahrzeug mit 60 kW Maximalleistung werden im letzten Schritt die Energieverluste der Spannungswandler eines konventionellen Antriebsstrangs mit denen des Antriebsstrangs mit DC-DC Wandler Erweiterung unter Anwendung aller verlustoptimierenden Betriebsstrategien verglichen. Die Ergebnisse zeigen den Vorteil des alternativen Antriebsstrangs bei Stadtfahrten im **Neuen Europäischen Fahrzyklus** mit bis zu 15,31% geringeren Energieverlusten aufgrund der einstellbaren Wandlerbetriebsart bei Teillasten unter Verwendung der entwickelten Betriebsstrategien.

Stichworte: Elektrofahrzeug, Interleaving DC-DC-Wandler, Schaltnetzteil, Betriebsstrategie, Regelungssystem Entwurf

Abstract

In the recent decades, the widespread adoption of internal combustion engine vehicles has been influenced by two significant challenges, namely the fluctuating price of oil and the resultant climate change caused by the emissions from fossil fuel vehicles. As a result, the development of performant electric vehicles and hybrid electric vehicles has gained much attention and become a trend in recent years. To achieve this goal, research investigations to enhance the electric vehicles in terms of cost, energy consumption, weight, and reliability are imperative. One of the most crucial objectives in the development of electric vehicles is the optimization of the electric drivetrain for maximum efficiency, with an important factor being the maximum range capability per full charge (analogous to a full tank in an engine-based vehicle).

The drivetrain components of commercial electric vehicles include the battery pack, inverter, and electric machine. However, in such a drivetrain configuration, the inverter input voltage (DC-Link voltage) is equal to the battery voltage, which presents some drawbacks. Firstly, different values are required to achieve the optimum voltage level during the battery stack and electric machine design process. Secondly, the battery state of charge negatively impacts the electric machine operating area. Additionally, as it will be demonstrated in this work, reducing the DC-Link voltage lowers inverter power losses. In operating points where the necessary machine voltage is lower than the battery voltage rated value, a fixed DC-Link voltage equal to the battery voltage results in additional inverter losses.

The focus of this work is on the design and analysis of a battery electric vehicle drivetrain using an additional DC-DC converter extension in it. Accordingly, the main objective is to investigate the energy efficiency benefits of shifting the operating points of the drivetrain components by placing a DC-DC converter between the battery and the inverter-fed machine. For this purpose, a multiphase interleaving converter is selected, and through comprehensive modeling of the drivetrain, the appropriate control system is designed and evaluated on the one hand, and loss optimizing operating strategies are developed on the other hand to take the most advantage of the integration of a DC-DC converter into the drivetrain.

A prototype multiphase interleaving DC-DC converter is built as a part of the research work to verify the developed models and control system under different load and operating mode conditions. In the final step, after dimensioning two different drivetrains for a prototype electric vehicle with 60 kW maximum power, the voltage converter energy losses of a conventional drivetrain is compared to that of the drivetrain with DC-DC converter extension under the utilization of all loss optimizing operating strategies. The results show the advantage of the alternative drivetrain during the city rides of **New European Driving Cycle** with up to 15.31%

lower energy losses due to the adjustable converter operating mode at partial loads using the developed operating strategies.

Keywords: Electric Vehicle, Interleaving DC-DC Converter, Switching Power Supply, Operating Strategy, Control System Design

1 Introduction

1.1 Motivation

The history of the first electric vehicles goes back to 19th century. This type of vehicles dominated the new vehicle registration until the late 1920s [15]. This lead was then overtaken by internal combustion engine vehicles due to better performance, lower cost and low fuel costs at the time. The development of petroleum as a predominant energy source began in the early 1900s, which was followed by the invention of methods to produce gasoline from crude oil [16]. In the early 1930s, the mass production of gasoline by refineries and its easier availability to the general public led to the proliferation of internal combustion engine vehicles and slowed down the development and production of electric vehicles.

In recent decades, the spread of internal combustion engine vehicles as the main means of transportation has been influenced by two new problems, namely the price of oil and climate change due to emissions from fossil fuel vehicles. Figure 1.1 shows the development of new oil discoveries as well as oil production (consumption) over time [1]. It can be clearly seen that the discovery volume is decreasing while production is increasing. These facts, together with the lack of investment in new oil fields, lead to an upward trend in future oil prices, which also means that transportation by combustion engine vehicles will become more expensive.

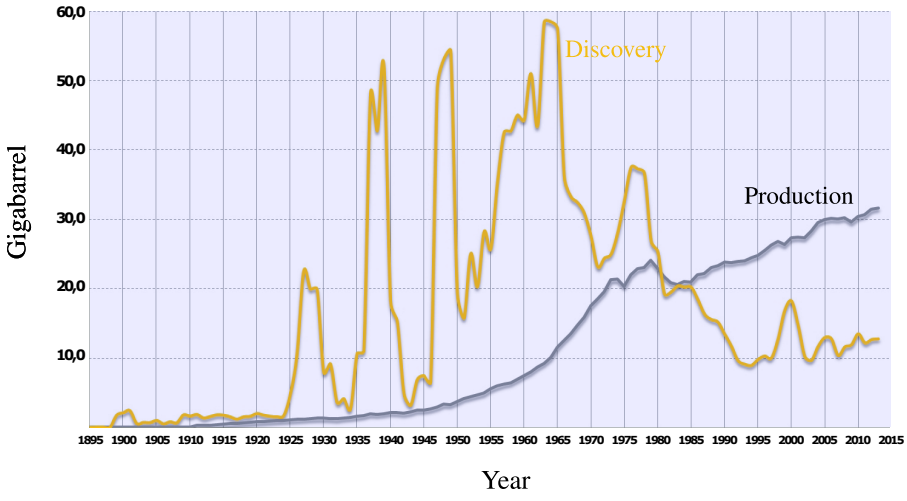

Figure 1.1: Oil discovery (yellow line) against oil production (gray line) in gigabarrel over time (from [1])

Moreover, climate change is becoming a major problem facing the earth and humanity today. One of main reasons for the global warming is the CO_2[1)] emissions from fossil fuels. Figure 1.2 shows the contribution of fossil fuels to global CO_2 emissions over time, as well as the contribution of oil as one of the main fossil fuels to global CO_2 emissions. According to this study ([2]), emissions from fossil fuels are increasing over time and should be stopped to prevent climate change and global warming. Because of this reason different countries and states in the world are trying to support the electrification of the transportation. As an example the California state in the US decided to ban the sale of new gasoline cars by 2035 to speed a wider transition to electric vehicles [17]. Also Germany pushes the use and development of electric and hybrid vehicles by subsidizing them up to 9000 Euros until the end of 2022 [18].

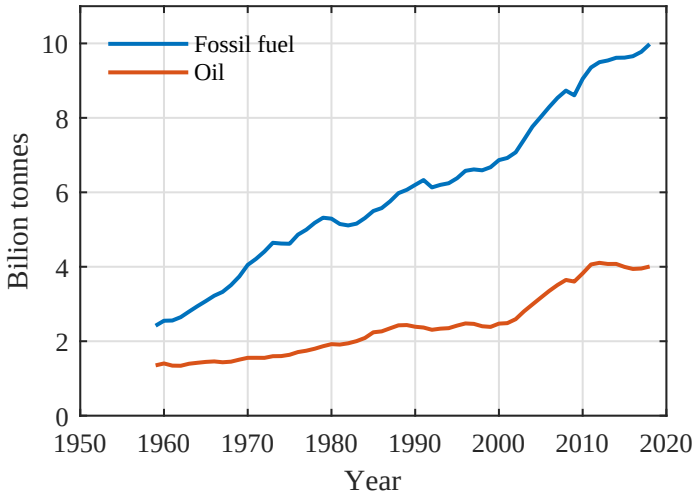

Figure 1.2: Global CO_2 emissions from fossil fuels in general and petroleum's share of total emission (from [2])

Due to rising fuel costs and the need for low-emission vehicles, the development of electric vehicles (EVs) and hybrid electric vehicles (HEVs) has attracted much attention and become a trend in the recent years. In order to achieve this goal, investigations to make EVs more efficient in terms of cost, energy consumption, weight, and reliability are necessary. From a consumer's point of view the electric vehicles should be reasonable enough, in terms of features, to replace the conventional engine vehicles. An important issue among the features is the maximum distance range capability per full charge (full tank in engine type vehicle) and accordingly, one of the most essential objectives in electric vehicle development is the optimization of the electric drivetrain for the maximum efficiency. In other words, investigations lead to extending the operating distance of the vehicle are a must-to-do task. Accordingly, the focus of this work is to investigate alternative drivetrains for an all-electric vehicle (can also be used in parallel plug-in hybrid electric vehicles) to achieve the maximum range per full charge.

In this chapter, the state of the art in the aforementioned field of research is discussed and, building on this, the problem statement is presented. This is then followed by the research objective and the structure of the thesis at the end of this chapter.

[1)] CO_2 is a greenhouse gas that acts like the glass of a greenhouse, trapping heat and warming the inside

1.2 Low Emission Drivetrains - State of the Art

The alternatives to vehicles with internal combustion engines are mainly divided into three main categories (discussed in [19]), namely battery electric vehicles, fuel-cell electric vehicles, and hybrid electric vehicles. These vehicle categories differ from each other by following items:

1. Fuel (electric charge, hydrogen, gasoline/diesel)
2. Energy storage technology (battery, super capacitor, fuel-cell)
3. Intermediate components (voltage converter)
4. Energy converter (electric machine, combustion engine)

In battery electric vehicles, the electric charge serves as the traction energy source. In a single battery cell, which consists of separate chambers with two electrodes, a separator and an electrolyte, the chemical reactions at the electrodes are used to convert the chemical energy into electrical energy (discharging) and vice versa (charging). There are different battery technologies depending on the electrode and electrolyte material, and the two types most commonly used in electric vehicles are nickel-metal hybrid and lithium-ion batteries [20]. During charging process of the battery, electrons taken from the positive electrode generate positive ions (Li^+ in lithium-ion batteries) that can move in the electrolyte through the ion-conducting separator and reach the negative electrode. These positive ions at the negative electrode are then combined with the electrons absorbed from the charging circuit and finally stored between the atom layers of the negative electrode (the left picture in figure 1.3 shows the charging process of a lithium-ion battery). This process gets reversed during the discharging phase, where the chemical energy is transferred back in electrical energy as shown in the right picture of figure 1.3 (chemical oxidation in the negative electrode → electron flow from the the outside circuit and positive ion flow through the electrolyte both towards the positive electrode → chemical reduction in the positive electrode).

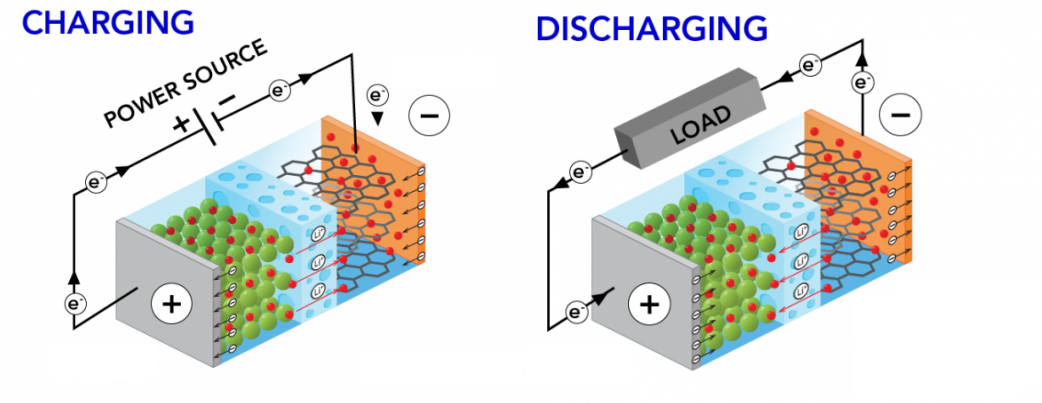

Figure 1.3: Charging and discharging processes of a lithium-ion battery, in which the lithium ions Li^+, shown with red dots, play an important role (from [3])

Figure 1.4 shows a typical drivetrain of a battery electric vehicle. One of the main advantages of the battery electric vehicle is its relatively simple drivetrain, which consists of the battery pack, a voltage converter and the electric machine. In addition to the simplicity of the drivetrain, the possibility of energy recovery during braking, and no local generation of CO_2 are the other two advantages of battery electric vehicles. On the other hand, the vehicle's range is limited due to the capacity constraints of existing battery technology, and recharging of the battery is a time-consuming process compared to the conventional refueling process for internal combustion engine vehicles. Furthermore, the lifetime of the battery (maximum number of charging and discharging cycles until the battery is unusable) is usually shorter than that of the vehicle itself, so the battery needs to be replaced during the life cycle of the vehicle [21].

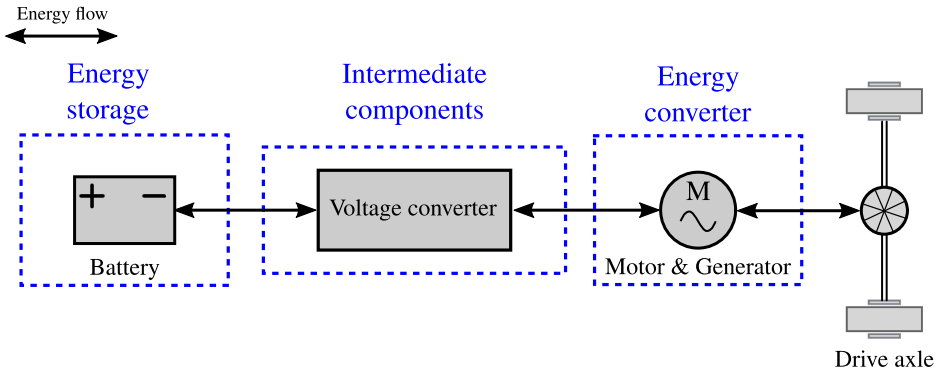

Figure 1.4: Drivetrain of a battery electric vehicle consists of a battery pack, a voltage converter, and an electric machine

The next type of vehicles are the fuel-cell electric vehicles, where generally the hydrogen is the main energy source. The fuel-cell is an electrochemical energy converter, that generates the electric energy from a fuel (in the most cases hydrogen) and an oxidizing element like the air oxygen. The Proton Exchange Membrane (PEM) is a common type of fuel-cell used in this type of vehicles [22]. Figure 1.5 shows the simplified structure of a fuel-cell single unit. It consists of a positive electrode (cathode) and a negative electrode (anode) separated by a plastic membrane that serves as an electrolyte. The electrodes consist of an electrically conductive material with a porous structure, and on their surfaces catalyst components are applied to accelerate the chemical reaction. The operation principle of a fuel-cell is based on the chemical reaction at the porous surface of the electrodes. The hydrogen molecules (fuel) present at the anode electrode gets oxidized, producing positive hydrogen ions H^+ and free electrons. The plastic membrane acts as an electron insulator, but allows the generated positive ions to diffuse towards the cathode electrode. At this stage, the hydrogen ions react with the available oxygen at the cathode and, more importantly, with the electrons traveling from the anode through the external circuit. This electron flow results in power being supplied to the load.

Figure 1.6 shows the drivetrain components of a fuel-cell electric vehicle. The primary components of such a drivetrain consist of the fuel-cell, voltage converter and electric machine. There are also some alternatives of this drivetrain consisting of an additional electrical energy storage (battery or super capacitor shown in figure 1.6) that can be used to shift the operating point of the fuel-cell when needed to either achieve better vehicle performance or drivetrain

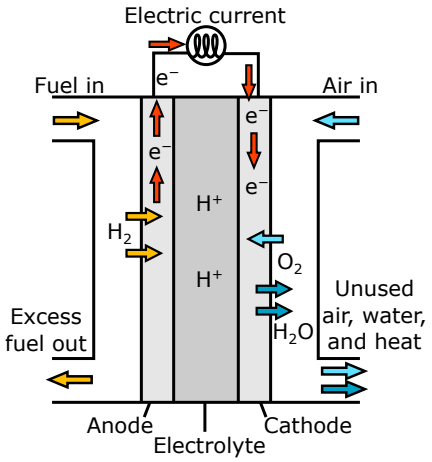

Figure 1.5: Internal structure of a Proton Exchange Membrane fuel-cell with the illustration of chemical reaction inside the cell (from [4])

efficiency, as presented in [23] and [9]. Furthermore, the use of this additional energy storage enables bidirectional energy flow and recuperation in the drivetrain.

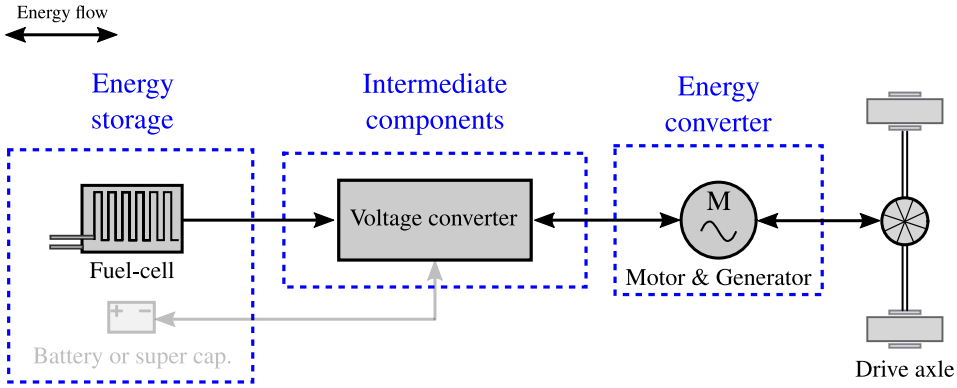

Figure 1.6: Drivetrain of a fuel-cell electric vehicle consists of a fuel, a voltage converter, and an electric machine with the option of using an additional energy storage for the system

One of the main advantages of fuel-cell EVs compared to battery EVs is that the vehicle's range is unlimited and comparable to that of the internal combustion engine due to short refueling time, assuming good hydrogen refueling station coverage. At the same time, the drivetrain maintains a better efficiency in comparison to the drivetrains with combustion engine. This is because of the fact that no thermal or mechanical processes are required in the energy conversion chain of a fuel-cell and unlike combustion engines it is not subject to Carnot-Cycle (discussed in [24] and [23]). Another positive aspect of this vehicle type is the CO_2 emission-free nature of the entire mobility chain, from the production of the required hydrogen fuel ([25]) to the drivetrain itself. The relatively lower power density of fuel cells and the lack of a widespread infrastructure of hydrogen refueling stations are two disadvantages of this drivetrain technology that make its battery-based counterparts more attractive to car companies.

The last category of alternative drivetrains are the so-called hybrid electric vehicles. The most important attribute of HEVs is that they have two different types of electromechanical energy

converters. Typically, this type of vehicle uses an electric energy converter (electric machine) in addition to a conventional combustion engine. The idea of the hybrid electric vehicle is to combine the advantages of the two worlds of the pure electric drive and the vehicle with combustion engine, namely the high efficiency of electric drivetrains and the large driving range of conventional vehicles. Furthermore, the use of an additional electric machine offers the possibility of optimizing the design of the combustion engine and shifting its operating points to achieve the maximum efficiency [26]. Depending on the arrangement of HEV components, there are different drivetrain variants, with serial HEVs and parallel HEVs being two main types of this vehicle category.

In a serial hybrid electric vehicle, the energy converter components (internal combustion engine and electric machine) are connected in series, the wheel drive system is purely electric, and the internal combustion engine is connected to an electric machine utilized in generator mode to convert the mechanical energy into electrical energy. This electric energy can either directly supply the electric machine or charge the optionally integrated battery. The inclusion of the battery in the drivetrain also has the advantage of enabling recuperation. Figure 1.7 shows the structure of a serial HEV. The parallel hybrid electric vehicles, unlike their serial counterparts, have the wheel drive shaft coupled to both the internal combustion engine and the electric machine, as shown in 1.8.

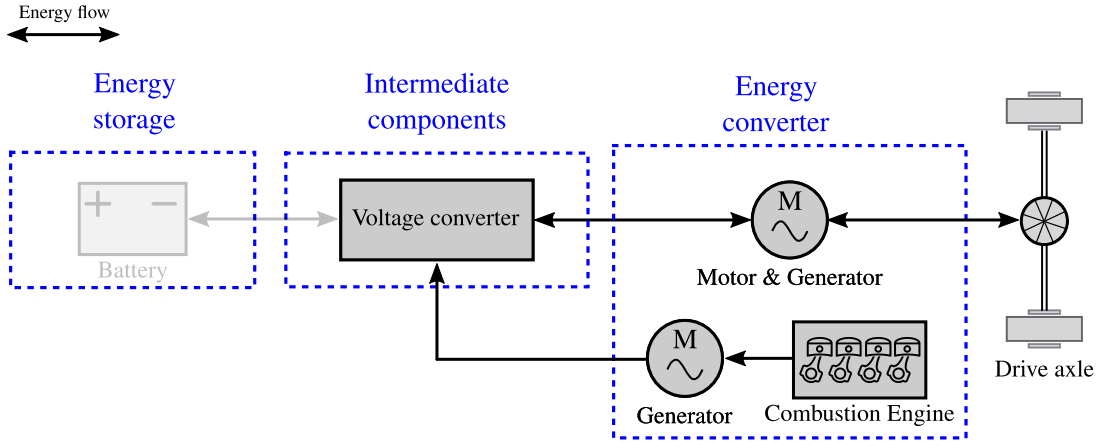

Figure 1.7: Drivetrain of a serial hybrid electric vehicle consists of a traction electric machine, a combustion engine, and a generator with the option of adding an electric energy storage to the system

In addition to the better efficiency of the HEV drivetrain compared to the conventional combustion engine drivetrain, it is possible to use the electric part of the drivetrain and drive purely electrically for the limited driving range allowed by the electric energy storage system ([27]). In other words, this means, the realization of CO_2 emission-free driving cycles out of a HEV drivetrain. Based on the available electric power in the HEV, the hybrid vehicles are classified into different categories, which represent the hybridization class of the vehicle. As discussed in [28], the more the electric power, the higher is the energy saving, but for that the higher is the manufacturing cost of the vehicle. With all that said, the complexity of the HEV drivetrains is very high, with all the required mechanical and electrical components and their control systems.

This is the main disadvantage of HEV, which makes them somehow a temporary solution for implementing a lower emission mobility.

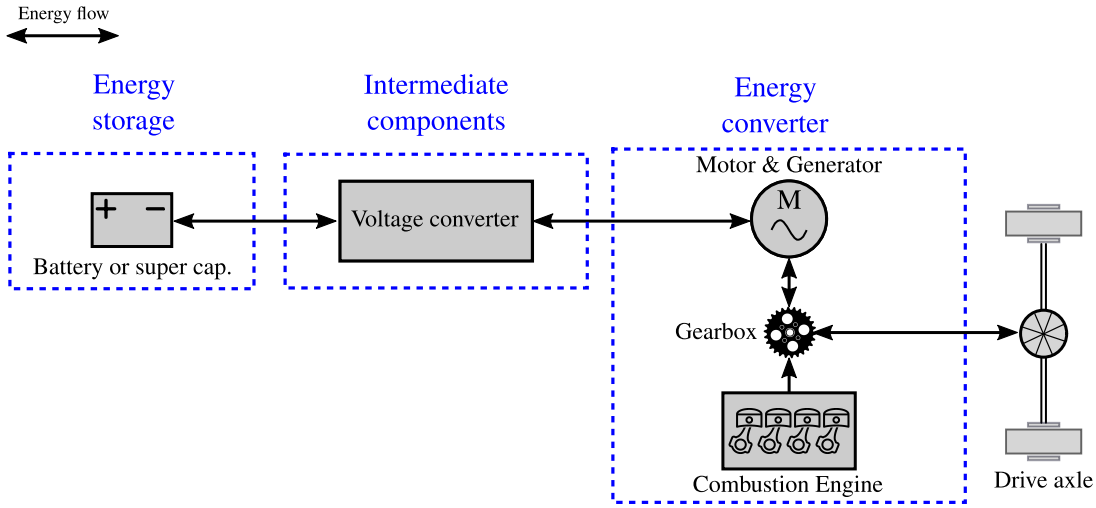

Figure 1.8: Drivetrain of a parallel hybrid electric vehicle consists of same components as a battery electric vehicle with an additional combustion engine coupled to the wheel drive shaft in parallel with the electric machine

As outlined in the overview of the state of the art low-emission drivetrains, the voltage converter is an essential component used in all of them. The design requirement of this voltage converter is different in each drivetrain application. In other words, the topology of the drivetrain (whether AC-DC, DC-DC, or DC-AC converter is needed) and its rating values (nominal voltage of the battery, the machine or the fuel cell) are two main aspects when defining the requirements and designing the voltage converter. Figure 1.9 shows the the voltage converter part of each one of the drivetrains. As it can be seen in this figure, the use of a DC to AC converter (referred to as an inverter in following parts of this work) is the common part among all drivetrains, and is a mandatory component to provide the required 3-phase voltage to the electric machine. Same is true for the AC to DC voltage converter shown in figure 1.9 (c), which in an HEV drivetrain converts the generator 3-phase voltages to a rectified DC-Link voltage at the input of the inverter. It should be noted that the necessity of using DC-DC converter in each of the voltage converter variants shown in the figure 1.9 depends on the design of the rest of the system as well as the operating points of each one of the components. In the following considerations, the focus in this work is on the drivetrain shown in figure 1.9 (a) [2)].

By reviewing commercial electric vehicles ([19]), the components of the drivetrain consisting of the battery pack, the inverter and the electric machine (same as the drivetrain shown in figure 1.9 (a) but without an additional DC-DC converter). For instance, Tesla Model S, VW eUP, and BMW i3 are three commercial electric vehicles using a similar topology in their drivetrains with the battery voltage of 375 volts. In such a configuration the input voltage of the inverter (DC-Link voltage) is always equal to the battery voltage which involves some drawbacks. First, in the design process of the battery stack and electric machine, the requirement for the optimum

[2)]For simplicity, from here on in the text, the term electric vehicle refers to battery-powered electric vehicle

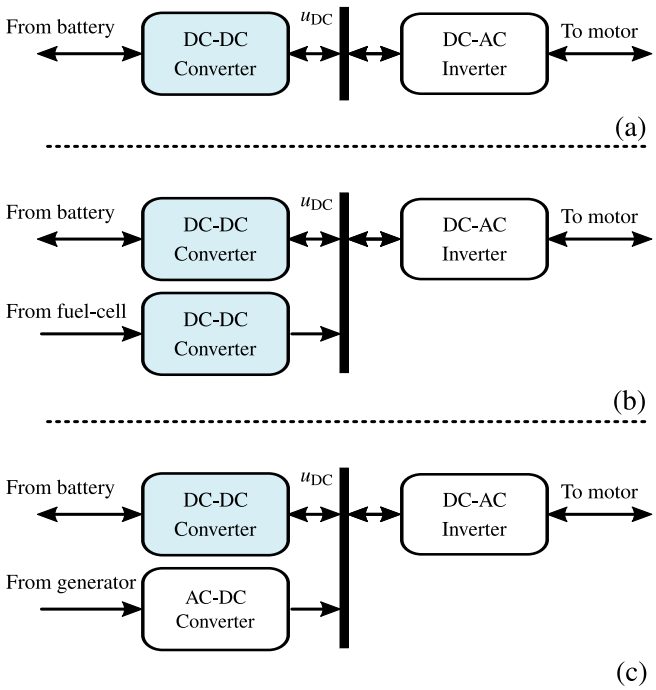

Figure 1.9: The voltage converter structure for different low-emission drivetrains (a) battery EV and parallel HEV (b) fuel-cell EV (c) serial HEV

voltage level yields different values (the optimal voltage of the battery is lower than that of the machine ([29])). Second, the operating area of the electric machine will be negatively affected by the state of charge of the battery. In addition, as it will be shown in this work, the inverter power losses will decrease as the DC-Link voltage decreases, and in the operating points where the required machine voltage is lower than the rated value of the battery voltage, additional losses will occur in the inverter if the DC-Link voltage is fixed to the battery voltage. Because of the aforementioned reasons, the DC-Link voltage level provides a means of optimization. In [30] and [31], it is concluded that by decreasing the DC-Link voltage at partial loads (low speeds) the efficiency of the drivetrain increases. It should be noted that according to [32] at the operating points close to the rated power of the machine a higher DC-Link voltage results in higher efficiency. Adjusting the DC-Link voltage based on the operating point of the motor and changing the inverter modulation strategy for the maximum utilization of the DC-Link voltage are two methods proposed in [29] to increase the drivetrain efficiency. As discussed in [33], for the maximum usage of the DC-Link voltage, the inverter modulation strategy can be extended to the six-step mode to maintain a higher phase voltage at the machine terminal.

A decoupling between the battery voltage and the inverter input voltage can be realized by implementing a DC-DC converter between these two components as shown in figure 1.9 (a). Accordingly, a lower voltage for the battery can be selected, whereas the operating area of the electric machine remains unchanged. In this alternative drivetrain and through the implementation of a variable DC-Link voltage, the power losses of the inverter and electric machine can be reduced. However using the DC-DC converter itself causes additional losses. Therefore it should be investigated whether or not the power savings outweigh the extra losses.

As discussed in [34], in commercial electric vehicles there are several topologies for implementing a DC-DC converter with relatively high voltage gain. For this type of application, the single-phase bidirectional boost converter is a common topology that has fairly high efficiency at voltage conversion ratios between two to four ([35]). Toyota Prius and Toyota Camry are two examples of commercial hybrid EVs (same drivetrain as presented in figure 1.9 (c)) in the market which use this component in their drivetrain ([36]). However the use of a single-phase converter has some disadvantages. On the one hand, limiting the current and voltage ripple to an acceptable level will result in large passive components; on the other hand, the DC-DC converter must be designed for the maximum output power of the vehicle, which leads to relatively high power losses at partial loads. In [37] a multiphase (12-phase) bidirectional boost DC-DC converter with a power of 100 kW is presented, where the proposed optimization for the utilization of the multiphase system is to change the number of active phases with respect to the operating point of the converter. This method is used to reduce the losses and volume of the converter. Based on [32], the major part of the converter losses occur in its inductor. By analytically calculating the induction losses (as a function of inductance and volume), an optimization scheme for inductor size selection can be performed given a particular drive cycle, as proposed in [32]. Another topology called Multi-Device Interleaved Multiple-Input Converter (MDI-MIC) is presented in [38]. The main advantage of this topology is the capability of using multiple DC sources. Accordingly, the proposed topology uses two bidirectional 4-phase converters for the battery and super-capacitor sources and one unidirectional converter for the fuel cell source. By using the interleaving switching method for the four-phase converter in [39], the frequency of the input current ripple becomes equal to four times the switching frequency, which means that the size of the EMI filter can be drastically reduced at a constant switching frequency.

The use of DC-DC converters for the vehicle drivetrain application is a current research topic, given the increasing demand for more efficient and cost-effective battery electric vehicles. In [40] published in 2022, a vehicle drivetrain consisting of interleaving DC-DC converter is investigated with respect to the lifetime of the power electronic devices used in the drivetrain. In this work the converter controller is designed, and with the help of the stress-based lifetime estimation approach, it has been concluded that the silicon carbide based (SiC-based) interleaving boost converter is more reliable in the city rides, but generally meets the target lifetime requirement. Another recent research published in 2021 ([41]) analyzed the use of DC-DC converter with SiC-MOSFET technology in the vehicle drivetrain, and its effect on the performance and energy losses of the vehicle drivetrain. In this work a multiobjective genetic algorithm is used to select drivetrain components to achieve lowest energy losses. It was found that the use of DC-DC converter in the drivetrain leads to a reduction in energy losses, but no specific loss-optimizing operating strategy for the DC-DC converter is proposed to further improve the energy savings. In [42] published in 2018, a simulation platform is proposed to model a modular drivetrain architecture that includes a SiC-based high-voltage DC-DC converter and various hybrid battery storage systems with different voltage levels (high-energy batteries and high-power batteries). In [43] the integration of a single phase boost DC-DC converter into the drivetrain of parallel hybrid electric vehicle is investigated. In this research the boost converter has been used as voltage stabilizer to cover the demanded HEV operation over the complete range of the battery state-of-charge. Another recent research on DC-DC converter application in BEV drivetrain

is provided in [44], where an interleaving buck converter is analyzed. The work focuses on designing the proper control system for the step down converter using averaged switch model technique. The dynamic performance of the developed controller is then verified with the help of a hardware-in-the-loop test setup. A dual-port bidirectional DC-DC converter topology is proposed in [45] to utilize multiple electrical energy sources (battery and photovoltaic panel in this case) in the drivetrain of the EVs. In this work, different operating modes of the developed converter topology are analyzed, focusing on the optimal energy distribution between the machine, the battery, and the photovoltaic.

1.3 Research Goal and the Structure of the Work

The main focus of this work is on the conception and analysis of the battery EV drivetrain shown in figure 1.4 [3)]. Unlike most commercial electric vehicles which use a standard DC-AC inverter in their drivetrain, the selected voltage converter consists of a DC-DC converter and an inverter, as shown in figure 1.9 (a). Accordingly, the main objective of this work is to investigate the energy efficiency benefits of shifting the operating points of the drivetrain components by placing a DC-DC converter between the battery and the inverter-fed machine in the drivetrain. For this purpose, a multiphase converter is chosen as the topology of choice. The converter should be optimally dimensioned for the application, and then the appropriate control system and the correct operating strategy (calculation of the load-dependent optimum of the output voltage, the switching frequency and the number of active phases) should be developed for the converter. Experimental results from a prototype converter being built as part of the research should verify the theoretical results. Finally, two different drivetrains should be designed and dimensioned with and without the DC-DC converter, to evaluate the advantages and disadvantages of using this additional component in the drivetrain.

In **chapter 2** different subcomponents of the electric drivetrain are modeled in terms of electrical characteristics and power losses. The DC-Link capacitor, the power inductor, the power transistor and the electric machine are the components modeled in this chapter using SIMULINK. Different types of losses are taken into consideration for each component. In the capacitor model, the ohmic and dielectric losses are included, and in the power inductor, the copper losses and core losses are the main loss elements modeled. For the power transistors, the switching and conduction losses are included in the model. In addition, a temperature model is provided for the power transistors to evaluate the temperature dependent losses of these switching elements. For the modeling of the electric machine, the ohmic losses of the stator and rotor winding packages are the main modeled power losses.

In **chapter 3** the above mentioned subcomponents are connected together to model the entire drivetrain, including DC-DC converter, inverter, and electric machine. This transient model of the plant is also referred to as the switching model of the drivetrain. The reason is the

[3)] Although the hybrid EV is not the focus of this work, the research results can also be applied to the parallel HEVs, since the same electric drivetrain can be used for the electric part of a parallel hybrid EV.

consideration of the switching state of each power transistor in the model over the course of the simulation time. This chapter also discusses the control system design of the drivetrain components (including the controller and the corresponding pulse modulator and measurement system of the multiphase converter and the inverter) and optimizing the controller parameters. This control system is then connected to the developed drivetrain model (converter, inverter, and the electric machine) to simulate the transient behavior of the drivetrain under load and operating point changes. In addition to the switching model of the inverter and the multiphase interleaving DC-DC converter, state-space average models of these components are developed to reduce the computational complexity and make the drivetrain model applicable for long simulation times (e.g., for simulating an entire driving cycle). At the end of this chapter the developed switching model and average model are compared with each other in terms of dynamic behavior as well as the power and energy losses.

In **chapter 4** various operating strategies are developed using the models presented in the previous chapter to reduce the power losses of the drivetrain, including the additional multiphase DC-DC converter. These operating strategies are all applied to the DC-DC converter part of the drivetrain, and require the implementation of various extensions to the drivetrain control system. The developed operating strategies are as follows: the variable DC link voltage, the variable number of active phases, the passive mode, and the variable switching frequency. In this chapter, the test setup built to verify the models and the developed loss-optimizing operation strategies is also presented in detail. Finally, the simulation results are validated against the experimental results derived from the test setup.

In **chapter 5** the so-called reference drivetrain (without DC-DC converter) is compared to the alternative drivetrain shown in figure 1.9 (a) in terms of power losses and energy consumption. For this comparison, a prototype vehicle is mechanically modeled which, along with a standard speed profile, replicates a realistic drivetrain load necessary for the power loss comparison. The resulting speed and torque profiles are then used to dimension and select different components of the aforementioned two drivetrains, which differs from each only in the battery voltage and the DC-AC voltage converter part. In the second part of this chapter, for the selected driving cycle, the power losses of the voltage converter in the reference drivetrain are compared with the voltage converter losses of the alternative drivetrain. This comparison is done after activation of various developed loss optimizing operating strategies.

Last but not least, **chapter 6** summarizes the research findings, draws a conclusion, and provides an outlook.

2 Component Modeling

As discussed in the previous section, an state of the art electric vehicle consists of a high voltage battery, a power inverter, and an electric machine. According to the research goal, the effect of a DC-DC converter (between the battery and the inverter) on the drivetrain should be investigated in this work. The comparison should be done in terms of the efficiency of the new drivetrain against the state of the art drivetrain.

In this section the modeling of the drivetrain components are presented. In this regard, the model of the utilized elements will be presented, which includes the passive components such as inductor and capacitor as well as the active power electronic components such as power MOSFET, power IGBT, electric machine, and battery.

The modeling at the component level is provided in a way that it can be used for the following use-cases:

1. Dimensioning of the drivetrain (stationary model)
2. Design and verification of the control system (transient model)
3. Development and evaluation of the operating strategies (quasi-transient model)

The stationary models are implemented using MATLAB in the form of MATLAB-classes and the transient models are realized with the help of SIMULINK as discrete subsystems. Some simulation results of the components which are used to implement the final hardware are included in this section as well.

The integration of the provided models into the main drivetrain model, which consists of 3-phase DC-AC inverter and multiphase DC-DC converter, will then be presented in the next chapter.

2.1 DC-Link Capacitor

The first component which is discussed in this chapter is the capacitor. High power capacitors are widely used in power conversion applications. The role of a power capacitor is to balance the instantaneous power between the two parts of the system while maintaining the voltage [46].

In the drivetrain application the power capacitor is utilized to decouple the power flow between

the inverter and the DC-DC converter, and stabilize the voltage at the DC-Link by delivering/absorbing the excessive power to/from DC-DC converter and inverter. Figure 2.1 shows the placement of the DC-Link capacitor in the drivetrain.

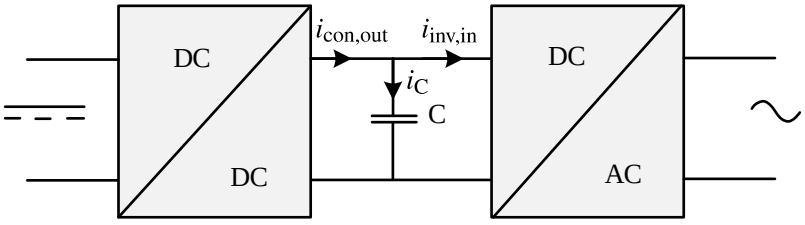

Figure 2.1: DC-Link capacitor in the drivetrain

According to the literature and from the reliability point of view, capacitors have a high failure rate in the power electronic devices [47], [48]; Therefore the proper selection of this component is very important, specially regarding the fact that in the automotive application the capacitor has to work under relatively harsh condition (high temperature and maybe humidity). Another essential point is the volume of the DC-Link capacitor. In the other words, achieving a high energy density of the DC-Link capacitor is another challenge in this area [49].

In order to model this component, different properties of an actual capacitor, which differentiate the characteristics of a practical capacitor from an ideal one, should be taken into account. Figure 2.2 (a) shows the elements included in the model of a given DC-Link capacitor [50]. In this model C_R represents the ideal capacitance, R_S is the series resistance caused by the lead and junction resistances, and L_S is the series inductance (in some literature it is noted with $L_{C,ES}$) which is dependent on the inductance of the electrodes and supply lines.

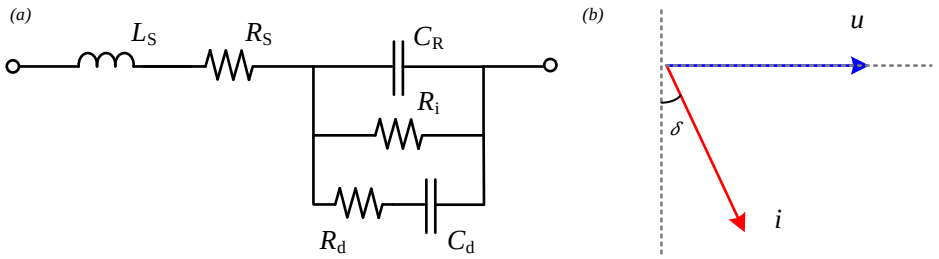

Figure 2.2: Lumped model of the capacitor (a) equivalent circuit (b) V-I phasor diagram for the frequencies below the resonance frequency of the capacitor

There are also some other elements which should be added into the model. These are shown in Figure 2.2 (a) with R_i (the leakage resistance which is usually very large), R_d (models the dielectric losses due to dielectric absorption and molecular polarization which is significant at high frequencies) and C_d (inherent dielectric absorption which is only significant in electrolytic capacitors). By neglecting the latter three elements, the impedance of the capacitor and its resonance frequency are calculated using equations 2.1 and 2.2 respectively.

$$Z_C = R_S + j\,\omega\,L_s - \frac{j}{\omega\,C_R} \tag{2.1}$$

$$\omega_{\text{res}} = \frac{1}{\sqrt{L_{\text{s}}\, C_{\text{R}}}} \tag{2.2}$$

The power losses of the DC-Link capacitor can be divided into two parts of ohmic losses ($P_{\text{C,ohm}}$) and dielectric losses ($P_{\text{C,diel}}$). These losses are modeled with the help of the resistive elements shown in figure 2.2. Regarding this, to represent the power losses of the DC-Link capacitor, an equivalent series resistance ($R_{\text{C,ES}}$) is defined, which contains both ohmic losses and dielectric losses. It should be noted that $R_{\text{C,ES}}$ is a frequency dependent quantity and the best way for its determination is to measure the power losses with a power analyzer and then calculate the $R_{\text{C,ES}}$ using equation 2.3.

$$P_{\text{C,loss}} = P_{\text{C,ohm}} + P_{\text{C,diel}} = R_{\text{ES}} \cdot {I_{\text{C}}}^2 \tag{2.3}$$

Another important term which is widely used in this area is the so-called dissipation factor. This is actually the ratio of the resistive power losses to the reactive power oscillating in the capacitor. This factor can be calculated by dividing the real part of the capacitor impedance to its imaginary component. For this reason, this factor is often represented by $tan\delta$ (the angel in figure 2.2 (b)). In some capacitor datasheets $tan\delta$ is provided instead of $R_{\text{C,ES}}$, and $R_{\text{C,ES}}$ can be calculated with the help of the following equation.

$$tan\delta = \frac{R_{\text{ES}}}{X_{\text{C}}} \tag{2.4}$$

There are several types of capacitors, which are utilizable for the DC-Link application. The most common types are Aluminum Electrolytic Capacitors (Al-Caps), Metalized Polypropylene Film Capacitors (MPPF-Caps), and high capacitance multi-layer Ceramic Capacitors (MLC-Caps) [51]. One major factor that determines the capacitor properties is its dielectric material.

Each dielectric material has a relative permittivity (dielectric constant) and a given maximum allowable electric field strength per unit length. For a given dielectric these two factors along with the system requirements (voltage and capacitance) are used to design the capacitor with resulting energy density. Figure 2.3 shows the relative permittivity, electric field strength, and energy density limits for three different dielectrics ([5]); These are AL_2O_3, polypropylene and ceramic which are the dielectric materials used in Al-Caps, MPPF-Caps and MLC-Caps respectively.

As it can been seen in figure 2.3 AL_2O_3 has the highest energy density among theses three dielectric types. This is because of the high breakdown field strength and high permittivity of AL_2O_3. Therefore aluminum capacitors have the lowest cost per joule, although this type of capacitors suffer from high power losses and low current ripple ratings due to their high $R_{\text{C,ES}}$. Another disadvantage of the aluminum capacitors is their limited lifetime because of the

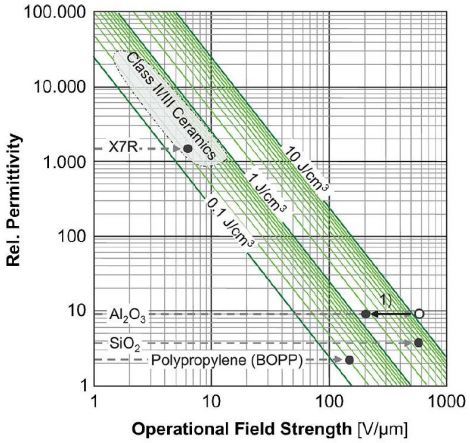

Figure 2.3: Energy storage density for various dielectrics (from [5])

electrolyte evaporation issue. As shown in figure 2.3 ceramic has the highest permittivity, but because of the low field strength capability of this material, achieving a high energy density is very challenging. Another issue of the ceramic capacitors is their relatively high cost and mechanical sensitivity. The MPPF capacitors on the other hand provide a balanced performance in terms of cost, $R_{\mathrm{C,ES}}$, ripple current, and reliability for high voltages. The weakness of this capacitor type is its relatively large volume and limited temperature ratings. A summary of the characteristics of these three capacitor types is presented in table 2.1.

Table 2.1: Comparison summary of the three types of capacitors: Aluminum Electrolytic, Metalized Polypropylene Film Capacitors, Multi-Layer Ceramic

	Al-Caps	MPPF-Caps	MLC-Caps
Capacitance	🟢	🟡	🟡
Voltage	🟡	🟢	🟢
Ripple Current	🔴	🟢	🟡
$R_{\mathrm{C,ES}}$ and $tan\delta$	🔴	🟢	🟡
Temperature	🟡	🔴	🟢
Lifetime	🔴	🟢	🟢
Energy Density	🟢	🔴	🟡
Cost	🟢	🟡	🔴

The DC-Link capacitor use case can be divided into two main applications; the high current ripple application and the low current ripple application. As stated in [52] the utilized DC-Link capacitor in the electric vehicle's drivetrain is a capacitor with high current ripple ratings and it should withstand high ripples. In [51] it has been discussed that the current ripple rating of the capacitors increases with the capacitance. This increase is much higher in MPPF-Caps and MLC-Caps in comparison with the AL-Caps (because of the higher $R_{\mathrm{C,ES}}$ of the aluminum electrolytic capacitors). Regarding the Multi-Layer Ceramic Capacitors, in the recent years

there are some high voltage components available in the market, specifically the TDK CeraLink Capacitors [53]. But, besides their relatively high price point, the problem with this type of MLC-Caps is the voltage dependency of its capacitance (increasing capacitance with increasing voltage), which makes the design of a system with variable DC-Link voltage very challenging. Based on these facts and along with the summary shown in table 2.1 the film capacitors are a good choice for the drivetrain application.

The capacitor used in this work for the test setup construction is a film capacitor made by EPCOS[1)]. The rating parameters of this power capacitor (*B25655J4507K*) is shown in table 2.2. In order to calculate the power losses of the capacitor for different operating points the measurement results included in the capacitor datasheet [6] are used.

Table 2.2: Nominal electric ratings of the DC-Link capacitor (EPCOS *B25655J4507K*) used for simulation and later on in test setup (from [6])

C_R	$U_{C,max}$	$I_{C,max}$	$W_{C,max}$	L_S	R_S	$tan\delta$ @50 Hz
500μF $\pm$10%	650 V	120 A	50 WS	15 nH	1 mΩ	$8{\cdot}10^{-4}$

Figure 2.4 shows the power losses of the capacitor. As mentioned above the power losses of this capacitor are divided into the ohmic losses and dielectric losses. In figure 2.4 (a) the capacitor ohmic losses in dependence of its effective current (I_C) are provided, and figure 2.4 (b) shows the dielectric power losses with respect to the amplitude of the DC-Link voltage ripple ($\widetilde{u}_{C,ac}$) and the frequency of the voltage ripple (f_{ac}). Therefore, for each operating point the mentioned three quantities (I_C, $\widetilde{u}_{C,ac}$, f_{ac}) are required to be calculated. In order to realize such parametrization some approximations have been made which are discussed in the following.

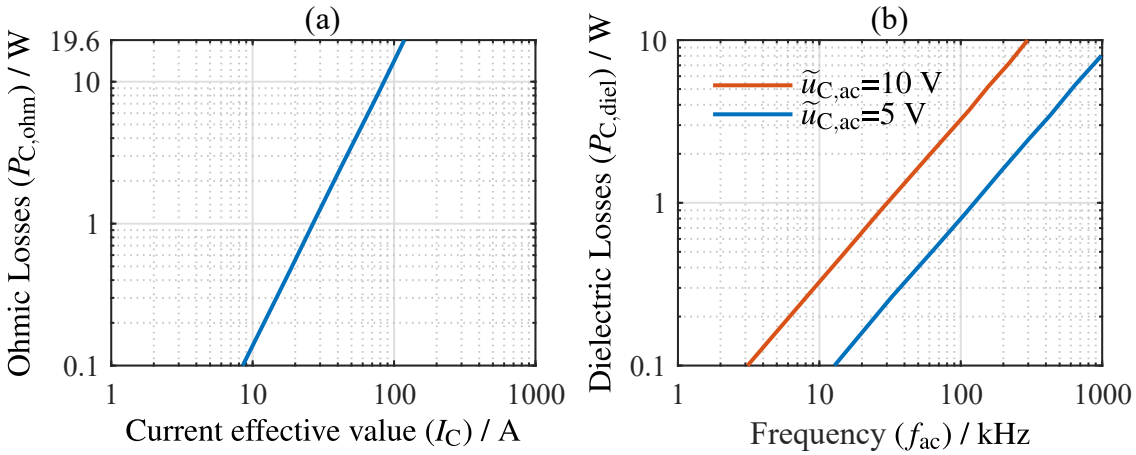

Figure 2.4: Power loss components of the film capacitor used in the Infineon's HybridbPACK 2 (EPCOS *B25655J4507K*) (a) ohmic power losses against the capacitor effective current (b) dielectric power losses against frequency and voltage ripple (from [6])

[1)]EPCOS, a TDK Group Company is a manufacturer of electronic components and this capacitor is integrated into a so-called HybridPACK 2 of Infineon which is a high power inverter module.

At first the calculation method for the capacitor current ripple (I_C) which is required for the ohmic losses estimation is discussed. As it can be seen in figure 2.1 the capacitor current is calculated by the subtraction of the DC-DC converter output current ($i_{con,out}$) from the inverter input current ($i_{inv,in}$). In order to calculate the effective value of the capacitor current ripple (I_C), one way is to make a numeric simulation at each operating point with the instantaneous value of the current as the input. A more practical way is to use an analytical method discussed in the following.

To investigate the relationship between the RMS value of the capacitor current and the DC-Link input and output currents ($i_{con,out}$ and $i_{inv,in}$), these variables are split into AC and DC components as follows:

$$i_{con,out} = i_{con,out,dc} + i_{con,out,ac} \qquad i_{inv,in} = i_{inv,in,dc} + i_{inv,in,ac}. \tag{2.5}$$

By assuming equal DC components of the input and output currents, the components which determine the capacitor current are the AC parts. In the following it will be proven that the maximum value of the capacitor RMS current (independent of the waveform shape of $i_{con,out,ac}$ and $i_{inv,in,ac}$) is equal to the sum of the AC component RMS values of the input and output currents (equation 2.6). Therefore as the worst-case scenario, this maximum value will be used as the input of the look-up-table (created from the ohmic losses shown in figure 2.4 (a)) to calculate the ohmic power losses of the capacitor at each operating point.

$$I_{C,max} = I_{con,out,ac} + I_{inv,in,ac} \tag{2.6}$$

It is known that the input and output currents shown in equation 2.6 have periodic waveforms (related to the switching frequencies of the converter and inverter as well as the output voltage frequency of inverter), therefore to prove the above statement, the maximum RMS value resulting from the sum of two time variable and periodic signals will be analytically calculated. In this case these signals represent the inverter and DC-DC converter currents which adds up together and flow into DC-Link capacitor shown in figure 2.5 (a) (for an easier understanding i_2 is shown in the opposite direction of $i_{inv,in}$ in figure 2.1, but this does not have any influence on the final result).

The above mentioned periodic signals can be decomposed into sinusoidal waveforms with a given fundamental frequency and higher frequency harmonics. By considering only the fundamental frequencies of the input and output signals (figure 2.5 (b)) the RMS value of the resulting summation is presented in equation 2.7 (taken from [7]). In this equation T_N is the period of the capacitor current waveform which is equal to the period of the sinusoidal with the lower frequency in the case of waveforms with different frequencies.

$$I_C^2 = \frac{1}{T_N}\left(\int_{T_N} i_1^2 + 2\int_{T_N} i_1\, i_2 + \int_{T_N} i_2^2\right) \tag{2.7}$$

In the equation above, the maximum value of the second integral term can be calculated with the help of Cauchy-Schwarz inequality which is presented in equation 2.8.

$$\left(\int i_1 i_2\right)^2 \leq \int i_1^2 \int i_2^2 = I_1^2 I_2^2 \tag{2.8}$$

Therefore the maximum value of the capacitor ripple current RMS is:

$$I_{C,max}^2 = I_1^2 + 2\, I_1\, I_2 + I_2^2 = (I_1 + I_2)^2, \tag{2.9}$$

which is the same as the presented current value in equation 2.6. It should be noted that the exact value of the second integral in equation 2.7 depends on the shape of the two waveforms. As an example if the waveforms does not have any correlation in the frequency domain the result of the integral will be equal to zero. Figure 2.5 (b) shows this typical situation, where i_1 and i_2 current waveforms are uncorrelated sinusoidals.

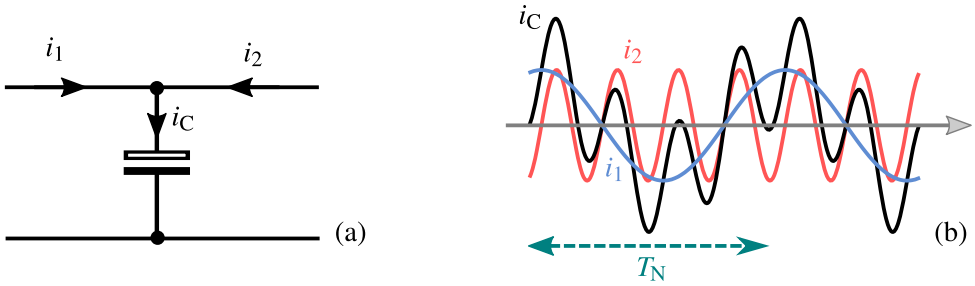

Figure 2.5: Capacitor current waveform in the case that the ac component of input and output currents are sinusoidal and have different frequencies (from [7] and modified)

In summary, to calculate the maximum RMS value of capacitor current ripple ($I_{C,max}$), the AC component RMS values of the DC-DC converter output and inverter input currents will be calculated at each operating point and will be added together. The resulting current will then be used as the input of the ohmic losses look-up-table ($LUT_{C,ohm}$) which is extracted from figure 2.4 (a). This will be done based on the worst-case approximation method, upon which the DC-Link capacitor ohmic losses are finally calculated.

The second step in calculating the capacitor power losses is to determine the dielectric part of the losses. As discussed above for this calculation the amplitude and the frequency of the DC-Link voltage ripple are required at each operating point. As it is known, the capacitor voltage ripple corresponds to the current that flows through the capacitor, and by decomposing the capacitor current into the sinusoidal terms with the fundamental frequency and the higher harmonics, the voltage ripple amplitude ($\widetilde{u}_{C,ac}$) at each frequency of the DC-Link current is calculated [2)] by

[2)] in this calculation $R_{C,ES}$ and $L_{C,ES}$ of the DC-Link capacitor are neglected.

equation 2.10.

$$\widetilde{u}_{\mathrm{C,ac,n}} = \frac{\widetilde{i}_{\mathrm{C,n}}}{2\pi\, f_{\mathrm{n}}\, C_{\mathrm{R}}} \tag{2.10}$$

In order to calculate the exact value of the voltage ripple, the frequency spectrum of the capacitor current at each operating point should be calculated, with which the DC-Link voltage ripple spectrum is determined using equation 2.10. As it has been discussed in [52] and [54] the spectrum of the inverter input current ripple is mostly concentrated on the switching frequency of the inverter and its sidebands. This is also true for the output current of the DC-DC converter. Therefore, as the worst-case, the capacitor current is estimated with a sinusoidal waveform resulting from the sum of converter output and inverter input current ripples. The capacitor current amplitude is derived form equation 2.9 and its frequency is estimated with the maximum switching frequency of the system. The capacitor voltage ripple can then be calculated with the help of the aforementioned two factors and equation 2.10 (figure 2.6). Finally the losses are calculated using the two dimensional dielectric losses look-up-table ($\mathrm{LUT_{C,diel}}$) extracted from figure 2.4 (b).

Based on the procedure mentioned above which is summarized in figure 2.6 the loss model of the capacitor is implemented both in MATLAB as the capacitor-class and also in the SIMULINK as a subsystem. The first one will be used in the stationary model of the drivetrain and the second one will be utilized in the in the quasi-transient model of the system [3)].

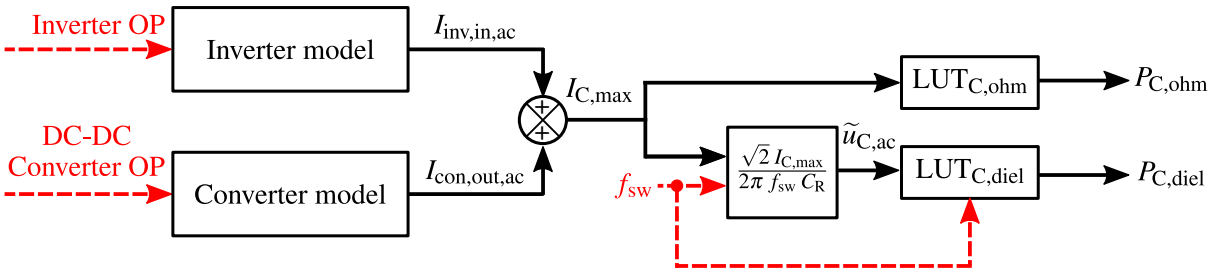

Figure 2.6: Capacitor loss calculation model implemented in MATLAB

2.2 Inductor

The schematic in figure 2.7 shows the structure of an inductor which is supposed to be used in the DC-DC converter part of the drivetrain. This figure shows a winding with a given number of turns N which is wrapped on a magnetic core. By a given current i_{L} flowing through the winding, a magnetic field $\vec{H}$ is produced in the magnetic core which can be calculated with the

[3)] The integration of the provided model in the system is discussed in the respective sections.

help of the Maxwell equation ([55]) and is shown in equation 2.11.

$$\oint_{\mathrm{c}} \vec{H} \cdot d\vec{l} = \iint_{\mathrm{A}} \left(\vec{J} + \frac{\partial \vec{D}}{\partial \vec{t}} \right) \cdot d\vec{A} \tag{2.11}$$

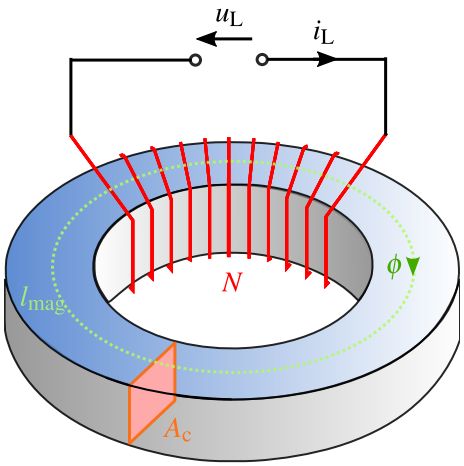

Figure 2.7: Structure of a prototype inductor used in the DC-DC converter

In the equation above, $\vec{J}$ is the current density and $\vec{D}$ is the density of the displacement current. By choosing the integral path c perpendicular to the cross section of the core (see figure 2.7) a complete revolution across the core will enclose the inductor current N times. By defining the path length as the magnetic length of the core (l_{mag}), the equation 2.11 is simplified as follows:

$$H\, l_{\mathrm{mag}} = N\, i_{\mathrm{L}} \triangleq \mathcal{F}. \tag{2.12}$$

The last term of the equation 2.12 is also called the magnetomotive force (MMF) and is presented with with $\mathcal{F}$. Based on the above result, the magnetic flux density B is:

$$B = N\, i_{\mathrm{L}}\, \frac{\mu_0\, \mu_{\mathrm{r}}}{l_{\mathrm{mag}}} \qquad (\text{with} \quad B = \mu_0\, \mu_{\mathrm{r}}\, H). \tag{2.13}$$

In this equation μ_0 is the permeability of air and μ_{r} is the relative permeability of the magnetic core. In some applications the magnetic core will be built with air gaps in order to increase the energy density of the inductor. This will change the relative permeability of the core to μ_{eff} and also affect the dissipation factor $tan\delta$ of the inductor by the factor of $\frac{\mu_{\mathrm{eff}}}{\mu_{\mathrm{r}}}$ in comparison with a core without air gap [56]. The effective permeability is then calculated as follows:

$$\mu_{\mathrm{eff}} = \frac{\mu_{\mathrm{r}}}{1 + \frac{l_{\mathrm{ag}}}{l_{\mathrm{mag}}}\, \mu_{\mathrm{r}}}, \tag{2.14}$$

in which l_{ag} is the length of the air gap. In the case of no air gap μ_{eff} will be equal to μ_r. By defining the core cross section area as A_c the magnetic flux is calculated as in the following.

$$\phi = N\, i_L\, \frac{\mu_0\, \mu_{eff}\, A_c}{l_{mag}} \qquad (\text{with} \quad \phi = B\, A_c) \tag{2.15}$$

Finally the flux linkage Ψ for an inductor with N turns winding is

$$\Psi = N^2\, i_L\, \frac{\mu_0\, \mu_{eff}\, A_c}{l_{mag}} \qquad (\text{with} \quad \Psi = N\, \phi), \tag{2.16}$$

from which the inductance of the inductor is defined as

$$L := \frac{\Psi}{i_L} = N^2\, \frac{\mu_0\, \mu_{eff}\, A_c}{l_{mag}} \triangleq N^2\, A_L. \tag{2.17}$$

The core manufacturers define a given inductance factor for each magnetic core which is presented by A_L (equation 2.17). From equation 2.17 and with the help of this factor it is concluded that for a given magnetic core the inductance of an inductor is proportional to the square of the number of turns.

The relationship between the equivalent magnetic circuit of the figure 2.7 and its corresponding electric circuit is presented in equation 2.18.

$$u_L = \frac{d\Psi}{dt} \qquad i_L = \frac{1}{L} \int u_L dt \tag{2.18}$$

After presenting the general equations of the inductor the loss model of this passive component is discussed in the following. There are two types of losses which are produced by a non-deal inductor. These are the core losses and the winding's copper losses (equation 2.19).

$$P_{L,loss} = P_{L,cu} + P_{L,core} \tag{2.19}$$

2.2.1 Copper Losses

The copper loss itself can be divided into two parts of DC losses and AC losses. The DC component of the losses are calculated using the ohmic resistance of the copper winding and

the average value of the inductor current:

$$P_{\mathrm{L,cu,dc}} = i_{\mathrm{L,dc}}^2 \, R_{\mathrm{L,cu}} \qquad (\text{with} \quad i_{\mathrm{L,dc}} = \frac{1}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}} i_{\mathrm{L}} \, dt), \tag{2.20}$$

in which the ohmic resistance at the room temperature (25 C°) can either be analytically calculated as in equation 2.21, or directly measured with a multimeter.

$$R_{\mathrm{L,cu,0}} = \frac{l_{\mathrm{win}} \, N}{A_{\mathrm{cu}} \, \sigma_{\mathrm{cu}}}. \tag{2.21}$$

In the equation above, σ_{cu} is the specific conductivity of the copper, A_{cu} is the cross section area of the wire, and l_{win} is the average length of one winding turn. The resistance value at the room temperature will then be used to calculate the resistance at any given temperature as follows:

$$R_{\mathrm{L,cu}} = R_{\mathrm{L,cu,0}} \left(1 + \Delta\theta \; \alpha_{\mathrm{cu}}\right). \tag{2.22}$$

In equation 2.22 $\Delta\theta$ is the temperature difference between the winding package and the ambient temperature, and α_{cu} is the temperature coefficient of the copper. The winding temperature is estimated with the temperature of an ideal heat-sink with a constant temperature of a typical value in electric vehicles (according to [57] θ_{hs} =70°C).

After covering the DC part, the AC component of copper losses is discussed in the following. These losses take place in a winding which is excited with an AC current (in this application it is $i_{\mathrm{L,ac}}$). To calculate such losses the so-called skin effect phenomenon should be taken into account. In general for a winding with an AC excitation the current will choose a path with the minimum impedance to flow in. Therefore the high frequency AC current tries to minimize the flowing area exposed by its self-generated magnetic field to decrease the inductance and accordingly the impedance seen by this AC current. Based on this fact the reduced copper area will result in a higher ohmic losses in the wire [4)].

One broadly used parameter to characterize the skin effect is the so-called skin depth δ_{cu}. It is actually a measure which determines the length between the conductor outer surface and a point in the cross section at which the current density is $\frac{1}{e}$ (about 37%) of the value at the surface. The skin depth is dependent on different factors such as the conductor material and the excitation frequency, and can be analytically calculated which is discussed in [58]. Equation 2.23 shows the skin depth in a copper wire for different current frequencies (f_{n}). In this equation the specific conductivity of the copper (σ_{cu}) is a temperature dependent factor which is included

[4)] A common way to decrease the AC power losses is to use litz wire in the winding which is discussed in [56].

in the skin depth evaluation as well.

$$\delta_{\mathrm{cu,f_n}} = \frac{1}{\sqrt{\pi\, f_\mathrm{n}\, \mu_0\, \sigma_\mathrm{cu}}} \tag{2.23}$$

Based on this formula the skin depth in a copper wire with a 50 Hz sinusoidal excitation current ($\delta_{\mathrm{cu,f_{50}}}$) is equal to 8.5 mm. With the help of this measure and the equation 2.23 the skin depth in a copper wire for a given sinusoidal current with the frequency of f_n can be calculated with equation 2.24.

$$\delta_{\mathrm{cu,f_n}} = \sqrt{\frac{50}{f_\mathrm{n}}}\, \delta_{\mathrm{cu,f_{50}}} \tag{2.24}$$

The role of the the skin effect in the inductor application is discussed in [23]. According to this, in the case of an inductor winding wrapped on a magnetic core the high frequency currents flow no longer uniformly through the cross section of the copper, but rather through the inner side of the winding (the current carrying cross section of the copper is shown in figure 2.8 with dark blue color). This is because of the fact, that the reduced cross section of the current-flow towards inner side of the winding will result in a lower effective area enclosed by the magnetic path. Based on equation 2.17 the resulting magnetic path shown with pink hashed lines in figure 2.8 will lead to a smaller overall inductance seen by the high frequency current, which matches with the above mentioned statement about the high frequency AC currents.

In order to calculate the AC copper losses of the winding the current distribution of the winding cross section should be calculated. The standard method to determine the current density in the wire is using **Finite Elements** [59], but in this work an approximation has been made and it has been assumed that the AC current is exponentially distributed through the wire [23].

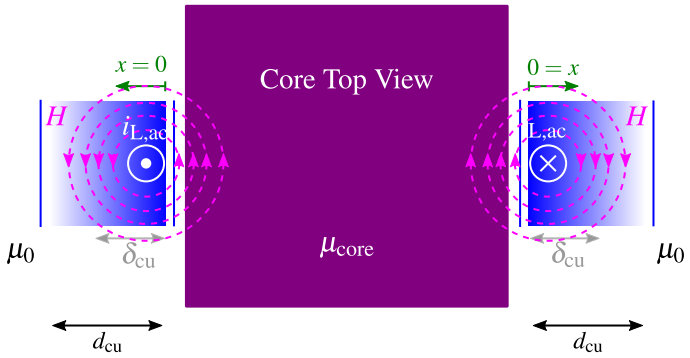

Figure 2.8: Top view of an inductor with magnetic core and the resulting current distribution under consideration of the skin effect

With the help of skin depth definition and the aforementioned current distribution over the winding cross section, the current density can be calculated. This comprehensively discussed in [23] and for the fundamental frequency of the inductor current with the frequency of f_1 (in

the case of a DC-DC converter it is equal to the switching frequency f_{sw}) and the amplitude of $\widetilde{i}_{L,ac,1}$[5)] the effective value of the current density ($J_{L,1}(x)$) over the winding cross section is calculated and shown in equation 2.25. In this equation d_{cu} is the wire diameter and the origin of x axis is on the surface of the winding (figure 2.8).

$$J_{L,1}(x) = \frac{\widetilde{i}_{L,ac,1}}{\sqrt{2}\, d_{cu}\, \delta_{cu,f_1} \left(1 - e^{\frac{-d_{cu}}{\delta_{cu,f_1}}}\right)} e^{\frac{-x}{\delta_{cu,f_1}}} \tag{2.25}$$

With the help of the equation 2.25 the AC power losses of the inductor current fundamental frequency (switching frequency of the converter in this case) is calculated by integrating the loss density function across the wire cross section as shown in equation 2.26.

$$P_{L,cu,ac,1} = \frac{N\, l_{win}\, d_{cu}}{\sigma_{cu}} \int_0^{d_{cu}} J_{L,1}^2(x)\, dx \tag{2.26}$$

According to [23] and by means of equation 2.25 and equation 2.26 the following result is achieved:

$$P_{L,cu,ac,1} = R_{L,cu} \frac{\widetilde{i}_{L,ac,1}^2\, d_{cu} \left(1 - e^{\frac{-2\, d_{cu}}{\delta_{cu,f_1}}}\right)}{4\, \delta_{cu,f_1} \left(1 - e^{\frac{-d_{cu}}{\delta_{cu,f_1}}}\right)^2}. \tag{2.27}$$

The above calculation will be done for all dominant harmonics of the current. For this reason a maximum harmonic order K is defined, at which the amplitude of the current is 5% of the the current amplitude at fundamental frequency ($\widetilde{i}_{L,ac,K} = 0.05\, \widetilde{i}_{L,ac,1}$). Finally based on the superposition principle the total AC ohmic losses are calculated. This computation is presented in equation 2.28.

$$P_{L,cu,ac} = \sum_{n=1}^{K} P_{L,cu,ac,n} \tag{2.28}$$

Figure 2.9 shows the procedure resulted from the equations above to calculate the inductor ohmic losses. The inductor model is implemented in MATLAB as the inductor-class and in the SIMULINK as the inductor-subsystem, and the shown procedure in figure 2.9 is included in the inductor-class and inductor-subsystem.

[5)] To calculate the effective current, the AC current, $i_{L,ac}$, should be decomposed into sinusoidal and cosinusoidal component using Fourier series [60]. The effective value of the AC part of the inductor current at a given frequency is then calculated from the effective values of these two components at each frequency.

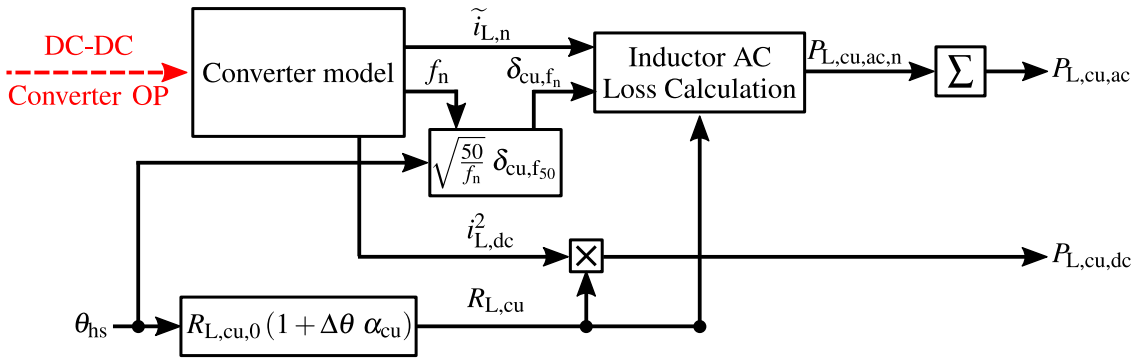

Figure 2.9: Inductor ohmic loss calculation model implemented in MATLAB

Table 2.3 shows the specification of the winding used for the inductor, which includes required inductor parameters needed for ohmic losses calculation of the inductor.

Table 2.3: The winding specification of the inductor used in the DC-DC converter

Description	Designator	Value	Unit
Copper diameter	d_{cu}	4	mm
Copper area	A_{cu}	12.56	mm^2
Number of turns	N	60	
Winding length per turn	l_{win}	130	mm
Copper specific conductivity	σ_{cu}	$5.96 \cdot 10^7$	$\Omega^{-1}.m^{-1}$
Copper temperature coefficient	α_{cu}	0.00404	

2.2.2 Core Losses

As mentioned above the core loss is another component of the inductor losses. There are two phenomena in the magnetic core which lead to power losses inside the core. The first one is the induction of an electric current inside the core (called eddy current) [61], and the second one is the phenomenon of hysteresis in the ferromagnetic materials [62]. These happen only when the magnetic flux is time variable. The amount of the losses is dependent on the core type and amplitude, DC value, frequency , and shape of the alternating flux density.

The so-called eddy current occurs because of the fact that the core's alternating magnetic flux will produce an electric field which accordingly generates electric current loops inside the core due to the Faraday's law of induction (figure 2.10). The magnitude of the current is proportional to the strength of the magnetic flux, changing ratio of magnetic flux, loop area, and electric conductivity of the core σ_{core}. In order to suppress the eddy current, one method is to use pressed iron powder or laminated sheets for the construction of the magnetic core [63]. This will reduce the induced current drastically which then leads to loss reduction. The core used in this work is also a pressed iron powder and therefore the eddy current losses are neglected.

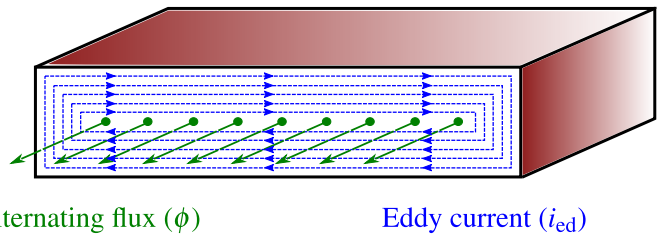

Figure 2.10: Eddy current in the cross section of a non-laminated magnetic core

The second type of the losses related to the core are the hysteresis losses which are due to a phenomenon that occurs in ferromagnetic materials. Generally, in such a material the magnetic flux will not return to zero when the external magnetomotive force is removed [64]. In other words there exists some magnetic flux residue after the external magnetic excitation ($\mathcal{F}$) is set to zero. Consequently the energy of the magnetic field will not transfer back to the external circuit entirely. This energy difference is equal to the energy losses absorbed by the magnetic core. Figure 2.11 shows the magnetization curve (induced magnetic flux density with respect to the magnetic field strength) of a typical ferromagnetic material. This curve is often referred to as the B-H hysteresis loop.

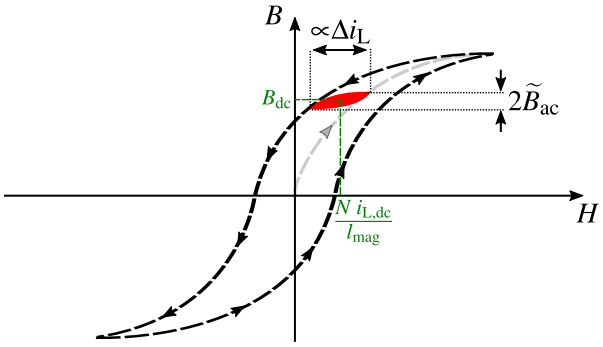

Figure 2.11: B-H Hysteresis loop of a typical ferromagnetic material

The smaller red cycle in the figure 2.11 corresponds to the inductor hysteresis loop for a given operating point in the DC-DC converter application. The hysteresis losses per unit volume of the core (Pv_{core}) are determined empirically for a given sinusoidal alternating flux density with the amplitude of $\widetilde{B}_{\text{ac}}$ and the frequency of f. These losses are expressed in the core's datasheet based on the Steinmetz equation [63] and in the form of three Steinmetz constants (a_{st}, b_{st}, c_{st}) as shown in equations 2.29 and 2.30.

$$\left(\frac{Pv_{\text{L,core}}}{\text{mW}\cdot\text{cm}^{-3}}\right) = a_{\text{st}} \cdot \left(\frac{\widetilde{B}_{\text{ac}}}{\text{T}}\right)^{b_{\text{st}}} \cdot \left(\frac{f}{\text{kHz}}\right)^{c_{\text{st}}} \tag{2.29}$$

$$\left(\frac{P_{\text{L,core}}}{\text{mW}}\right) = \left(\frac{Pv_{\text{L,core}}}{\text{mW}\cdot\text{cm}^{-3}}\right) \cdot 10^{-3} \cdot \left(\frac{V_{\text{core}}}{\text{mm}^3}\right) \tag{2.30}$$

In the equations above, the unit of $Pv_{\text{L,core}}$ is milli-Watt per cubic centimeter (mW.cm^{-3}) and

the frequency and flux density are given in kilo-Hertz and Tesla respectively.

As stated above the Steinmetz equation is only valid for a sinusoidal alternating flux density. In a DC-DC converter with the boost topology, which is the one used in this work, the inductor current waveform is not sinusoidal but an asymmetrical triangular. Consequently equation 2.29 can not be used anymore. Since the hysteresis losses are physically generated by the flux density variation, the Steinmetz equation can be modified for a random periodic flux density with the peak value of $\widetilde{B}_{\mathrm{ac}}$ and the frequency of f_{sw} as follows (discussed in [64] and [65]):

$$\left(\frac{P v_{\mathrm{L,core}}}{\mathrm{mW \cdot cm^{-3}}}\right) = a_{\mathrm{st}} \cdot \left(\frac{f_{\mathrm{eq}}}{\mathrm{kHz}}\right)^{(c_{\mathrm{st}}-1)} \cdot \left(\frac{\widetilde{B}_{\mathrm{ac}}}{\mathrm{T}}\right)^{b_{\mathrm{st}}} \cdot \left(\frac{f_{\mathrm{sw}}}{\mathrm{kHz}}\right), \tag{2.31}$$

in which f_{eq} is defined as the equivalent sinusoidal frequency of the alternating flux density and is calculated as follows [63]:

$$f_{\mathrm{eq}} = \frac{1}{2\,\pi^2\,\widetilde{B}_{\mathrm{ac}}^2} \int_0^{T_{\mathrm{sw}}} \left(\frac{dB}{dt}\right)^2 dt. \tag{2.32}$$

Therefore to calculate the hysteresis losses of the inductor used in the DC-DC converter, the equivalent frequency of the core's varying flux density should be calculated. Figure 2.12 shows the flux density and its derivative inside the magnetic core of a DC-DC converter. These are required for the evaluation of equation 2.32.

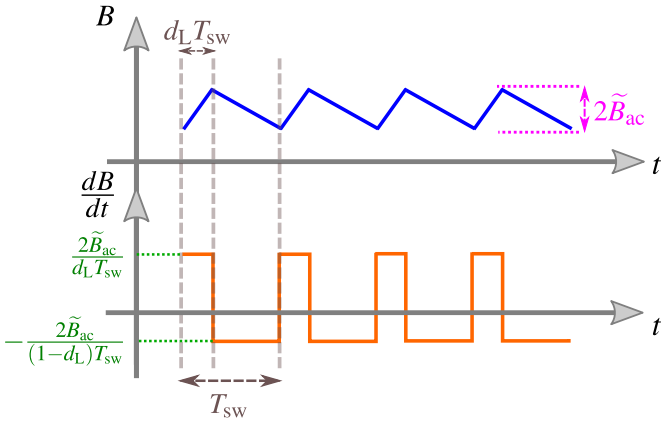

Figure 2.12: Magnetic core's flux density and its derivative at a given DC-DC converter operating point with boost topology

Equation 2.33 presents the calculation of the equivalent frequency of the flux density at a given

DC-DC converter operating point shown in figure 2.12.

$$f_{eq} = \frac{1}{2\,\pi^2\,\widetilde{B}_{ac}^2}\left(\int_0^{d_L T_{sw}}\left(\frac{2\widetilde{B}_{ac}}{d_L\,T_{sw}}\right)^2 dt + \int_{d_L T_{sw}}^{T_{sw}}\left(\frac{2\widetilde{B}_{ac}}{(1-d_L)\,T_{sw}}\right)^2 dt\right) = \frac{2}{\pi^2\,d_L\,(1-d_L)}\cdot f_{sw} \triangleq F_{CF}\cdot f_{sw} \tag{2.33}$$

Figure 2.13 shows the frequency correction factor (F_{CF}) as a function of the converter duty cycle (d_L). It is concluded that the higher the changing rate of the flux density is, the higher the equivalent frequency gets. Consequently very low or very high duty cycles will increase the losses drastically (equation 2.31).

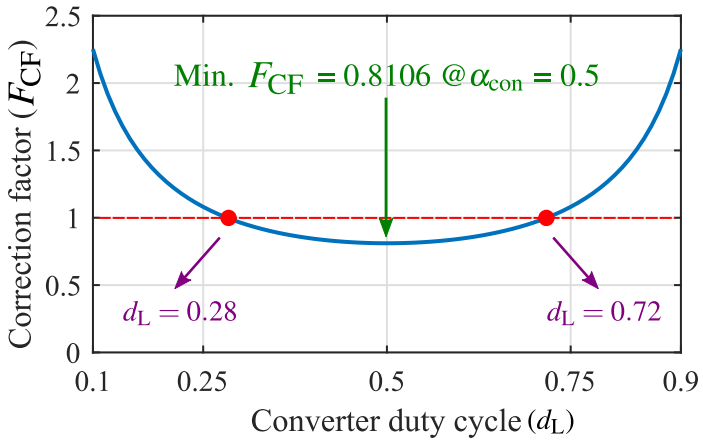

Figure 2.13: Correction factor of the flux density frequency for core losses calculation at different duty cycles

The procedure for the magnetic core losses calculation of the inductor used in the DC-DC converter is also included in the MATLAB inductor-class, and SIMULINK inductor-subsystem. This procedure is shown in figure 2.14, and it should be mentioned that in this computation, equation 2.13 has been used to calculate the amount of flux density ripple based on the inductor current ripple.

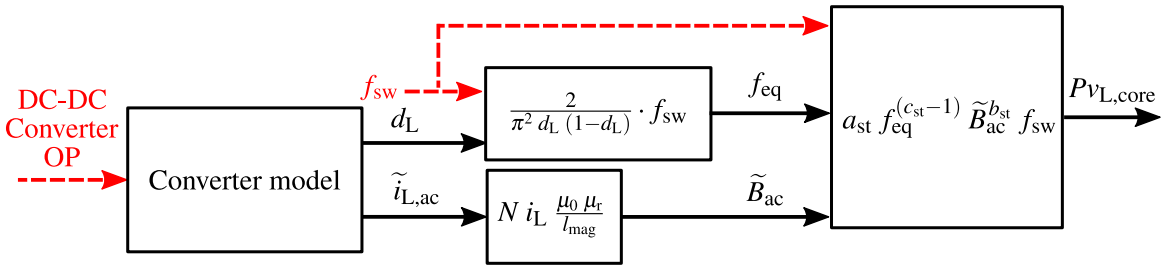

Figure 2.14: Magnetic core loss calculation model implemented in MATLAB

The following table shows the specification of the magnetic core used for the inductor. These parameters are included in the the model shown in figure 2.14.

Table 2.4: Core specification (MAGNETICS *58338A2*) of the inductor used in DC-DC converter

Description	Designator	Value	Unit
Relative permeability	μ_r	40	1
Outer diameter	D_{out}	132.56	mm
Inner diameter	D_{inn}	78.59	mm
Height	h_{core}	25.4	mm
First steinmetz constant	a_{st}	492.31	1
Second steinmetz constant	b_{st}	2.218	1
Third steinmetz constant	c_{st}	1.240	1
Average magnetic path length	l_{mag}	324.3	mm
Core volume	V_{core}	219	cm^3
Weight	m_{core}	1.73	kg

2.3 Power Transistor

Another component used in DC-DC converters and DC-AC inverters is the power transistor which is presented in this section. After introducing different types of these semiconductors, the static and dynamic characteristic of them will be discussed. Power semiconductors are the core components in the design and construction of the power converters, and because they produce the main part of the converter's losses, choosing the proper power semiconductor technology is an essential task for the final design of the converter. There are mainly two types of semiconductor technologies: unipolar power transistors and bipolar power transistors.

In unipolar semiconductors only one type of charge carriers (electrons in n-channel devices or holes in p-channel devices) are taking part in the current flow. Metal Oxide Semiconductor Field Effect Transistors (MOSFET) and Junction Field Effect Transistors (JFET) are two major types of this family. The forward voltage drop of MOSFETs and JFETs do have predominantly ohmic characteristic, and the reason is the low concentration of minority charge carrier in the drift region of the field effect transistor [66]. As it will be discussed later on, in order to design the unipolar transistors for higher breakdown voltages the only way is to increase the thickness of drift region (the epitaxial layer) which will increase their on-resistance and consequently results in higher conduction losses in comparison with bipolar semiconductor technologies [67]. On the other hand since there is only one type of charge carrier in the drift region there is no need for the removal (construction) of minority carriers during switching off (switching on). This will lead to shorter switching times and lower switching losses compared to bipolar devices. In the other words unipolar semiconductors are appropriate for converters with high switching frequencies [68].

The second type of power transistors are bipolar devices. In this semiconductor technology, both types of charge carriers participate in current flow. Insulated Gate Bipolar Transistor (IGBT) is one of the important power transistors of this group. In contrast to FETs, the drift region resistance of the IGBTs is drastically reduced by the relatively high concentration of the injected minority carrier during on-state ([69]). IGBTs are suitable for scaling up of the blocking voltage, since the electric field can be formed in a way that for a constant required blocking voltage, a thinner drift region is needed in comparison to their unipolar counterparts. Consequently, the IGBTs benefit from a lower on-resistance of the drift region for higher voltages (in these transistor types, the threshold voltage of the corresponding PN junction should also be included in their overall voltage drop during on-state[6)] as discussed in [66]). On the other hand, with respect to the fact that removing the injected minority charge carriers from drift region during switch-off process[7)] leads to a longer turn-off time, the bipolar transistors are not appropriate for higher switching frequency applications.

Between different semiconductor devices, IGBTs and MOSFETs are two possible candidates for the DC-DC and DC-AC converters in the drivetrain application [70]. For the given application, based on the operating voltage and switching frequency, one of the aforementioned semiconductors can be selected as illustrated in figure 2.15.

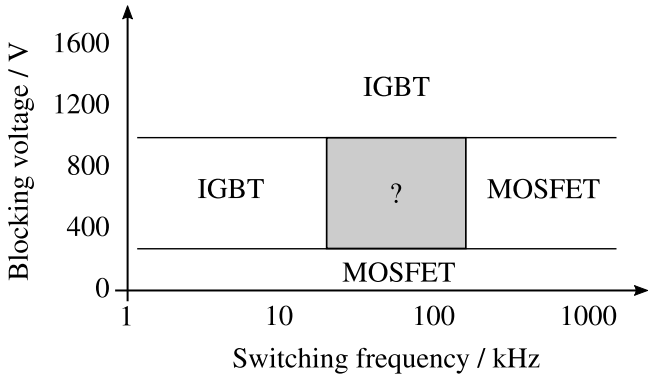

Figure 2.15: Typical application area for IGBTs and MOSFETs (based on [8], from [9])

In this work, IGBTs are selected as the power transistors due to the voltage class of the electrical machine and in view of the relatively low switching frequency of the DC-DC converter and inverter. For voltage converter topologies with soft-switching capabilities (out of scope of this work) MOSFETs are the preferable devices as discussed in [71]. In the following, the operating principle of the IGBT is presented in detail and the power dissipation and the way it is modeled and included in the simulation are discussed. First, however, for the sake of completeness and to illustrate the structural differences between a unipolar and a bipolar transistor, the structure and properties of the power MOSFET is briefly presented.

[6)] As it will be discussed in the IGBT section the collector-emitter voltage during on-state is determined by the voltage drop between the p^+ collector and n^- drift region.

[7)] Minority carriers can mainly be removed from the drift region by recombination, and the current flow during this interval is called tail current.

2.3.1 Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

Figure 2.16 (a) shows the structure of an n-channel MOSFET [72]. The MOSFET is a voltage-controlled unipolar semiconductor device which has three terminals: Gate (G), Drain (D), and Source (S). In power electronic applications n-channel MOSFETs are more common among unipolar devices. The reason for that is the higher mobility of electrons in comparison with holes in p-channel MOSFETs. The higher mobility leads to lower switch-on resistance of this type of MOSFETs. In an n-channel MOSFET by applying a positive voltage between gate and source (u_{GS}), a channel will be created beneath the gate plate in the p^+-well region, and through this channel electrons can freely flow toward the drain or source terminals, according to the external applied voltage (u_{GS}).

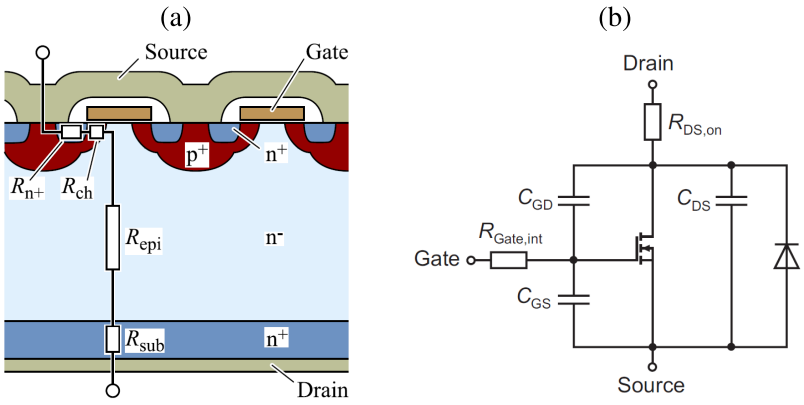

Figure 2.16: Physical structure of (a) an n-channel MOSFET and (b) equivalent model (from [9])

The equivalent model of a non-ideal MOSFET is shown in figure 2.16 (b), which consists of an ideal MOSFET as well as a few capacitors and resistors. In this model the drain-source capacitor (C_{DS}) replicates the capacitance of n^--drift p^+-well junction, which evolves from the space-charge expansion resulting from the u_{DS} voltage. Based on [73] this capacity is dependent on the MOSFET cheap-area and drain-source voltage (equation 2.34).

$$C_{DS} \propto \frac{A_{chip}}{\sqrt{u_{DS}}} \tag{2.34}$$

The gate-drain capacitance (C_{GD}) which is also known as miller-capacitance, is originated from the overlap of the gate plate and n^--drift region. It is therefore made up of a constant capacitance of the oxide layer underneath the gate (determined by the thickness of the silicon dioxide) in series with the voltage dependent (u_{DS}) capacitance of the depletion layer in the n^--drift region. Last but not least, there exists a gate-source capacitance (C_{GS}), which is resulting from the overlap of the gate and source metallizations.

Regarding the capacitors, the semiconductor manufacturers use mostly another parameters to quantify these capacitances. Input capacitance (C_{iss}), reverse transfer capacitance (C_{rss}), and output capacitance (C_{oss}) are the voltage dependent parameters which are declared in the most

MOSFET datasheets [74]. The relationship between these parameters and the above mentioned gate-source, gate-drain, and drain-source capacitances are shown in the following equations.

$$C_{\text{iss}} = C_{\text{GS}} + C_{\text{GD}} \tag{2.35}$$
$$C_{\text{rss}} = C_{\text{GD}} \tag{2.36}$$
$$C_{\text{oss}} = C_{\text{GD}} + C_{\text{DS}} \tag{2.37}$$

It is said that an n-channel MOSFET is in the blocking state if in the absence of u_{GS} a positive voltage is applied between drain and source ($u_{\text{DS}} > 0$). In this state if a positive voltage is applied between gate and source terminals, as soon as u_{GS} becomes larger than the threshold voltage (u_{th}) of the transistor, an inversion layer (n-conductive channel) starts expanding inside the p^+-well region underneath the gate terminal and the MOSFET switches into the conduction state.

It is worth to mention that if the the applied drain-source voltage gets negative, then the current can flow through the positively biased body diode of the the MOSFET (p^+-n^- junction in figure 2.16) regardless of u_{GS}. But in order to decrease the voltage drop over the transistor, it will be driven with a positive gate-source voltage. This kind of operating mode is called the synchronous rectification mode [66], in which the electrons can flow from the drain to source through the channel.

In the switch-on state of the n-channel MOSFET, the electrons can flow freely between the source and drain terminals. On their way electrons should go through the following regions (figure 2.16): n^+-source, conductive channel inside p^+-well, n^--drift (also know as epitaxy layer), and n^+-substrate. According to this, the drain to source resistance during conduction state (represented by $R_{\text{DS,on}}$) is calculated as follows:

$$R_{\text{DS,on}} = R_{\text{n}^+} + R_{\text{ch}} + R_{\text{epi}} + R_{\text{sub}}. \tag{2.38}$$

The proportion of each one of the above mentioned resistances to the total $R_{\text{DS,on}}$ depends mostley on the breakdown voltage (U_{BR}), for which the MOSFET is designed [75]. In order to realize a higher breakdown voltage the thickness of the n^--drift region should be increased. This will result in higher R_{epi} which consequently leads to the fact that in MOSFETs with higher U_{BR}, the major part of the $R_{\text{DS,on}}$ is the the resistance of the epitaxy layer. As an example the ratios of R_{ch} and R_{epi} to $R_{\text{DS,on}}$ in a 30 V MOSFET is approx. 28% and 29%, and for a 600 V MOSFET 1.5% and 95.6% respectively [66]. The increase of MOSFET drift region resistance with increasing breakdown voltages is derived in [75] and is presented in the following equation.

$$R_{\text{epi}} \cdot A_{\text{chip}} = 8.3 \cdot 10^{-9} \cdot \left(\frac{U_{\text{BR}}}{V}\right)^{2.5} \cdot \Omega \cdot \text{cm}^2 \tag{2.39}$$

In the other words, equation 2.39 shows that the conduction losses of the MOSFET increase with the increasing breakdown voltage more than quadratic. Therefore conventional MOSFETs are mostly limited to the breakdown voltages of around 600 V. There are some technological improvements carried out on the MOSFET structure (figure 2.17) which help to overcome the breakdown voltage limitation of the MOSFET [70, 66].

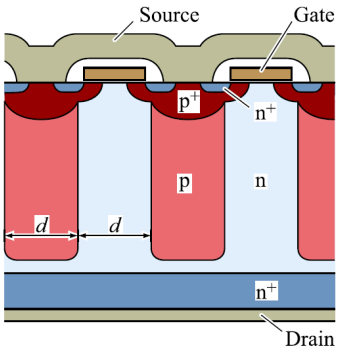

Figure 2.17: The structure of a super-junction MOSFET (from [9])

This kind of modified MOSFETs are called super-junction MOSFETs [76]. The main advantage of these power semiconductors is their lower $R_{DS,on}$ (lower conduction losses), which results from the possibility of doping the n-region much higher than their conventional counterparts. This is achieved by inserting p-doped columns with the same doping as the n-doped region inside the epitaxy layer, as shown in figure 2.17. Using this new structure, the charge carrier distribution in the blocking state will result in a nearly constant electric field strength over the entire drift region, which is in contrast to the decaying electric field of the conventional MOSFET in the epitaxial region. Since the reverse bias voltage is the result of integrating the electric field strength across the transistor thickness, super junction MOSFETs have a higher breakdown voltage than conventional MOSFETs. According to [76], for super-junction MOSFETs the relationship between the switch-on resistance and breakdown voltage is changed from the equation 2.39 to the equation 2.40.

$$R_{epi} \cdot A_{chip} = 1.98 \cdot 10^{-6} \cdot \left(\frac{d}{\mu m}\right)^{1.25} \left(\frac{U_{BR}}{V}\right) \cdot \Omega \cdot cm^2 \tag{2.40}$$

In the equation above, d is a constant which relates to the geometrical construction of the super-junction MOSFET. This equation shows that using the super-junction technology results in overcoming the so-called *Silicon Limit* of the conventional MOSFETs [77]. Despite this advantage of the super-junction MOSFETs, they are not the right choice for the use in bridge pairs applications, and accordingly not suitable for the inverter and DC-DC converter implementation in this work. This is due to the switch-off transient of the body diode of the super-junction MOSFET, where the relatively large area of the PN-junction in the epitaxy layer and the evenly doped p-region and n-region lead to an abrupt current interruption during switch-off ([9]). The rapidly changing current, together with the parasitic inductances at the terminals and in the layout, lead to high over voltages in the bridge switching nodes.

Figure 2.18 shows the voltage-current characteristic of a MOSFET. In the blocking state ($u_{GS} = 0$) the operating point is somewhere on the positive area of the horizontal axis (depending on the value of u_{DS}). In this state the current which flows through the transistor is called leakage current and is very small and negligible. The so-called switch-on state of the MOSFET is located in the ohmic-region shown in figure 2.18. The MOSFET operates in the ohmic-region if u_{GS} is large enough (for the given drain-source current, $u_{GS,min}$ is determined based on the MOSFET transconductance characteristic) so that the ratio of the forward voltage to the drain-source current is determined by the $R_{DS,on}$ mentioned above.

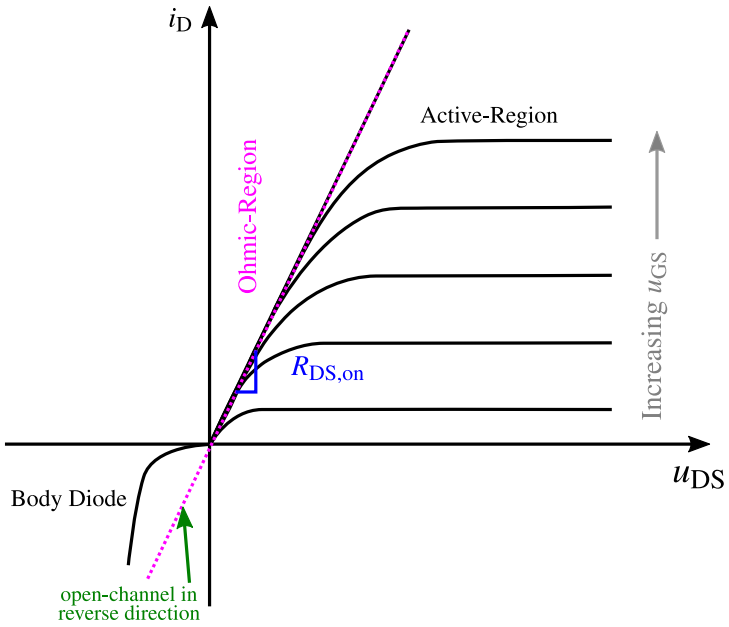

Figure 2.18: voltage-current characteristic of a MOSFET

As it will be discussed in chapter 5, in this work the power transistors are utilized to implement a DC-AC converter for traction application, and drive an inverter-fed machine with line-line voltage level of 400 V. In [31], two different drivetrains with different semiconductor types (silicon based MOSFET and IGBT) and two different DC-Link voltages (u_{DC} =48 V and u_{DC} =400 V) are compared with each other in terms of power losses. It has then been concluded that using Si-IGBT power transistors for the DC-Link voltage of 400 V will result in the highest efficiency among the different designs. This is due to the fact that the $R_{DS,on}$ of silicon based MOSFETs are increased with increasing blocking voltage level of the device, therefore the Si-MOSFET are less appropriate for higher voltage levels.

Utilizing MOSFETs with wide band gap technology, such as silicon carbide MOSFET, can be considered as a feasible alternative for the execution of the converter. Nonetheless, due to the lower cost associated with IGBT power transistors in comparison to SiC-MOSFETs, and as indicated in [78], the inability to fully utilize the benefits of the wide band gap technology in the context of the designated machine voltage of 400 V, Si-IGBTs have been utilized for the analysis presented in this study. This brings the discussion of MOSFETs to an end. In the following, the focus will be on IGBTs to discuss the operating principle in more detail and develop a proper model for them.

2.3.2 Insulated Gate Bipolar Transistor (IGBT)

Two major types of IGBTs are Punch-Through (PT) IGBT and Non-Punch-Through (NPT) IGBT, which their cross section are shown in figure 2.19. The structure of an NPT-IGBT (figure 2.19 (b)) is very similar to the structure of an n-channel MOSFET and the only difference is the additional p^+ layer at the collector terminal, which forms a PNP bipolar transistor in the collector side of the semiconductor device. The IGBT can therefore be modeled with a bipolar transistor (BJT) cascaded with a MOSFET as presented in [66] (figure 2.19 (c)). Based on this model, the IGBT possesses the output characteristic of a BJT, controlled with the gate-emitter voltage instead of base current in the conventional bipolar transistor.

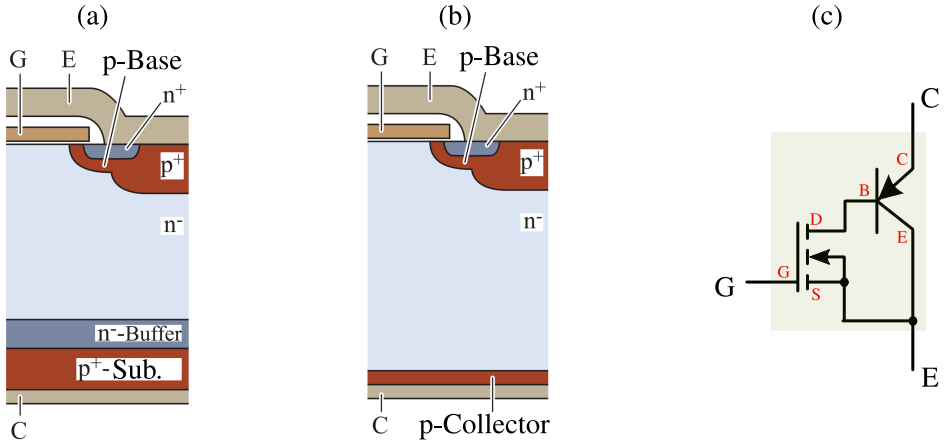

Figure 2.19: Physical structure of (a) PT-IGBT and (b) NPT-IGBT (from [9]) and (c) the equivalent model consisting cascaded MOSFET and BJT

The difference of the Punch-Through IGBT (figure 2.19 (a)) and the NPT-IGBT is in the very low-doped drift region (n^-) as well as the additional buffer layer on top of the p^+-collector. This will ensure a very small drop of the electric field strength through the drift region in the blocking state. This means that for the same maximum blocking voltage the PT-IGBT has a thinner drift region in comparison to the NPT alternative. This will consequently lead a lower saturation voltage of the NPT-IGBTs in on-state. Figure 2.20 shows the output characteristic of an IGBT. Based on the bipolar operation of the device and the high concentration of the injected minority carriers (holes) in the drift region, the resistance of this layer is drastically reduced, and during the switch-on state the voltage drop of the device will mostly be determined by the voltage drop of the forward biased PN-junction between the collector and drift region. The entire voltage drop of the IGBT can then be calculated with the help of equation 2.41.

$$u_{CE} = U_{0,CE} + R_{CE,on} \cdot i_C \tag{2.41}$$

Similar to the MOSFET, the conduction losses of the IGBT are derived from the forward voltage drop (equation 2.41). The result is shown in equation 2.42.

$$P_{IGBT,cond} = u_{CE} \cdot i_C = U_{0,CE} \cdot i_C + R_{CE,on} \cdot i_C^2. \tag{2.42}$$

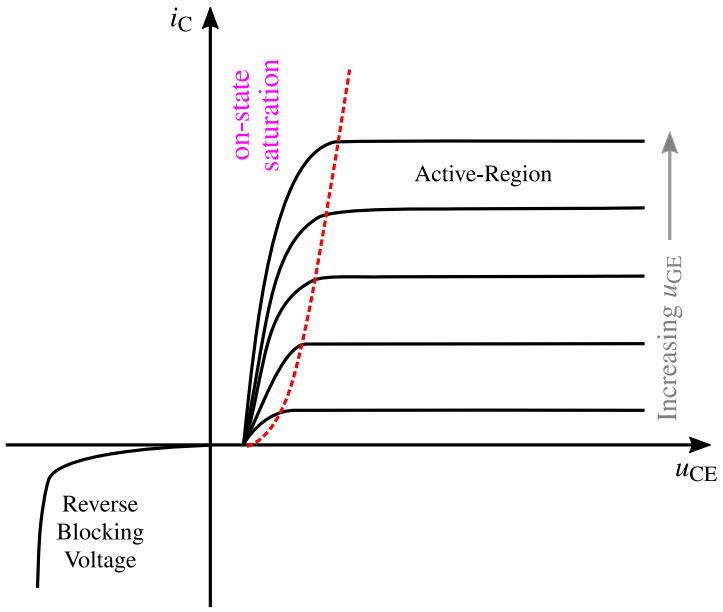

Figure 2.20: voltage-current characteristic of an IGBT

The conduction losses are calculated in MATLAB using the implemented IGBT-class (subsystem) which includes the temperature dependent characteristic of the IGBT in the form of look-up-tables. In this work, the power electronic module form Infineon (HybridPACK 2 for the multiphase DC-DC converter) is used for the test setup, which consist of three half-bridges with high-side and low-side IGBT and anti-parallel diode. Figure 2.21 shows the voltage-current characteristics of the IGBT and anti-parallel diode, from which the parameters for the equation 2.42 are extracted (for a given temperature), and the conduction power losses are calculated.

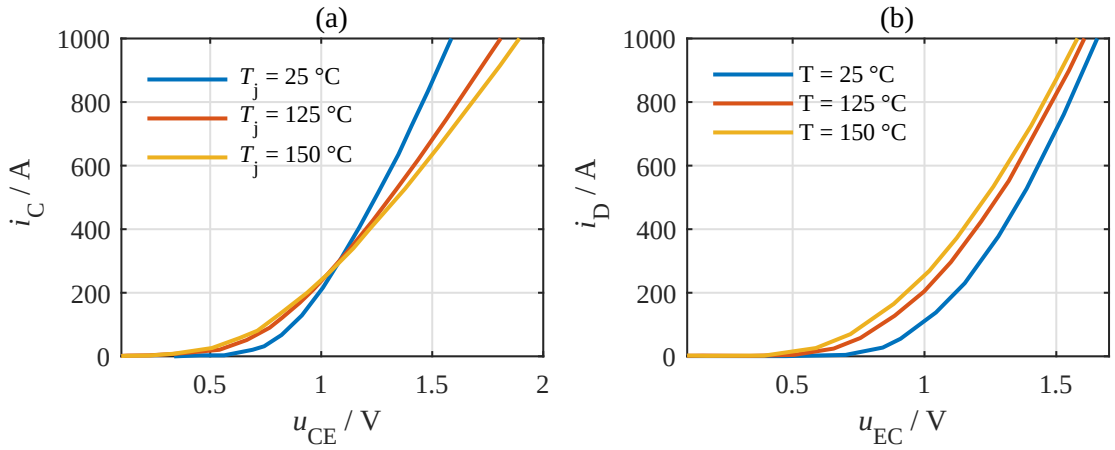

Figure 2.21: *"FS800R07A2E3"* IGBT module of HybridPACK 2 characteristic (a) output characteristic of the IGBT (b) output characteristic of the anti-paralleled diode (extracted from [10])

To investigate the switching behavior of the IGBT, the test circuit shown in figure 2.22 is used. This circuit consists of a very large pure inductive load ($L \to \infty$), a free-wheeling diode, and a switching IGBT is used for the analysis.

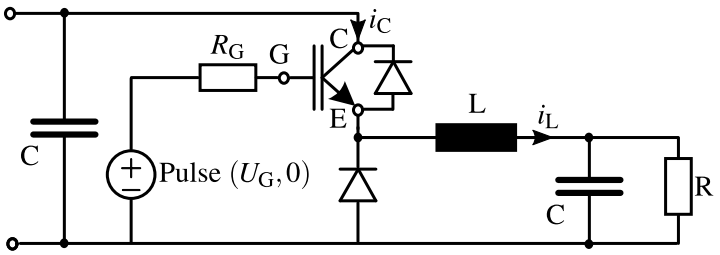

Figure 2.22: Switching test circuit for the IGBT with an inductive load

Figure 2.23 shows the switching-on behavior of the IGBT. As discussed in the beginning of this section, the IGBT can be modeled with a BJT cascaded with a MOSFET (figure 2.19 (c)). The switching-on process starts by applying a positive voltage between the gate and emitter of the IGBT. Once the gate-source voltage of the internal MOSFET exceeds the threshold voltage, the drain-source current of the internal MOSFET starts increasing which is resulting in the rise of the base current of the internal BJT. Accordingly, the collector current of the IGBT starts growing and at t_1 the entire diode current is flowing through the IGBT.

As shown in figure 2.23 after t_1 time-stamp i_C increases further. This is because of the fact that until this point the current was flowing through a bipolar device (the diode in the circuit of figure 2.22), for which the aforementioned stored minority carriers should be removed from both sides of PN-junction. This process is called reverse recovery and the peak value of this additional current is called the maximum reverse recovery current (I_{RRM}) which depends on the reverse recovery charge (Q_{RR}) and the decreasing rate of the diode current. After this process, the blocking voltage over the diode starts to build up at t_2, and the IGBT collector-emitter voltage decreases. At t_3 the switching-on process ends and the voltage drop over the IGBT is determined by equation 2.41.

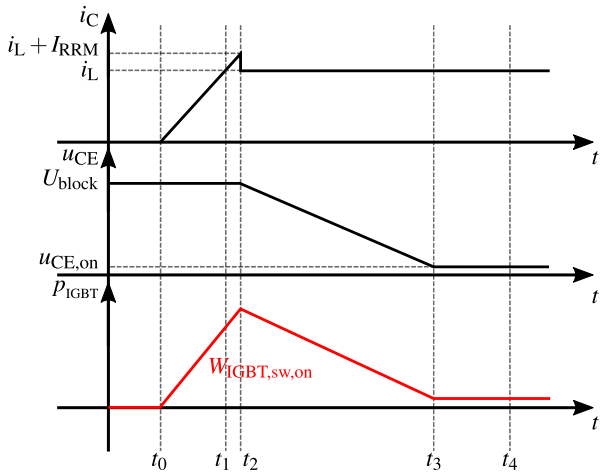

Figure 2.23: Switching-on behavior of an IGBT under the assumption of switching an inductive load

Figure 2.24 shows the voltage and current waveforms of the IGBT during switching-off time interval. It can be seen that after the time that the emitter-collector voltage is fully built up, the

collector current starts falling. After the initial abrupt fall of the collector current there is a point in the waveform (t_3) at which the change rate of the current reduces distinctly and the reason for this rate change is clarified in the following.

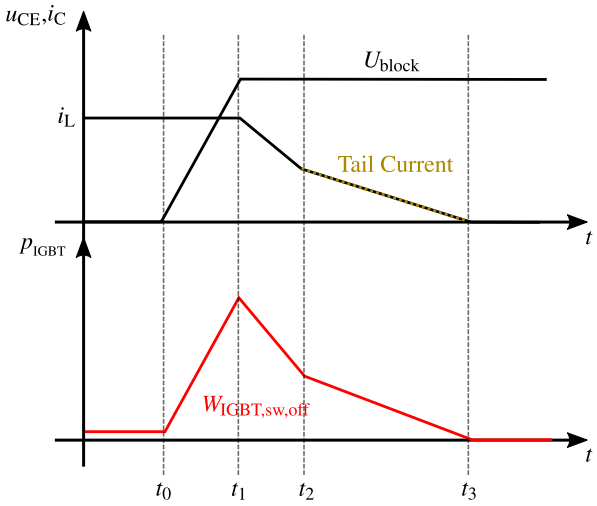

Figure 2.24: Switching-off behavior of an IGBT under the assumption of switching an inductive load

During the switching-off process and at the beginning of the current fall period, the minority carriers in the p^+-collector region (electrons) are quickly swept out to the external circuit, while the depletion regions are expanded into the drift region. As a result the minority carriers in the drift region (holes) will be trapped there, and can not flow out to the external circuit. These carriers can then only be removed from the drift region through recombination ([66]), and the speed of this process is dependent on the minority carrier lifetime. Since flowing the tail current is happening during the time at which the entire blocking voltage is available on the device, the power losses originated from the tail current increase the IGBT switching losses in comparison to MOSFET. There are two typical methods to reduce the duration of the tail current. One of them is to decrease the amount of minority carriers injected from the collector into the drift region, and the other method is to reduce the lifetime of these minority carriers [77]. However both of these techniques cause a rise in on-state voltage drop which will increas the conduction losses of the device. This is the reason why the IGBTs are only appropriate for the applications with switching frequencies lower than about 50 kHz [79].

The switching-on and switching-off energy losses of the IGBT power transistors as well as the reverse-recovery energy losses of their anti-parallel diode are generally available in the data sheet provided by the manufacturer. Figure 2.25 shows the temperature dependent switching energy losses and reverse-recovery energy losses of the HybridPACK 2 IGBT-module (made by Infineon) for a given collector-emitter voltage U_{ref}. These energy losses are included as LUTs in the IGBT-class (subsystem) which is implemented in MATLAB (Simulink). With the help of these look-up-tables and based on the temperature and current, the switching energy losses are calculated. Finally the switching power losses of the IGBT and its anti-parallel diode are calculated as shown in equations 2.43 and 2.44 respectively.

$$P_{\mathrm{IGBT,sw}} = f_{\mathrm{sw}} \cdot (W_{\mathrm{IGBT,sw,on}} + W_{\mathrm{IGBT,sw,off}}) \cdot \frac{U_{\mathrm{block}}}{U_{\mathrm{ref}}}. \tag{2.43}$$

$$P_{\mathrm{D,RRM}} = f_{\mathrm{sw}} \cdot (W_{\mathrm{D,RRM}}) \cdot \frac{U_{\mathrm{block}}}{U_{\mathrm{ref}}}. \tag{2.44}$$

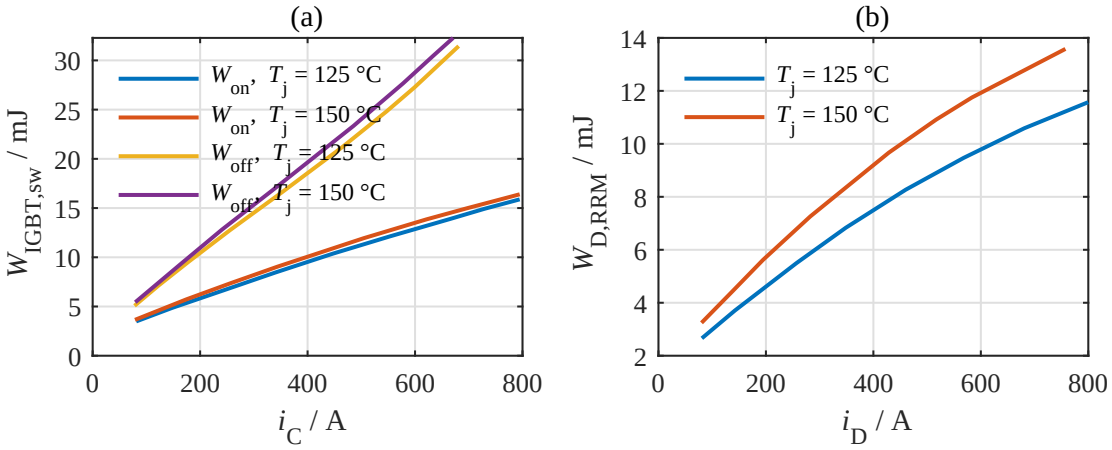

Figure 2.25: *"FS800R07A2E3"* IGBT module HybridPACK 2 power losses for the reference test voltage of $U_{\mathrm{ref}} = 300$ V and $U_{\mathrm{G}} = 15$ V (a) switching on and switching off losses of the IGBT with $R_{\mathrm{G,on}} = 1.8\Omega$ and $R_{\mathrm{G,off}} = 0.75\Omega$ (b) reverse recovery losses with $R_{\mathrm{G,on}} = 1.8\Omega$ (extracted from [10])

As shown in equations 2.43 and 2.44, the energy losses extracted from the LUTs should be multiplied with the ratio of the actual blocking voltage to the reference blocking voltage (U_{ref}) used for energy losses measurements. The linearity of the IGBT switching losses with respect to its blocking voltage is discussed in [80]. Figure 2.26 shows one measurement example from [11]. As it can be seen in this figure, the total switching losses of the IGBT is changing from 4.65 mJ to 9.66 mJ by doubling the collector-emitter blocking voltage from 400 V to 800 V.

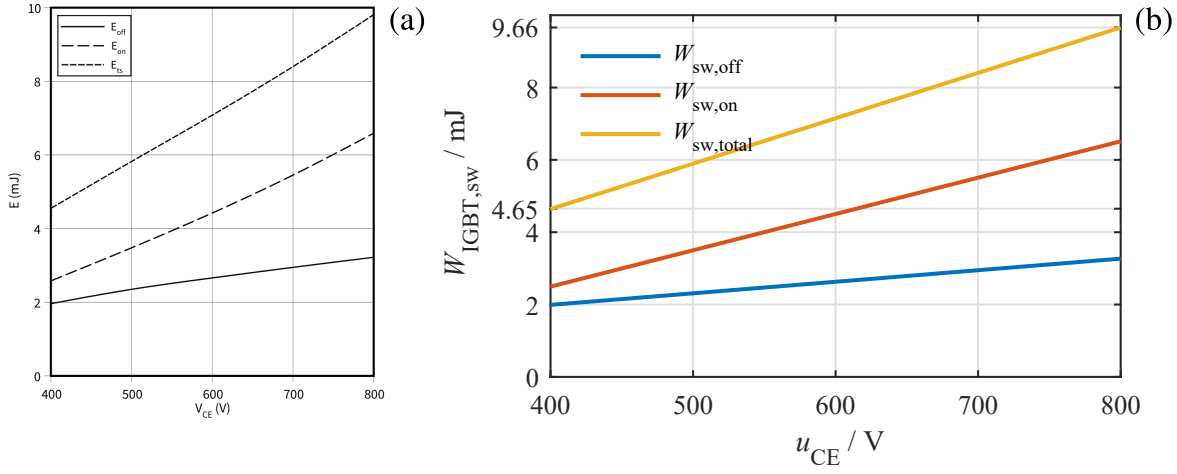

Figure 2.26: *"IKW40N120H3"* IGBT power losses over collector-emitter voltage with $I_{\mathrm{D}} = 40$ A, $U_{\mathrm{G}} = 15$ V, and $R_{\mathrm{G}} = 12\Omega$ (from [11], (a) original picture, (b) extracted picture)

2.3.3 Thermal Model

In this section the utilized thermal model is presented, which will be used in the temperature dependent power losses evaluation of the power transistors. In order to develop this model a typical packaging of the semiconductor module will be taken into account in the first place. Figure 2.27 shows the cross section of the of the HybridPACK 2 IGBT-module mounted on a so-called pin fin water-cooled base plate.

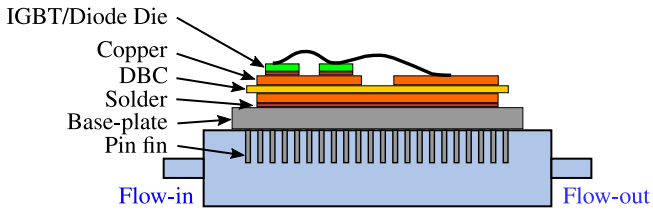

Figure 2.27: HybridPACK 2 IGBT-module cross section of the module mounted on a so-called pin fin water-cooled base plate

According to this setup, the generated heat at transistor (or diode) junction will be transferred to the water-cooled heat-sink by flowing through different layers such as Si-chip, solder, substrate, and base-plate. Equation 2.45 shows the relationship between the junction to fluid temperature difference ($\theta_J - \theta_F$) and the transistor (or diode) power losses. In this equation $R_{th,JF}$ is the so-called thermal resistance between the junction and the fluid, and is determined based on the heat conductivity capability of the materials used in each layer.

$$\theta_J - \theta_F = R_{th,JF} \cdot P_{loss} \tag{2.45}$$

It should be noted that the equation above is only valid for stationary state. This is because of the fact, that the physical layers shown in figure 2.27 have another thermal property which is called the thermal capacitance. This is a factor which is related to the actual heat storage capability of the material [81]. These thermal capacitances, together with the aforementioned thermal resistances of the various layers, form a thermal network that gives the system a certain temperature dynamic over time. The thermal equivalent circuit of the mounted transistors (or diodes) in a given package can be provided using different modeling methods [82], which are discussed in the following. With the help of this equivalent circuit the thermal impedance of the dissipation path is determined, and finally the transient behavior of the junction temperature will be calculated.

The first modeling approach is using the so-called continued-fraction thermal model (also known as Cauer-model), which replicates the actual physical layer stacking of the mounted transistor in the package. Accordingly, in the equivalent circuit of this thermal model each layer does have a given thermal resistance (e.g. $R_{th,Si}$) as well as a thermal capacity (e.g. $C_{th,Si}$). Figure 2.28 shows the Cauer equivalent circuit of a power transistor module, with which for the given power losses the junction temperature can be calculated. This model requires detailed

knowledge about the material characteristics of the individual layers, and therefore the correct mapping of the thermal spreading is very sophisticated [83].

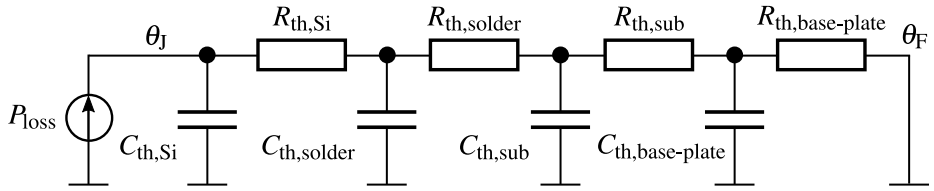

Figure 2.28: Continued-fraction thermal model (Cauer-model) of the transistor

The second method of the modeling is called the partial-fraction thermal model (also known as Foster-model). Figure 2.29 shows the equivalent circuit of transistor using the Foster-model, which is broadly used by the module manufacturers. Based on the Foster-model, the nodes do not have physical replica, and the RC elements shown in figure 2.29 are weighted in a way that the junction temperature does have a good match with the heat-up and cooling curves measured after the manufacturing process.

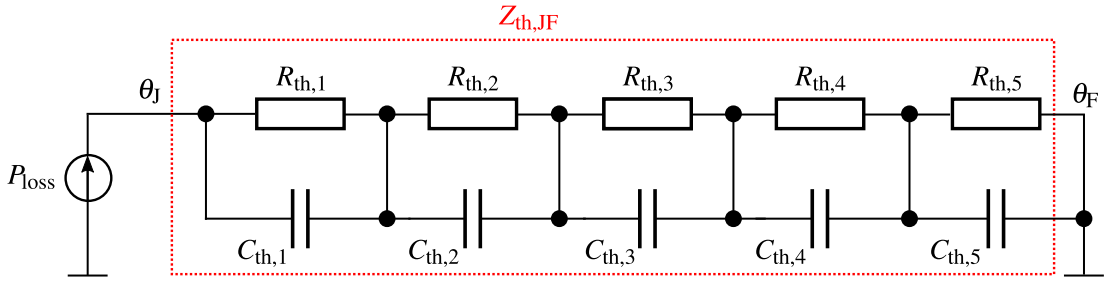

Figure 2.29: Partial-fraction thermal model (Foster-model) of the transistor (5^{th} order)

The transient behavior of the junction temperature can then be calculated with the help of the time constants resulting from the equivalent thermal resistances and capacitances shown in figure 2.29. The junction temperature unit step response over the course of time is calculated using the modified version of the equation 2.45 as shown in the following.

$$\theta_{\text{JF}}(t)\Big|_{P_{\text{loss}}=1} = \sum_{i=1}^{n} R_{\text{th,i}} \cdot \left(1 - e^{\frac{-t}{\tau_{\text{th,i}}}}\right) \; ; \qquad \text{with} \quad \tau_{\text{th,i}} = R_{\text{th,i}} \cdot C_{\text{th,i}} \tag{2.46}$$

In the data sheets of the module manufacturers, the temperature profile resulting from the unit step response of the system (transient temperate over the course of time with the input power loss of $P_{\text{loss}} = 1\text{W}$) is called the transient thermal impedance ($Z_{\text{th,JF}}$). Figure 2.30 shows the transient thermal impedance of the IGBT and anti-parallel diode used in HybridPACK 2 module with a pin fin heat-sink cooling system and 10 dm^3/min flow rate. With the help of this heating curve the 5^{th} order foster model thermal quantities, namely the thermal resistances and time constants, can be calculated. Table 2.5 presents these parameters which are used to estimate the transient thermal impedance. These thermal parameters are also included in the transistor-class properties and SIMULINK-subsystem described in previous subsections (IGBT and MOSFET),

and they will be used in the equivalent circuit of figure 2.29, with which the junction temperature is calculated.

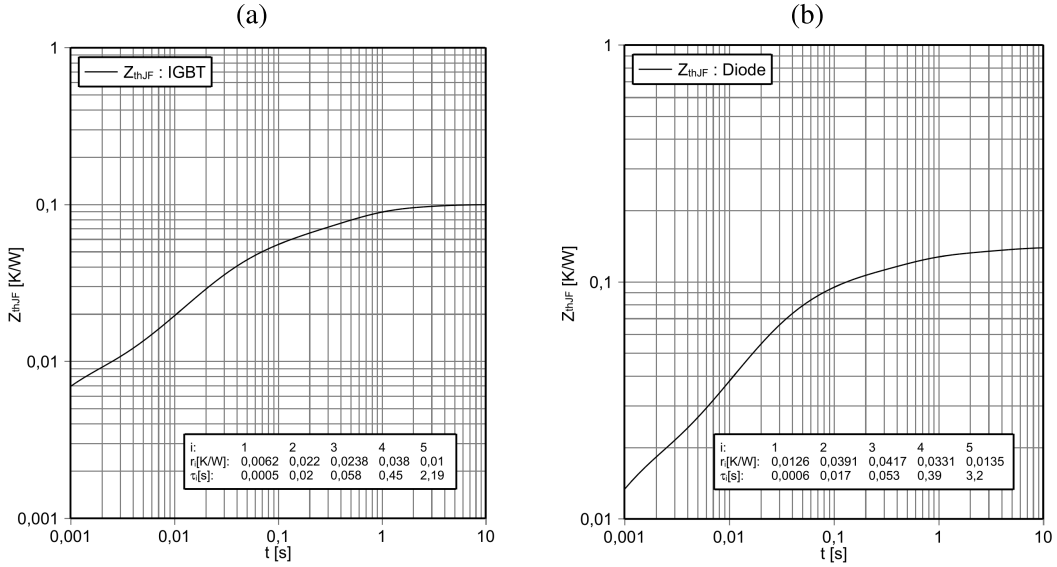

Figure 2.30: Transient thermal impedance of the HybridPACK 2 (a) IGBT and (b) Diode for the given flow rate of 10 dm^3/min with pin fin heat-sink (from [10])

Table 2.5: 5^{th} order foster model thermal parameters for IGBTs and anti-parallel diodes of HybridPACK 2 module with pin fin cooling system and the flow rate of 10 dm^3/min (from [10])

i	1	2	3	4	5
$R_{\mathrm{th,T,i}}/\mathrm{K}\cdot\mathrm{W}^{-1}$	0.0062	0.022	0.0238	0.038	0.01
$\tau_{\mathrm{th,T,i}}/\mathrm{s}$	0.0005	0.02	0.058	0.45	2.19
$R_{\mathrm{th,D,i}}/\mathrm{K}\cdot\mathrm{W}^{-1}$	0.0126	0.0391	0.0417	0.0331	0.0135
$\tau_{\mathrm{th,D,i}}/\mathrm{s}$	0.0006	0.017	0.053	0.39	3.2

As shown in previous subsections, different parameters of the power transistors such as the voltage-current characteristics and switching energy losses are implemented in the corresponding class or subsystem as temperature dependent look-up-tables. With the help of the above described thermal model of the transistor and by means of equation 2.46, the actual junction temperature is calculated based on the power losses extracted from the LUTs (for the temperature input of the LUTs, the junction temperature of the previous time sample is used).

Figure 2.31 shows the implemented procedure to calculate the temperature dependent power losses of the transistors. It should be mentioned that in the evaluation of the junction temperature, it has been assumed that the instantaneous value of the power losses during one switching period is constant, and is equal to the average value of the switching losses plus conduction losses during that period.

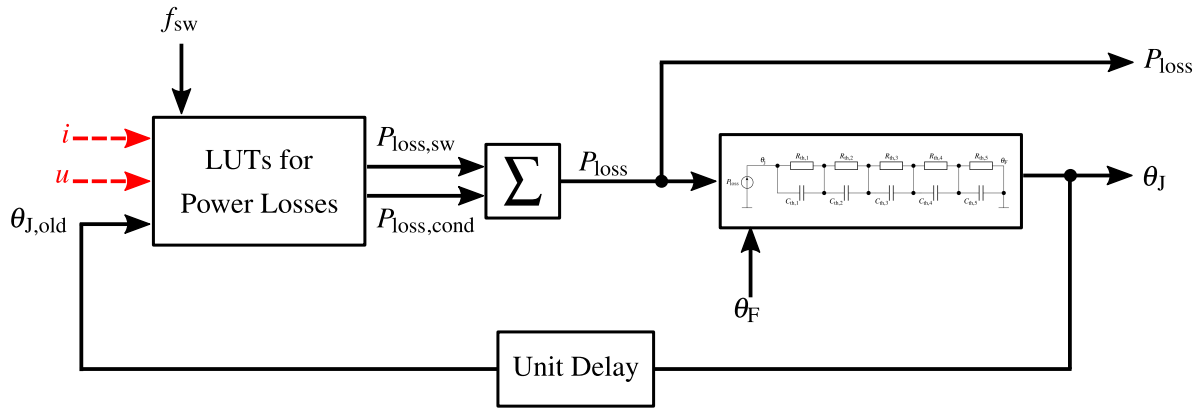

Figure 2.31: Temperature dependent loss calculation procedure implemented in MATLAB as a class and subsystem

2.4 Electric Machine

One of the important components used in the drivetrain of the electric vehicles are the electric machines. Although they are not the main focus of this work, but their principle of operation will be presented qualitatively, and the static and dynamic equations of the specific type of electric machine used in this work will be provided in the following.

In general definition, an electric machine is an energy conversion device, which converters the electric energy into mechanical energy in a form of a rotatory or a linear movement [84]. There are different methods with which the electric machines are realized. Direct current machines (DC machines) and alternating current machines (AC machines) are two main categories of the electric machines [85].

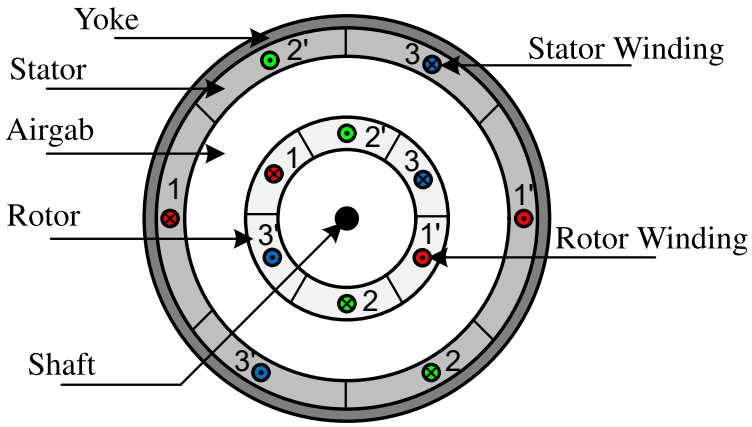

Figure 2.32: Cross section of typical wound-rotor induction electric machine with pole pair equal to one ($p = 1$)

Figure 2.32 shows the cross section of an induction electric machine (also known as asynchronous machine) which is used for the evaluation of the drivetrain in this work. The stator of such electric machine type consists of three winding groups which form the three phases of the

machine. The windings of each of the phases are placed in the stator slots with 120° mechanical angle difference with respect to the other phases. For simplicity it has been assumed that the windings belonging to each phase are distributed in the stator slots in a way that the resulting magnetic field has a sinusoidal distribution in the air gap between the stator and the rotor, and thereby the higher order harmonics of the magnetic fields are neglected.

On the stator side, further assumptions and simplifications are made to simplify the evaluation of the induction machine. These are as follows:

- All three winding groups are symmetrical and do have equal number of winding turns ⇒ Equal inductances and resistances
- Core saturation and eddy current are neglected ⇒ Linear dependance between the winding currents and magnetic fields
- Relative permeability of the core ($\mu_{\mathrm{r,core}}$) is infinite ⇒ No tangential magnetic field in the air gap
- Three phases of the stator are star-connected ⇒ Sum of stator currents equals to zero.

The rotor of the induction machine is generally available in two different variants. The first type is the so-called squirrel-cage rotor which is made of a laminate steel cylinder with embedded aluminum or copper bars in its surface. The second rotor type is the wound-rotor which is shown in figure 2.32 and consists of three phase windings which either can be shortened on both sides or connected to an external three phase supply via slip-rings (known as doubly-fed induction machine). The working principle is similar in both rotor types, and is based on the Faraday's law of induction. According to this, the rotating magnetic field of the stator produces an induced voltage in the rotor bars (or windings). This induced voltage will then results in a flowing current in the rotor bars, and due to the interaction of this current with the stator magnetic field a mechanical torque will be applied to the rotor (resulting form the Lorentz law mentioned before), and finally the rotor starts rotating. The current continues flowing in the rotor bars and consequently the rotor keeps rotating only if there is speed difference between the rotating speed of the rotor ω_{m} and the rotating speed of the stator magnetic field ω_{r}. The reason for naming this type of electric machine the asynchronous machine is exactly because of the mentioned difference between the stator magnetic field speed and rotor rotation speed.

In order to drive the machine, the three stator phases are connected to a symmetrical 3-phase AC voltage source which is parametrized as shown in the following equations:

$$\begin{aligned} u_{\mathrm{s},1}(t) &= \sqrt{2}\, U_{\mathrm{s}} \cdot \cos(\omega_{\mathrm{s}} t) \\ u_{\mathrm{s},2}(t) &= \sqrt{2}\, U_{\mathrm{s}} \cdot \cos(\omega_{\mathrm{s}} t - 120^\circ) \\ u_{\mathrm{s},3}(t) &= \sqrt{2}\, U_{\mathrm{s}} \cdot \cos(\omega_{\mathrm{s}} t + 120^\circ)\,. \end{aligned} \tag{2.47}$$

In the equation above, ω_{s} is the angular frequency of the voltage, which also determines the

angular speed of the stator magnetic field. With the help of Clarke-transformation[8)] (also known as (α,β)-transformation) the symmetrical three phases are represented in the form of a complex vector. Figure 2.33 shows the three stator voltages which have 120° spacial difference with each other. According to the Clarke-transformation the alpha-axis of the mentioned complex vector is fixed to the first stator voltage phase, and the vector angle and amplitude is calculated as in equation 2.48 with the help of the transformation matrix $\mathbf{T}_{\alpha\beta}$ presented in [13].

$$\underline{\vec{u}}_{\mathrm{s},\alpha\beta} = \begin{bmatrix} u_{\mathrm{s},\alpha} \\ u_{\mathrm{s},\beta} \end{bmatrix} = \mathbf{T}_{\alpha\beta} \cdot \begin{bmatrix} u_{\mathrm{s},1} \\ u_{\mathrm{s},2} \\ u_{\mathrm{s},3} \end{bmatrix} = \sqrt{2}\, U_{\mathrm{S}} \cdot e^{j\omega_{\mathrm{s}} t} \tag{2.48}$$

The stator currents are also transformed into the vector form (referenced to the stator frame) using $\mathbf{T}_{\alpha\beta}$. Same as the stator voltages and currents, the rotor quantities should also be transformed into the stator reference frame as vectors. Figure 2.33 shows the mechanical position of the rotor (δ) which is used to convert the rotor 3-phase voltages and currents into the stator reference frame. This is realized with the help of the so-called Park-transformation[9)]. Finally as all vectors are in the same reference frame (fixed to stator) the dynamic equations of the stator voltage and rotor voltage can be driven with the help of the corresponding currents, inductances, and resistances as shown equations 2.49 an 2.50. It has to be taken into account that the derivative of the current vector in stator reference frame results in rotary component in the rotor voltage equation as shown in equation 2.50.

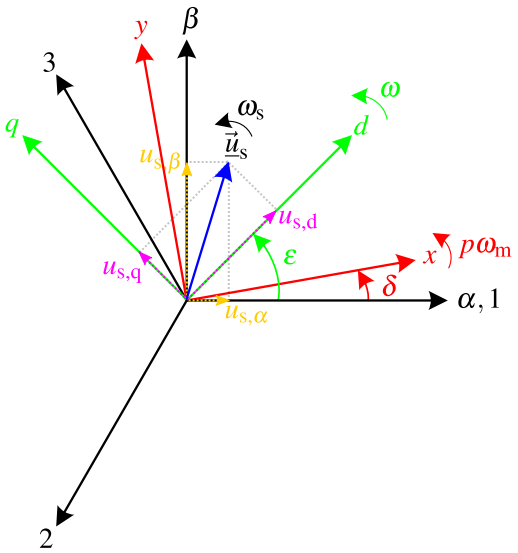

Figure 2.33: Vector representation of the induction machine phase voltages in three different reference frames: fixed to the stator (α,β)-Coordinate System(COS) (black), fixed to the rotor (x,y)-COS (red), and fixed to an arbitrary rotating axis (d,q)-COS (green)

[8)] The detail of Clarke-transformation is explained in [13].
[9)] The detail of Park-transformation is explained in [13].

$$\begin{aligned}\vec{\underline{u}}_{\mathrm{s},\alpha\beta} &= R_\mathrm{s}\,\vec{\underline{i}}_{\mathrm{s},\alpha\beta} + \frac{d}{dt}\left(L_\mathrm{s}\cdot\vec{\underline{i}}_{\mathrm{s},\alpha\beta} + L_\mathrm{m}\cdot\vec{\underline{i}'}_{\mathrm{r},\alpha\beta}\right)\\ &= R_\mathrm{s}\,\vec{\underline{i}}_{\mathrm{s},\alpha\beta} + \frac{d}{dt}\vec{\underline{\Psi}}_{\mathrm{s},\alpha\beta} \qquad (2.49)\\ \vec{\underline{u}'}_{\mathrm{r},\alpha\beta} &= R'_\mathrm{r}\,\vec{\underline{i}'}_{\mathrm{r},\alpha\beta} + \frac{d}{dt}\left(L'_\mathrm{r}\cdot\vec{\underline{i}'}_{\mathrm{r},\alpha\beta} + L_\mathrm{m}\cdot\vec{\underline{i}}_{\mathrm{s},\alpha\beta}\right) - jp\omega_\mathrm{m}\cdot\left(L'_\mathrm{r}\cdot\vec{\underline{i}'}_{\mathrm{r},\alpha\beta} + L_\mathrm{m}\cdot\vec{\underline{i}}_{\mathrm{s},\alpha\beta}\right)\\ &= R'_\mathrm{r}\,\vec{\underline{i}'}_{\mathrm{r},\alpha\beta} + \frac{d}{dt}\vec{\underline{\Psi}'}_{\mathrm{r},\alpha\beta} - jp\omega_\mathrm{m}\cdot\vec{\underline{\Psi}'}_{\mathrm{r},\alpha\beta} \qquad (2.50)\end{aligned}$$

In the equations above, the rotor quantities are reflected to the stator side, which can be calculated with the help of the stator and rotor winding turns and winding factors (dependent on the winding distribution) as shown in equation 2.51. Furthermore the stator and rotor inductances are split into two parts of magnetizing inductance (represented by L_m and resulting from the magnetic flux which passes the air gap and encircles the counterpart winding) and the leakage inductance (represented by L_σ and resulting from the magnetic flux which encircles only the exciter winding) as shown in equation 2.52.

$$i'_\mathrm{r} = \frac{N_\mathrm{r}\zeta_\mathrm{r}}{N_\mathrm{s}\zeta_\mathrm{s}}\cdot i_\mathrm{r};\qquad u'_\mathrm{r} = \frac{N_\mathrm{s}\zeta_\mathrm{s}}{N_\mathrm{r}\zeta_\mathrm{r}}\cdot u_\mathrm{r};\qquad L'_\mathrm{r} = \frac{N_\mathrm{s}^2\zeta_\mathrm{s}^2}{N_\mathrm{r}^2\zeta_\mathrm{r}^2}\cdot L_\mathrm{r};\qquad R'_\mathrm{r} = \frac{N_\mathrm{s}^2\zeta_\mathrm{s}^2}{N_\mathrm{r}^2\zeta_\mathrm{r}^2}\cdot R_\mathrm{r} \qquad (2.51)$$

$$L_\mathrm{s} = L_\mathrm{m} + L_{\mathrm{s}\sigma};\qquad L'_\mathrm{r} = L_\mathrm{m} + L'_{\mathrm{r}\sigma} \qquad (2.52)$$

It should be noted that in equations 2.49 and 2.50 the flux linkage consists of two components. The first part is the so-called air gap magnetic flux which is resulting form the sum of the reflected rotor current and the stator current multiplied by the magnetizing inductance (L_m). The second part resulting from the product of the corresponding leakage inductance ($L_{\mathrm{s}\sigma}$ or $L'_{\mathrm{r}\sigma}$) and current. Equations 2.53 and 2.54 present the stator linkage flux and rotor linkage flux respectively.

$$\vec{\underline{\Psi}}_{\mathrm{s},\alpha\beta} = \vec{\underline{\Psi}}_{\mathrm{s},\sigma,\alpha\beta} + (\vec{\underline{\Psi}}_{\mathrm{s,m},\alpha\beta} + \vec{\underline{\Psi}'}_{\mathrm{r,m},\alpha\beta}) = \vec{\underline{\Psi}}_{\mathrm{s},\sigma,\alpha\beta} + \vec{\underline{\Psi}}_{\mathrm{ag},\alpha\beta} \qquad (2.53)$$

$$\vec{\underline{\Psi}'}_{\mathrm{r},\alpha\beta} = \vec{\underline{\Psi}'}_{\mathrm{r},\sigma,\alpha\beta} + (\vec{\underline{\Psi}'}_{\mathrm{r,m},\alpha\beta} + \vec{\underline{\Psi}}_{\mathrm{s,m},\alpha\beta}) = \vec{\underline{\Psi}'}_{\mathrm{r},\sigma,\alpha\beta} + \vec{\underline{\Psi}}_{\mathrm{ag},\alpha\beta} \qquad (2.54)$$

With the help of stator and rotor voltage equations the stationary model of the induction machine can be derived. During the stationary condition the motor rotates with a constant speed (ω_m) and the single-phase equivalent model of the machine is extracted from equations 2.49 an 2.50. Figure 2.34 shows this equivalent circuit, in which $L_{\mathrm{s}\sigma}$ and $L'_{\mathrm{r}\sigma}$ are the leakage inductance of the stator and rotor (reflected to the stator) respectively, and s stands for rotor slip described in

equation 2.55.

$$s = \frac{\omega_s - p\omega_m}{\omega_s} = \frac{\omega_r}{\omega_s} \tag{2.55}$$

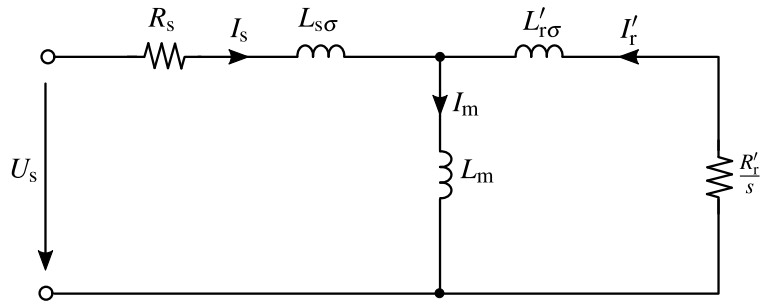

Figure 2.34: Stationary single-phase equivalent circuit of an induction electric machine under the assumption of equal number of rotor and stator winding turns ($N_s = N_r$) and same winding factor of the rotor and stator windings ($\zeta_s = \zeta_r$)

Another important point which should be mentioned is that the reference frame of the mentioned vector transformation can also be set to an arbitrary rotating coordinate system. As an example the green lines in figure 2.33 represent the coordinate system (d,q) which rotates with the speed of ω. If the reference frame is fixed to the d-axis of (d,q)-Coordinate System then the stator-fixed vectors can be transformed into this arbitrary reference frame with the help of equation 2.56.

$$\vec{\underline{x}}_{dq} = e^{-j\varepsilon} \cdot \vec{\underline{x}}_{\alpha\beta} \tag{2.56}$$

In the equation above, ε is the angle difference between the direct axis of the rotating reference frame and the direct axis of the stationary reference frame fixed to the stator. With the help of equation 2.56 the stator and rotor voltage equations in stator-fixed reference frame (α,β) (equations 2.57 and 2.58) can be transformed into the (d,q)-COS as follows:

$$\vec{\underline{u}}_{s,dq} = R_s \vec{\underline{i}}_{s,dq} + \frac{d}{dt}\vec{\underline{\Psi}}_{s,dq} + j\omega\vec{\underline{\Psi}}_{s,dq} \tag{2.57}$$

$$\vec{\underline{u'}}_{r,dq} = R'_r \vec{\underline{i'}}_{r,dq} + \frac{d}{dt}\vec{\underline{\Psi'}}_{r,dq} + j\omega\vec{\underline{\Psi'}}_{r,dq} - jp\omega_m \cdot \vec{\underline{\Psi'}}_{r,dq}. \tag{2.58}$$

The last point is the calculation of the machine produced torque. In an induction machine the output torque is calculated using the cross product of the rotor magnetizing flux linkage and stator magnetizing flux linkage [86]. Equation 2.59 shows the resulting torque, in which the number of pole pairs are taken into account. The included factor in the equation results from the

use of a reference-component invariant Clarke-transformation (explained in [13]).

$$T_\mathrm{e} = \frac{3}{2}p \cdot \left\| (\underline{\vec{\Psi}}'_{\mathrm{r,m,dq}} \times \underline{\vec{\Psi}}_{\mathrm{s,m,dq}}) \right\| = \frac{3}{2}p \cdot L_\mathrm{m} \left\| (\underline{\vec{i}}'_{\mathrm{r,dq}} \times \underline{\vec{i}}_{\mathrm{s,dq}}) \right\| = \frac{3}{2}p \cdot L_\mathrm{m}(i'_{\mathrm{r,d}} \cdot i_{\mathrm{s,q}} - i'_{\mathrm{r,q}} \cdot i_{\mathrm{s,d}}) \tag{2.59}$$

With the help of equation 2.60 the dynamics of the motor speed can now be calculated for a given mechanical load ([87]).

$$J_\mathrm{R} \cdot \frac{d\omega_\mathrm{m}}{dt} = T_\mathrm{e} - T_\mathrm{L} \tag{2.60}$$

Table 2.6 shows different parameters of the induction machine used in this work. With the help of these values the dynamic model of the machine is implemented in Simulink using the so-called PLECS toolbox.

Table 2.6: Induction machine parameters modeled in Simulink using PLECS toolbox

Description	Designator	Value	Unit
Nominal power	P_n	30	kW
Nominal voltage	$u_{\mathrm{LL,n}}$	400	V
Nominal torque	T_n	63.5	Nm
Breakdown torque	T_bd	230	Nm
Nominal frequency	$f_{\mathrm{s,n}}$	76	Hz
Stator resistance	R_s	51	mΩ
Rotor resistance	R'_r	41.8	mΩ
Magnetizing inductance	L_m	21.7	mH
Stator leakage inductance	$L_{\mathrm{s}\sigma}$	700	μH
Rotor leakage inductance	$L'_{\mathrm{r}\sigma}$	2	mH
Pole pairs	p	1	-
Moment of inertia	J_R	6.45	g/m^2

The power losses of the machine have also been included in the Simulink model. Because of the complexity the hysteresis losses and the additional losses caused by high order harmonics are not taken into account in this model. The components of the machine power losses $P_{\mathrm{M,loss}}$ are the stator ohmic losses and rotor ohmic losses. These can be calculated with the help of stator and rotor winding resistances shown in table 2.6 and the measured machine currents as in the following:

$$P_{\mathrm{s,cu,loss}} = \frac{3}{2} \cdot R_\mathrm{s} \cdot (i^2_{\mathrm{s,d}} + i^2_{\mathrm{s,q}}) \tag{2.61}$$

$$P_{\mathrm{r,cu,loss}} = \frac{3}{2} \cdot R'_\mathrm{r} \cdot ({i'_{\mathrm{r,d}}}^2 + {i'_{\mathrm{r,q}}}^2). \tag{2.62}$$

It should be mentioned that the simplified machine loss model provided here does not take into account the iron-losses and the effects of a non-sinusoidal supply on the machine losses. As discussed in detail in chapter 5, the machine model is used in this work only to obtain a realistic load at the output of the DC-AC converter part of the drivetrain. The influence of different parameters of the converter type (for example the modulation index, and switching frequency of the 3-phase PWM inverter) on the iron losses of the machine is outside the scope of this study, and for the analysis in chapter 5, reference is made to the existing literature on this subject.

3 Drivetrain modeling and Control System Design

In this chapter the components which are introduced and modeled in chapter 2 will be combined together to form and model the drivetrain. Figure 3.1 shows the components of a conventional drivetrain (battery, DC-AC inverter, and electric machine) as well as a DC-DC converter which is added between the battery and the inverter as an extension. In the following the topologies used for the inverter and the DC-DC converter as well as the implemented control system are introduced. The stationary and transient model of the inverter and DC-DC converter and finally the entire drivetrain will be presented in this chapter as well.

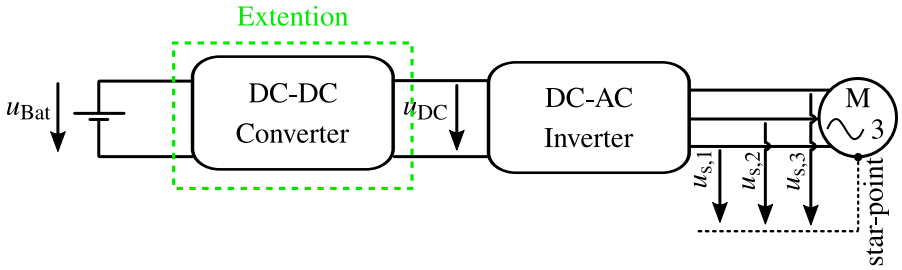

Figure 3.1: The drivetrain of an electric vehicle with the option of using a DC-DC converter in addition to the inverter and electric machine

3.1 3-phase 2-level DC-AC inverter

Figure 3.2 shows a 3-phase 2-level DC-AC inverter. The role of an inverter is to convert a constant DC input voltage to a three phase output voltage with a variable frequency and amplitude [88]. This 3-phase voltage will then be fed into an electric machine to drive it. As shown in figure 3.2 the 3-phase 2-level inverter consists of an input capacitor (DC-Link capacitor) and three so-called half-bridges. Each half-bridge contains two power transistors, called high-side and low-side transistors, and the middle points of the half-bridges are connected to the motor phases.

3.1.1 Transient Model

In a three phase two level inverter the high-side and low-side switches of each one of the half-bridges are activated complementarily and with the switching functions of $s_{\mathrm{inv,i}}(t)$ and $-s_{\mathrm{inv,i}}(t)$

respectively. As shown in [12], the switching function value $s_{\mathrm{inv}}(t)$ can either be 1 (turning on of the transistor) or -1 (turning off of the transistor), and the inverter output voltages[1)] $\vec{u}'_{\mathrm{s}}$ are calculated using the DC-Link voltage and the switching state of the corresponding phase as shown in equation 3.1.

$$\vec{u}'_{\mathrm{s}} = \begin{bmatrix} u'_{\mathrm{s,1}} \\ u'_{\mathrm{s,2}} \\ u'_{\mathrm{s,3}} \end{bmatrix} = \frac{u_{\mathrm{DC}}}{2} \cdot \begin{bmatrix} s_{\mathrm{inv,1}}(t) \\ s_{\mathrm{inv,2}}(t) \\ s_{\mathrm{inv,3}}(t) \end{bmatrix} = \frac{u_{\mathrm{DC}}}{2} \cdot \vec{s}(t) \qquad \text{with} \quad s_{\mathrm{inv,i}} \in (-1;1) \tag{3.1}$$

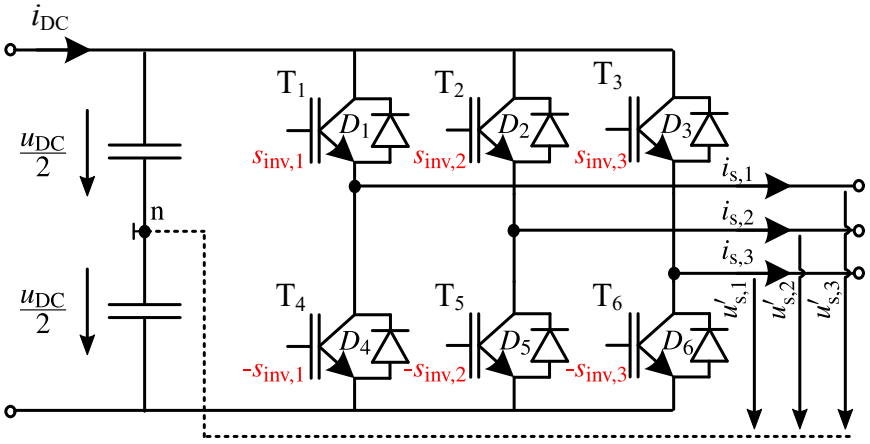

Figure 3.2: Basic structure of a 3-phase 2-level DC-AC inverter topology (taken and modified from [12])

The motor phase voltages $u_{\mathrm{s,i}}$ (inverter output voltages with respect to the star point of the motor) are calculated with the help of the voltage difference between the DC-Link middle point (neutral point) and the motor star point. In the case of a symmetrical motor, this voltage difference which is also known as the common-mode voltage is calculated using equation 3.2.

$$u_0 = \frac{u'_{\mathrm{s,1}} + u'_{\mathrm{s,2}} + u'_{\mathrm{s,3}}}{3} \tag{3.2}$$

With the help of the common-mode voltage the motor phase voltages are calculated as follows:

$$u_{\mathrm{s,i}} = u'_{\mathrm{s,i}} - u_0. \tag{3.3}$$

Based on equation 3.3 the relationship between the motor phase voltages (with respect to motor star-point) and the inverter output voltages (with respect to DC-Link middle point) is determined

[1)] The output voltages of the inverter are defined as the voltage difference between each phase and the DC-Link middle point voltage (also known as neutral point)

using the transformation matrix shown in equation 3.4.

$$\vec{u}_{\mathrm{s}} = \begin{bmatrix} u_{\mathrm{s},1} \\ u_{\mathrm{s},2} \\ u_{\mathrm{s},3} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \cdot \begin{bmatrix} u'_{\mathrm{s},1} \\ u'_{\mathrm{s},2} \\ u'_{\mathrm{s},3} \end{bmatrix} \tag{3.4}$$

An overview of all possible inverter switching states as well as the resulting motor phases voltages are presented in table 3.1.

Table 3.1: Inverter switching states and the resulting motor phase voltages with respect to the DC-Link neutral point ($u'_{\mathrm{s,i}}$) and motor star point ($u_{\mathrm{s,i}}$)

States	$s_{\mathrm{inv},1}$	$s_{\mathrm{inv},2}$	$s_{\mathrm{inv},3}$	$\frac{u'_{\mathrm{s},1}}{\frac{u_{\mathrm{DC}}}{2}}$	$\frac{u'_{\mathrm{s},2}}{\frac{u_{\mathrm{DC}}}{2}}$	$\frac{u'_{\mathrm{s},3}}{\frac{u_{\mathrm{DC}}}{2}}$	$\frac{u_{\mathrm{s},1}}{\frac{u_{\mathrm{DC}}}{2}}$	$\frac{u_{\mathrm{s},2}}{\frac{u_{\mathrm{DC}}}{2}}$	$\frac{u_{\mathrm{s},3}}{\frac{u_{\mathrm{DC}}}{2}}$
0	-1	-1	-1	-1	-1	-1	0	0	0
1	1	-1	-1	1	-1	-1	$\frac{4}{3}$	$\frac{-2}{3}$	$\frac{-2}{3}$
2	1	1	-1	1	1	-1	$\frac{2}{3}$	$\frac{2}{3}$	$\frac{-4}{3}$
3	-1	1	-1	-1	1	-1	$\frac{-2}{3}$	$\frac{4}{3}$	$\frac{-2}{3}$
4	-1	1	1	-1	1	1	$\frac{-4}{3}$	$\frac{2}{3}$	$\frac{2}{3}$
5	-1	-1	1	-1	-1	1	$\frac{-2}{3}$	$\frac{-2}{3}$	$\frac{4}{3}$
6	1	-1	1	1	-1	1	$\frac{2}{3}$	$\frac{-4}{3}$	$\frac{2}{3}$
7	1	1	1	1	1	1	0	0	0

In order to drive the motor connected to the inverter the desired amplitude and frequency of the motor phase voltages[2)] shown in equation 2.47 should be provided at the inverter output. This will be achieved by implementing a proper modulator which controls each one of the inverter half-bridges, and toggles between different states of table 3.1.

A transient model of the inverter shown in figure 3.2 is implemented in SIMULINK using PLECS toolbox. This toolbox offers the option to include the thermal model of the power transistors discussed in section 2.3 by importing the thermal impedance of the utilized IGBT (HybridPACK 1 in this case) into the PLECS transistor database. In addition, the following temperature dependent look-up-tables are imported into the PLECS transistor database:

1. Switching-on energy losses (figure 3.3 (a))
2. Switching-off energy losses (figure 3.3 (b))
3. Voltage-current characteristics for conduction losses calculation (figure 3.3 (c)).

As shown in Figure 3.3 (d), in the implemented model, the heat sink-temperature is given as an input, and based on the output load and the switching states of the transistors, the voltage

[2)] As it will be shown in this section, these values are determined by the motor controller for any given operating point.

and current of each transistor (anti-parallel diodes) are determined, and using the provided database, the transient junction temperature and power dissipation are calculated. The provided inverter model is then integrated into the overall system in SIMULINK and placed between the modulator unit, discussed in the next subsection, and the machine model discussed in 2.4.

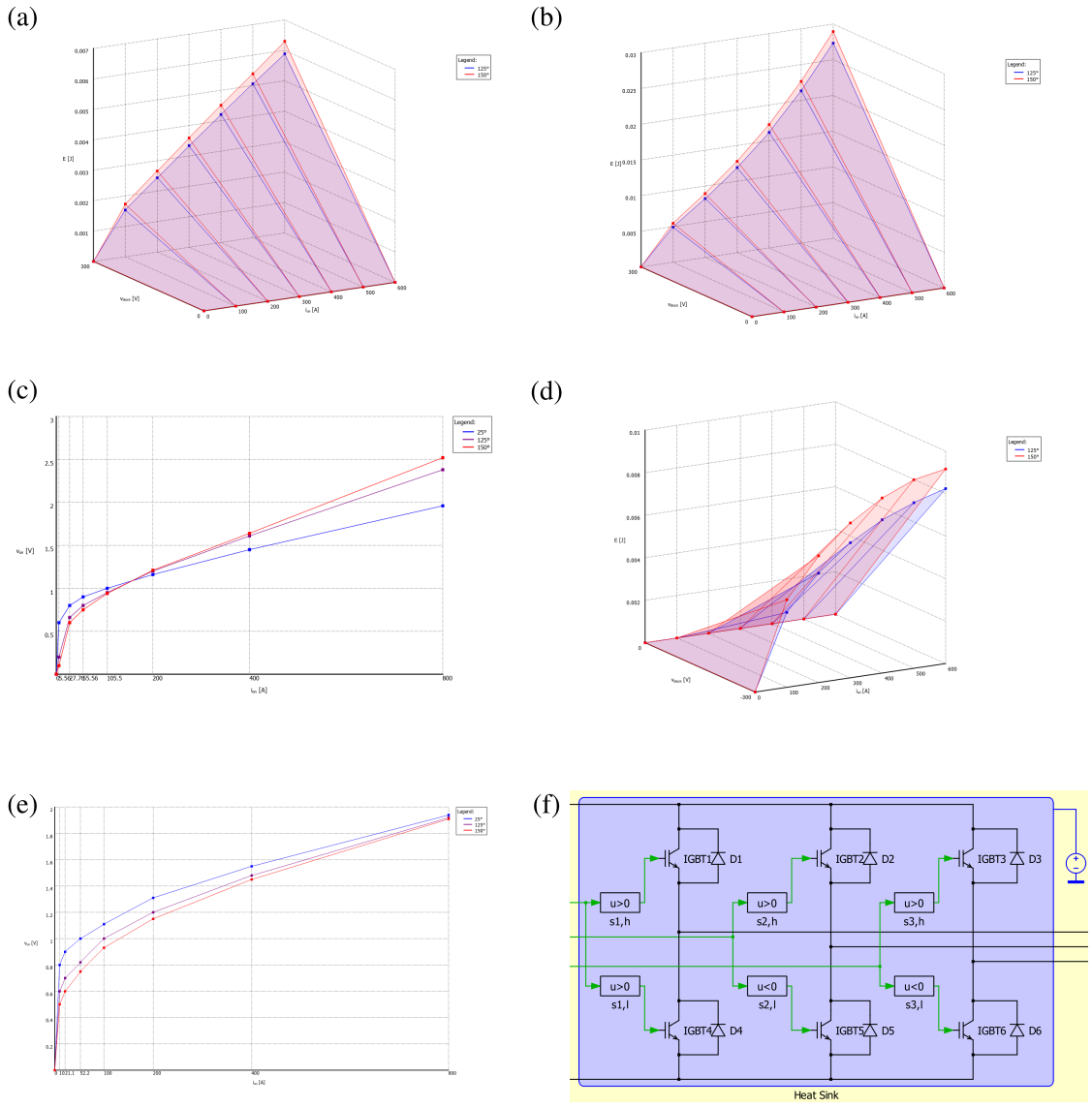

Figure 3.3: Temperature dependent model of HybridPACK 1 Module ($''FS400R07A1E3''$) implemented in SIMULINK using PLECS tool box. (a) IGBT switching on losses (b) IGBT switching off losses (c) IGBT voltage-current characteristics (d) Diode reverse recovery losses (e) Diode voltage-current characteristics (f) inverter implementation with heat-sink in PLECS

Another point which should be mentioned here is the complexity of the implemented model. As disused above this unit includes a fully transient model of the inverter, in which every state-toggle is simulated precisely, and the SIMULINK solver calculates the exact operating point of the components during each switching time. This requires a very small sampling time

which makes the entire simulation very slow. That would not be critical for the simulation of a few operating points, but in the case of an entire driving cycle evaluation, the simulation time will be unacceptably long. Therefore, additional to the switching model of the inverter, the so-called state-space average method [89] is used to develop a model which estimates (and average) the operating points of the components. This simplified quasi-transient model is presented at the end of this section along with a comparison with the switched inverter model (in terms of energy losses and transients).

3.1.2 Pulse Generator

Figure 3.4 shows a typical pulse generator used for the 3-phase 2-level inverter. This unit consists of a comparator, which compares a triangular signal (carrier) with the three modulation signals. The outputs of the comparator will then provide the PWM signals of the three half-bridges (the switching signals can also be interpreted as the duty cycle of each one of the switches). In this work the lower and upper limits of the normalized signals are set to 0 and 1 respectively. As shown in Figure 3.4, the carrier signal at the input of the comparator alternates between 0 and 1 with the same frequency as the switching frequency of the inverter (f_{sw}), and the modulation signals (which also alternate between 0 and 1) are derived from the desired amplitude and frequency of the motor phase voltages considering the implemented modulation scheme.

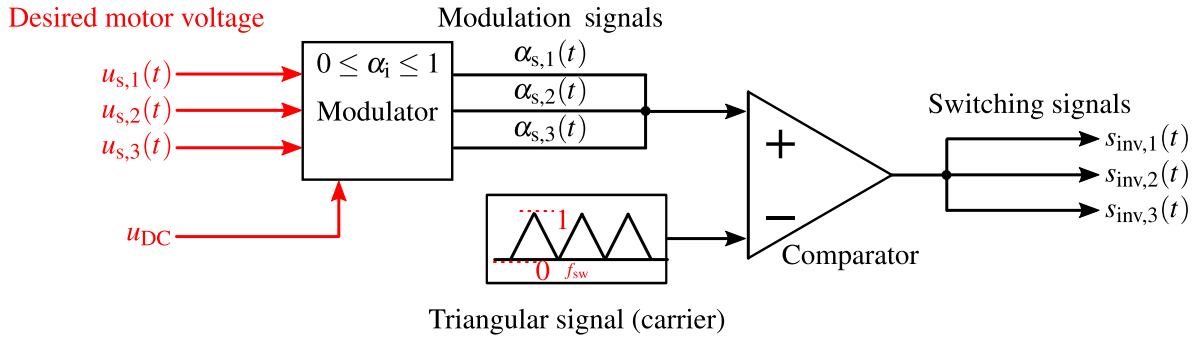

Figure 3.4: A typical pulse generator for a 3-phase 2-level inverter

There are different types of modulation strategies developed for different use-cases [90]. The sinusoidal pulse width modulation (SPWM) is one of the basic modulation strategies, in which, during the stationary operating condition, the modulating signals are sinusoidal waveforms with the maximum amplitude of half of the DC-Link voltage ($\frac{u_{DC}}{2}$) and the phase difference of 120 degree between each other. This ensures the operation of the modulator in the so-called linear modulation region, in that there is a linear dependency between the amplitude of the modulation signal and the amplitude of the output voltage fundamental frequency.

In this method, the transient value of the modulating signal is equal to the instantaneous value of the desired motor voltage normalized to the half the of DC-Link voltage. Equation 3.5 shows the calculation of this modulation signal, where $u_{s,i}(t)$ is the motor phase voltage (dynamically fed from the motor controller). It should be noted that because of the selection of the lower and

upper limits of the triangular carrier signal (figure 3.4), the normalized value of the desired output voltage is scaled down and shifted up so that the minimum and maximum value of the modulation signal remains between 0 and 1.

$$\alpha_i(t) = 0.5 \cdot \frac{u_{\mathrm{s,i}}(t)}{\frac{u_{\mathrm{DC}}}{2}} + \frac{1}{2} \tag{3.5}$$

During the stationary operating mode of the motor the desired value of the motor phase voltage is a pure sinusoidal waveform with a constant amplitude and fundamental frequency. The so-called modulation index M is another useful parameter which is defined as the ratio of the stationary amplitude of the desired motor voltage to the half of the DC-Link voltage, which is shown in equation 3.6.

$$M = \frac{\hat{U}_{\mathrm{out}}}{\frac{u_{\mathrm{DC}}}{2}} \tag{3.6}$$

Accordingly, in the stationary condition, the amplitude of the modulation signals are calculated based on the modulation index resulting from the desired amplitude of the motor phase voltages. As shown in equation 3.7 the resulting values will then be scaled down and shifted up in a way that it gets inside the boundaries of the signal generator carrier signal.

$$\begin{aligned}
\alpha_{\mathrm{s,1,SPWM}}(t) &= \frac{1 + M \cdot \cos(\omega_{\mathrm{s}} t)}{2} \\
\alpha_{\mathrm{s,2,SPWM}}(t) &= \frac{1 + M \cdot \cos(\omega_{\mathrm{s}} t - 120^\circ)}{2} \\
\alpha_{\mathrm{s,3,SPWM}}(t) &= \frac{1 + M \cdot \cos(\omega_{\mathrm{s}} t + 120^\circ)}{2}
\end{aligned} \tag{3.7}$$

As stated above, for the operation inside the linear modulation range the modulation index value (M) should be equal or smaller than 1. This means that the maximum amplitude of the output signal fundamental frequency is half of the DC-Link voltage (equation 3.6).

The modulation strategy which has been used in this work is called the space vector modulation [91]. The difference between SVM and SPWM is in the value of the common-mode voltage (u_0 in equation 3.2). In the SVM method instead of setting the star point voltage (common-mode voltage) to zero, it will be changed in a way that a higher maximum linear modulation index is achieved. The operation principle of this modulation strategy is explained with the help of figure 3.5 (from [12]). In this figure the dashed lines represent the reference value of the motor phase voltages during stationary operation normalized to $\frac{u_{\mathrm{DC}}}{2}$. As shown in equation 3.4, in a symmetrical machine, the sum of the motor phase voltages ($u_{\mathrm{s,123}}$) is always zero and adding or subtracting a given voltage term to all three inverter output voltages ($u'_{\mathrm{s,123}}$) will have no impact on the value of the motor phase voltages referenced to the star point voltage. According to the

SVM strategy, the normalized value of the inverter output voltages (shown with solid lines in figure 3.5) are calculate by adding a given zero component to all three motor reference voltages [92].

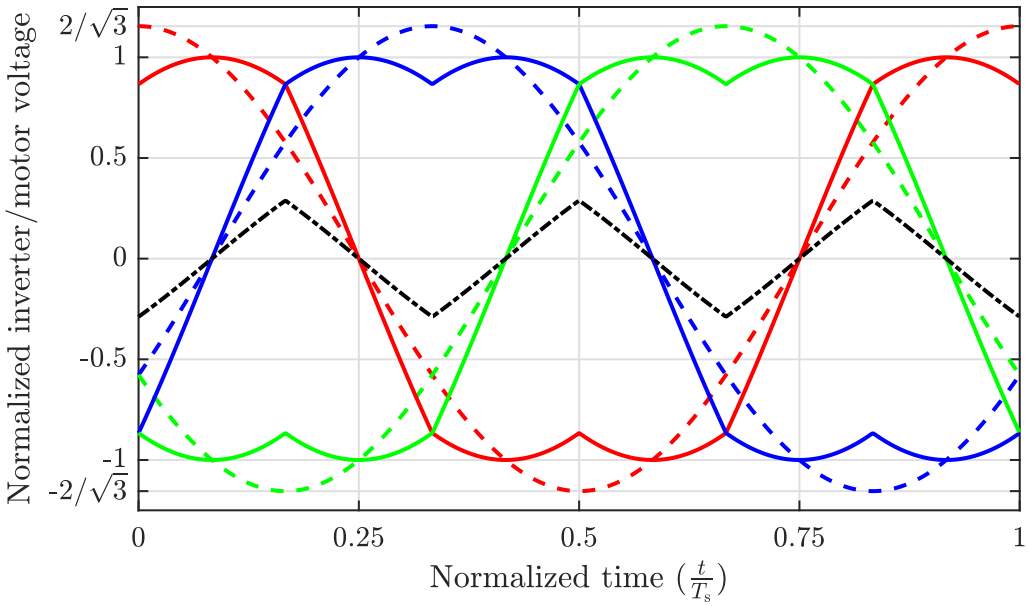

Figure 3.5: Inverter output to neutral point voltages normalized to $\frac{u_{DC}}{2}$ - solid lines, motor phase to star point reference voltages normalized to $\frac{u_{DC}}{2}$ - dashed lines, and added zero component - black dashed-dotted line (from [12])

The above mentioned zero voltage should be selected in a way, that the full DC-Link voltage is utilized and the theoretical limit of the linear modulation, which according to [12] equals $(\cos\ 30°)^{-1}$, is reached. The zero voltage component which is selected in this work is shown in figure 3.5 with black dashed-dotted line, and is calculated with the help of the normalized value of the motor set point voltages ($u_{s,i,norm}$) as shown in equation 3.8. By this selection the distance between the largest inverter modulation signal to the upper limit (+1) is the same as the smallest modulation signal to the lower limit (-1), which, according to table 3.1, leads to the same activation time interval of state 0 and state 7.

$$u_{0,norm} = -\frac{\max(u_{s,1,norm}, u_{s,2,norm}, u_{s,3,norm}) + \min(u_{s,1,norm}, u_{s,2,norm}, u_{s,3,norm})}{2}. \tag{3.8}$$

Equation 3.9 shows the SVM-based normalized value of the inverter output voltages during stationary operation of the motor (constant amplitude controlled by M and constant frequency controlled by ω_s).

$$\begin{aligned}
u'_{s,1,norm}(t) &= u_{0,norm}(t) + M \cdot \cos(\omega_s t) &&= u_{0,norm}(t) + u_{s,1,norm}(t) \\
u'_{s,2,norm}(t) &= u_{0,norm}(t) + M \cdot \cos(\omega_s t - 120°) &&= u_{0,norm}(t) + u_{s,2,norm}(t) \\
u'_{s,3,norm}(t) &= u_{0,norm}(t) + M \cdot \cos(\omega_s t + 120°) &&= u_{0,norm}(t) + u_{s,3,norm}(t)
\end{aligned} \tag{3.9}$$

Finally to calculate the duty cycle of the inverter phases, the calculated inverter output voltages should be scaled down and shifted up in a way that the results get inside the boundaries of the generator carrier signal of figure 3.4 (0 and 1). Equation 3.10 shows the duty cycles of the inverter with utilized SVM strategy.

$$\alpha_{s,i,SVM}(t) = \frac{1 + u'_{s,i,norm}(t)}{2} \tag{3.10}$$

As stated before, in order to operate in linear modulation region the maximum value of the normalized inverter output voltages $u'_{s,i,norm}$ should be equal to 1. As shown in figure 3.5, the maximum value of $u'_{s,i,norm}$ reaches 1, when the maximum value of the normalized motor voltages $u_{s,i,norm}$ (or the modulation index M) gets equal to 1.154. This additional amplitude (15.4%) of the motor voltages is actually the main benefit of using SVM strategy against SPWM.

For the dynamic operation the desired value of the motor phase voltages (set points which are the outputs of the motor controller discussed in the next section) will be fed into the modulator block shown in figure 3.6. This is actually the implemented SVM-based modulator in SIMULINK used in the motor controller block.

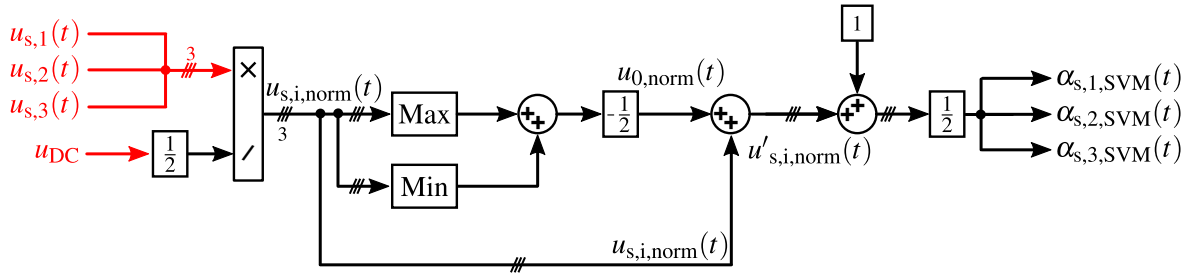

Figure 3.6: Implemented space vector modulator in SIMULINK

The introduced pulse generator of figure 3.4 with the utilized SVM strategy in its modulator unit is implemented and modeled in SIMULINK to provide switching signals to the inverter. The input of this SIMULINK unit is the desired three phase motor voltages, which themselves are the outputs of the controller unit presented in the following subsection.

3.1.3 Control System

In this section the implemented control scheme used to drive the connected electric traction motor is presented. As it has already been discussed in section 2.4 a wound-rotor induction machine (with shortened rotor coils) is used as the traction motor in this work. The machine has been modeled in SIMULINK using the parameter presented in table 2.6, and then it is connected to the provided inverter and modulator models. In order to design the controller based on the derived dynamic equation of the machine, a method called the Field Oriented Control (FOC) scheme is used [93].

The idea of vector-based control concept is to decouple the torque-producing component from the flux-producing component of the stator current vector. The dynamic voltage equations of the machine transformed into a rotating reference frame (fixed to a random position with rotating speed of ω) are presented in equations 2.57 and 2.58. In this step a new fictive variable is defined which is called the rotor magnetizing current and defined as follows:

$$\vec{\underline{i}}_{\mathrm{r,mg,dq}} = \frac{1}{L'_{\mathrm{r}}} \cdot \vec{\underline{\Psi}}'_{\mathrm{r,dq}} = \vec{\underline{i}}'_{\mathrm{r,dq}} + \frac{L_{\mathrm{m}}}{L'_{\mathrm{r}}} \cdot \vec{\underline{i}}_{\mathrm{s,dq}} = \vec{\underline{i}}'_{\mathrm{r,dq}} + \frac{1}{1+\sigma_{\mathrm{r}}} \cdot \vec{\underline{i}}_{\mathrm{s,dq}}. \tag{3.11}$$

By setting the rotating speed of the (d,q) coordinate system ((d,q)-COS) to the angular frequency of the stator voltage ω_{s}, and replacing the rotor current with the introduced rotor magnetizing current, the dynamic equations of the stator voltage and rotor voltage derived in section 2.4 (see equations 2.57 and 2.58) can be simplified as shown in the following equations.

$$\vec{\underline{u}}_{\mathrm{s,dq}} = R_{\mathrm{s}} \cdot \vec{\underline{i}}_{\mathrm{s,dq}} + \frac{d}{dt}\sigma_{\mathrm{eq}} L_{\mathrm{s}} \cdot \vec{\underline{i}}_{\mathrm{s,dq}} + j\omega_{\mathrm{s}}\sigma_{\mathrm{eq}} L_{\mathrm{s}} \cdot \vec{\underline{i}}_{\mathrm{s,dq}} + \frac{d}{dt} L_{\mathrm{m}} \cdot \vec{\underline{i}}_{\mathrm{r,mg,dq}} + j\omega_{\mathrm{s}} L_{\mathrm{m}} \cdot \vec{\underline{i}}_{\mathrm{r,mg,dq}} \tag{3.12}$$

$$\vec{\underline{u}}'_{\mathrm{r,dq}} = R'_{\mathrm{r}} \cdot (\vec{\underline{i}}'_{\mathrm{r,mg,dq}} - \frac{1}{1+\sigma_{\mathrm{r}}} \cdot \vec{\underline{i}}_{\mathrm{s,dq}}) + \frac{d}{dt} L'_{\mathrm{r}} \cdot \vec{\underline{i}}_{\mathrm{r,mg,dq}} + j\omega_{\mathrm{r}} L'_{\mathrm{r}} \cdot \vec{\underline{i}}_{\mathrm{r,mg,dq}} \tag{3.13}$$

In the equations above, ω_{r} is the angular frequency of the rotor voltage and σ_{eq} is the equivalent leakage coefficient calculated as follows:

$$\sigma_{\mathrm{eq}} = 1 - \frac{1}{(1+\sigma_{\mathrm{s}}) \cdot (1+\sigma_{\mathrm{r}})}. \tag{3.14}$$

$$\sigma_{\mathrm{s}} = \frac{L_{\mathrm{s}\sigma}}{L_{\mathrm{m}}} \quad \text{and,} \quad \sigma_{\mathrm{r}} = \frac{L'_{\mathrm{r}\sigma}}{L_{\mathrm{m}}} \tag{3.15}$$

With respect to the fact that the rotor windings are shortened on both sides ($\vec{\underline{u}}'_{\mathrm{r,dq}} = 0$) equation 3.13 can be solved for the rotor magnetizing current, which results in the following differential equation:

$$T_{\mathrm{r}} \cdot \frac{d}{dt}\vec{\underline{i}}_{\mathrm{r,mg,dq}} + (1 + j\omega_{\mathrm{r}} T_{\mathrm{r}}) \cdot \vec{\underline{i}}_{\mathrm{r,mg,dq}} = \frac{L_{\mathrm{m}}}{L'_{\mathrm{r}}} \cdot \vec{\underline{i}}_{\mathrm{s,dq}} = \frac{1}{1+\sigma_{\mathrm{r}}} \cdot \vec{\underline{i}}_{\mathrm{s,dq}}, \tag{3.16}$$

in which T_{r} is the rotor time constant resulting from its resistance and inductance. In this step for further simplification the direct axis of the (d,q)-COS will be fixed to the rotor magnetizing current. Consequently the imaginary component of the magnetizing current vector gets equal to zero as in equation 3.17, and the stator and rotor voltage equations will be simplified as well.

$$\vec{\underline{i}}_{\mathrm{r,mg,dq}} = i_{\mathrm{r,mg}} \tag{3.17}$$

To summarize the implemented Park-transformation for the field oriented control application it can be referred to figure 2.33, in which the direct axis of (d,q)-COS should rotate with the angular frequency of ω_s and should be fixed to the magnetizing current vector of the rotor. The name of field oriented control is chosen since the angle of rotating d-axis (ε) represents also the angle of the rotor magnetizing flux vector (see equation 3.11).

By splitting the equation 3.16 into the real part and the imaginary part the following equations are obtained:

$$T_r \cdot \frac{d}{dt} i_{r,mg} + i_{r,mg} = \frac{1}{1+\sigma_r} \cdot i_{s,d}, \tag{3.18}$$

$$\omega_r \cdot T_r \cdot i_{r,mg} = \frac{1}{1+\sigma_r} \cdot i_{s,q}. \tag{3.19}$$

With the help of equation 2.59 the electrical torque of the machine with respect to the rotor magnetizing current and stator current can be derived as follows:

$$T_e = \frac{3}{2} p \cdot L_m \cdot i_{r,mg} \cdot i_{s,q}. \tag{3.20}$$

As mentioned in the beginning of this subsection the goal of the field oriented vector-based control strategy is to decouple the torque-producing component of the stator current from the flux-producing part. This goal is achieved by implementing the introduced (d,q)-transformation with which the torque-producing part is the d-current component (equation 3.20) and the flux-producing component is the stator q-current (equation 3.18). It is also important to mention that these two stator current components are no longer alternating quantities, since the (d,q) reference frame is rotating with the same angular speed as the stator current vector.

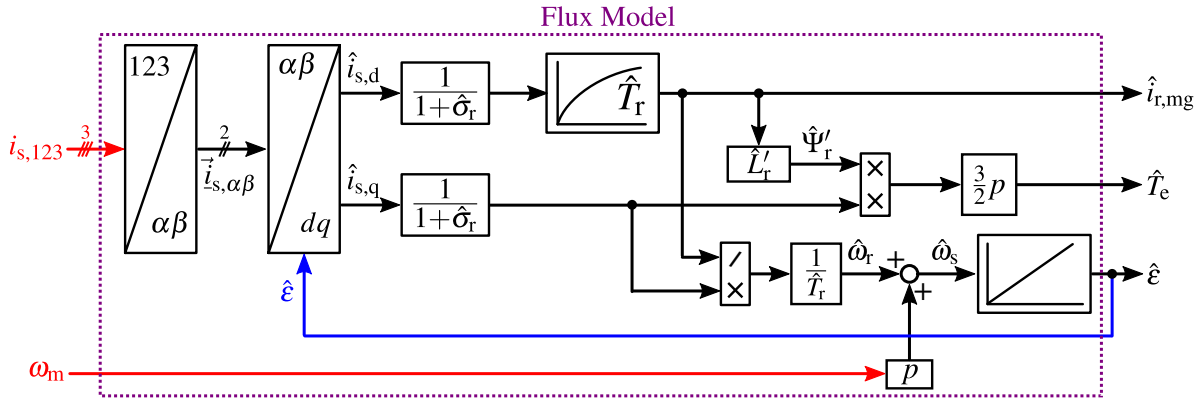

Figure 3.7: Flux model of the induction machine, in which the estimated value of the electric torque, magnetizing current, and magnetic flux angle are calculated based on the machine parameters and measured stator current and mechanical speed (from [13])

With the help of equations 3.18 to 3.20 a flux model is provided for the induction machine. In

this model the produced electric torque $\hat{T}_e$, the rotor magnetizing current $\hat{i}_{r,mg}$, and the angle of the rotor magnetic flux $\hat{\varepsilon}$ are estimated[3)] based on the machine parameters and measured stator current and mechanical speed. The estimated angle of the rotor magnetizing flux is also used internally to provide the reference angle for the (d,q)-transformation.

In this step the implemented control structure used for the induction machine is presented. This controller consists of two cascaded control loops which regulates two main machine variables, namely the rotor magnetizing flux and the mechanical speed. Figure 3.8 illustrates an overview of the controller implemented in SIMULINK.

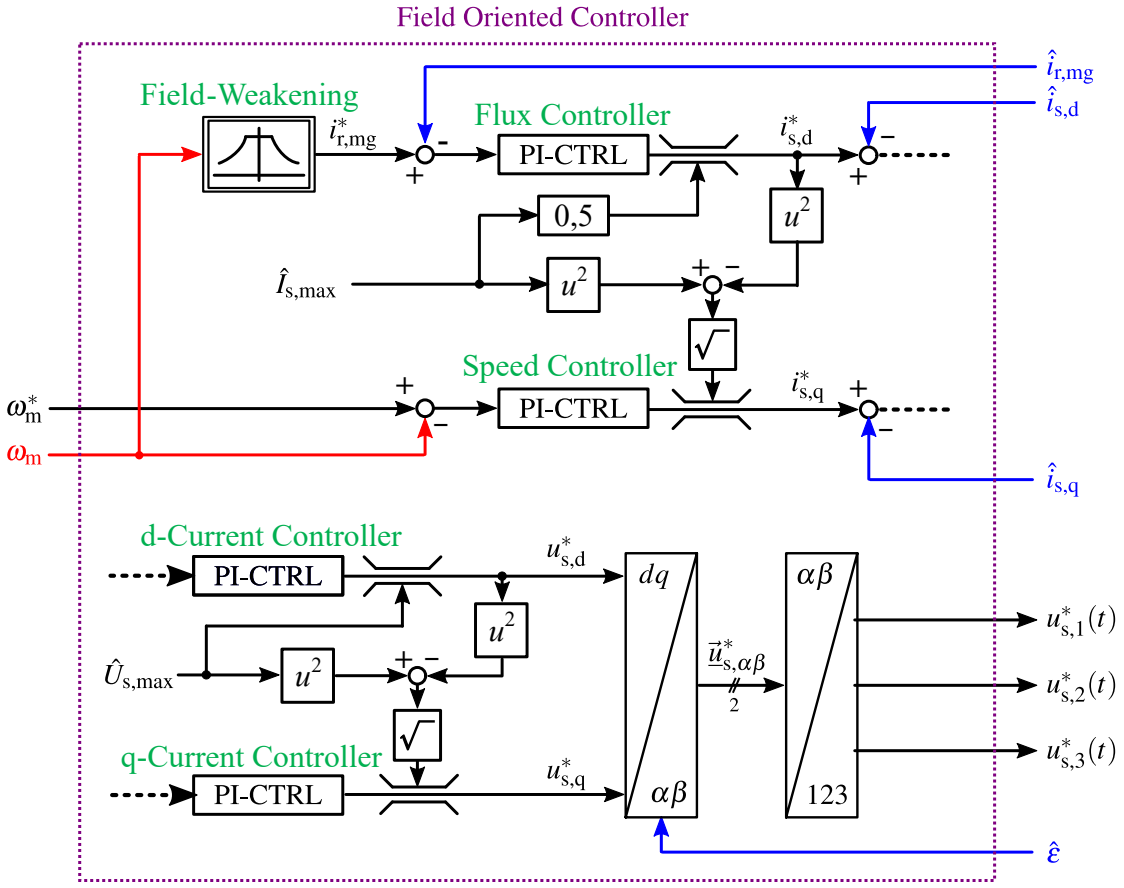

Figure 3.8: Field oriented controller of the induction machine, consists of two cascaded control loops to control the rotor magnetizing current (rotor flux) and mechanical angular speed

The first cascaded loop is composed of an inner d-current control loop and an outer flux control loop. According to this cascade structure the flux controller determines the set point of the d-current controller $i^*_{s,d}$, and the output of this current controller provides the set point of the stator voltage direct component $u^*_{s,d}$. The desired value of the outer loop flux controller itself (in this case it has been implemented using the rotor magnetizing current $i^*_{r,mg}$ which is directly coupled to the rotor magnetic flux through the equation 3.11) is calculated with the help of a

[3)] The outputs of the flux model are estimated values, because for the use in the controller block, the motor is modeled with constant winding inductance and resistance, and the effect of the temperature, high-order harmonics, and core saturation on the winding parameters are neglected.

look-up-table with the mechanical rotation speed ω_m as input. The actual value of the rotor magnetizing current and the stator d-current component are calculated in the flux model shown in figure 3.7 and fed into the controller unit as feedback signals.

The above mentioned look-up-table for the rotor magnetizing current has been extracted from the introduced machine model. With the help of a simulation the rotor magnetizing current is calculated at different rotation speeds under no-load condition. This LUT also includes the field-weakening operating area in which the stator voltage limit ($\hat{U}_{s,max}$) is reached and the rotation speed is higher than the nominal value of the machine speed (this is realized at the cost of a lower maximum produced torque than the machine nominal torque value as shown in [13]).

In the second cascaded loop the set point of the rotation speed ω_m^* is fed into the system as the input of the outer control loop. This set point will then be compared with the actual measured speed ω_m and the resulted error signal forms the input of the speed controller. Finally the output of the speed controller provides the set point of the q-current controller $i_{s,q}^*$, which in turn outputs the desired value of the stator voltage q-component $u_{s,q}^*$. The flux model is used here as well to feed back the actual value of the q-current to the current controller. As mentioned before the actuator of the controlled system is a voltage source inverter, therefore the output of the current controllers should be the set points of the inverter voltages. The assumption that the inverter provides the desired phase currents precisely and with a good dynamics is only valid if the inverter switching frequency is high enough and or the winding time constant is low enough [13]. Since the switching frequency of the inverter in this work is equal to 10 kHz the controller works properly with no additional effort.

As shown in figure 3.8 in the final stage the calculated stator voltage set point described in (d,q)-COS first transformed into the stator-fixed coordinate system with the help of the estimated flux vector angle $\hat{\varepsilon}$ (resulted from the flux model), and then the stator voltage vector will be decomposed into the three stator phase voltages using inverse Park-transformation. These phase voltages will be connected to the input of the modulator unit as the desired voltages of the machine.

All of the controllers shown in figure 3.8 are PI-controllers with anti-windup[4)] as described in [94], with the following transfer function.

$$G_{PI}(s) = \frac{K_P \cdot (1 + T_I \cdot s)}{T_I \cdot s} \tag{3.21}$$

In equation 3.21 the gain (proportional part) of the controller and the integral time constant are shown with K_P and T_I respectively. In order to choose these parameters for all four PI-controllers shown in figure 3.8 different optimizing methods are used to provide a balance between the controller settling time and the overshoot. As discussed in [95], [13], and [94], the selection of the parameter optimization method should be based on the given controlled part of the plant.

[4)] For the anti-windup block the limits of the voltage $\hat{U}_{s,max}$ and current $\hat{I}_{s,max}$ are determined according to the maximum values provided in machine datasheet.

This is presented the following for the four controllers shown in figure 3.8.

To select the parameters of the d-current controller ($K_{\mathrm{P,i,d}}$ and $T_{\mathrm{I,i,d}}$), it is required to calculate the open-loop transfer function of the motor current in d-axis including the current controller and the actuator (with reference to figure 3.8, from the input of d-controller to the actual d-current in feedback path). Figure 3.9 shows the equivalent block diagram of the d-current control loop. The PI-controller transfer function itself is given in equation 3.21, and the actuator (the inverter including its PWM modulator) is modeled using a delay block with the delay time (dead time) of T_{dead}. The amount of this dead time is dependent on the way that the modulator carrier signal is synchronized with the controller update rate and the measurement sampling rate. In this work the current and voltage measurements as well as the controller are synchronized with the carrier signal and are executed one time at the beginning of each switching period T_{sw}. As shown in [94], for such a configuration the dead time is equal to $1.5 \times T_{\mathrm{sw}}$.

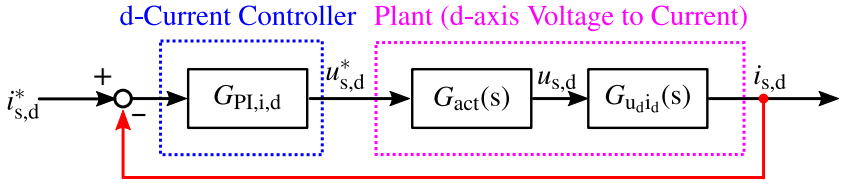

Figure 3.9: The current control loop of the motor d-axis consists of the PI current controller and the current controlled plant

To derive the transfer function of the stator voltage to the stator current in d-axis, equation 3.12 is used. In this derivation for the simplification the q-current component part in the d-axis voltage equation is neglected. Furthermore the derivative of the rotor magnetizing current ($\frac{di_{\mathrm{r,mg}}}{dt}$) term in equation 3.12 is calculated with the help of equation 3.18 and with respect to the stator d-current. Equation 3.22 shows the open-loop (OL) transfer function of the d-current path.

$$G_{\mathrm{OL,i_d}}(s) = \frac{K_{\mathrm{P,i,d}} \cdot \left(1 + T_{\mathrm{I,i,d}} \cdot s\right)}{T_{\mathrm{I,i,d}} \cdot s} \cdot \frac{1}{1 + T_{\mathrm{dead}} \cdot s} \cdot \frac{L'_{\mathrm{r}}}{\left(R_{\mathrm{s}} L'_{\mathrm{r}} + R'_{\mathrm{r}} \left(1 - \sigma_{\mathrm{eq}}\right) L_{\mathrm{s}}\right) + \sigma_{\mathrm{eq}} L_{\mathrm{s}} L'_{\mathrm{r}} \cdot s} \tag{3.22}$$

The d-current controller is designed with the help of a so-called magnitude-optimum method, which is a parameter optimization way performed in the frequency domain. Based on this method, to achieve a good dynamic response (reasonable settling time and overshoot) on the one side the bandwidth of the system should be maximized, and on the other side the ratio of the output to input amplitudes should be kept close to 1. In order to realize this, to achieve a higher bandwidth the slowest time constant of the plant is compensated by the controller (the zero of the controller transfer function should cancel out the smallest pole of the plant transfer function). Furthermore, to achieve lower overshoot, the magnitude of the resulting second-order closed-loop transfer function is set to 1 at frequencies lower than the natural frequency of the second-order system. As shown in [94], the latter requirement is fulfilled if the damping ratio of the resulting 2nd-order closed-loop is set to $\frac{1}{\sqrt{2}}$. As the result the gain and time constant of the

d-current controller are calculated using equations 3.23, 3.24, and 3.25.

$$T_{\mathrm{I,i,d}} = T_{\mathrm{N,s,d}} = \frac{\sigma_{\mathrm{eq}} \cdot T_{\mathrm{r}} \cdot T_{\mathrm{s}}}{T_{\mathrm{r}} + (1-\sigma_{\mathrm{eq}}) \cdot T_{\mathrm{s}}} \qquad \text{with} \qquad T_{\mathrm{s}} = \frac{L_{\mathrm{s}}}{R_{\mathrm{s}}}, \quad \text{and} \quad T_{\mathrm{r}} = \frac{L'_{\mathrm{r}}}{R'_{\mathrm{r}}}. \tag{3.23}$$

$$K_{\mathrm{P,i,d}} = \frac{T_{\mathrm{I,i,d}}}{2 \cdot K_{\mathrm{N,s,d}} \cdot T_{\mathrm{dead}}} \tag{3.24}$$

$$K_{\mathrm{N,s,d}} = \frac{T_{\mathrm{r}} \cdot T_{\mathrm{s}}}{L_{\mathrm{s}} \cdot (T_{\mathrm{r}} + (1-\sigma_{\mathrm{eq}}) \cdot T_{\mathrm{s}})}. \tag{3.25}$$

In the equations above, T_{s} and T_{r} are the stator and rotor electric time constants, and $K_{\mathrm{N,s,d}}$ and $T_{\mathrm{N,s,d}}$ are the gain and pole of the stator d-axis voltage to d-axis current transfer function respectively.

The magnitude-optimum method is used for the q-current controller design as well. The actuator transfer function is approximated with the same delay block as above, and the q-voltage to q-current transfer function is derived with the help of equation 3.12 (this time the d-current component is assumed as a disturbance source and is excluded from the equation as a simplification). With this, the controller gain and time constant are presented in equations 3.27 and 3.26 respectively.

$$T_{\mathrm{I,i,q}} = T_{\mathrm{N,s,q}} = \sigma_{\mathrm{eq}} \cdot T_{\mathrm{s}} \tag{3.26}$$

$$K_{\mathrm{P,i,q}} = \frac{T_{\mathrm{I,i,q}}}{2 \cdot K_{\mathrm{N,s,q}} \cdot T_{\mathrm{dead}}} \tag{3.27}$$

In the equation above, $K_{\mathrm{N,s,q}}$ is the gain of the stator q-axis voltage to q-axis current transfer function and calculated as in the following equation.

$$K_{\mathrm{N,s,q}} = \frac{1}{R_{\mathrm{s}}} \tag{3.28}$$

The last controller which uses the magnitude-optimum method is the magnetizing current controller with the resulting parameters shown in equations 3.29 and 3.30. To derive the parameters, the transfer function of the inner d-current control loop is approximated with a delay block with the delay value of $2 \cdot T_{\mathrm{dead}}$ (obtained from the d-current closed-loop transfer function), and the corresponding transfer function of the d-current to magnetizing current is calculated using 2.59.

$$T_{\mathrm{I,i,mg}} = T_{\mathrm{r}} \tag{3.29}$$

$$K_{\mathrm{P,i,mg}} = \frac{(1+\sigma_{\mathrm{r}}) \cdot T_{\mathrm{r}}}{4 \cdot T_{\mathrm{dead}}} \tag{3.30}$$

Last but not least is the design of the rotation speed controller. With respect to the fact that the speed open-loop transfer function derived from equations 2.60 and 3.20 includes an integrator term, the magnitude-optimum method used in the design of the other three controllers cannot be employed here (unstable closed-loop system). Therefore, another method which focuses on realizing the maximum phase margin of the system (and with that the optimum damping behavior) is deployed for the speed controller parameter design. Based on this method, which is called symmetrical-optimum ([96]), the zero-dB frequency (crossover frequency) of the open-loop transfer function is placed exactly in the geometric mean of the frequencies of the PI-controller zero and controlled plant pole (the name is arises from the resulting symmetry of bode phase plot with respect to the crossover frequency). The controller parameters [5)] ($T_{\mathrm{I},\omega}$ and $K_{\mathrm{P},\omega}$) as well as the gain of the q-current to rotation speed transfer function ($K_{\mathrm{N},\omega}$) are presented in equations 3.31 to 3.33.

$$T_{\mathrm{I},\omega} = 8 \cdot T_{\mathrm{dead}} \tag{3.31}$$

$$K_{\mathrm{P},\omega} = \frac{1}{4 \cdot T_{\mathrm{dead}} \cdot K_{\mathrm{N},\omega}} \tag{3.32}$$

$$K_{\mathrm{N},\omega} = \frac{\frac{3}{2} p \cdot L_{\mathrm{m}} \cdot i_{\mathrm{r,mg}}}{J_{\mathrm{R}}} \tag{3.33}$$

Figure 3.10 shows the different parts of the inverter-fed induction machine model and controller implemented for the power losses evaluation. As stated before the machine model as well as the inverter model are implemented using PLECS toolbox and the rest of the system is implemented in SIMULINK.

With the help of the provided system shown in figure 3.10 the 4-quadrant operation of the machine control system has been evaluated and is presented in the following. For this evaluation a simulation has been run with a constant DC-Link voltage set to 300 V and a variable speed which covers both the accelerating and the braking operation of the machine. The results of this simulation are presented in figure 3.11. Based on the implemented test case the machine is being magnetized during the first 0.5 seconds and the set point of the rotor magnetizing current will be reached (figure 3.11 (c)). At the end of this period the machine starts accelerating to the nominal speed of 2400 rpm (figure 3.11 (a)). As it is shown in figure 3.11 (b) during the acceleration the produced torque reaches its nominal value and it is correlated with the q-component of the

[5)] The detailed parameter calculation procedure is presented in the voltage controller design of the DC-DC converter (section 3.2.3), which is applied here as well.

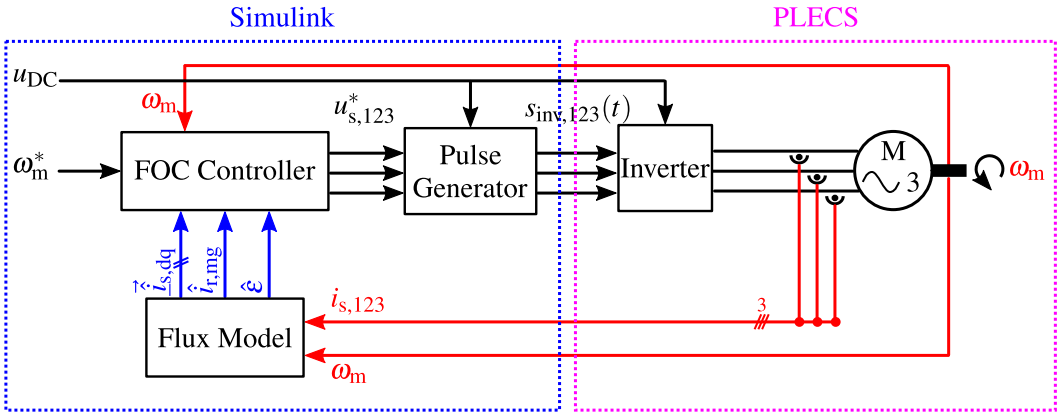

Figure 3.10: The entire control system of the inverter-fed machine consists of inverter model and machine model implemented using PLECS toolbox and the flux model, controller, and modulator implemented in SIMULINK

stator current vector (figure 3.11 (d)). At 0.7 seconds the machine starts breaking to rotate in the reverse direction with the nominal speed, and the torque reaches the nominal negative value. Finally the machine is accelerated to zero speed and with that the complete 4-quadrant operation is covered. The simulation results verifies the complete functionality of the field oriented control scheme, since all the set points are followed by the actual values precisely.

3.1.4 State-Space Average Model

As stated in section 3.1.1 the PLECS-based inverter model is a complete transient model which provides the circuit equivalent electrical and thermal differential equations (with the help of the imported temperature dependent characteristics of the power transistors) to the SIMULINK solver including each switching toggle of the inverter. Based on these information the SIMULINK solver calculates the exact operating point, operating temperature, and the power losses of each component independently. In addition to that, the control system is also being executed in parallel, and all this makes the entire simulation very slow. This is not critical for a few operating points, but for the evaluation of a complete driving cycle, the simulation time will be unacceptably long. Therefore, a method is to be developed to estimate the switching model of the inverter in terms of operating point and power losses.

To solve this problem, a simplified model has been provided to calculate the operating point of the components based on the state-space averaging (SSA) technique [97]. In the new system, instead of modeling the inverter in PLECS, a SIMULINK-based average model is provided which estimates the inverter output voltages based on their average values during each switching period. To realize this model, the inverter shown in figure 3.10 is removed and replaced with an ideal three phase controllable voltage source to provide the input voltage of the connected machine. Furthermore the inverter PWM signals $s_{inv,123}(t)$ at the pulse generator output are terminated, and the voltage set points of the three phase source are provided using the normalized value of the inverter output voltages $u'^*_{s,123,norm}$. These are calculated inside the space vector

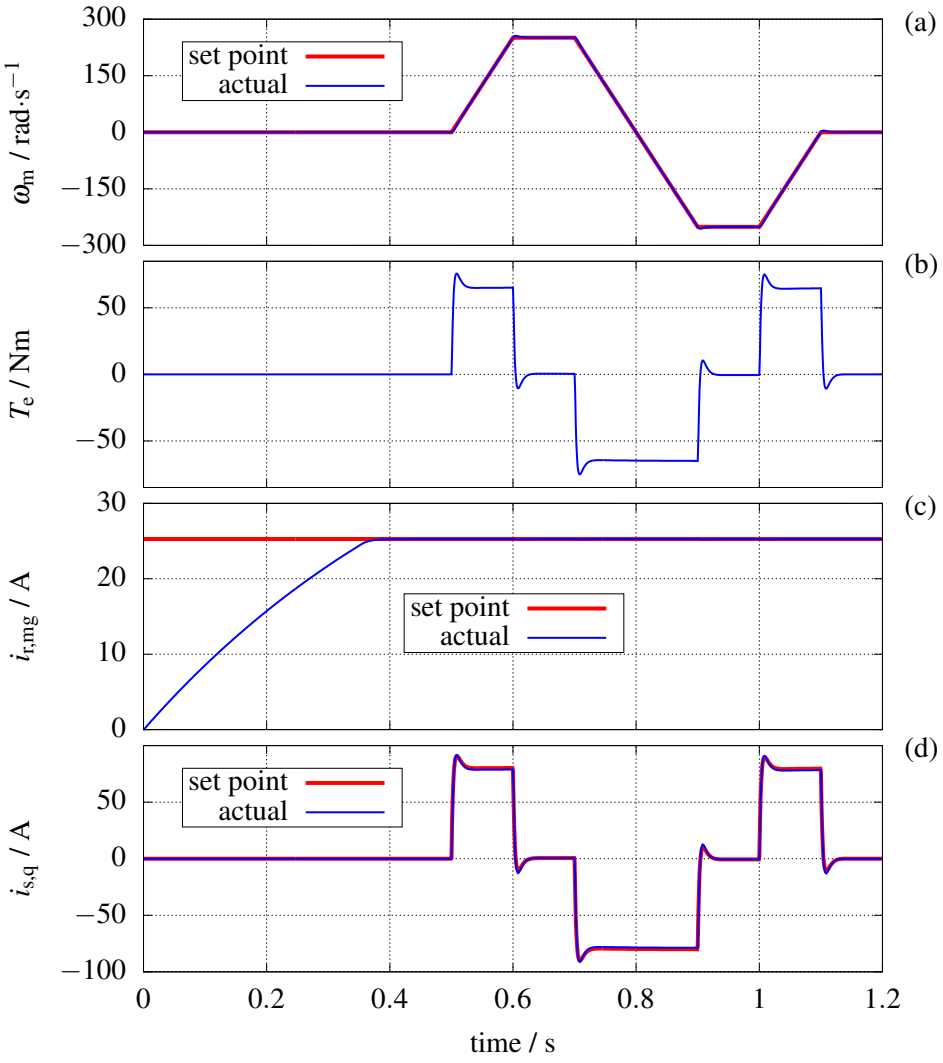

Figure 3.11: The simulation results of the induction machine driven by an inverter with 300 V DC-link voltage, SVM modulation and field oriented control system (a) rotation speed (b) produced electric torque (c) rotor magnetizing current (d) rotor d-axis current

modulator block and in its pulse generator unit which includes the added SVM zero voltage component of equation 3.8 (figure 3.6). Since these values are the normalized voltages referenced to the inverter DC-Link middle point, they should be scaled up to provide the control signals of the three phase voltage source as follows:

$$u'^{*}_{s,123} = u'^{*}_{s,123,norm} \cdot \frac{u_{DC}}{2}. \tag{3.34}$$

Figure 3.12 shows the SIMULINK-based SSA model integrated into the rest of the system, in which the same field oriented controller, flux model, and induction machine model[6)] are

[6)]The model of the induction machine is still implemented in PLECS since it does not include any temperature dependent state and it is not much computation intensive.

used. Figure 3.13 presents a comparison between the PLECS model and the state-space average model in terms of the control system behavior and induction machine operating point. As it is clear the SSA model has a very good match with the switching model of the system.

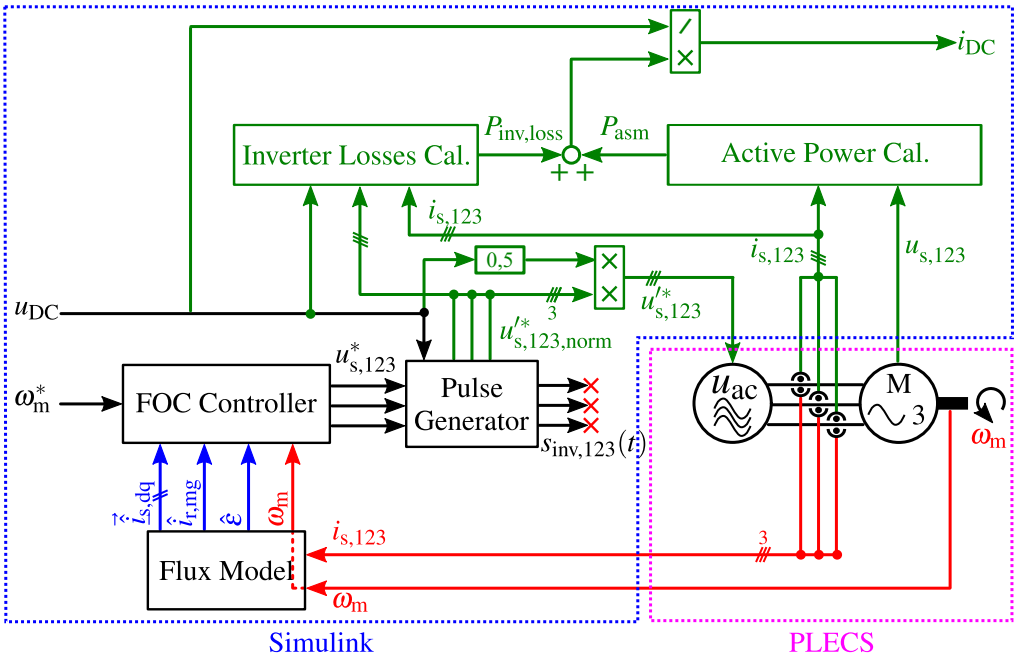

Figure 3.12: SIMULINK-based state-space average model of the inverter (including the inverter power loss calculation module) integrated into the control system of the inverter-fed machine implemented in SIMULINK

Another important objective that should be fullfield by the SSA model is the implementation of a temperature dependent power loss calculation unit. This should estimate the inverter losses based on the input voltage, switching frequency and the induction machine operating point. These power losses will then be added to the input power of the induction machine and determine together the total power which should be delivered by the DC-Link. The result will be used later as the output load of the DC-DC converter.

The power consumption of the induction machine is calculated using the motor voltage and current at the given operating point of the machine. Equation 3.35 presents the formula implemented in the motor power calculation unit in figure 3.12.

$$P_{asm}(t) = u_{s,1}(t) \cdot i_{s,1}(t) + u_{s,2}(t) \cdot i_{s,2}(t) + u_{s,3}(t) \cdot i_{s,3}(t) \tag{3.35}$$

In the inverter power loss unit of figure 3.12 the losses are calculated with the help of power module look-up-tables and equations introduced in section 2.3, which provide the switching energy losses as well as the forward voltage drop of the power transistor and the anti-parallel diode for a given current, blocking voltage, and temperature. According to the inverter operating principle, in an inverter leg only one transistor[7)] and its complimentary diode are conducting

[7)] Based on the current direction, either high-side transistor (+ current) or low-side transistor (- current).

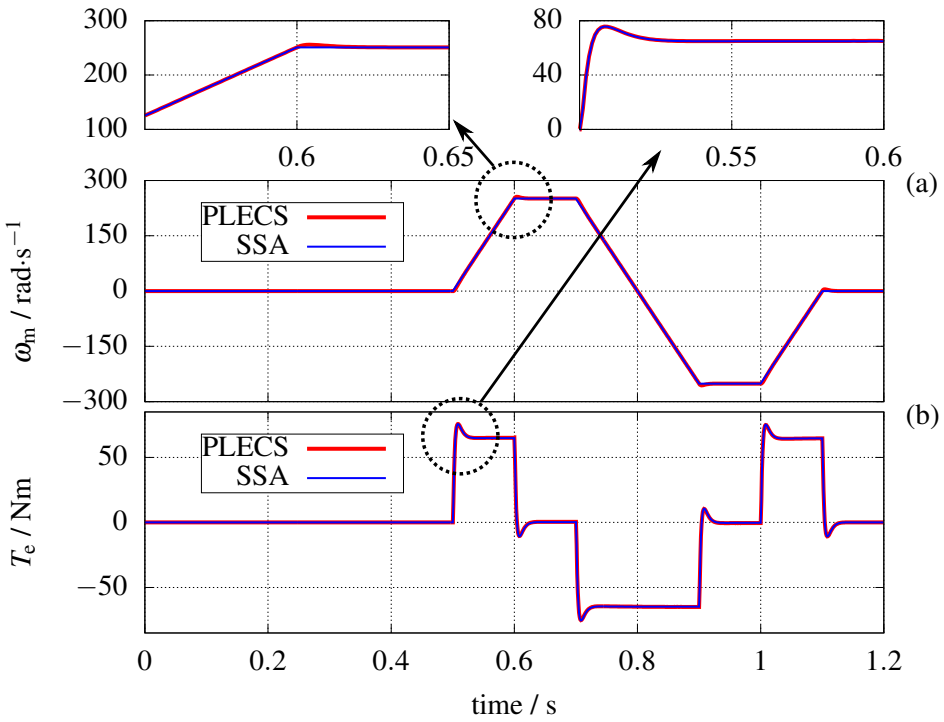

Figure 3.13: Comparison between the state-space average model and the PLECS model in terms of induction machine operating point (a) rotational speed (b) electric torque

the current during a given switching period. Therefore the losses of each leg composed of two elements at a time, namely: the high-side transistor losses + complimentary diode losses for the positive phase currents (same current direction as shown in figure 3.2) or the low-side transistor losses + complimentary diode losses for the negative phase currents. In the following these losses are quantitatively calculated, and in the evaluation process, based on the sign of the motor current either of the high-side or low-side transistor losses (including its corresponding complimentary diode) are included in the overall transient loss calculation process.

The conduction losses of the transistor (or its complimentary diode) are calculated by multiplying the forward voltage drop of the corresponding component with its average current value during a switching period (this is calculated by using the duty cycle of the transistor or its complimentary diode). Equations 3.36 and 3.37 are the equations implemented in the SIMULINK to evaluate the conduction losses of the transistor and complimentary diode in each leg. It should be noted that the high-side transistor and its complimentary diode (low-side transistor and its complimentary diode) generate losses only during the the positive (negative) half-wave of the motor current, and this is considered in the equation implementation. In other words the losses are calculated and attached to the corresponding loss generating components of each leg based on the current

direction.

$$P_{\text{loss,T}_\text{i},\text{cond}}(t) = \frac{1+u'^{*}_{\text{s,i,norm}}(t)}{2} \cdot \left|i_{\text{s,i}}(t)\right| \cdot u_{\text{T}}(t) \quad \text{with} \quad u_{\text{T}}(t) = f(\left|i_{\text{s,i}}(t)\right|, \theta_{\text{T,i}}(t)) \tag{3.36}$$

$$P_{\text{loss,D}_\text{i},\text{cond}}(t) = \frac{1-u'^{*}_{\text{s,i,norm}}(t)}{2} \cdot \left|i_{\text{s,i}}(t)\right| \cdot u_{\text{F}}(t) \quad \text{with} \quad u_{\text{F}}(t) = f(\left|i_{\text{s,i}}(t)\right|, \theta_{\text{D,i}}(t)) \tag{3.37}$$

The switching energy losses can directly be extracted from the corresponding LUTs or equations presented in section 2.3 for IGBTs. They should then be scaled up or down to the ratio of the the blocking voltage to reference voltage (the voltage for which the energy losses are calculated or declared in datasheet) and multiplied with the switching frequency as shown in the following equations.

$$P_{\text{loss,T}_\text{i},\text{sw,on}}(t) = f_{\text{sw}} \cdot W_{\text{T}_\text{i},\text{sw,on}}(t) \cdot \frac{u_{\text{DC}}}{U_{\text{ref}}} \quad \text{with} \quad W_{\text{T}_\text{i},\text{sw,on}}(t) = f(\left|i_{\text{s,i}}(t)\right|, \theta_{\text{T,i}}(t)) \tag{3.38}$$

$$P_{\text{loss,T}_\text{i},\text{sw,off}}(t) = f_{\text{sw}} \cdot W_{\text{T}_\text{i},\text{sw,off}}(t) \cdot \frac{u_{\text{DC}}}{U_{\text{ref}}} \quad \text{with} \quad W_{\text{T}_\text{i},\text{sw,off}}(t) = f(\left|i_{\text{s,i}}(t)\right|, \theta_{\text{T,i}}(t)) \tag{3.39}$$

$$P_{\text{loss,D}_\text{i},\text{RRM}}(t) = f_{\text{sw}} \cdot W_{\text{D}_\text{i},\text{RRM}}(t) \cdot \frac{u_{\text{DC}}}{U_{\text{ref}}} \quad \text{with} \quad W_{\text{D}_\text{i},\text{RRM}}(t) = f(\left|i_{\text{s,i}}(t)\right|, \theta_{\text{D,i}}(t)) \tag{3.40}$$

The calculated power losses of the transistor and its complimentary diode in each inverter leg are then fed back into the corresponding thermal network (the Foster network introduced in section 2.3.3) to evaluate the average temperature of the components at the end of each switching period. The calculated temperatures along with the measured phase currents are then used as the inputs of the LUT blocks to provide the required values for the evaluation of equations 3.36 to 3.40. The following figure shows the power losses calculation unit implemented in SIMULINK. In figure 3.14 an ideal heat-sink is assumed with a constant temperature of a typical value in electric vehicles (according to [57] around 70°C).

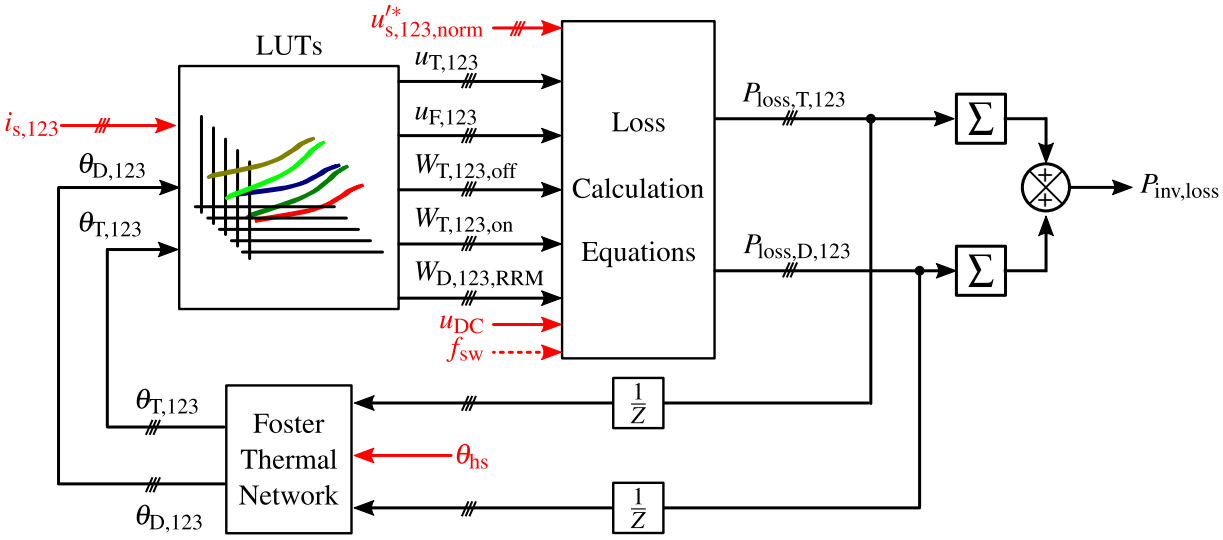

Figure 3.14: SIMULINK unit for power loss calculation of the inverter SSA-model

After implementing the SSA model, in this part a comparison is made between the PLECS-based model and the developed SSA-model in terms of power losses and energy losses, in order to evaluate the accuracy of the SIMULINK-based power loss unit of figure 3.12. For this comparison the same 4-quadrant test case presented in figure 3.11 with the inverter switching frequency of 10 kHz is used. Figure 3.15 (a) shows the power losses of the PLECS-model and the SSA-model, and Figure 3.15 (b) presents the calculated energy losses during the mentioned test case for each of the models. As it can be seen in the figure the difference between the average model and the switching model stays below 0.53% during the entire cycle which proves the accuracy of the SSA-model.

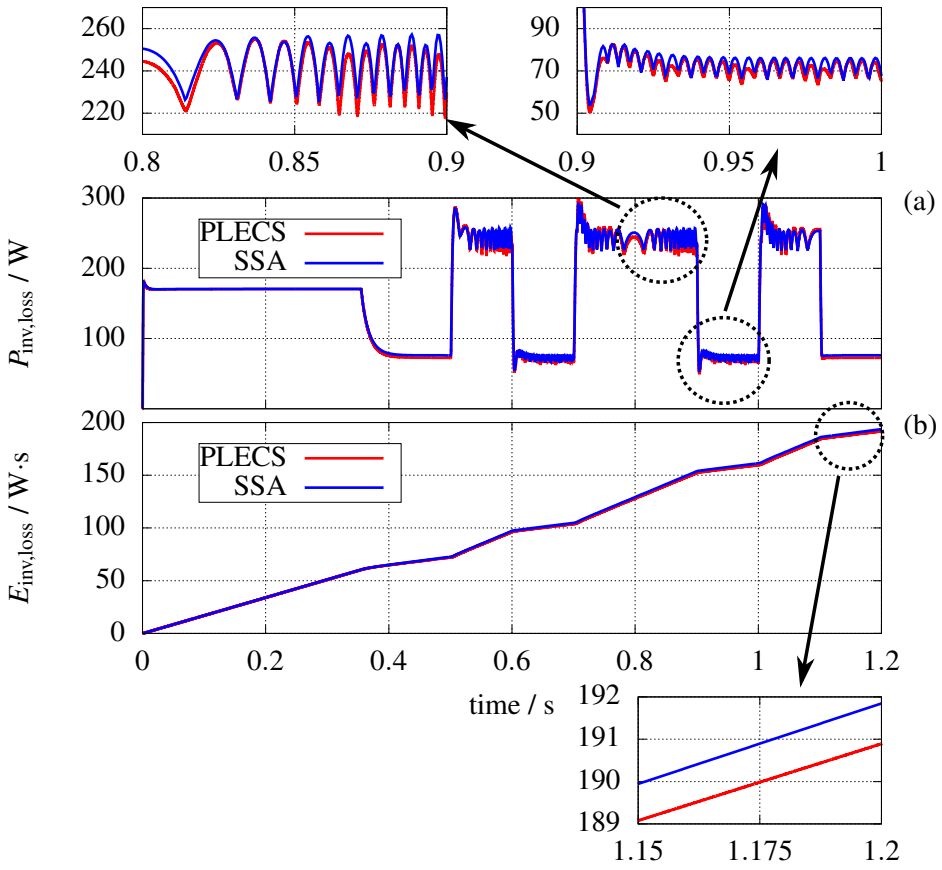

Figure 3.15: A comparison between the PLECS-based model and the developed SSA-model in terms of (a) power losses and (b) energy losses

3.2 Multiphase Interleaving DC-DC Converter

As shown in figure 3.1 a DC-DC converter is used in the drivetrain as an extension in order to provide the option of changing the DC-Link voltage to optimize the inverter operation in terms of power losses. There are different topologies to realize such DC-DC converter which

are reviewed in [34]. For this kind of application, the single-phase bidirectional boost converter is a common topology which provides a reasonably high efficiency for voltage conversion ratios between two and five [35].

However, using a single-phase converter has some drawbacks. On the one hand, maintaining the current and voltage ripples in an acceptable limit will lead large passive components. On the other hand, the converter has to be designed for the maximum output power of the vehicle which causes relatively high power losses at partial loads. In order to overcome the drawbacks and utilize the converter more efficiently, a multiphase topology is used in this work. This provides the possibility to operate with a variable number of active phases with respect to the output power, and consequently to reduce the losses at partial loads. An interleaving switching strategy with variable switching frequency described in [98] is used as well, in order to reduce the input current ripple of the converter even further. Figure 3.16 shows the basic structure of a 3-phase step-up DC-DC converter. In the following subsections the transient model, control system, and state-space average model of the converter along with some simulation results are presented.

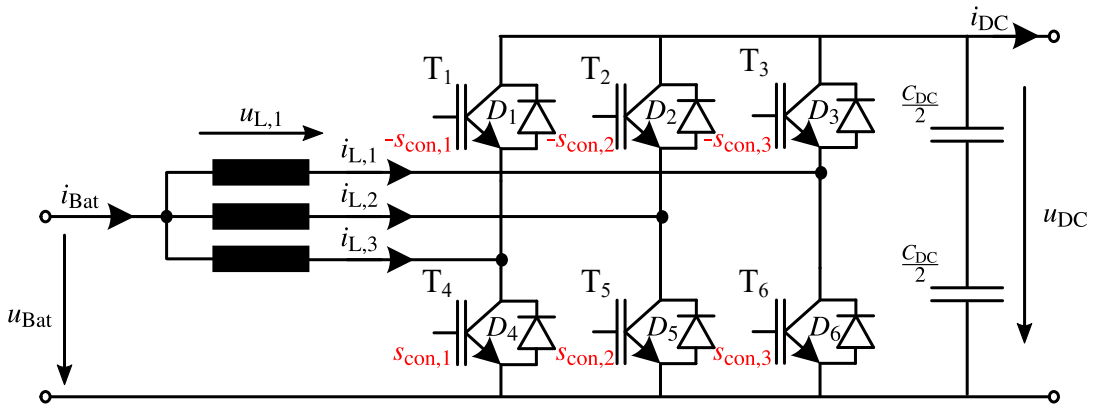

Figure 3.16: Basic structure of a multiphase (3-phase in this case) bidirectional DC-DC voltage converter (step-up)

3.2.1 Transient Model

The converter shown in figure 3.16 consists of three conventional boost converters connected together at the input side and working on the same DC-Link capacitor. For the sake of simplicity at first the operating principle of a single phase boost converter is presented, which then will be extended to a 3-phase unit. In a convectional boost converter the output voltage is controlled by the duty cycle of the half-bridge (in the case of the step-up converter duty cycle is the switch-on time ratio of the low-side to the high-side). The value of the voltage is calculated on the basis of the fact that for a steady-state operating point of the converter to avoid saturation of the inductor core, the average voltage of the inductor $\overline{u}_L$ during a switching period should be zero. Assuming a constant input voltage and output voltage and using ideal power semiconductors, the equations for the induced voltage for two converter states during one switching period are given in the

following equations.

$$u_{\mathrm{L}}\Big|_{\text{low-side on}} = u_{\mathrm{Bat}} \tag{3.41}$$

$$u_{\mathrm{L}}\Big|_{\text{high-side on}} = u_{\mathrm{Bat}} - u_{\mathrm{DC}} \tag{3.42}$$

With respect to the given duty cycle d_{L} the average value of the inductor voltage during a switching period is calculated using equation 3.43.

$$\overline{u}_{\mathrm{L}} = d_{\mathrm{L}} T_{\mathrm{sw}} \cdot u_{\mathrm{Bat}} + (T_{\mathrm{sw}} - d_{\mathrm{L}} T_{\mathrm{sw}}) \cdot (u_{\mathrm{Bat}} - u_{\mathrm{DC}}) \tag{3.43}$$

As mentioned above, in the stationary state equation 3.43 is equal to zero, and consequently the output voltage of the converter with respect to the duty cycle and battery voltage is calculated as follows:

$$u_{\mathrm{DC}} = \frac{u_{\mathrm{Bat}}}{1 - d_{\mathrm{L}}}. \tag{3.44}$$

Figure 3.17 shows the switching signal of the half-bridge as well as the inductor voltage and current waveforms (for an ideal converter) in a stationary operating point with a load current equal to zero. According to the EV application the battery current during the operation can also become negative (energy recuperation at braking intervals). Therefore, a bidirectional topology is chosen to realize this 2-quadrant operation requirement. Figure 3.17 (c) shows the conducting elements of the half-bridge during a switching period in case of zero load current. As expected by toggling the inductor current sign the transistor or the anti-paralleled diode takes over the current flow.

Same as the inverter transient model implementation described in section 3.1.1 the multiphase converter is also implemented in SIMULINK using PLECS toolbox. For the converter the electrical and thermal characteristics of HybridPACK 2 IGBT module are imported in the PLECS. This results in a switching model of the converter, with which the operating point and power losses (including conduction losses and switching losses) of the power transistors (and anti-paralleled diodes) are calculated under consideration of each switch state. Table 3.2 shows the specifications of the rest of the components used in the converter.

It should be mentioned that the inductor and the DC-Link capacitors are modeled in the PLECS as ideal lossless components and the detailed loss model of them are implemented in SIMULINK as described in chapter 2. In the capacitor model (EPCOS *B25655J4507K*) the ohmic losses and dielectric losses are included as described in section 2.1 and figure 2.6. In the inductor model

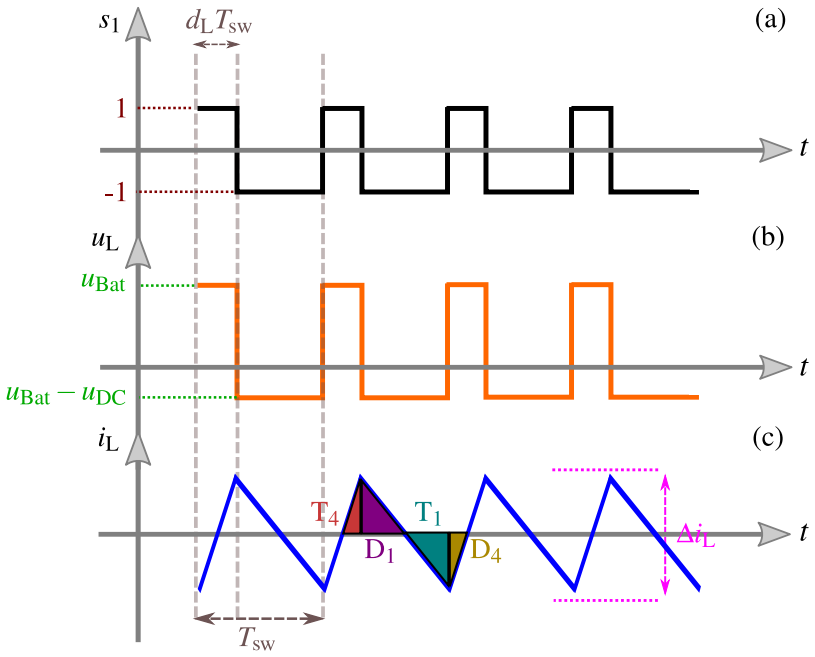

Figure 3.17: Stationary operating point of an ideal (lossless) 1-phase bidirectional step-up converter with zero load current ($i_{DC} = 0$) (a) half-bridge switching signal (b) inductor voltage (c) inductor current

Table 3.2: Rating specifications of the components used in the three phase interleaving DC-DC converter

Description	Designator	Value	Unit
Battery voltage	u_{Bat}	110	V
DC-Link capacitor	c_{DC}	500	μF
Inductance per phase	L_i	300	μH
Inductor ohmic resistance @25°C	$R_{L,cu,0}$	10.6	mΩ

the copper losses and core losses are included as presented in subsections 2.2.1 and 2.2.2, and figures 2.9 and 2.14 respectively. Both SIMULINK-based loss models are fed by the operating point of the converter calculated in the PLECS model.

3.2.2 Interleaving Pulse Generator

The converter half-bridge pulses shown in figure 3.16 are provided by the so-called interleaving pulse generator unit of figure 3.18. The term interleaving refers to a fixed time offset (phase shift) between the inverter phases. The phase lags $\phi_{lag,i}$ are used as the input of the triangular carrier blocks and their outputs together with duty cycles $d_{L,i}$ form the inputs of the comparators.

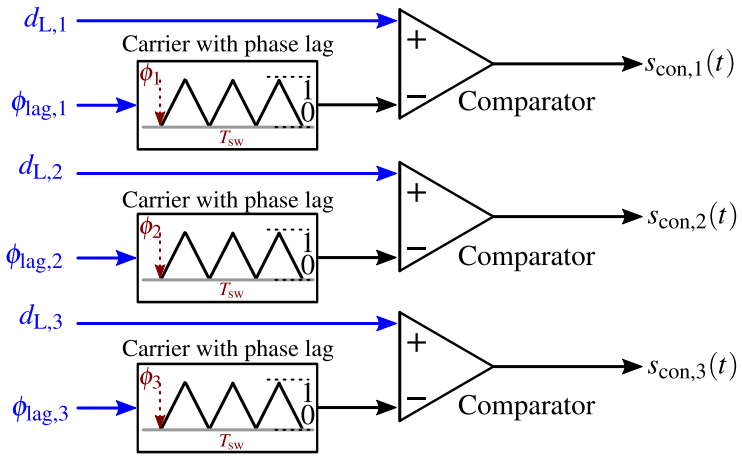

Figure 3.18: Interleaving pulse generator of a three phase DC-DC converter

According to the interleaving switching scheme the phase shift between the half-bridge pulse trains is determined depending on the number of active half-bridges of the cnverter (N_{ph}) and equals:

$$\phi_{lag} = \frac{2\pi}{N_{ph}}. \tag{3.45}$$

The main advantages of using interleaving scheme is the frequency increase of the input current ripple ($f_{\Delta i_{Bat}}$) on one hand, and the amplitude reduction of the battery current ripple Δi_{Bat} on the other hand. According to [23], in the stationary operation the battery current ripple of a multiphase interleaving DC-DC converter is calculated as shown in equation 3.46.

$$\Delta i_{Bat} = \frac{u_{DC}}{L \cdot f_{sw}} \cdot \left(d_L - \frac{x}{N_{ph}} \right) \cdot \left(x + 1 - N_{ph} \cdot d_L \right) \tag{3.46}$$

$$\text{in which} \qquad d_L \in \langle \frac{x}{N_{ph}} \cdots \frac{x+1}{N_{ph}} \rangle; \quad N_{ph} = 1 \cdots \infty; \quad x = 0 \cdots (N_{ph} - 1)$$

Figure 3.19 shows the normalized value of the battery current ripple for an interleaving converter with different number of active phases. Based on this figure, a decreasing battery current ripple over the entire duty cycle range (wide range of input to output voltage ratio) is observable as a higher number of phases operate actively in interleaving mode. The lower current ripple is also achievable with the help of the interleaving operation at the DC-Link side and for the DC-Link capacitor current. This feature of the interleaving operation can be used to reduce to DC-Link capacitor power losses (in comparison with a non-interleaving converter), or optimize the size of the output capacitor to meet the maximum DC-Link voltage ripple requirement. Another possibility is to optimize the half-bridges in terms of power losses by changing the number of active phases or decreasing the switching frequency of the converter. This power loss optimizing

strategy will be presented in detail in chapter 4.

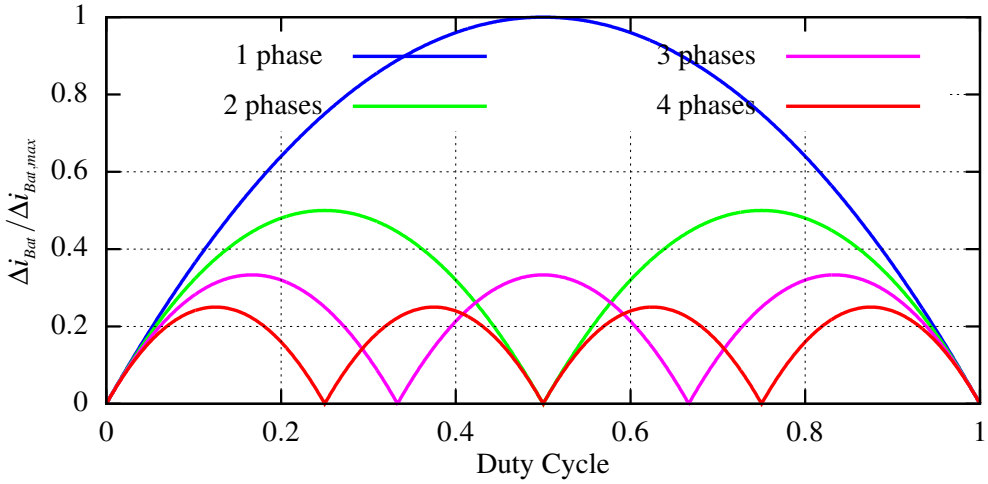

Figure 3.19: Normalized input current ripple of an interleaving multiphase DC-DC converter with different number of active phases

3.2.3 Control System

In this section the control system design of the multiphase interleaving DC-DC converter is discussed. The objective is to implement a controller which ensures a constant output voltage under different disturbances such as variable PWM switching frequencies, variable number of active phases, and variable output load demanded by the inverter-fed machine. To be able to design the controller and select the optimal controller parameters, at first, the mathematical model of the multiphase converter including its load should be determined. In the drivetrain application the inverter-fed machine can be modeled as a constant power load to replicate the correct dynamics at the load side of the DC-DC converter. But in this section, as the starting point and for the controller parameter selection, the load of the converter is modeled as a pure resistive load. This will simplify the rather complicated non-linear dynamic equations of the converter output voltage. It should be noted that later for the evaluation of the controller dynamic performance, the real model of the inverter and electric machine are used at the output of the DC-DC converter.

In a conventional single-phase bidirectional boost converter, the differential equations of the inductor current i_{L} and output voltage u_{DC} with respect to the duty cycle of the low-side switch d_{L}, inductance L and DC-Link capacitance C_{DC} for a given resistive load R are calculated as follows:

$$\frac{di_{\mathrm{L}}}{dt} = \frac{u_{\mathrm{Bat}}}{L} - \frac{(1-d_{\mathrm{L}})u_{\mathrm{DC}}}{L} \tag{3.47}$$

$$\frac{du_{\mathrm{DC}}}{dt} = \frac{(1-d_{\mathrm{L}})i_{\mathrm{L}}}{C_{\mathrm{DC}}} - \frac{u_{\mathrm{DC}}}{RC_{\mathrm{DC}}}. \tag{3.48}$$

Regarding the system state variables, equations 3.47 and 3.48 are non-linear equations, and it is not possible to make a frequency analysis of the system behavior with the help of Laplace transform. A common linearization method is to rewrite the equations in the vicinity of a given operating point and build a small-signal model of the system as described in [35]. The results of this linearization are shown in equations 3.49 and 3.50.

$$\frac{d\tilde{i}_\mathrm{L}}{dt} = \frac{1}{L}\tilde{u}_\mathrm{Bat} - \frac{(1-D_\mathrm{L})}{L}\tilde{u}_\mathrm{DC} + \frac{U_\mathrm{DC}}{L}\tilde{d}_\mathrm{L} \tag{3.49}$$

$$\frac{d\tilde{u}_\mathrm{DC}}{dt} = \frac{(1-D_\mathrm{L})}{C_\mathrm{DC}}\tilde{i}_\mathrm{L} - \frac{1}{RC_\mathrm{DC}}\tilde{u}_\mathrm{DC} - \frac{I_L}{C_\mathrm{DC}}\tilde{d}_\mathrm{L} \tag{3.50}$$

In the equations above, U_DC, I_L and D_L represent the given operating point, and the differential equations describe the system behavior near this stationary operating point with respect to the small-signal variables $\tilde{x}$. Another point worth mentioning is that (3.49) and (3.50) are only valid for continuous current conduction mode which is the case for a bidirectional boost converter with complementary operation of the low-side and high-side switches. At this point, the transfer function of the system can be calculated using Laplace transform of the small-signal model. For a negligible input voltage ripple, the duty ratio to inductor current transfer function and the inductor current to output voltage transfer function are given as

$$G_\mathrm{di}(s) = \left.\frac{\tilde{i}_\mathrm{L}}{\tilde{d}_\mathrm{L}}\right|_{\tilde{u}_\mathrm{Bat}=0} = \frac{RC_\mathrm{DC}U_\mathrm{DC}\cdot s + U_\mathrm{DC} + (1-D_\mathrm{L})I_\mathrm{L}R}{RLC_\mathrm{DC}\cdot s^2 + L\cdot s + (1-D_\mathrm{L})^2 R} \tag{3.51}$$

$$G_\mathrm{iu}(s) = \left.\frac{\tilde{u}_\mathrm{DC}}{\tilde{i}_\mathrm{L}}\right|_{\tilde{u}_\mathrm{Bat}=0} = \frac{-RI_\mathrm{L}L\cdot s + (1-D_\mathrm{L})U_\mathrm{DC}R}{RC_\mathrm{DC}U_\mathrm{DC}\cdot s + U_\mathrm{DC} + (1-D_\mathrm{L})I_\mathrm{L}R}. \tag{3.52}$$

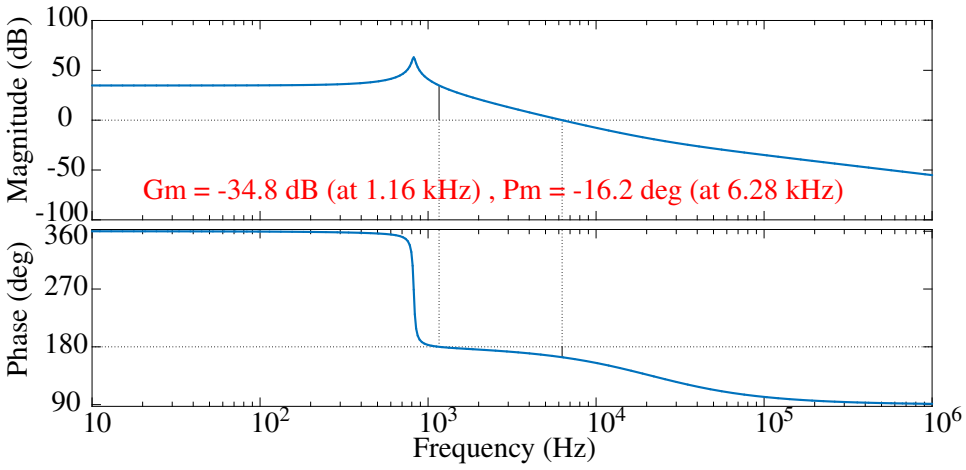

Figure 3.20: The frequency response of the output voltage with respect to the duty cycle as the input which is unstable because of the high resonance pole

Figure 3.20 represents the frequency response of the converter small-signal model for the given parameters of $u_{Bat} = 110$ V, $L = 300\ \mu H$, and $C_{\mathrm{DC}} = 500\ \mu F$ and in the vicinity of the stationary operating point with 50% duty cycle and a load equal to 11 Ω. It is clear that this system has a high resonance pole in the duty ratio to inductor current transfer function which causes the intrinsic instability of the closed-loop system without the controller (phase margin of -16.2 deg and gain margin of -24.8 dB).

By defining a new auxiliary variable instead of the duty ratio in such a way that it cancels out this high resonance pole, it is possible to round the open-loop behavior of the controlled plant. This method is called nonlinear feedforward scheme ([99]). In the case of an step-up converter the inductor voltage is defined to be the new auxiliary variable as shown in equation 3.53. The idea is to use the inductor voltage as the new virtual input of the controlled plant. This inductor voltage can then be converted to the real input of the controlled system, i.e. the duty cycle, using the voltage measurements and the equation 3.53.

$$d_{\mathrm{L}} = 1 + \frac{u_{\mathrm{L}} - u_{\mathrm{Bat}}}{u_{\mathrm{DC}}} \tag{3.53}$$

By replacing the newly defined variable in equations 3.49 and 3.50, the small-signal model transfer functions are given as follows:

$$G_{\mathrm{u_L i}}(s) = \frac{\tilde{i}_{\mathrm{L}}}{\tilde{u}_{\mathrm{L}}}\bigg|_{\tilde{u}_{\mathrm{Bat}}=0} = \frac{1}{L \cdot s} \tag{3.54}$$

$$G_{\mathrm{iu}}(s) = \frac{\tilde{u}_{\mathrm{DC}}}{\tilde{i}_{\mathrm{L}}}\bigg|_{\tilde{u}_{\mathrm{Bat}}=0} = \frac{U_{\mathrm{DC}}}{I_{\mathrm{L}}} \frac{-LI_{\mathrm{L}}/U_{\mathrm{Bat}} \cdot s + 1}{RC \cdot s + 2}. \tag{3.55}$$

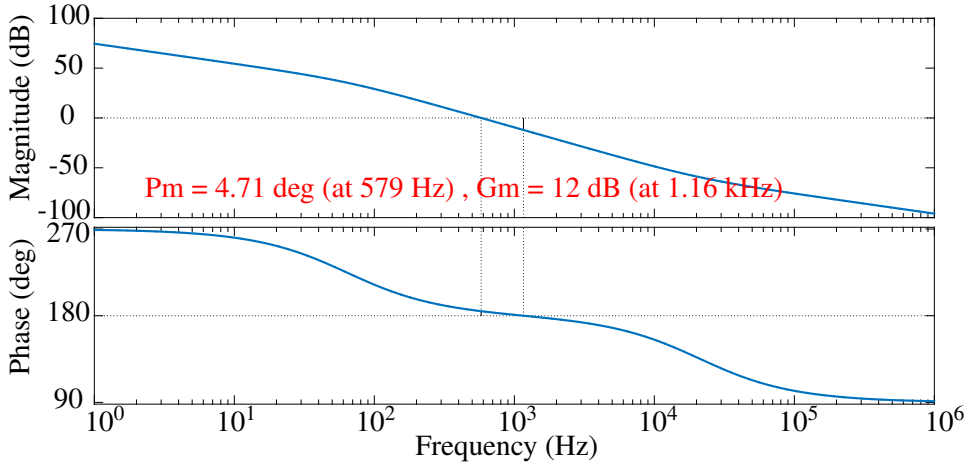

Figure 3.21: The frequency response of the output voltage with respect to the new auxiliary variable as the input, which shows the compensation of the high resonance pole

The frequency response of the system for the same stationary operating point shows that the high resonance pole is compensated (figure 3.21). With the help of the new regulating variable (inductor voltage, u_{L}^{*}) as the input of the under-controlled plant, the control system can be split into two parts: the inductor current controller with the inductor voltage reference value as its output (inner control loop), and the output voltage controller with the inductor current reference value as its output (outer control loop). They are placed in a cascade structure, and realized using two PI controllers, as in equation 3.56, equipped with anti-windups.

$$G_{\mathrm{PI}}(s) = K_{\mathrm{P}} \frac{1 + T_{\mathrm{I}} \cdot s}{T_{\mathrm{I}} \cdot s} \tag{3.56}$$

3.2.3.1 Current Controller Design

In order to design the current controller with the help of the new control variable (the inductor voltage shown equation 3.53) the transfer function of the controlled plant should be evaluated (figure 3.22). By extending the model of the inductor and including its ohmic resistance in equation 3.54, the inductor voltage set point with respect to the inductor current is calculated as follows:

$$u_{\mathrm{L}}^{*} = u_{\mathrm{Bat}} - (1 - d_{\mathrm{L}}) \cdot u_{\mathrm{DC}} = R_{\mathrm{L,cu,0}} \cdot i_{\mathrm{L}} + L \cdot \frac{di_{\mathrm{L}}}{dt}, \tag{3.57}$$

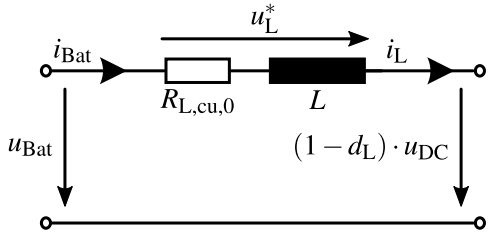

Figure 3.22: The voltage controlled inductor current which forms the plant of the inner current control loop

based on which the transfer function of the inductor voltage to inductor current is calculated and shown in equation 3.58.

$$\begin{aligned} G_{\mathrm{u_L i}}(s) &= \frac{I_{\mathrm{L}}(s)}{U_{\mathrm{L}}(s)} = \frac{1}{L \cdot s + R_{\mathrm{L,cu,0}}} = \frac{K_{\mathrm{L}}}{T_{\mathrm{L}} \cdot s + 1} \\ \text{in which} \quad K_{\mathrm{L}} &= \frac{1}{R_{\mathrm{L,cu,0}}}, \text{ and } T_{\mathrm{L}} = \frac{L}{R_{\mathrm{L,cu,0}}} \end{aligned} \tag{3.58}$$

In the above transfer function K_{L} and T_{L} are the amplification factor and the time constant of the voltage controlled inductor current. Another part of the controlled plant is the actuator (pulse

generator and the transistors) which is modeled as a PT-1 element with an average time constant equal to the dead time of the actuator. Same as the inverter dead time, specified in controller design of section 3.1.3, the dead time of the DC-DC converter as the actuator is calculated based on the measurement sampling rate and controller update rate, and their timing relation with the pulse generator carrier signal. For the DC-DC converter, same as the inverter, the voltage measurement, the current measurement, and the controller are synchronized with the carrier signal and are executed one time at the beginning of each switching period (T_{sw}). Accordingly, the transfer function of the actuator is calculated as in the following equation.

$$G_{act}(s) = \frac{1}{T_{dead} \cdot s + 1} \qquad \text{with} \qquad T_{dead} = 1.5 \cdot T_{sw} \tag{3.59}$$

Figure 3.23 shows the structure of the inductor current control loop which is composed of the PI controller, the transfer function of the actuator, and the transfer function of the inductor voltage to inductor current.

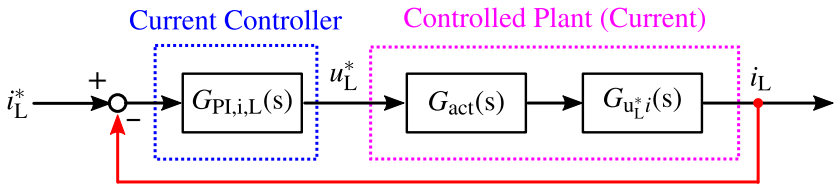

Figure 3.23: Inductor current control loop consists of the PI current controller and the current controlled plant

Based on equations 3.59, 3.58, and 3.56 the open-loop transfer function of the current control loop is calculated as

$$G_{open,i,L}(s) = K_{P,i,L} \cdot \frac{T_{I,i,L} \cdot s + 1}{T_{I,i,L} \cdot s} \cdot \frac{1}{T_{dead} \cdot s + 1} \cdot \frac{K_L}{T_L \cdot s + 1}. \tag{3.60}$$

The parameters of the PI current controller are chosen with the help of the magnitude optimum method described in [96]. Based on this method in order to achieve the optimal controller settling time the PI controller zero in equation 3.56 should cancel out the slower time constant of the plant. As a result with respect to equation 3.60 the amplification of the PI controller is as follows:

$$T_{I,i,L} = T_L. \tag{3.61}$$

On the other hand, to achieve optimal overshoot of the inductor current, the damping ratio of the resulting second-order closed-loop transfer function of the current controller should be set

to $\frac{1}{\sqrt{2}}$. By selecting the proportional term of the current controller in equation 3.56 as follows:

$$K_{\mathrm{P,i,L}} = \frac{T_{\mathrm{L}}}{2 \cdot K_{\mathrm{L}} \cdot T_{\mathrm{dead}}}, \tag{3.62}$$

the closed-loop transfer function will be:

$$G_{\mathrm{close,i,L}}(s) = \frac{1}{2T_{\mathrm{dead}}^2 \cdot s^2 + 2T_{\mathrm{dead}} \cdot s + 1}. \tag{3.63}$$

Another point which should be mentioned here is the implementation of the current controller in SIMULINK and its connection to the introduced modulator. As shown in figure 3.23 the output of the current controller is the inductor voltage. On the other hand the input of the modulator is the duty cycle of the corresponding phase of the converter. Based on the control rule defined in equation 3.53 a so-called nonlinear feedforward block is placed between the the current controller and the modulator, which calculates the required duty cycle for the next control cycle with the help of the measured battery voltage and DC-Link voltage.

Figure 3.24 shows the overview of the actual SIMULINK implementation of the current controller of the three phase DC-DC converter (figure 3.16) with an integrated feedforward block. As shown in figure 3.24 each phase of the converter has its own current controller. The saturation limits of the PI-controllers are calculated with the help of the actual input voltage and output voltage of the converter and the set point of the inductor currents are the same and are determined by the outer loop voltage controller introduced in the following subsection.

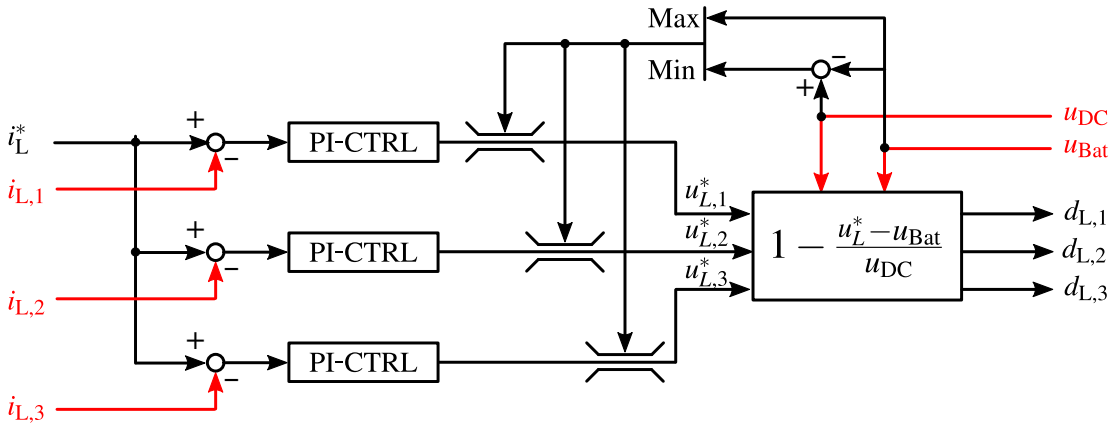

Figure 3.24: Three phase current controller of the interleaving DC-DC converter with an integrated feedforward block

3.2.3.2 Voltage Controller Design

The voltage controller is placed cascaded with the three current controllers and determines the set point of the inductor current of the three phases. In the voltage control loop the same PI-controller with anti-windup is used which is described in equation 3.56. Figure 3.25 shows the control plant of the outer voltage control loop. The capacitor voltage is calculated as shown in equation 3.64. In this equation (and the corresponding figure of the equivalent circuit) an ideal lossless converter (input and output power equality) with time invariant parameters is assumed.

$$\frac{du_{\mathrm{DC}}}{dt} = \frac{1}{C_{\mathrm{DC}}} \cdot i_{\mathrm{C}} = \frac{1}{C_{\mathrm{DC}}} \cdot \left(N_{\mathrm{ph}} \cdot \frac{u_{\mathrm{Bat}}}{u_{\mathrm{DC}}} \cdot i_{\mathrm{L}} - i_{\mathrm{DC}}\right). \tag{3.64}$$

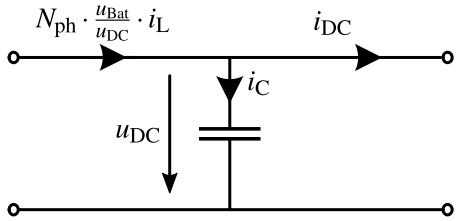

Figure 3.25: The current controlled capacitor voltage which forms the plant of the outer voltage control loop

As stated above, the resulting output of the voltage controller block is the inductor current, with which the DC-Link capacitor current is influenced, and finally the DC-Link voltage is regulated. As shown in equation 3.64, the relationship between the inductor current and capacitor voltage is affected by some disturbance sources such as the actual value of DC-Link voltage and current, and the battery voltage. As shown in the following, a feed-forward compensator block is used to minimize the effect of these disturbances. Figure 3.26 shows the entire voltage controller block, which consists of a PI-controller with anti-windup as well as the mentioned feed-forward compensator block.

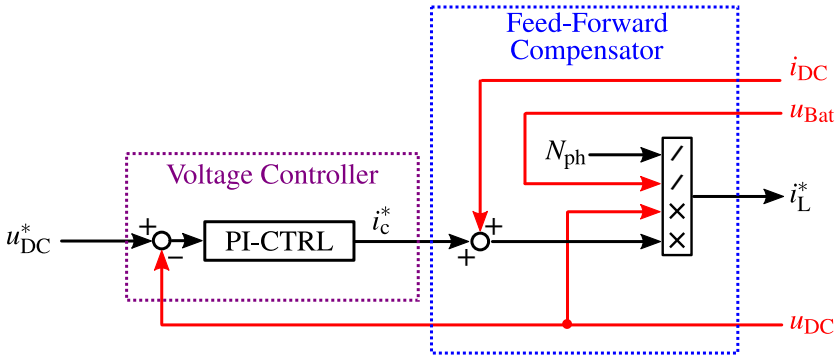

Figure 3.26: Outer loop voltage controller of a multiphase DC-DC converter consists of PI-controller and a feed-forward compensation

The idea of using the compensator is to (ideally) predict the effect of the aforementioned

disturbances on the DC-Link voltage dynamic behavior (using equation 3.64) and counteract them. This is done by scaling and shifting the level of the control current set point (i_c^*) in the opposite direction of the disturbance changes before passing the output to the current controller as the inductor current set point. It means that the output of the voltage controller is added to the DC-Link current and then multiplied with a correction factor as shown in equation 3.65.

$$i_L^* = (i_c^* + i_{DC}) \times \frac{1}{N_{ph}} \cdot \frac{u_{DC}}{u_{Bat}} \tag{3.65}$$

Under the assumption of an ideal dynamic compensation of the $N_{ph} \cdot \frac{u_{Bat}}{u_{DC}}$ factor and i_{DC} offset at the output of the voltage controller the Laplace transformation of the control voltage (i_c^*) to DC-Link voltage is derived from equations 3.64 and 3.65 and is shown in the following.

$$G_{ucu}(s) = G_{close,i,L}(s) \cdot \frac{1}{C_{DC} \cdot s} \tag{3.66}$$

In order to select the proper parameters for the PI-controller the transfer function of the closed-loop current control system is estimated with a PT-1 element as follows:

$$G_{close,i,L}(s) = \frac{1}{T_{est,i,L} \cdot s + 1} \qquad \text{with} \quad T_{est,i,L} = 2 \cdot T_{dead}. \tag{3.67}$$

The resulting open-loop transfer function of the entire system can be calculated as shown in equation 3.68.

$$G_{open,u,L} = K_{P,u,L} \cdot \frac{T_{I,u,L} \cdot s + 1}{T_{I,u,L} \cdot s} \cdot \frac{1}{T_{est,i,L} \cdot s + 1} \cdot \frac{1}{C_{DC} \cdot s} \tag{3.68}$$

For the parameter dimensioning of the voltage controller, despite the current controller dimensioning, the magnitude-optimum method can not be used. The same reason as stated in section 3.1.3 for the design of the speed controller is applied here as well, which is the instability of the closed-loop system because of the integrator term in the transfer function of the controlled plant. Identical to the speed controller design, the symmetrical-optimum method is used here for the outer loop voltage controller parameter selection. As mentioned in section 3.1.3, according to this method, to achieve the maximum phase margin and optimum damping of the system the optimum value of the crossover frequency (ω_{cross}) of the open-loop transfer function should be found. As it is known, the magnitude of the transfer function at its crossover frequency is equal to 0 dB. Therefore, the transfer function magnitude in terms of frequency should be derived from equation 3.68 to calculate the crossover frequency of the system. With the help of the frequency dependent magnitude of the transfer function the first dimensioning criteria is

calculated by setting $\left|G_{\text{close,i,L}}(\omega)\right|$ at $\omega = \omega_{\text{cross}}$ to 1 as follows:

$$K_{\text{P,u,L}} \cdot \frac{\sqrt{1+T_{\text{I,u,L}}^2\omega_{\text{cross}}^2}}{T_{\text{I,u,L}}\omega_{\text{cross}}} \cdot \frac{1}{\sqrt{1+T_{\text{est,i,L}}^2\omega_{\text{cross}}^2}} \cdot \frac{1}{C_{\text{DC}}\omega_{\text{cross}}} = 1. \tag{3.69}$$

According to the symmetrical-optimum principle the crossover frequency (ω_{cross}) shown in equation 3.69 should be selected in a way that it is exactly in the geometric mean point of the system corner frequencies, namely $\omega_{\text{I,u,L}} = \frac{1}{T_{\text{I,u,L}}}$ and $\omega_{\text{est,i,L}} = \frac{1}{T_{\text{est,i,L}}}$. Consequently, the second dimensioning criteria obtained from the above condition is as follows:

$$\omega_{\text{cross}} = \sqrt{\omega_{\text{I,u,L}} \cdot \omega_{\text{est,i,L}}} = \sqrt{\frac{1}{T_{\text{I,u,L}}} \cdot \frac{1}{T_{\text{est,i,L}}}}. \tag{3.70}$$

By replacing ω_{cross}^2 term in equation 3.69 with the corresponding value given in equation 3.70, the PI controller parameters in terms of crossover frequency are determined and shown in equations 3.71 and 3.72.

$$K_{\text{P,u,L}} = C_{\text{DC}} \cdot \omega_{\text{cross}} \tag{3.71}$$

$$T_{\text{I,u,L}} = \frac{1}{T_{\text{est,i,L}} \cdot \omega_{\text{cross}}^2} \tag{3.72}$$

According to the above two dimensioning equations there are three unknown variables (ω_{cross}, $K_{\text{P,u,L}}$, and $T_{\text{I,u,L}}$) which should be chosen. As a result there are indefinite number of parameter sets (intersection line of the two surfaces) which can satisfy equations 3.71 and 3.72. As it has been shown in [13] and [96], by setting the controller time constant related to the corner frequency ($T_{\text{I,u,L}}$) 4 times of the inner current control loop time constant ($T_{\text{est,i,L}}$) the best trade-off between the overshoot and settling time of the closed-loop system response is made. Consequently the final parameters are calculated as follows:

$$K_{\text{P,u,L}} = \frac{C_{\text{DC}}}{2 \cdot T_{\text{est,i,L}}}, \tag{3.73}$$

$$T_{\text{I,u,L}} = 4 \cdot T_{\text{est,i,L}}. \tag{3.74}$$

After introducing the inner current control loop and the outer voltage control loop and dimensioning their control parameters, the overview of the implemented system and the simulation results are presented in this part. Figure 3.27 shows the entire system, in which the controller and the modulator are implemented using SIMULINK and same as the inverter section, the temperature dependent model of the converter is implemented using PLECS. According to the system realization the control section is executed with a sampling rate equal to the converter

switching frequency (10 kHz in this case) and the PLECS model is running with a much higher sampling rate (50 times of the switching frequency) to replicate the actual DC-DC converter behavior.

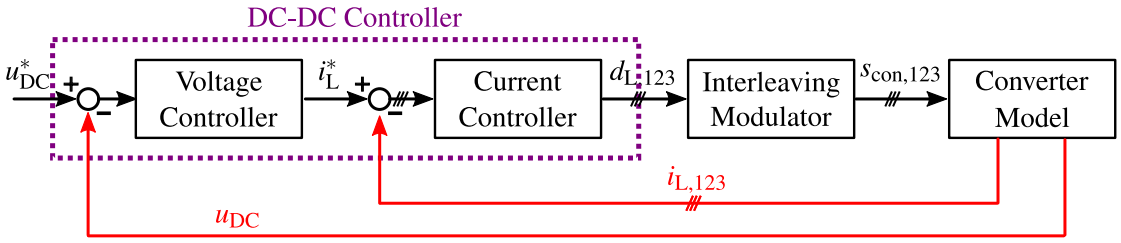

Figure 3.27: Implemented control system and the model of multiphase DC-DC converter

In order to evaluate the controller performance the introduced test case presented in subsection 3.1.3 for the inverter part is also used here for the converter simulation. This means that the output load of the multiphase converter is set based on the input load of the inverter-fed machine resulting from the machine driving cycle shown in figure 3.11.

Figure 3.28 shows the simulation results of the converter for the above mentioned driving cycle. In this test case the battery voltage is equal to 110 V and the desired output voltage of the converter is set to 300 V. The DC-Link voltage performance during different load variations is presented in figure 3.28 (a). As it has been mentioned in subsection 3.1.3 the inverter-fed machine is operating both in regenerative mode (during breaking periods) and motor operating mode (during acceleration periods), which results in positive and negative current at the DC-DC converter output (figure 3.28 (b)). Based on the simulation results, the DC-Link remains stable during both operating modes, and the maximum dynamic regulation of the converter equals to 353 mV/A during this driving cycle. Finally the inductor currents of the three phases are presented in figure 3.28 (c), which shows a prefect distribution of the load current between the three phases.

As it has been discussed in the first part of this section, an interleaving modulation strategy is utilized to control the phases of the DC-DC converter. In order to evaluate the performance of this modulator and the effect of the interleaving on the input current ripple, the inductor current waveforms of three phases for 10 switching periods during the driving cycle shown in figure 3.28 are evaluated separately. Figure 3.29 (a) shows the current distribution between the three phases of the converter which provides a perfectly balanced load allocation between the inductors. On the other hand due to the interleaving operation and 120° phase offset between the phases the battery current ripple is reduced drastically as shown in figure 3.29 (b). Another advantage of the interleaving operation which is the increased frequency of the battery current ripple in comparison with the inductor current ripple (tripled in this case) is seen in figure 3.29 (b).

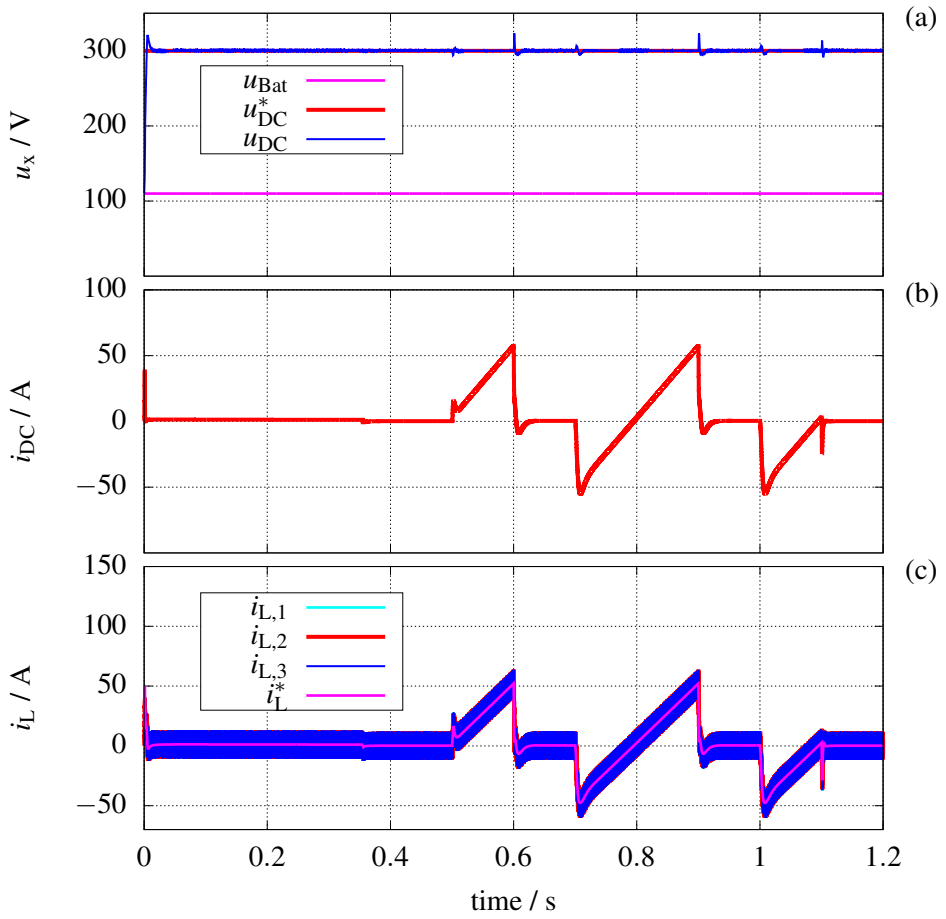

Figure 3.28: Simulation Results of the multiphase DC-DC converter with 110 V input voltage and an output voltage set to 300 V (a) output voltage set point and actual value (b) output current of the converter resulted from the inverter-fed machine driving cycle shown in subsection 3.1.3 (c) set point and actual value of the inductor currents of each one of the converter phases

3.2.4 State-Space Average Model

Same as the inverter model, the implemented model of the DC-DC converter in PLECS is not suitable for the simulation of long driving cycles because of time consuming calculation of the switching converter model. For this reason based on the similar principles presented in section 3.1.4 a state-space average is provided for the multiphase DC-DC converter. This model includes the simplified equations of the power stage, the temperature dependent power semiconductor loss calculation unit as well as the comprehensive loss model of the inductor introduced in section 2.2. Figure 3.30 shows the implementation of the mentioned model in SIMULINK.

In order to reproduce the dynamic behavior of the converter the same developed controller is used in the average model. Under the assumption of identical properties of the three inductors (inductance and resistance) the duty cycles of the three phases will be the same and is shown

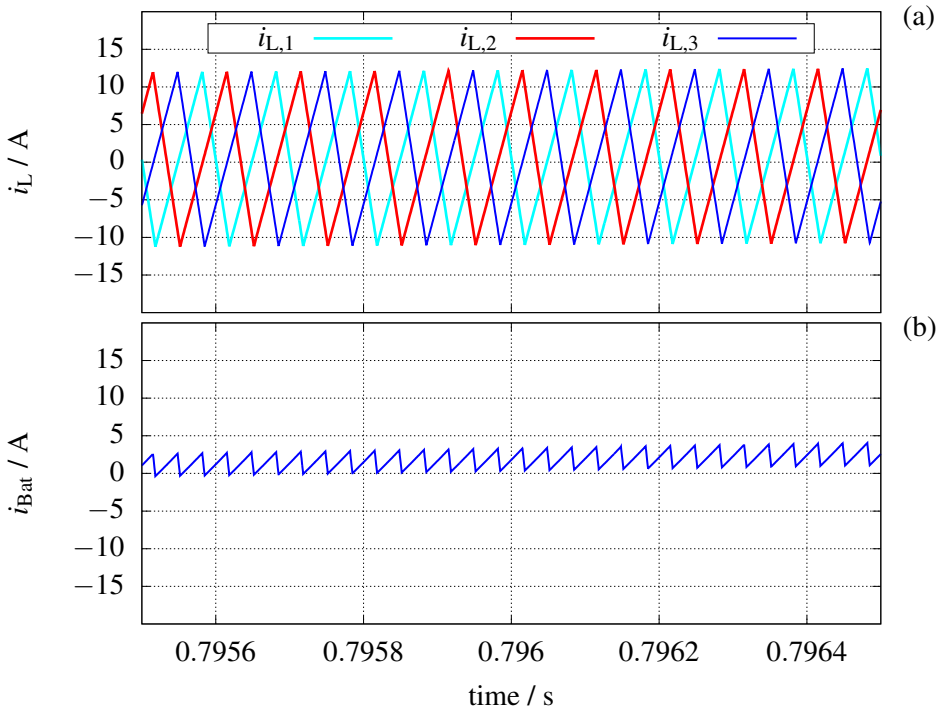

Figure 3.29: Interleaving operation of the converter (a) current distribution between three phases of the converter (b) input current waveform of the converter

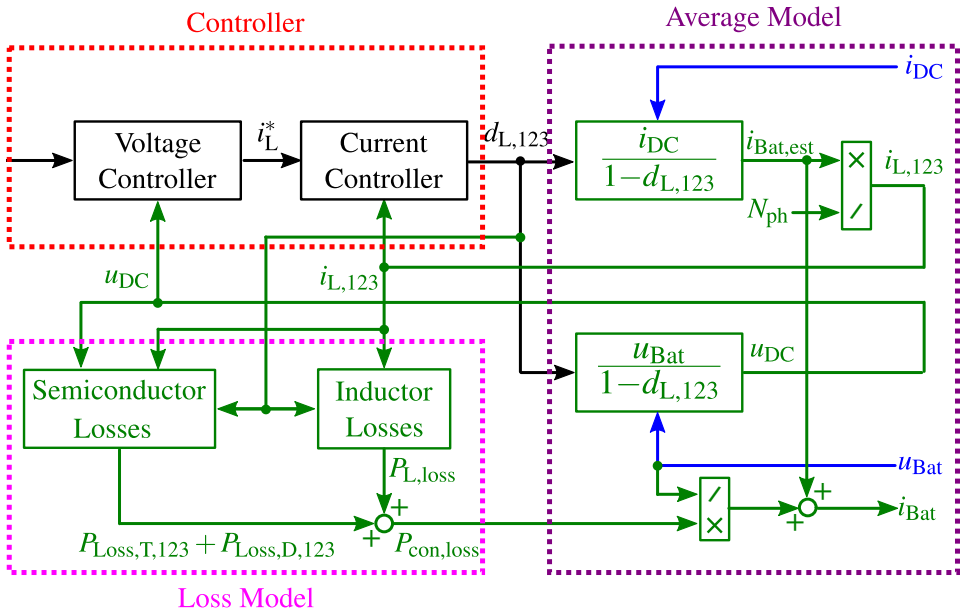

Figure 3.30: Implemented state-space average model of the multiphase DC-DC converter consists of the developed controller, the power-stage model and the temperature dependent power loss model of the semiconductors and inductor

with $d_{L,123}$ as in equation 3.75.

$$d_{L,123} = 1 - \frac{u_{Bat} - u_L}{u_{DC}} \tag{3.75}$$

In order to model the power stage the DC-Link voltage is calculated with the help of the voltage equation of the converter as follows:

$$u_{\mathrm{DC}} = \frac{u_{\mathrm{Bat}}}{1 - d_{\mathrm{L,123}}}, \tag{3.76}$$

and the result is used as feedback signal in the the voltage controller block and the semiconductor losses calculation block. Finally the input current of the converter is estimated using equation 3.77 for a lossless DC-DC converter.

$$i_{\mathrm{Bat,est}} = \frac{i_{\mathrm{DC}}}{1 - d_{\mathrm{L,123}}} \tag{3.77}$$

In order to evaluate the performance of the state-space average model of the multiphase converter a comparison is made between the SSA-model and the switching model . As the load of the converter the same driving cycle of the inverter-fed machine shown figure 3.11 is used. The DC-Link voltage and the inductor currents of the SSA-model and switching model are presented in figure 3.31. Based on these results there is a pretty good match between the two models. The only significant difference is the DC-Link voltage behavior during DC-Link current jumps at the load side. The reason for this discrepancy is discussed in the following.

In the switching model of the converter a DC-Link current increase will result in the capacitor voltage reduction and the voltage controller reacts to this deviation of the output voltage from its set point. The controller increases the value of the inductor current set point (i_{L}^{*}) at its output, which consequently leads to an increment of the duty cycle (d_{L}). Because of the limited bandwidth of the converter, and the fact that the the slew rate of the inductor average current is smaller that the duty cycle change, at first, the output voltage drops further (higher duty cycle increase than inverter average current increase results in a lower DC-Link capacitor current). The voltage will eventually come back to the set point as the inductor current builds up and reaches the set point imposed by the control loop. On the other hand, in the SSA-model shown in figure 3.30, the converter is modeled with equations 3.76 and 3.77. This means that the inductor current ripple is neglected and the average value of the inductor current is directly coupled to the duty cycle. Consequently, in the average model a positive load current jump results in a lower estimated value of the battery current (equation 3.77) and a higher actual value of the inductor current. This will lead to a negative value at the current controller input, a smaller duty cycle, and finally an increase in the output voltage (equation 3.76) directly after the current jump. This reaction chain is the main reason for the output voltage overshoots during positive load jumps shown in figure 3.31.

As stated in subsection 3.1.4, the main requirement of the SSA model is to replicate the power losses of the converter with the help of a quasi-transient operating point calculation as good as possible and simultaneously decrease the processing complexity of the model so that it is utilizable for longer driving cycle simulations. At the end of this section, it will be shown that the dynamic behavior discrepancy of the average model from the switching model (figure 3.31)

has a negligible influence on the energy loss calculation.

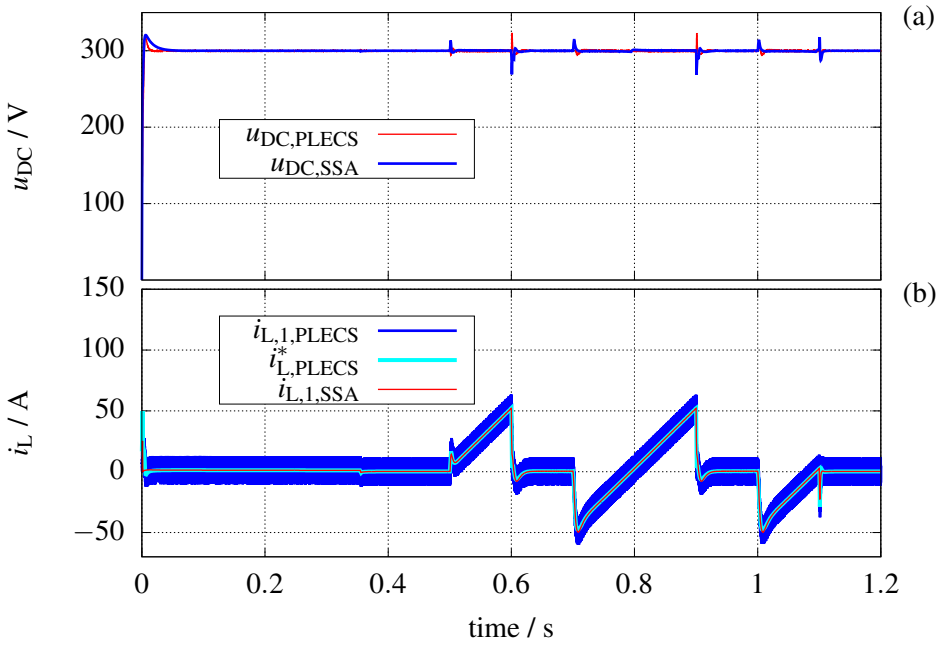

Figure 3.31: Comparison between the state-space average model and the PLECS model of the 3-phase DC-DC converter in terms of operating point (a) DC-Link voltage (b) inductor current set value and average value

Last but not least, a loss calculation model of the converter should be provided that includes the inductor losses model and the power transistor losses model. As shown in figure 3.30 the actual input current of the converter results from the sum of its estimated value (calculated using equation 3.77) and the additional current resulted from the converter losses. In order to calculate the inductor power losses the method extensively presented in section 2.2 is used, and for the calculation of the losses of the power transistor the same procedure is used which is presented in the power transistor introduction (section 2.3).

As already mentioned in section 2.3 the losses of the power semiconductors (in this case the IGBTs and diodes in the HybridPACK 2 module) are divided into two main parts: the conduction losses and the switching losses. The conduction losses of the transistor and its complimentary diode in each leg of the converter are calculated by multiplying the forward voltage drop of the corresponding component (extracted from the semiconductor temperature and current dependent look-up-table of the voltage drop or $R_{DS,on}$ explained in section 2.3) by the average value of the current flow through that component during each switching period. The current average value can be calculated with the help of the instantaneous duty cycle of that leg during the switching period. Equations 3.78 and 3.79 present the conduction losses of the power semiconductors for each converter leg.

$$P_{\text{loss,T}_i,\text{cond}}(t) = d_L \cdot \left|i_{L,i}(t)\right| \cdot u_T(t) \qquad \text{with} \qquad u_T(t) = f(\left|i_{L,i}(t)\right|, \theta_{T,i}(t)) \tag{3.78}$$

$$P_{\text{loss,D}_i,\text{cond}}(t) = (1-d_L) \cdot \left|i_{L,i}(t)\right| \cdot u_F(t) \qquad \text{with} \qquad u_F(t) = f(\left|i_{L,i}(t)\right|, \theta_{D,i}(t)) \tag{3.79}$$

To calculate the converter switching losses the same method as for the inverter switching loss calculation is used which is described in section 3.1.4. Based on this method, the switching energy losses can directly be extracted from the corresponding LUTs provided in section 2.3 for IGBT module. It should be mentioned that with respect to the fact that in the bidirectional converter the inductor current average value can either be positive or negative, the calculated semiconductor losses are attached to the corresponding components which participate in the current conduction and generate the losses (low-side transistor and high side diode in the case of positive $I_{\mathrm{L.avg}}$ and vise versa) [8)].

The above calculation provides the instantaneous power losses of each converter leg. Finally the power losses will be fed to the Foster Thermal Network of the converter (presented in section 2.3.3) in the form of a closed-loop system to calculate the power semiconductor and or indcutor temperature increase. The detailed calculation procedure and required equations are the same as the inverter loss calculation method presented in the SSA-model part of section 3.1.4.

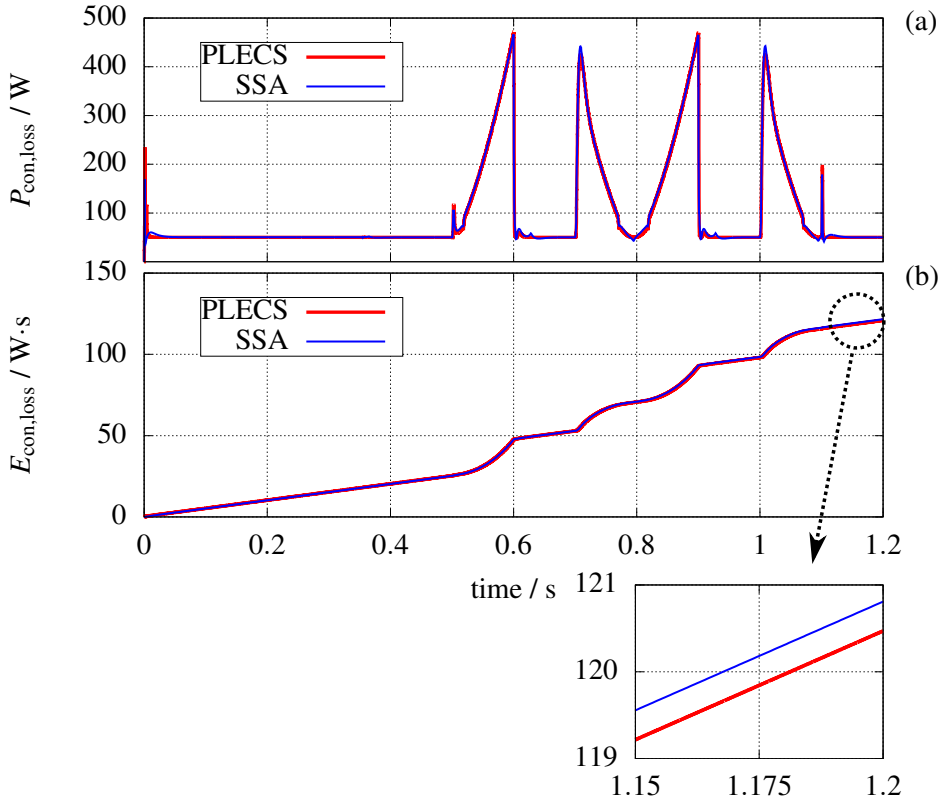

Figure 3.32: Comparison between the state-space average model and the PLECS model of the 3-phase DC-DC converter in terms of losses (a) power losses (b) energy losses

Figure 3.32 provides a comparison between the two models in terms of losses. The power losses are illustrated in figure 3.32 (a) and shows a good match between the two models. The energy

[8)] During the loss calculation process of the converter, at every step it is evaluated if the inductor average current is smaller that the half of the inductor current ripple at that given operating point. If that is the case, then based on the positive to negative current peaks ratio the calculated losses will be distributed between the low-side and high-side transistors (diode) respectively.

losses difference during the driving cycle remains always below 0.21% (see figure 3.32 (b)) which proves the validity of the state-space average model-based loss calculation method.

In the next chapter the new adjustable variables such as DC-Link voltage, switching frequency and number of active phases of the converter are investigated further to realize some optimizing strategies with the new drivetrain. At the end of this chapter, it should be mentioned that the future simulation results used to develop optimizing strategies are all based on the switching model of the converter, and the provided SSA-models are only used for the evaluation of the energy losses for longer driving cycles such as NEDC [9)].

[9)] New European Driving Cycle.

4 Optimizing Strategies

In the previous chapters the model of different units and components of the drivetrain are provided. The corresponding control system of different drivetrain components has been developed and introduced in the previous chapter as well. Finally with the help of some simulation results the dynamic behavior of the system as well as the validity of the state-space average model (SSA-model) have been investigated.

With the help of the provided models and control systems and by means of the new possibilities that the alternative drivetrain of figure 3.1 is facilitating, different loss optimizing operating strategies will be developed and presented in this chapter. The factors which can be manipulated using the additional DC-DC converter in the drivetrain are as follows:

1. DC-Link voltage level
2. The number of active phases of the multiphase converter
3. Active or passive operation of the DC-DC converter
4. Switching frequency of the converter

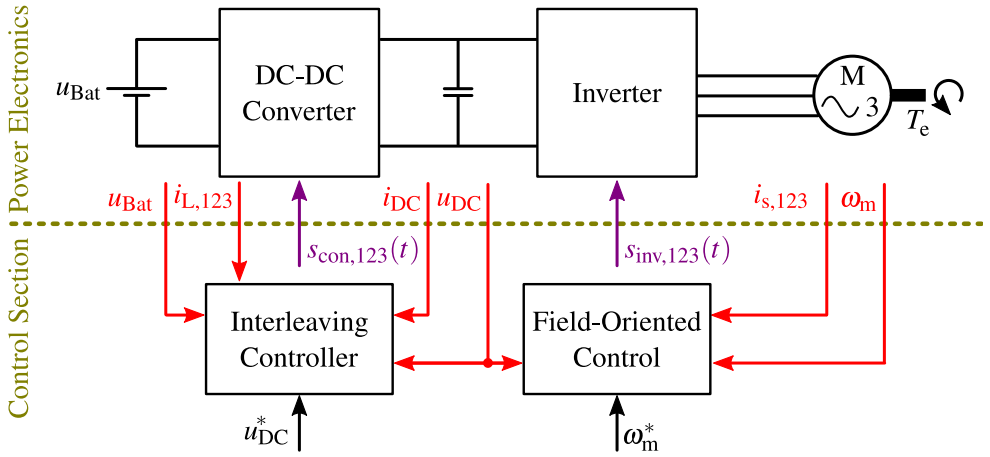

Figure 4.1: Drivetrain control system and the model of the power electronic components (switching model / SSA model) of an electric vehicle with a DC-DC converter as an extension

An overview diagram of the provided drivetrain is presented in figure 4.1, which shows the developed controller along with the model of the included components (power electronic parts and the electric machine). The controller section consists of the field-oriented control of the inverter-fed machine and the interleaving control of the DC-DC converter. Various

interconnections between the controller and the power electronic parts are all shown in figure 4.1 as well. In order to extend the control system for loss optimization purpose, the influence of various parameters, set by the controller, on the power losses of the whole system should be evaluated.

As shown in figure 4.1 the input of the drivetrain controller is the set point of the induction machine rotation speed (or the electric torque), while other parameters of the system such as DC-Link voltage, switching frequencies, and the pulse modulators are all consistent during the vehicle operation. These parameters are generally selected in the design process of the drivetrain, and the design criteria of each one of them are different than the other. As an example the DC-Link voltage is selected in a way that the voltage at the input of the inverter (DC-Link) is large enough to ensure the operation of the induction machine at its nominal rotation speed and torque. In the following sections the impact of these parameters (e.g. DC-Link voltage) on the power losses of the drivetrain components are investigated, with which different operating strategies will be developed and integrated into the main control system.

In the second part of this chapter, in order to verify the accuracy of the loss models on the one hand and the functionality of the control system with the activated operating strategies on the other hand, the built experimental setup consisting of a three-phase interleaving DC-DC converter is presented and measurement results are provided. A list of the components which have been utilized in the simulation models is given in table 4.1. These simulation results are used in this chapter for the development of the loss optimizing operating strategies for the DC-DC converter. The same components as in the simulation are utilized later on to build the experimental setup, consisting of the 3-phase interleaving DC-DC converter.

Table 4.1: The components used for the realization of various parts of the drivetrain, which are employed in the simulation and subsequently in the DC-DC converter test setup for the model verification

Use case	Component	Modeled losses	Reference
DC-Link capacitor	Film capacitor *B25655J4507K*	Ohmic losses and dielectric losses	section 2.1
Inductor	MPP *58338A2* and given winding	Ohmic losses and core losses	section 2.2
DC-DC converter half-bridges	IGBT Module *FS800R07A2E3*	Conduction losses and switching losses	section 2.3.2
Inverter half-bridges	IGBT Module *FS400R07A1E3*	Conduction losses and switching losses	section 2.3.2
Electric machine	Induction machine	Ohmic losses [a]	section 2.4

[a] The simplified model of the machine is only used to model a realistic load for the DC-AC converter part of the drivetrain; the machine itself is not the focus of the efficiency analysis (refer to section 5.2).

4.1 Variable DC-Link voltage

As mentioned in the introduction of this chapter, in a conventional drivetrain the value of the DC-Link voltage is imposed by the value of the high-voltage battery. According to [100], in the design process of the battery stack and the electric machine, the requirement for the optimum voltage level yields different values (the optimal voltage of the battery is lower than that of the machine), and therefore the DC-Link voltage level carries optimization potential. With the help of the added DC-DC converter to the drivetrain this potential is now utilizable, and is evaluated in the following section.

In the first step, the correlation between the DC-Link voltage and the power losses of the inverter and the DC-DC converter should be calculated to evaluate the impact of the DC-Link voltage level on the drivetrain efficiency. In section 3.1 and section 3.2 the detailed calculation method of the inverter power losses and the 3-phase interleaving DC-DC converter power losses are presented respectively. These models are utilized in the following to investigate the effect of the DC-Link voltage level on the losses. For these simulations, the components listed in table 4.1 are used in the models.

In equations 3.38 to 3.40, which apply to both the DC-DC converter and the inverter, it was shown that the amount of switching losses (consisting of the switching-on and switching-off losses of the transistor and the reverse recovery losses of the anti-parallel diode) correlates with the amount of DC link voltage. As discussed in section 2.3.2 and shown in particular in figure 2.26, the voltage-dependent switching losses can be observed in the IGBT module example, i.e. the higher the DC-Link voltage, the higher the switching power losses. Figure 4.2 shows the efficiency of a 3-phase interleaving DC-DC converter (simulation model using the components of table 4.1) with respect to the converter output power (up to 30 kW) for a constant battery voltage of 110 V and three different DC-Link voltages (140 V, 220 V, and 300 V).

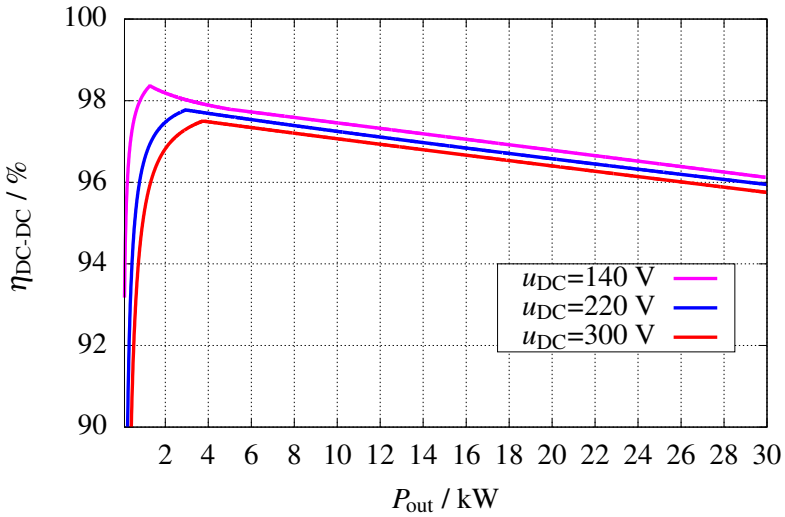

Figure 4.2: Efficiency of the three-phase converter with the components presented in table 4.1 for different DC-link voltages and output powers with u_{Bat} = 110 V and f_{sw} = 10 kHz

As expected the efficiency of the converter increases with the decreasing DC-Link voltage. It is important to mention that the efficiency improvements at partial loads is much higher (maximum efficiency of 140 V against 300 V DC-Link voltage takes place at 1.3 kW and is equal to 2.39% efficiency improvement) in comparison with high loads (for output loads higher than 4 kW the amount of efficiency improvements is only 0.36%). Another important effect that can be observed is the pattern of efficiency change that actually changes at a given output load. For example, at 220 V DC-Link voltage and 3 kW output power, the derivative of the efficiency curve with respect to output power changes its sign and starts to decrease. The resulting inductor current at this output power is 9.16 A per inductor phase. This current value is exactly half of the total inductor current ripple for the given converter voltage gain (relates to duty cycle) and switching frequency. In the other words, at 3 kW output power, the minimum value of the inductor current (triangular waveform of the figure 3.17) crosses the 0 A line, changes its sign, and becomes positive. This means that high-side and low-side devices that contribute to the current flow, and generating power losses are changing. It is known that at the minimum inductor current, the high-side part of the half-bridge should switch off and the low-side device should switch on. In the case of a negative minimum inductor current, the high-side transistor switches off under zero current condition since the low-side diode has already taken over the current flow at toggling point of the current sign. But for a positive minimum inductor current both high-side diode and low-side transistor will generate losses ($P_{\mathrm{D,RRM}}$ and $P_{\mathrm{IGBT,sw,off}}$ respectively) which leads to the further reduction of the converter efficiency. The same effect applies to the efficiency of converter for the other two voltages of figure 4.2 (for each DC-Link voltage, the turning point happens at a different output power because the converter duty cycle and thus the inductor current ripple is different).

In the next step, the voltage dependency of the losses of the 3-phase inverter is evaluated in detail. As with the DC-DC converter, it is expected that the inverter switching losses are dependent on the DC-Link voltage as well (according to equations 3.38 to 3.40). To investigate this dependency, the electric machine presented in section 2.4[1)] with 400 V nominal line-line voltage is used to simulate a realistic load at the output of the inverter, which is modeled with the components shown in table 4.1 . For this analysis the inverter-fed machine is supplies at first with 320 V DC-Link voltage and the inverter losses ($P_{\mathrm{inv,loss,320V}}$) and efficiency ($\eta_{\mathrm{inv,320V}}$) are calculated point by point over the entire operating area of the machine. It should be noted that with the maximum modulation index of the inverter ($2/\sqrt{3}$), the 320 V DC-Link voltage resulting in a maximum motor line-line voltage of 226.27 V. This means that the field-weakening operation of the machine starts already at 56.5 % of the nominal speed of the machine (4560 rpm). In the next step, the same loss and efficiency calculation is repeated but this time with 400 V supply voltage, which results in $P_{\mathrm{inv,loss,400V}}$ and $\eta_{\mathrm{inv,400V}}$ over the torque-speed map. To achieve a comparable result, the same field-weakening range is used as for the system with 320 V supply voltage (the modulation index of the inverter is limited to 56.5 % of its maximum value).

[1)] In this part, the focus is on the voltage dependency of the energy losses of the voltage converter, therefore the provided model of the machine, which contains only the ohmic losses of rotor and stator, is sufficient. The effect of the inverter operating point (e.g. modulation index) on the losses of the electrical machine is discussed separately at the end of section 5.2.

Figure 4.3 shows the difference between the power losses and efficiencies of the inverter after increasing the DC-Link voltage voltage from 320 V to 400 V (left figure shows $P_{\text{inv,loss,320V}}$-$P_{\text{inv,loss,400V}}$ and right figure represent $\eta_{\text{inv,320V}}$-$\eta_{\text{inv,400V}}$). This means that negative values for the power loss difference and positive values for the efficiency difference represent an advantage of the lower DC-Link voltage over the higher DC-Link voltage. According to the results decreasing the DC-Link voltage leads to a power loss reduction up to 90 W. The influence of voltage variation on efficiency leads to an average improvement between 0.5% to 1.5%, with a maximum value of 4% at partial load (low speed and low torque).

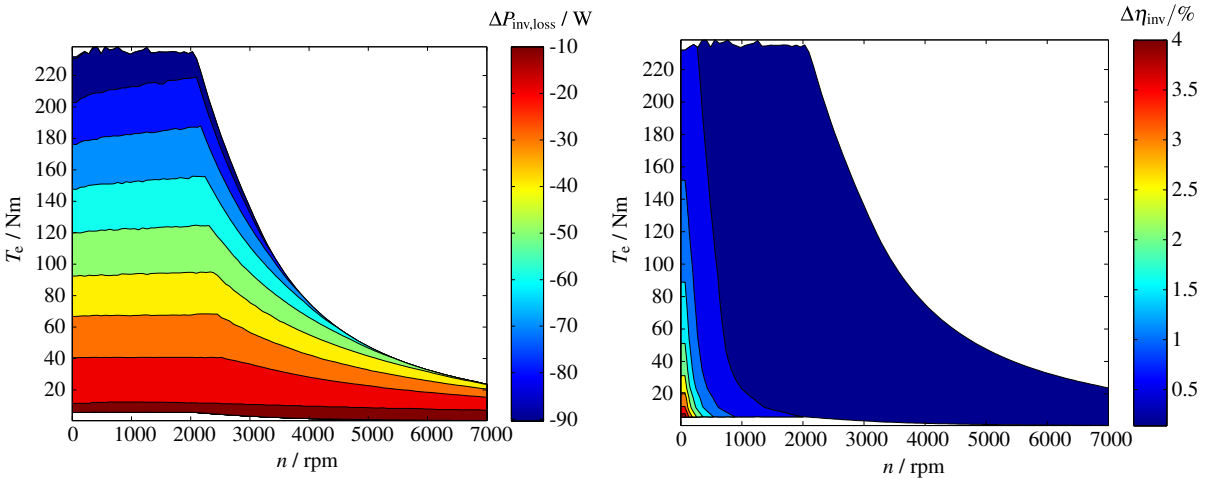

Figure 4.3: Inverter power losses difference (left) and inverter efficiency difference (right) in the case of increasing the supply voltage from 320 V to 400 V (f_{sw} is set to 10 kHz and for the inverter and electric machine the components presented in table 4.1 are used)

4.1.1 Optimum DC-Link Voltage Set Point

According to the simulation results which are presented and discussed in the previous subsection, at each operating point of the inverter-fed machine an optimum DC-Link voltage can be calculated. As shown in figure 4.2 and figure 4.3 a lower DC-Link voltage yields to higher efficiencies of the both DC-DC converter and inverter (this result is also verified by the measurements presented in section 4.5). Therefore, at any given operating point of the motor the goal is to set the DC-Link voltage to the lowest value required by the machine to be properly driven. In order to achieve this minimum voltage, the inverter modulation index (equation 3.6) should be set to its upper limit which in the case of the space vector modulation, discussed in section 3.1.2, is as follows:

$$M_{\text{max,SVM}} = \frac{2}{\sqrt{3}}. \tag{4.1}$$

In the stationary condition, and with the help of equations 3.6 and 4.1 the desired DC-Link

voltage at each operating point of the induction machine is calculated as follows:

$$u_{\mathrm{DC}} = \frac{2 \cdot \hat{U}_{\mathrm{s}}}{M_{\mathrm{max,SVM}}} = \sqrt{3} \cdot \hat{U}_{\mathrm{s}}. \tag{4.2}$$

In equation 4.2 the amplitude of the required motor phase voltage in the stationary condition is represented by $\hat{U}_{\mathrm{s}}$. For the implementation of the variable DC-Link voltage in the control system, the current controller outputs of the field oriented control, discussed in section 3.1.3, are used to determine the required transient amplitude of the motor phase voltage. As illustrated in figure 4.4, in order to calculate the target DC-Link voltage for a given dynamic speed set point and the load of the motor, the transient amplitude of the stator voltage vector is extracted from the controller and multiplied by the factor given in equation 4.2. The result is then pushed through a low pass filter with a time constant of 1 ms to prevent rapid changes of the DC-Link voltage set point.

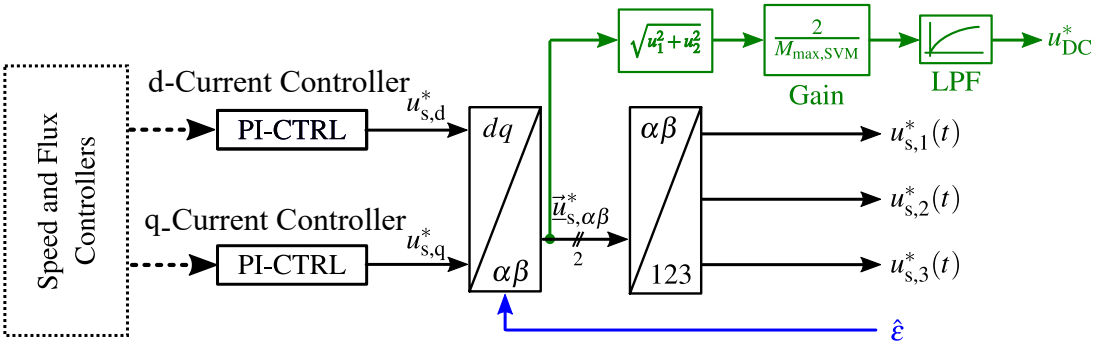

Figure 4.4: Modified FOC controller to calculate the minimum required DC-Link voltage at a given operating point

Finally, figure 4.5 shows the integration of the modified FOC controller on the system level to realize a variable DC-Link voltage control strategy. In this figure it is shown that the DC-Link voltage set point is calculated in the motor controller and fed back to the DC-DC converter controller to regulate its output.

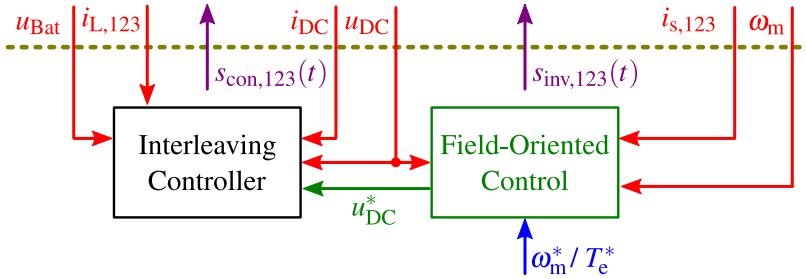

Figure 4.5: Integration of the variable DC-Link voltage operating strategy into the top-level controller of the drivetrain

4.2 Variable Number of Active Phases

As shown in figure 3.2 the selected converter for the alternative drivetrain is a multiphase converter. Additional to the interleaving operation capability of a multiphase converter, another feature which is utilizable by using such topology is the ability to activate only the necessary number of the converter phases [98]. This can lead to lower power losses of the converter under different load conditions. In order to evaluate the effect of the number of active phases on the total power losses, the switching model of the converter developed and presented in section 3.2 is used. The power losses and efficiency of a 3-phase converter (using the components of table 4.1) are calculated for three different number of active phases (N_{ph}), and for different output currents.

With the above mentioned goal a simulation is undertaken for a DC-DC converter with a constant input voltage of 110 V and a constant DC-Link voltage of 300 V. Figure 4.6 shows the efficiency of the converter for different output power and number of activated phases. Based on the simulation results, it is clear that to achieve the maximum efficiency in the partial load region (output current below 6.8 A, which corresponds to an output power below 2040 W), only one of the converter phases should be activated. With increasing output load the second and finally the third phases of the converter should be activated at 6.8 A and 11.38 A respectively. The calculated efficiency of the converter shown in figure 4.6 evaluates this dependency only at one DC-Link voltage. In order to cover the full output voltage range of the converter the above simulation should be repeated for different DC-Link voltages.

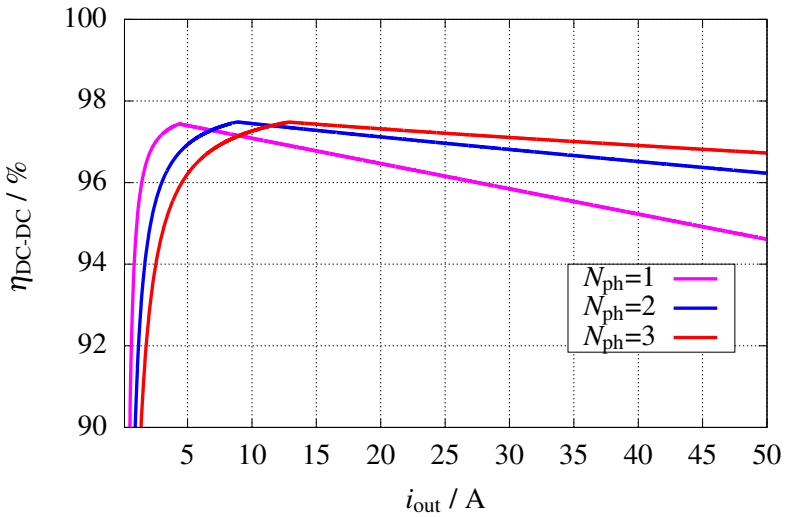

Figure 4.6: Efficiency of the DC-DC converter (the simulation model with the components presented in table 4.1) for different number of active phases and output currents with u_{Bat} = 110 V and u_{DC} = 300 V

Same simulation as in figure 4.6 are repeated with the same battery voltage and different DC-Link voltages. The results are shown in figure 4.7, with which for different output voltages the current limit of the first toggling point (from one to two active phases) and second toggling point (from two to three active phases) are determined. According to figure 4.7 the higher the

DC-Link voltage is, the lower the output current value of the toggling point gets.

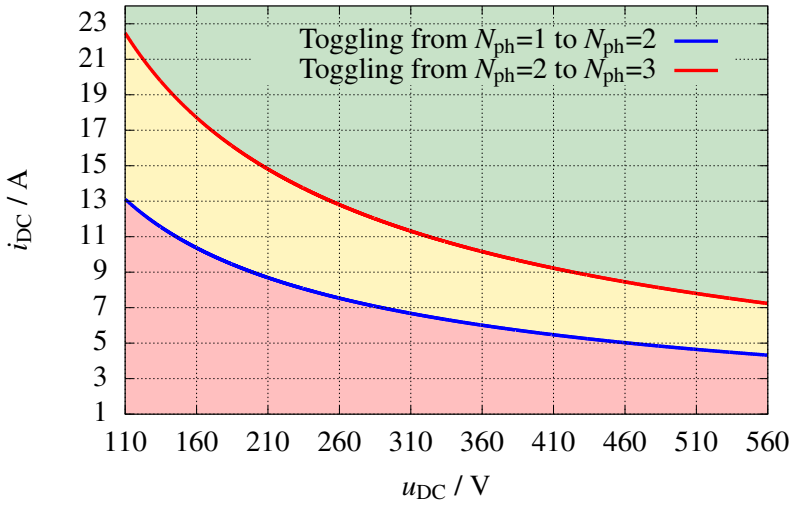

Figure 4.7: Toggling point of the DC-DC converter optimum number of active phases for different DC-Link voltages and load currents (battery voltage u_{Bat} is constant and equal to 110 V)

The reason for the voltage dependency of the toggling point shown in figure 4.7 relies on the converter losses distribution between the switching losses and conduction losses. It is known that incrementing the number of active phases will result in the current distribution between more power transistors, and this means that for a constant converter current and voltage, higher number of active phases will lead to higher switching losses and lower conduction losses. On the other hand by increasing the DC-Link voltage the contribution of a current increase on the converter switching losses becomes greater (see section 2.3). With respect to these two facts it can be concluded that the current value, at which the activation of an additional converter phase results in a higher conduction power losses reduction than switching losses increase, is getting lower by increasing the DC-Link voltage. This conclusion matches with the provided simulation results in figure 4.6 and 4.7.

In order to implement the new loss optimizing operating strategy, a two dimensional look-up-table is created from the simulation results of figure 4.7, which determines the optimal number of the active phases based on the output current and the DC-Link voltage. Low-pass filtering of the measured load current and an additional hysteresis with the amplitude of 1 A will prevent any oscillation at toggling point. Figure 4.8 shows the so-called N_{ph} operating strategy add-on, which is implemented in the existing voltage control loop of the converter.

To integrate the above mentioned operating strategy into the control system of the converter, an additional signal is required to disable the integrator part of the corresponding current controllers (figure 3.24 in section 3.2.3), and deactivate the pulse generator of the affected phases in the modulator. This will guarantee a soft start after reactivating the phases. This so-called phase enable signal is an array of three elements shown in figure 4.8 with $N_{ph,en,123}$ at the output of the hysteresis block. Another variable which is important for a proper interleaving operation is the modulator phase lag (ϕ_{lag} in figure 4.8) which is calculated based on N_{ph} and equation 3.45.

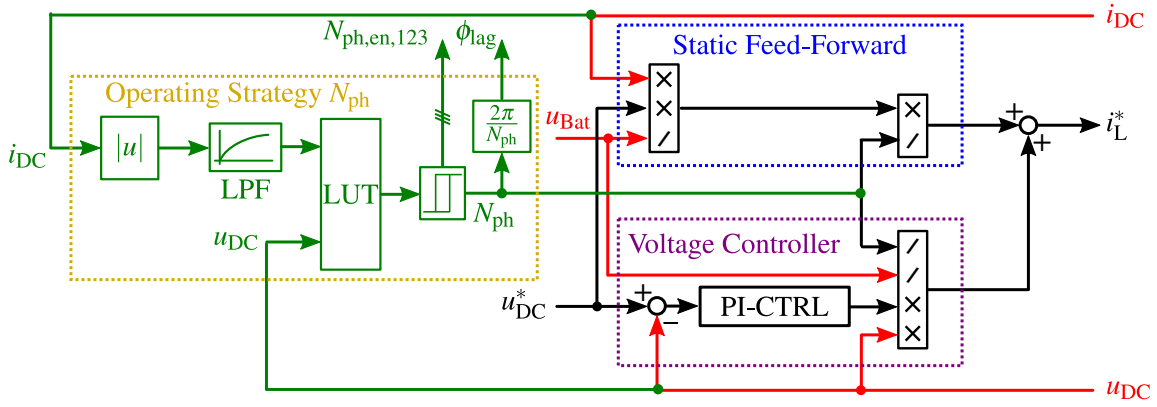

Figure 4.8: N_{ph} operating strategy which is added to the outer loop voltage controller of a multiphase DC-DC converter, and determines the optimal number of active phases

Figure 4.9 shows the placement of the variable phase operating strategy (OS N_{ph}) in the top-level controller and power stage model of the DC-DC converter. As discussed above, the measured load current and DC-link voltage is the input of the added block, and the enable signal as well as the modulator phase lag are the output of the OS N_{ph} block.

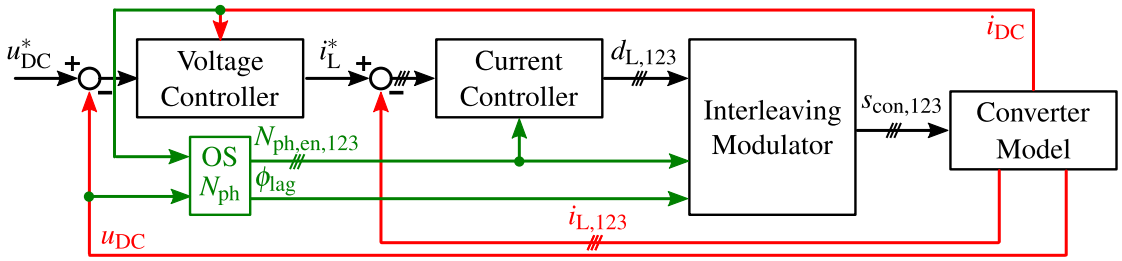

Figure 4.9: Integration of the operating strategy into the top-level DC-DC converter controller

4.2.1 Transient Behavior

In the previous section an operating strategy has been developed and integrated in the control system, which toggles the number of the active phases of the converter to achieve the maximum efficiency for a given operating point (DC-Link voltage and output load). In order to evaluate the feasibility of the provided strategy for a DC-DC converter in an EV drivetrain application, the output voltage transients which are resulting from the toggling of the active phases should be investigated. In this section the simulation results are presented, and the practical results are covered extensively in section 4.5.

Figure 4.10 shows the simulation results of a converter with the battery voltage of 110 V and the output voltage set point equal to 300 V. In order to present all variations of the number of active phases in a short time window, the LUT block shown in figure 4.8 is modified in a way that the converter toggles to 2 and 3 active phases if the current reaches 15 A and 17 A

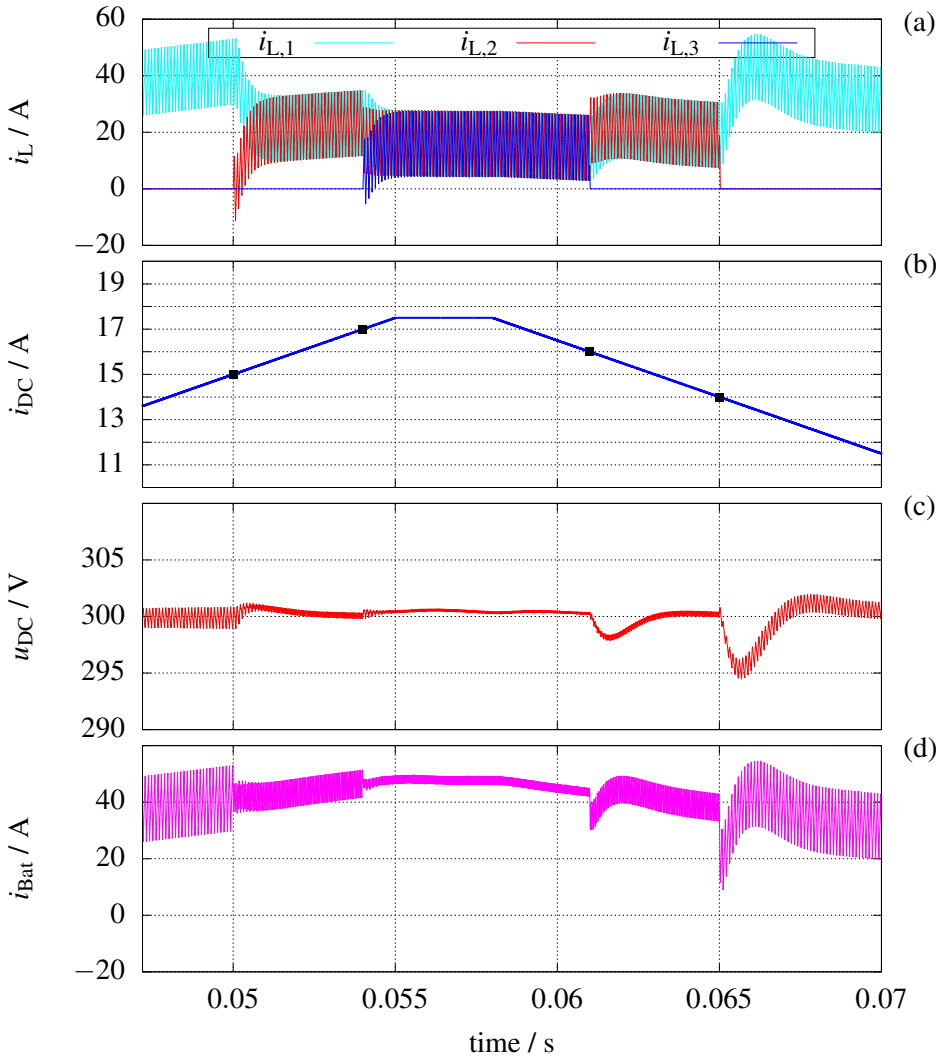

Figure 4.10: Transient behavior of the multiphase converter in the case of activating and deactivating different phases (a) inductor current of the phases (b) load current (c) DC-Link voltage (d) battery current (u_{Bat} = 110 V and u_{DC} = 300 V)

respectively. As mentioned before, each transition level has a hysteresis amplitude of 1 A which will be added to the set limits. The toggling points are all marked in figure 4.10 (b), and it can be seen that they match the chosen current set points. The transient behavior of the phase currents in the vicinity of toggling points presented in figure 4.10 (a) shows a soft transition without any apparent oscillation. The DC-Link voltage transient shown in figure 4.10 (c) proves the good performance of the controller, as in the provided test case the maximum output voltage overshoot/undershoot is as low as 1.7% of the absolute value of the output voltage. Because of the good voltage regulation of the converter during phase toggling, the inverter-fed machine as the converter load remains unaffected from these transients. Therefore, no changes are required on the field-oriented control system, and the developed operating strategy is utilizable without any further ado. Another point worth mentioning is the effect of the converter interleaving operation discussed in section 3.2.2. It is expected that the increased frequency of the output

current (due to interleaving) should result in a lower amplitude of voltage ripple. This can be easily observed on the input current and output voltage in figure 4.10 (c) and 4.10 (d), in which activating an additional converter phase leads to further increase of the ripple frequency and decrease of the ripple amplitude.

4.3 Passive Mode Operation

As discussed in section 4.1 the optimum DC-Link voltage of the converter varies with the operating point of the inverter-fed machine to achieve maximum efficiency of the drivetrain. On the other hand, it is known that the given DC-DC converter topology presented in section 3.2 is a step-up converter which can only boost the voltage to values larger than the battery voltage. According to these facts if the optimum set point value of the DC-Link voltage is smaller than the battery voltage, there is no need for PWM activation, and by sending the converter into the so-called passive mode the amount of generated power losses will be reduced (no switching losses are available).

During the passive mode operation the outer voltage control loop and the inner current control loop (figure 3.27) are running in the background, but their integrator parts are all deactivated. This guarantees a soft start of the converter in the case of toggling back to active operation. Furthermore, to realize the passive operation the duty cycles of the converter phases ($d_{\mathrm{L},123}$) are all set to 0. This will put the high side transistors of the three phases into the conduction mode, and depending on the output current direction either the high side diodes or the high side transistors take over the current conduction. Figure 4.11 shows the implementation of the passive mode operation in the control system. The added block (OS PM) will either pass through the current controller outputs ($d_{\mathrm{L},123}$) directly to the modulator, or set all of the duty cycles to zero in the case of an enabled passive mode.

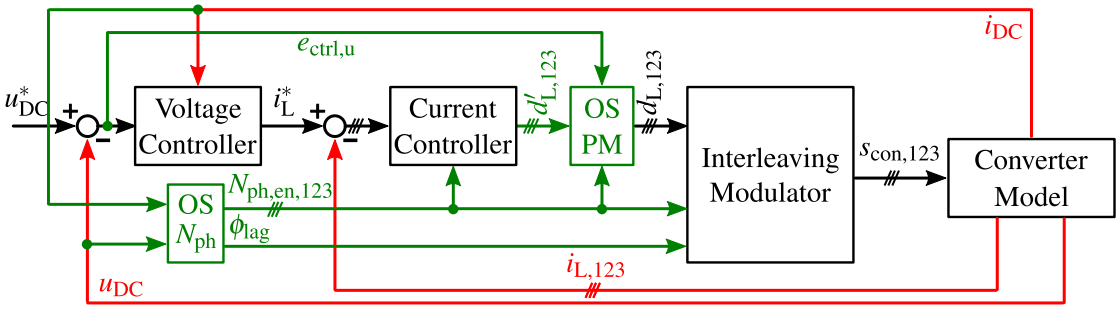

Figure 4.11: Integration of the passive mode operating strategy into the top-level DC-DC converter controller

In the first place, enabling the passive mode operation and setting the duty cycles to zero will be started by checking the value of the error signal at the input of the voltage controller. If the controller deviation $e_{\mathrm{ctrl,u}}$ is smaller than a given limit (in this case 2 V) and at the same time one of the following conditions is satisfied, then the controller goes to the passive mode.

- If the first phase is activated ($N_{\text{ph,en,1}} = 1$) and its duty cycle is smaller than 1% ($d_{\text{L,1}} \leq 0.01$)
- If the second phase is activated ($N_{\text{ph,en,2}} = 1$) and its duty cycle is smaller than 1% ($d_{\text{L,2}} \leq 0.01$)
- If the third phase is activated ($N_{\text{ph,en,3}} = 1$) and its duty cycle is smaller than 1% ($d_{\text{L,3}} \leq 0.01$)

During the time that the controller is in the passive mode the voltage deviation is being evaluated continuously, and as soon as it becomes more than 2 V again, the controller toggles to active operating mode and all integrators in figure 3.26 and figure 3.24 get enabled.

4.3.1 Transient Behavior

In order to evaluate the transient behavior resulted from activating and deactivating the passive mode, the system shown in figure 4.11 is implemented and a test case presented in figure 4.12 is provided. In the beginning of this test case the DC-Link voltage is set to 130 V and at 0.02 s the set point is decreasing with the ratio of 500 V/s so that it falls below the battery voltage ($u_{\text{Bat}} = 110$ V), as shown in figure 4.12 (b). During this time interval the duty cycles of the three phases are decreasing and they reach 0.01 at 0.0605 s. Exactly at this point all the conditions for passive operation are satisfied, and the converter toggles to this operation mode and set all the duty cycles to zero as shown in figure 4.12 (c) and (d). The test case is then continued and at 0.07 s the voltage set point variation changes its direction and starts increasing with the same rate of 500 V/s. Finally at 0.0815 s the control deviation (difference between the voltage set point and actual value) gets larger than 2 V and the DC-DC converter wakes up and tries to regulate the output voltage.

As shown in figure 4.12 (a) the inductor currents of the converter phases are distributed symmetrically throughout the passive mode. Furthermore, during the transition times from active to passive operation and vice versa the output voltage of the converter shows an acceptable transient response (see figure 4.12 (b)). This means that this operating strategy can be utilized in the drivetrain controller without any significant effect on the inverter-fed machine control system. It is worth to mention that the voltage and current oscillations which are emerging directly after passive mode activation are because of the abrupt shutdown of the converter. This will lead to three floating switching nodes shown in figure 3.16, which in turn results in the excitation of the resonant circuit formed by the phase inductors and the DC-Link capacitor. This oscillation will eventually be damped through the internal resistances of the inductor and capacitor and doesn't create any opertional problem.

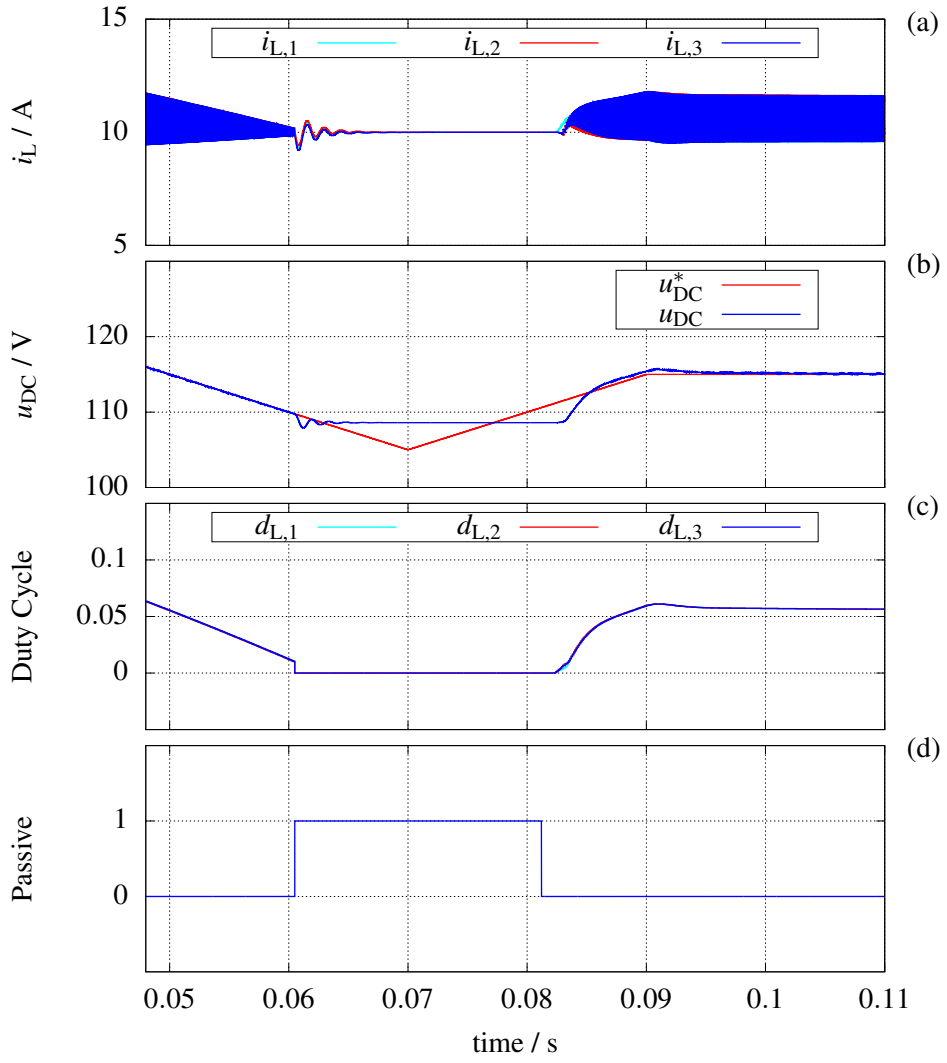

Figure 4.12: Transient behavior of the multiphase converter in the case of activating and deactivating the passive mode (a) inductor current of the phases (b) DC-Link voltage set point and actual value (c) duty cycles of the three phases (d) passive mode (u_{Bat} = 110 V)

4.4 Variable Switching Frequency

As it has been discussed in section 3.2.2 a multiphase converter can operate in the interleaving mode, in which implementing a phase delay between the pulses of each phase leads to the input current ripple reduction. Regarding this, it has been shown that the input current ripple is depending, inter alia, on the number of the active phases, switching frequency, and output voltage. This dependency has been formulated using equation 3.46. With the help of this equation and for a 3-phase converter with the parameters stated in table 3.2 the input current ripple is calculated for different switching frequencies, output voltages, and number of active phases. Figure 4.13 presents three diagrams each shows the current ripple of the converter for a given number of active phases N_{ph} and in dependency of switching frequency and DC-Link voltage.

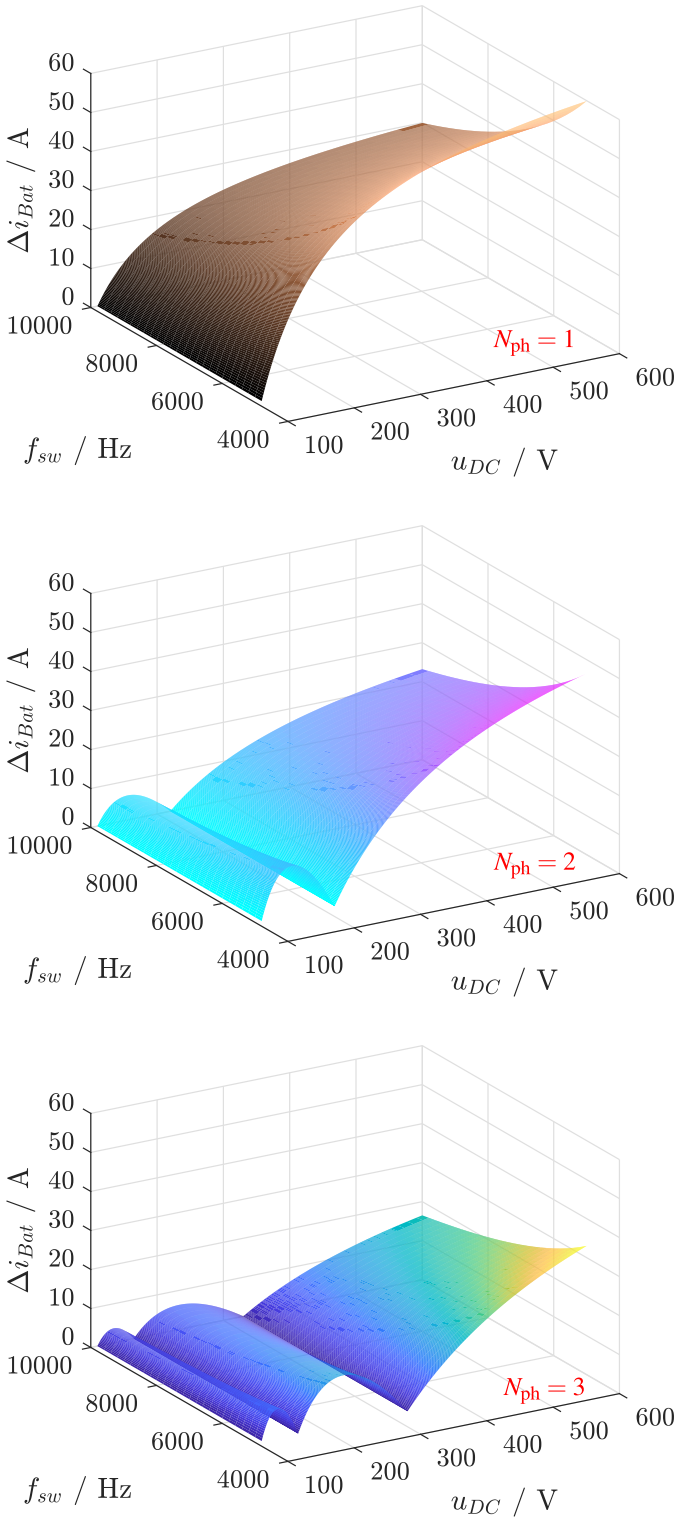

Figure 4.13: Input current ripple of a multiphase DC-DC converter with u_{Bat} = 110 V for different switching frequencies, DC-Link voltages, and number of interleaving active phases

In the design process of the system, a maximum acceptable value is defined for the battery current ripple ($\Delta i_{\mathrm{Bat,fix}}$). As it has been shown in figure 4.13, the input current ripple of the converter has an inverse relation to the switching frequency of its half-bridges. In the case of a current ripple smaller than the maximum acceptable value, the frequency dependency of the current ripple can be exploited to reduce the switching power losses of the converter by reducing the switching frequency. In conjunction with the aforementioned operating strategies, namely the variable DC-Link voltage (section 4.1) and variable number of active phases (section 4.2), this operating strategy is the last piece of the puzzle and determines the minimum possible switching frequency for a given DC-Link voltage and number of active phases, so that the input current ripple remains in the defined limit of $\Delta i_{\mathrm{Bat,fix}}$.

For the implementation purposes the switching frequency is calculated using equation 3.46, so that the second part of this equation is realized in the form of a look-up-table with the inputs shown in equation 4.3. In this equation x is an integer between zero and $N_{ph}-1$, and is calculated so that the duty cycle of the converter d_{L} at the given operating point gets inside the range of $\frac{x}{N_{\mathrm{ph}}}$ and $\frac{x+1}{N_{\mathrm{ph}}}$.

$$\mathrm{LUT}_{\mathrm{freq}}(d_{\mathrm{L}},N_{\mathrm{ph}}) = \left(d_{\mathrm{L}} - \frac{x}{N_{\mathrm{ph}}}\right)\cdot\left(x+1-N_{\mathrm{ph}}\cdot d_{\mathrm{L}}\right) \tag{4.3}$$

The resulting LUT output which is calculated for a given duty cycle and number of active phases is then used in equation 4.4 to determine the required switching frequency, with which the input current ripple of the converter is limited to $\Delta i_{\mathrm{Bat,fix}}$.

$$f_{\mathrm{sw}} = \mathrm{LUT}_{\mathrm{freq}}\cdot u_{\mathrm{DC}}\cdot\frac{1}{L\,\Delta i_{\mathrm{Bat,fix}}} \tag{4.4}$$

The calculated frequency in equation 4.4 is then quantized to 100 Hz, and limited to the minimum and maximum switching frequencies imposed by the hardware. Figure 4.14 shows the algorithm implemented in the controller to calculate the loss optimized switching frequency.

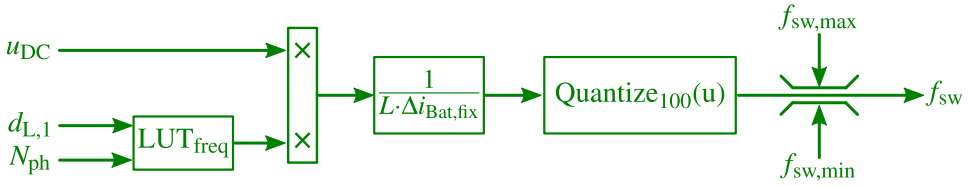

Figure 4.14: Implemented procedure in the controller to calculate the proper switching frequency required for achieving a maximum input current ripple of $\Delta i_{\mathrm{Bat,fix}}$

Finally the third operating strategy with a variable switching frequency is integrated into converter controller as shown in figure 4.15. The new block calculates the optimal switching frequency and feed the result into the interleaving modulator.

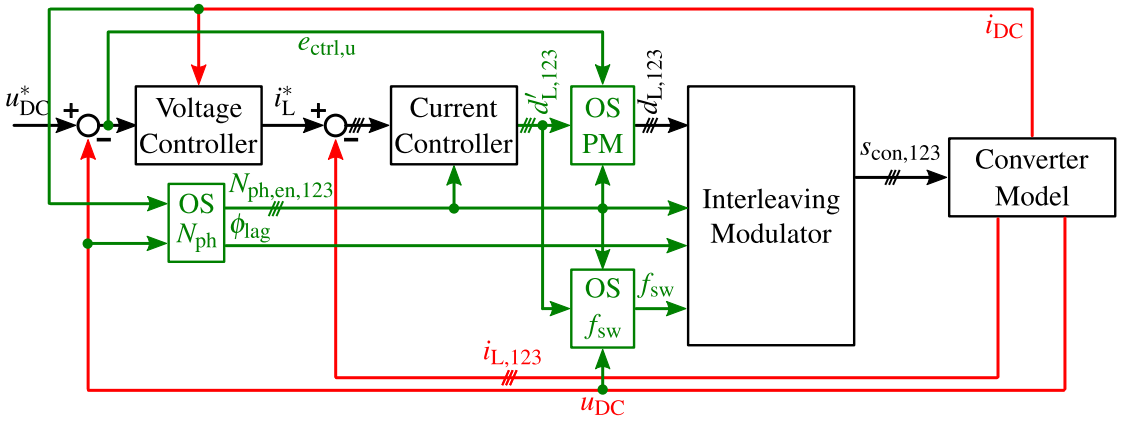

Figure 4.15: Integration of the variable switching frequency operating strategy into the top-level DC-DC converter controller

4.4.1 Transient Behavior

In order to evaluate the transients caused by changing the switching frequency a test case is provided, in which while the DC-Link voltage is set to 300 V (battery voltage is equal to 110 V) the load current increases from 14 A to 17.5 A in 70 ms. During this time the operating strategy introduced in section 4.2 changes the number of active phases automatically to achieve a maximum efficiency. For the implementation of the new operating strategy, the lower and upper switching frequency limits of the converter are set to 5 kHz and 16 kHz respectively, and the maximum allowed input current ripple is set to 15 A.

In the beginning of this test case only one phase is activated, and the input current ripple resulted from the selected switching frequency (15.5 kHz) is equal to to 14.6 A. At 0.05 s the number of active phases changes from one to two, and the new operating strategy detects the changes in the input current ripple and automatically sets the switching frequency to 6.5 kHz so that the resulted input current ripple (figure 4.16 (e)) remains the same as the ripple before the phase toggling. As shown in figure 4.16 (a) and (c) the frequency change does handle by the control system pretty well, and the phase currents and the output voltage preserve their good dynamic behavior. This is also true when N_{ph} is increased to three active phases at 0.054 s and the switching frequency is set to its minimum of 5 kHz (figure 4.16 (c)). With respect to the acceptable dynamic behavior of the system, the new operating strategy with variable switching frequency is feasible and can be evaluated on a prototype test setup without changing anything in the field oriented control of the inverter-fed machine.

4.5 Test-setup and Experimental Results

After the simulation-based evaluation of the drivetrain and its control system using the developed switching model and the state-space average model, in this section these simulation results are

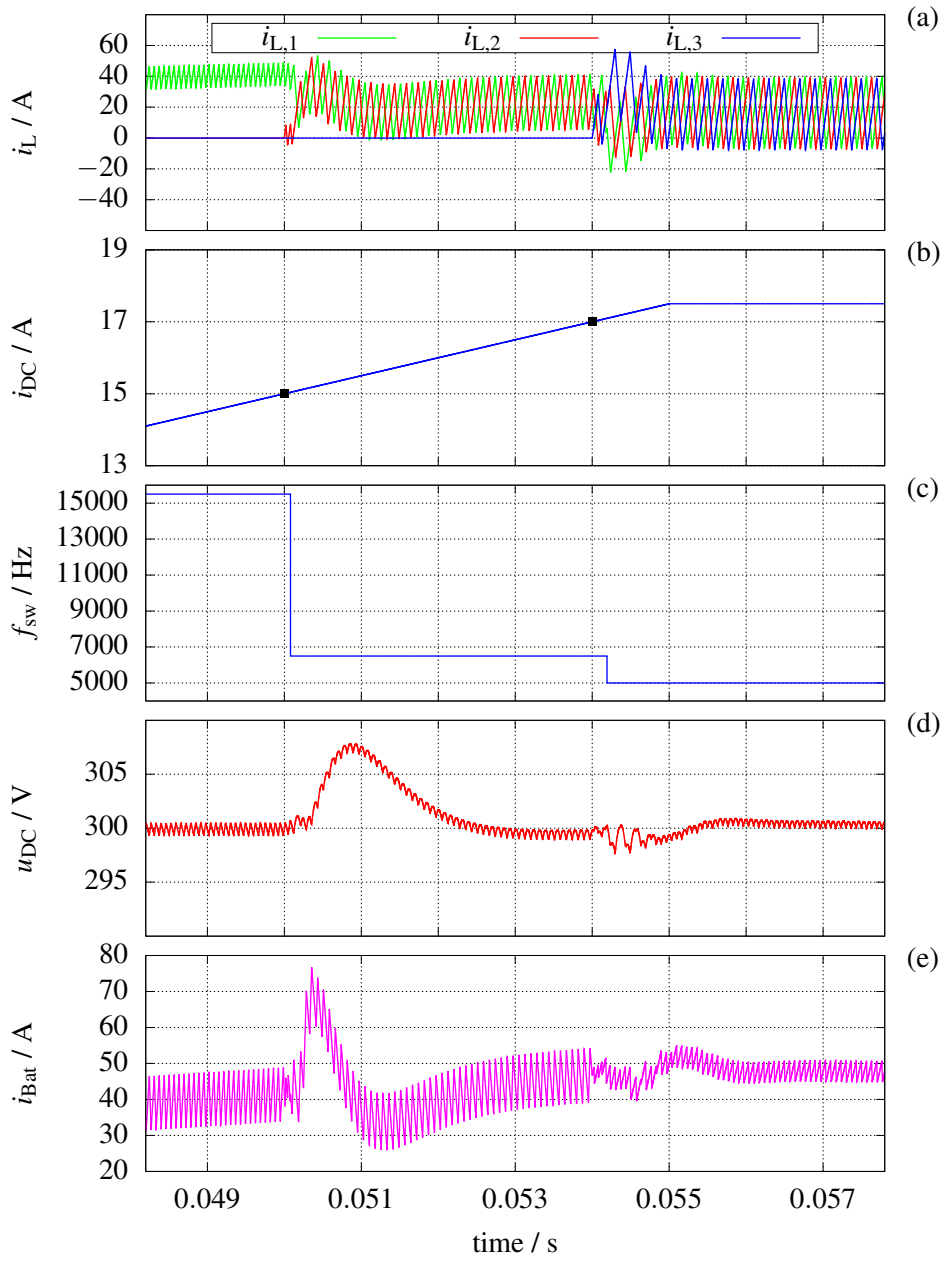

Figure 4.16: Transient behavior of the multiphase converter (table 4.1) in the case of variable switching frequency (a) inductor current of the phases (b) DC-Link current (c) switching frequency (d) DC-Link voltage (e) input current (u_{Bat} = 110 V and u_{DC} = 300 V)

verified and validated in practice. The focus of this verification is on the DC-DC converter part of the drivetrain. For this purpose, a test setup is constructed to investigate the dynamic behavior of the control system as well as the efficiency and power dissipation of the converter. The test setup created can be integrated into the existing setup of the conventional drivetrain for future works.

4.5.1 Construction of the Test-Setup

The heart of the test setup is a three-phase DC-DC converter with the dedicated control and protection system. As shown in figure 4.17 the power transistors of the converter are realized using the HybridPACK 2 module from Infineon, which composed of three IGBT-based half-bridges, dedicated gate-drivers, and a 500 μF DC-Link capacitor (various characteristics of this module are already presented in chapter 2).

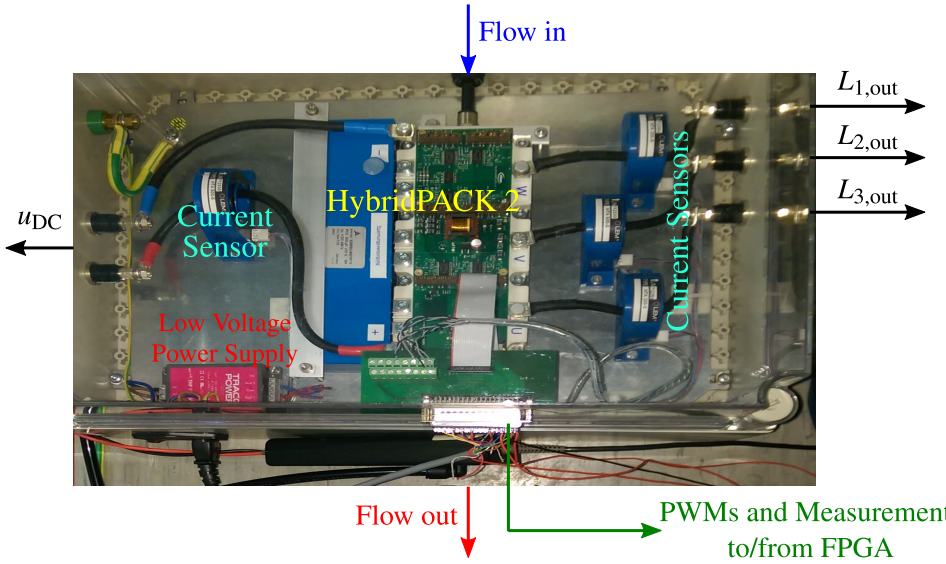

Figure 4.17: HybridPACK 2 equipped with current sensors and a low voltage power supply built in the frame of the research work

This IGBT module is mounted on a water-cooled heat-sink, which its in- and outlet are driven by a cooling rack from Innovatek company with the rating dissipation power of 500 W. As shown in figure 4.17 the integrated driver and control board of the IGBT-module is powered by a low voltage power supply from Traco Power, and four current sensors (LEM HTA500) are included in the main setup-box to measure the phase inductor currents as well as the DC-Link current. The setup-box are equipped with safety plugs to provide connections to the three inductors, and the output DC-Link. Furthermore the measurement signals and the IGBT-module control signals are accessible through a Sub-D connecter on the side of the setup-box.

An overview of the developed test setup which contains the aforementioned setup-box is presented in figure 4.18. At the input side of the box three inductors each with the inductance of 300 μH are utilized, for which the iron-powder toroid cores with the properties of table 2.4 and the winding specifications of table 2.3 are used. As described in [56], this type of core material is appropriate for frequency ranges of around 10 kHz. The input side of the converter is connected to a DC power supply through a pre-charged capacitor bank and a high-speed relay, which can disconnect the supply from the converter. The relay control signal is routed via the FPGA to the central protection unit. At the output side of the converter an electrical load can be

switched on and off. Additionally the converter output is protected against overvoltage with the help of a chopper circuit, which loads the converter with an extra break resistor in the case of an overvoltage. In such an event a flag is sent to the central protection unit in parallel to actively disable the PWM unit of the control board. The measurement interface of the setup-box (figure 4.17) are connected to a custom designed data acquisition board equipped with ΣΔ analog to digital converters. The data acquisition board actively oversample the current and voltage values during a PWM period and send the result to a connected FPGA board (Protolar FPGA.Comm communication module), which provides the proper ADC clock signal for ΣΔ converters and catches and processes the ADC outputs. Another role of the FPGA is to communicate with the dSPACE system to send the last measurements and receive the PWM signals and finally forward them to the setup-box.

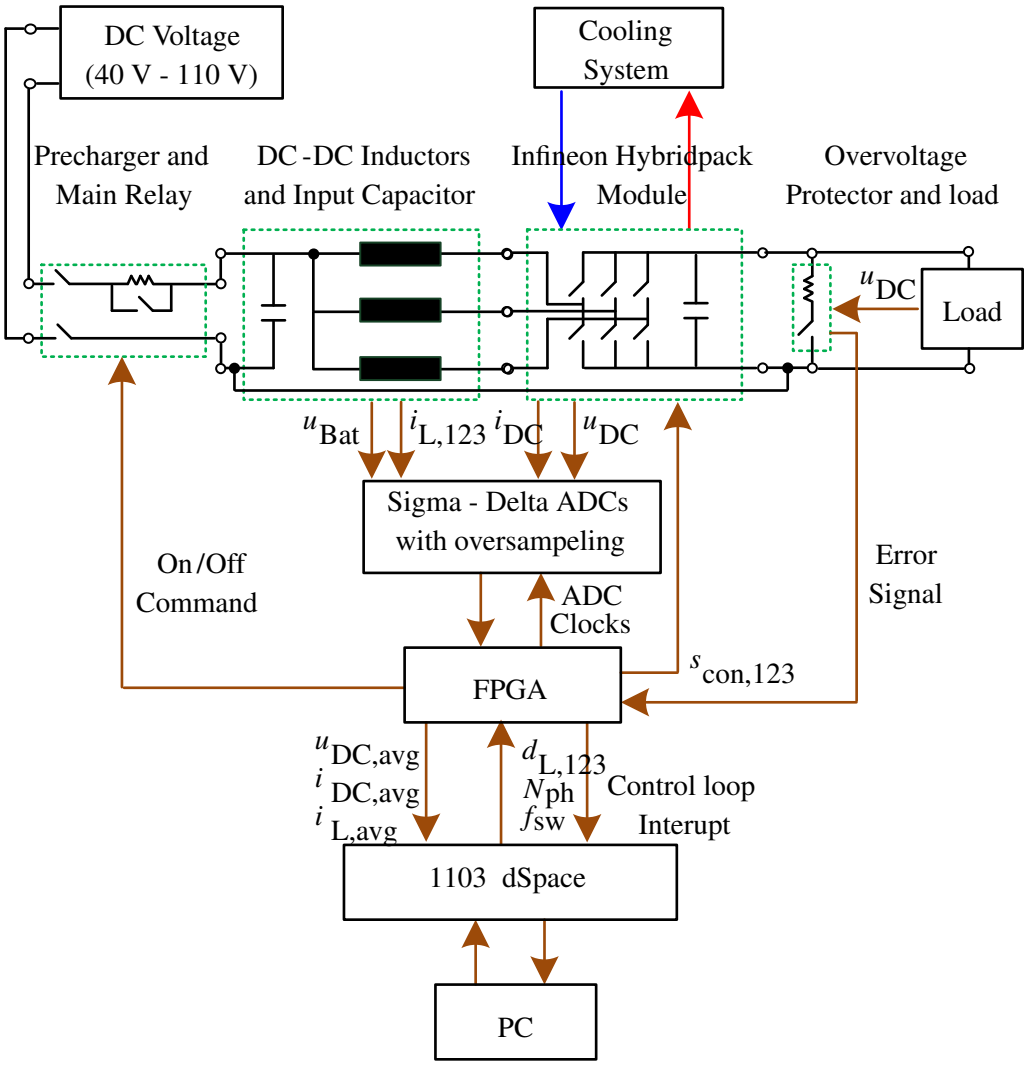

Figure 4.18: Developed three-phase DC-DC converter with the dedicated control system and protection system

4.5.1.1 Control and Measurement Unit

The control and protection algorithm are designed and modeled in SIMULINK and a real-time control prototyping system (dSPACE 1103) is used to execute the algorithm at the hardware level in real time. On the hardware side the dSPACE system provides a real-time target which together with the real-time workshop from the MathWorks enable an automatically generated real-time code from SIMULINK models and implement it on the dSPACE real-time hardware. Additional to that the dSPACE hardware contains various IOs, which can be used for the control and protection system interaction with the rest of the system. In this work the respected IOs are all configured and included in the SIMULINK to provide the proper interface between the algorithm on the dSPACE and the FPGA.Comm communication module. On the other hand the FPGA.Comm drive the connected data acquisition board, and sample and process the ADC outputs. The FPGA.Comm module is the central communication and measurement processing unit of the control and protection system and is responsible for the tasks listed in the following enumeration. The FPGA Firmware is therefore personalized and extended to realize and fulfill these requirement.

1. Implementing a 3-phase interleaving modulator for DC-DC converter with variable number of active phases and variable switching frequency
2. Periodically triggering the interrupt service routine of the control and protection algorithm on the dSPACE based on the PWM period (switching frequency) at the given operating point
3. Driving the data acquisition board with the proper ADC clock signal
4. Processing the generated bit stream at the output of the $\Sigma\Delta$ converters and calculate the signal average value during a PWM period
5. Providing a communication kernel between the dSPACE and FPGA.Comm

Figure 4.19 shows an overview of the relevant components of the converter control and protection system and their interconnections. The dSPACE system provides a graphical user interface (ControlDesk) in addition to the hardware module, which runs on the host PC. This user interface enables the interaction with the control system and can be populated with different user-defined monitoring, data logging, and control elements. These virtual push bottoms, sliders, and data plotters/logger (shown in figure 4.19) are directly connected to different internal variables and signals of the control and protection system through the so-called dSPACE link board card (installed in the PCI slot of the host PC). With the help of the created user interface the converter can be switched on and off, and different operating modes such as fixed DC-Link voltage, switching frequency, or the number of active phases can be activated. Furthermore different signals such as phase currents and input and output voltages can be logged with a sampling frequency equals the ISR frequency.

As discussed above and shown in figure 4.19 a custom code on the FPGA.Comm provides the 3-phase interleaving modulator functionality (see figure 3.18 in section 3.2.2). This modulator

is implemented based on a two-level state machine concept, in which the actual register value of the PWM counters of each converter phases are determined according to the number of active phases. Furthermore the maximum value of the PWM counters are determined based on the switching frequency. During the transition intervals (toggling the switching frequency or the number of active phases) the actual register values are optimized in a way to achieve minimum state discontinuities.

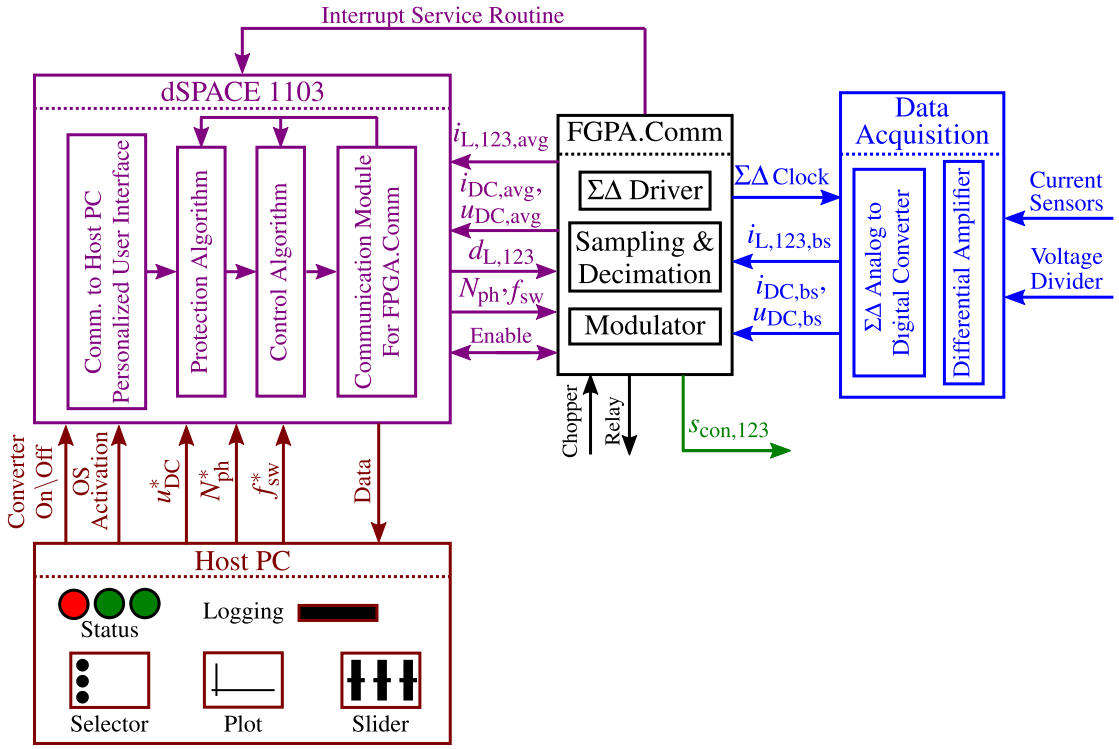

Figure 4.19: Central role of FPGA.Comm and its connection to the custom data acquisition board, dSPACE, setup-box, and host PC

Another implemented part in the customized code of the FPGA.Comm realizes the driving signals of the ΣΔ modulators on the data acquisition board (DAB), and samples and processes the resulted bit streams received from the output of the modulators. Figure 4.20 shows the developed data acquisition board and its interconnection with the FPGA.Comm. The DAB itself consists of five analog input channels, four of which connect the LEM current sensors to LMP8350 on the DAB, which is an ultra-low distortion fully-differential precision instrumentation amplifiers. The fifth input channel of the DAB is dedicated for the DC-Link voltage measurement, and is connected to a voltage divider and an amplifier with high input impedance on the DAB.

The input analog stage of the data acquisition board is followed by the analog to digital data conversion stage, which consists of five ΣΔ modulators realized using ACPL-796J from AVAGO Technologies. Basically, the so-called ΣΔ analog to digital converter is including an oversampling modulator and a digital/decimation filter that together produce a high resolution data-stream. In this structure the output of the modulator is a high frequency 1-bit data stream, which is calculated by integrating the error signal resulted from the deviation of the analog input signal of interest from the modulator output at the previous step (the digital output is converted

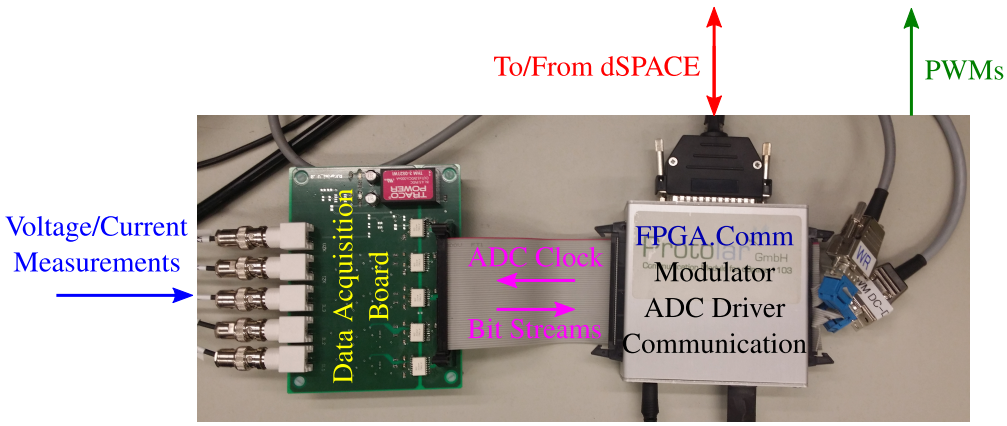

Figure 4.20: Data acquisition board and its connection to the FPGA.Comm with the custom programmed ΣΔ driver and processor

to an analog signal switched between the non-inverted and the inverted value of the internal reference voltage of the modulator in the case of logic high and logic low respectively).

Figure 4.21 shows the signal chain between the analog measured current (or voltage) all the way up to the generated digital output for the controller implemented in the dSPACE. After the analog conversion of the input signal, an oversampled 1-bit data stream is produced at the output of the modulator which then is accumulated and averaged over the time with the help of the customized digital/decimation filter implemented in FPGA.Comm. One of the advantages of using ΣΔ analog to digital conversion approach is its intrinsic noise shaping feature [101], which shifts the low frequency noises to high frequency domains using oversampling and then removing the noise at the decimation stage. As shown in figure 4.21 the clock signal of the ΣΔ modulator is synchronized with 1000 times of DC-DC converter PWM frequency (also known as the controller update rate), and can be changed over the course of time and based on the given operating point of the converter (see section 4.4). Finally the implemented decimation block (the decimation factor is set to 1000) averages the bit-stream data and provides an output digital signal which is synchronized with the controller frequency.

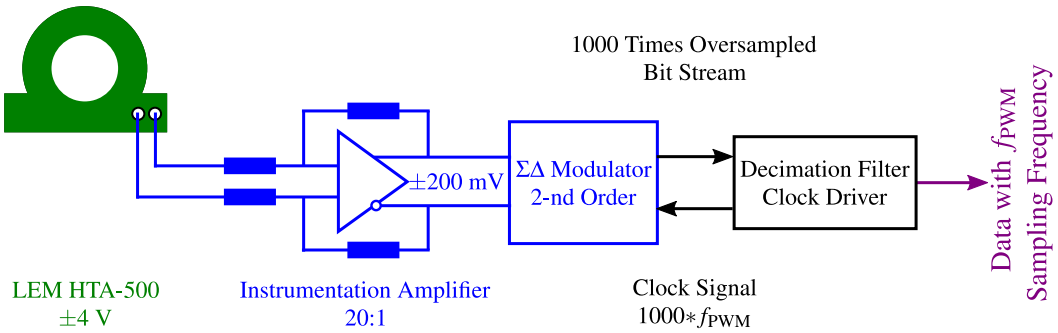

Figure 4.21: Analog to digital signal chain using instrumentation amplifier and ΣΔ modulator with 1000 times oversampling

4.5.2 Experimental Results

After introducing the test setup itself, some experimental results are provided in this section in order to evaluate the functionality of the control concept, and to verify the developed loss models, based on which the loss optimizing operating strategies are designed. In the first step the output voltage regulation of the converter is experimentally evaluated. Figure 4.22 shows the data acquisition board log data measured using FPGA and sampled by dSPACE with the same data rate as the frequency of the interrupt service routine (figure 4.19). The executed test case includes three output voltage set point steps of 100 V, 180 V, and 260 V and the constant input voltage ($u_{\mathrm{in}} = 80$ V), output load ($R_{\mathrm{load}} = 11\ \Omega$), switching frequency ($f_{\mathrm{sw}} = 10$ kHz), and the number of active phases ($N_{\mathrm{ph}} = 3$). As shown in figure 4.22 (c) the output voltage of the converter is perfectly reaching the desired set point and according to figure 4.22 (b) the input current is distributed symmetrically between the three converter phases.

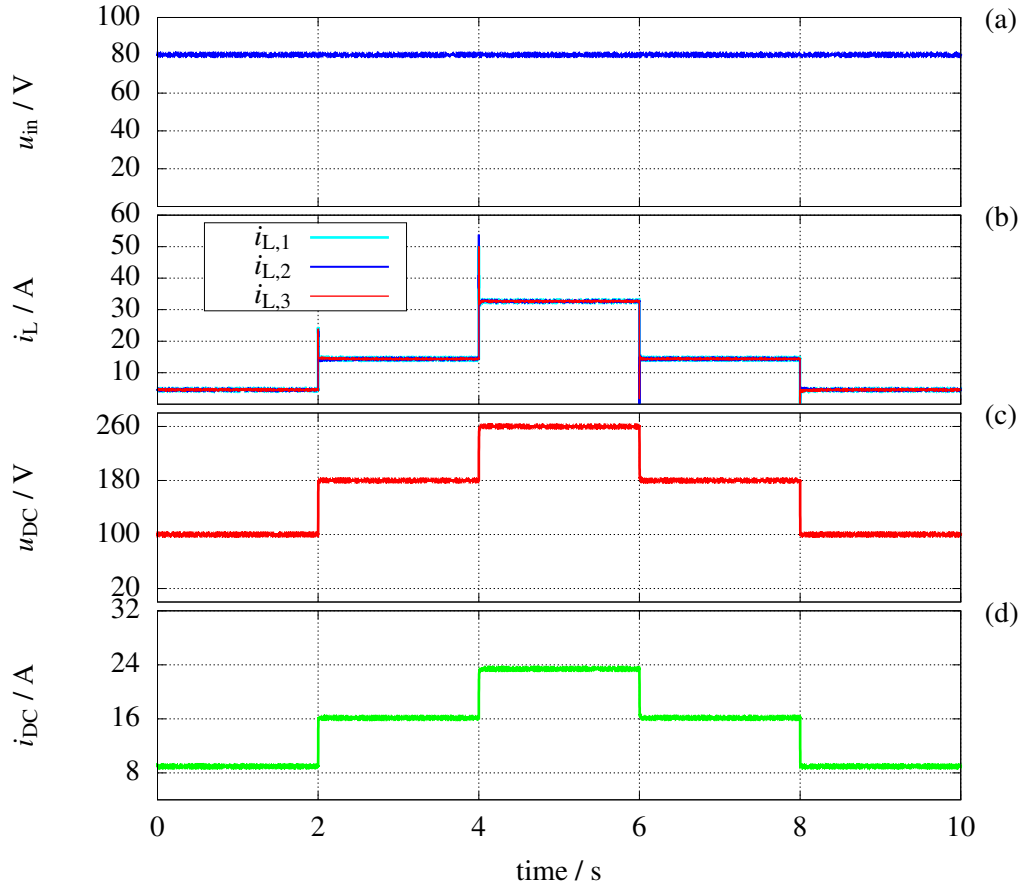

Figure 4.22: Data acquisition board log data to investigate the line regulation under variable output voltage set point ($u^*_{\mathrm{DC}} = 100$ V, 180 V, and 260 V) and a constant input voltage ($u_{\mathrm{in}} = 80$ V) and resistive load ($R_{\mathrm{load}} = 11\ \Omega$) (a) input voltage (b) inductor current of the three converter phases (c) DC-Link voltage (d) DC-Link current

In the next test case the input and output voltages are set to constant values ($u_{\mathrm{in}} = 40$ V and $u^*_{\mathrm{DC}} = 90$ V) and the output load is changed between $R_{\mathrm{load}} = 11\ \Omega$ and $R_{\mathrm{load}} = 9\ \Omega$ in 0.5 Ω steps. Additional to that during this test case the variable number of active phases is enabled according

to the operating strategy developed and introduced in section 4.2. Figure 4.23 presents the results of this experiment which indicates on the one hand an acceptable load regulation of the converter and on the other hand correct toggling of the converter between different number of the active phases.

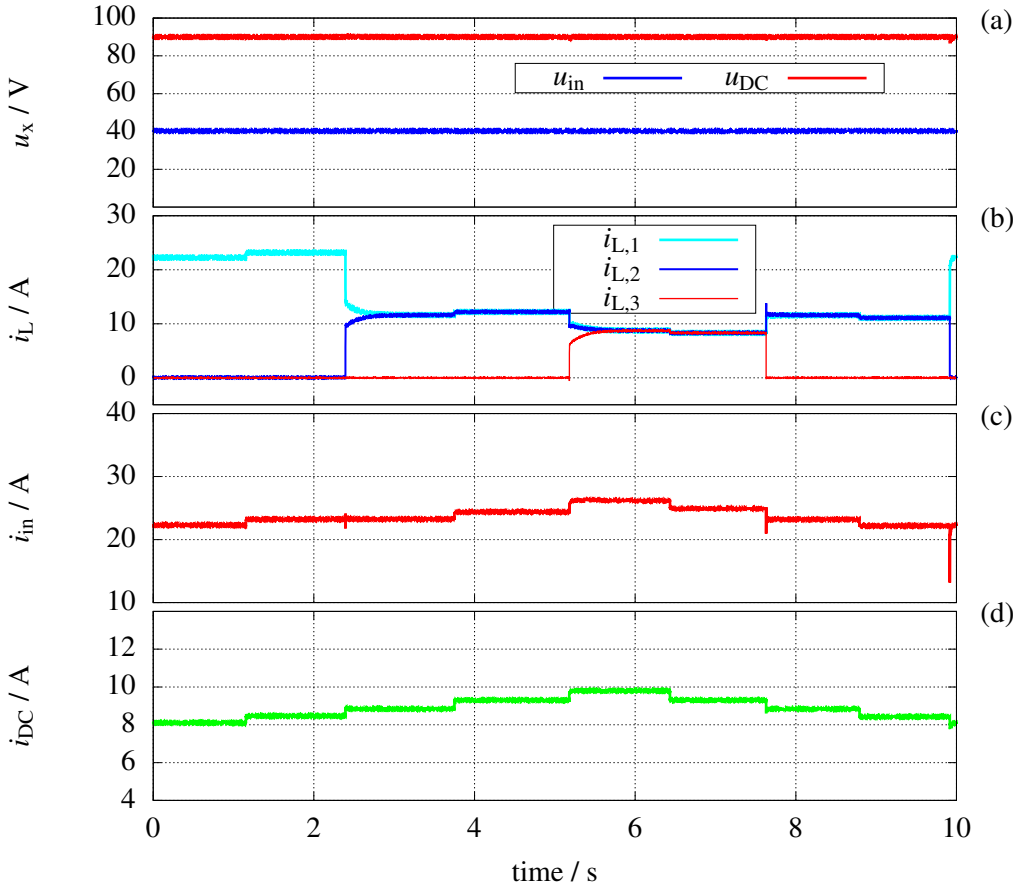

Figure 4.23: Data acquisition board log data to investigate the load regulation under variable output load (R_{load} =11 Ω to 9 Ω) and a constant input voltage ($u_{in} = 40$ V) and output voltage set point (u^*_{DC} =90 V) (a) input and output voltages (b) inductor current of the three converter phases (c) input current (d) DC-Link current

As stated above the experimental results shown in figures 4.22 and 4.23 are solely the signals measured and feed into the converter controller implemented in dSPACE. In order to evaluate the actual transient behavior of the converter, the desired signals such as output voltage and inductor currents should be measured with a high resolution oscilloscope during the transition times. Therefore, in the next step the controller performance is evaluated under three test conditions which are relevant for the implementation of the operating strategies, namely the variable DC-Link voltage, the variable number of active phases, and the variable switching frequency. In all three tests, the input voltage is set to 80 V, and a 10 Ω resistor is used as a resistive load. Figure 4.24 shows the result of the first test case, in which the output voltage set point jumps from 90 V to 135 V. As shown in this figure a smooth voltage transition takes place within 570 μSec and a symmetrical decrease of the duty cycles of the three phases of the converter is observable through the inductor currents.

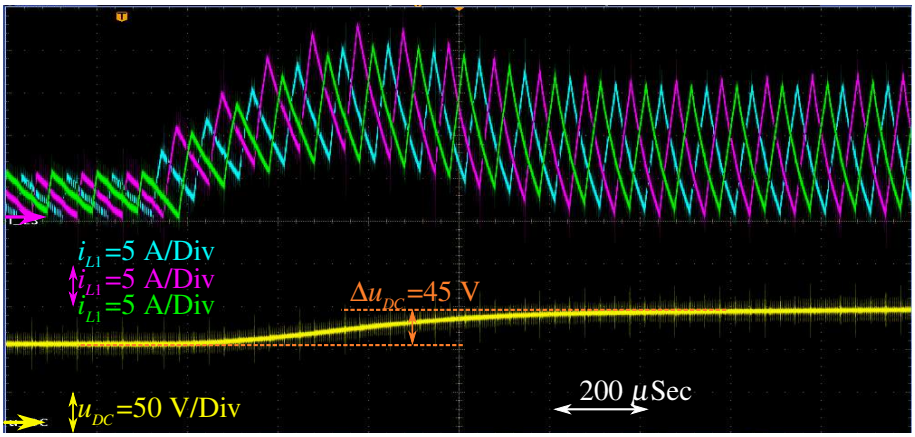

Figure 4.24: The transient response of the converter for variable DC-link voltage $u^*_{\mathrm{DC}} = 90\ \mathrm{V} \Rightarrow 135\ \mathrm{V}$, $f_{\mathrm{sw}} = 10\ \mathrm{kHz}$, and $N_{\mathrm{ph}} = 3$

The next test case covers the transient behavior of the converter during the transition between different number of active phases. Figure 4.25 shows the converter output voltage and inductor currents after changing N_{ph} from three to two active phases. Based on this result the converter can handle this transition without any considerable impact on the output voltage regulation. Another point worth mentioning is the proper operation of the interleaving modulator. As discussed in section 3.2.2, in the interleaving mode the phase lag between the converter phases should change according to the number of active phases in order to achieve the minimum input current ripple. With respect to the inductor current waveforms shown in figure 4.25 the phase lag between the currents is changing from 120° to 180° after the transition, which matches the requirements defined in equation 3.45 and proves the correct functionality of the modulator.

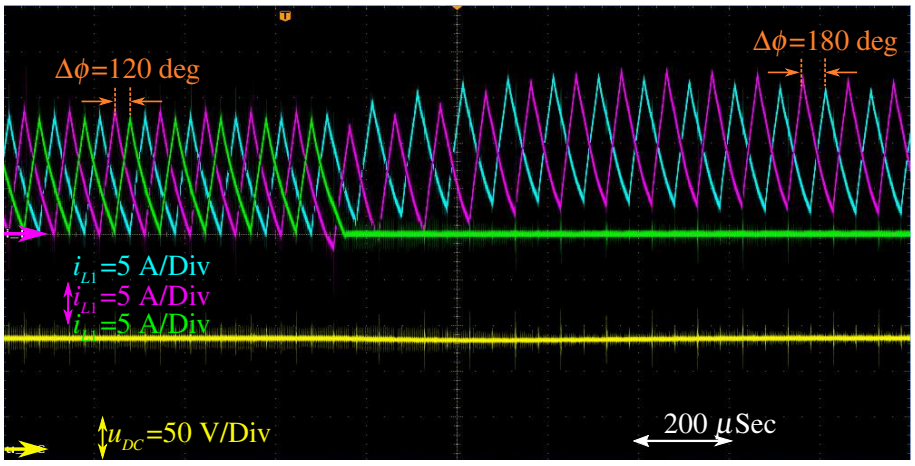

Figure 4.25: The transient response of the converter for variable phase number $N_{\mathrm{ph}} = 3 \Rightarrow 2$ (phase delay between the phases from 120° to 180°), $u^*_{\mathrm{DC}} = 120\ \mathrm{V}$, and $f_{\mathrm{sw}} = 10\ \mathrm{kHz}$

In the last test case the transient behavior of the converter under variable switching frequency operation is investigated. Figure 4.26 shows the result of this test case, in which the switching frequency is changed from 10 kHz to 5 kHz under the load. With respect to this result the output

voltage regulation of the converter is properly maintained under this specific operation and the phase currents remain stable and symmetrical during and after this transition. As expected by halving the switching frequency the current ripple of each one of the converter phases is doubled.

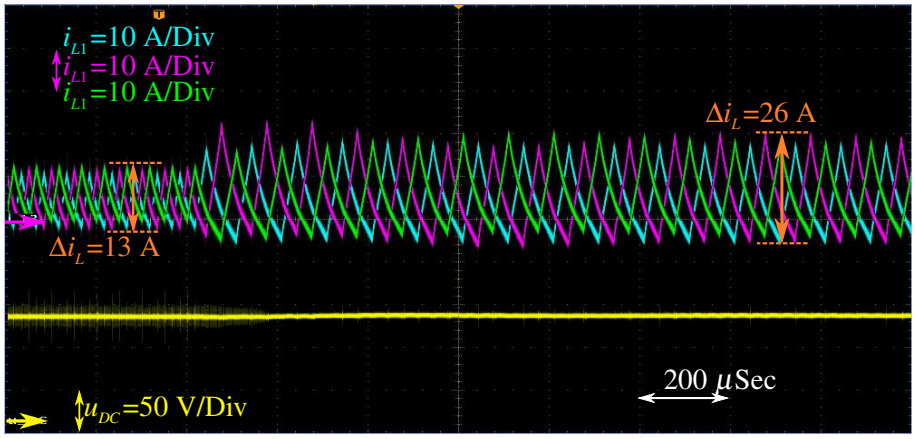

Figure 4.26: The transient response of the converter for variable switching frequency $f_{sw} = 10$ kHz $\Rightarrow$ 5 kHz, $u^*_{DC} = 120$ V, and $N_{ph} = 3$

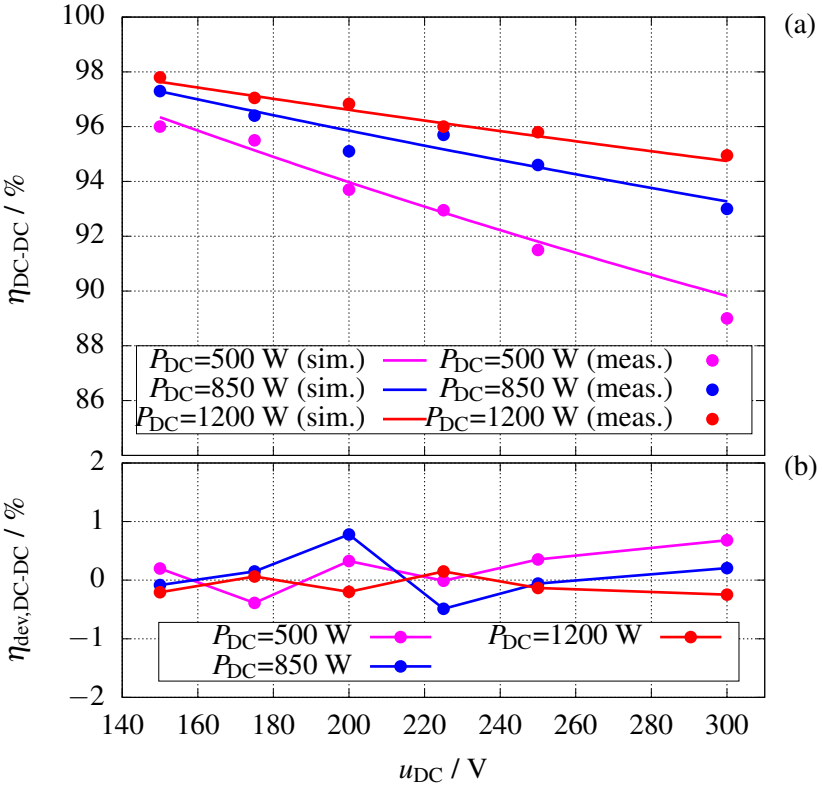

Figure 4.27: The efficiency of the converter for different DC-Link voltages and output powers ($u_{Bat} = 110$ V, $N_{ph} = 3$, and $f_{sw} = 10$ kHz) (a) simulated efficiency against measured efficiency (b) deviation between the simulation and measurement

After evaluating the controller performance and the transient response of the inverter using different operating strategies, this part examines the DC-DC converter efficiency to verify, on the one hand, the accuracy of the developed converter loss models and, and on the other hand, the actual benefits of using the above operating strategies. For the efficiency measurement the LMG 500 power analyzer from Zimmer is used with a 4-wire configuration of the input and output of the converter. In addition to that, in order to have a better control over the load, instead of a resistive load, an electronic load from EA (ELR 9000 series) with the maximum power of 10 kW is used.

The first point which should be verified is the dependency of the efficiency of the converter on the DC-Link voltage. As discussed in section 4.1 and with reference to the simulation results shown in figure 4.2, the most efficiency improvements are achieved by varying the DC link voltage at partial loads. Therefore, for the model verification regarding the efficiency dependency on the DC-Link voltage, the multiphase converter is operated in partial load condition (three different load values are applied) and 6 different output voltages from 150 V to 300 V (input voltage of the converter is set to 110 V, all three phases are enabled, and the switching frequency is 10 kHz). Figure 4.27 (a) shows the efficiency measurement results for the above operating points together with the simulation results of the model. The deviation between the simulation result and the measurement at each operating point is illustrated in figure 4.1 (b). The overall picture depicted in figure 4.27, matches and verifies the simulation results presented and discussed

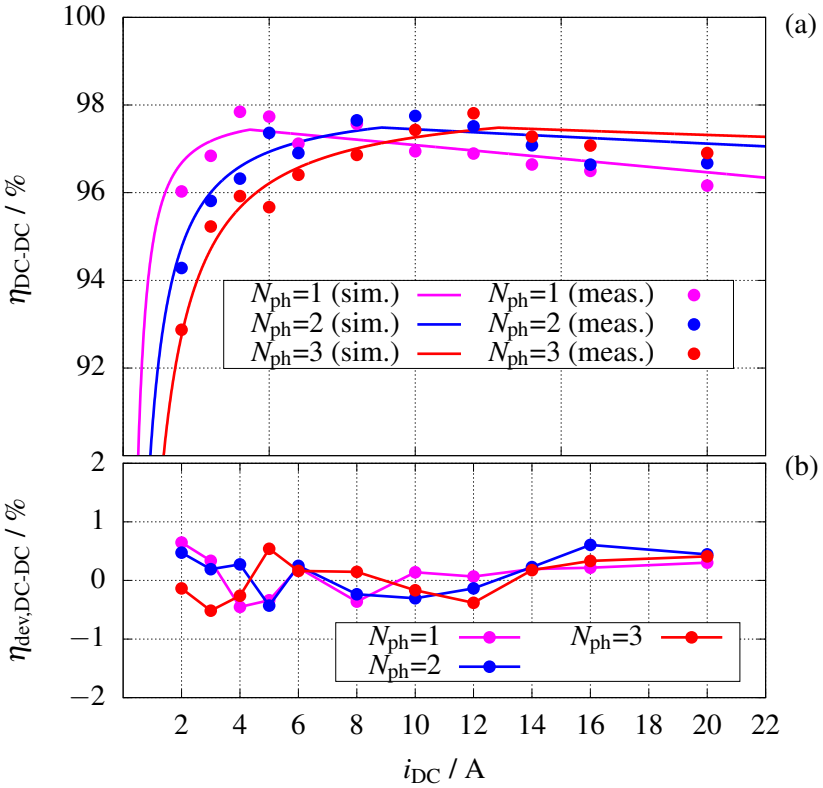

Figure 4.28: The measured efficiency of the converter for different load and the number of active phases ($u_{\text{Bat}} = 110$ V, $u_{\text{DC}} = 300$ V, and $f_{\text{sw}} = 10$ kHz) (a) simulated efficiency against measured efficiency (b) deviation between the simulation and measurement

in section 4.1, which indicate that the converter efficiency decreases by increasing the output voltage. This result also confirms the statement that at lower speeds of the inverter-fed machine, the DC-Link voltage should be set to the minimum required value to maximize the efficiency of the inverter.

In the last step, the effect of the number of active phases on the efficiency is measured and presented in figure 4.28. In this test case, the input and output voltage of the converter are fixed to 110 V and 300 V respectively. For that, the converter output load and N_{ph} are varying (the load from 600 W up to 6000 W and N_{ph}=1,2,3). Same as the previous test case, figure 4.28 present the simulation and measurement results together with the deviation between the two. According to this, as expected, at partial loads the maximum efficiency is achieved by activating only one phase of the interleaving converter. By further increase of the output output current the second and at the end the third phase should be activated for the efficiency optimization.

The measurement-based model verification confirms the process in developing the loss optimizing operating strategies of the DC-DC converter presented and discussed in the first part of this chapter. This leads us to the next chapter, where a complete electric vehicle drivetrain will be designed and sized, and the efficiency benefits of using a DC-DC converter in the drivetrain will be evaluated.

5 Dimensioning and Efficiency Analysis of the Alternative Drivetrain

In this chapter the efficiency of drivetrains with different battery voltages and topologies are compared with each other. After dimensioning the drivetrains with and without DC-DC converter extension (referred to as alternative drivetrain and reference drivetrain) at the beginning of this chapter, the models derived and presented in the previous chapters are used for the actual efficiency analysis. In addition, the operating strategies developed in chapter 4 will be employed in the drivetrain based on its topology, where applicable, to verify the benefits of using these operating strategies.

5.1 Drivetrain Dimensioning

The component selection of the aforementioned drivetrains, which are compared in this chapter, is presented below.

5.1.1 Vehicle

The first step in dimensioning a drivetrain is to select a specific vehicle, into which the drivetrain is to be integrated, and then characterize and model this vehicle from the mechanical point of view. The vehicle's equations of motion, together with the mechanical parameters, form a vehicle model that can be used to determine the torque and speed requirements of the electric motor used in the drivetrain for a given load profile. In this work a conventional compact class vehicle is used as the mechanical load on the motor. The modeling parameters of this prototype vehicle is shown in table 5.1.

When it comes to the mechanical modeling of the vehicle in terms of translational movement, the Newton's second law is applied. It states that the sum of all forces[1)] applied on an object (F_{Total}) is equal to the derivative of the object translational speed (v) multiplied by the mass of

[1)] The force can either be in positive direction and contribute to an acceleration, or in negative direction and makes a deceleration.

Table 5.1: Mechanical parameters of a compact-class prototype vehicle

Parameter	Designation	Value	Unit
Mass of the vehicle	m_{V}	1360	kg
Wheel radius	R_{W}	0.2811	m
Air density	ρ_{air}	1.25	kg/m^3
Drag coefficient	c_{d}	0.325	-
Rolling resistance coefficient	c_{r}	0.01	-
Front area	A_{V}	2.2	m^2
Gear ratio	G_{m}	6.54	-

the object (m_{Total}). Accordingly, equation 5.1 shows the acceleration force demand $F_{\mathrm{acc,W}}$ at the wheel in the translational coordinate system resulting form speed changes of the vehicle.

$$F_{\mathrm{acc,W}} = m_{\mathrm{Total}} \cdot \frac{dv}{dt} \tag{5.1}$$

In the simplified mechanical model of the vehicle developed here, in addition to the acceleration force $(F_{\mathrm{acc,W}})$, two other force components are included in the total force demand calculation at the vehicle's wheels ($F_{\mathrm{V,W}}$) to keep the vehicle moving with the desired speed. Namely, the force resulting from the air drag force ($F_{\mathrm{drag,W}}$), and the force resulting from the rolling resistance of the wheels ($F_{\mathrm{roll,W}}$). As shown in [102], with the help of mechanical parameters of the vehicle and its translational speed (v) the air drag force of the vehicle and rolling resistance of the wheels can be calculated on the wheel reference as shown in equations 5.2 and 5.3 respectively.

$$F_{\mathrm{drag,W}} = \frac{1}{2} \cdot c_{\mathrm{d}} \cdot A_{\mathrm{V}} \cdot \rho_{\mathrm{air}} \cdot v^2 \tag{5.2}$$

$$F_{\mathrm{roll,W}} = c_{\mathrm{r}} \cdot m_{\mathrm{V}} \cdot g \cdot v \tag{5.3}$$

By using equations 5.1 to 5.3 the required vehicle force on the wheel ($F_{\mathrm{V,W}}$) is calculated as follows:

$$F_{\mathrm{V,W}} = m_{\mathrm{V}} \cdot \frac{dv}{dt} + F_{\mathrm{drag,W}} + F_{\mathrm{roll,W}}. \tag{5.4}$$

In order to calculate the demanded torque of the motor, equation 5.4 should be transformed into the rotary system at the motor shaft. This means that the forces and translational speeds should be converted into torques and rotation speeds at the motor shaft respectively. As presented in [102], the conversion is done based on the wheel radius (R_{W}) and the gear ratio between the wheel and motor (G_{m}). The following equations show the relationship between these factors (x

is a placeholder for different force quantities).

$$v = R_{\mathrm{W}} \cdot \omega_{\mathrm{W}} \tag{5.5}$$
$$\omega_{\mathrm{m}} = G_{\mathrm{m}} \cdot \omega_{\mathrm{W}} \tag{5.6}$$
$$T_{\mathrm{x}} = R_{\mathrm{W}} \cdot F_{\mathrm{x}} \tag{5.7}$$
$$T_{\mathrm{x,W}} = G_{\mathrm{m}} \cdot T_{\mathrm{x,m}} \tag{5.8}$$

To perform the conversion described above, the transnational system (equation 5.4) is first converted to the rotary coordinate system at the wheel shaft using equations 5.5 and 5.7. The result is presented in the following equation, in which the moment of inertia of the vehicle including the wheels is shown with J_{V} and is equal to the product of the total mass and the square of wheel radius.

$$T_{\mathrm{V,W}} = J_{\mathrm{V}} \cdot \frac{d\omega_{\mathrm{W}}}{dt} + T_{\mathrm{drag,W}} + T_{\mathrm{roll,W}} \tag{5.9}$$

Finally, the above equation is converted from the rotary coordinate system at the wheel to the rotary system at the motor shaft using equations 5.6 and 5.8 as follows:

$$T_{\mathrm{V,m}} = J'_{\mathrm{V}} \cdot \frac{d\omega_{\mathrm{m}}}{dt} + T_{\mathrm{drag,m}} + T_{\mathrm{roll,m}}. \tag{5.10}$$

In the equation above, J'_{V} is the vehicle's moment of inertia reflected into motor shaft rotational system ($J'_{\mathrm{V}} = J_{\mathrm{V}}/G_{\mathrm{m}}^2$). Since all quantities are now in the motor shaft coordinate, the torque calculated in equation 5.10 is valid to be used as load torque (T_{L}) in the mechanical equation of the motor presented in section 2.4, equation 2.60. With that, for a given motor speed the required motor torque (T_{e}) is calculated as follows:

$$T_{\mathrm{e}} = (J'_{\mathrm{V}} + J_{\mathrm{R}}) \cdot \frac{d\omega_{\mathrm{m}}}{dt} + T_{\mathrm{drag,m}} + T_{\mathrm{roll,m}}. \tag{5.11}$$

5.1.2 Driving Cycle

After selecting the vehicle which will be used for the drivetrain simulation, the load profile (driving cycle) of the vehicle should be chosen. A common driving cycle used by many automakers to determine various specifications of their vehicles, such as the maximum range of an electric vehicle or the maximum emissions and fuel consumption of an internal combustion engine vehicle, is the **New European Driving Cycle** (NEDC) as stated in [103]. Figure 5.2 shows the vehicle velocity profile during NEDC. This driving cycle is 1180 s and 11 km long and consists of 4 identical city rides and one highway ride.

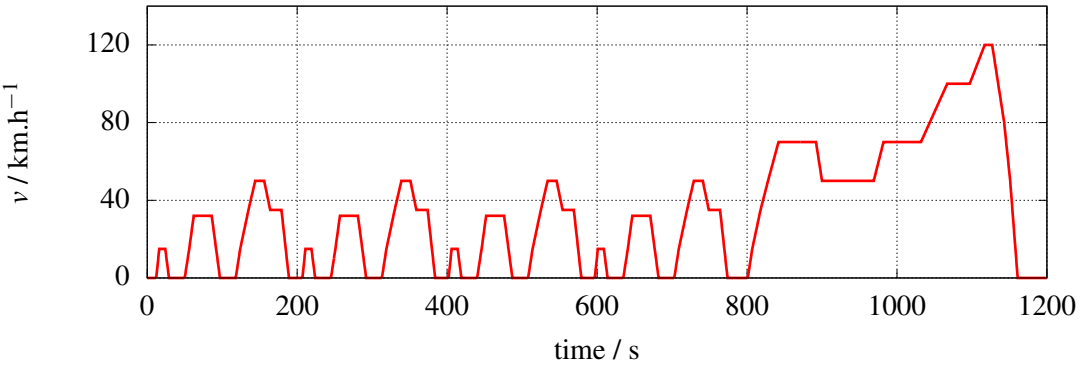

Figure 5.1: Speed profile of the New European Driving Cycle

In this work, the NEDC driving cycle described above is chosen as the speed set point of the vehicle during the driving period. This speed profile (figure 5.2) is then used in equations 5.5 and 5.6 to calculate the rotation speed of the electric motor (ω_m) at every operating point. The drag and rolling resistance torques for the vehicle on the motor shaft are then calculated using the speed profile and equations 5.2, 5.3, 5.7, and 5.8. Figure 5.2 shows the demanded speed, torque , and power of the electric motor during NEDC for the above mentioned prototype vehicle with the given gear ratio between motor shaft and wheel (G_m).

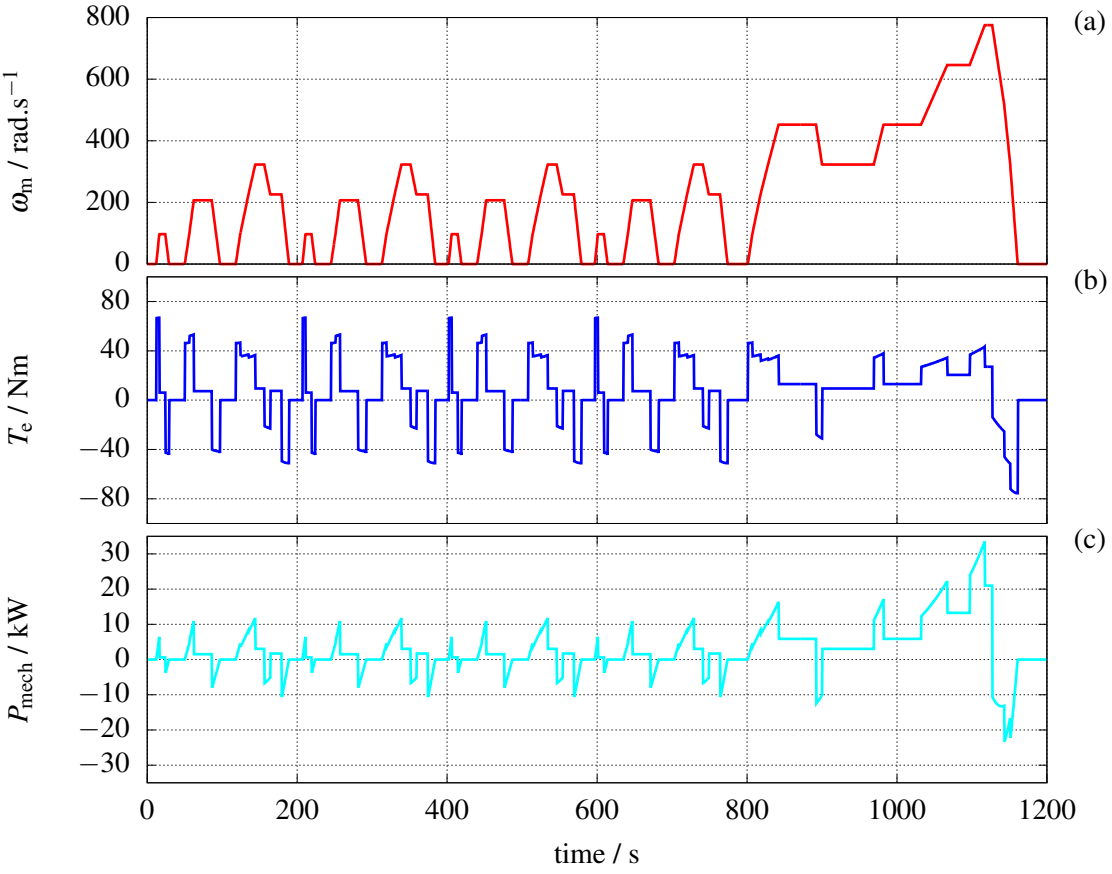

Figure 5.2: Required speed, torque, and power of the motor for the prototype vehicle during NEDC

5.1.3 Electric Motor

Based on the load profile on the motor shaft calculated in the previous subsection (figure 5.2), the electric motor requirements can be derived. Table 5.2 shows the absolute maximum as well as the root mean squares of the three main motor quantities (speed, torque, and power) during the NEDC driving cycle.

Table 5.2: Motor sizing quantities for the given vehicle, driving cycle, and gear ratio (absolute maximums and effective values during the driving cycle)

Quantity	Value	Unit
Maximum speed	775.17	$\mathrm{rad.s^{-1}}$
Effective value of speed	292.86	$\mathrm{rad.s^{-1}}$
Maximum torque	66.94	Nm
Effective value of torque	26.69	Nm
Maximum power	33.53	kW
Effect value of power	7.51	kW

Based on the entries of table 5.2, the induction motor introduced in the section 2.4 is a suitable choice for this application. The parameter set of this induction machine are presented in the table 2.6. This motor can provide a continuous output power of 30 kW with the rated speed (synchronous) and torque of 4560 rpm and 63.5 Nm respectively. In addition to that, the breakdown torque of the machine ($T_{\mathrm{e,bd}}$) is equal to 3.66 times of its nominal value, which corresponds to a short-time maximum power of 110 kW at the nominal motor speed.

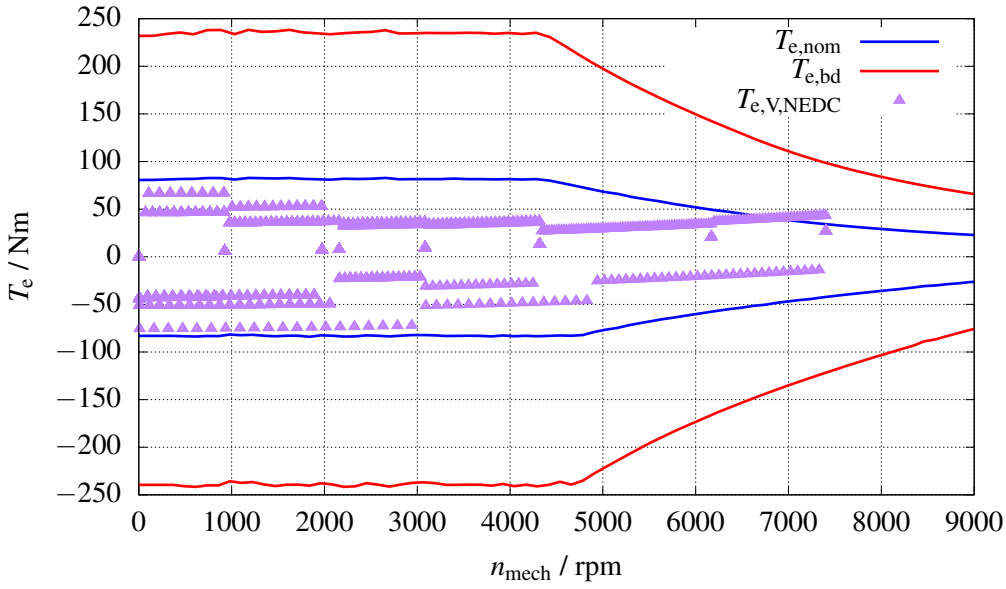

Figure 5.3: Speed-torque characteristic of the machine for two different maximum torques (nominal torque $T_{\mathrm{e,nom}}$, and breakdown torque $T_{\mathrm{e,bd}}$), as well as torque and speed demands of the vehicle at motor shaft $T_{\mathrm{e,V,NEDC}}$ for the selected gear ratio and during NEDC

Figure 5.3 shows the speed-torque characteristic of the machine for two different maximum torques, namely the nominal torque ($T_{e,nom}$) and the breakdown torque ($T_{e,bd}$). These characteristics are valid under the assumption that the machine is driven by a three-phase power supply with variable frequency and amplitude, where the maximum amplitude of the supply voltage is equal to the nominal voltage of the machine. Therefore, the field-weakening operating area of the machine, where the available maximum torque starts to decrease, first begins at the rated speed of the machine.

To evaluate if the selected motor meets the torque and speed requirements of the vehicle, the torque and speed demands of the vehicle at the motor shaft during NEDC (the data points are sampled every 0.5 seconds) are depicted in the same speed-torque map of figure 5.3. Based on this results, the selected machine perfectly covers the required operating range of the vehicle. To ensure that the machine is driven within its safe operating range, the maximum torque is limited to twice the value of the machine's rated torque (127 Nm, which corresponds to a peak power of 60 kW) to avoid reaching the breakdown torque of the machine. This will still provide sufficient torque reserve also during trips with higher accelerations.

5.1.4 Battery and DC-AC Converter

In the previous subsections the vehicle is selected, and based on the applied load profile (NEDC) the torque and speed requirements are calculated. Finally, the appropriate electric machine is chosen to meet the load requirements. In this subsection, the remaining components of the drivetrain (DC-AC converter and the battery) should be selected to finalize the dimensioning process. Table 5.3 shows the maximum value of various parameters at the output of the DC-AC converter (in other words, at the input of the machine), which are of relevance for sizing the converter.

Table 5.3: Maximum value of various parameters at the output of the DC-AC converter

Quantity	Designator	Value	Unit
Maximum output power	$P_{inv,out,max}$	60	kW
Maximum phase current (effective value)	$I_{s,i,max}$	110	A
Maximum line to line voltage (effective value)	$u_{LL,max}$	400	V
Maximum output fundamental frequency	$f_{1,max}$	202	Hz

The entries of the table above are the basis for the component selection of the converter. As already discussed in chapter 3 and shown in particular in figure 3.1, two different topologies are considered in this work for implementing the DC-AC power conversion. The first variant, which consists of a high-voltage battery and a 2-level inverter, is used in the drivetrain that is referred to as the reference drivetrain. The second DC-AC topology is used in the so-called alternative drivetrain, where a DC-DC converter is utilized between the battery pack (with a lower voltage compared to the reference drivetrain) and the 2-level inverter. In the following, the

component selection of the reference drivetrain and the alternative drivetrain are presented in detail. For this purpose the sub-components such as power transistors and passive components should be properly sized and selected to cover the entire machine's operating points (continuous and short-time) shown in figure 5.3.

5.1.4.1 Reference Drivetrain

Based on the maximum line to line voltage requirement of the machine (table 5.3) the voltage class of the power transistors used in the 2-level inverter can be determined using the equation 3.6. According to this equation, the minimum DC-Link voltage required to cover $u_{\mathrm{LL,max}}$ at the output of the inverter is calculated by setting the modulation index to its maximum value. The maximum modulation index depends on the modulation strategy used (section 3.1.2), and in the case of the SVM-based modulator this value is equal to $2/\sqrt{3}$, resulting in a minimum DC-Link voltage of $\sqrt{2}\cdot 400$ V. The voltage level of the battery pack is also selected equal to $\sqrt{2}\cdot 400$ V to match the minimum required DC-Link voltage. The battery is modeled in this work with an ideal voltage source and an internal resistance of 13 mΩ [104].

For the correct selection of the voltage class of the transistor used in the inverter, the impact of the parasitic inductances between the DC-Link capacitor and switching transistors should also be considered. The rapid drop of the transistor current during the turn-off process (Figure 2.24) leads to voltage drops across the parasitic inductors and accordingly voltage overshoots at the switching nodes. Therefore, an additional 20% blocking voltage headroom is included in the requirement of the transistor voltage class. This 678 V blocking voltage requirement combined with the maximum current requirement of table 5.3 lead to the selection of the following IGBT transistor for the inverter part of the drivetrain. This component from Infineon is available as an integrated module with three half-bridges inside (including anti-parallel diodes), mounted on a double side water-cooled heat-sink, as described in [11], to achieve the given thermal characteristics.

Table 5.4: Nominal electric ratings of the IGBT used in the inverter module (HybridPACK DSC L) of the reference drivetrain

Type	Product name	Voltage	Current
IGBT	*FS200R07A02E3*	700 V	200 A

The DC link capacitor is the last part of the reference drivetrain that should be selected. As discussed in [105] and section 2.1, the capacitor should be dimensioned in a way to both keep the input voltage ripple of the inverter at an acceptable level and to bypass the high frequency inverter input current ripple from the battery pack. Based on [7] the effective value of the

capacitor current ripple fundamental frequency $I_{C,1}$ is calculated using equation 5.12.

$$I_{C,1,inv} = I_s \cdot \sqrt{2 \cdot M \left[\frac{\sqrt{3}}{4\pi} + cos^2(\phi) \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16} \cdot M \right) \right]} \tag{5.12}$$

The above equation applies to an SVM-based modulator and shows the dependency of the capacitor current ripple on the rms value of the output phase current I_s, the inverter modulation index M, and the load power factor $cos\phi$. As discussed comprehensively in [7], the equation 5.12 can be evaluated for an induction machine load to estimate a worst-case current-stress across the DC link capacitor. The result of this estimation is shown in equation 5.13.

$$I_{C,1,inv} \simeq \frac{1}{2} \cdot I_s \tag{5.13}$$

Based on the equation 5.13 and the maximum phase current requirement of table 5.3, the capacitor to be selected should withstand an effective current value of 55 A. Another criteria for choosing the amount of capacitance is the maximum allowable voltage ripple over the capacitor at the input of the inverter. For the purpose of this drivetrain and based on the selected transistor voltage class on one side and the minimum DC-Link voltage requirement on the other, the amplitude of the voltage ripple on the capacitor should not exceed 22 V. The required capacitance can then be calculated using equation 5.14 [2)], and for the given switching frequency of the inverter (10 kHz).

$$C_{min,inv} = \frac{\tilde{i}_{C,1,inv,max}}{2\pi \cdot f_{sw} \cdot \tilde{u}_{C,max}} \tag{5.14}$$

Using the above equation, at an inverter switching frequency of 10 kHz, a minimum capacitance of 56 μF is required to meet the 22 V maximum voltage ripple requirement. To realize the maximum current ripple and the minimum capacitance requirements, a Metalized Polypropylene Film capacitor from TDK is used. The nominal values of this capacitor is shown in table 5.5.

Table 5.5: Nominal electric ratings of the reference drivetrain DC-Link capacitor

Type	Product name	Capacitance	Voltage	Current	Number in parallel	Total volume
MPPF	*B32678G1206K*	20 μF	750 V	28 A	3	301.8 cm^3

[2)] As presented in [105] as an estimation for inverter-fed motor application it is valid to only consider the first harmonic of the capacitor current for the voltage ripple calculation.

5.1.4.2 Alternative Drivetrain

In the alternative drivetrain of figure 3.1 the 2-level inverter design (power transistors and DC-Link capacitor) and its power, voltage, and current requirements are identical to the design of the reference drivetrain presented in the previous subsection. The first step in the sizing of the DC-DC converter extension is to determine the input voltage of the converter (battery voltage) based on the converter topology and the output voltage range. As it has been discussed in section 4.1 regarding the voltage dependency of the inverter losses, to take the most benefit of the power loss reduction at partial loads, the lower the DC-Link voltage, the more advantageous the developed operating strategy is (for the selected DC-DC converter topology presented in section 3.2 the battery voltage is the lowest value which can be set at the DC-Link). At the same time, the converter should provide enough voltage at the maximum speed operating points of the inverter-fed machine (according to subsection 5.1.4.1 this voltage is equal to $\sqrt{2} \cdot 400$ V). Therefore, by selecting a battery pack with the voltage rating of 110 V, on one side the DC-Link voltage can be kept as low as 110 V at partial loads, and on the other side the voltage gain of the converter at maximum output voltage operating points remains below an acceptable value of 5.1 (the upper limit of the duty cycle remains below 80% and provides sufficient reserve) [106]. As in the previous subsection, the battery pack is modeled with an ideal voltage supply and an internal resistance, which in this case is equal to 3 mΩ because of the lower voltage of the battery pack.

After determining the input voltage level and the output voltage range of the DC-DC converter, the maximum static current requirement should be evaluated for the given electromechanical system. Since the inverter is designed for a maximum output power of 60 kW, the 3-phase interleaving converter should also cover this amount of power [3)]. For the given output voltage, output power and battery voltage, various parameters of the DC-DC converter are calculated and presented in the table 5.6, which are important for sizing and component selection.

Table 5.6: Maximum value of various parameters of the internal DC-DC converter

Quantity	Designator	Value	Unit
Maximum output power	$P_{\mathrm{con,out,max}}$	60	kW
Maximum inductor phase current	$I_{\mathrm{L,i,max}}$	182	A
Maximum output current	$i_{\mathrm{DC,max}}$	106	A
Maximum output voltage	$u_{\mathrm{DC,max}}$	$\sqrt{2} \cdot 400$	V
Maximum battery voltage	$u_{\mathrm{bat,max}}$	110	V

According to the maximum voltage and current requirements of the interleaving DC-DC converter power transistors, the same components as for the inverter (table 5.4) can be used also for the 3-phase converter. The next step is to select the phase inductors. To calculate the required

[3)] The losses of the converter and inverter are not considered in the dimensioning process, since sufficient current reserves are taken into account in the selection of the power transistors and the passive components such as DC-Link capacitors and DC-DC converter phase inductors.

inductance of the coils, it is important to determine the maximum acceptable current ripple of the battery pack. According to [105], the current ripple of the battery should not exceed 10% of the battery current rating. To design the converter in such a way that no additional capacitor is needed at the input side, the mentioned current ripple requirement should be fulfilled with the help of a properly sized inductor.

In this work a maximum input current ripple of 30 A is determined as the converter design requirement, which corresponds to 5.5% of the maximum current rating of the battery. As it has been illustrated in figure 3.19, the total ripple of the input current (the sum of the three triangular phase-shifted inductor currents) decreases drastically in interleaving mode due to the switching time offsets of the converter phases. Nevertheless, because of the utilized operating strategy with variable active phases (section 4.2), the partial load operation of the machine at maximum rotation speed is used as the worst-case condition for the inductance calculation. In this operating mode, where the converter voltage gain is at its maximum and only one phase is activated (no interleaving advantage), the input current ripple of the converter is as its maximum.

For a DC-Link voltage equal to $\sqrt{2} \cdot 400$ V (corresponds to the maximum voltage gain of the converter with duty cycle (d_L) of 80%), N_{ph} of 1, and switching frequency of 10 kHz[4)], the required phase inductance of the converter for keeping the input current ripple in the range (30 A) is calculated using equation 3.46. Accordingly, the resulting inductance value is equal to 295 μH, which is rounded up to 300 μH for this design. In order to realize an inductor with the given specification, the proper winding and magnetic core should be selected. This is done based on the maximum current of the winding and the peak magnetic flux density of the core. By referring to table 5.6 the maximum DC current bias of the inductor is equal to 182 A. For this current rating, the proper magnetic core and the required number of turns of the winding can be selected to achieve the desired inductance.

For this application, the so-called High-Flux magnetic core series from MAGNETICS is chosen. As discussed in [107], these type of cores are made of an iron-powder material to optimize the core losses and at the same time provide high saturation flux density (twice as much as MPP and three times higher than ferrite core materials). Table 5.7 shows the detailed specification of the selected core. Using the DC-bias curve of the core shown in [108], the inductance factor A_L is extracted for the maximum dc current of 182 A and the number of turns of 68. Using the derived inductance factor of 32.5 nH/T^2, the resulting inductance at the maximum current operating point is equal to 150.2 μH. This means that in order to achieve the desired inductance (300 μH) for each phase of the converter, two cores are used and the selected winding package is wound on the cores with the specified number of turns.

To verify that the core flux density during the maximum current operating point still remains below the saturation level of the core (for MAGNETICS high-flux cores this is 1 T), the equation 5.15 and the B-H curve of the magnetic core are used. Accordingly, the core flux density is

[4)] The designed converter can work with a variable frequency between 5 kHz and 10 kHz, but according to the variable switching frequency operating strategy (section 4.4), the maximum switching frequency will automatically be selected during partial loads since only one of the phases is activated.

calculated at the maximum current operating point and is equal to 0.54 T.

$$H_{\max} = \frac{N}{l_{\mathrm{mag}}} \cdot (I_{\mathrm{L,i,max}} + \frac{\Delta i_{\mathrm{L}}}{2}) \tag{5.15}$$

Table 5.7: Core specification (MAGNETICS *58164A2*) of the inductor used in the alternative drivetrain

Description	Designator	Value	Unit
Relative permeability	μ_{r}	14	1
Outer diameter	D_{out}	165.10	mm
Inner diameter	D_{inn}	102.41	mm
Height	h_{core}	31.75	mm
First steinmetz constant	a_{st}	968.54	1
Second steinmetz constant	b_{st}	2.218	1
Third steinmetz constant	c_{st}	1.189	1
Average magnetic path length	l_{mag}	412	mm
Core volume	V_{core}	407	cm^3
Weight	m_{core}	2.4	kg

For the core winding package, a copper wire with cross-section of 8.25 mm is chosen (AWG gauge of 0), which results in an acceptable maximum current density of the copper equal to 3.45 $\mathrm{A/mm}^2$[5)]. Specially with respect to the fact that the winding factor of the core is equal to 44.1% for the given inner diameter of the selected core and the given number of turns, which provides a relatively good cooling condition as discussed in [56]. The specification of the winding package is shown in table 5.8.

Table 5.8: The winding specification of the inductor used in the DC-DC converter of the alternative drivetrain

Description	Designator	Value	Unit
Copper diameter	d_{cu}	8.25	mm
Copper area	A_{cu}	53.4	mm^2
Number of turns	N	68	
Winding length per turn	l_{win}	192	mm
Total winding weight	m_{win}	7.4	kg

Selecting the proper input and output DC capacitors are the final steps in the dimensioning process of the alternative drivetrain. On the input side of the converter, no additional capacitor is

[5)] The current density is calculated for the DC component of the inductor current. As presented in section 2.2.1, the AC copper losses are all included in the losses calculation model. However, these losses can be neglected for dimensioning purposes when selecting the copper diameter, since the resulting AC copper losses are less than 2.5% of the total copper losses (the skin depth is equal to 0.6 mm for 10 kHz switching frequency and the AC losses is calculated using equation 2.27 for the selected copper diameter and resistance).

required in parallel with the battery, since the current ripple is already kept within the maximum limit of the battery pack by correctly dimensioning the inductors and taking advantage of the interleaving operation (the 5% ripple of the rated battery current is acceptable as in [105]).

On the output side of the converter, which is actually the DC-Link rail of the drivetrain[6)], the same statements that have been used for sizing the inverter input capacitor apply (subsection 5.1.4.1). This means that first the RMS value of the capacitor current should be calculated, and on this basis the correct capacitor with the minimum required capacitance should be selected to meet the requirement of the maximum DC-Link voltage ripple. Figure 5.4 shows the converter output capacitor current waveform for a given operating point with a fixed duty cycle (output voltage) and output current if only one phase of the converter is activated.

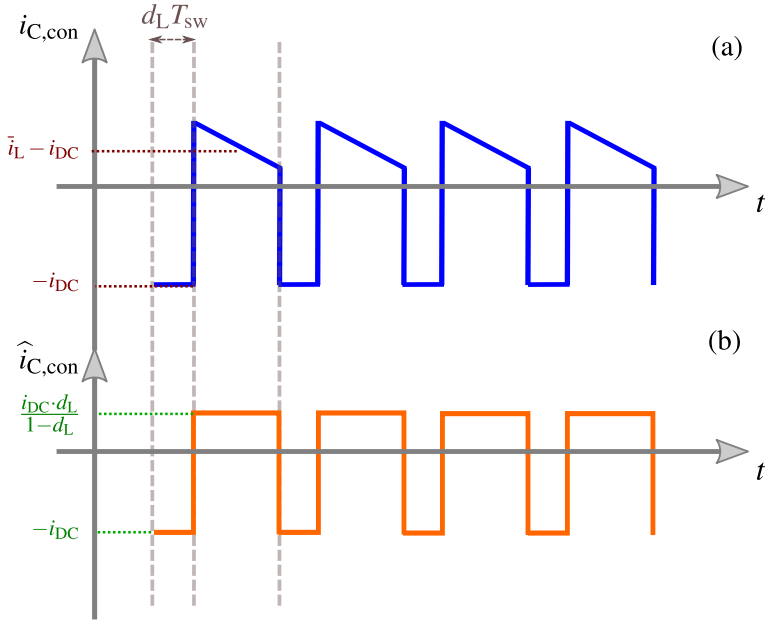

Figure 5.4: DC-DC converter output capacitor current ripple for 1 active phase (a) exact value (b) estimated value

The above operation is generalized for up to three interleaving phases, and the effective value of the capacitor current ripple normalized to i_{DC} is calculated for different duty cycles up to 0.8, which corresponds to the operating point with the maximum voltage gain of the converter. Figure 5.5 shows the overview of the normalized capacitor current ripple for different number of active phases. Based on these results, regardless of N_{ph}, the maximum capacitor current ripple is always happening at the maximum voltage gain of the converter. Another interpretation from figure 5.5 is that at a given output current, the interleaving operation with higher N_{ph} not only reduces the maximum capacitor current ripple, but also drastically reduces the resulting capacitor voltage ripple according to equation 5.14 (doubling and tripling the capacitor current frequency in the case of $N_{ph} = 2$ and $N_{ph} = 3$ respectively).

[6)] It is worth mentioning that according to section 2.1, and for the worst-case operating condition, the sum of AC current components at the input of the inverter and at the output of the converter will flow in the DC-Link capacitor. This means that in addition to the capacitors selected for the input of the inverter, further capacitors are required to compensate the additional voltage fluctuations at the output of the DC-DC converter.

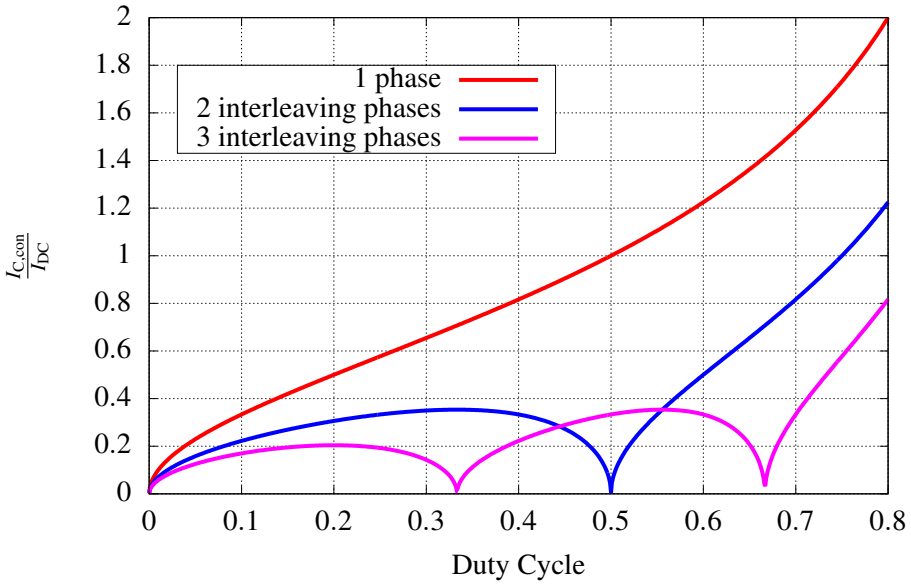

Figure 5.5: Normalized effective value of the capacitor current at the output of the interleaving DC-DC converter with variable number of active phases

To derive the worst-case condition in terms of capacitor current ripple and resulting voltage ripple, the operating strategies with the variable number of active phases and the variable switching frequency (section 4.2 and section 4.4) should be taken into account. Since the capacitor current ripple is directly related to the output current of the converter, and the current ripple value increases with voltage gain of the converter, the operating point with the maximum DC-Link voltage ($\sqrt{2} \cdot 400$ V) and current (106 A) is considered as the worst-case operating condition[7]. According to figure 4.7 and the LUT implemented in figure 4.14, at this operating point N_{ph} is equal to 3 and the switching frequency is equal to 5 kHz. For this operating point, and by using figure 5.5, the effective value of DC-Link current ripple is calculated and is equal to 81.2 A. Finally with the help of equation 5.16 and with respect to the fact that the maximum acceptable voltage ripple amplitude should be equal to 4% of the DC-Link voltage (22 V), the minimum required DC-DC converter output capacitance is calculated and is equal to 55 μF.

$$C_{min,con} = \frac{\tilde{i}_{C,1,con,max}}{2\pi \cdot N_{ph} \cdot f_{sw} \cdot \tilde{u}_{C,max}} \tag{5.16}$$

Accordingly, the required capacitance at the DC-Link (converter output and inverter input) is equal to 111 μF, and the capacitor bank should withstand a maximum current ripple of 136.2 A. Table 5.9 shows the specification of this capacitor bank. After designing both drivetrains, an efficiency comparison between the two is presented in the following section.

[7] As shown in figure 4.7, during the partial load condition the converter operates with a lower number of active phases, which could result in a higher output capacitor current ripple. However, since on the one hand the maximum output current at these operating conditions is far below the assumed worst-case value of 106 A and on the other hand these partial load maximum currents are only present at lower voltage gain of the converter (figure 4.2), the resulting capacitor current ripple at partial load remains below this value at full load.

Table 5.9: Nominal electric ratings of the reference drivetrain DC-Link capacitor

Type	Product name	Capacitance	Voltage	Current	Number in parallel	Total volume
MPPF	*B32678G1206K*	20 μF	750 V	28 A	6	603.6 cm^3

5.2 Efficiency Analysis Between Drivetrains

After dimensioning the reference drivetrain as well as the alternative drivetrain, in this section these two drivetrain topologies are compared with each other in terms of efficiency and energy losses. In this context, the developed loss optimizing operating strategies of the alternative drivetrain are quantitatively evaluated. For this comparison, the respective vehicle and driving cycle as well as the electric motor presented in section 5.1 are used and, in particular, the losses of the DC-AC converter part of both drivetrain variants are compared [8)]. Using the comparison results, the possible advantages or disadvantages of the alternative drivetrain against the reference drivetrain are presented and discussed.

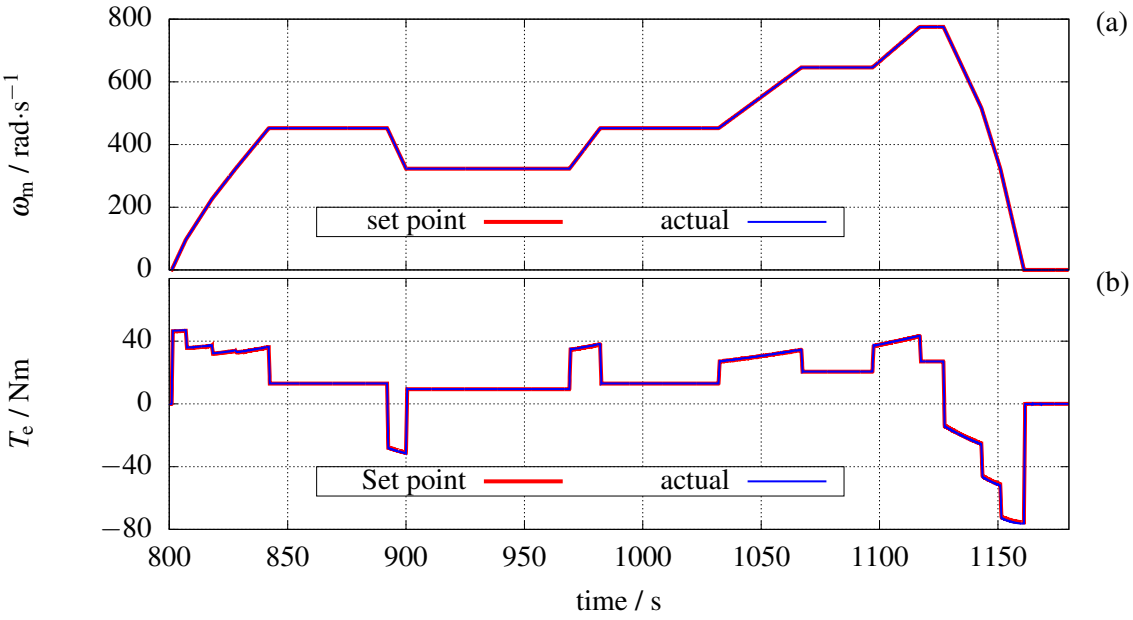

Figure 5.6: Motor (a) speed (b) and torque during NEDC highway ride for the reference drivetrain to evaluate the dynamic behavior of the drivetrain

As mentioned above, a real world mechanical load on the drivetrain is required for the efficiency comparison. Regarding this, for the given vehicle and driving cycle, the resulting mechanical

[8)] The reason for focusing on the DC-AC converter losses instead of drivetrain losses is because of the lack of an iron losses model of the induction machine, which includes the dependency of these losses on the inverter modulation index. As it will be discussed at the end of this chapter, according to the literature, using a higher inverter modulation index results in lower machine iron losses. This argues in favor of the alternative drivetrain where the DC-Link voltage can be adjusted to reach the maximum modulation index of the inverter and optimize the machine iron losses.

load characteristics are all implemented in the form of look-up-tables that are used as the motor torque and motor speed set point in the drivetrain plant model and the inverter control system (input of the speed controller) respectively, as shown in figure 4.1.

In the first step the NEDC speed and torque are applied to the reference drivetrain with a constant input voltage. In order to evaluate the dynamic behavior of the drivetrain the entire NEDC is simulated and the set points are compared with the actual values. Figure 5.6 shows the set point and actual values of the motor speed and torque during the highway ride of the NEDC, which represent the most torque and speed demanding operating points of the machine (figure 5.2). It can be seen that the set points are perfectly tracked by the actual values. This is also the case for the operating points during city ride as shown in figure 5.7. Due to the perfect match between the set point and the actual value, in the following figures only the actual values of various quantities of the drivetrain are shown.

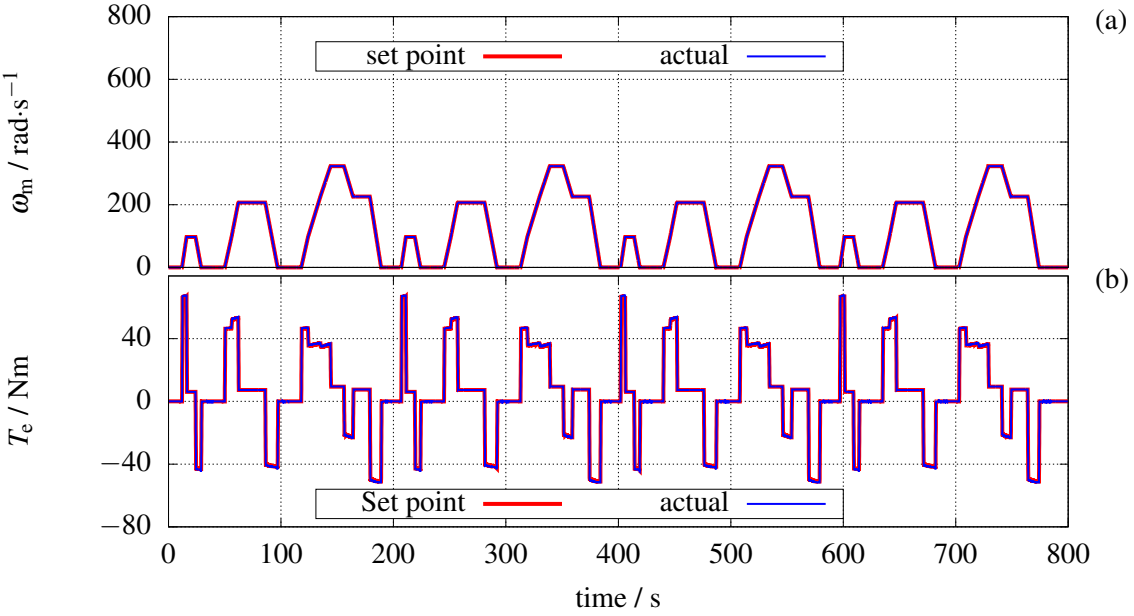

Figure 5.7: Motor (a) speed and (b) torque during NEDC city ride for the reference drivetrain to evaluate the dynamic behavior of the drivetrain

For the entire driving cycle the actual value of the induction motor rotation speed is shown in figure 5.8 (a), and it is clear that every operating point during NEDC is seamlessly drivable with the reference drivetrain. Figure 5.8 (b) shows the magnetizing current of the motor, which indicates the field-weakening operation during the highway rides and at the point where the speed becomes larger than 455 rad.s^{-1}. This value corresponds to the rated synchronous speed of the induction machine presented in table 2.6. The torque producing component of the stator current ($i_{s,q}$) is shown in figure 5.8 (c), and by comparing this waveform with the required torque of the vehicle shown in figure 5.2 (b) the correlation is distinguishable.The inverter IGBT temperature during NEDC is presented in figure 5.8 (d), and the last two waveforms of the figure 5.8 are presenting the produced mechanical output power of the drivetrain (figure 5.8 (e)) and power losses of the DC-AC converter part of the reference drivetrain (figure 5.8 (f)). The power losses calculation of the reference drivetrain DC-AC converter (equation 5.17) includes

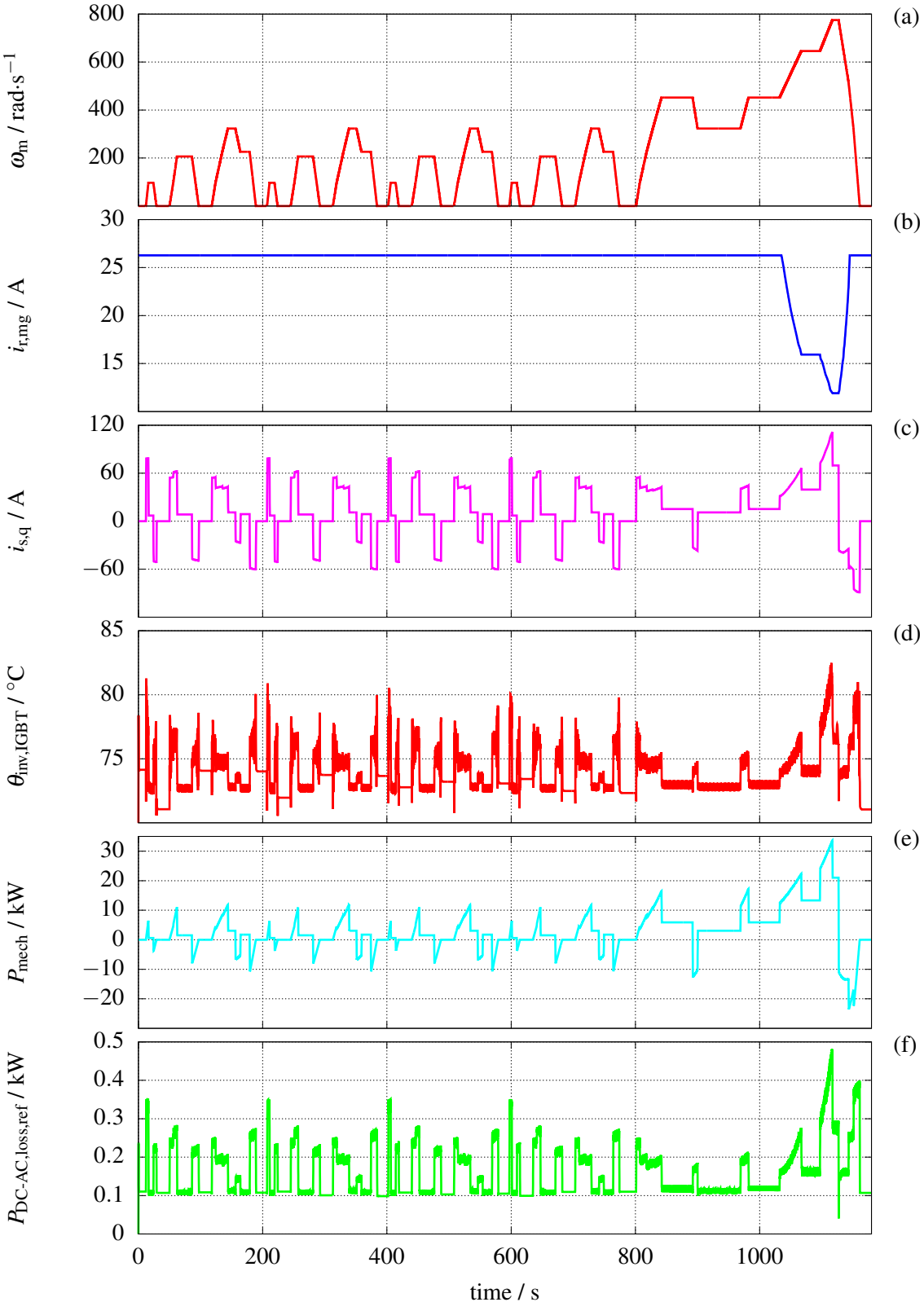

Figure 5.8: Actual value of various quantities for the reference drivetrain during NEDC ($u_{Bat} = u_{DC} = \sqrt{2} \cdot 400$) (a) rotation speed (b) rotor magnetizing current (c) torque producing component of the stator current (q-axis stator current) (d) IGBT junction temperature in inverter ($\theta_{hs} = 70\ °C$) (e) drivetrain mechanical output power (f) DC-AC converter power losses

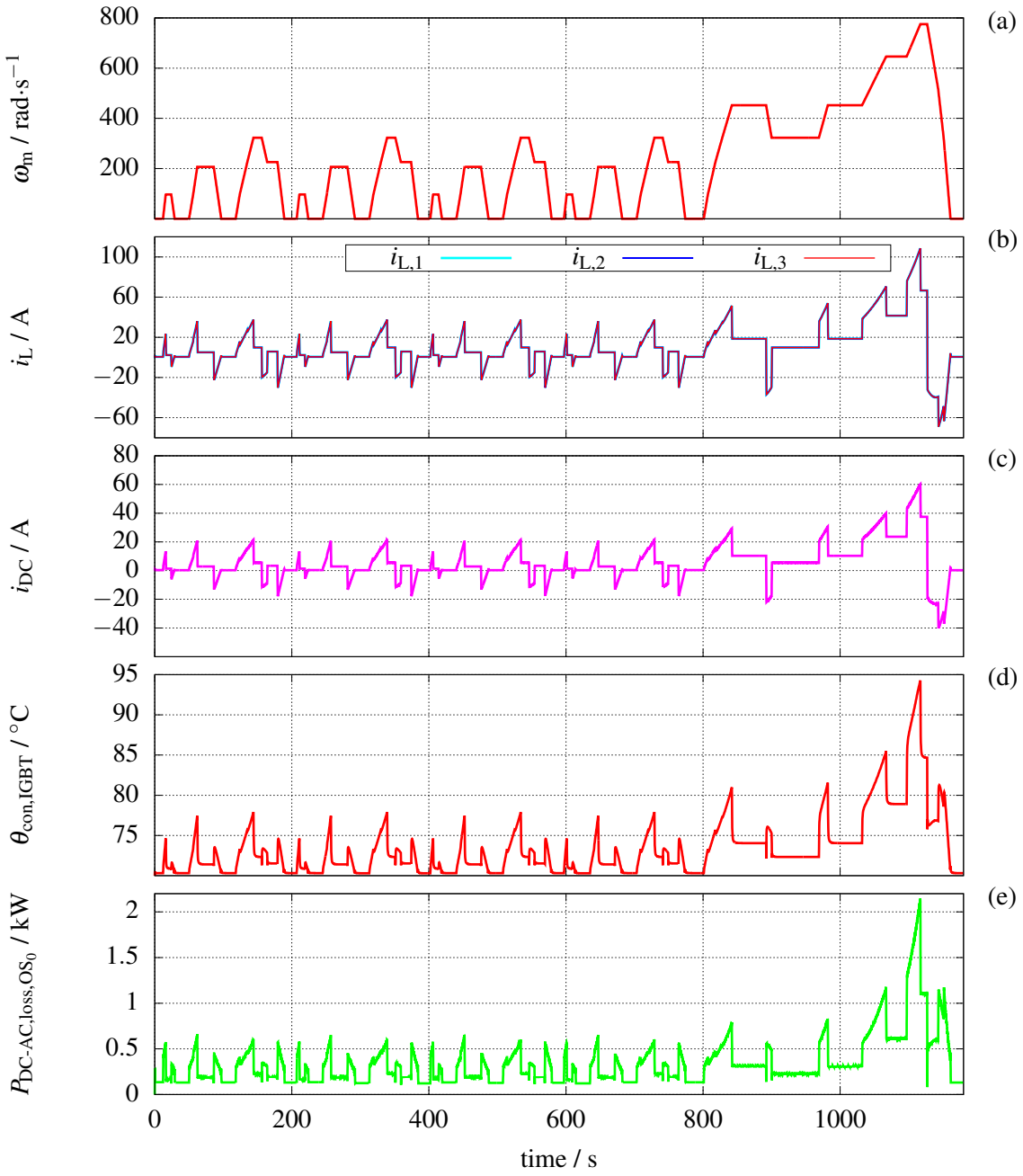

Figure 5.9: Actual value of various quantities of the alternative drivetrain during NEDC without activating any operating strategy ($u_{DC} = \sqrt{2} \cdot 400$, $N_{ph} = 3$, and $f_{sw} = 10$ kHz) (a) rotation speed (b) inductor currents (c) DC-Link current (d) IGBT junction temperature in converter (θ_{hs} = 70 °C) (e) DC-AC converter power losses

the following parameters: the inverter losses (switching losses and conduction losses of the half-bridges) and the DC-Link capacitor losses, all of which are discussed in detail in chapters 2 and 3.

$$P_{DC-AC,loss,ref} = P_{inv,loss} + P_{C,loss} \tag{5.17}$$

After evaluating the reference drivetrain in terms of dynamic behavior and power losses, the 3-phase interleaving DC-DC converter is added to drivetrain and the control system is extended to include the converter with an input voltage (u_{Bat}) of 110 V (figure 4.1). In the first step the DC-Link voltage set point is regulated to the same value as the battery voltage in the reference drivetrain ($u_{\mathrm{DC}} = \sqrt{2} \cdot 400$ V), and all of the loss optimizing operating strategies developed and presented in chapter 4 stay deactivated. The simulation results are presented in figure 5.9. According to the resulting motor speed shown in figure 5.9 (a), all operating points of the induction machine during NEDC are perfectly drivable using the drivetrain with a DC-DC converter and the lower battery voltage. Figure 5.9 (b) shows the inductor currents of the DC-DC converter phases during NEDC. The resulting output current of the DC-DC converter (DC-Link current) is shown in figure 5.9 as well. Since the inverter quantities, such as d-current and q-current components, are identical to the values of the reference drivetrain (figure 5.8), they are not presented again, but the converter's IGBT temperature with the heat-sink temperature of 70 °C is depicted in figure 5.9 (d).

Finally the DC-AC converter losses of the alternative drivetrain during NEDC are calculated and shown in figure 5.9 (e). These losses include inter alia, the losses of the inductors which are comprehensively presented in section 2.2. Equation 5.18 shows all power loss components of the DC-AC converter of the alternative drivetrain, which include the following parts: DC-DC converter power losses, inductor power losses, inverter losses, DC-Link capacitor losses, all of which are discussed in detail in chapters 2 and 3.

$$P_{\mathrm{DC-AC,loss,OS_n}} = P_{\mathrm{con,loss}} + P_{\mathrm{L,loss}} + P_{\mathrm{inv,loss}} + P_{\mathrm{C,loss}} \tag{5.18}$$

In the equation above, $\mathrm{OS_n}$ indicates the alternative drivetrain and the number of activated loss optimizing operating strategies of the DC-DC converter, which are presented in chapter 4 and summarized in the table 5.10.

Table 5.10: Operating strategy designators of the DC-DC converter in the alternative drivetrain

Designator	Description
$\mathrm{OS_0}$	No operating strategy is activated ($u_{\mathrm{DC}} = \sqrt{2} \cdot 400$, $N_{\mathrm{ph}} = 3$, and $f_{\mathrm{sw}} = 10$ kHz)
$\mathrm{OS_1}$	Activating the variable DC-Link voltage
$\mathrm{OS_2}$	$\mathrm{OS_1}$ + Variable number of active phases
$\mathrm{OS_3}$	$\mathrm{OS_2}$ + Passive mode
$\mathrm{OS_4}$	$\mathrm{OS_3}$ + Variable switching frequency (5 kHz ... 10 kHz)

The first activated operating strategy is the variable DC-Link voltage presented in section 4.1. It should be noted that the induction machine torque and speed values are not affected by the DC-Link voltage variation and they look the same as the waveforms shown in figure 5.2 (this

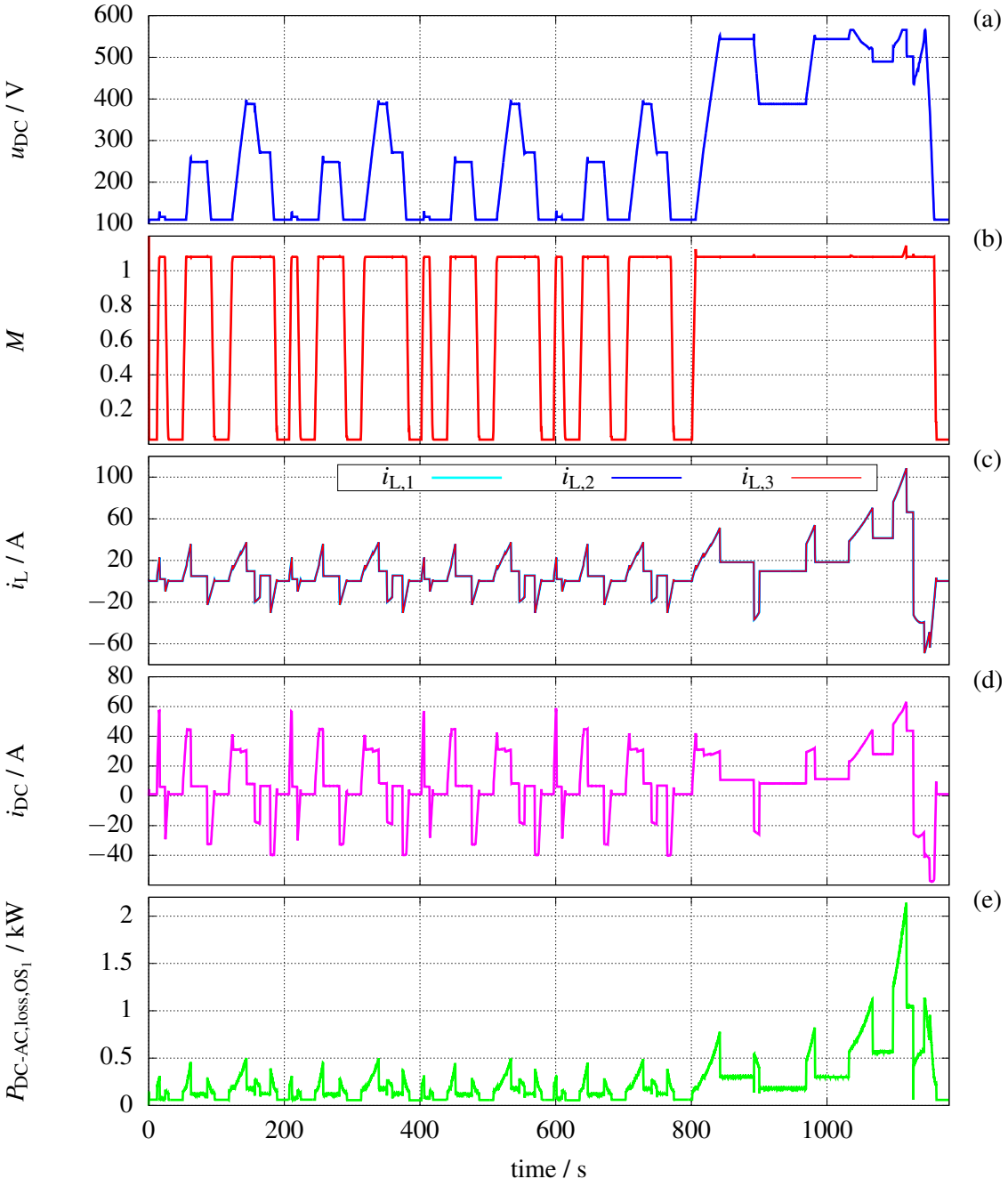

Figure 5.10: Various quantities of the alternative drivetrain during NEDC with activated variable DC-Link voltage operating strategy ($N_{ph} = 3$, and $f_{sw} = 10$ kHz) (a) DC-Link voltage (b) inverter modulation index (c) inductor currents (d) DC-Link current (e) DC-AC converter power losses

does apply to all of the following operating strategies, therefore the motor speed and torque waveforms will not be presented over and over again for every operating strategies). Figure 5.10 (a) shows the DC-Link voltage variation during NEDC, and as expected, there is a correlation between the motor speed and DC-Link voltage. In other words, this operating strategy is to adjust the DC-Link voltage to the lowest possible value required to provide sufficient voltage to

the motor at every operating point.

Using this operating strategy results in utilizing the inverter in an operating region with the maximum modulation index (according to equation 4.1 is equal to $2/\sqrt{3}$) during the time intervals that the speed set point is not zero (figure 5.10 (b)). Accordingly, the DC link voltage is set to lower values (240 V, or 374 V) while driving in the city, and is boosted to the values above 550 V during the highway rides. In the latter case, this voltage is required (equation 3.6 and table 2.6) to maintain an inverter output voltage close to the motor nominal voltage. The DC-DC converter inductor currents after activating OS_1 are presented in figure 5.10 (c), which because of the same battery voltage as before are very similar to the currents of figure 5.9 (b) with a constant DC-Link voltage. This does not apply to the DC-Link current, which is shown in figure 5.10 (d) and differs from the current waveform of figure 5.9 (c). This is because of the fact that the output power of the inverter remains the same as in OS_0, but the DC-Link current becomes higher for the lower DC-Link voltages shown in 5.10 (a). Finally the entire power losses of the drivetrain ($P_{DC-AC,loss,OS_1}$) are calculated and presented in figure 5.10 (e). A comparison between power losses (energy losses) will be presented at the end of this section.

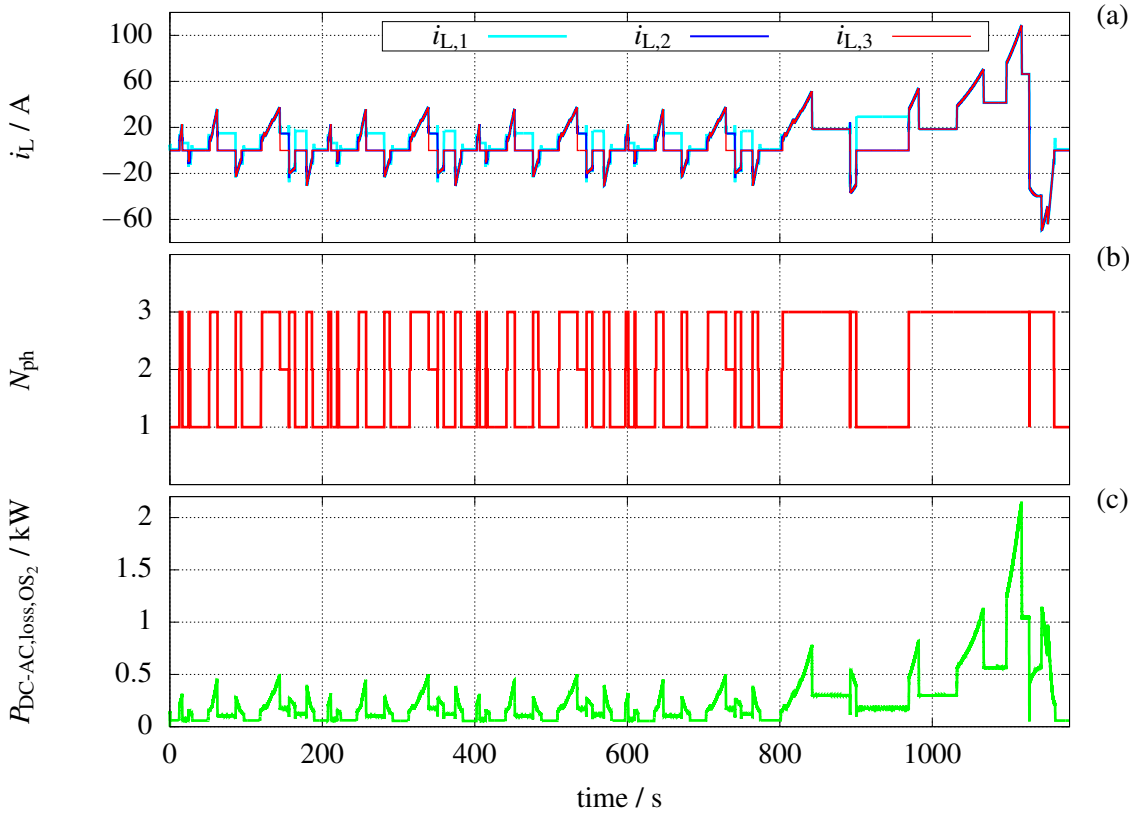

Figure 5.11: Various quantities of the alternative drivetrain during NEDC with activated variable DC-Link voltage and variable number of active phases operating strategies ($f_{sw} = 10$ kHz) (a) inductor currents (b) number of active phases (c) drivetrain power losses

The next activated loss optimizing operating strategy is the variable number of active phases presented in section 4.2. As already discussed, with the help of this operating strategy and based on the output voltage and output current of the converter the proper number of active phases is

determined to minimize the power losses. Figure 5.11 (a) and (b) show the current distribution between the inductors and the actual number of phases respectively. Based on the results it can be seen that during city rides the phases are toggle more frequently, and during highway ride the converter runs with full three active phases most of the time. Power losses of the the drivetrain after activating this operating strategy are shown in figure 5.11 (c).

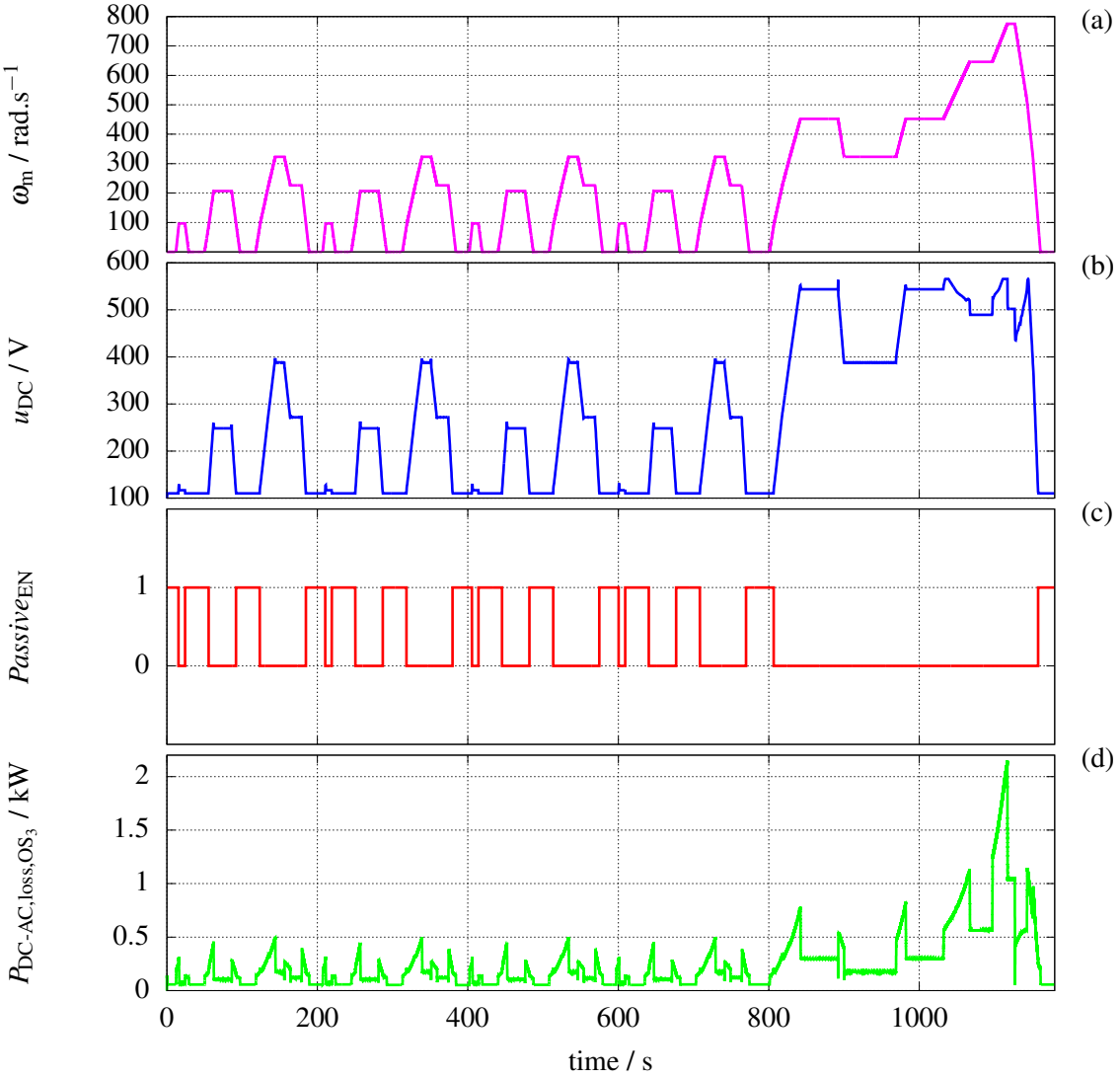

Figure 5.12: Various quantities of the alternative drivetrain during NEDC with activated variable DC-Link voltage, variable number of active phases, and passive mode operating strategies ($f_{sw} = 10$ kHz) (a) motor rotational speed (b) DC-Link voltage (c) passive mode enable signal (d) drivetrain power losses

The next operating strategy is the passive mode. As presented in section 4.3 the idea here is to disable the switching of the power transistors if the desired DC-Link voltage resulting from OS_1 is below the battery voltage. First of all to double check if the machine operates as expected after activating the aforementioned operating strategies, the motor speed is presented in figure 5.12 (a). Other than that, figure 5.12 (b) and (c) show the DC-Link voltage as well as the passive mode enable signal respectively. As expected the passive mode is activated at low rotation

speeds of the motor (figure 5.12 (a)), which correspond to lower DC-Link voltages. During the time that the passive mode is enabled the three high-side switches are in switch-on state, and the DC-Link voltage is in the range of the battery voltage (in this case 110 V). The power losses of the drivetrain after including this new operating strategy are presented in figure 5.12 (d).

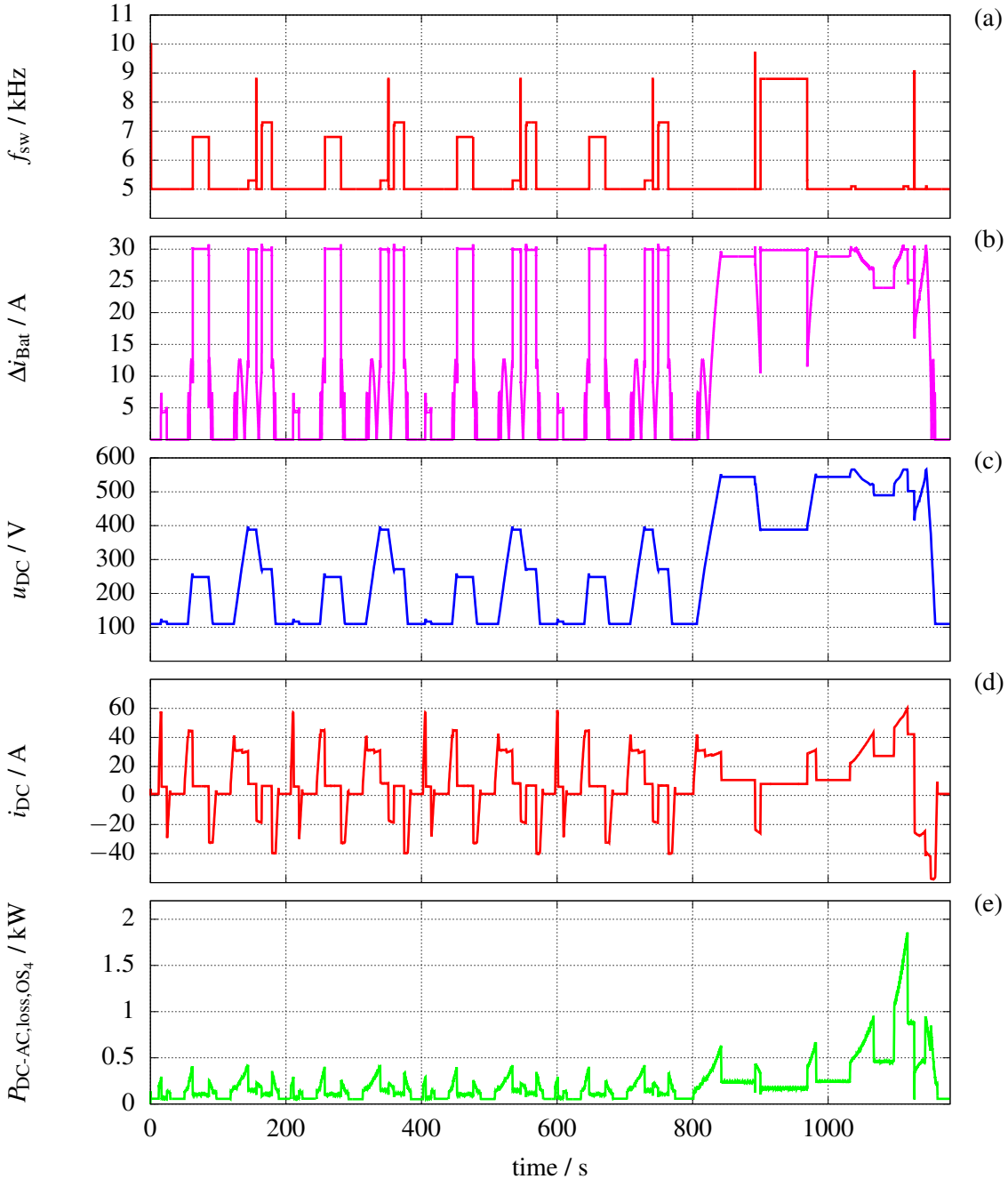

Figure 5.13: Various quantities of the alternative drivetrain during NEDC with activated variable DC-Link voltage, variable number of active phases, passive mode, and variable switching frequency operating strategies (a) switching frequency (b) input current ripple of the DC-DC converter (c) DC-Link voltage (d) drivetrain power losses

The last activated operating strategy is the variable switching frequency which is introduced in section 4.4. The result of this operating strategy is presented in figure 5.13. In order to optimize the converter losses, this operating strategy reduces the switching frequency as much as possible so that, on the one hand, the input current ripple of the DC-DC converter does not exceed the maximum limit of the battery and, on the other hand, the converter still exhibits good dynamic regulation. The optimum frequency in terms of power losses is calculated based on the DC-Link voltage and the number of active phases (interleaving operation for $N_{\mathrm{ph}} \geq 2$).

As discussed in section 5.1.4.2 the maximum acceptable current ripple at the input of the converter is equal to 30 A (approximately 5% of the rating DC current of the battery). On the other hand, the lowest switching frequency of converter is set to 5 kHz to maintain a proper dynamic performance, and provide an stable DC-Link voltage over the entire operating range. Accordingly the switching frequency range is selected to be between 5 kHz and 10 kHz and the desired maximum current ripple is set to 30 A. Figure 5.13 (a) shows the switching frequency variation during NEDC and the corresponding battery current ripple is shown in figure 5.13 (b) which remains always below 30 A. According to figure 5.13 (c) and (d) the output voltage and current of the converter are regulated perfectly, even at lower switching frequencies. Looking at these two figures together with the figure 5.11 (b), which represents the number of active phases, it can be seen that the more the operating point of the inverter is shifted towards higher DC-Link voltages and lower DC-Link currents (resulting in a lower number of active phases and lower effectiveness of interleaving operation), the higher the required switching frequency set point. This result is expected and can be concluded from equation 4.4. Finally, figure 5.13 (e) shows the power losses of the DC-AC converter after activating all operating strategies.

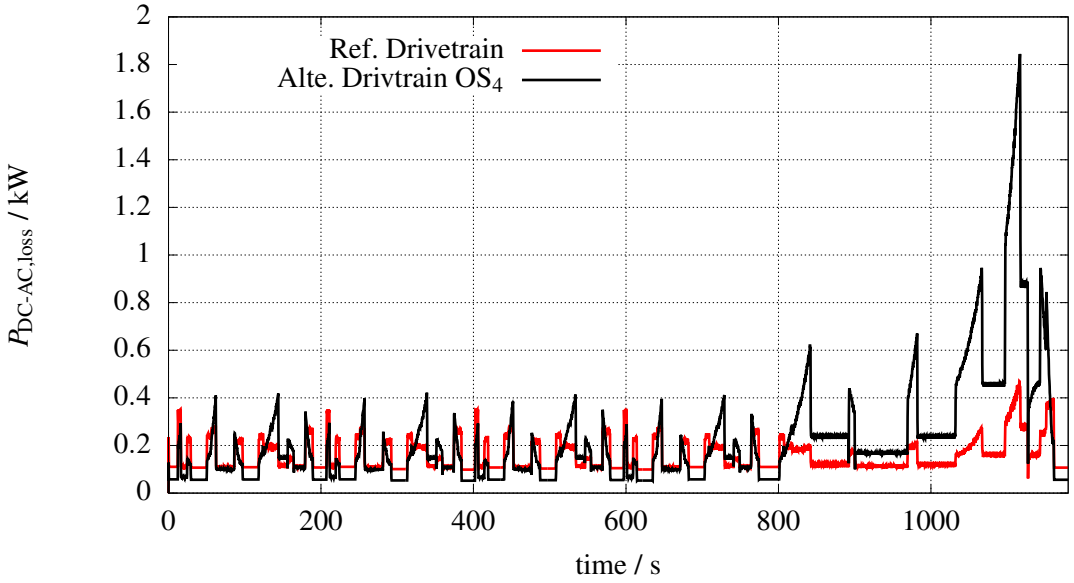

Figure 5.14: AC-DC converter power losses during NEDC for the conventional drivetrain and the alternative drivetrain after activating different operating strategies of table 5.10

Figure 5.14 shows the DC-AC converter power losses of the reference drivetrain along with the alternative drivetrain after activating all loss optimizing operating strategies. This provides an overview of the effect of adding the DC-DC converter to the drivetrain in terms of power losses.

Based on this result it is observable that the use of alternative drivetrain leads to lower power losses at partial loads (lower speed and torque). These are actually the vehicle operating points during the city rides, which are placed in the first 800 seconds of the NEDC.

To facilitate a quantitative comparison between the drivetrains, in this step energy losses of the DC-AC converter part in both the reference drivetrain and the alternative drivetrain during the NEDC are calculated and compared with each other. Figure 5.15 shows the normalized energy losses of the mentioned drivetrains. For the alternative drivetrain, the energy losses are presented stepwise and after activation of each of the loss optimizing operating strategies.

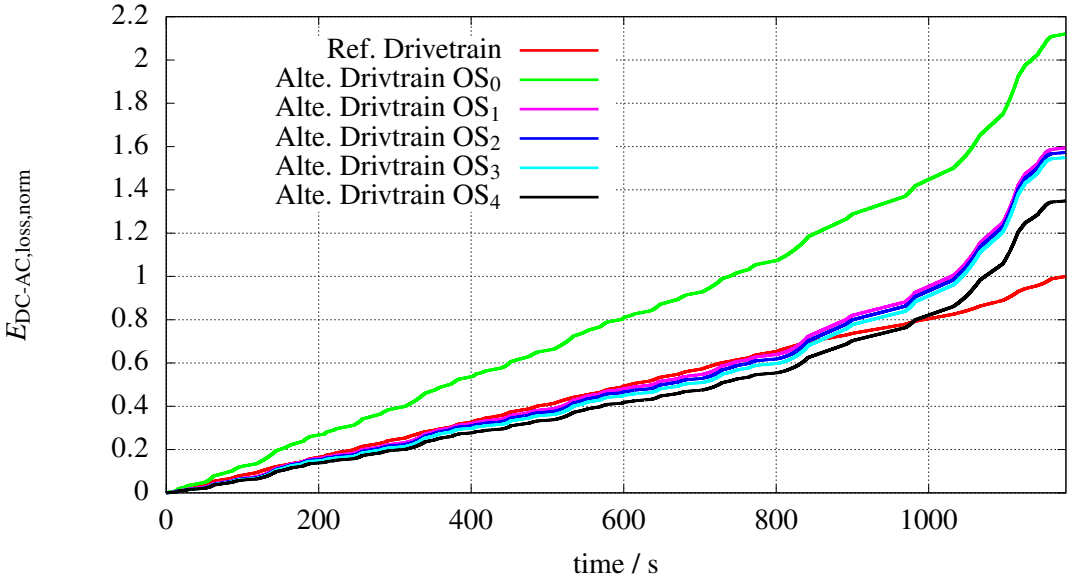

Figure 5.15: AC-DC converter energy losses during NEDC (normalized to the total energy losses of the conventional drivetrain at the end of NEDC) for the conventional drivetrain and the alternative drivetrain after activating different operating strategies of table 5.10

All of the calculated energy losses (DC-AC converter losses) shown in figure 5.15 are normalized to the total energy losses value of the conventional drivetrain at the end of the driving cycle. The red line in figure 5.15 shows the normalized energy losses of the convectional drivetrain, which its value reaches 1 at the end of the driving cycle. By adding the DC-DC converter to the drivetrain and fixing the DC-Link voltage to the same value as the conventional drivetrain (OS_0), the total DC-AC converter energy losses of the alternative drivetrain are more than twice as high as the losses of the conventional drivetrain DC-AC converter. This is expected, since the losses of the inverter part of the alternative drivetrain remain the same as the losses in the reference drivetrain (because of the same DC-Link voltage), and the additional multiphase converter generates extra losses. This leads to efficiency reduction of the alternative drivetrain.

By activating the variable DC-Link voltage operating strategy (OS_1), the switching losses of both the interleaving converter and the 3-phase inverter are reduced, which is due to the lower DC-Link voltages during the partial load intervals of the NEDC (figure 5.10). This will partly compensate for the additional DC-DC converter losses of the alternative drivetrain. As a result the total energy losses of the DC-AC converter part decrease by 52.66 % after using

OS_1. Activation of the variable number of active phases, passive mode, and variable switching frequency operating strategies results in further 24.53 % reduction in energy losses. Figure 5.16 shows an overview of the energy losses (the DC-AC converter part) during the entire driving cycle using different drivetrains and operating strategies. In this diagram, the total converter energy losses of the reference drivetrain at the end of NEDC are used as the basis for comparison (the resulting total losses is mapped to 100%), and the losses of the alternative drivetrain are normalized to this value.

By comparing the total converter energy losses of the alternative drivetrain with different activated operating strategy, it is found that after the variable DC-Link voltage operating strategy, the variable switching frequency operating strategy represents the largest leap in loss reduction. This is mainly because this operating strategy is effective at higher DC-Link voltages as well, where the advantages of interleaving operation come into play (lower switching frequencies are required to keep the input current ripple in range, which are resulting in lower switching losses as presented in section 4.4). The smaller improvement of the drivetrain efficiency after enabling OS_2 and OS_3 is due to the fact that these operating strategies are mainly effective in lower speed ranges (figures 5.11 and 5.12). In these operating regions, losses are already low due to OS_1 and the lower DC link voltage set points, even before the additional operating strategies are activated.

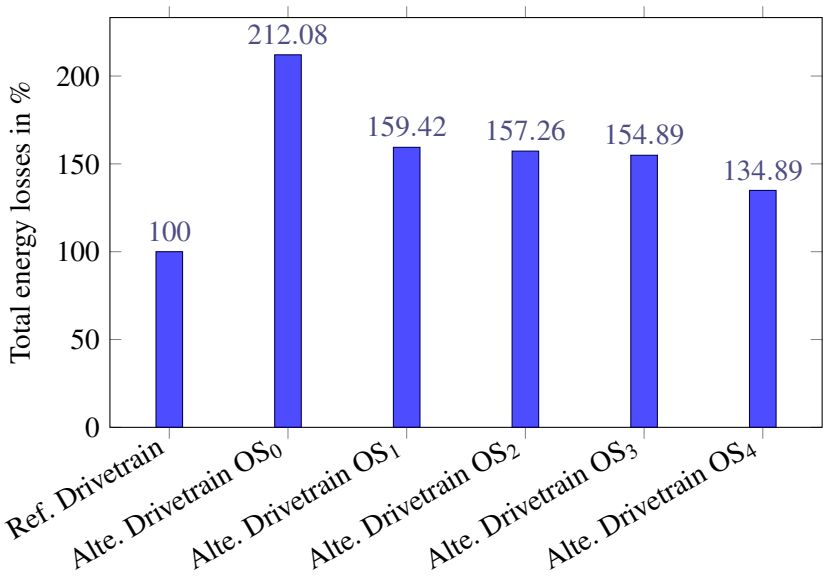

Figure 5.16: DC-AC converter total energy losses comparison between the conventional drivetrain and the alternative drivetrain after activating different operating strategies for the entire NEDC

The overall results shown in figure 5.16 indicate that adding the interleaving DC-DC converter to the drivetrain leads to 34.89 % more energy losses (DC-AC converter part of the drivetrain) in comparison with the reference drivetrain in the best case. By having a closer look at the figure 5.15 and the speed profile of NEDC it can be observed that if only the city rides are included in the evaluation, the alternative drivetrain with activated operating strategies is of advantage compared to the drivetrain without the DC-DC converter. Figure 5.17 shows the same energy

consumption comparison as figure 5.16 with the difference that only the first 800 seconds of the driving cycle (city rides) are considered in the normalized energy losses calculation. In this case, after activating all operating strategies in the alternative drivetrain, the energy losses of the DC-AC converter decrease by 12.17 % in compared to the reference drivetrain.

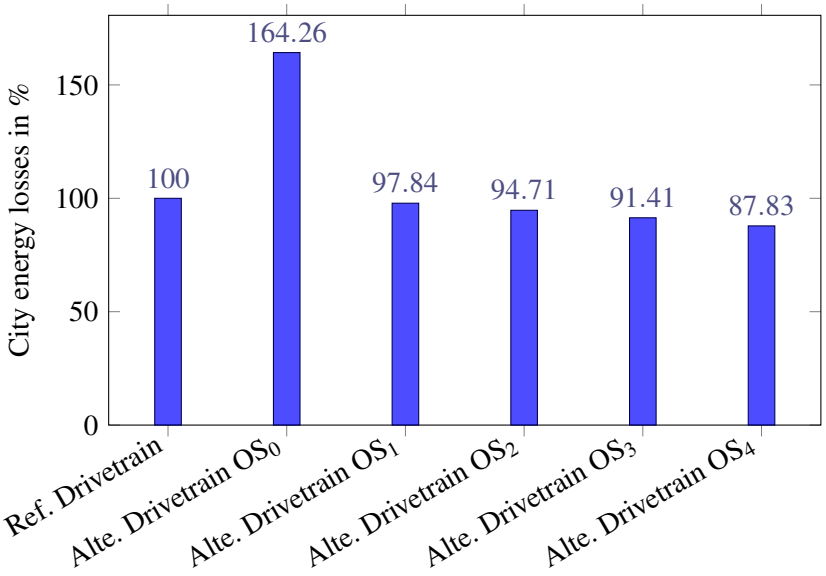

Figure 5.17: DC-AC converter energy losses comparison between the conventional drivetrain and the alternative drivetrain after activating different operating strategies for the city rides of NEDC

The approx. 12 % lower energy losses during city rides makes the alternative drivetrain a proper option for the utilization in parallel hybrid electric vehicle (HEV) discussed in chapter 1 and presented in figure 1.7. In [109] different vehicle concepts for HEV are reviewed. By integrating an interleaving DC-DC converter into the drivetrain, a higher purely electric range can be realized if a suitable power management system distributes the load between the combustion engine and electric motor. The development of a power management system for an HEV with an alternative electric drivetrain, as shown in figure 3.1, and its evaluation is beyond the scope of this work, but the main concept of such a power management system is to generally[9)] activate the combustion engine during highway rides and switch to pure electric mode during city rides.

Another factor that should be investigated in the alternative drivetrain is the influence of the battery voltage level on the energy losses of its DC-AC converter part. For this analysis, the same alternative drivetrain components presented in section 5.1 are used, but this time, instead of $u_{\mathrm{Bat}} = 110$ V, the battery voltage is set to different values. As before, the DC-AC converter energy losses of the drivetrain are calculated over the course of the driving cycle. Figure 5.18 shows the simulation results of the normalized energy losses for the city rides. A comparison between results shows that the use of 330 V instead of 110 V battery voltage reduces the efficiency improvement margin at partial loads and resulting in 5.33 % more energy losses. This is mainly due to the lower DC-Link voltage requirement at lower speeds, where the use of a

[9)] There are several aspects and parameters that should be considered when developing the power management system, with the battery state of charge as one of the most important parameters.

lower battery voltage allows a further reduction of the DC-Link voltage and the corresponding switching losses of the DC-DC converter and inverter. On the other hand, increasing the minimum DC-Link voltage of the system to 330 V (specified by the battery) will reduce the inductor average current and voltage gain of the DC-DC converter for a given output load and output speed, respectively. This can reduce the total ohmic losses and inductor current ripple of the DC-DC converter during the city rides. In other words, the optimum battery voltage should be somewhere between 110 V and 330 V, where a trad-off is made between higher switching losses and lower ohmic losses. After performing a point-by-point simulation in terms of battery voltage (10 V step), it has been determined that a battery voltage of 210 V results in the lowest energy losses during city driving. With that, using the alternative drivetrain reduces the overall energy losses of the system by 15.31 %.

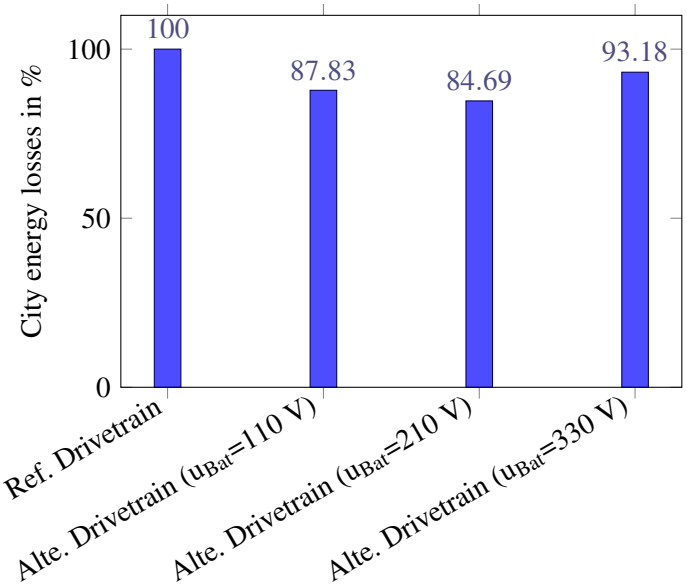

Figure 5.18: DC-AC Converter energy losses comparison for the entire NEDC city rides between the conventional drivetrain and the alternative drivetrain with different battery voltages

At the same time by taking a look at the normalized energy losses over the entire driving cycle including the highway rides (figure 5.19 shows the DC-AC converter energy losses comparison for the reference drivetrain, and the alternative drivetrain with three different battery voltages), it is observable that the alternative drivetrain disadvantages at full load conditions (much higher speeds and output loads compared to the city rides) are more compensated in the drivetrain with higher battery voltages. The reason for this difference is that in the drivetrain with higher battery voltages, the larger DC-Link voltages required at higher speeds result in lower voltage gain and lower input current of the DC-DC converter. This leads to a reduction of the copper losses of the three inductors as well as the conduction losses of the power transistors and diodes of the DC-DC converter.

As stated in the beginning of this section, the power losses comparison is performed on the DC-AC converter part of the both reference drivetrain and alternative drivetrain. The reason for this is the lack of proper machine model which includes the effect of non-sinusoidal supply (the modulation index, and switching frequency of the 3-phase PWM inverter) on the machine losses

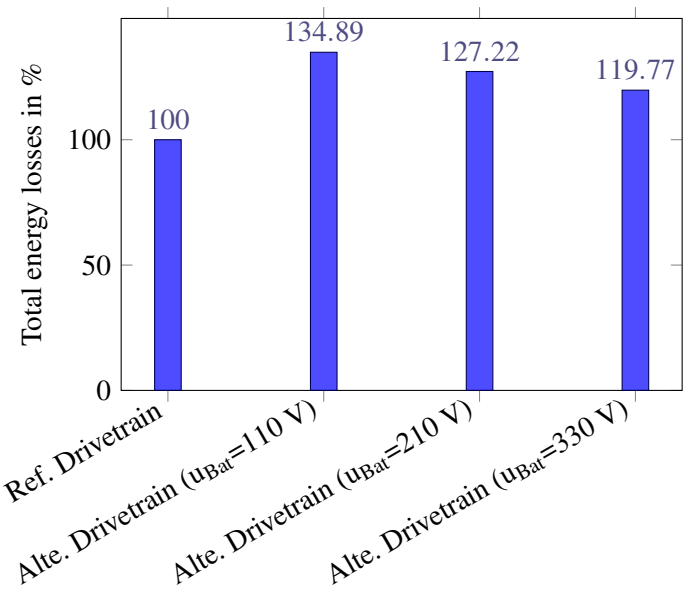

Figure 5.19: DC-AC Converter energy losses comparison for the entire NEDC between the conventional drivetrain and the alternative drivetrain with different battery voltages

(iron losses in particular). There are different methods to develop such a loss model as shown in [110] and [111]. In the context of this work, only the simple machine model presented in 2.4 is used to obtain a realistic load at the output of the DC-AC converter. Nevertheless, the influence of a controllable DC-Link voltage at the input of the inverter-fed machine on the machine iron losses should be evaluated.

Similar to the inductor losses (presented and analyzed in section 2.2), the machine core losses are also dependent on the magnetic flux changes inside the core. It is known that the use of a non-sinusoidal supply at the input of the machine leads to high-order voltage harmonics, which in turn generate harmonics of the higher-order magnetic flux, thus increasing the iron losses in the machine core (hysteresis and eddy current losses of the stator iron and rotor iron). In [14] the effect of different PWM parameters of a 3-phase inverter on the core losses of an induction machine is investigated. These parameters are the modulation index and DC-Link voltage, the switching frequency, and the modulation waveform of the inverter. To investigate this dependency, a special test machine is used in [14] where the rotor cage is made of non-conductive materials, which helps to isolate the losses of the stator core and measure them accurately. The machine can then be fed by an ideal sinusoidal power supply or a 3-phase inverter with variable input DC-Link voltage, modulation index, and switching frequency [10)]. In [14], the following tests are performed on the special test machine:

1. The machine is fed by a sinusoidal supply with different voltages and frequencies up to the nominal operating point values of the machine (constant ratio of voltage and frequency is used to maintain constant flux linkage over the operating region)

[10)] In [14], SPWM is used as the modulation strategy, and other modulation strategies such as SVM are not implemented and tested. The reason for this is that according to [112] the modulation waveform has no significant influence on the iron losses of the machine.

2. The machine is fed by the inverter, which generates the same voltage (fundamental) and frequency as in the first test case, with a constant DC-Link voltage (set to maximum) and variable modulation index
3. The machine is fed by the inverter which, generates the same voltage (fundamental) and frequency as in the first test case, with a constant modulation index (set to maximum) and variable DC-Link voltage

Figure 5.20 shows the iron losses of machine after implementing the three test cases described above. Using a sinusoidal power supply forms a baseline for the machine iron losses (blue curve in the figure), which increase as expected with the motor line voltage and frequency (higher hysteresis losses and eddy current losses). The red and yellow lines in figure 5.20 show the motor iron losses in the case of utilizing an inverter-fed machine with two different control strategies. A comparison of these two curves with the baseline losses shows that using a constant modulation index (set to 1 in the case of SPMW) results in lower iron losses at lower voltages and frequencies (lower speed of the machine). In other words, at lower speeds of the machine it is more efficient to reduce the DC-Link voltage and set the modulation index of the inverter to maximum.

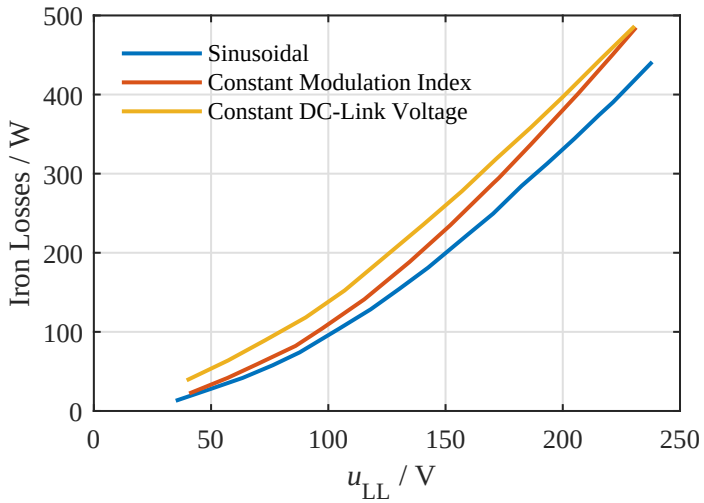

Figure 5.20: Total iron losses of an induction machine as a function of its terminal voltages, with three different power supplies: ideal 3-phase sinusoidal, 3-phase inverter with constant DC-Link voltage and 2 kHz switching frequency, and three phase inverter with constant modulation index and 2 kHz switching frequency (from [14])

Furthermore, in the last two test cases where an inverter is used, in addition to the voltage and frequency variation, the inverter switching frequency is also changed as an extra parameter. By comparing the resulting losses in [14] for different test cases, it is clearly observable that the switching frequency of the converter has a negligible influence on the machine iron losses. The presented influence of the DC-Link voltage and modulation index on the machine iron losses is investigated recently in [41] for the drivetrain application, and same results as in [14] are concluded.

The above iron losses reduction requirement is perfectly fulfilled with first operating strategy

developed and presented in section 4.1. This efficiency improvement of the machine at partial loads is an additional energy saving factor which sums up to the energy losses reduction of the DC-AC converter during city rides presented in figure 5.17.

6 Conclusion and Outlook

In this chapter, a summary of the research findings is presented, highlighting the key results and significant contributions of the study. Following the summary, the chapter concludes with an outlook on the potential implications and future directions for research in this field.

After reviewing the architecture of different low emission drivetrains with different energy storage technologies and energy converters, the optimization of a battery electric vehicle drivetrain in terms of power losses has been chosen as the main focus of this work. In comparison to the state of the art BEV drivetrain, the main change in the drivetrain under investigation is in its DC-AC converter part, where in addition to the 3-phase inverter, it includes a multiphase interleaving DC-DC converter as well. To analyze the alternative drivetrain behavior compared to the standard drivetrain (drivetrain without DC-DC converter extension), in the first step all of its active and passive subcomponents such as power transistor (including temperature dependent power loss model), electric machine, inductor, and capacitor are modeled using SIMULINK. The developed models are then utilized to compile the entire drivetrain model and design the appropriate control system for it. In addition to the switching model of the DC-DC converter and the 3-phase inverter, the state-space average model of these components have been developed and evaluated as well. As a result of state-space averaging, the simulation's computational complexity is reduced, allowing for longer driving cycles to be simulated and drivetrain performance to be evaluated in terms of power losses and control behavior.

In order to optimize the power losses of the DC-AC voltage converter part of the drivetrain, four different operating strategies for the multiphase interleaving DC-DC converter have been developed and proposed using the drivetrain model. It has been been shown that decreasing the DC-Link voltage to the minimum level required by the inverter-fed machine (depending on its operating point) resulting in lower power losses of the DC-AC converter. Furthermore adjusting the variable number of active phases based on the DC-DC converter load condition improved the efficiency under partial load conditions. Diactivating the PWM unit of the DC-DC converter in the case of DC-Link set point voltages lower than the battery voltage was another proposed method to reduce the power losses of the DC-DC converter. Last but not least, the use of the interleaving feature of the DC-DC converter enabled the reduction of the switching frequency and thus the switching power losses, while the battery current ripple remained within the required range. The drivetrain control system has been extended accordingly to support the operating strategies mentioned above. The transient response of the system has been extensively analyzed using simulations while the DC-DC converter toggled between different operation modes. The results demonstrated promising control performance under the above conditions and load changes.

The prototype IGBT-based three-phase interleaving DC-DC converter built in the frame of this work has been thoroughly tested, focusing on the verification of the developed power loss model and validation of the controller stability under different modes of operation. In this test setup the controller and monitoring algorithm have been executed on a dSPACE system. Furthermore, a custom data acquisition board with the oversampling feature was developed using ΣΔ-ADCs to ensure symmetrical load sharing between converter phases in the presence of interleaving and variable switching frequency operations. The interface between the measurement board, the IGBT driver board, and the dSPACE has been utilized using a personalized FPGA board, which is programmed to operate as an ADC driver, a variable frequency PWM modulator, and a communication layer between the data acquisition board and dSPACE. The measurement results showed a robust converter control performance under different transients such as variable switching frequency, variable number of active phases, and variable DC-Link voltage, which are matching the simulation results. In addition to the controller performance evaluation, the test setup has also been used to verify the developed loss model of the DC-DC converter. The presented converter efficiency measurement results showed an acceptable deviation between measurement and simulation of maximum 1%.

In the final step, the DC-AC converter energy losses of the reference drivetrain has been compared to that of the alternative drivetrain, which included the additional multiphase interleaving DC-DC converter. For this comparison, the mechanical model of a prototype electric vehicle has been used, and for a given maximum torque and speed of the vehicle, the two aforementioned drivetrains have been dimensioned separately. Aside from the DC-AC converter part, the only difference between the two drivetrains was the battery voltage, as the alternative drivetrain was able to operate with lower battery voltages and boost the voltage to the level required by the inverter-fed machine. The **New European Driving Cycle** is used as the mission profile to evaluate the energy losses of each drivetrain. The results revealed that by incorporating the DC-DC converter into the drivetrain and activating all the loss optimizing operating strategies, the energy losses of the DC-AC converter increased by 36.89 % over the course of NEDC. It has been discussed that this is mainly due to the high voltage demand of the inverter-fed machine during highway driving, where the DC-DC converter generates additional losses, while the losses of the rest of the drivetrain remain at the same level as the reference drivetrain. In this regard if only the city rides of NEDC are included in the evaluation, it has been shown that over the course of the city rides the DC-AC converter energy losses of the alternative drivetrain are reduced by 12.17% in comparison to the reference drivetrain. This improvement could be increased further to 15.31% by optimizing the selected battery voltage of the alternative drivetrain (210 V instead of 110 V). This increase in the battery voltage level led to a better balance between the ohmic losses generated by the inductors and transistors of the DC-DC converter and the switching losses of the power transistors.

The impact of the non-sinusoidal power sources (in this case the DC-AC converter) on the electric machine iron losses has been briefly touched upon in this work. By reference to the literature, it has been shown that the amplitude of higher harmonics and the associated iron losses decreased by increasing the modulation index of the inverter. This means that, implementing a DC-AC converter with adjustable DC-Link voltage, same as the converter used in the alternative drivetrain, will lead to a reduction in the iron losses of the electric machine, resulting in an

improvement of the overall drivetrain efficiency. However, the focus of this study was solely on the DC-AC converter losses, and therefore, modeling the voltage converter characteristic (specifically, the switching frequency and modulation index of the inverter part) on the machine iron losses was not within the scope of this work. Nevertheless, the outcomes of this research can be utilized and expanded in future studies to encompass the iron losses model of the inverter-fed machine, and assess the energy savings quantitatively for the drivetrain with variable DC-Link voltage (similar to the recent research presented in [41]).

The findings from this work indicated that the drivetrain incorporating the DC-DC converter exhibited reduced energy losses during city rides, suggesting its potential as a viable alternative for parallel hybrid electric vehicle applications. With respect to the fact that the HEV drivetrain was out of scope of this work, it was pointed out that these results can be used in future research to develop an effective energy distribution algorithm. Such an algorithm could allow for the real-time adjustment of the traction source based on driving behavior, resulting in further optimization of the drivetrain efficiency.

This study employed Si-based IGBTs as the power transistors for the DC-AC converter implementation. By referring to the literature, it has been discussed that Si-IGBTs will lead to higher converter efficiencies against the Si-based MOSFETs[1)] for the selected machine voltage level (400 V). The use of MOSFETs with wide band gap technology (e.g. silicon carbide MOSFET) could be another option for the implementation of the converter, but the lower cost of the IGBT power transistors compared to SiC-MOSFETs, and the fact that the advantages of wide band gap technology could not be fully exploited for the selected machine voltage ([78]), were two reasons why the Si-IGBTs are used for the analysis in this work. Nevertheless, utilizing SiC-MOSFETs brings some advantages, such as reducing the size of passive components by operating the transistors at higher switching frequencies ([113]) as well as further reduction of the converter power losses in partial load ([78]). Since using wide band gap technology in the DC-DC converter for drivetrain application is still a relevant topic (e.g. [40]), as a future research, the results presented in this work can be used and complemented by extending the developed models for the SiC-MOSFETs, and comparing the results between the SiC-MOSFET and Si-IGBT implementations.

As mentioned above, using SiC-MOSFET could help reducing the switching losses, but in a conventional hard-switched operation of power transistors, the switching losses become significant at higher switching frequencies. On the other hand, the hard-switched converters suffer from high EMI emissions generated by high rate of voltage changes (dv/dt) at higher switching speeds [114]. Accordingly, another aspect which can be initiated as a future research topic is the use of SiC based DC-DC converters with soft switching capability, to further reduce the losses under zero-voltage switching (ZVS) and zero-current switching (ZCS) conditions for the drivetrain application.

[1)] As stated in section 2.3.1, in the conventional MOSFETs with planar structure, switch-on resistance ($R_{\mathrm{DS_{on}}}$) increases with the increasing maximum blocking voltage level of the MOSFET.

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directional buck+boost DC-DC converters," *Power Electronics Conference (IPEC), 2010 International*, 2010.

Curriculum Vitae

Name:	Rashidreza Karimi
Date of birth:	24.05.1987
Place of birth:	Esfahan, Iran
Nationality:	German

Work Experience:

10/2016 - Present	Lead project engineer, Baker Hughes, Celle, Germany
10/2013 - 09/2016	Research assistant, Institute for Drive Systems and Power Electronics, Hannover, Germany

Education:

10/2013 - 09/2016	Ph.D. in Electrical Engineering, Leibniz University of Hannover, Germany
10/2010 - 09/2012	M.Sc. in Electrical Engineering, Leibniz University of Hannover, Germany
10/2005 - 09/2010	B.Sc. in Electrical Engineering, Esfahan University, Esfahan, Iran

School:

10/2004 - 09/2005	Sadegh pre-university, Esfahan, Iran
10/2001 - 09/2004	Bagher high school, Esfahan, Iran
10/1993 - 09/2001	Nikbakht elementary school, Esfahan, Iran

Publications and Presentations

R. Karimi, T. Koeneke, D. Kaczorowski, T. Werner, and A. Mertens, "Low voltage and high power DC-AC inverter topologies for electric vehicles," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, pp. 2805-2812 Sept 2013.

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R. Karimi, D. Kaczorowski, A. Zlotnik, and A. Mertens, "Loss Optimizing Control of a Multiphase Interleaving DC-DC Converter for Use in a Hybrid Electric Vehicle Drivetrain", in *Energy Conversion Congress and Exposition (ECCE), 2016 IEEE*, pp. 1-8, Sept 2016.