Applying temperature-sensitive electrical parameters to SiC power modules considering parasitic effects

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Kurzfassung

Temperatursensitive elektrische Parameter (TSEPs) können für die Zustandsüberwachung von unmodifizierten Leistungsmodulen oder zur Bestimmung der virtuellen Sperrschichttemperatur von Leistungshalbleitern eingesetzt werden.

Die Erfassung von TSEPs an schnellschaltenden Wide-Bandgap-Halbleitern stellt dabei besondere Herausforderungen an die benötigte Messauflösung und die Störempfindlichkeit der Messschaltungen. Neben der Sperrschichttemperatur werden TSEPs von einer Vielzahl von anderen Größen beeinflusst. Diese Querempfindlichkeiten können in solche unterteilt werden, die bereits im normalen Umrichterbetrieb miterfasst werden, zum Beispiel der Laststrom, und in parasitäre Einflüsse, welche nur schwer zu bestimmen sind oder deren Erfassungsaufwand zu groß wäre. Parasitäre Störeinflüsse können zu signifikanten Abweichungen in der bestimmten virtuellen Sperrschichttemperatur führen.

In dieser Dissertation wird die Anwendbarkeit von TSEPs an schnellschaltenden SiC-MOSFETs, unter besonderer Beachtung von parasitären Störeinflüssen, untersucht. Beispiele von parasitären Störeinflüssen sind Änderungen der Treibertemperatur oder Instabilitäten der Gatetreiberspannungen. Das Ziel ist die rechtzeitige Erkennung eines bevorstehenden Modulausfalls.

Mehrere TSEPs werden in direkter Abfolge erfasst und anschließend kombiniert. Die betrachteten TSEPs sind die Durchlassspannungen der SiC-MOSFETs sowie zwei Schaltzeiten während des Einschaltvorgangs. Die Kombination erlaubt die Reduktion von parasitären Störeinflüssen. Dabei wird insbesondere die Eignung von künstlichen neuronalen Netzen zur Kombination der TSEPs zu einer vereinten Temperaturaussage untersucht und mit Ansätzen verglichen, die auf den physikalischen Wirkprinzipien der Halbleiter beruhen.

Eine Vielzahl detaillierter Halbleitermodelle werden gebildet, deren Eignung zur Unterscheidung temperaturbedingter und strombedingter Änderungen der betrachteten TSEPs ermittelt wird. Dabei wird auch untersucht, welcher Detaillierungsgrad der Modelle für eine Temperaturbestimmung nötig ist.

Neben den theoretischen Untersuchungen wird Messhardware zur Erfassung der Durchlassspannung sowie der Schaltzeiten von schnellschaltenden SiC-MOSFETs untersucht und entworfen. Diese Messhardware wird genutzt, um TSEPs sowohl in Doppelpulsversuchen als auch im regulären Schaltbetrieb zu erfassen. Dabei entstehen durch die kurzen Leitphasen der schnellschaltenden SiC-MOSFETs sowie durch schaltbetriebsspezifische Effekte besondere Herausforderungen.

Ein detailliertes thermisches Modell der Module sowie des Prüfstands wird erstellt. Zusätzlich entsteht ein Strommodell, welches die Bestimmung des Momentanstromwertes beim Einschalten der Halbleiter aus dem skalaren Messwert des regulären Umrichterstromsensors erlaubt.

Abschließend werden beschleunigte Alterungstests durchgeführt. Dabei werden mehrere Leistungsmodule mit thermischen Lastzyklen beaufschlagt, um realistische thermomechanische Alterungseffekte zu erzeugen. Die Leistungsmodule werden während der Alterung regelmäßig mit der TSEP-Messhardware analysiert. Mit den Testergebnissen wird verifiziert, dass die TSEP-Messhardware genutzt werden kann, um eine Degradation der Leistungsmodule rechtzeitig vor dem Erreichen des Endes der Lebensdauer der Module zu erkennen.

Schlagworte:
Temperatursensitive elektrische Parameter, Zustandsüberwachung, Siliziumcarbid, MOSFET Modelle , Künstliche neuronale Netze, Thermische Impedanz, Alterungstests

Abstract

Temperature-sensitive electrical parameters (TSEPs) can be used to monitor the condition of unmodified power modules or to measure the virtual junction temperature of a semiconductor. The measurement of TSEPs on fast-switching wide-bandgap semiconductors poses new challenges with regard to the required measurement accuracy and the high EMI tolerance capability. Furthermore, TSEPs are affected by many parameters beside the virtual junction temperature or the degradation state of the module. These cross-dependencies can be separated into parameters that are typically measured during operation, e.g., the load current, and parasitic impacts that are unknown, or cannot be feasibly acquired.

In this thesis, the application of TSEPs to fast-switching wide-bandgap silicon carbide (SiC) MOSFETs is studied, giving special consideration to parasitic impacts. Examples of these impacts are changes in the gate driver's temperature or instabilities in the gate driver's voltages. Parasitic impacts can lead to significant deviations in the virtual junction temperature determined.

Several TSEPs are acquired simultaneously and combined to reduce the effects of these impacts on the TSEP-based temperature estimation. The TSEPs used are the on-state voltages of the switches and two switching times during turn-on. The suitability of artificial neural networks for combining and mapping multiple TSEPs to a single virtual junction temperature estimate is investigated and compared to physics-based approaches.

A variety of detailed analytical models representing the on-state voltage and switching times during turn-on are investigated, including SiC-specific effects. The aim is to determine which level of model complexity is necessary to separate the temperature-dependent behavior from the current-dependent behavior of the considered TSEPs. Simultaneously, the analytical modeling identifies numerous possible parasitic impact factors which affect the measurement of TSEPs.

Beside the theoretical aspects, TSEP measurement hardware for the on-state voltage and switching times of SiC MOSFETs is designed. This is used to acquire TSEP measurements in double-pulse experiments as well as during continuous PWM operation. Challenges arising from the short conduction phases at high switching frequencies and also from PWM-specific effects are studied and compensation concepts are presented.

Detailed thermal models of the power module and test setup are created, together with a current model which determines the instantaneous current during turn-on from the scalar current sample provided by the inverter sensors.

Finally, accelerated aging tests are conducted. Several power modules are power cycled until they reach their end of life. During the testing they are periodically analyzed with the TSEP measurement system. The test results verify that the TSEP measurement system is capable of detecting thermomechanical degradation mechanisms before the module reaches its end of life.

Keywords:
temperature-sensitive electrical parameters, condition monitoring, silicon carbide, MOSFET models, artificial neural networks, thermal impedance, aging tests

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Symbol conventions

x	variable
$\boldsymbol{x}$	vector
X	constant value
$\boldsymbol{X}$	matrix
$\boldsymbol{X}^{\mathrm{T}}$	transpose of a matrix
x'	related quantity or relative quantity
$\tilde{x}$	measured value
$\lvert x \rvert$	absolute value
$\overline{x}$	mean value
$\underline{x}$	complex number
$\dot{x}, \ddot{x}$	first and second derivative of x with regard to the time
x_{sp}	set point
x^{*}	fit model function
$x^{(\mathrm{description})}$	additional description, context-dependent
$S_x = \{x_1, x_2, ...\}$	set containing elements of x
$F(s)$	Laplace transform of f or transfer function
$F(j\omega)$	Fourier transform of f or frequency response
$P(X \mid Y)$	conditional probability of X under the condition Y
$\overset{!}{=}$	condition
$y(x) \in \mathcal{O}(f(x))$	asymptotic notation; $\lim\limits_{x\to\infty} y(x) \overset{!}{=} a \lim\limits_{x\to\infty} f(x), \quad a \in \mathbb{R}$
$\lim\limits_{t\to 0^{+}}(x), \lim\limits_{t\to 0^{-}}(x)$	one-sided limits of x
$\mathbb{N}_0$	positive natural number or zero

Abbreviations

4H-SiC	silicon carbide crystal structure, repeating its structure every four layers
6H-SiC	silicon carbide crystal structure, repeating its structure every six layers
AC	alternating current
ADC	analog-to-digital converter
ANN	artificial neural network
ANOVA	analysis of variance
BJT	bipolar junction transistor
BNC	Bayonet Neill–Concelman connector
CAS	computer algebra system
CMOS	complementary metal–oxide–semiconductor
CTE	coefficient of thermal expansion
DCB	direct-copper-bonded
DC	direct current
DIBL	drain-induced barrier lowering
D-MOSFET	planar MOSFET
DUT	device under test
EMI	electromagnetic interference
EOL	end of life
FB	full-bridge
FEM	finite-element-method
GND	ground
H3TRB	high humidity, high temperature reverse bias
HB	half-bridge
HF	high-frequency
HS	high side
HTGS	high temperature gate stress
HTRB	high temperature reverse bias
HV	high voltage
IC	integrated circuit

ID	identifier
IGBT	insulated-gate bipolar transistor
IISB	Fraunhofer Institute for Integrated Systems and Device Technology IISB
IQR	interquartile range
IR	infrared
JFET	junction field-effect transistor
LDO	low dropout voltage regulator
LIDAR	light detection and ranging
LP	low-pass
LS	low side
LVDS	low voltage differential signaling
LV	low voltage
MISO	master input slave output
MOSFET	metal-oxide-semiconductor field-effect transistor
MOSI	master output slave input
MOS	metal-oxide semiconductor
NTC	negative temperature coefficient
PCB	printed circuit board
PCT	power-cycling test
$\mathbf{PC_{min}}$	thermal cycling
$\mathbf{PC_{sec}}$	power-cycling
PE	protective earth
PGNN	physics-guided neural network
PTC	positive temperature coefficient
PWM	pulse-width modulation
RMSD	root-mean-square deviation
SCLK	serial clock
SOA	safe operating area
SPICE	simulation program with integrated circuit emphasis
SPI	serial peripheral interface
STD	standard deviation
TDC	time-to-digital converter
TIM	thermal interface material
TSEP	temperature-sensitive electrical parameter

TST	thermal shock test
TVS	transient voltage suppressor
U-MOSFET	U-shaped MOSFET or trench MOSFET
p.u.	per unit

Nomenclature

Latin Letters

a_f	acceleration factor in lifetime models
a_i	regression parameter; usually not the same across different model fitting functions, see Section 1.2
b_sc	width of the space-charge region
B_ch	width of the MOS channel (normal to the current direction, oriented towards the bulk)
B_g	width of the charge located on the gate contact
B_geo	effective width of the JFET channel
B_ins	width of the insulator of a MOS structure
B_jfet	width of a JFET channel with constant width
B_n	width of the inversion layer
$B_\mathrm{sc,th}$	width of the space-charge region when the threshold voltage is applied
C_dc	dc-link capacitance
$C_\mathrm{dr,off}$	decoupling capacitance of the negative gate driver voltage
$C_\mathrm{dr,on}$	decoupling capacitance of the positive gate driver voltage
C_ds	drain-source capacitance
C_g	gate capacitance
C_gd	drain-gate or Miller capacitance
C_gs	gate-source capacitance
$C_{\mathrm{g},i}$	capacitance value of a piecewise linear gate charge curve
C_iss	input capacitance
C_node	node capacitance
C_oss	output capacitance
C_ox	oxide charge
C_rss	reverse transfer capacitance
C_tdc	input capacity of the time-to-digital converter
d	duty cycle
d_i	duty cycle of half-bridge i
D_ch	depth of the MOS channel (normal to the current direction, parallel to the insulator)
D_ox	thickness of the oxide insulating the MOS channel from the gate contact
e_0	elementary charge

E	Young's module
E_{aff}	electron affinity
E_{c}	lower energy level of the conduction band
E_{crit}	critical electrical field
E_{F}	Fermi level
$E_{\mathrm{F,G}}$	Fermi level of a gate metal
$E_{\mathrm{F,S}}$	Fermi level of a semiconductor
E_{G}	bandgap
E_{i}	Fermi level of an intrinsic semiconductor
E_{M}	cost function component corresponding to measurements
$E_{\mathrm{n,eff}}$	effective electric field in the MOS channel
E_{ox}	electric field in the oxide insulating the MOS channel from the gate contact
E_{ref}	reference loss energy of the switching-loss model
E_{sw}	switching-loss energy
$E_{\mathrm{sw,off}}$	switching losses during turn-off
$E_{\mathrm{sw,on}}$	switching losses during turn-on
E_{Si}	electric field in a silicon semiconductor
E_{v}	upper energy level of the valence band
E_{vac}	vacuum energy
E_{work}	work function
E_{W}	cost function component corresponding to regression weights
f_{pwm}	switching frequency of the PWM
i_{c}	collector current, oriented flowing into the collector terminal
i_{com}	commutation current
i_{d}	drain current, oriented flowing into the drain contact
i_{g}	gate current
i_{L}	load current
$\overline{I}$	sample of the average current during a PWM period
$I_{\mathrm{c,ANN}}$	collector current predicted by an ANN
$I_{\mathrm{c,co}}$	cross-over current
$I_{\mathrm{d,sat}}$	saturation drain current
$I_{\mathrm{d,sp}}$	drain current set point
I_{heat}	heating current
I_{meas}	measurement current used in the V_{ce}-method
I_{mid}	instantaneous at the midpoint of a PWM period
I_{N}	nominal current
I_{plateau}	current of the middle current plateau during a PWM period
I_{rrm}	maximum reverse recovery current

I_{sat}	saturation current
I_{scope}	instantaneous turn-on current measured with an oscilloscope
I_{ton}	instantaneous current at the turn-on of a switch
$I_{\text{ton,HS}}$	instantaneous current at the turn-on of a high-side switch
$I_{\text{ton,LS}}$	instantaneous current at the turn-on of a low-side switch
I_1	current step corresponding to the first pulse during a PWM
I_2	current step corresponding to the second pulse during a PWM
K	transconductance
K_{A}	approximation factor used for the accumulation layer
L_{aux}	additional auxiliary inductance to lower a resonant frequency
L_{ch}	length of the MOS channel (in the current direction)
L_{dc}	parasitic dc-link inductance
L_{D}	Debye length
L_{g}	gate loop inductance
L_{jfet}	length of the JFET region
L_{ks}	parasitic inductance between the source and the Kelvin source terminal
L_{R}	parasitic inductance of a resistor
M_{dg}	magnetic coupling between the drain-source path and the gate loop
n_{cal}	number of used calibration measurements
$\overline{n}_{\text{ch}}$	average electron concentration in the channel
n_{cycle}	number of PC_{sec} stress cycles
n_{end}	last evaluated ADC sample
n_{i}	intrinsic carrier concentration
n_{meas}	total number of measurements
n_{n}	electron concentration in the n region
n_{n0}	unbiased electron concentration in the n-doped region
n_{p}	electron concentration in the p region
n_{par}	number of used regression parameters
n_{poly}	degree of a polynomial
n_{p0}	unbiased electron concentration in the p-doped region
n_{start}	first evaluated ADC sample
N_{A}	concentration of the acceptor atoms
N_{A}^{-}	concentration of the ionized acceptor atoms
N_{C}	state density of the conduction band
N_{D}	concentration of the donator atoms
N_{D}^{+}	concentration of the ionized donator atoms
N_{f}	number of cycles until failure
N_{V}	state density of the valence band

p	power
p_{c}	conduction losses
p_{n}	hole concentration in the n region
p_{n0}	unbiased hole concentration in the n-doped region
p_{p}	hole concentration in the p region
p_{p0}	unbiased hole concentration in the p-doped region
p_{sw}	switching losses
P_{heat}	heating power
$\overline{P}_{\mathrm{sw,off}}$	average losses during a PWM period due to the turn-off losses
$\overline{P}_{\mathrm{sw,on}}$	average losses during a PWM period due to the turn-on losses
Q_{ch}	MOS channel charge
Q_{g}	gate charge
Q_{n}	charge of the inversion layer
Q_{node}	charge of the node capacitance
Q_{oss}	charge stored in the output capacitance
Q_{p}	charge of the accumulation layer
Q_{rr}	reverse recovery charge
Q_{s}	total charge in the MOS channel
Q_{sc}	charge of the space-charge region
$Q_{\mathrm{sc,max}}$	maximum charge of the space-charge region
R_{A}	resistance of the accumulation layer
R_{ch}	channel resistance
R_{charge}	shunt resistor used in the gate charge curve measurement
R_{CD}	resistance of a metal-semiconductor contact at the drain contact
R_{CH}	resistance of the channel
R_{CS}	resistance of a metal-semiconductor contact at the source contact
R_{dr}	internal driver resistance
$R_{\mathrm{ds,on}}$	on-state resistance
$R_{\mathrm{d,dc}}$	resistance between the MOSFET drain and the positive dc-link potential
R_{D}	resistance of the drift region
$R_{\mathrm{ek,d},i}$	discrete resistance placed inside an IGBT module into the Kelvin emitter terminal path
R_{epi}	resistance of the epitaxial layer
R_{g}	gate resistance
R_{gas}	ideal gas constant
$R_{\mathrm{g,chip}}$	on-chip gate resistance
$R_{\mathrm{g,d},i}$	discrete resistance placed inside an IGBT module into the gate terminal path
$R_{\mathrm{g,ext}}$	overall external gate resistance

$R_{\mathrm{g,int}}$	internal gate resistance including discrete resistances in the module
$R_{\mathrm{g,off,ext}}$	external gate resistance in turn-off path
$R_{\mathrm{g,on,ext}}$	external gate resistance in turn-on path
R_{JFET}	resistance of the JFET region
R_{L}	load resistance
$R_{\mathrm{N+}}$	resistance of the n-drift region
R_{SUB}	resistance of the highly-doped N^{+} substrate
R_{t}	chip-to-terminal resistance
R_{th}	thermal resistance
$R_{\mathrm{th,ca}}$	thermal resistance between the the case and ambient
$R_{\mathrm{th,HS,HS}}$	thermal resistance of the self heating of the high-side switch
$R_{\mathrm{th,HS,LS}}$	thermal resistance of the cross coupling from the high-side switch to the low-side switch
$R_{\mathrm{th,HS,NTC}}$	thermal resistance of the cross coupling from the high-side switch to the NTC sensor
$R_{\mathrm{th,ja}}$	thermal resistance between the junction and ambient
$R_{\mathrm{th,jc}}$	thermal resistance between the junction and the case
$R_{\mathrm{th,jh}}$	thermal resistance between the junction and the heat sink
$R_{\mathrm{th,LS,HS}}$	thermal resistance of the cross coupling from the low-side switch to the high-side switch
$R_{\mathrm{th,LS,LS}}$	thermal resistance of the self heating of the low-side switch
$R_{\mathrm{th,LS,NTC}}$	thermal resistance of the cross coupling from the low-side switch to the NTC sensor
s_{FB}	output signal of a full-bridge
$s_{\mathrm{HB},i}$	switching signal of half-bridge HBi
s_i	switching signal of switch i
$S_{U_{\mathrm{ds,virt}}}$	set containing all virtual on-state voltage measurements
t_{charge}	charge time of an RC element
t_{d}	turn-on delay time
$t_{\mathrm{d}}^{\prime(\mathrm{HS})}$	turn-on delay time of the high-side switch, normalized to its value before aging
$t_{\mathrm{d}}^{\prime(\mathrm{LS})}$	turn-on delay time of the low-side switch, normalized to its value before aging
t_{fb}	time when the flat-band voltage is reached
t_{fixed}	assumed fixed time between the switching process and the first ADC sample
$t_{i,\mathrm{HB},j}$	turn-on moment i of half-bridge k
t_{off}	duration of the cooling phase during the $\mathrm{PC}_{\mathrm{sec}}$ tests
$t_{\mathrm{off,HS}}$	turn-off moment of a high-side switch
$t_{\mathrm{off,LS}}$	turn-off moment of a low-side switch

t_{on}	duration of the heating phase during the $\mathrm{PC_{sec}}$ tests
$t_{\mathrm{on,HS}}$	turn-on moment of a high-side switch
$t_{\mathrm{on,LS}}$	turn-on moment of a low-side switch
t_{ri}	current rise time
$t'^{(\mathrm{HS})}_{\mathrm{ri}}$	current rise time of the high-side switch, normalized to its value before aging
$t'^{(\mathrm{LS})}_{\mathrm{ri}}$	current rise time of the low-side switch, normalized to its value before aging
t_{rr}	reverse recovery time
t_{rrm}	time until the overcurrent peak during turn-on is reached
$t'^{(\mathrm{HS})}_{\mathrm{rrm}}$	time until the overcurrent peak of the high-side switch is reached, normalized to its value before aging
$t'^{(\mathrm{LS})}_{\mathrm{rrm}}$	time until the overcurrent peak of the low-side switch is reached, normalized to its value before aging
t_{start}	start time of a switching time measurement
t_{trig}	TDC trigger delay
T_{delay}	delay between the gate signal and the first ADC sample
$T_{\mathrm{d,L}}$	delay caused by the gate inductance
$T_{\mathrm{d,off}}$	constant turn-off delay time
$T_{\mathrm{d,on}}$	constant turn-off delay time
T_{D}	interlock time
T_{Dvf}	reduction in the effective interlock time
T_{fv}	voltage fall time
T_{ideal}	ideal width of an applied voltage pulse
T_{offset}	time offset between the switching process and the first ADC sample
T_{p}	propagation delay of a switching signal carrier
T_{plateau}	duration of the middle current plateau during a PWM period
T_{pulse}	duration of a time-to-digital converter trigger pulse
T_{pwm}	duration of a PWM period
T_{rv}	voltage rise time
T_{sample}	sampling distance of ADC samples
T_1	duration of the first voltage pulse during a PWM
T_2	duration of the second voltage pulse during a PWM
u_{ADC}	voltage at the input of the ADC
u_{ce}	collector-emitter voltage
$u_{\mathrm{dr,off}}$	negative gate driver voltage
$u_{\mathrm{dr,on}}$	positive gate driver voltage
$u_{\mathrm{dr,out}}$	output voltage of the gate driver
$u_{\mathrm{dr,supply}}$	supply voltage of the gate driver
u_{ds}	drain-source voltage

$u_{\mathrm{ds,hs}}$	on-state drain-source voltage of the high-side switch
$u_{\mathrm{ds,ls}}$	on-state drain-source voltage of the low-side switch
$u_{\mathrm{ds,on}}$	on-state drain-source voltage
u_{g}	gate voltage
$u_{\mathrm{g,t}}$	gate voltage as measured at the power module’s terminal contacts
$u_{\mathrm{HB},i}$	output voltage of half-bridge i
u_{i}	load voltage
u_{L}	load voltage
u_{out}	output voltage of a full-bridge setup
u_{sig}	voltage of a signal generator
u_{sk}	voltage between the source and the Kelvin source contact
u_{start}	start trigger signal of the TDC
$u_{\mathrm{stop},t_{\mathrm{d}}}$	stop trigger signal of the TDC for t_{d}
$u_{\mathrm{stop},t_{\mathrm{rrm}}}$	stop trigger signal of the TDC for t_{rrm}
U_{a}	voltage drop across the accumulation layer
U_{base}	base voltage of the JFET region
U_{bi}	built-in potential
U_{br}	breakdown voltage
U_{cc}	positive supply voltage
U_{ce}	collector-emitter voltage
U_{ces}	maximum collector-emitter voltage
U_{ch}	voltage drop across the MOS channel
$U_{\mathrm{ch,po}}$	pinch-off voltage of the MOS channel
U_{dc}	dc-link voltage
$U_{\mathrm{dc,ANN}}$	dc-link voltage predicted by an ANN
$U_{\mathrm{dc,sp}}$	dc-link voltage set point
U_{drift}	voltage drop across the drift region
$U_{\mathrm{dr,off,0}}$	initial value of negative driver voltage
$U_{\mathrm{dr,on,0}}$	initial value of positive driver voltage
$U_{\mathrm{ds,on,HS}}$	on-state drain-source voltage of the high-side switch
$U_{\mathrm{ds,on,LS}}$	on-state drain-source voltage of the low-side switch
$U_{\mathrm{ds,virt,turnoff}}$	virtual on-state voltage measured and calculated before turn-off
$U'^{(\mathrm{HS})}_{\mathrm{ds,virt,turnoff}}$	virtual on-state voltage of the high-side switch acquired before turn-off, normalized to its value before aging
$U'^{(\mathrm{LS})}_{\mathrm{ds,virt,turnoff}}$	virtual on-state voltage of the low-side switch acquired before turn-off, normalized to its value before aging
$U_{\mathrm{ds,virt,turnon}}$	virtual on-state voltage measured and calculated after turn-on

$U'^{(\mathrm{HS})}_{\mathrm{ds,virt,turnon}}$	virtual on-state voltage of the high-side switch acquired after turn-on, normalized to its value before aging
$U'^{(\mathrm{LS})}_{\mathrm{ds,virt,turnon}}$	virtual on-state voltage of the low-side switch acquired after turn-on, normalized to its value before aging
U_{f}	diode forward voltage measured before turn-off
U_{fb}	flat-band voltage
U_{gb}	gate-bulk voltage
U_{gs}	gate-source voltage
$U_{\mathrm{g,0}}$	initial gate voltage
U_{jfet}	voltage drop across the JFET region
U_{M}	Miller plateau voltage
U_{n}	voltage drop across the space-charge component in the n-region
U_{p}	voltage drop across the space-charge component in the p-region
U_{po}	pinch-off voltage of the JFET region
U_{sb}	source-bulk voltage
U_{surf}	voltage at the surface of a MOS channel
$U^{(\mathrm{surf})}_{\mathrm{th}}$	voltage at the surface of a MOS channel if the threshold voltage is applied to the gate
U_{t}	voltage drop across the chip-to-terminal resistance
U_{th}	threshold voltage referenced to the source
$U_{\mathrm{th_0}}$	unbiased threshold voltage
$U_{\mathrm{th,b}}$	threshold voltage referenced to the bulk
$U_{\mathrm{th,down}}$	threshold voltage in the downward direction
$U_{\mathrm{th,up}}$	threshold voltage in the upward direction
U_{trig}	trigger voltage of the TDC front ends
$U_{\mathrm{trig,max,sc}}$	maximum induced voltage across the parasitic source inductance during a short circuit
U_{T}	thermal voltage
$U_{\mathrm{uncompensated}}$	on-state voltage increase during the accelerated aging tests without current compensation
v_{d}	drift velocity
$v_{\mathrm{d,sat}}$	saturation drift velocity
$v_{\mathrm{d,sat,n}}$	saturation drift velocity in the n-region
$\boldsymbol{V}$	Vandermonde matrix
w	weight
W_{D}	width of the drift region
W_{jfet}	width of the JFET region
$\hat{y}$	predicted value of y
$\tilde{y}$	measured value of y

$z_{\mathrm{th}}^{(\mathrm{cd})}$	time response of the thermal impedance during cool down
$z_{\mathrm{th,d}}^{(\mathrm{cd})}$	time response of the adapted Foster model during cool down
Z_{th}	thermal impedance
$Z_{\mathrm{th,d}}$	transfer function of the adapted Foster model
$Z_{\mathrm{th,HS,HS}}$	thermal impedance of the self heating of the high-side switch
$Z_{\mathrm{th,HS,LS}}$	thermal impedance of the cross coupling from the high-side switch to the low-side switch
$Z_{\mathrm{th,HS,NTC}}$	thermal impedance of the cross coupling from the high-side switch to the NTC sensor
$Z_{\mathrm{th,LS,HS}}$	thermal impedance of the cross coupling from the low-side switch to the high-side switch
$Z_{\mathrm{th,LS,LS}}$	thermal impedance of the self heating of the low-side switch
$Z_{\mathrm{th,LS,NTC}}$	thermal impedance of the cross coupling from the low-side switch to the NTC sensor
$Z_{\mathrm{th,vj,H}}^{(\mathrm{DS})}$	thermal impedance from the junction to the heat sink according to the datasheet

Greek Letters

α_{ϑ}	exponent with regard to the temperature
α_{I}	exponent with regard to the current
α_{t}	temperature coefficient of the chip-to-terminal resistance
$\Delta\varepsilon_{\mathrm{acc}}$	accumulated mechanical strain cycles
$\Delta\tau_{M}$	modification of the gate loop time constant due to the magnetic drain-current feedback
ΔI_{cm}	common-mode component of the two current steps during a PWM period
ΔI_{dm}	differential-mode component of the two current steps during a PWM period
$\Delta I_{\mathrm{ripple}}$	ripple current
$\Delta I_{\mathrm{slope}}$	current step between I_{mid} and the turn-on process of a switch
ΔW_{acc}	accumulated mechanical energy cycles
ε	mechanical strain
$\varepsilon_{\mathrm{cr}}$	creep
$\varepsilon_{\mathrm{ox}}$	permittivity of the oxide insulating the MOS channel from the gate contact
ε_{p}	primary creep
ε_{r}	relative permittivity
$\varepsilon_{\mathrm{Si}}$	(absolute) permittivity; product of relative and vacuum permittivity
$\varepsilon_{\mathrm{Si}}$	permittivity of a silicon semiconductor
$\varepsilon_{\mathrm{SiC}}$	permittivity of a silicon carbide semiconductor
ζ	damping
ϑ	temperature
ϑ_{a}	ambient temperature

ϑ_{bp}	baseplate temperature
ϑ_{c}	temperature of the cooler surface below the module casing
ϑ_{dr}	temperature of the driver
ϑ_{D}	temperature of the body diode of the partner switch
ϑ_{max}	maximum temperature
ϑ_{min}	minimum temperature
ϑ_{MOS}	temperature of the MOSFET turning on
ϑ_{NTC}	temperature of the NTC sensor
ϑ_{ref}	reference temperature
ϑ_{sp}	temperature set point
$\vartheta_{\mathrm{stress}}$	stress temperature
ϑ_{vj}	virtual junction temperature
$\vartheta_{\mathrm{vj,ANN}}$	virtual junction temperature predicted by an ANN
$\vartheta_{\mathrm{vj,ANN,full,3}}$	virtual junction temperature predicted by an ANN with three hidden neurons and the inverter sensors as input
$\vartheta_{\mathrm{vj,ANN,full,6}}$	virtual junction temperature predicted by an ANN with six hidden neurons and the inverter sensors as input
$\vartheta_{\mathrm{vj,ANN,red,6}}$	virtual junction temperature predicted by an ANN with six hidden neurons without the inverter sensors as input
$\vartheta_{\mathrm{vj,hs}}$	virtual junction temperature of the high side
$\vartheta_{\mathrm{vj,ls}}$	virtual junction temperature of the low side
$\vartheta_{\mathrm{vj,PM}}$	virtual junction temperature predicted by the physics-based model
λ	thermal conductivity
λ_{DIBL}	linear coefficient of the drain-induced barrier lowering
μ_{n}	electron mobility
$\mu_{\mathrm{n,bulk}}$	electron mobility in the bulk
$\mu_{\mathrm{n,ch}}$	electron mobility in the channel
$\mu_{\mathrm{n,eff}}$	effective electron mobility
ξ	ionization degree
ξ_{A}	ionization degree of acceptor atoms
ξ_{D}	ionization degree of donator atoms
σ	mechanical stress, specific conductance or standard deviation
τ_{d}	delay time of the adjusted Foster model
$\tau_{\mathrm{dr,supply}}$	time constant of the driver supply
τ_{g}	time constant of the gate loop
$\tau_{\mathrm{HL,0}}$	high level minority carrier lifetime
Φ_{bulk}	bulk potential
Φ_{c}	potentional assosiated with electron affinity of a semiconductor

Φ_{G}	potentional assosiated with work function of the gate material
Φ_{surf}	surface potential
Φ_{S}	potentional assosiated with work function of a semiconductor
Φ_{vac}	reference potential

Part I

Introduction

1 Introduction

Power electronic devices are one of the key components employed in today's power generation, mobility and manufacturing. These fields have demanding requirements for the reliability of power electronics [1]. In power generation or manufacturing, an unexpected failure of the power electronics leads to a loss of production. In electric vehicles, safety considerations become a major concern, especially when considering the increasing levels of autonomy [2].

Predictive maintenance concepts allow for the scheduled replacement of degraded power electronic components before a failure occurs or to reduce stress and extend their remaining useful lifetime. The first step in applying predictive maintenance is knowing when to expect a failure. This requires "self-aware" components [3] that supply a monitoring signal describing their state of degradation.

Conventional power modules and gate drives do not typically have sufficient, or sufficiently accurate, monitoring capabilities to detect an upcoming module failure in time [4]. This thesis focuses on monitoring techniques that can be added to typical, unmodified power modules to provide information concerning their degradation state.

The objective is the identification of thermomechanical degradation effects based on changes in the switching and conduction characteristics of the power module. Beside the degradation itself, the switching and conduction characteristics of a power module are also affected by the junction temperature of the semiconductors. Separating changes caused by the degradation from those caused by a variation in the junction temperature is challenging. Therefore, the monitoring techniques investigated are usually strongly coupled with determining the junction temperature of the semiconductors.

Temperature-sensitive electrical parameters (TSEPs) are on-line measurements on the module-level that contain information regarding the monitored degradation and the junction temperature simultaneously, e.g., the on-state voltage of a semiconductor. Usually, the degradation of the power module is challenging to detect with a single TSEP and no additional information, as changes in the TSEP may be caused either by the progressive degradation or changes in the junction temperature. Changes in the junction temperature can easily occur if the cooling system is not independent of the environmental conditions or if the cooling system itself shows degradation. Furthermore, the changes in the TSEP due to the degradation or the junction temperature are usually small compared to changes which depend on the operating point of the power electronics, e.g., the load current.

In addition to the previously mentioned challenges of TSEP-based degradation detection or temperature estimation, the monitored switching or conduction characteristics usually depend strongly on the gate driver. A change in the gate driver voltages affects most TSEPs which may be misinterpreted as degradation of the module or a change in the junction temperature. Unfortunately, gate drivers can be considered to be power amplifiers whose temperature and load stabilities are typically not designed to allow high-accuracy measurements of semiconductor characteristics.

The concept of TSEPs has mostly been developed for silicon (Si) semiconductors. Today, the share of wide-bandgap silicon carbide (SiC) semiconductors is increasing in many applications. Power modules with SiC semiconductors typically have much shorter switching times and conduction phases than those with Si semiconductors. Additionally, the faster voltage and current rise and fall times lead to higher electromagnetic interference (EMI). As a consequence, TSEP measurement systems for SiC require a higher bandwidth while simultaneously needing a higher EMI withstand capability.

1.1 Objective

The vision behind this work is the widespread applicability of TSEPs to the thermal and degradation monitoring of power modules with SiC semiconductors. As a contribution to this vision, this thesis has two main objectives.

1. Assessing the applicability of TSEPs to wide-bandgap SiC power modules. TSEP measurement hardware is designed and used to monitor fast-switching SiC power modules. A key aspect is the transition from the TSEP application under laboratory conditions to regular inverter operation.
2. Making TSEP-based temperature estimations less sensitive to unknown parasitic effects, e.g., instabilities of the gate driver voltages or inaccuracies of the load current sensors. To achieve this objective, the possible parasitic impacts are identified, their effect on TSEP-based temperature estimation is determined and methods are developed to counteract their impacts.

1.2 Definitions

In this work, accelerated aging tests are conducted based on the ECPE guideline AQG 324 "Qualification of Power Modules for Use in Power Electronic Converter Units in Motor Vehicles" [5] and IEC 60749-34 "Semiconductor devices - Mechanical and climatic test methods - Part 34: Power-cycling" [6]. This standard and guideline also provide several definitions that are used unaltered or slightly modified throughout this work.

Topological switch AQG 324 defines a half-bridge power module as consisting of two *topological switches*, a high-side topological switch and a low-side topological switch. A topological switch is defined as one or more switches that are paralleled and controlled simultaneously to represent the function of a single switch. In power modules, one topological switch is usually realized as a parallelization of multiple semiconductor chips.

In the context of TSEP-based temperature estimation or degradation detection, the internal structure of a topological switch cannot usually be distinguished from outside the module. Most of the time, the switch type discussed is the topological switch. Within this work, a *topological switch* will simply be referred to as a *switch*. If a further clarification is needed, it will be provided in the text, i.e., by referencing the separate *semiconductor chips*.

Chip-near interconnects *chip-near interconnects* are the electrical connections on the top and bottom sides of a semiconductor chip [5]. This includes bond wire connections, chip solder and other technologies.

Bond connection The bonding contact consists of a variety of different materials, connection points and connection technologies. The term *bond connection* will be used to refer to all relevant components of the chip-near interconnects between the semiconductor surface and the middle of the bond wire [7]. This includes the transition between the semiconductor and its top-side metallization, between the metallization and the bond heel and between the bond heel and the middle of the bond wire.

Virtual junction temperature During operation, the lateral distribution of the junction temperature of a semiconductor chip is typically highly heterogeneous [8]. The *virtual junction temperature* ϑ_{vj} is defined as the junction temperature that was estimated according to the V_{ce}*-method* [8]. This definition is chosen to match the requirements of AQG 324 [5]. The virtual junction temperature is scalar and basically matches the average temperature of the junction.

V_{ce}-method The ECPE guideline AQG 324 directly names the publication [8] as the method for determining the virtual junction temperature. This V_{ce}-method involves the measurement of the virtual junction temperature by injecting a low measurement current through a switch and determining the temperature according to the temperature dependency of the corresponding on-state voltage.

Model fitting parameters In this work, numerous model fitting functions will be presented. Model fitting functions for the quantity f are denoted with an asterisk to become f^*. Each model fitting function f^* has several regression parameters a_i, e.g.,

$$f^*(x) = a_0 + a_1 x + a_2 x^2 + \ldots + a_n x^n, \quad a_i \in \mathbb{R}. \tag{1.1}$$

To avoid the introduction of numerous regression parameter variable names throughout this work, most fit models will use the same variable names a_i. Consequently, the regression parameters a_i are usually *not* the same across different model fitting functions.

1.3 Outline

One option for the use of TSEPs in the context of a condition-monitoring or thermal management system is depicted in Figure 1.1. A conventional monitoring approach is shown in the top row. The inverter sensors for the load current and the dc-link voltage are used to estimate the conduction and switching losses of each power device. The losses are processed in a thermal model to determine the virtual junction temperature. Finally, the temperature waveform of the virtual junction temperature is used in estimations of the remaining useful lifetime.

The bottom row shows the addition of one or more TSEP measurements into the monitoring system. In this work, several TSEPs are acquired and combined to compensate for disturbances caused by external parasitic effects. Many TSEPs have a high sensitivity to the load current. The current measurement of the inverter sensors typically does not include the current ripple, so a detailed current model is needed to determine the instantaneous current conducted by the power device at the time when the TSEP is measured.

In Figure 1.1, the TSEPs are combined and evaluated to yield a single temperature estimate $\vartheta_{\mathrm{vj}}^{(\mathrm{TSEP})}$, which is provided to a tracking filter to merge the TSEP-based temperature

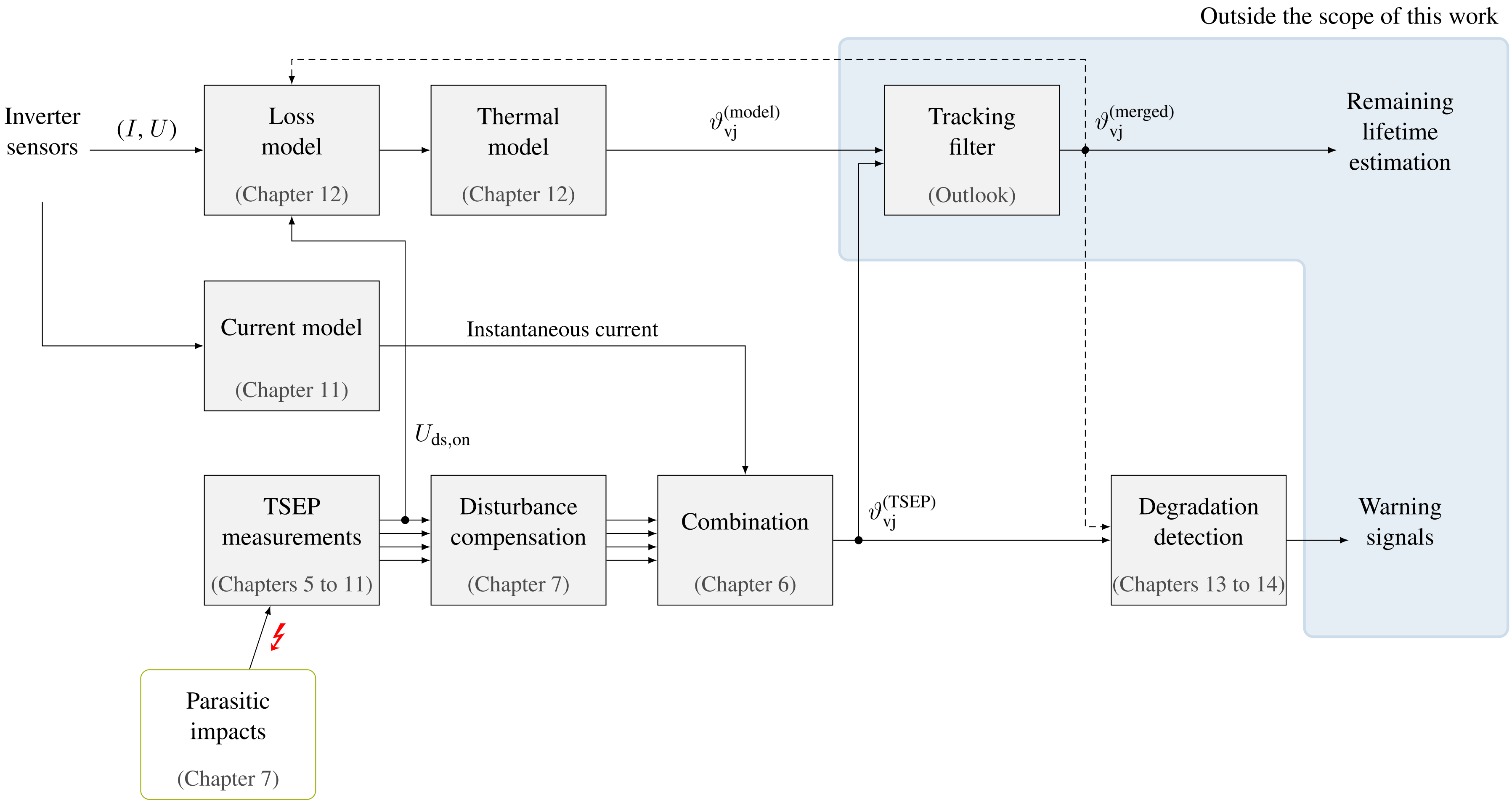

Figure 1.1: TSEPs in the context of a condition-monitoring system; the corresponding chapters in this work are listed in each block

estimate with the model-based temperature estimate $\vartheta_{\mathrm{vj}}^{(\mathrm{model})}$. Depending on the tracking filter used, e.g., an extended Kalman filter, the raw TSEP measurements themselves can be provided to the tracking filter for use in a predictor-corrector method.

The TSEPs represent on-line measurements and can therefore be used to detect degradation of the power module, either directly from the TSEP measurements or by monitoring discrepancies between the temperature predicted by a model $\vartheta_{\mathrm{vj}}^{(\mathrm{model})}$ and estimated from the TSEPs $\vartheta_{\mathrm{vj}}^{(\mathrm{TSEP})}$.

> **Remark:** Creating a well-designed tracking filter is highly complex and will be omitted from the scope of this work. It is important to note that none of the methods presented in this work are designed to substitute for subsequent tracking filters. The methods do not require more than one set of samples, i.e., there are no filters employed and no more than a single set of TSEP samples is used[1]. All developed methods can be applied before using the TSEP measurements in subsequent tracking filters. Therefore, this work constitutes an addition to the preprocessing of TSEPs and may be added to existing tracking filters.

1.3.1 Chapter overview

This work is split into four parts. After the introduction, preparatory work using insulated-gate bipolar transistor (IGBT) power modules is presented in Part II. At the time of the investigations, these modules were available. The IGBT power modules have a higher power rating and slower switching times than the SiC power modules used for the subsequent parts. The presented concepts are transferable.

In Part III, semiconductor models for generic Si and SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) are investigated with respect to their suitability for TSEP-based temperature estimations. Although the results in this part are validated using the SiC power modules, the results are mostly applicable to all MOSFETs. Nevertheless, the more detailed effects focus on short-channel SiC MOSFETs.

The TSEP measurement system for SiC power modules, the modules themselves and the conducted accelerated aging tests are presented in Part IV. This part is the main part of this work.

Part I - Introduction

Chapter 2 - Degradation of power modules An overview of the structure of power modules, typical degradation mechanisms and their physical manifestations is presented. Lifetime models and general concepts for condition monitoring are discussed.

Chapter 3 - Temperature-sensitive electrical parameters This chapter provides an introduction to a variety of TSEP measurements.

Chapter 4 - Overview of the mathematical concepts used Concepts for linear and non-linear fitting problems and the training of artificial neural networks (ANNs) are introduced.

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[1] Except for the thermal model used to provide a reference temperature

Part II - Preparatory work with Si IGBTs

Chapter 5 - System overview Although this work focuses on SiC devices, some concepts were developed using Si IGBT modules. In this chapter, the selection of a set of multiple TSEPs and a corresponding measurement concept is outlined. An introduction to the hardware design for TSEP measurement systems is provided.

Chapter 6 - Combining multiple TSEPs After a system which acquires four TSEPs has been presented, different approaches to combining these measurements into a single temperature estimate are investigated, focusing on the suitability of ANNs for this task.

Chapter 7 - Parasitic impacts Furthermore, parasitic impacts on TSEPs are identified, e.g., changes in the driver voltages. Their impact on the temperature estimation is quantified. Methods for reducing these impacts are shown.

Part III - TSEP models for Si and SiC MOSFETs

Chapter 8 - On-state voltage State-of-the-art analytical models for the first investigated TSEP are summarized from literature. Only models for MOSFETs are considered. This chapter begins with models of generic device properties, applicable to Si and SiC devices alike. Afterwards, the models are extended with effects specific to the SiC material, the current SiC manufacturing process and the used type of MOSFET, i.e., a short-channel MOSFET.

Numerous model variants and levels of detail are then fitted to measured data from multiple modules. It is assessed what level of model complexity is needed to appropriately describe the temperature and current dependencies of the TSEPs.

Chapter 9 - Turn-on times This chapter is analogous to Chapter 8, but analyzes the second type of investigated TSEPs.

Part IV - TSEP measurement system for SiC MOSFETs

Chapter 10 - TSEP measurement hardware for SiC MOSFETs An elaborate discussion of the implemented TSEP measurement hardware and the TSEP acquisition, with regard to the investigated SiC devices, is presented.

Chapter 11 - Turn-on current estimation A current model that maps the scalar current measurement from the inverter sensor to the instantaneous current at the turn-on of the switches is designed.

Chapter 12 - Thermal characterization The power module and the test setup are characterized by a thermal impedance measurement. The thermal model includes cross coupling between the switches or to the module temperature sensor. A loss model for continuous pulse-width modulation (PWM) operation is described. The thermal impedance model is used to generate a reference of the virtual junction temperature. The TSEP-based temperature estimations are compared to this reference.

Chapter 13 - Emulated solder degradation The TSEP measurement system is validated against an emulated degradation, and it is validated whether or not the TSEP system could be used for degradation detection.

Chapter 14 - Accelerated aging tests Accelerated aging tests with seven power modules are conducted until they reach their end of life. The modules are periodically analyzed using the TSEP measurement system. It is assessed whether the TSEP system could be used to detect realistic thermomechanical degradation effects.

Chapter 15 - Current rise time at unequal junction temperatures One of the investigated TSEPs corresponds to the current rise time. This measurement depends on the temperature of both switches in a half-bridge. In this chapter, the temperature dependency of this TSEP is investigated when the two switches are at different temperatures.

2 Degradation of power modules

During its lifetime, a power module is stressed by a variety of external impact factors, e.g., temperature, corrosion or mechanical vibrations [9]. All these stresses degrade the module simultaneously and trigger different failure mechanisms. Nevertheless, a power module model, in conjunction with a specific mission profile, typically fails due to one dominant failure mechanism first [1, 9]. This work focuses on thermomechanical wear-out processes only. The two selected degradation mechanisms of interest are the degradation of the bond connections and the degradation of the solder layers. Failures of the gate insulation, manufacturing defects and failures due to overstress are not considered in this work. In this chapter, the basic construction of a power module is outlined. Afterwards, several known thermomechanical degradation processes will be briefly discussed.

The cross-section of a typical power module is shown in Figure 2.1. Power modules consist of a multilayer structure. Different materials are required to provide electrical interconnections, thermal conductivity, electrical insulation and mechanical stability.

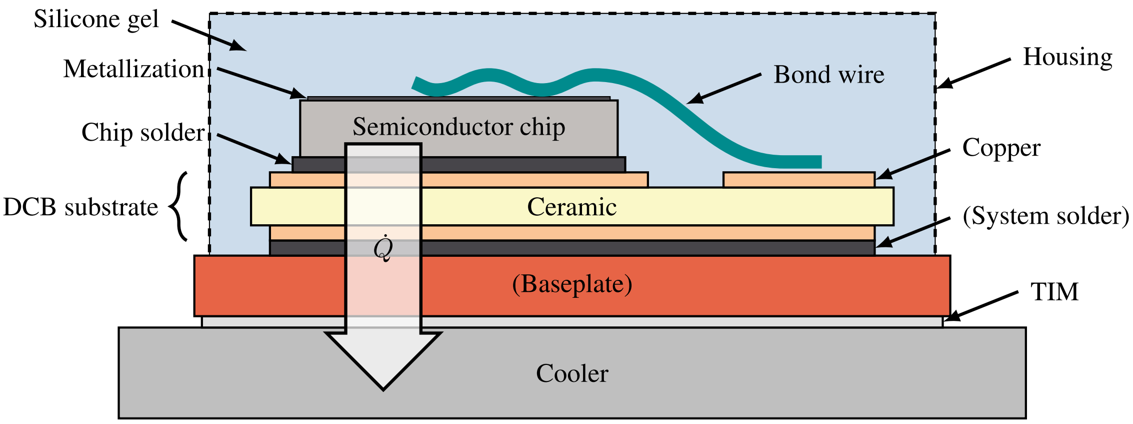

Figure 2.1: Cross-section of a typical power module according to [7]; the electrical connections of the module are not shown

The semiconductor chips are soldered onto a direct-copper-bonded (DCB) substrate using the chip solder. On the top side of the semiconductors, bond wire connections are formed using ultrasonic wedge bonding [7]. The DCB substrate consists of a ceramic insulator with copper layers on both sides for contacting. In large power modules, the bottom of the DCB is soldered onto a larger baseplate using the system solder. Multiple DCB substrates can be placed on a single baseplate. The bottom of the baseplate usually defines the outer limits of the module. On top of the DCB substrate, semiconductors and bond wires are usually sealed with a silicone gel and a housing. With regard to reliability, the silicone gel hinders humidity from reaching the semiconductors and reduces the mechanical vibrations of the otherwise exposed bond wires.

The module is mounted on a cooler. A thermal interface material (TIM) is applied between the module and the cooler to fill possible cavities that would otherwise significantly increase the thermal resistance of the interface. The TIM can be a thermal paste or foils, depending on the application.

In this work, large IGBT power modules based on silicon are investigated and small MOSFET modules based on silicon carbide. The investigated SiC MOSFET modules do not include a baseplate or system solder. Instead, the bottom surface of the DCB substrate is directly mounted on the cooler with TIM.

2.1 Thermomechanical degradation effects

During operation of the power module, losses are generated in the semiconductors. The thermal power flow $\dot{Q}$ is mainly transported vertically through the DCB substrate to the cooler, heating up the different layers of the module. Each layer expands according to the product of its temperature increase and its coefficient of thermal expansion (CTE). The variety of materials used leads to a CTE mismatch [7] and shear stresses occur at the material interfaces [9]. Thermal cycling in particular degrades the material interfaces [10].

In typical industrial applications, an Al_2O_3 ceramic is used as the DCB substrate and copper as the baseplate. In traction drives, an AlN ceramic and an AlSiC baseplate can be employed, resulting in a smaller CTE mismatch [7]. Even a module with perfectly matched CTEs would experience shear stresses, due to the temperature gradiant across the module [11].

2.1.1 Degradation of the bond connection

Bond wires are usually made from aluminum, although copper bond wires can be used in high-power applications [7]. The bond wires are attached to the top of the semiconductors using ultrasonic wedge bonding [7]. The surface of the semiconductor is metallized with an aluminum layer for compatibility [12]. Bond wire diameters are typically in the range of 300 µm to 500 µm and conduct a current of up to 10 A each [13].

At the contact point of the semiconductor metallization and the bond heel, the bond wire experiences the entire temperature swing of the semiconductor, plus a temperature swing due to its own conduction losses. At the point where the bond wire is connected to the copper layer of the DCB substrate, the thermal swing is much smaller, and bond connection failures typically do not occur there [13].

Bond wire lift-off At the point of contact between the metallization and the bond wire, portions of each material diffuse into the other, forming a polycrystalline alloy. If the shear stresses due to the thermal expansion exceed the limits of elastic deformation, an irreversible degradation of the connection occurs. A crack starts to form at the edges of the connection and grows inwards along the grain boundaries. The grain size at the contact point is smaller than in the bond wire itself [14]. Here, the growth of a crack is interrupted more frequently by the changing orientation of the grain boundaries, and therefore the crack typically forms in the bond wire slightly above the bond wire connection [14, 15]. Ultimately, a bond wire lift-off is caused, as shown in Figure 2.2.

Bond wire heel cracking Bond wire heel cracking can occur due to cyclic changes in the bond wire shape. When the temperature of the bond wires increases, this leads to their thermal expansion. The bond wire's start and end locations are fixed, and therefore the

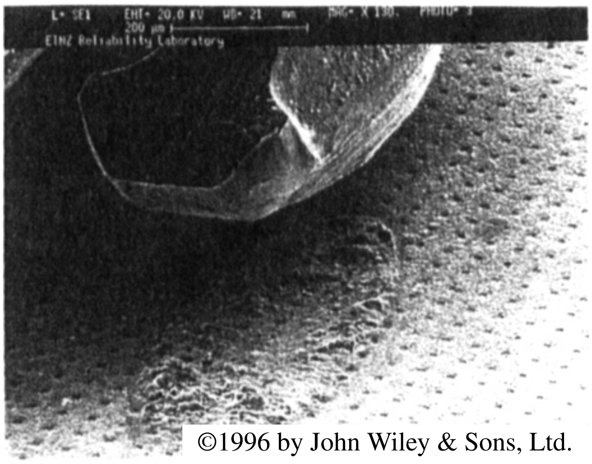

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Figure 2.2: Example of a bond wire lift-off [16]

shape of the bond wire's arc changes. The largest change in bond wire angle occurs at the fixed bonding locations [13]. Repeated cycling ultimately leads to a crack that generally originates at the heel, as shown in Figure 2.3. This type of failure can also occur at the bond wire end which is welded to the copper of the DCB substrate, if the bond wire exhibits high self heating [13].

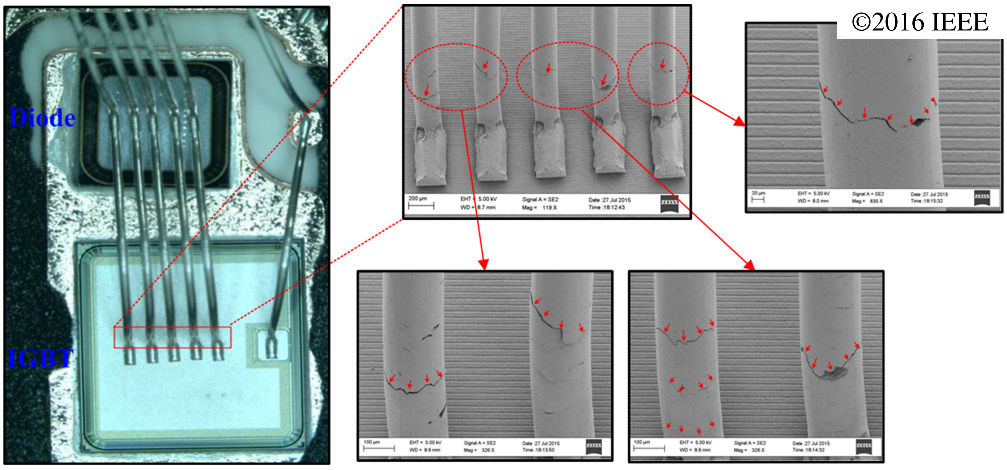

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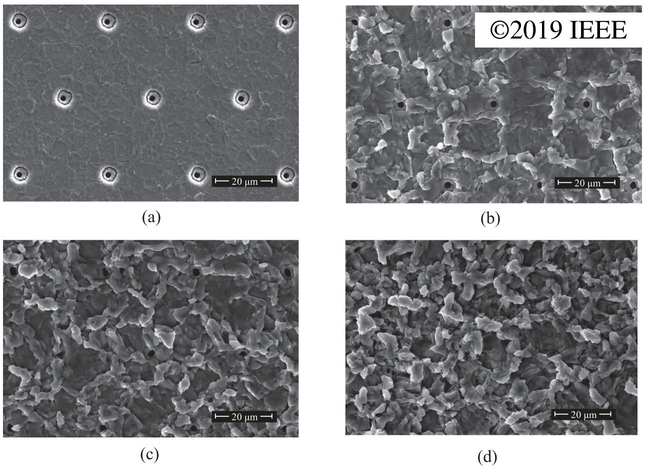
Figure 2.3: Heel cracks in bond wire connections [17]

Metallization reconstruction In a similar way to the bond wire to metallization contact, the contact between the metallization and the semiconductor is also stressed during operation. The thermal expansion cycles of the semiconductor lead to diffusion creep, grain boundary sliding and plastic deformation [16]. The semiconductor metallization becomes rough (reconstructed) [16], degrading the electrical contact, as can be seen in Figure 2.4. When stressed, the elastic deformation region in the metallization must be exceeded in order to cause a noteworthy reconstruction of the metallization, which typically occurs where the junction temperature of the device exceeds 120 °C [19]. The temperature of the semiconductors is much higher in the center of the chips [8], therefore the reconstruction happens more significantly at the center of the chips [13], see Figure 2.5. Additionally, the local



(a) (b) (c) (d)

Figure 2.4: Scanning electron microscopy images of an aluminum metallization layer at different aging stages [18]

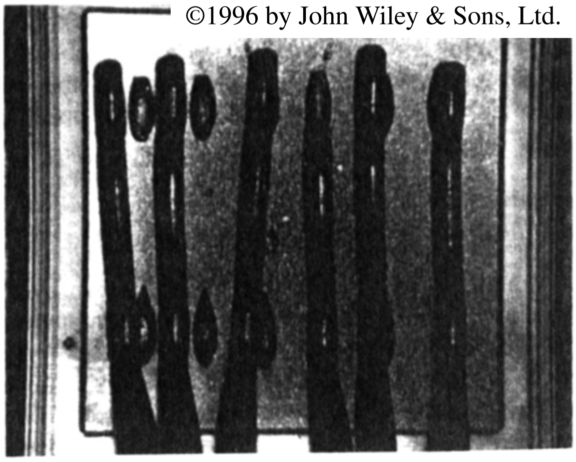

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Figure 2.5: Reconstructed metallization of an aged semiconductor [16]; areas darken as the reconstruction progresses because the surface becomes rougher

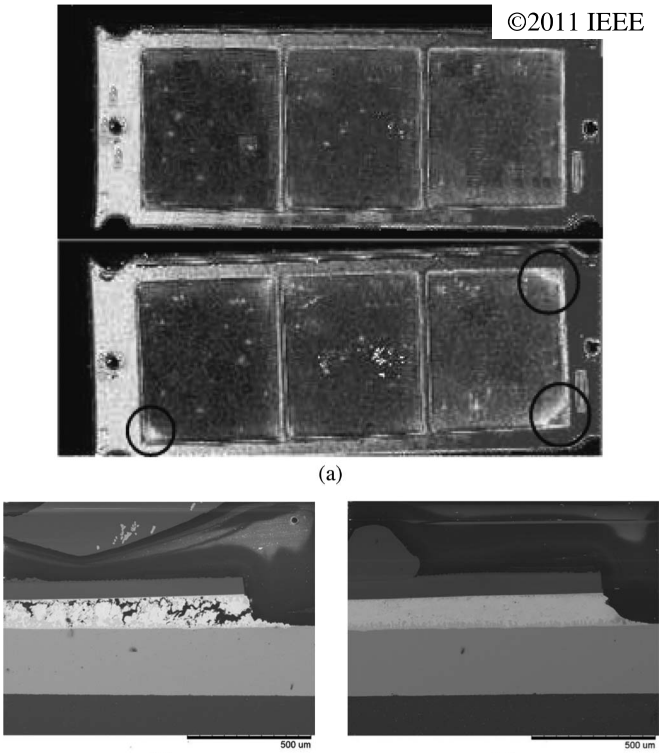
temperature underneath the bond wire contacts is higher than at other locations, causing the metallization reconstruction to be accompanied by a bond wire lift-off as a secondary mechanism [13]. This can also be seen in the more advanced metallization reconstruction below the bond wire shown in Figure 2.2. In contrast to the bond wire lift-off and heel cracking, this effect typically leads to a slow increase in the on-state voltage over a longer time.

In the course of this work, bond wire lift-off, bond wire heel cracking and the reconstruction of the metallization will generally be referred to as bond connection degradation.

2.1.2 Solder degradation

Solder degradation describes the growth of cracks and voids in the solder, due to the thermal expansion cycles of the solder and the two bonded materials. Although voids can occur anywhere in the solder area, the degradation typically starts in the corners of the solder area, as this is where the mechanical stress is highest [20].

Predominantly, the temperature cycling and the corresponding solder creep will affect the



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(a)

(b) (c)

Figure 2.6: Solder degradation [10]; (a) the delamination starts in the corners of the system solder, (b) cross-section of an aged corner, (c) cross-section of an intact solder corner

soldered connection [21]. The voids and cracks generated reduce the thermal conductivity of the solder. In a power module, this type of degradation directly increases the junction temperature of the semiconductors, accelerating the aging process.

Solder creep Creep describes a situation in which the material does not stop deforming as long as a constant stress is applied, see Figure 2.7. A set of independent mechanisms that take place concurrently in the material make up the total creep rate [23]. The different mechanisms can have different nonlinear dependencies on the applied stress. The absolute strain ε at which they are relevant and the maximum strain they can provide varies.

Creep is divided in primary, secondary and tertiary creep. During the primary creep phase, the solder is deformed easily. The transition from primary to secondary creep occurs when some of the mechanisms contributing to the creep, e.g., hardening of the material due to plastic deformation, have been fully depleted and stop contributing. The creep rate $\frac{\mathrm{d}\varepsilon}{\mathrm{d}t}$ then stays constant during the secondary creep phase. Tertiary creep corresponds to a sudden increase in the creep rate, e.g., corresponding to necking effects.

The total strain of a material is the sum of the elastic strain, plastic strain and creep over time. According to [21], plastic deformation can be neglected in solder lifetime calculations, as it is negligible compared to the creep.

Stress-strain relationship Grivas *et al.* showed that the two relevant mechanisms for solder are conventional and superplastic deformation [24]. Several models for the constant secondary creep rate $\frac{\mathrm{d}\varepsilon_{\mathrm{s}}}{\mathrm{d}t}$ of solder are available [21]. The two most relevant [25] are the

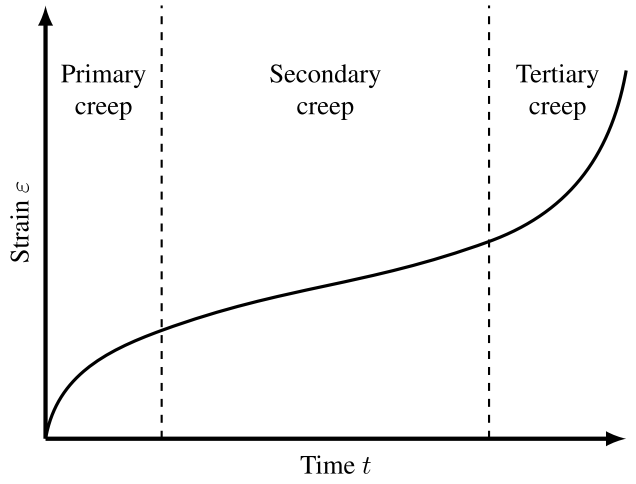

Figure 2.7: Strain over time with different stages of creep according to [22]

double-power-law approach (2.1) and the hyperbolic sine creep model (2.2)

$$\text{Schubert } et\ al.\ [26]: \quad \frac{\mathrm{d}\varepsilon_{\mathrm{s}}^{(\mathrm{PL})}}{\mathrm{d}t} = a_0\sigma^{a_1}\mathrm{e}^{\frac{-a_2}{R_{\mathrm{gas}}\vartheta}} + a_3\sigma^{a_4}\mathrm{e}^{\frac{-a_5}{R_{\mathrm{gas}}\vartheta}}, \quad a_i \in \mathbb{R} \tag{2.1}$$

$$\text{Wiese } et\ al.\ [27]: \quad \frac{\mathrm{d}\varepsilon_{\mathrm{s}}^{(\mathrm{sinh})}}{\mathrm{d}t} = a_0 \sinh\left(a_1\sigma\right)^{a_2}\mathrm{e}^{\frac{-a_3}{R_{\mathrm{gas}}\vartheta}}, \quad a_i \in \mathbb{R}. \tag{2.2}$$

The model includes the universal gas constant R_{gas}, the temperature ϑ and the applied mechanical stress σ. The power-law approach provides good results for lead-based solder while the hyperbolic sine is better suited to lead-free solder [25].

The primary creep $\varepsilon_{\mathrm{p}}(t)$ can then be prepended as an exponential term according to [23]

$$\varepsilon(t) = \varepsilon_{\mathrm{p}}(t) + \frac{\mathrm{d}\varepsilon_{\mathrm{s}}^{(\mathrm{PL})}}{\mathrm{d}t}t \tag{2.3}$$

$$= \varepsilon_{\mathrm{sat}}\left(1 - \exp\left(-K\left(\frac{\mathrm{d}\varepsilon_{\mathrm{s}}^{(\mathrm{PL})}}{\mathrm{d}t}t\right)^n\right)\right) + \frac{\mathrm{d}\varepsilon_{\mathrm{s}}^{(\mathrm{PL})}}{\mathrm{d}t}t, \tag{2.4}$$

$$\varepsilon_{\mathrm{sat}}, K > 0, n \in \mathbb{R}. \tag{2.5}$$

Impact of thermal cycling Immediately after applying a mechanical stress to the solder, it creeps quickly due to the thermal expansion of the materials. The creep rate $\frac{\mathrm{d}\varepsilon}{\mathrm{d}t}$ per unit stress σ decreases over time while simultaneously the creep ε, or the expansion of the solder, relieves the mechanical stress on the solder. Therefore, the creep process slowly approaches an upper limit of the total solder expansion. When the mechanical stress changes, i.e., due to a cooling down of the contact materials, the process starts anew, starting with a high creep rate. As a consequence, thermal cycles have a major impact on solder degradation.

Further details of thermomechanical failure mechanisms in power modules can be found in [9, 10, 13, 28].

2.2 Lifetime models

Lifetime tests must be conducted much faster than the actual lifetime of a power module. Accelerated aging tests are used to quickly cause module degradation that is equivalent to the degradation at the end of the module's lifetime. During accelerated aging tests, the modules are subjected to a higher stress than they experience during their regular life cycle, thereby inflicting more degradation per unit time. Power-cycling tests are often used in this context, where the semiconductors are repeatedly heated with a high heating current and then cooled down. The parameters are chosen to cause a high temperature swing. Details of accelerated aging tests, specifically power-cycling tests, are discussed in Chapter 14.

The stress cycles used in the tests must be mapped to the actual expected lifetime of the module, for which lifetime or accelerated aging models are used. There are different lifetime models for different types of aging mechanism. Two generic lifetime models relevant to the thermomechanical degradation mechanisms described are the Arrhenius model and the Coffin-Manson model [7]

$$\text{Arrhenius model:} \quad N_\text{f} \propto \exp\left(\gamma\left(\frac{1}{\vartheta_\text{ref}} - \frac{1}{\vartheta_\text{stress}}\right)\right), \quad \gamma < 0, \tag{2.6}$$

$$\text{Coffin-Manson model:} \quad N_\text{f} \propto \left(\frac{\Delta\vartheta_\text{stress}}{\Delta\vartheta_\text{ref}}\right)^c, \quad c < 0. \tag{2.7}$$

These describe the number of stress cycles N_f which may be applied before a predefined degradation limit is reached at the given stress level. The Arrhenius model describes processes that require an activation energy that must be overcome and can be used to model reaction rates. These processes typically accelerate with increased temperature [29].

The Coffin-Manson model can be used to describe material fatigue and cyclic mechanical loading. In Section 2.1.2, it was discussed how the thermal cycling and the corresponding material expansion lead to cyclic mechanical stress on the solder and bond wire connections. Therefore, the Coffin-Manson model can be applied to the thermomechanical aging mechanisms considered in this work.

In [30], the LESIT[1] model was presented. It is a descriptive model for the lifetime of power modules based on empirical data from a single module type. During the experiments, the lifetime of power modules at different thermal-cycle temperature swings $\Delta\vartheta$ and at different average temperatures $\overline{\vartheta}$ was measured. The data was fitted using a model function that combines the Arrhenius model and the Coffin-Manson model

$$\text{LESIT model:} \quad N_\text{f} \propto \left(\frac{\Delta\vartheta}{1\,\text{K}}\right)^\alpha \exp\left(\gamma\left(\frac{Q}{R_\text{gas}\overline{\vartheta}}\right)\right), \quad Q > 0, \alpha < 0, \gamma < 0. \tag{2.8}$$

The parameter Q corresponds to the activation energy which must be overcome to trigger an aging mechanism. The LESIT model combines the dependency on the thermal-cycle temperature swings $\Delta\vartheta$ and the average temperature $\overline{\vartheta}$ at which the modules are operated. When the parameters are known, the model also allows an assessment of which of the average temperature or the size of the thermal swings is most relevant for the aging. It can also be used to determine whether it is beneficial to operate at a higher average temperature, if the size of the thermal swings can be reduced in turn, e.g., by increasing the losses in a device during a low-load time. See *active thermal management* for details [31].

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[1] Named after the project framework it was developed in

There are test parameters that are not included in the LESIT model. As described in Section 2.1.2, the duration of a mechanical stress impacts the inflicted degradation per cycle, with regard to the creep rate. In [32], the CIPS2008 model was presented

$$\text{CIPS2008 model:}\quad N_\mathrm{f} \propto \left(\frac{\Delta\vartheta}{1\,\mathrm{K}}\right)^{\beta_1} \exp\left(\frac{\beta_2}{\frac{\vartheta_\mathrm{min}}{1\,\mathrm{K}}}\right) \left(\frac{t_\mathrm{on}}{1\,\mathrm{s}}\right)^{\beta_3} \left(\frac{I}{1\,\mathrm{A}}\right)^{\beta_4} \left(\frac{V}{1\,\mathrm{V}}\right)^{\beta_5} \left(\frac{D}{1\,\mathrm{m}}\right)^{\beta_6}, \tag{2.9}$$

$$\beta_1, \beta_3, \beta_4, \beta_5, \beta_6 < 0, \beta_2 > 0.$$

It is an extended model compared to the LESIT model and was determined based on empirical lifetime data of different module types and stress conditions. The CIPS2008 model includes additional stress parameters, like the duration of the applied stress t_on and the magnitude of the heating current. Interestingly, the relevant current is not the total current conducted by the module nor the current per bond wire, but the current I per bond wire foot [32]. Additionally, the model includes specific power module parameters, like the bond wire diameter D, and the voltage class V of the module. The voltage class is not directly relevant, but it correlates with the chip thickness [32]. The exponent β_6, corresponding to the bond wire thickness, was determined to be negative. This was accounted to the larger bond interfaces on the chip and the resulting greater absolute differences in the thermal expansion [32] when using thicker bond wires. In [32], it is also discussed whether the minimum, maximum or average temperature should be used in the Arrhenius term $\exp\left(\frac{\beta_2}{\vartheta}\right)$. When using an existing model, these temperatures can be used interchangeably if the coefficients β_i are adjusted accordingly

$$\overline{\vartheta} = \frac{\vartheta_\mathrm{max} + \vartheta_\mathrm{min}}{2}, \quad \Delta\vartheta = \vartheta_\mathrm{max} - \vartheta_\mathrm{min}, \quad \vartheta_\mathrm{min} = \overline{\vartheta} - \frac{\Delta\vartheta}{2}. \tag{2.10}$$

However, when fitting the model parameters to measured data, the correlation between temperature swing $\Delta\vartheta$ and the temperatures $\overline{\vartheta}, \vartheta_\mathrm{min}$ and ϑ_max in the data set should be considered [32]. An aging test with a high temperature swing $\Delta\vartheta$ often leads to a high maximum temperature or high average temperature as well. For the data used in [32], the lowest correlation was observed between $\Delta\vartheta$ and ϑ_min, and therefore the use of ϑ_min for the Arrhenius term was suggested when fitting.

Compared to the LESIT model, the CIPS2008 model can be used to assess the impact of changing durations and stress levels, and also to compare data from similar power module models.

Lifetime models for varying loads The lifetime models presented so far describe the number of stress cycles before a predefined degradation limit is reached. The parameters of one stress cycle are kept as constant as possible in these tests.

These lifetime models need to be projected on a realistic load profile with changing stress levels, e.g., changing wind conditions experienced by a wind turbine or the driving cycle of a vehicle. Cycle counting is a methodology used to accumulate the impact of stress cycles of varying magnitude. The definition of a cycle depends on the counting method. One of the most commonly used [4, 33–36] algorithms is the rainflow counting method, standardized in ASTM E1049-85 [37]. It extracts the closed cycles a material experiences on a stress-strain curve. Each of the extracted cycles is weighted with a corresponding used lifetime according to the lifetime models and subtracted from the estimated remaining useful lifetime.

2.2.1 Severity of temperature swings versus average temperature

Parameter values for β_1 to β_6 were published for the CIPS2008 model [32], which allows a quantified assessment of the regions in which it is beneficial to trade a higher minimum temperature ϑ_{min} for smaller temperature swings $\Delta\vartheta$. This investigation assumes that the module is kept the same, while only the thermal parameters are changed. Therefore, only the Arrhenius and Coffin-Manson terms are relevant. Let the acceleration factor a_{f} be inversely proportional to the number of stress cycles N_{f} before a predefined degradation limit is reached [7]. Using the acceleration factor a_{f} yields

$$
\begin{aligned}
a_{\mathrm{f}} &\propto N_{\mathrm{f}}^{-1}, && (2.11)\\
a_{\mathrm{f}} &:= \left(\frac{\Delta\vartheta}{1\,\mathrm{K}}\right)^{-\beta_1} \exp\left(\frac{-\beta_2}{\frac{\vartheta_{\mathrm{min}}}{1\,\mathrm{K}}}\right), && (2.12)\\
\beta_1 &= -4.416 \pm 0.281 \quad [32], && (2.13)\\
\beta_2 &= 1284 \pm 269 \quad [32].
\end{aligned}
$$

The specific definition of the confidence interval in (2.13) and (2.14) could not be found in [32]. For simplicity, the coefficient of proportionality is set to unity. A contour plot of the normalized acceleration factor a_{f}' is shown in Figure 2.8. Any movement along the contour lines does not impact the aging rate of a module. An arbitrary operating point is marked on the diagram, with possible changes to the cooling system shown as vectors. Case A

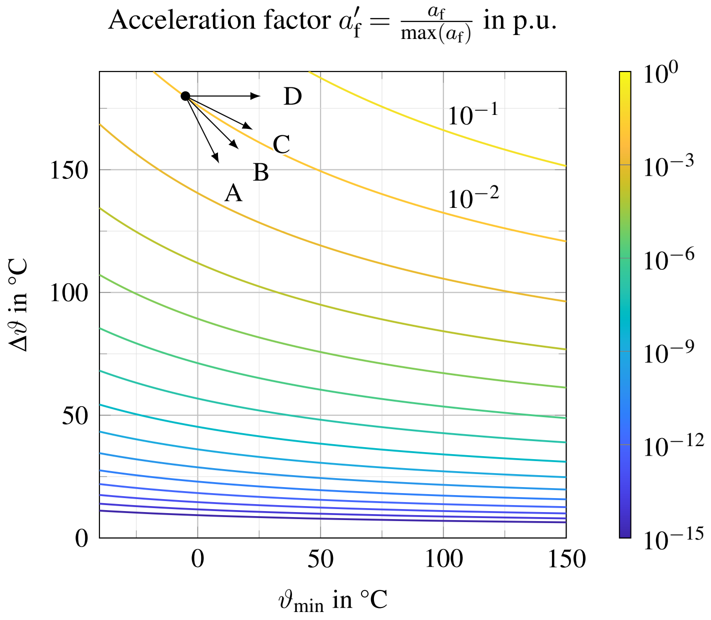
Acceleration factor $a_{\mathrm{f}}' = \frac{a_{\mathrm{f}}}{\max(a_{\mathrm{f}})}$ in p.u.

Figure 2.8: Contour plot of the normalized acceleration factor a_{f}'; the values are normalized to the maximum acceleration factor occurring in the range shown. An arbitrary operation point is marked by a dot. Four cases for possible changes to the cooling system are shown as vectors. Contour lines are spaced logarithmically with a distance of 10^1.

illustrates a situation in which the temperature swing $\Delta\vartheta$ can be lowered while the minimum temperature ϑ_{min} is only slightly increased. Case D shows a situation in which only the average temperature of the system is raised. Whether or not a movement along the contour lines is possible depends on specific changes that can be made to the cooling system and will be discussed in the further parts of this chapter.

Condition for lifetime improvement Using a first-order Taylor approximation, a change Δa_{f} in the acceleration factor, depending on changes $\Delta\vartheta_{\text{min}}$ in the minimum temperature and changes $\Delta(\Delta\vartheta)$ in the temperature swing $\Delta\vartheta$, can be described as

$$\Delta a_{\text{f}} = \frac{\partial a_{\text{f}}}{\partial \vartheta_{\text{min}}} \Delta\vartheta_{\text{min}} + \frac{\partial a_{\text{f}}}{\partial \Delta\vartheta} \Delta(\Delta\vartheta)\,. \tag{2.14}$$

The expected lifetime of the module can be increased if the change in the acceleration factor is negative

$$\Delta a_{\text{f}} \overset{!}{<} 0 \tag{2.15}$$

$$\frac{\partial a_{\text{f}}}{\partial \vartheta_{\text{min}}} + \frac{\partial a_{\text{f}}}{\partial \Delta\vartheta} \frac{\Delta(\Delta\vartheta)}{\Delta\vartheta_{\text{min}}} < 0 \tag{2.16}$$

$$\frac{\Delta(\Delta\vartheta)}{\Delta\vartheta_{\text{min}}} < -\frac{\frac{\partial a_{\text{f}}}{\partial \vartheta_{\text{min}}}}{\frac{\partial a_{\text{f}}}{\partial \Delta\vartheta}} = \frac{\beta_2 \Delta\vartheta}{\vartheta_{\text{min}}^2 \beta_1}, \quad \beta_1 < 0 \tag{2.17}$$

$$\Leftrightarrow \quad \Delta\vartheta < \frac{\vartheta_{\text{min}}^2 \beta_1}{\beta_2} \frac{\Delta(\Delta\vartheta)}{\Delta\vartheta_{\text{min}}}, \tag{2.18}$$

$$\text{with } \Delta\vartheta_{\text{min}}, \Delta\frac{\partial a_{\text{f}}}{\partial \Delta\vartheta} > 0 \text{ and } \frac{\beta_2}{\vartheta_{\text{min}}^2 \beta_1} < 0. \tag{2.19}$$

The relational operator switches in (2.18) since β_1 is negative, as stated in (2.13). The ratio $\frac{\Delta(\Delta\vartheta)}{\Delta\vartheta_{\text{min}}}$ depends on the changes that are made to the system or its operation. Only negative values of $\frac{\Delta(\Delta\vartheta)}{\Delta\vartheta_{\text{min}}}$ are considered here, as the impact of increasing or decreasing ΔT and ϑ_{min} simultaneously is obvious. Furthermore, only an increase in the minimum temperature $\Delta\vartheta_{\text{min}} > 0$ is considered here to assess whether an increase in $\Delta\vartheta_{\text{min}}$ is beneficial. The answer to the negated question, whether or not it is beneficial to reduce the minimum temperature $\Delta\vartheta_{\text{min}} < 0$ while increasing the temperature swing $\Delta(\Delta\vartheta) > 0$ is given intrinsically. The remaining conditions in (2.19) are fulfilled.

Cases of possible changes to the cooling system Three cases of conceivable changes in the temperature swing and the minimum temperature are illustrated in Figure 2.9, in order to determine realistic values for $\frac{\Delta(\Delta\vartheta)}{\Delta\vartheta_{\text{min}}}$ and the corresponding practical changes to the cooling system or the cooling strategy which would be required. In case A, the thermal capacitance of the system is increased, without increasing the thermal resistance. Thus, the temperature swing $\Delta\vartheta$ is reduced, while the average temperature $\overline{\vartheta}$ is unchanged. In case B, the cooling system is unmodified, but the power device is heated during the cooled-down phases to reduce the temperature swing. Case C represents a situation where the thermal capacitance of the cooling system is increased, while also increasing the thermal resistance, e.g., by using a thicker cooler. In the example shown, the maximum temperature ϑ_{max} only rises half as much as the minimum temperature ϑ_{min}. Case D shows the edge case

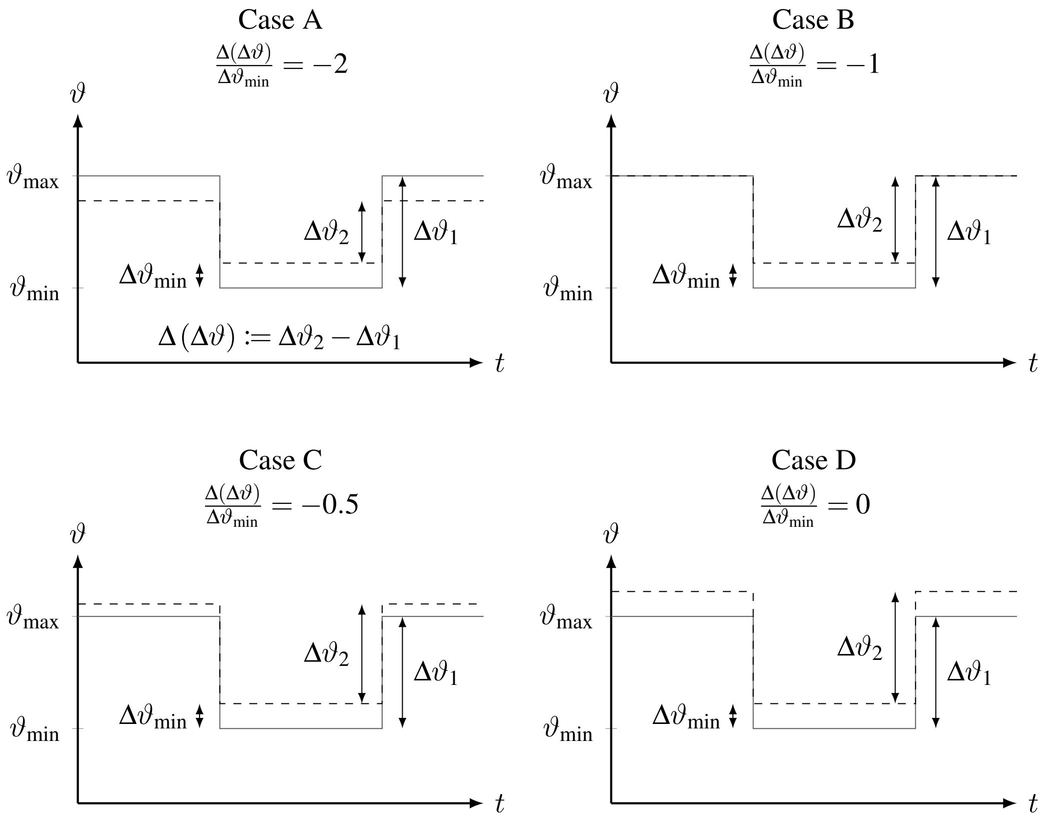

Figure 2.9: Different cases of changes in the system or its operation affecting the temperature swing $\Delta\vartheta$ and the minimum temperature $\vartheta_{\min}$; the cases match the labels in Figure 2.8; reference is a solid line, modified temperature curve is dashed

of useful system modifications. The minimum temperature is increased and the maximum temperature increases by the same value, thus shifting the temperature curve upwards.

Beneficial trade-offs Finally, Figure 2.10 shows the regions in which it is beneficial to increase the minimum temperature $\vartheta_{\min}$ in order to reduce the temperature swing $\Delta\vartheta$. The safe operating area (SOA) is split into two areas according to (2.19). The characteristic depends on the ratio $\frac{\Delta(\Delta\vartheta)}{\Delta\vartheta_{\min}}$ that can be achieved. Case B represents a situation where the power module is heated during idle time, without increasing the maximum junction temperature. With regard to the module lifetime, heating during the idle time is almost always beneficial within the SOA, as long as the maximum temperature is not increased. If the maximum junction temperature is also increased, i.e., $\frac{\Delta(\Delta\vartheta)}{\Delta\vartheta_{\min}} > -1$, the results depend on the initial operating point.

> **Remark:** The parameters β_i provided in [32] target 1200 V IGBT4 modules by Infineon. The underlying data set consists of approximately 170 data points. It includes semiconductors in voltage classes from 600 V to 3300 V, bond wire currents from 3 A to 23 A, as well as seven bonding technologies and packages. Due to the large data set and wide range of parameters, it is expected that the parameters provided can be used to estimate degradation of similar modules. Transferring the results to other types of devices depends on the comparability of the bonding, soldering and other packaging techniques.

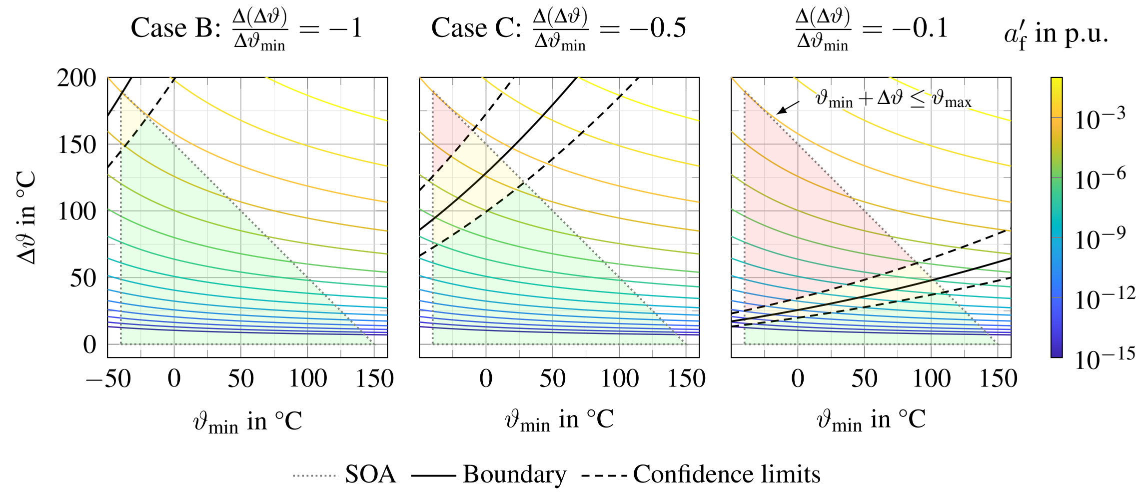

Figure 2.10: Regions where increasing the minimum temperature to reduce the temperature swing is beneficial (green) and not beneficial (red); Compare Figure 2.9 for case examples; Case A not shown; the yellow region marks the area where the result is unknown due to the confidence intervals of the parameters β_1 (2.13) and β_2 (2.14) [32]; contour lines are spaced logarithmically with a distance of 10^1

2.3 Concepts for thermal monitoring

Thermal monitoring requires knowledge of the temperature of the monitored device. The temperatures relevant for power modules can be obtained through measurement or model-based approaches.

2.3.1 Temperature sensing

Module-integrated NTC temperature sensor A temperature sensor can be used to gather information about the junction temperature. The negative temperature coefficient (NTC) temperature sensor placed on the module's DCB substrate is not accurate enough to detect module degradation [4, 38]. It is usually designed to be electrically insulated from the DC contacts and the phase terminal and is therefore placed at a distance from the chips. The losses of the semiconductors mostly traverse vertically through the module structure. Thus, the corresponding temperature increase in the lateral direction is reduced. Therefore, the displacement of the NTC sensor makes junction temperature sensing more difficult [39, 40]. Furthermore, typically only a single NTC sensor is placed inside a power module, although multiple topological switches are included. Determining several independent junction temperatures from the single NTC sensor readout without the use of observer models is not possible. Additionally, the weak thermal coupling between the semiconductors of interest and the strong thermal coupling to the cooler make the NTC sensor susceptible to the losses of neighboring modules on the same cooler or attached to the same cooling loop [39].

Semiconductor-integrated temperature sensors Once the restriction of the electrical insulation is removed, new options for the sensor placement arise. A temperature-sensing diode can be integrated into the semiconductor chip [7, 41, 42]. The diode can be placed in the middle of the chips, where the largest temperature increase is expected, providing a high-bandwidth temperature measurement. For IGBTs, one of the diode terminals can be tied to the emitter of the IGBT, while the other terminal can be made accessible as a module terminal. This allows the integration of the measurement circuitry into the existing gate driver. However, the temperature-sensing diode occupies space on the semiconductor that could otherwise be used as active area [43].

Relocated NTC temperature sensors A hybrid solution is moving the NTC sensor closer to the semiconductors, or even stacking an NTC sensor on top of the semiconductor [44]. This approach does not reduce the active area of the chips, but has a smaller bandwidth compared to the temperature sensing diode.

Electroluminescence of semiconductors Another remarkable approach uses the electroluminescence of the semiconductors [45, 46]. Typical silicon and silicon carbide devices are based on indirect semiconductors. Therefore, recombination methods with light-emission play a minor role [45]. The light-emission is small, yet is sufficiently high to be measured. The light-emitting recombination process can only take place when electrons and holes combine. Consequently, the effect only occurs while the body diode is active in SiC MOSFET modules [46]. Figure 2.11 shows the electroluminescence of SiC MOSFETs. The emitted light depends on the current and the junction temperature. In [46], it was shown that the current and the temperature affect individual wavelengths of the emitted spectrum differently. Therefore, the current and the temperature can be determined separately if light sensors with different spectral sensitivities are combined. Measurements based on electroluminescence can be conducted contactless.

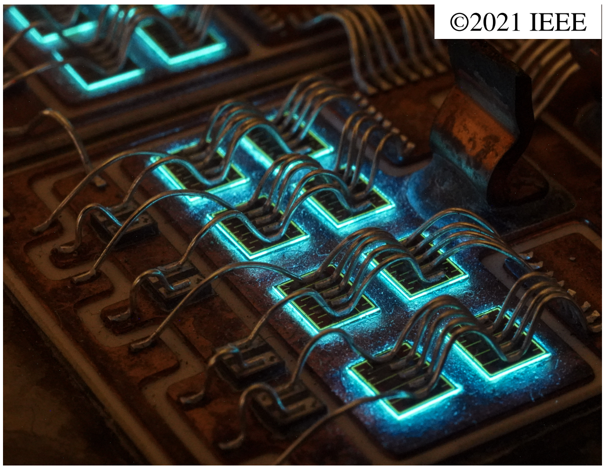

Figure 2.11: Electroluminescence of SiC MOSFETs [47]

Temperature-sensitive electrical parameters TSEPs are electrical parameters that can be measured on the module, e.g., the temperature-dependent on-state voltage of a semiconductor or its switching times. As the semiconductor itself serves as a sensor, TSEP-based temperature estimations offer a very high bandwidth. No modification of the power module is required. However, the measurement circuitry required for TSEP measurements requires special attention and some additional expense.

Using TSEPs for temperature measurements does not reduce the active area of the semiconductors and requires neither volume inside the module nor additional terminals. TSEP-based temperature measurements can be retrofitted to existing power electronics. Before a temperature can be estimated from a TSEP, it is usually calibrated against a known temperature, i.e., on a hot plate. Semiconductor properties show large variations between different devices. The TSEP calibration is usually done on a per-switch basis. TSEPs also often depend more on other parameters, e.g., the load current, than on the temperature. Therefore, they exhibit high noise levels due to their small signal-to-noise ratio.

The use of some TSEPs is already standard in controlled laboratory experiments [8]. A detailed discussion of different aspects of TSEPs will be provided in Chapter 3.

Optical methods In a laboratory environment, options that require a modification of the module, like the use of infrared cameras, are available [8].

2.3.2 Observer structures

Beside the measurement of the junction temperature, model-based approaches can be used to predict the virtual junction temperature. Combining model-based approaches with measurements leads to an observer structure [4, 47].

Feed-forward temperature prediction A fundamental method to determine the junction temperature purely predicatively is the use of a feed-forward model, see Figure 2.12. Starting from a mission profile for a power module, a loss profile is created. The losses are typically determined from look-up tables depending on the switched currents, dc-link voltage and estimated junction temperature. These losses are then mapped to a junction temperature using a thermal model of the module and the surrounding cooling system. The resulting junction temperature curve can ultimately be used in a rainflow counting algorithm to estimate the remaining useful lifetime.

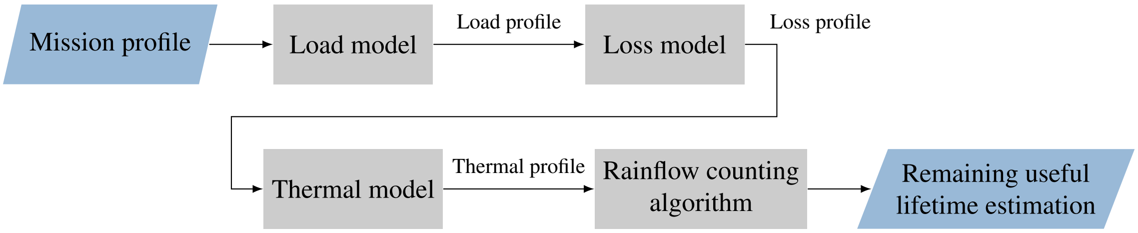

Figure 2.12: Feed-forward model to predict virtual junction temperature and the remaining useful lifetime

No measurements in addition to those from the pre-existing inverter sensors are needed for this approach. The approach can be employed during the design stage or during the operation of an inverter. The disadvantages of this approach are the uncertainties in the losses and the thermal model. The losses vary from module to module. The thermal model provided on the datasheets is usually only valid from the junction to the outside of the module casing[2]. The surrounding cooling system not only extends the thermal model from the datasheet; it can also influence the specified parameters. Furthermore, the degradation of the solder

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[2] Depending on the datasheet, the thermal interface material is included or excluded in the thermal model.

layers changes the thermal model itself, accelerating the aging. As the lifetime models follow power laws or exponential curves, these changes can have significant impact on the estimated remaining useful lifetime.

Observer structure Combining a thermal model of the system with a temperature measurement creates an observer structure. The on-line feedback signal makes it possible to compensate for model inaccuracies and drifts. An example of an observer structure is shown in Figure 1.1.

Of the sensor concepts mentioned, one or more can be used in an observer structure. In [48], a Kalman filter is used to combine the thermal model of the system with the NTC sensor signal. In [49–51] a Kalman filter is used to combine the thermal model with a TSEP of an IGBT module. The on-state voltage measurement is used as a TSEP in [49]. This measurement is only possible when the IGBT is conducting. During the times when its antiparallel diode is conducting the current, the thermal model included in an observer provides purely predictive temperature estimations. It was also shown that the TSEP measurements can be too noisy for an unfiltered junction temperature determination [49], thus a low adaptation rate of the Kalman filter is chosen. The high-frequency components of the junction temperature estimation were mostly provided by the thermal model components and the TSEP measurements were used only to compensate for model inaccuracies, low-frequency disturbances and slow drifts in the thermal resistance of the cooling system [49].

2.3.2.1 Degradation detection

Degradation of the bond connection manifests itself as an increase in the on-state voltage. A bond wire lift-off or heel crack leads to a sudden step-like increase in the on-state voltage [52], whereas reconstruction of the metallization leads to a gradual increase in the on-state voltage.

Measuring the on-state voltage can be directly used to detect these types of degradation if the junction temperature is known from another source [53]. Otherwise, a measured increase in the on-state voltage could be caused by either a bond connection degradation or an increased junction temperature. The increase in junction temperature can be due to external factors, e.g., when an air cooler is used at changing ambient temperature or the degradation of the cooling system. The design requirements for cooling systems are typically not precise enough to allow a direct distinction between the different causes of changes in the on-state voltage.

Solder degradation increases the thermal resistance between the semiconductors and the cooler. This type of degradation is only visible under load, when the losses in the semiconductors lead to an increased junction temperature. The change in thermal resistance is typically gradual. Any measurement that provides information about on the junction temperature can be directly used to detect this type of degradation. In [49], the residuals of the Kalman filter were proposed as a means to detect changes in the thermal resistance of the module.

3 Temperature-sensitive electrical parameters

TSEPs can be categorized according to whether the measurements can be conducted online during regular inverter operation or must be performed offline [43]. The offline aspect can either refer to laboratory environments or to the case where the measurement requires a significant change in the operation of the inverter.

3.1 On-state voltage measurement

The on-state voltage of a device depends on both the current and the temperature. On-state voltage measurements at low currents are already widely used in the laboratory environment [7, 8, 30, 39, 52], and are even incorporated into standards for qualification testing [5]. These measurements apply a low measurement current through a diode, a turned-on IGBT or the body diode of a MOSFET. Heating due to the current can be neglected. This method allows for a simple measurement of the forward voltage of a p-n junction. The resulting voltage-temperature characteristic is linear at low currents. Details of the relevant semiconductor properties will be discussed in Chapter 8. The practical application of these methods will be presented in Chapter 12.

A low-current measurement requires the interruption of regular inverter operation. During operation, it is generally the case that only measurements at high current are possible. The on-state voltage measurement at high currents is a widely used TSEP during operation [49, 52, 54–57]. The voltage-temperature characteristic is current dependent and the simple linear model at low currents is unsuitable at the high currents during normal operation. Figure 3.1 presents an example of an on-state voltage measurement of an IGBT. At high collector currents I_c, the on-state voltage U_ce shows a positive temperature coefficient (PTC). In this region, the temperature characteristic of the voltage drop across the drift region of the module is dominant. At low currents, the on-state voltage exhibits NTC behavior, as the temperature behavior of the threshold voltage dominates over the temperature behavior of the on-state voltage.

The change from NTC to PTC behavior is typical for non-punch-through IGBTs [7] and leads to a cross-over region[1], where the on-state voltage is temperature independent. In this region, the temperature estimation using this TSEP is impossible. Of course, the transition between NTC and PTC behavior happens gradually. As a consequence, the temperature sensitivity of this TSEP is low across a wide range around the cross-over region. Details of the internal structures and temperature dependencies of semiconductors are discussed in Chapter 8.

The on-state voltage measurement can only be used to determine a scalar temperature value, but this TSEP is impacted by the junction temperature of all paralleled semiconductor

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[1] The term cross-over point is also used literature [58], but the location of the cross-over point drifts with temperature, as will be shown in Chapter 6.

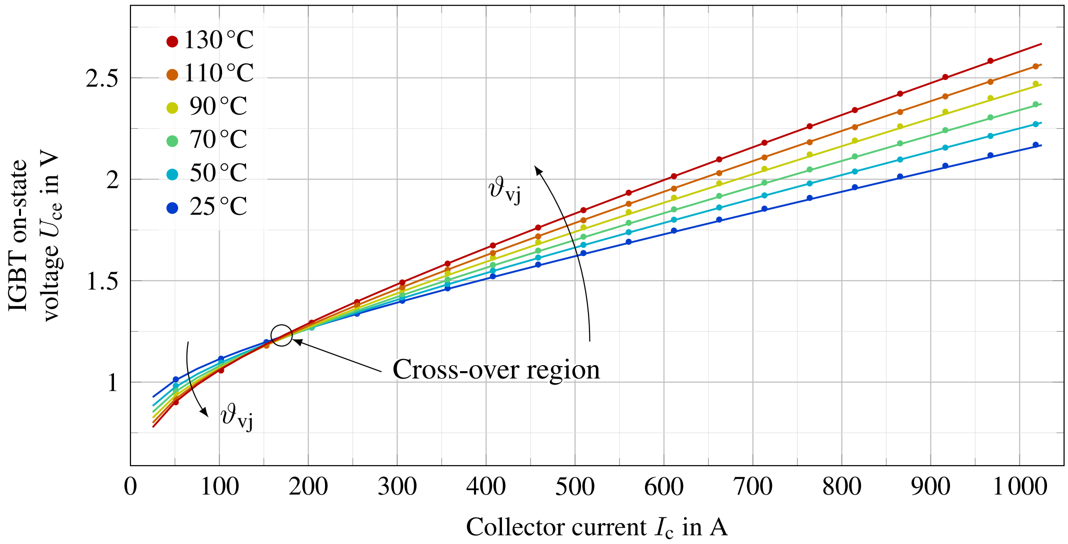

Figure 3.1: On-state voltage example for a 1000 A IGBT module

chips and even all paralleled cells. Due to the high current during inverter operation, the lateral temperature distribution across the semiconductor becomes inhomogeneous. For the on-state voltage, it was shown that the TSEP-based temperature estimation is close to the average surface temperature, even at highly inhomogeneous temperature distributions [8, 59]. In high-power modules, the ohmic voltage drop across the module terminals and internal connections becomes relevant for the measurement and must be considered in the temperature estimation [57, 59, 60].

Similar to the impact of the module terminals and internal connections, the degradation of the bond connection directly affects the on-state voltage. This can be an advantage or a disadvantage, depending on the aim of the application. If the monitoring of the junction temperature is the primary objective, the changes due to the degradation are undesirable; they lead to temperature estimation errors that must be accounted for. But if the degradation detection is the objective, a measurement of the on-state voltage provides information on the condition of the bond connection. For degradation detection alone, an evaluation of the IGBT on-state voltage in the cross-over region has been suggested [61], as it exhibits little temperature dependency.

3.2 Switching times

The switching times of IGBTs and MOSFETs depend on many parameters, such as the threshold voltage, internal gate resistances, transistor capacitances, and load current. Therefore, a change in the switching time can be used as a TSEP [62]. Switching time measurements can be split into turn-on time and turn-off time measurements. Much finer distinctions are possible, e.g., in [62, 63] the turn-on delay time is used as a TSEP. The turn-off delay time is investigated in [53, 62, 64–66] and the current rise time in [67]. Turn-off times typically have a higher temperature sensitivity than turn-on times [53]. All switching times depend on the dc-link voltage, as this voltage impacts the Miller capacitance of the semiconductors.

Figure 3.2 shows a MOSFET half-bridge module, configured for a double-pulse experiment. Here, the low side (LS) switch is the device under test (DUT). The high-side switch is

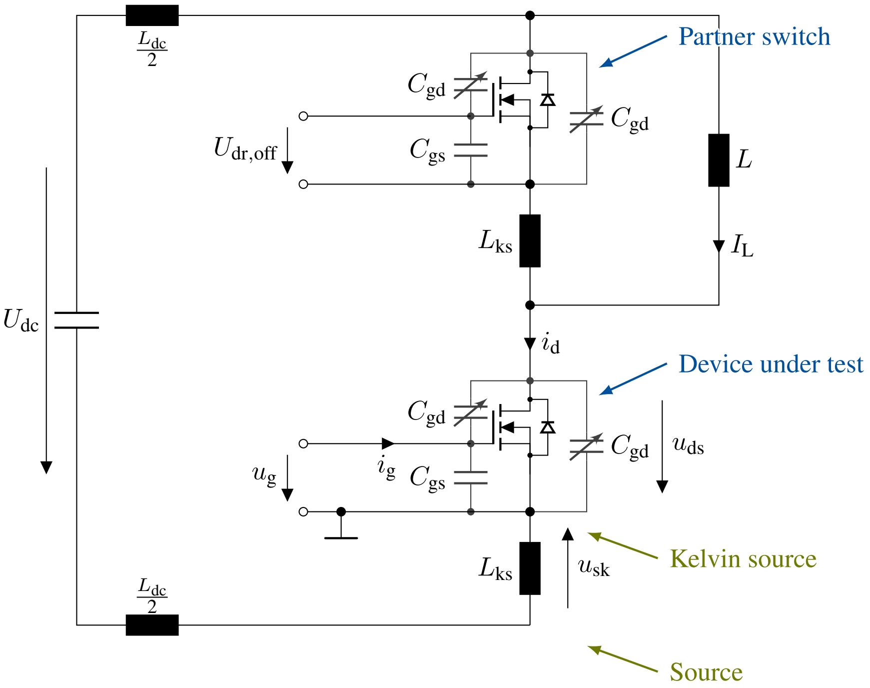

Figure 3.2: Schematic of a half-bridge in double-pulse configuration; here, the low-side switch is the device-under test

the partner switch. A typical turn-on process [68, 69] is shown in Figure 3.3. The concepts of switching time measurements as TSEPs will only be discussed for the turn-on process. Measurements at turn-off are conducted analogously. At the beginning of the turn-on process t_{start}, the driver output voltage switches from the negative gate driver voltage $U_{dr,off}$ to the positive gate driver voltage $U_{dr,on}$ and the gate capacitance is being charged. When the gate voltage u_g reaches the threshold voltage U_{th}, the DUT begins to turn on. The time elapsed between the start t_{start} and this point in time is the turn-on delay time t_d [70]. When the drain current i_d reaches the value of the load current I_L, the body diode of the partner switch begins to turn off. Approximately when the peak of the reverse recovery current I_{rrm} is reached, the drain-source voltage u_{ds} begins to fall according to the gate current and the Miller capacitance C_{gd}. At this point, the gate has reached the Miller plateau voltage U_M. The turn-on time describes the time elapsed between t_{start} and the time when the device is fully turned on, i.e., when $U_{ds} \approx 0\,\mathrm{V}$ is reached.

The durations of the different periods are affected by several temperature-dependent semiconductor properties, e.g., the threshold voltage and the transconductance. Beside the temperature dependencies, the load current I_L and the dc-link voltage U_{dc} affect the durations.

The high current change rate $\frac{\mathrm{d}i_d}{\mathrm{d}t}$ during turn-on induces large voltage spikes across all parasitic inductances. The module itself has a parasitic inductance [71]. The voltage drop u_{sk} across the effective parasitic inductance between the Kelvin source and the source L_s can be used for turn-on time measurements [62, 64, 72]. The turn-on delay time t_d can be measured from the switching of the driver output at t_{start} to the point when the induced voltage u_{sk} becomes negative. Analogously, the time t_{rrm} elapsed until the overcurrent peak is reached can be measured to the point when the induced voltage becomes positive. The

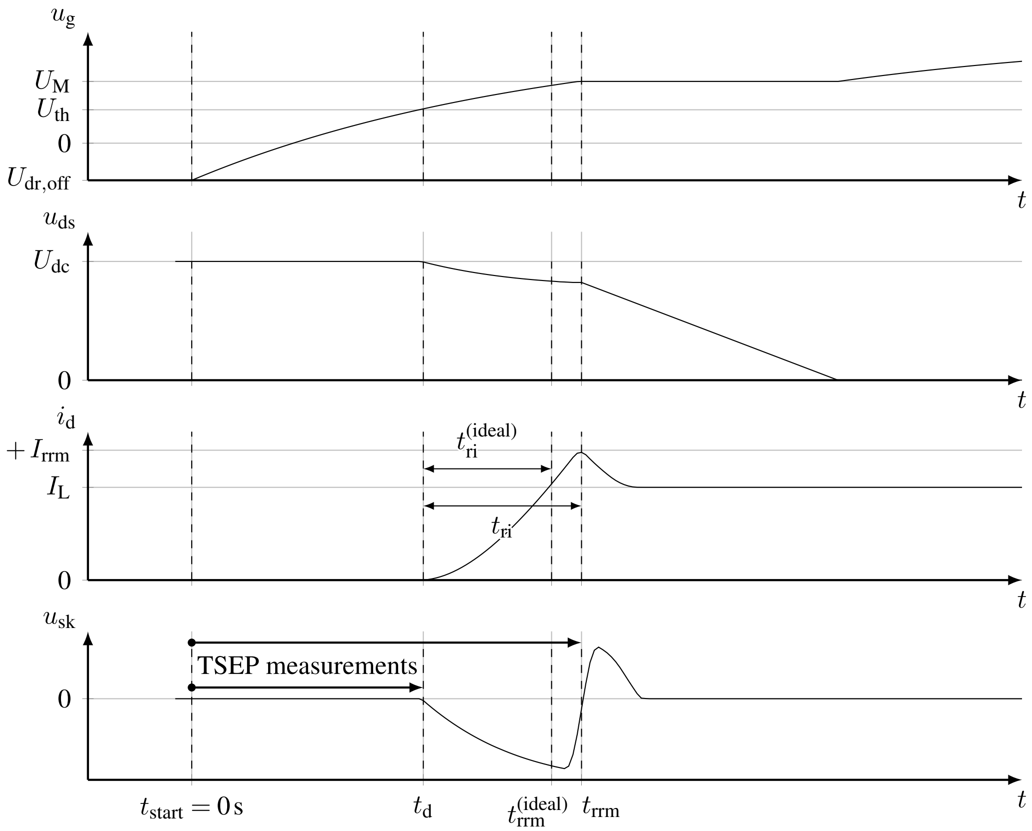

Figure 3.3: Illustration of a turn-on process with an inductive load and possible switching time measurements using the induced voltage across the module inductances

difference between these two durations is the current rise time

$$t_\mathrm{ri} = t_\mathrm{rrm} - t_\mathrm{d}. \tag{3.1}$$

To determine the temperature of the DUT, a measurement of the time until the load current is reached $t_\mathrm{rrm}^\mathrm{(ideal)}$ would be beneficial. Up to this point, the turn-on process is not affected by any properties of the partner switch. The following reverse recovery peak is influenced by the temperature of the body diode in the partner switch and the load current. In practice, only the time t_rrm until the overcurrent peak is reached can feasibly be measured. Therefore, this specific time measurement is affected by the temperature of both switches. The impact of this cross sensitivity is analyzed in Chapter 15.

3.3 Further TSEPs and approaches

The possible ways to deduce the virtual junction temperature from different measurable parameters are manifold. In this section, a brief overview of the TSEP concepts not used in this work is given.

Internal gate resistance The internal gate resistance typically increases with temperature. As the on-chip gate resistance is closely coupled to the junction temperature, it can be used as a TSEP. A concept for measuring the internal gate resistance of an IGBT during regular inverter operation was presented in [73, 74] and transferred to other devices in [75, 76]. The gate capacitance, the internal gate resistance and the parasitic inductance of the gate loop L_g can be modeled as a series resonator. While a negative gate voltage $U_\mathrm{dr,off}$ is applied and the IGBT is blocking, a high-frequency perturbation is added to the gate voltage, see Figure 3.4. The perturbation is small enough not to impact the blocking capability of the IGBT. A frequency close to the resonant frequency of the gate loop is chosen. The gate current can be determined from the voltage drop across the external gate resistor $R_\mathrm{g,ext}$. The internal gate resistance can be determined from the resulting high-frequency gate current. An additional inductance L_aux can be added to the measurement path to adjust the resonant frequency of the measurement circuit. One of the key challenges of this design is the consideration of the portion of the high-frequency current that passes through the driver. As will be presented in Section 9.5, the internal resistance of the driver IC has a significant temperature dependency.

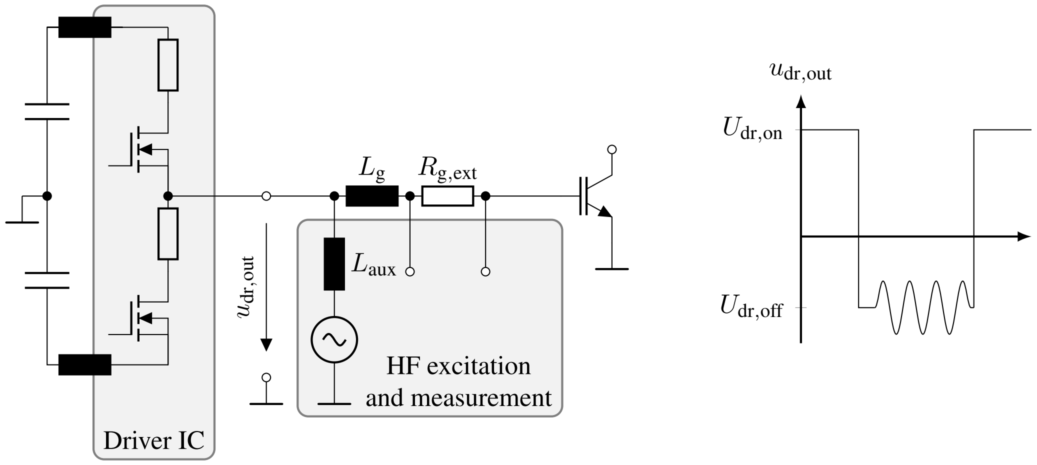

Figure 3.4: Internal gate resistance measurement using a high-frequency (HF) identification signal according to [73, 74]

In [77], the temperature dependencies of the internal gate resistances of different semiconductors are compared. The study includes devices based on silicon, silicon carbide and gallium nitride. It shows that the temperature dependency of the internal gate resistance in SiC devices is much lower than for Si devices. It also demonstrates that the temperature dependency does not necessarily exhibit monotonic behavior. One of the tested SiC junction field-effect transistors (JFETs) and also an Si IGBT exhibit behavior which changes between PTC and NTC.

Threshold voltage The threshold voltage of an IGBT or MOSFET exhibits a comparatively strong temperature dependency, while having few cross dependencies [78]. The measurement of the threshold voltage during inverter operation requires a fast analog-to-digital converter (ADC) with a well-timed sampling trigger [79–81]. The trigger can be derived from the voltage pulse induced between the Kelvin emitter and the emitter of an IGBT module. The application of this TSEP to high-power IGBT modules was investigated in [81]. When the threshold voltage was measured during turn-on, the measured temperature dependency was much lower than expected from the temperature characteristics of the threshold voltage. The switching speed of the module was kept at typical values, resulting in a high gate charge current. The gate voltage that can be measured at the terminals of the power module corresponds to the gate voltage on the chip level altered by the voltage drop across the internal gate resistances [81]. The internal gate resistance showed PTC behavior, partly compensating for the NTC behavior of the threshold voltage. Further details will be presented in Section 9.5.

Measuring the threshold voltage during turn-off corresponds to a measurement of the Miller plateau voltage. This voltage persists for a longer duration, simplifying the measurement. Additionally, the temperature dependency of the internal gate resistance complements the temperature dependency of the threshold voltage in this case, increasing the sensitivity [4, 81]. Using the Miller plateau voltage introduces an additional dependency on the load current.

Saturation current The saturation current of an IGBT is temperature dependent and can therefore be used as a TSEP. Of course, measuring the saturation current nondestructively is challenging in regular inverter operation. In [82], the measurement of the saturation current at a reduced gate voltage was proposed. During the times when the power module is usually turned off, a fixed gate voltage was applied. An external voltage source was added to the system, causing a current flow through the device. The gate voltage was chosen only slightly higher than the threshold voltage of the module at room temperature, limiting the resulting saturation current.

Applying a time-limited short-circuit pulse at nominal gate voltage level was proposed in [83]. As this TSEP requires a significant change in the operation of an inverter, it will not be considered in this work.

Statistical approaches In [84], a statistical approach for measuring the switching times was presented. It uses an on-state voltage detection circuit to implement a switching time measurement.

The on-state voltage of an IGBT is usually sampled behind a voltage limiter. In this setup, the limited voltage is continuously sampled. When the monitored IGBT is blocking, the samples typically assume an easily identifiable high value. Therefore, it can be detected for each sample whether the power module is blocking or conducting. The sampling frequency is not synchronized with the switching frequency.

The expected conducting and blocking durations of the IGBT are known from the employed duty cycles and other factors. From the on-state voltage measurements, the number of consecutive samples that indicate a blocking or a conducting state can be counted, thus measuring the duration of both phases. Of course, these measurements have a very high quantization noise, and a single duration measurement contains little useful information. Nevertheless, aggregating a large number of these noisy measurements allows for a statistical evaluation and the estimation of turn-on and turn-off times. This approach is well suited to monitoring slow, long-term drifts of TSEPs.

Conclusion Finding an electrical parameter that is not temperature-dependent is much more challenging than finding an electrical parameter dependent on the temperature. Consequently, a large variety of other parameters have been investigated as TSEPs, e.g., voltage-change rates, current-change rates, the gate current or oscillations [85]. Further details and an overview of the TSEPs already investigated can be found in [43, 86].

4 Overview of the mathematical concepts used

In this chapter, a short overview of the mathematical concepts and properties relevant to this work will be given.

4.1 Regression analysis

Regression analysis is used to find the best fit of a predefined model function to measured data. This section is based on [87].

Linear least-squares function approximation In a linear least-squares function approximation, a best mapping between a fit function $\boldsymbol{f}(\boldsymbol{x},\boldsymbol{a})$ and measured data $\tilde{\boldsymbol{y}}$ is estimated [87]. The fit function contains multiple independent variables x_i and regression coefficients a_i. A deviation $\boldsymbol{e}$ between the predicted values $\boldsymbol{f}(\boldsymbol{x},\boldsymbol{a})$ and the measured values $\tilde{\boldsymbol{y}}$ occurs. A linear system in this context is defined as

$$\tilde{\boldsymbol{y}} = \boldsymbol{M}(\boldsymbol{x})\,\boldsymbol{a} + \boldsymbol{e}. \tag{4.1}$$

The matrix $\boldsymbol{M}(\boldsymbol{x})$ does not depend on the regression coefficients $\boldsymbol{a}$, but may depend on the independent variables $\boldsymbol{x}$. This is only possible if the partial derivative of $\boldsymbol{f}(\boldsymbol{x},\boldsymbol{a})$ for each regression coefficient a_i is independent of all regression coefficients

$$\frac{\partial \boldsymbol{f}(\boldsymbol{x},\boldsymbol{a})}{\partial a_i} = g(\boldsymbol{x}). \tag{4.2}$$

The remainder of this section will be illustrated using a polynomial fit using the Vandermonde matrix $\boldsymbol{V}$, although all concepts are transferable to any linear least-squares fit using $\boldsymbol{M}$.

Example Let x_k be one unique sample point of the independent variable and $\tilde{y}_k$ be the corresponding measurement. Let n_{meas} be the total number of measurements. For a polynomial of degree n_{poly}, the fit function can be described using the Vandermonde matrix $\boldsymbol{V}$

$$\boldsymbol{f} = \boldsymbol{M}(\boldsymbol{x})\,\boldsymbol{a}, \quad \boldsymbol{M}(\boldsymbol{x}) := \boldsymbol{V}(\boldsymbol{x}) = \begin{bmatrix} 1 & x_1 & x_1^2 & \dots & x_1^{n_{\text{poly}}} \\ 1 & x_2 & x_2^2 & \dots & x_2^{n_{\text{poly}}} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & x_{n_{\text{meas}}} & x_{n_{\text{meas}}}^2 & \dots & x_{n_{\text{meas}}}^{n_{\text{poly}}} \end{bmatrix}, \quad \boldsymbol{a} := \begin{bmatrix} a_0 \\ a_1 \\ \vdots \\ a_{n_{\text{poly}}} \end{bmatrix}, \tag{4.3}$$

with $n_{\text{meas}} \geq n_{\text{poly}}$.

Explicit determination of the global minimum A linear least-squares problem is the minimization of the sum of the square of the deviation of each measurement $\tilde{\boldsymbol{y}}$ and the approximation $\boldsymbol{V}(\boldsymbol{x})\,\boldsymbol{a}$ to estimate the regression coefficients

$$\boldsymbol{a} = \underset{\boldsymbol{a}' \in \mathbb{R}^n}{\arg\min} \underbrace{\|\boldsymbol{V}(\boldsymbol{x})\,\boldsymbol{a}' - \tilde{\boldsymbol{y}}\|_2^2}_{\text{cost function}}. \tag{4.4}$$

This leads to the best approximation if the measurement deviations $\boldsymbol{e}$ are normally distributed [88]. In a linear least-squares function approximation, every local minimum of the cost function is also a global minimum. Consequently, the global minimum is comparatively easy to find using a gradient method.

Linear least-squares function approximations can be solved explicitly without an iterative optimization process. In order to explicitly solve the optimization, QR decomposition is applied. The matrix $\boldsymbol{V}$ is decomposed into a product of an orthogonal matrix $\boldsymbol{Q}$ and an upper triangular matrix $\boldsymbol{R}$.

$$\boldsymbol{V} := \boldsymbol{Q}\boldsymbol{R}. \tag{4.5}$$

The matrix $\boldsymbol{Q}$ is orthogonal, so its transpose is equal to its inverse

$$\boldsymbol{Q}^{\mathrm{T}} = \boldsymbol{Q}^{-1}, \quad \boldsymbol{Q}\boldsymbol{Q}^{\mathrm{T}} = \boldsymbol{I}. \tag{4.6}$$

Here, $\boldsymbol{I}$ is the identity matrix. If the number of measurements n_{meas} is larger than the number of regression parameters n_{poly}, the Vandermonde matrix $\boldsymbol{V}$ shown in (4.3) and the upper triangular matrix $\boldsymbol{R}$ have more rows than columns

$$\boldsymbol{R} = \begin{bmatrix} r_{1,1} & r_{1,2} & \cdots & r_{1,n_{\text{poly}}} \\ 0 & r_{2,2} & \cdots & r_{2,n_{\text{poly}}} \\ \vdots & \ddots & \ddots & \vdots \\ 0 & \cdots & 0 & r_{n_{\text{poly}},n_{\text{poly}}} \\ 0 & \cdots & \cdots & 0 \\ \vdots & & & \vdots \\ 0 & \cdots & \cdots & 0 \end{bmatrix}. \tag{4.7}$$

All rows below the n_{poly}-th are zero. The orthogonal matrix $\boldsymbol{Q}$ must be a square matrix

$$\boldsymbol{Q} = \begin{bmatrix} q_{1,1} & q_{1,2} & \cdots & q_{1,n_{\text{poly}}} & \cdots & q_{1,n_{\text{meas}}} \\ q_{2,1} & q_{2,2} & \cdots & q_{2,n_{\text{poly}}} & \cdots & q_{2,n_{\text{meas}}} \\ \vdots & \vdots & & \vdots & \ddots & \vdots \\ q_{n_{\text{meas}},1} & q_{n_{\text{meas}},2} & \cdots & q_{n_{\text{meas}},n_{\text{poly}}} & \cdots & q_{n_{\text{meas}},n_{\text{meas}}} \end{bmatrix}. \tag{4.8}$$

The dimensions of each matrix are

$$\begin{aligned}
&\boldsymbol{V} \in \mathbb{R}^{n_\text{meas} \times n_\text{poly}}, \quad \boldsymbol{Q} \in \mathbb{R}^{n_\text{meas} \times n_\text{meas}}, \quad \boldsymbol{R} \in \mathbb{R}^{n_\text{meas} \times n_\text{poly}}, \\
&\boldsymbol{a} \in \mathbb{R}^{n_\text{poly} \times 1}, \quad \tilde{\boldsymbol{y}} \in \mathbb{R}^{n_\text{meas} \times 1}, \quad \boldsymbol{I} \in \mathbb{R}^{n_\text{meas} \times n_\text{meas}}.
\end{aligned}$$

Using the QR decomposition, the global minimum of the cost function can be determined explicitly from the measurements

$$\begin{aligned}
&& \boldsymbol{V} &= \boldsymbol{Q}\boldsymbol{R} && (4.9)\\
&\Rightarrow & \boldsymbol{a} &= \underset{\boldsymbol{a}' \in \mathbb{R}^2}{\arg\min} \left(\|\boldsymbol{Q}\boldsymbol{R}\boldsymbol{a}' - \tilde{\boldsymbol{y}}\|_2^2 \right), && (4.10)\\
& & \|\boldsymbol{Q}\boldsymbol{R}\boldsymbol{a}' - \tilde{\boldsymbol{y}}\|_2^2 &= \left(\boldsymbol{Q}\boldsymbol{R}\boldsymbol{a}' - \tilde{\boldsymbol{y}}\right)^\mathrm{T} \left(\boldsymbol{Q}\boldsymbol{R}\boldsymbol{a}' - \tilde{\boldsymbol{y}}\right) && (4.11)\\
& & &= \left(\boldsymbol{Q}\boldsymbol{R}\boldsymbol{a}' - \tilde{\boldsymbol{y}}\right)^\mathrm{T} \boldsymbol{Q}\boldsymbol{Q}^\mathrm{T} \left(\boldsymbol{Q}\boldsymbol{R}\boldsymbol{a}' - \tilde{\boldsymbol{y}}\right), \quad \boldsymbol{Q}\boldsymbol{Q}^\mathrm{T} = \boldsymbol{I} && (4.12)\\
& & &= \left(\boldsymbol{R}\boldsymbol{a}' - \boldsymbol{Q}^\mathrm{T}\tilde{\boldsymbol{y}}\right)^\mathrm{T} \left(\boldsymbol{R}\boldsymbol{a}' - \boldsymbol{Q}^\mathrm{T}\tilde{\boldsymbol{y}}\right) && (4.13)\\
& & &= \|\boldsymbol{R}\boldsymbol{a}' - \boldsymbol{Q}^\mathrm{T}\tilde{\boldsymbol{y}}\|_2^2. && (4.14)
\end{aligned}$$

By definition, all rows below the n_poly-th row of the upper rectangular matrix $\boldsymbol{R}$ shown in (4.7) are zero. The QR decomposition can be split into two parts satisfying

$$\boldsymbol{V} = \boldsymbol{Q}\boldsymbol{R} := \begin{bmatrix} \boldsymbol{Q_1} & \boldsymbol{Q_2} \end{bmatrix} \begin{bmatrix} \boldsymbol{R_1} \\ \boldsymbol{0} \end{bmatrix} = \boldsymbol{Q_1}\boldsymbol{R_1} + \boldsymbol{Q_2}\boldsymbol{0}, \tag{4.15}$$

$$\begin{aligned}
&\boldsymbol{Q_1} \in \mathbb{R}^{n_\text{meas} \times n_\text{poly}}, \quad \boldsymbol{Q_2} \in \mathbb{R}^{n_\text{meas} \times \left(n_\text{meas} - n_\text{poly}\right)}, \\
&\boldsymbol{R_1} \in \mathbb{R}^{n_\text{poly} \times n_\text{poly}}, \quad \boldsymbol{0} \in \mathbb{R}^{\left(n_\text{meas} - n_\text{poly}\right) \times n_\text{poly}}.
\end{aligned}$$

The matrix $\boldsymbol{R_1}$ contains all rows that can have nonzero entries, i.e., the first n_poly rows and $\boldsymbol{Q_1}$ contains only the first n_poly columns of $\boldsymbol{Q}$.

Definition (4.15) can be used to split the cost function (4.14) into two parts, where $\boldsymbol{R_1}$ is invertible

$$\begin{aligned}
\|\boldsymbol{R}\boldsymbol{a}' - \boldsymbol{Q}^\mathrm{T}\tilde{\boldsymbol{y}}\|_2^2 &= \left\| \begin{bmatrix} \boldsymbol{R_1} \\ \boldsymbol{0} \end{bmatrix} \boldsymbol{a}' - \begin{bmatrix} \boldsymbol{Q}_1^\mathrm{T} \\ \boldsymbol{Q}_2^\mathrm{T} \end{bmatrix} \tilde{\boldsymbol{y}} \right\|_2^2, \quad \text{with} \begin{bmatrix} \boldsymbol{Q_1} & \boldsymbol{Q_2} \end{bmatrix}^\mathrm{T} = \begin{bmatrix} \boldsymbol{Q}_1^\mathrm{T} \\ \boldsymbol{Q}_2^\mathrm{T} \end{bmatrix} && (4.16)\\
&= \|\boldsymbol{R_1}\boldsymbol{a}' - \boldsymbol{Q}_1^\mathrm{T}\tilde{\boldsymbol{y}}\|_2^2 + \underbrace{\|\boldsymbol{0}\boldsymbol{a}' - \boldsymbol{Q}_2^\mathrm{T}\tilde{\boldsymbol{y}}\|_2^2}_{\substack{\text{invariant to changes in } \boldsymbol{a}' \\ \text{and zero for } n_\text{meas} = n_\text{poly}}}. && (4.17)
\end{aligned}$$

The cost function is minimal with regard to $\boldsymbol{a}'$ if the left-hand side summand is zero. The summand has full rank, resulting in a unique solution

$$\begin{aligned}
&& \boldsymbol{a} &= \underset{\boldsymbol{a}' \in \mathbb{R}^2}{\arg\min} \left(\|\boldsymbol{Q}\boldsymbol{R}\boldsymbol{a}' - \tilde{\boldsymbol{y}}\|_2^2 \right) && (4.18)\\
&\Leftrightarrow & \boldsymbol{a} &= \underset{\boldsymbol{a}' \in \mathbb{R}^2}{\arg\min} \left(\|\boldsymbol{R_1}\boldsymbol{a}' - \boldsymbol{Q}_1^\mathrm{T}\tilde{\boldsymbol{y}}\|_2^2 \right) && (4.19)\\
&& \boldsymbol{a} &= \boldsymbol{R}_1^{-1}\boldsymbol{Q}_1^\mathrm{T}\tilde{\boldsymbol{y}}. && (4.20)
\end{aligned}$$

Therefore, the optimal regression parameters $\boldsymbol{a}$ can be determined explicitly using the measurements $\tilde{\boldsymbol{y}}$ without any iterative optimization. Both matrices $\boldsymbol{R}_1^{-1}(\boldsymbol{x})$ and $\boldsymbol{Q}_1^{\mathrm{T}}(\boldsymbol{x})$ are independent of the measurements and can be determined a priori if the sample points x_k are known. This property of polynomial regressions will be used in Section 10.5 to determine a linear regression of the voltage samples explicitly.

Nonlinear least-squares function approximation In a nonlinear least-squares function approximation, the partial derivatives of $\boldsymbol{f}(\boldsymbol{x},\boldsymbol{a})$ are no longer independent of the regression coefficients

$$\tilde{\boldsymbol{y}} = \boldsymbol{f}(\boldsymbol{x},\boldsymbol{a_i}) + \boldsymbol{e}, \tag{4.21}$$

$$\frac{\partial \boldsymbol{f}(\boldsymbol{x},\boldsymbol{a})}{\partial a_i} = \boldsymbol{g}(\boldsymbol{x},\boldsymbol{a}), \tag{4.22}$$

$$\boldsymbol{a} = \underset{a_i' \in \mathbb{R}}{\arg\min} \underbrace{\left\|\boldsymbol{f}\left(\boldsymbol{x},\boldsymbol{a'}\right) - \tilde{\boldsymbol{y}}\right\|_2^2}_{\text{cost function } E_{\mathrm{M}}}. \tag{4.23}$$

The resulting minimization problem typically has multiple local minima. In these cases, a gradient method converges to one of these minima. Assessing whether the found minimum is a global minimum is usually not feasible.

As a consequence, the result found may not be the best function approximation, as it depends on the gradient method used and the chosen initial values. The chosen initial values especially affect the result, since the minimum search tends to converge to a minimum close to the initial values.

In the course of this work, highly nonlinear fit functions with a high number of regression parameters will be fitted to data, e.g., for the on-state voltage of an SiC MOSFET. In those cases, appropriate initial values for most parameters had to be determined beforehand, in order to find acceptable function approximations.

Measurement offsets and gain errors In the context of this work, a representative fitting process consists of three steps: forming a fit model function, conducting measurements on a semiconductor and fitting the fit model function to the measured data. It must be kept in mind that the final fitting step does not fit the true semiconductor characteristic, but rather the output data of the used measurement system.

Considering the nonideal behavior of the measurement system in the fit function can improve the fit results significantly. One typical deviation of a measurement system is an offset. Figure 4.1 shows a simulated example of measuring the voltage across a resistor of $R = 1\,\Omega$ depending on the current. In the example, the measured voltage values $\tilde{U}$ and the current values $\tilde{I}$ have an offset and noise. The ideal fit function U can be extended to include offsets in all measured values

$$U \approx RI, \quad U = \tilde{U} - U_0, \quad I = \tilde{I} - I_0, \tag{4.24}$$

$$\tilde{U} \approx R\left(\tilde{I} - I_0\right) + U_0, \tag{4.25}$$

$$\tilde{U} \approx R\tilde{I} + U_0'. \tag{4.26}$$

In this simple example, the offsets of both measurements cannot be separated and collapse into a single parameter. As can be seen in Figure 4.1, not forcing the fit to pass through

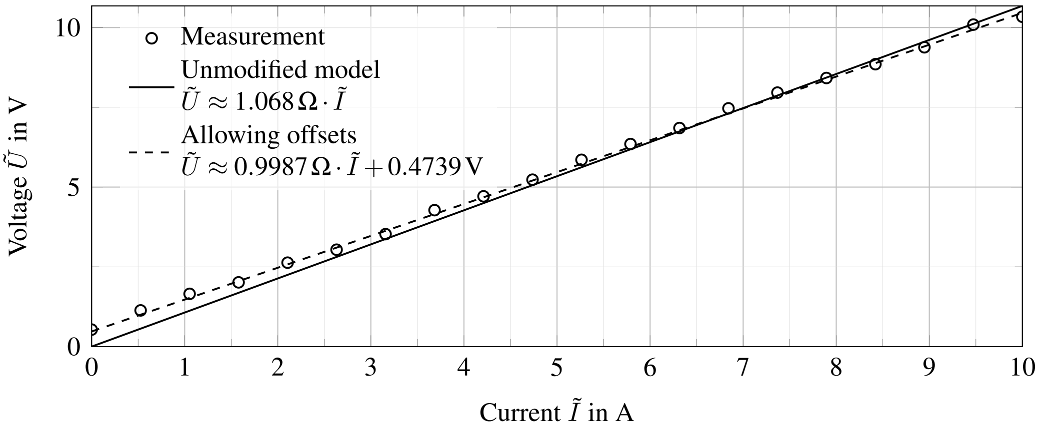

Figure 4.1: Example of a simulated voltage measurement across a 1 Ω-resistor with measurement offsets and noise

the origin $U(I = 0\,\mathrm{A}) = 0\,\mathrm{V}$ allows for a better approximation of the true behavior of the resistor.

In the same manner a gain error can be incorporated, e.g., $\tilde{I} = aI$. A typical cause of a gain error is a signal level adaptation using a voltage divider, e.g., to adapt a high-voltage signal level to the input voltage level of an ADC. Even though the models and data sets used throughout this work are complex enough to identify several offsets and gain errors simultaneously, the observed improvement when including a gain error was marginal.

Within this work, possible measurement offsets are added to every fit model during the fitting process. Gain errors are not considered. This is applied to all measured physical quantities in the fitting process, regardless of them being used as dependent or independent variables. For reasons of brevity, the notation of the offsets is omitted in the fit model functions.

Unintended weighting Using weights is common practice in fitting data. Beside the intended weighting of data, unintended weighting can be caused by the sample point density or data correlations of the independent variables. In the context of this work, an unintended weighting by the sample point density occurs when fitting the on-state voltage of an IGBT module. The on-state voltage is acquired in double-pulse experiments at different load currents, junction temperatures and dc-link voltage levels. At very high dc-link voltages, the maximum current that can be reached is reduced due to the current-dependent voltage drop of the dc-link capacitor during the first pulse. As a consequence, the data set of the on-state voltage contains fewer samples at high currents. An unintended, larger weight of measurements at low currents arises if not accounted for [89]. The problem does not occur in the later SiC MOSFET measurements, as all current, temperature and voltage set points could be applied without restrictions.

A correlation issue was shown in context of the CIPS2008 model, where the measurements at a high average temperature correlated with also having a high temperature swing [32], see Section 2.2.

Inverse problem In an ordinary problem, effects are determined based on known causes. In an inverse problem, the cause is determined from observed effects. A classic example is the application of sonar to localize an object. Determining the time-of-flight between the sender and the known location of an object is trivial. In the inverse problem, the location of the object must be determined from a measured time-of-flight. Using a single measurement, only the distance to the object can be determined. This inverse problem is not uniquely solvable. Distinguishing whether one tries to solve an ordinary or inverse problem becomes relevant in Section 6.1, where a branch decision for a solution tree is only possible if the correct solution is already known.

4.2 Artificial neural networks

The field of artificial intelligence is composed of a large variety of different concepts. In this section, one small part of these concepts will be outlined shortly, limited to the extent it is used in this work. This section is based on [90], in which the corresponding concepts are discussed in detail.

In a classical fitting approach

1. relevant input features are selected (TSEPs),
2. a model to map between the input features and the desired output is created manually (fit function), and
3. the model is trained to the data (fitting).

Using ANNs, the second step can be replaced by an automated process.

An exemplary ANN structure with two input neurons, a single hidden layer of three neurons and a single output neuron is shown in Figure 4.2.

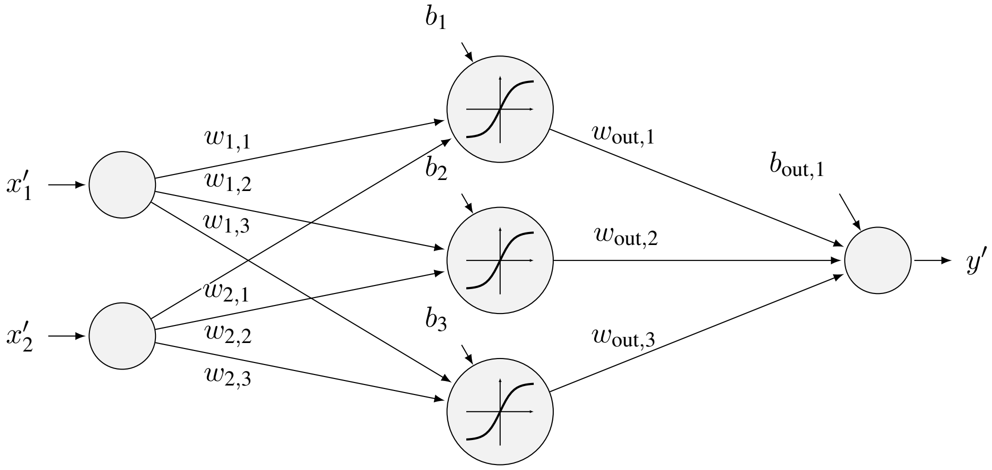

Figure 4.2: Example structure of an ANN with two input neurons, a single hidden layer of three neurons and a single output neuron [90], [89]

First, each input x_i is scaled and offset-corrected into a normalized value x'_i. This is done in order to avoid effects like *loss of significance*, e.g., when combining inputs ranging in different orders of magnitude. The scaling is done systematically, e.g., by mapping the input x_i to the interval $x'_i \in [-1, 1]$ based on the minimum and maximum known value of x_i. Therefore, the scaling and offset correction is not considered a regression coefficient.

Next, from each input neuron, the value is passed to every neuron of the next layer with an individual weighting factor $w_{k_\text{I},k_\text{H}}$. Let k_I be the current input neuron and n_I the total number of input neurons. Let k_{H} be the current hidden layer neuron and n_{H} the total number of hidden neurons.

In the hidden neurons, all inputs are summarized and a neuron-specific bias $b_{k_{\mathrm{H}}}$ is added. Afterwards, a vector-to-scalar activation function φ is applied to the accumulated input. The type of the activation function can be chosen depending on the application. Here, a hyperbolic tangent sigmoid function is used as the activation function, as suggested for regression problems in [91]

$$\varphi(\alpha) \mathrel{\widehat{=}} \tanh(\alpha) = \frac{\mathrm{e}^{\alpha} - \mathrm{e}^{-\alpha}}{\mathrm{e}^{\alpha} + \mathrm{e}^{-\alpha}}, \tag{4.27}$$

$$\alpha_{k_{\mathrm{H}}} \mathrel{\widehat{=}} \sum_{k_{\mathrm{I}}=1}^{n_{\mathrm{I}}} \left(w_{k_{\mathrm{I}},k_{\mathrm{H}}} x'_{k_{\mathrm{I}}}\right) + b_{k_{\mathrm{H}}}. \tag{4.28}$$

Its typical shape is illustrated in Figure 4.2. The biases $b_{k_{\mathrm{I}}}$ select a base operating point on the curve, while the sum of the weighted inputs can be seen as perturbation from this point.

For more advanced tasks, multiple hidden layers can be chained to achieve a more complex functionality

$$\varphi^{(\text{total})} = \varphi_1\left(\varphi_2\left(\varphi_3\left(\ldots\right)\right)\right). \tag{4.29}$$

Feedback paths are another option to increase the level of functionality an ANN can achieve. In the context of regressions, a single hidden layer, or shallow neural network, and a feed-forward ANN are sufficient [91, 92].

Finally, the outputs of the neurons in the hidden layer are weighted individually by $w_{\text{out,k}_{\text{H}}}$ and summarized with a bias $b_{\text{out},1}$ in the output neuron. Multiple output neurons could be defined. In the context of this work, if more than one output is to be estimated from the same input data, separate ANNs are trained for each output.

The overall functional dependency of the output y' on the inputs $x'_{k_{\mathrm{I}}}$ is given by

$$y' = \sum_{k_{\mathrm{H}}}^{n_{\mathrm{H}}} \left(w_{\text{out,k}_{\text{H}}} \cdot \varphi \left(\sum_{k_{\mathrm{I}}}^{n_{\mathrm{I}}} \left(w_{k_{\mathrm{I}},k_{\mathrm{H}}} x'_{k_{\mathrm{I}}}\right) + b_{k_{\mathrm{H}}} \right) \right) + b_{\text{out},1}. \tag{4.30}$$

As before, for nonlinear least-squares function approximations, (4.30) can be interpreted as a nonlinear fitting function. The overall function (4.30) can be conceptualized as an extended linear combination of exponential-function-like terms, which makes it well suited to fit the continuous characteristics of semiconductors.

The total number of regression parameters n_{par} of a shallow neural network depends on the number of inputs n_{I} and hidden neurons n_{H}

$$n_{\text{par}} = \underbrace{n_{\mathrm{I}} n_{\mathrm{H}}}_{\text{input weights}} + \overbrace{n_{\mathrm{H}}}^{\text{hidden neuron biases}} + \underbrace{n_{\mathrm{H}}}_{\text{output weights}} + \overbrace{1}^{\text{output bias}} \tag{4.31}$$

$$n_{\text{par}} = n_{\mathrm{I}} n_{\mathrm{H}} + 2 n_{\mathrm{H}} + 1. \tag{4.32}$$

In this work, an ANN with six inputs and a single hidden layer with six neurons is used as default. This results in a total of $n_{\text{par}} = 49$ regression parameters.

4.2.1 Selecting an appropriate fit result

The nonlinear fitting problem, represented by (4.30), can have a very large amount of local minima if the number of neurons or hidden layers is increased. In the context of ANNs, the search of the global minimum is generally waived. Instead, a local minimum that performs sufficiently well is searched, see Figure 4.3. Finding a sufficiently low local minimum can generally be achieved by repeating the minimum search.

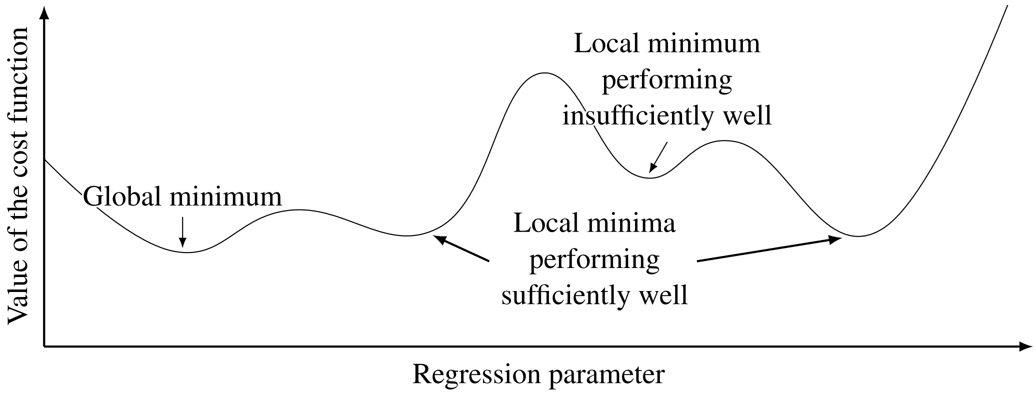

Figure 4.3: Illustration of minima in a cost function [90]; a found local minimum is accepted if it is sufficiently low

Additionally, overfitting is a large concern when using ANNs. When the ratio of available measurement data to the amount of total fit parameters is low, the flexible structure of the ANN (4.30) may start to also fit measurement noise.

Early stopping Early stopping is a method to mitigate the effects of overfitting. The total available measurement data is split into three parts.

1. **Training data:** The largest portion of the data is used as data for the gradient method to search for local minima.
2. **Validation data:** A portion of the available data is excluded from the search of local minima to serve as validation data. Validation data is randomly selected from the available data. This data is used to assess overfitting.
3. **Test data:** Some data is kept from the training process entirely. The data is not used in any way, until the final result has been found. These remaining data samples can be used to assess whether the ANN can be generalized and correctly predict the results for previously unknown data.

The use of test data is especially important if discontinuities or significant nonlinearities are expected in the data. In the context of TSEPs, continuous physical characteristics with low curvatures are fitted. Thus, the use of training data is omitted.

During training , usually the Levenberg–Marquardt algorithm is used to find a local minimum of the cost function and the corresponding set of weights and biases. In this work, only the training data is used. Afterwards, the minimum search is restarted with new initial values to find another local minimum.

Typically, new and lower local minima are found during the repeated training. At the end of each epoch, the found set of weights and biases is applied to determine the value of the cost function with regard to the validation data only, which was not included during the minimum search. The set of weights and biases that has the lowest cost function value on the validation data is kept. At the point where the training begins to overfit the data, it is expected that the result of cost function applied to the training data keeps decreasing, while the value of the cost function applied to the validation data starts to increase.

The final result of the training process is not the set of weights and biases with the best fit performance on the training data, but on the validation data.

4.2.1.1 Bayesian regularization

Bayesian regularization is another approach to find and assess an appropriate local minimum, while avoiding overfitting. It is a stochastic approach that considers the distribution of measurement noise and the distribution of the found local minima conjointly [92–94].

For simplicity, some of the previous definitions are generalized. Let $\tilde{y}_i$ be a measurement and $\hat{y}_i$ the prediction of this measurement made by a fit function or an ANN. Let w_k be any regression parameter, independently of whether it is used as a weight or bias in Figure 4.2 or (4.30). Let n_{par} be the total number of regression parameters and let n_{meas} be the total number of measurements. The function f maps an input value x_i to the prediction $\hat{y}$ using the weights $\boldsymbol{w}$

$$\hat{y} = f\left(x_i, \boldsymbol{w}\right). \tag{4.33}$$

Regularization In a regularization, an additional term E_{W} is added to the cost function E_{M} (4.23).

The regularization term can be used to add information to the cost function. In Bayesian regularization, the square sum of the weights is used [94]

$$E_{\text{W}} := \sum_{k=1}^{n_{\text{par}}} {w_k}^2, \tag{4.34}$$

$$E_{\text{M}} = \underbrace{\sum_{i=1}^{n_{\text{meas}}} \left(\tilde{y}_i - \hat{y}_i\left(\boldsymbol{w}\right)\right)^2}_{\substack{\text{representation in}\\ \text{ANN training}}} \quad \widehat{=} \underbrace{\left\|\boldsymbol{f}\left(\boldsymbol{x}, \boldsymbol{a}'\right) - \tilde{\boldsymbol{y}}\right\|_2^2}_{\substack{\text{representation in nonlinear}\\ \text{least-squares approximation}}}, \tag{4.35}$$

$$E := \beta E_{\text{M}} + \alpha E_{\text{W}} \tag{4.36}$$

$$E = \beta \sum_{i=1}^{n_{\text{meas}}} \left(\tilde{y}_i - \hat{y}_i\left(\boldsymbol{w}\right)\right)^2 + \alpha \sum_{k=1}^{n_{\text{par}}} {w_k}^2. \tag{4.37}$$

The ratio of α and β could be chosen freely to control whether the optimization favors minimizing the prediction error E_{M} or the sum of the squared weight sizes E_{W}.

Penalizing large weights The sensitivity of the ANN's output y' towards the inputs $x_{k_{\text{I}}}$ is

$$\frac{\partial y'}{\partial x_{k_{\text{I}}}} = \sum_{k_{\text{H}}}^{n_{\text{H}}} \left(w_{\text{out,k}_{\text{H}}} \cdot \frac{\partial \varphi\left(a\right)}{\partial a} w_{k_{\text{I}}, k_{\text{H}}} \right). \tag{4.38}$$

Small weights lead to a low sensitivity of the output y' towards changes in the inputs. Training results with small weights are associated with a high smoothing or filtering effect.

The cost function according to the Bayesian regularization (4.37) penalizes large weights if α is large compared to β. An optimal ratio of α and β can be determined to find the most-likely fitting result under given assumptions.

Optimization assumptions First, let an ANN be trained with randomly initialized weights and no measurement data. Even though all independent and dependent variables can be considered zero, the gradient descent method is likely to converge to a random local minimum, where the weights are nonzero. The possible resulting weight sizes $\boldsymbol{w}$ in this case are therefore conceptualized as a random variable. Their distribution is assumed to be a normal distribution [94]. Second, the measurement error $\tilde{y}-\hat{y}$ is assumed to be normally distributed, as usual.

The optimization target in a Bayesian regularization is the maximization of the likelihood of the weights $\boldsymbol{w}$ depending on the measured data, which is equivalent to minimizing the cost function (4.37) [94]

$$\boldsymbol{w} = \underset{\boldsymbol{w'}\in\mathbb{R}^n}{\arg\max}\left(P\left(\boldsymbol{w'}|\tilde{\boldsymbol{y}},\alpha,\beta\right)\right). \tag{4.39}$$

The shape of the distribution changes with α and β. The corresponding derivations are not discussed here, but are explained in detail in [94].

Optimization algorithm The optimization of (4.39) can be done without prior knowledge of the standard deviation of the weights or the measurement error [94]. Finding the values for α and β that lead to the largest probability in (4.39) is done as follows [94].

1. The regularization parameter are initialized as $\alpha_0 = 0$ and $\beta_0 = 1$, meaning the initial training does not penalize weight size.
2. A local minimum of the cost function (4.36) is searched using a gradient method

$$\boldsymbol{w} = \arg\min\left(\beta_j E_\mathrm{M} + \alpha_j E_\mathrm{W}\right). \tag{4.40}$$

3. The effective number of parameters γ is determined from the curvature of the local minimum

$$\gamma = n - \frac{2\alpha_j}{\sum\limits_{k=1}^{n}\frac{\partial^2 E}{\partial {w_k}^2}}, \quad 0 \leq \gamma \leq n. \tag{4.41}$$

The factor γ describes how many of the model parameters are effectively used in the fit.

4. The parameters are adapted according to

$$\alpha_{j+1} = \frac{\gamma}{2E_\mathrm{W}(\boldsymbol{w})} \quad \text{and } \beta_{j+1} = \frac{n-\gamma}{2E_\mathrm{M}(\boldsymbol{w})}. \tag{4.42}$$

5. Repeat from step 2 until the paramters α and β converge.

A large curvature of the local minimum corresponds to large changes in the cost function value if the input values or regression parameters change slightly. The input values are the true values superimposed by measurement noise. Consequently, the found weights are very sensitive towards measurement noise. If the local minimum has a large curvature, the parameters α and β of the cost function are shifted to increase the penalization on large weights E_{W}. This increases the effective smoothing of the fit.

A small curvature means that the cost function changes less with changes in the measured values. The found weights are less susceptible to measurement noise. If the local minimum has a small curvature, the parameters α and β of the cost function are shifted to reduce the penalization on large weights E_{W}.

This concept is also illustrated in Figure 4.3. The graph shows the cost function in one iteration of the optimization. It changes in each iteration, as the parameters α and β shift the penalization ratio between large weights or large prediction errors.

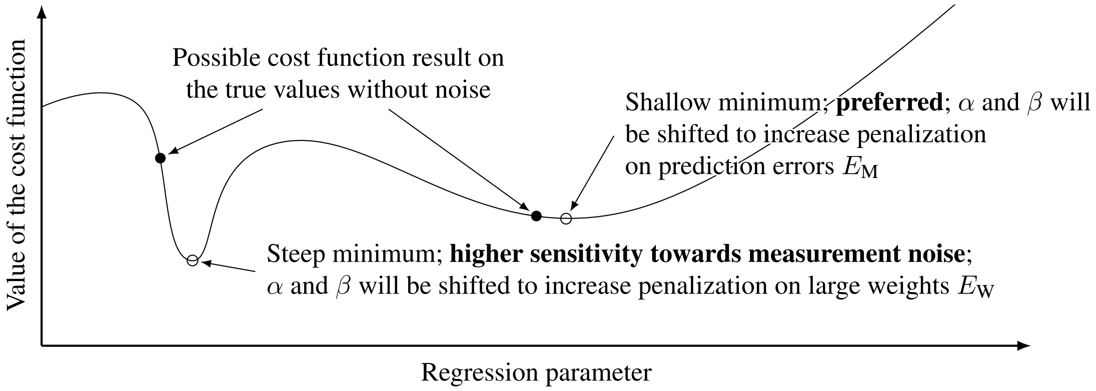

Figure 4.4: Example of a steep and a shallow minimum, considering the effect of the noise included in the training data

It must be kept in mind that the cost function minimization is done using noisy measurement data. The cost function result of the true values is likely to be slightly shifted away from the minimum. In a steep minimum, this leads to larger discrepancy between the found minimum and the cost function value of the true data, which is unknown.

Summary With Bayesian regularization, shallow local minima are preferred over steep minima. This generally results in larger errors between the measured data and the predicted value.

In return, the fit result's dependency on the random noise contained in the measurements is reduced. The achieved training results are more reproducible and their applicability to new data, not included in the training data, improves. Throughout this work, Bayesian regularization is used when training ANNs.

Part II

Preparatory work with Si IGBTs

5 System overview

In this chapter, preparatory work for the TSEP acquisition concepts, their postprocessing and the required measurement hardware will be presented. It was done before developing the TSEP measurement system for SiC MOSFET power modules. IGBT modules with commercial drivers are used for the preparatory work. The developed concepts and investigations were done with the subsequent transition to fast-switching SiC devices in mind.

First, The fundamental concept of combined TSEPs will be outlined. The selection of a suitable set of TSEPs will be discussed. Afterwards, the implementation of preliminary versions of the TSEP measurement circuits will be presented. Different combination methods for TSEPs will be compared and the cross-sensitivity of TSEPs towards unwanted parasitic impacts will be investigated.

The methodologies and results obtained from the IGBT modules are transferable to SiC MOSFET devices and the designed hardware will be adapted to work with the SiC MOSFET modules in Chapter 10.

The test setup consists of an IGBT full-bridge setup, see Figure 5.1. The IGBT module and driver parameters are listed in Table 5.1.

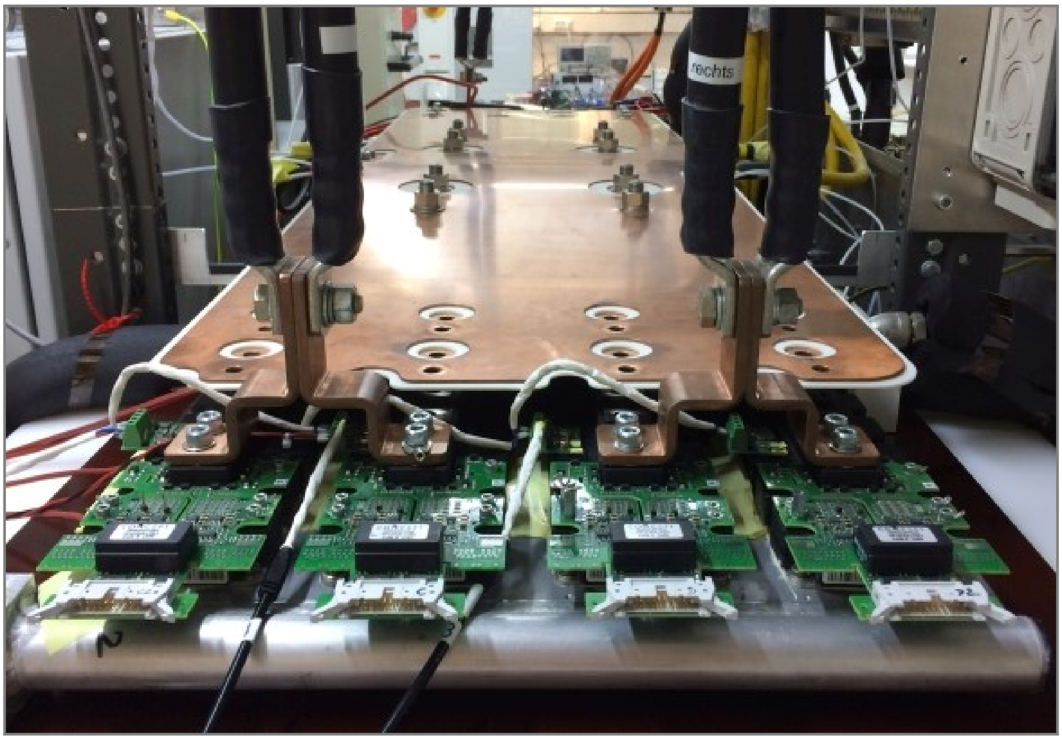

Figure 5.1: Photo of the IGBT testbench

Table 5.1: Used IGBT hardware for preparatory work

Power module:		
Manufacturer		Infineon
Type		Primepack IGBT Module
Name		FF1000R17IE4D_B2
Nominal current	I_{N}	1000 A
Breakdown voltage	U_{ces}	1700 A
Driver:		
Manufacturer		Power Integrations
Type		Scale-2
Name		2SP0320T2E0-FF1000R17IE4
Gate driver voltages	$U_{\mathrm{dr,on}}, U_{\mathrm{dr,off}}$	$+15\,\mathrm{V}$, $-10\,\mathrm{V}$
External gate resistors	$R_{\mathrm{g,on,ext}}, R_{\mathrm{g,off,ext}}$	$1.2\,\Omega$, $3.3\,\Omega$
System:		
DC-link capacitance		3.6 mF
Load inductance	L	2.12 mH
Switching frequency	f_{pwm}	1 kHz

5.1 Selection of a suitable set of TSEPs

Most TSEPs depend not only on the virtual junction temperature ϑ_{vj}, but also other common system parameters like the load current I_{L} or the dc-link voltage U_{dc}. Using the inverter sensors for load current and dc-link voltage measurements entangles the design requirements of the TSEP system and the fundamental inverter functionalities. The inverter sensors are designed according to the operational requirements of the system, e.g., current control. The accuracy class of the sensors may not be sufficient for sensitive TSEP-based measurements.

The inverter sensors usually take samples once per PWM period, i.e., a single sample precisely in the middle of the period or an average result across the entire PWM period. Due to the ripple current, the instantaneous current differs from these values during the course of a PWM period. For some TSEPs this issue can be easily circumvented, i.e., by sampling the on-state voltage in the center of the PWM period.

Transient TSEP measurements, i.e., switching time measurements, require the instantaneous current during the switching process. Determining this current value from the scalar sensor measurement depends on constant system parameters, as well as the dc-link voltage, applied duty cycles and the load voltage. Therefore, switching time measurements cannot be trivially synchronized with the current measurements. A reduced dependency on the inverter sensor accuracy and timing is desirable for TSEP-based temperature estimations.

One way to achieve this is the combination of multiple TSEP measurements in order to substitute the inverter sensor measurements. In [95] the combination of the current rise time during turn-on with the current fall time during turn-off was investigated. Both times depend on the junction temperature and the load current. The aim was to eliminate the load current dependency from the junction temperature estimation. Although the system worked as intended, the results showed large deviations between the expected and the determined temperature. Causes for these deviations will be analyzed in Chapter 7. Even if the sensor measurements are not substituted entirely, a reduction in the sensitivity towards sensor measurement deviations may be achieved.

Selected TSEPs This work focuses on thermomechanical degradation mechanisms. These manifest as solder degradation and bond connection degradation, see Chapter 2. Detecting an increase in the on-state voltage is most feasibly done with an on-state voltage measurement. This will be one of the TSEPs selected for the system. Knowledge of the junction temperature is required to detect degradation using this TSEP as an increased on-state voltage can either be caused by degrading interconnects or an increased junction temperature of the semiconductor. Measuring this TSEP alone in conjunction with a thermal model can already be used for a simple condition-monitoring system [96]. Here, additional TSEPs are introduced to serve as temperature reference.

Switching times are generally not affected by the degradation of the chip-near interconnects, as the overall impedance of the gate path is dominated by the gate resistance and the gate loop inductance. They can be used as supplementary TSEPs to serve as independent junction temperature references. Discrepancies between the virtual junction temperature estimated from the switching times and the one estimated from the on-state voltage can be used to distinguish whether an increase in the on-state voltage is due to an increased virtual junction temperature or degradation of the chip-near interconnects. Switching times can be acquired mostly digitally, simplifying the design of measurement systems with a low ambient temperature sensitivity. They are commonly measured using the induced voltage spike between the Kelvin emitter and the emitter. Combining measurements during turn-on and turn-off will be avoided due to the change in load current between the measurements. This issue is less relevant if the system is extended with a tracking filter, which is outside the scope of this work. During turn-off, only the current fall time can be acquired feasibly. Although this is a TSEP well-suited for virtual junction temperature estimation [53, 62], the turn-on process is chosen for the TSEP measurements. During turn-on, two times can be acquired as TSEPs;

- the turn-on delay time t_d between starting the switching process and reaching the threshold voltage U_th at the gate, and
- the current rise time t_ri.

Another advantage is that these two times are measured at the same gate driver voltage levels. This enables an identification of the gate driver voltage levels or the reduction of the impact of changing gate driver voltage levels during operation.

The time t_rrm until the overcurrent peak is reached and the current rise time t_ri can be used mostly interchangeably

$$t_\mathrm{ri} := t_\mathrm{rrm} - t_\mathrm{d}. \tag{5.1}$$

Implications of using t_ri compared to t_rrm will be discussed in Chapter 7. The on-state voltage measurement of the semiconductor will be timed to occur as quickly after the turn-on process as possible. The aim is to keep the changes in the load current and dc-link voltage between the acquisition of the different TSEPs small.

The dependency of t_rrm on the reverse recovery behavior of the switching partner introduces a cross dependency between the junction temperatures of the high-side and low-side switches, thus introducing an additional dependency into the temperature estimation. To counteract this additional dependency, an additional measurement is incorporated in the set of TSEPs. The on-state voltage of the switching partner diode U_f will be measured in reverse right before turn-on of the switched IGBT, which can be done using the already existing measurement hardware for the on-state voltage measurement if designed bidirectional.

The final four TSEPs selected are

1. the on-state voltage of the partner switch U_f before the partner switch turns off,
2. the turn-on delay time t_d,
3. the time t_rrm until the overcurrent peak is reached, and
4. the on-state voltage of the IGBT U_f after the IGBT turned on.

The concept is illustrated in Figure 5.2. These four TSEPs are acquired in close succession,

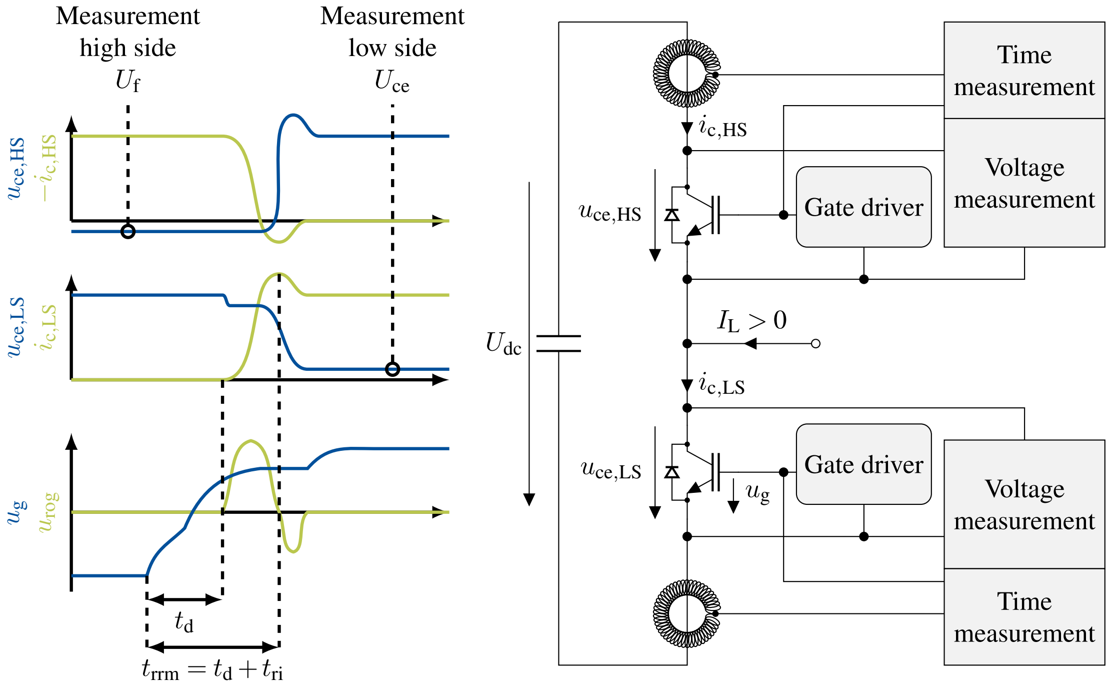

Figure 5.2: Concept of the acquired TSEPs at turn-on [67] (left); concept of the implemented measurement hardware [89], [67] (right)

reducing the differences in current and dc-link voltage as much as possible.

> **Remark:** In this preliminary investigation, a Rogowski coil was used to acquire the voltage pulse caused by the commutation current. The aim was to investigate whether a Rogowski coil is suitable for this application, as it would allow the contactless mounting of the measurement system anywhere

in the commutation loop. Using a Rogowski coil or directly contacting the emitter can be interchanged as desired from a functional point of view. A Rogowski coil will always be slower than a direct connection, as the self inductance of the coil limits its output signal rise time.

Resulting system of equations The most significant dependencies of the chosen TSEPs are listed in Table 5.2. The four measured TSEPs depend on four unknown parameters and the resulting system of equations presumably has full rank. In theory, the four TSEPs could be used to directly determine the semiconductors' virtual junction temperatures, the switched load current and the dc-link voltage. Unfortunately, this only works when the module degradation is neglected. As soon as an on-state voltage increase arises due to a bond connection degradation, the results would be affected.

Table 5.2: Most significant dependencies of the four proposed TSEPs

TSEP Dependency	t_d	t_ri	U_ce	U_f
Junction temperature IGBT	✓	✓	✓	
Junction temperature diode		✓		✓
Load current		✓	✓	✓
DC-link voltage	✓	✓		
Bond wire lift-off			✓	✓
Solder degradation	✓	✓	✓	✓

Instead, the load current I_L and the dc-link voltage U_dc will be included as two additional measurements. Consequently, the system has six inputs and four outputs and is overdetermined. The additional two measurements can be used to eliminate other unknown parameters, i.e., disturbances, compare Table 5.3. Note that the solder degradation is not listed as

Table 5.3: Measurement inputs and planned output parameters; Order has no significance

Inputs			Determined parameters
Turn-on delay time	t_d	$\rightarrow$	Junction temperature IGBT
Current rise time	t_ri		Junction temperature diode
On-state voltage DUT	U_ce		Bond wire lift-off
On-state voltage switching partner	U_f		Disturbance 1
Load current	I_L		Disturbance 2
DC-link voltage	U_dc		Disturbance 3

an independent parameter, as it strongly correlates with the junction temperatures.

5.1.1 Illustration of a disturbance elimination

The switching times not only depend on the semiconductor, but also on the gate driver. Changes in the gate driver voltages or the external gate resistance could be one of the disturbances to be eliminated. Consider the gate loop to be a trivial RC element that is charged from the negative gate driver voltage $U_{\mathrm{dr,off}}$ to the positive gate driver voltage $U_{\mathrm{dr,on}}$. The switching times t_{d} and t_{rrm} could be described as

$$u_{\mathrm{g}}(t) = U_{\mathrm{dr,off}} + \left(U_{\mathrm{dr,on}} - U_{\mathrm{dr,off}}\right)\left(1 - \mathrm{e}^{-\frac{t}{R_{\mathrm{g}}C_{\mathrm{g}}}}\right), \quad \tau_{\mathrm{g}} := R_{\mathrm{g}}C_{\mathrm{g}} \tag{5.2}$$

$$t_{\mathrm{d}} = \tau_{\mathrm{g}} \ln\left(\frac{U_{\mathrm{dr,on}} - U_{\mathrm{dr,off}}}{U_{\mathrm{dr,on}} - U_{\mathrm{th}}}\right) \tag{5.3}$$

$$t_{\mathrm{rrm}} = \tau_{\mathrm{g}} \ln\left(\frac{U_{\mathrm{dr,on}} - U_{\mathrm{dr,off}}}{U_{\mathrm{dr,on}} - U_{\mathrm{M}}}\right). \tag{5.4}$$

The turn-on delay t_{d} is the time when the threshold voltage U_{th} is reached. The time t_{rrm} corresponds to the gate voltage reaching the Miller plateau voltage U_{M}, with respect to the load current and reverse recovery current. A change in the gate time constant τ_{g} will proportionally affect the measured times. As a countermeasure the time constant τ_{g} can be eliminated, by determining the ratio of the measured times

$$\frac{t_{\mathrm{rrm}}}{t_{\mathrm{d}}} = \frac{\tau_{\mathrm{g}} \ln\left(\frac{U_{\mathrm{dr,on}} - U_{\mathrm{dr,off}}}{U_{\mathrm{dr,on}} - U_{\mathrm{M}}}\right)}{\tau_{\mathrm{g}} \ln\left(\frac{U_{\mathrm{dr,on}} - U_{\mathrm{dr,off}}}{U_{\mathrm{dr,on}} - U_{\mathrm{th}}}\right)} = \frac{\ln\left(\frac{U_{\mathrm{dr,on}} - U_{\mathrm{dr,off}}}{1\,\mathrm{V}}\right) - \ln\left(\frac{U_{\mathrm{dr,on}} - U_{\mathrm{M}}}{1\,\mathrm{V}}\right)}{\ln\left(\frac{U_{\mathrm{dr,on}} - U_{\mathrm{dr,off}}}{1\,\mathrm{V}}\right) - \ln\left(\frac{U_{\mathrm{dr,on}} - U_{\mathrm{th}}}{1\,\mathrm{V}}\right)}. \tag{5.5}$$

Changes in the driver voltages will affect the times nonlinearly.

Similarly, the impact of changes in the negative gate driver voltage $U_{\mathrm{dr,off}}$ canbe eliminated by using the difference of the times

$$t_{\mathrm{rrm}} - t_{\mathrm{d}} = t_{\mathrm{ri}} = \tau_{\mathrm{g}} \ln\left(\frac{U_{\mathrm{dr,on}} - U_{\mathrm{dr,off}}}{U_{\mathrm{dr,on}} - U_{\mathrm{M}}}\right) - \tau_{\mathrm{g}} \ln\left(\frac{U_{\mathrm{dr,on}} - U_{\mathrm{dr,off}}}{U_{\mathrm{dr,on}} - U_{\mathrm{th}}}\right) \tag{5.6}$$

$$= \tau_{\mathrm{g}} \ln\left(\frac{U_{\mathrm{dr,on}} - U_{\mathrm{th}}}{U_{\mathrm{dr,on}} - U_{\mathrm{M}}}\right). \tag{5.7}$$

This illustrates how multiple TSEP measurements may be combined to eliminate dependencies on unknown parameter changes. These concepts will be extended and investigated in Chapter 7.

5.2 Preliminary measurement front ends

Figure 5.2 showed the concept of the implemented preliminary TSEP measurement system for IGBTs. The voltage measurements and the time measurements require an analog front end. Measuring TSEPs is challenging with regard to EMI, accuracy and temperature stability. There are many different design solutions, none of which are universally ideal. The TSEP hardware design for the IGBT modules and the corresponding double-pulse measurements were carried out in a master's thesis [89] and published in [67].

5.2.1 Time measurement

The time measurement uses a time-to-digital converter (TDC) TDC7200 by Texas Instruments. It is designed for ultrasonic time-of-flight measurements with a resolution of approximately 55 ps. More advanced TDCs from LIDAR applications can be used if a better resolution is required. The TDC expects a CMOS-level input, while the voltage spike across the Rogowski coil or between the Kelvin emitter and the emitter can be in the order of 100 V. The requirements on the front end are:

- voltage level adaptation
- protection of subsequent measurement circuitry
- low propagation delay
- low sensitivity towards the ambient temperature
- cost, space and energy consumption

The propagation delay usually increases with each circuitry stage, which is why fewer stages are preferred. A voltage level adaptation could be implemented using a voltage divider with a small divider ratio. A high-speed comparator could be used to trigger at a predefined voltage level [97]. Even though the propagation delay still depends on the overdrive at the comparator's input, this setup would allow fine control of the system. Unfortunately, the found comparators in the required speed class commonly had low voltage differential signaling (LVDS) output, requiring additional adaptation stages.

Instead, a simple transistor trigger is chosen as input. A MOSFET is not used, as its gate is sensitive to overvoltages and protective components would be required. This usually results in the insertion of a series resistance and clamping diodes (TVS diodes). Preliminary investigations have shown that the capacitance of the clamping diodes in conjunction with prepended resistor lead to notable propagation delays. The final design uses high-frequency bipolar junction transistors (BJTs), see Figure 5.3. The signal waveforms are illustrated in Figure 5.4. BJTs allow a current flow through its base-emitter path. If a high-voltage spike occurs at the input of the front end, almost the entire voltage drops across the base resistors, protecting the BJT and subsequent circuitry. The trigger level is chosen as low as possible to reduce the propagation delay.

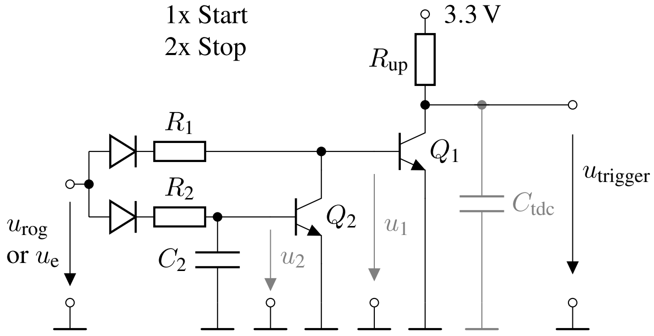

Figure 5.3: Concept of a TDC analog front end for the trigger generation [89], [67]; Q_1 generates a falling edge on the trigger line, while Q_2 releases the trigger line after a defined time T_{pulse}; the TDC input pin is listed with an input capacitance of $C_{\text{tdc}} = 3\,\text{pF}$ [98];

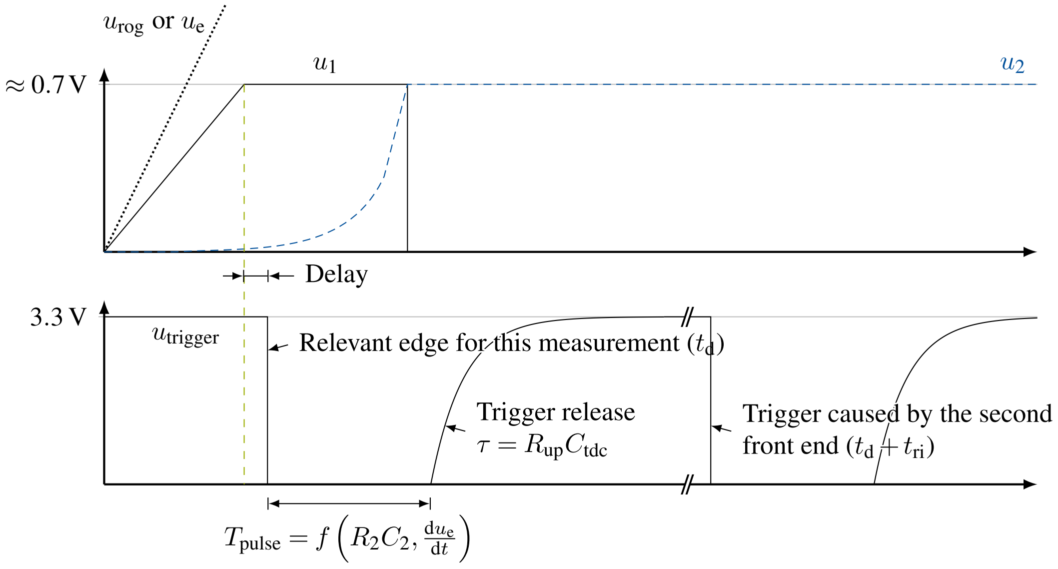

Figure 5.4: Illustration of the front end signals for the first stop pulse generated for the measurement of the turn-on delay time t_{d}; Q_1 generates a falling edge on the trigger line[1], while Q_2 releases the trigger line after a defined time T_{pulse};

When a voltage spike occurs at the input, the transistor Q_1 shorts the input capacitance of the TDC to ground. After a delay defined by $R_2 \cdot C_2$, the transistor Q_2 shorts the base of Q_1, releasing the trigger output u_{trigger} to a weak high state[2]. This generates a negative pulse on the trigger line with a defined width T_{pulse}. A single TDC can measure multiple switching times during one turn-on process if they are provided as a pulse train. Therefore, the circuitry is implemented twice, once for the turn-on delay time t_{d} and once for reaching time of the overcurrent peak t_{rrm}. The signal of the Rogowski coil is rectified on the printed circuit board (PCB) and provided to the two trigger circuits with appropriate polarity. Both circuits are paralleled at the output, generating a pulse train corresponding to the two measured times[3].

The front end's temperature dependency is dominated by the temperature dependency of the base-emitter forward voltage of Q_1. Detailed investigations will be shown in Section 9.4. The same front end is also used to generate the start signal from the gate driver's output, introducing a matching propagation delay in the start and stop triggers. A more detailed analysis and measurements of this circuitry will be shown for the final SiC design in Chapter 10.

5.2.2 Voltage measurement

An on-state voltage measurement at the collector or drain of a power module poses a significant challenge. An accuracy in the millivolt range during the on-state is desired, while the input voltage is as high as the dc-link voltage when the power device is blocking. Typically, analog front ends switch their mode of operation depending on the switch state of the power

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[1] During the initial ramp, neither the input diode nor the base-emitter path of Q_1 are conducting. In this phase, the voltage u_1 significantly depends on the voltage divider formed by the parasitic capacitances of the diodes and BJTs.

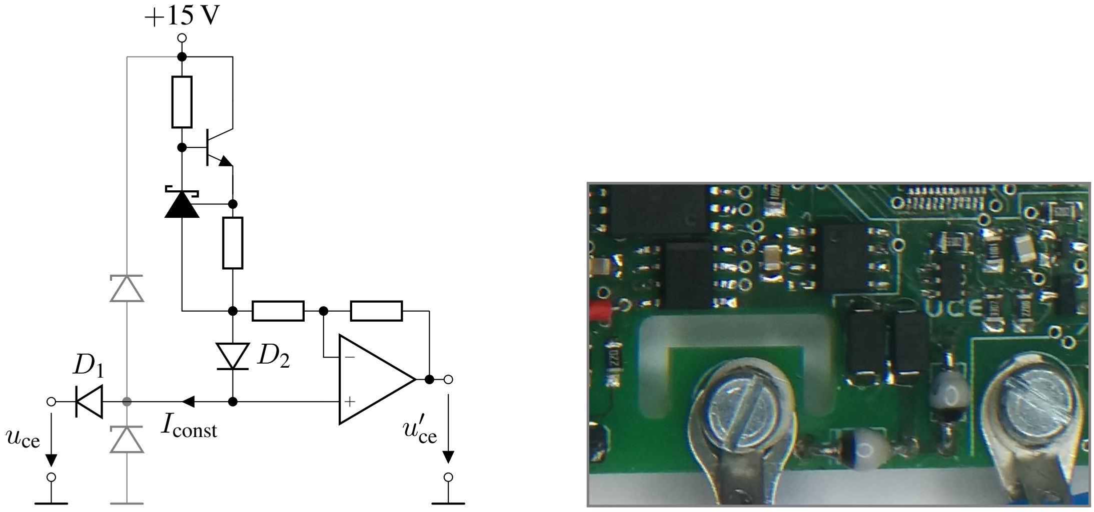
[2] The output is high, but with a large output resistance

[3] The pulse train concept will not be applied to SiC MOSFETs as the time between pulses is too short.

module. The analog front end of the ADC has to meet the following requirements:

- protection of the subsequent circuitry
- sufficient accuracy to determine temperature-related changes in the on-state voltage
- sufficient bandwidth to acquire measurement samples during the limited on-time of the power module
- temperature stability with regard to the ambient temperature
- cost, space and energy consumption

One of the most common front ends uses a diode to block the dc-link voltage similarly to a desaturation detection [52, 54], see Figure 5.5a. If the collector-emitter voltage u_{ce} rises above the circuit's supply level, the diode D_1 blocks the high voltage. When the input voltage u_{ce} falls significantly below the supply voltage level of 15 V, a constant current source generates a current I_{const}, which is driven through the diode D_1 and the collector-emitter path of the contacted IGBT. The collector-emitter voltage u_{ce}, falsified by the forward voltage drop across D_1, can be found at the anode of the diode D_1. A matching diode D_2 is inserted in the path of the constant current I_{const}. Its forward voltage drop is subtracted from the falsified voltage at the anode of D_1 to compensate the deviation depending on the diode temperature and measurement current.



(a) On-state voltage measurement using a diode to block the dc-link voltage [52, 54, 81, 99]

(b) Photo of the diodes D_1, D_2 and the insulation distances required at the bottom; this PCB was developed in previous work [81]

This circuitry was investigated and tested in previous work [53],[81]. Experienced difficulties were the matching of the diodes and their thermal coupling. In order to achieve a good thermal coupling, the devices should be placed close to each other and connected with a thermal interface material. In practice, this requirement is difficult to fulfill due to insulation coordination, see Figure 5.5b. The entire dc-link voltage drops across the diode D_1 when the IGBT is blocking. When moving to smaller power modules, i.e., SiC MOSFETs, the measurement PCB is directly mounted onto the module. The electrical contact to the collector or drain is done by press-fit connection. Unfortunately, this also creates a tight thermal coupling between the module's DCB and the PCB. Heat soaks from the hot DCB through the pins and affects diode D_1 more than diode D_2, thus causing a mismatch in their forward voltages. The forward voltage difference between D_1 and D_2 cannot be distinguished from changes in the on-state voltage of the IGBT. Nevertheless, this concept is well-designed and broadly applied in literature.

As an alternative, a passive voltage limiter is chosen as ADC front end, see Figure 5.6. When the input voltage u_{ce} rises, the capacitance C_1 is charged. This decreases the gate-source voltage of the MOSFET Q_1 until it blocks. The first stage limits the voltage to levels within the gate driver supplies, but the voltage limitation is not precise enough to directly attach an ADC. A second stage is added to limit the voltage to the ADC's positive supply level more accurately to the required limits of the subsequent ADC.

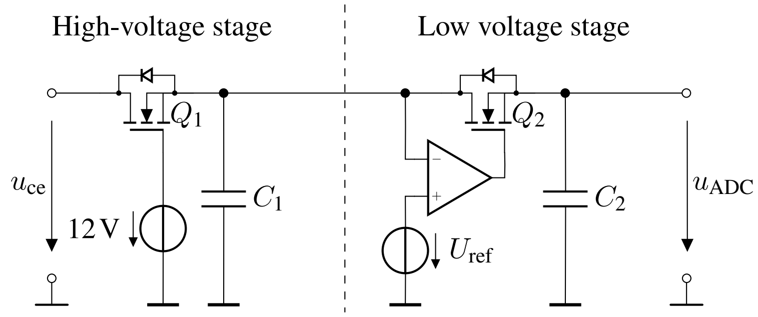


Figure 5.6: ADC front end; a passive voltage limiter with two stages [89], [67]

During on-state of the power device, the voltages at C_1 and C_2 are well below the gate voltages applied to Q_1 and Q_2. The MOSFETs are turned-on and the ADC is almost directly attached to the collector of the power module. The on-state resistance of Q_1 and Q_2 is very small compared to the input resistance of the ADC, thus the voltage drop across Q_1 and Q_2 can be neglected. This is the main advantage of the design, as the on-state voltage can be measured directly.

One concern with this circuitry is the leakage current through Q_1 and Q_2. Given the high dc-link voltage, even small currents can cause heating of the MOSFET Q_1. A comparator is added in the preliminary version of circuit. It actively turns off Q_2 when a high voltage at its input is detected, greatly reducing any leakage current through Q_1 and Q_2. The comparator will be removed in the final design, as a passive limitation is sufficient, see Chapter 10.

Another concern with this circuitry is the more complex design phase. During voltage transients on u_{ce}, high charge currents pass through the output capacitances of Q_1 and Q_2. Additionally, their output capacitances form a capacitive voltage divider with C_1 and C_2, causing a voltage feedthrough at the ADC input during switching. Both aspects must be limited to be within the specifications of the MOSFETs and the subsequent ADC. After turn-on of the power module, the on-state resistances of Q_1 and Q_2 together with C_1 and C_2 form a low-pass filter. The low-pass filter is nonlinear, as the on-state resistances of Q_1 and Q_2 change with their changing gate-source voltages. Design parameters are the threshold voltages and on-state resistances of the chosen MOSFETs and the voltage references at their gates. SPICE simulations during transients of u_{ce} are used to choose matching MOSFETs and gate voltages. A more detailed analysis and measurements of this circuitry will be shown for the final SiC design in Chapter 10.

5.2.3 Double-pulse experiment results

Setup The preliminary PCB for IGBTs is shown in Figure 5.7. The system is operated in double-pulse experiments. During the current build-up in the first turn-on phase of the double-pulse experiment, the voltage of the dc-link capacitor drops. Before each double-pulse experiment is begun, the dc-link capacitor is precharged to a higher voltage, so that the dc-link voltage matches the target voltage U_{dc} at the end of the first turn-on phase [95]. Thus, the measured turn-on and turn-off processes are conducted at the controlled voltage level U_{dc}, independently of the load current. At high target dc-link voltage levels and high currents, the precharge voltage would have been higher than permissible in the test bench. Consequently, calibration points at high target voltage levels U_{dc} and high currents I_{c} could not be acquired. An overview of the used calibration points is shown in Figure 5.8. Ultimately, 1620 distinct calibration points are acquired for the preliminary tests. The test bench was automated to a large extent and was set up to execute approximately two double-pulse experiment per second, when the temperature was stable. Reaching the steady-state temperature took 20 to 30 minutes between each set point.

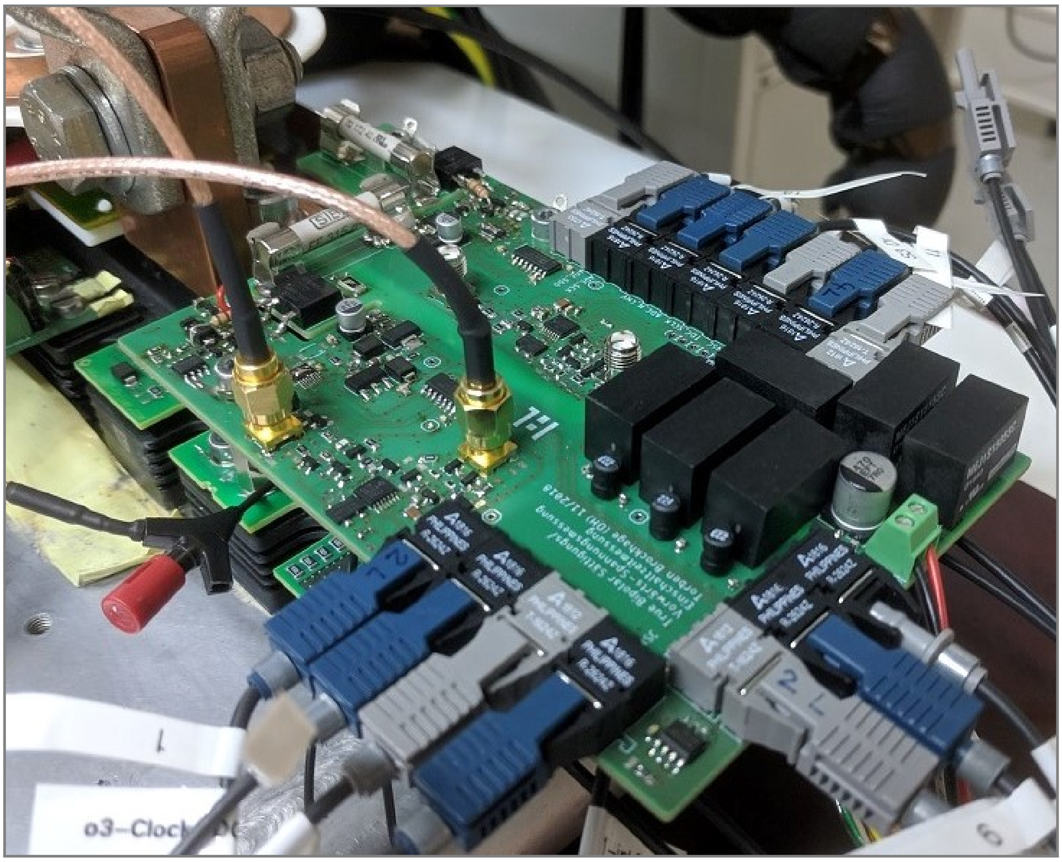


Figure 5.7: Photo of the TSEP measurement system for IGBTs [67, 89]; retrofitted on top of the existing gate driver; gate driver outputs contacted with coaxial cables for start signal generation

The preliminary experiments were also used to validate the test bench. Each calibration point was measured nine times in close succession, i.e., every 0.5 s, to validate the experimental setup. If the self-heating of the semiconductors was higher than expected, a trend line would occur. The acquired nine samples are shown for two exemplary calibration points in Figure 5.9. No prominent trend lines are obvious in the samples. The precision is mostly in

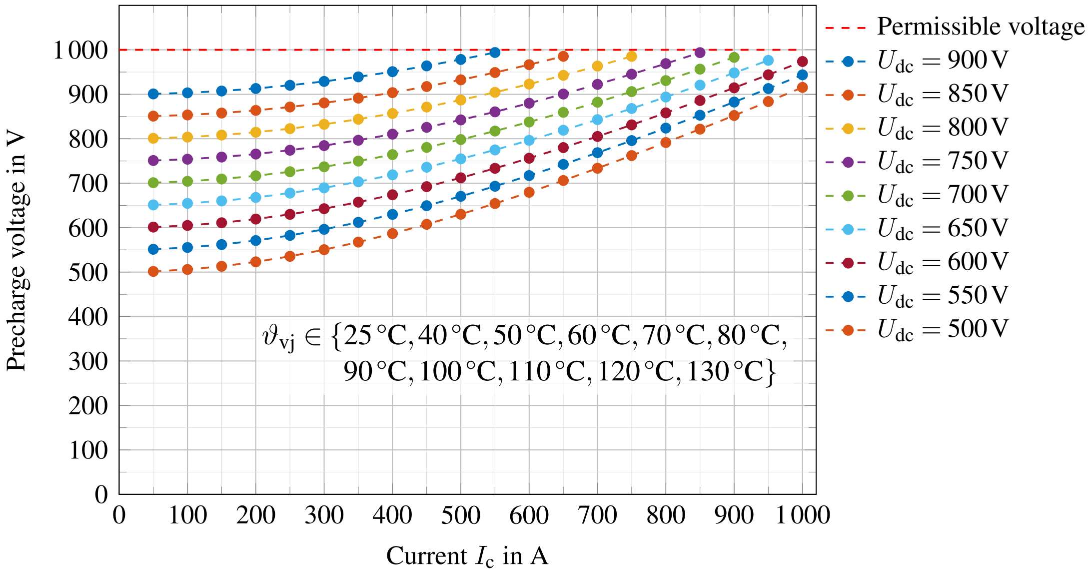


Figure 5.8: Double-pulse experiment calibration points for the preliminary TSEP measurement system and the required precharge voltage to compensate the voltage drop of the dc-link capacitor; voltage and current are stepped in 50 V and 50 A steps; each pair of current and voltage shown is acquired at eleven temperatures ϑ_{vj}

the range of the ADC and TDC resolution. The measurements are grouped closely together, showing a good repeatability of the experiments.

The low noise level and the absence of trends in the measurement repetition lead to two decisions. First, all nine samples are averaged for each of the 1620 distinct calibration points to reduce the amount of (redundant) data without wasting existing information. Thus, the 1620 calibration points used in investigations shown in this section use slightly filtered data. Second, sampling the same calibration point more than once is omitted in all subsequent investigations, i.e., the SiC measurement system.

Measurements The acquired TSEP measurements with the PCB are shown in Figure 5.10. Generally, the TSEP measurements have little noise and show expected behavior, compare Chapter 3. The IGBT saturation voltage and the diode forward voltage show their temperature sensitivity changing gradually from NTC to PTC behavior. The current rise time increases with the switched current and the temperature. All switching times are decreased by applying a higher dc-link voltage, as the Miller capacitance is reduced.

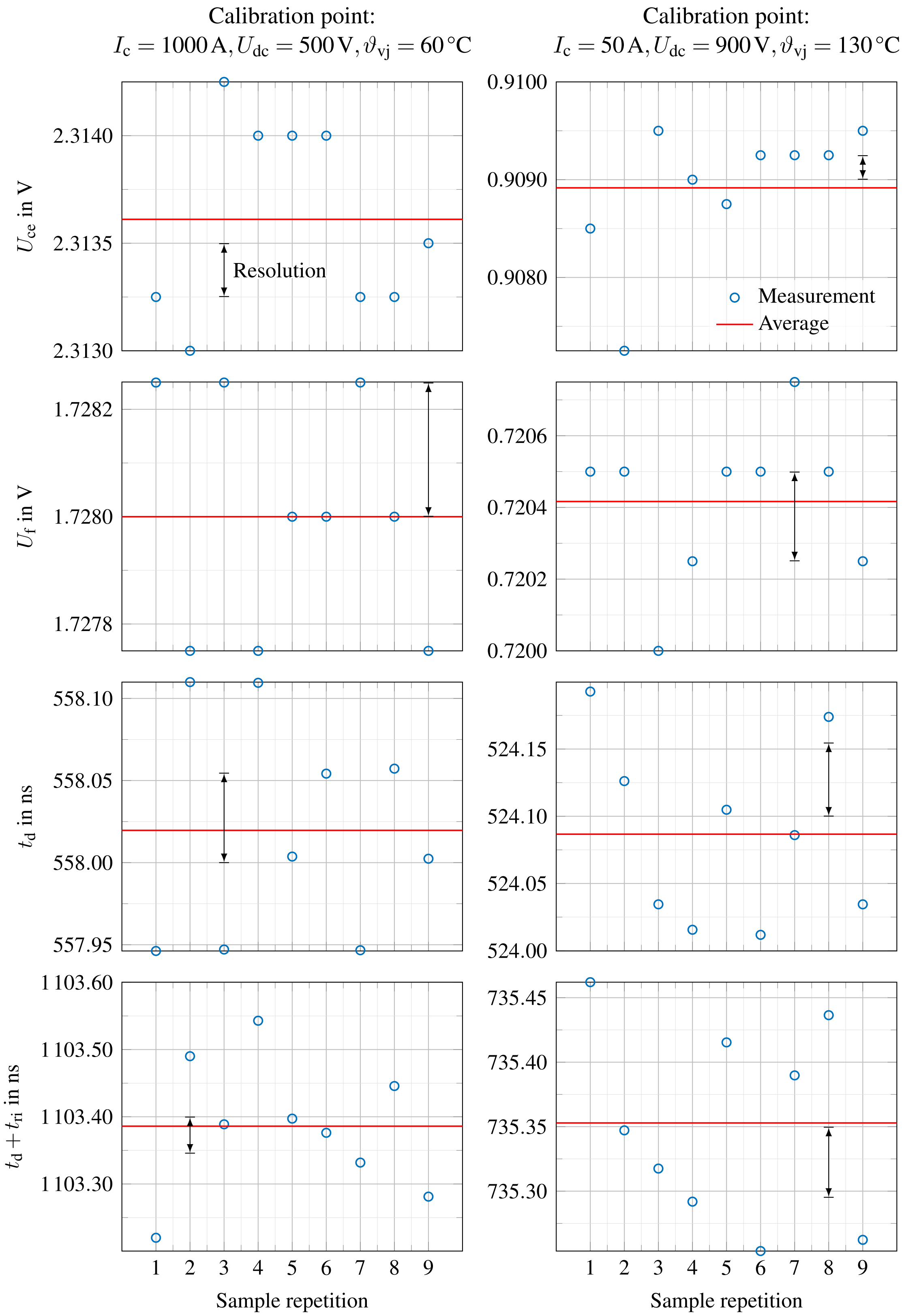


Figure 5.9: Repeated TSEP measurements at two calibration points; the ADC resolution is 0.25 mV; the TDC resolution is ≈55 ps, but varies in each sample [98]; the resolution is illustrated in each plot by black arrows; the varying resolution of the TDC leads to differences between the samples that are smaller than the nominal resoultion

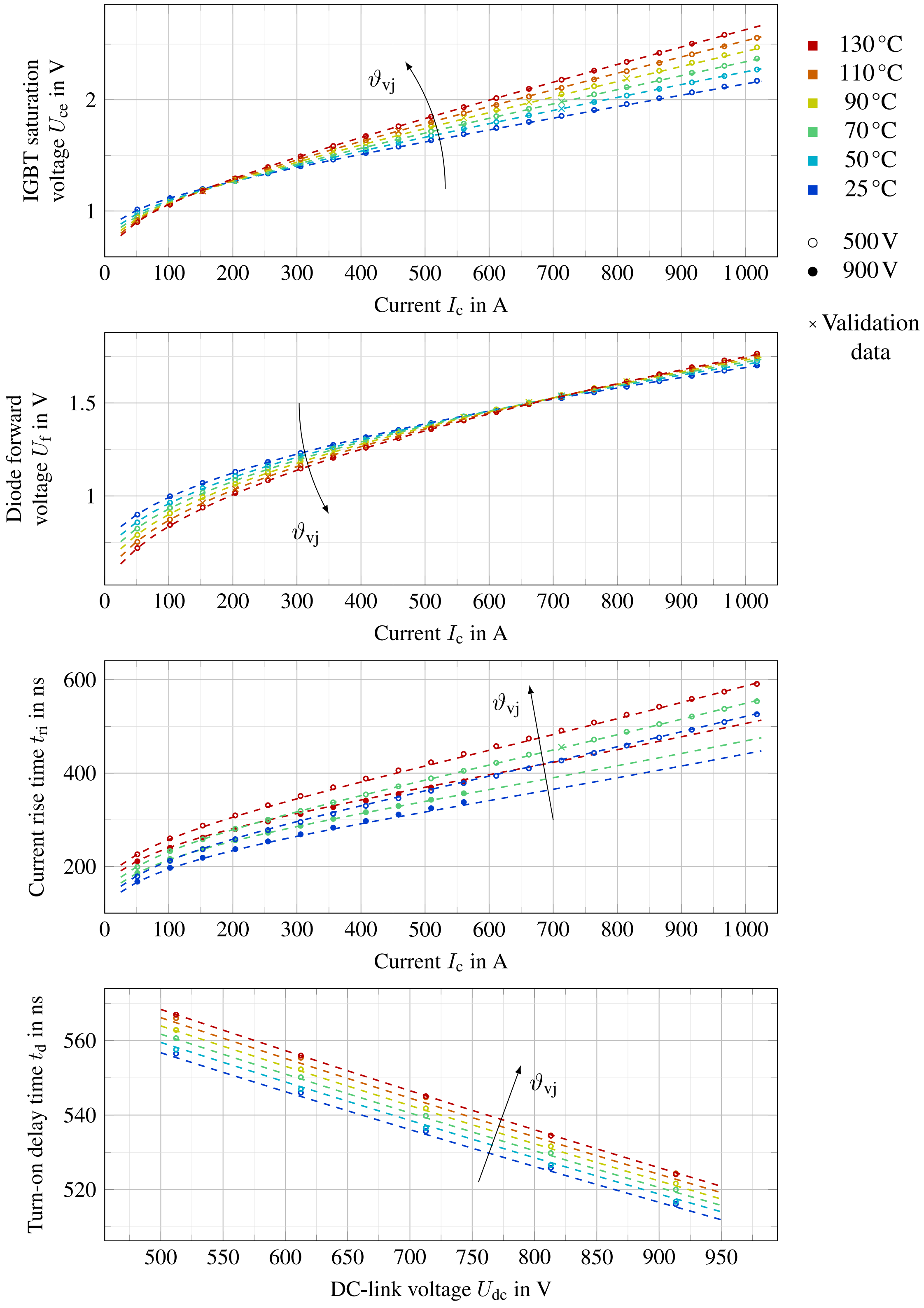


Figure 5.10: Example subset of acquired TSEP measurements using the preliminary TSEP measurement system in double-pulse experiments [89], [67]; fit results shown as dashed lines; data points excluded as validation data as diamonds; only an excerpt of the acquired measurements are shown; each calibration point is the average of up to ten repetitions of the same experiment

Fit functions The fit results (dashed lines) shown in Figure 5.10 use the following fit functions [67, 89]

$$\begin{aligned} U_{\mathrm{ce}}^{*}\left(I_{\mathrm{c}},\vartheta_{\mathrm{vj}}\right) =& a_1 + a_2\cdot\vartheta_{\mathrm{vj}} + a_3\cdot\vartheta_{\mathrm{vj}}^2 + \left(a_4 + a_5\cdot\vartheta_{\mathrm{vj}}\right)\cdot I_{\mathrm{c}} && (5.8)\\ &+ \left(a_6 + a_7\cdot\vartheta_{\mathrm{vj}}\right)\cdot\ln\left(I_{\mathrm{c}}/\left(1\,\mathrm{A}\right)\right), \\ U_{\mathrm{f}}^{*}\left(I_{\mathrm{c}},\vartheta_{\mathrm{vj}}\right) =& b_1 + b_2\cdot\vartheta_{\mathrm{vj}} + b_3\cdot\vartheta_{\mathrm{vj}}^2 + \left(b_4 + b_5\cdot\vartheta_{\mathrm{vj}}\right)\cdot I_{\mathrm{c}} && (5.9)\\ &+ \left(b_6 + b_7\cdot\vartheta_{\mathrm{vj}}\right)\cdot\sqrt{I_{\mathrm{c}}/\left(1\,\mathrm{A}\right)}, \\ t_{\mathrm{d}}^{*}\left(U_{\mathrm{dc}},\vartheta_{\mathrm{vj}}\right) =& c_1 + c_2\cdot U_{\mathrm{dc}} + c_3\cdot\vartheta_{\mathrm{vj}} + c_4\cdot U_{\mathrm{dc}}^2 + c_5\cdot U_{\mathrm{dc}}\cdot\vartheta_{\mathrm{vj}}, && (5.10)\\ t_{\mathrm{ri}}^{*}\left(I_{\mathrm{c}},U_{\mathrm{dc}},\vartheta_{\mathrm{vj}}\right) =& d_1 + d_2\cdot I_{\mathrm{c}} + d_3\cdot I_{\mathrm{c}}^2 + \left(d_4 + d_5\cdot I_{\mathrm{c}}\right)\cdot\vartheta_{\mathrm{vj}} && (5.11)\\ &+ \left(d_6 + d_7\cdot I_{\mathrm{c}}\right)\cdot U_{\mathrm{dc}} + \left(d_8 + d_9\cdot\vartheta_{\mathrm{vj}}\right)\cdot\sqrt{I_{\mathrm{c}}/\left(1\,\mathrm{A}\right)}. \end{aligned}$$

These specific fit functions are chosen from a pool of possible fit functions, ranging from simple to complex models [89]. First, the TSEP calibration data from the double-pulse experiments is separated into training (85 %) and validation data (15 %). For each TSEP the fit function with the best root-mean-square deviation (RMSD) on the validation data is chosen. All functions and results are listed in Appendix A.

> **Remark:** The validation data is selected from the range of temperatures, load currents and dc-link voltages applied during the double-pulse experiments. The IGBT saturation voltage and the diode forward voltage do not depend on the dc-link voltage, therefore the calibration data of these TSEPs contains multiple measurements at different dc-link voltages that are equivalent with regard to the fitting. If one calibration point is selected as validation data, all other points conducted at the same temperature and current, but different dc-link voltage, must also be selected to avoid unintended weighting, as described in Section 4.1. Analogously, the turn-on delay time does not depend on the load current, leading to multiple equivalent measurements due to the varied load current. [89]

Figure 5.11 shows the RMSD of the TSEP-based temperature estimation for each TSEP. The large peaks in the IGBT saturation voltage and the diode forward voltage are caused by

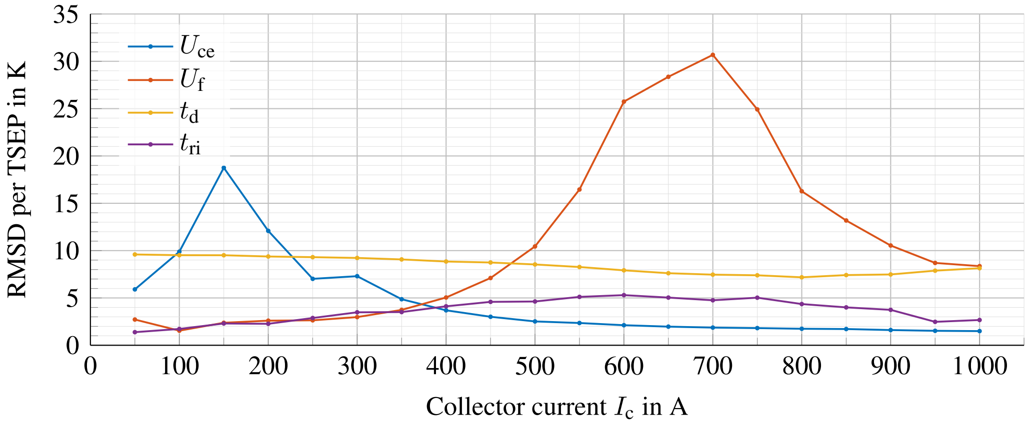


Figure 5.11: RMSD for each TSEP depending on the load current operating point [67, 89]

the polarity change in the temperature dependency of the IGBT's and the diode's on-state voltage, see Figure 5.10. When the load current is within the cross-over region of the temperature sensitivity of these parameters, the deviation goes to infinity and a pole would occur if no quantification or measurement noise was present. For the IGBT saturation voltage U_{ce}, this range is small and at low currents. This may not allow a temperature monitoring at low output currents of the system, but it does allow monitoring at high currents, and therefore high losses. The mission profile of the application must be considered when using this TSEP alone, to validate that the region of low load is left often enough to ensure degradation detection in time. The diode's range of low sensitivity is at high currents and it spans a more significant part of the operating range. Here, the comparatively high sensitivity at low currents can be used for degradation detection, as low currents occur periodically in an AC application. It can be seen that the IGBT saturation voltage U_{ce} has the smallest deviations at high currents, while the diode forward voltage U_{f} is better suited at low currents. The turn-on delay time t_{d} is generally less accurate than the other TSEPs. The current rise time t_{ri} shows a moderately low and consistent deviation across the entire current range. These results demonstrate the typically high RMSD of TSEP-based temperature estimations.

6 Combining multiple TSEPs

In the previous sections, double-pulse experiment results for four TSEPs have been presented. Each TSEP was evaluated independently, providing four separate virtual junction temperature estimates. During inverter operation, a single temperature estimate per topological switch, topological IGBT or topological diode is desired. In this chapter, different methods to combine the four TSEPs to gain a single virtual junction temperature estimate will be investigated and compared.

The central investigation will be whether ANNs are suited to combine multiple TSEPs into a single junction temperature estimate. As reference, it will be compared to a physics-based model , i.e., fit functions. Physical models incorporate knowledge of the underlying behavior of the semiconductors. Simple ANNs do not have, nor require, any knowledge of the underlying physics of the system which makes them easy to apply. Physics-based models can only fit those physical effects that are included in their models. Without detailed manufacturer information, some parameters or characteristics can only be estimated. If an insufficiently well modeled characteristic of the semiconductor becomes relevant for the fit accuracy, a physics-based model cannot compensate the discrepancy. It cannot be more accurate than the underlying models allow. ANNs are not restricted by imperfect models and are purely data driven, aside from design choices made for the ANN structure. This enables them to also fit semiconductor characteristics that are unknown, nonlinearities of the measurement hardware or even blatant mistakes by the engineer.

There also exist hybrid concepts, like physics-informed ANNs [100, 101], where ANN methods are merged with physical models. An example is the physics-guided neural networks (PGNNs). A simple approach presented for PGNNs is to fit the results with a physics-based model function first. Afterwards, the fit is used to create additional training data, mixing the measured data with model-based data points [102]. An ANN is now trained on the combined training data. Another approach presented in [102] is the disfavouring of ANN training results that violate known physical principals. For example, for the measured IGBT it is known that the current rise time t_{ri} increases strictly monotone with temperature and current. Any point in the ANN that would predict a current rise time t_{ri} decreasing with temperature or current would have significantly higher weight in the cost function, compare Section 4.2.1.1.

A further well-known option is the use of tracking filters with a predictor-corrector model. In [49], a single TSEP is combined with a thermal model using a Kalman filter. This concept could be extended to incorporate as many TSEP measurements as desired.

6.1 Physics-based model

The used analytical fit functions (5.8) to (5.11) have been introduced in the previous section. They represent the basis of the physics-based model. Each function can be solved for the temperature explicitly. The equations for the IGBT saturation voltage (5.8) and the diode forward voltage (5.9) are quadratic with respect to the temperature, leading to two solutions.

The selection of the correct branch will be discussed for the IGBT saturation voltage and can be applied to the diode forward voltage analogously.

$$\begin{aligned}\vartheta_{1,2}\left(U_{\mathrm{ce}}, I_{\mathrm{c}}\right) = & \\ & -\frac{a_2 + a_5 \cdot I_{\mathrm{c}} + a_7 \cdot \ln\left(\frac{I_{\mathrm{c}}}{1\,\mathrm{A}}\right)}{2 \cdot a_3} \\ & \pm \sqrt{\left(\frac{a_2 + a_5 \cdot I_{\mathrm{c}} + a_7 \cdot \ln\left(\frac{I_{\mathrm{c}}}{1\,\mathrm{A}}\right)}{2 \cdot a_3}\right)^2 - \frac{a_1 - U_{\mathrm{ce}} + a_4 \cdot I_{\mathrm{c}} + a_6 \cdot \ln\left(\frac{I_{\mathrm{c}}}{1\,\mathrm{A}}\right)}{a_3}}.\end{aligned} \tag{6.1}$$

The correct branch depends on whether the operating point is within the PTC or NTC range of the TSEP. Interestingly, the cross-over point ($I_{\mathrm{c,co}}$, U_{ce}) where the on-state voltage's behavior switches from NTC to PTC behavior is not at a fixed current

$$\frac{\mathrm{d}U_{\mathrm{ce}}\left(\vartheta_{\mathrm{vj}}, I_{\mathrm{c,co}}\right)}{\mathrm{d}\vartheta_{\mathrm{vj}}} \overset{!}{=} 0 \tag{6.2}$$

$$0 = a_2 + 2a_3\vartheta_{\mathrm{vj}} + a_5\vartheta_{\mathrm{vj}}I_{\mathrm{c,co}} + a_7 \ln\left(I_{\mathrm{c,co}}/\left(1\,\mathrm{A}\right)\right) \tag{6.3}$$

$$\Rightarrow I_{\mathrm{c,co}} = I_{\mathrm{c}}\Big|_{\frac{\mathrm{d}U_{\mathrm{ce}}}{\mathrm{d}\vartheta}=0} = f\left(\vartheta_{\mathrm{vj}}\right). \tag{6.4}$$

The cross-over point of the temperature sensitivity is temperature dependent. As a result, the range where the cross-over point may be located during operation is referred to as cross-over region. The locus curve of the point of temperature insensitivity is shown in Figure 6.1. The top graphs shows how the locus curve moves through the minima of the parabolic fit results before it leaves the range of feasible temperatures. The bottom graph shows how the cross-over point drifts within the U-I diagram. Of course, the precise shape depends on the chosen fit function.

Here, the correct branch of (6.1) can be determined, as the real current and temperature are known from the double-pulse experiment. The following investigations will assume that this is always the case. This results in a best-case scenario for the physics-based model.

During operation, the inverse problem must be solved. Only the current is known, while the temperature is to be determined, and therefore unknown[1]. In practice, the simplest solution is choosing one branch, when the operating point is clearly above the point of temperature insensitivity, i.e., $I_{\mathrm{c}} > 250\,\mathrm{A}$, and the other branch clearly below, i.e., $I_{\mathrm{c}} < 100\,\mathrm{A}$. In between, the estimation is unreliable anyway due to the low temperature sensitivity.

Weighted temperatures The four fit functions (5.8) to (5.11) cannot be explicitly combined to yield a single temperature estimate. Instead, all four TSEPs will be evaluated separately, yielding four separate temperature results $\vartheta_{\mathrm{vj}}^{(U_{\mathrm{ce}})}$, $\vartheta_{\mathrm{vj}}^{(U_{\mathrm{f}})}$, $\vartheta_{\mathrm{vj}}^{(t_{\mathrm{d}})}$ and $\vartheta_{\mathrm{vj}}^{(t_{\mathrm{ri}})}$. Figure 5.11 showed that the four TSEPs have varying accuracy depending on the operating point. Thus, the four temperature estimates will be weighted and averaged into a single temperature esti-

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[1] If a temperature observer or tracking filter is used, the existing temperature estimation may be used for the branch determination.

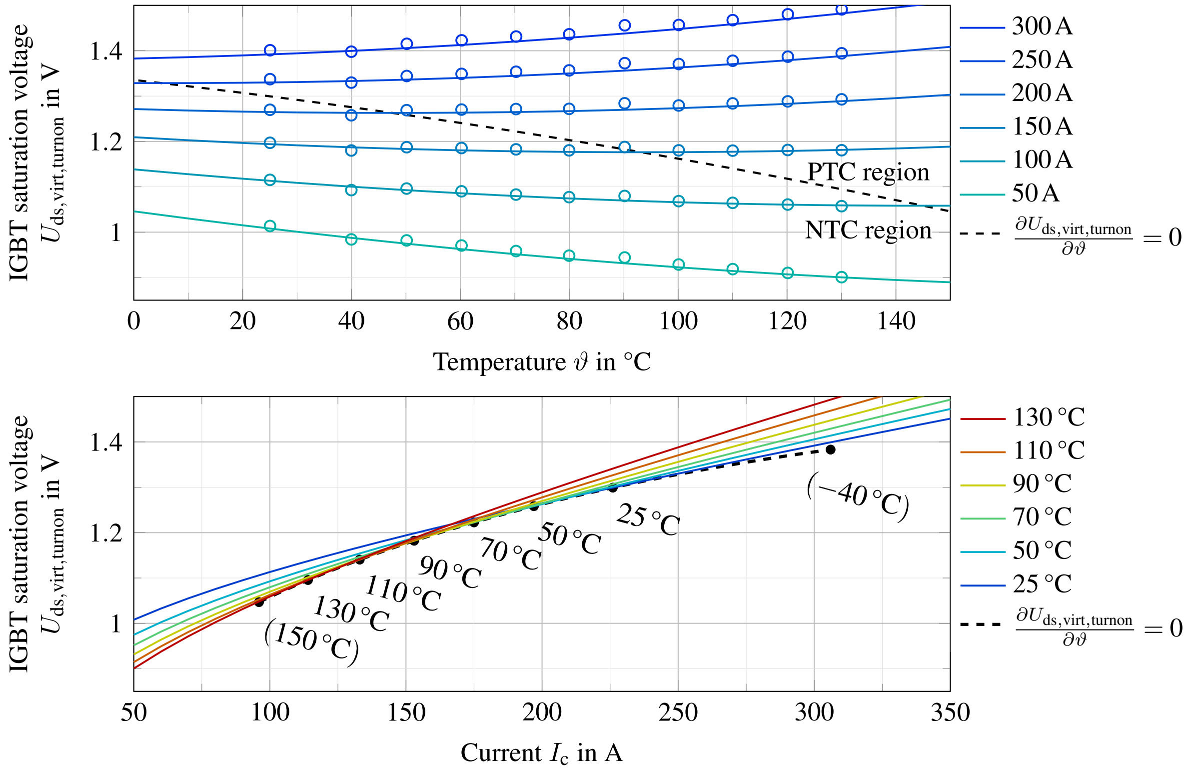


Figure 6.1: Locus curve of the point of temperature insensitivity [67]; values in brackets are extrapolated

mation $\vartheta_{\mathrm{vj,PM}}$, according to their expected RMSD at the current operating point

$$S_{\mathrm{TSEP}} := \{U_{\mathrm{ce}}, U_{\mathrm{f}}, t_{\mathrm{d}}, t_{\mathrm{ri}}\} \tag{6.5}$$

$$\vartheta_{\mathrm{vj,PM}} = \sum_{i \in S_{\mathrm{TSEP}}} \left(w^{(i)}(I_{\mathrm{c}}) \cdot \vartheta_{\mathrm{vj}}^{(\mathrm{i})} \right), \quad \text{with } w^{(i)}(I_{\mathrm{c}}) = \frac{1}{\mathrm{RMSD}^{(i)}(I_{\mathrm{c}})}. \tag{6.6}$$

Figure 6.2 shows the concept as a block diagram.

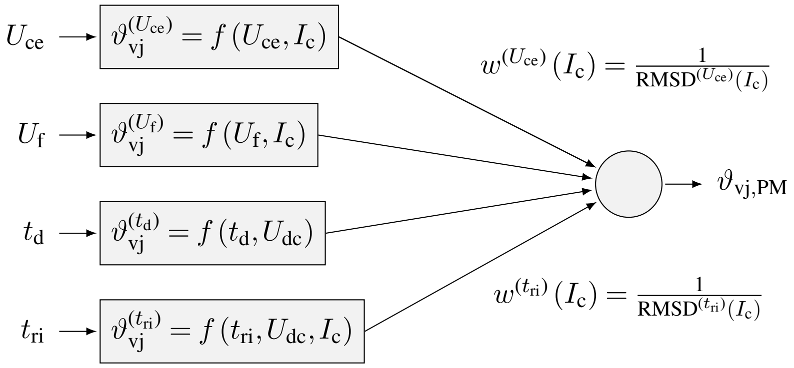


Figure 6.2: Concept of the weighted temperature estimates

6.2 Combination using an artificial neural networks

In contrast to the described physics-based model, an ANN-based approach does not require fit functions to describe the TSEPs. An ANN with a single hidden layer of six neurons and a hyperbolic tangent sigmoid as activation transfer function is used, in accordance with [91]. The ANN uses the four TSEPs S_{TSEP} (6.5), the load current I_{L} and dc-link voltage U_{dc} as inputs. It is trained using the double-pulse calibration data, mapping the six inputs to the baseplate temperature during calibration.

The ANN with six neurons has a total of $n_{\mathrm{par}} = 49$ fit parameters, while the physics-based model has only $n_{\mathrm{par}} = 28$. In order to compare the fit performance between the ANN-based approach and the physics-based model, an additional ANN with only three neurons and $n_{\mathrm{par}} = 25$ parameters will be trained. Furthermore, ANNs without the inverter sensors as inputs are trained, as well as ANNs that determine the load current and dc-link from the four TSEPs, compare Table 6.1.

Table 6.1: Overview of the compared models, inputs, outputs and the number of total parameters n_{par}

	Inputs	Outputs	n_{par}
Physics-based model	U_{ce}, U_{f}, t_{d}, t_{ri}, I_{c}, U_{dc}	$\vartheta_{\mathrm{vj,PM}}$	28
ANN with six neurons	U_{ce}, U_{f}, t_{d}, t_{ri}, I_{c}, U_{dc}	$\vartheta_{\mathrm{vj,ANN,full,6}}$	49
ANN with three neurons	U_{ce}, U_{f}, t_{d}, t_{ri}, I_{c}, U_{dc}	$\vartheta_{\mathrm{vj,ANN,full,3}}$	25
ANN with six neurons and no inverter sensors	U_{ce}, U_{f}, t_{d}, t_{ri}	$\vartheta_{\mathrm{vj,ANN,red,6}}$	37
Load current ANN	U_{ce}, U_{f}, t_{d}, t_{ri}	$I_{\mathrm{c,ANN}}$	37
DC-link voltage ANN	U_{ce}, U_{f}, t_{d}, t_{ri}	$U_{\mathrm{dc,ANN}}$	37

Figure 6.3 shows the deviation histograms of the trained ANNs and the physics-based model with regard to the temperature in double-pulse experiments. Figure 6.4 shows the RMSD of each combination method depending on the operating point. All combination methods show more consistent behavior across the range of load currents than the individual TSEPs in Figure 6.4. The results $\vartheta_{\mathrm{vj,ANN,full,6}}$ using the ANN with six neurons in the hidden layer show the lowest RMSD across the entire range. The reduced ANN with only three neurons in the hidden layer $\vartheta_{\mathrm{vj,ANN,full,3}}$ generally leads a lower RMSD than the physics-based model $\vartheta_{\mathrm{vj,PM}}$ with fewer fit parameters. This validates that the improved accuracy stems from the concepts of the ANN rather than the number of fit parameters. Even the ANN without the load current I_{L} and dc-link voltage U_{dc} information $\vartheta_{\mathrm{vj,ANN,red,6}}$ leads to good accuracy, ranging between the results of the full ANN $\vartheta_{\mathrm{vj,ANN,full,6}}$ and the physics-based reference model $\vartheta_{\mathrm{vj,PM}}$.

The deviation histogram of the ANNs predicting the load current and dc-link voltage from the TSEPs only are shown in Figure 6.5 The RMSD is surprisingly low, especially considering that the stated sensor accuracies are 8 A and 28 V. It must be kept in mind that

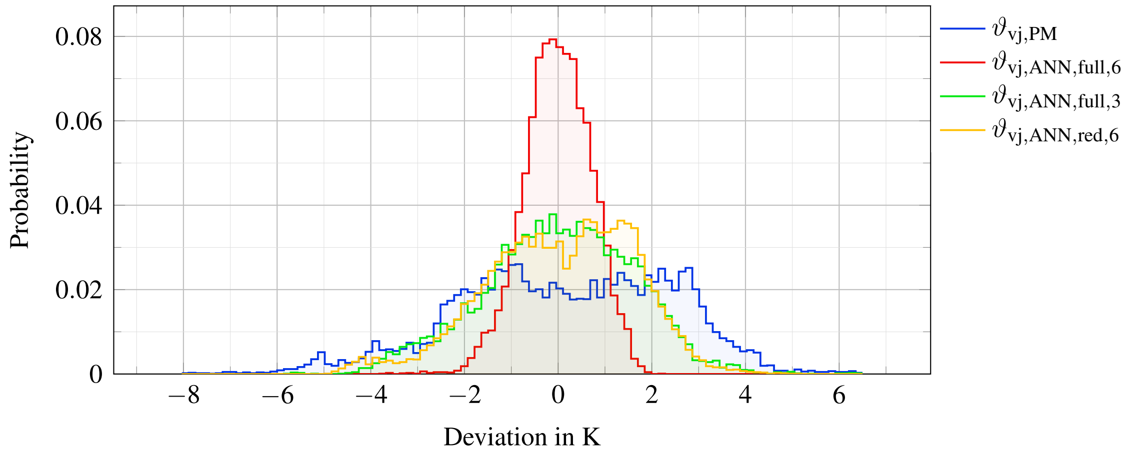


Figure 6.3: Deviation histogram of the trained ANNs and the physics-based model [67]; 100 bins used; 1620 sample points

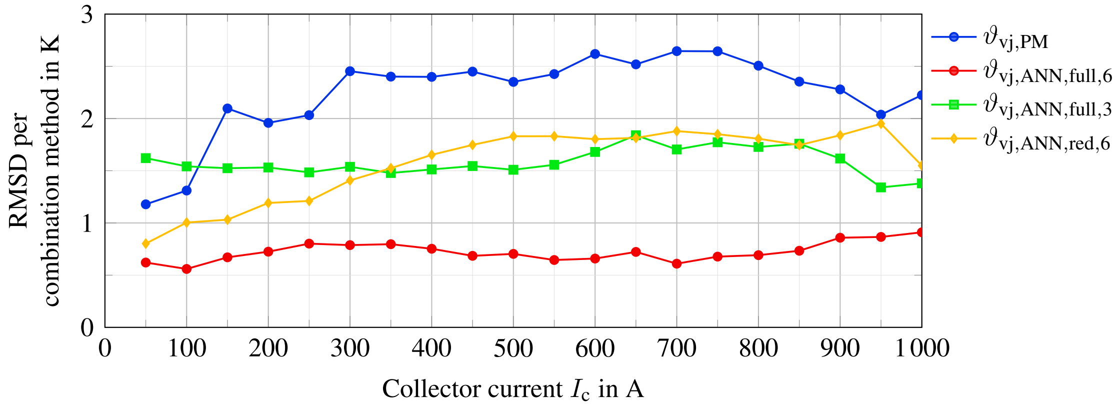


Figure 6.4: RMSD of the temperature estimation for the different combination methods [67]; 1620 sample points

the ANN's RMSD corresponds to the sensor precision, rather than accuracy. The fact that these two fits are this precise validates that the dependencies of the chosen subset of four TSEPs in Table 5.3 form a solvable system of equations.

The results are summarized in Figure 6.6 for comparison. It can be seen that the combination of TSEPs generally improves the fit accuracy. ANNs are easy to apply and have better RMSD than the physics-based model. The full ANN with six neurons $\vartheta_{\mathrm{vj,ANN,full,6}}$ has an RMSD below 1 K when fitting double-pulse calibration data. The RMSDs of the individual TSEPs $\vartheta_{\mathrm{vj}}^{(U_\mathrm{ce})}$ and $\vartheta_{\mathrm{vj}}^{(U_\mathrm{f})}$ include their poles when the temperature sensitivity crosses zero. Blanking the current ranges with high RMSD is an option, but a universally valid current limit cannot be defined in the context of this work. Especially the pole of the diode forward voltage $\vartheta_{\mathrm{vj}}^{(U_\mathrm{f})}$, shown in Figure 5.11, extends across half the operating range. For these reasons, the overall RMSDs of $\vartheta_{\mathrm{vj}}^{(U_\mathrm{ce})}$ and $\vartheta_{\mathrm{vj}}^{(U_\mathrm{f})}$ in Figure 6.6 misrepresent their behavior and would theoretically go to infinity.

Throughout the rest of this work, an ANN with six neurons in the hidden layer will be used to determine the virtual junction temperature $\vartheta_{\mathrm{vj,ANN,full,6}}$ if not stated otherwise. All four TSEPs and both inverter sensors are used as inputs.

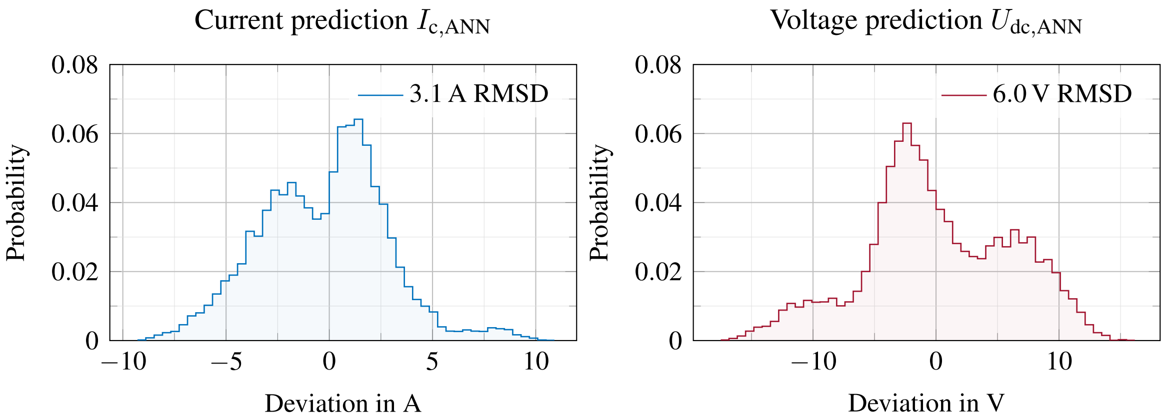


Figure 6.5: Deviation histograms of the predicted load current I_c and the dc-link voltage U_dc from the four TSEPs in double-pulse experiments

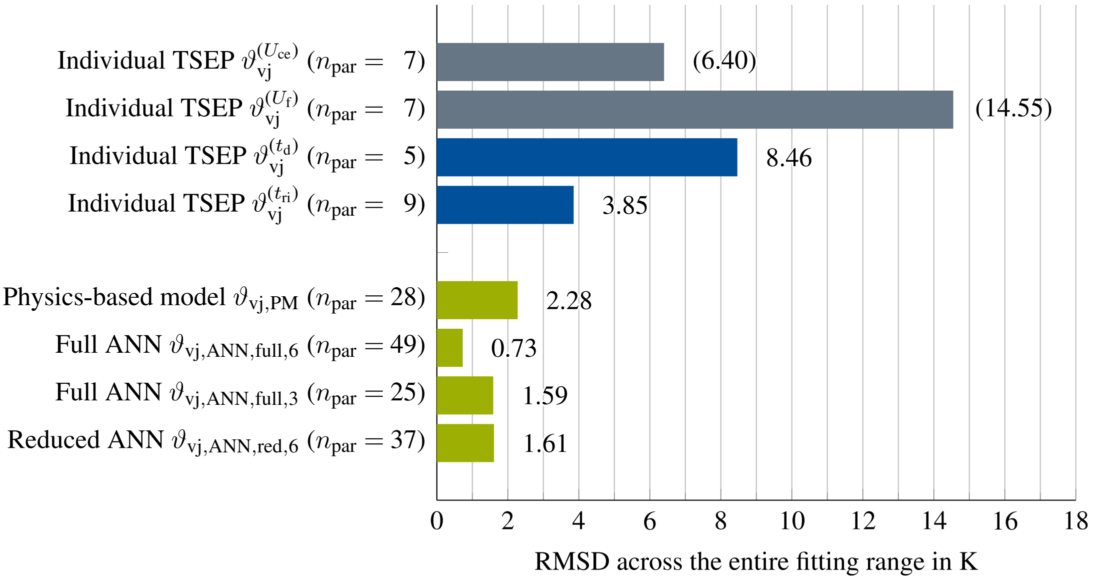


Figure 6.6: RMSD of the combination methods across the entire range of operation [67]; n_par is the number of fitting parameters used; $\vartheta_{\mathrm{vj}}^{(U_\mathrm{ce})}$ and $\vartheta_{\mathrm{vj}}^{(U_\mathrm{f})}$ include their pole

6.2.1 Disadvantages of using ANNs

The low RMSD of the ANNs in Figure 6.6 show that ANNs are a good option for TSEP calibration. However, there are more aspects to consider. So far, over 1600 calibration points with regard to temperature, load current and dc-link voltage were used as training data. Each calibration point is measured several times. It is expected that ANNs require a higher number of calibration points to provide good fit accuracy, whereas the physics-based model should be better suited for low numbers of calibration points due to the incorporated model of the TSEP characteristics. To investigate the required amount of calibration data, the ANN training and the physics-based model training has been repeated for different sets of available calibration data. The existing calibration data is thinned, by keeping the outer edges of current, voltage and temperature, while the data point density is reduced. The effects of reducing the range of calibration points will be investigated in a further paragraph.

Fitting ANNs is a nonlinear optimization problem and is prone to converge in *a* local minimum. Therefore, for each set of calibration points, the ANN is fitted 100 times with varying initializations to provide insight into the distribution of the fit quality. Figure 6.7 shows the resulting overall RMSDs of the ANNs and the physics-based model for a varying number of calibration points for training in a log-log plot. The RMSD is calculated over all 1620 calibration points of available data, so it introduces interpolation. The interquartile ranges of the ANNs generally show behavior similar to the physics-based model. The ANN begins to reliably generate more precise fits when the number of calibration data exceeds approximately 450 calibration points. At a low number of calibration points the median of the ANNs RMSD is generally higher than the results of the physics-based model. Here, the ANN fit performance varies widely with many insufficiently precise results. Interestingly, in every case an ANN could be found that has better RMSD than the physics-based model results, simply by retraining the net multiple times.

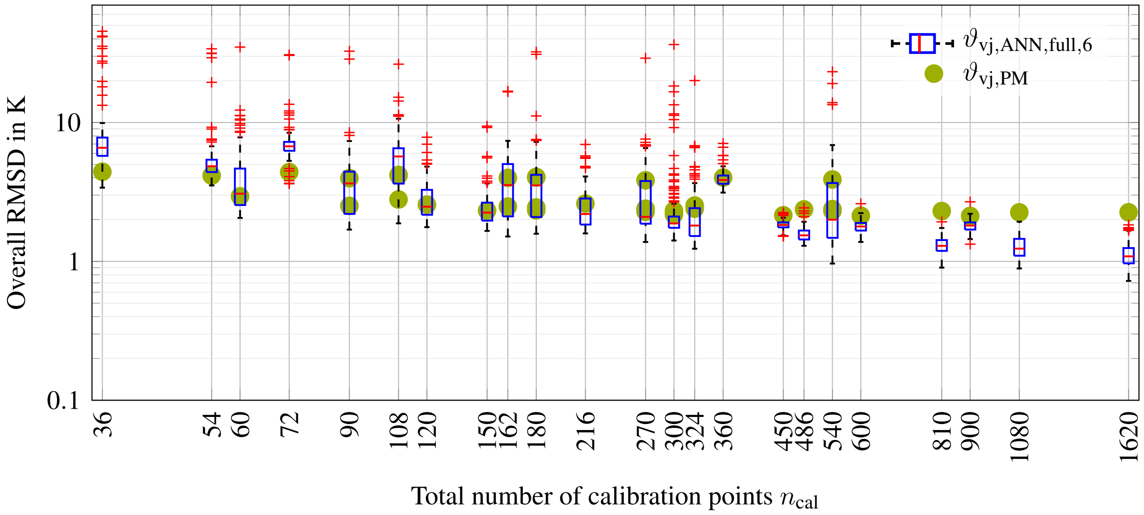


Figure 6.7: Overall RMSD of the fits depending on the used number of calibration points; the ANN is shown as box plot of 100 fit results; yellow circles mark the physics-based model result; 25th to 75th percentile in blue box; whiskers mark extreme data that s not yet considered outliers; outliers as red crosses; if the number of calibration points is matched by multiple combinations, the ANN results are merged into a single box plot, while multiple markers for the physics-based model are shown [67]

Identifying the best ANN on the reduced data set The RMSD shown in Figure 6.7, which was determined considering all available 1620 calibration points, illustrates how the fits may perform in the application. An important question is whether a sufficiently good ANN for the overall data could be identified based solely on the available, reduced calibration data set.

Figure 6.8 shows the RMSD of the fit results calculated from the reduced calibration data only. Considering only the reduced calibration data represents the situation where a suitable ANN must be chosen from the reduced number of calibration points and no other calibration points are known. For a high number of calibration points, the results are similar to those in Figure 6.7, as the difference in the underlying data set shrinks. On the reduced data set, even at low numbers of calibration points, the ANNs generally show a significantly lower RMSD. This is in stark contrast to the overall RMSD result in Figure 6.7. It illustrates that the ANN

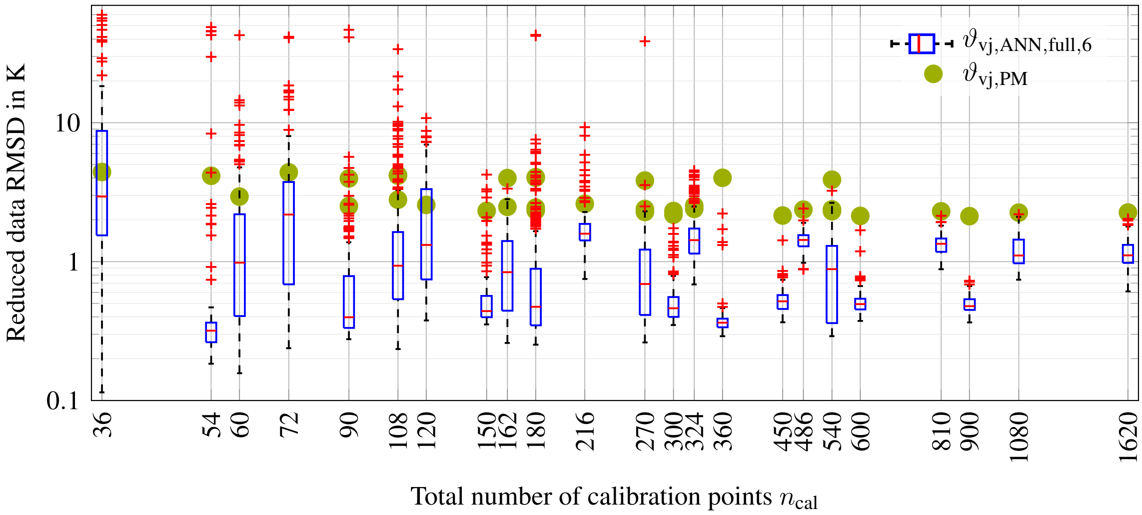


Figure 6.8: RMSD of the fits depending on the used number of reduced calibration points on the reduced calibration data set only; ANN results generally better than physics-model based results; otherwise matches Figure 6.7

precision on small sets of calibration data may seem very good, but larger deviations may occur in the application.

In order to assess how a low RMSD on the reduced training data correlates to the RMSD on the overall data set of 1620 points, scatter plots are created. Figure 6.9 shows these scatter plots of the achieved RMSD on the reduced number of calibration points compared to the overall RMSD on all available calibration points. The red points mark the ANN that would have been chosen based on the lowest RMSD on the calibration data set. The green point marks the best known ANN for the overall data, i.e., the lowest RMSD on the overall data set.

While the correlation is low at low numbers of used calibration points, at 1080 calibration points the correlation is high. Whether this is caused by actually including enough data points or simply by approaching the reference of 1620 calibration points cannot be assessed. In the cases of $n_{\mathrm{cal}} = 108$ and $n_{\mathrm{cal}} = 270$, large discrepancies between the performance of the selected ANN and the best known ANN occurs.

If only the reduced calibration data was available, the ANN with the lowest RMSD on the reduced calibration might be chosen as best fit, which is not necessarily the best result on the overall data. Figure 6.10 shows the performance of the ANNs that would have been chosen by selecting the ANN with the lowest RMSD on the reduced calibration data set (red crosses). The ANN selected solely on the reduced calibration data seems to correspond to a good match in overall performance when choosing at least 360 to 600 sample points.

Extrapolation drawbacks The previous investigations considered a thinned out calibration data set, where the calibration points at the minimum and maximum current, dc-link voltage and temperature are always kept. When calibrating TSEPs, conducting multiple measurements at different load currents or dc-link voltages can be done in rapid succession. Acquiring calibration data at different temperatures is time consuming, considering the high thermal time constants of a module and the required hot plate, compared to the duration of a double-pulse experiment. Therefore, it would be advantageous if not the entire range of possible operating temperatures had to be mapped. Very high or very low temperatures

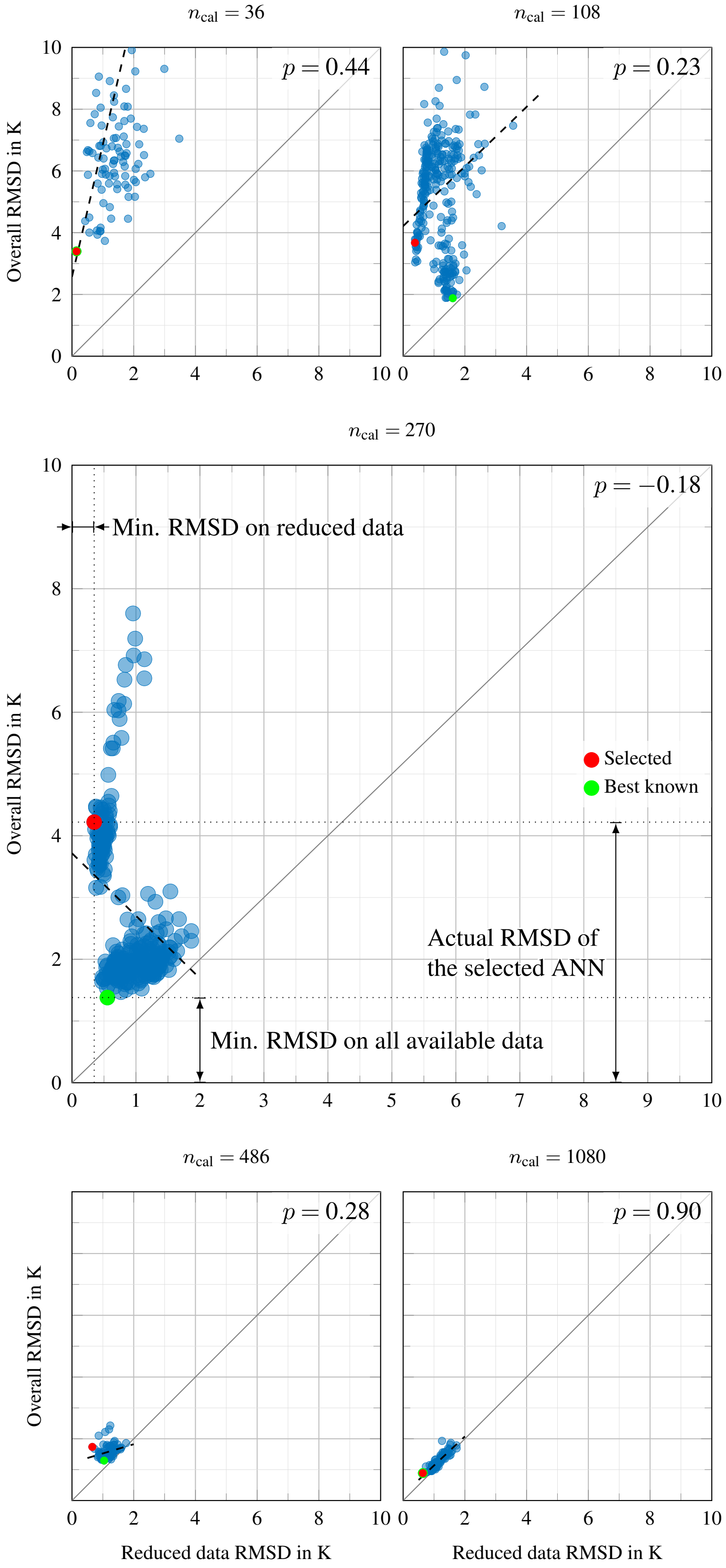


Figure 6.9: Scatter plots of the achieved RMSD for a reduced number of calibration points (n_{cal}) and the overall RMSD for all available calibration points (1620), as well as the Pearson correlation coefficient p

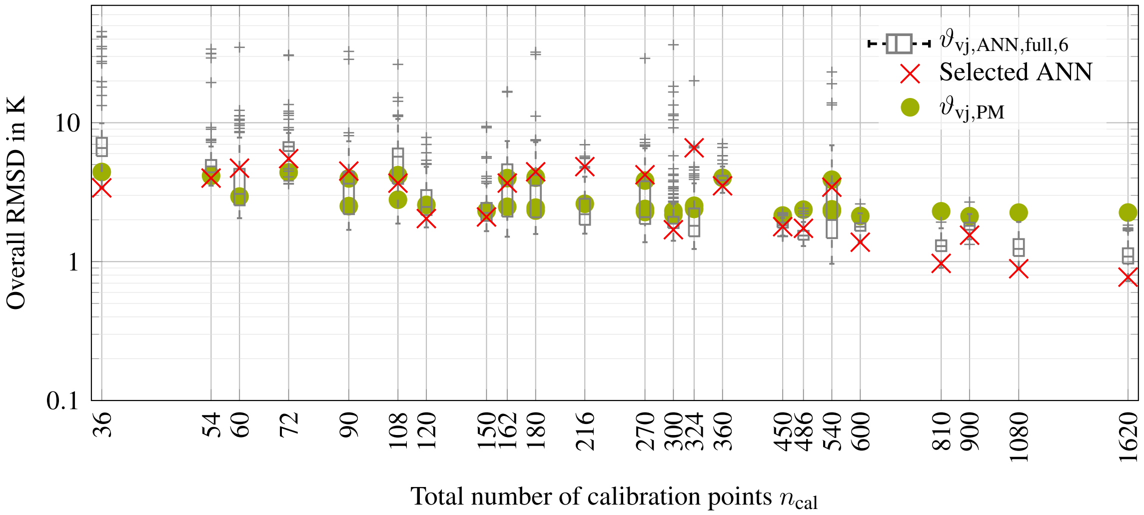


Figure 6.10: Selected ANNs based on the lowest RMSD on the reduced number of calibration points; RMSD of the validation data is shown; gray data only shown for reference and is equal to Figure 6.7

could be extrapolated, depending on the required accuracy.

In this paragraph, the calibration point density will be kept, but the maximum range of calibration points will be reduced. The physics-based model and the ANN will be retrained and refitted on the reduced calibration range only and their performances compared in the extrapolated regions. The results are shown in Figure 6.11. The ANN with only three

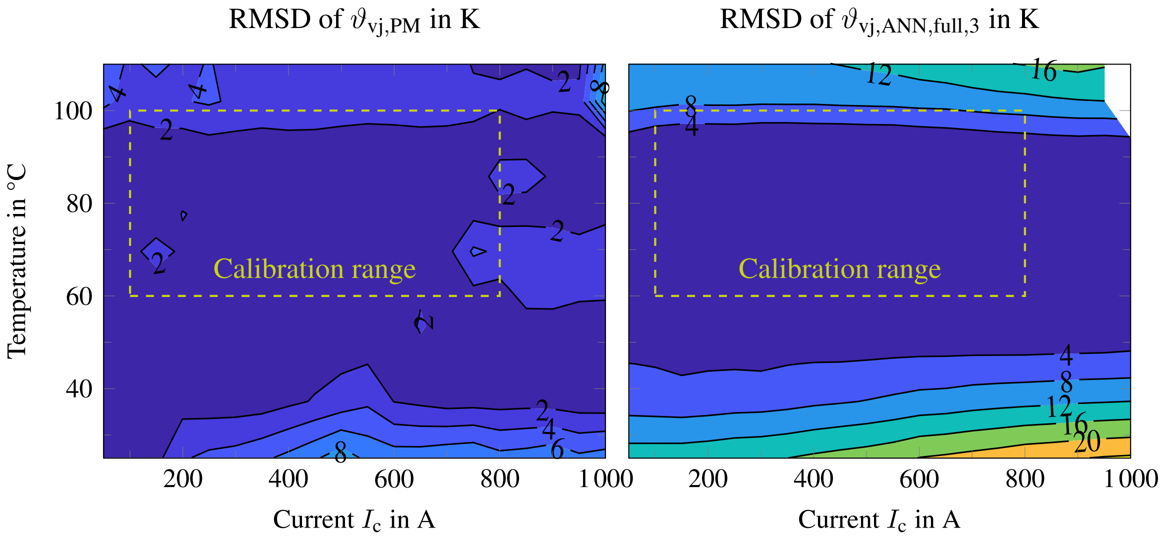


Figure 6.11: RMSD in extrapolated regions for the physics-based model $\vartheta_{\mathrm{vj,PM}}$ and the ANN $\vartheta_{\mathrm{vj,ANN,full,3}}$ [67]

hidden neurons is chosen in order to have a similar amount of fit parameters in both cases. It can be seen that the RMSD of the ANN in the extrapolated region is significantly higher than the physics-based results. A physics-based model can extrapolate farther than an ANN and could therefore be calibrated with a smaller range of calibrated temperatures. As a consequence, the calibration effort can be reduced when using physics-based models.

7 Parasitic impacts

As mentioned in Chapter 1, the low temperature sensitivity and high cross-sensitivities of TSEPs lead to a low signal-to-noise ratio. In order to find possible sources of parasitic impacts on TSEP-based temperature estimations, an analytical model of the turn-on time will be created. Expected impacts include variations in the gate driver voltages, changes in the gate resistance and current sensor inaccuracies. The size of these impacts will be measured on the available commercial hardware.

7.1 Measured parasitic impacts

Internal Gate Resistance The IGBT under test is a large power module variant consisting of six paralleled DCB substrates, or IGBTs and diodes respectively. It has discrete internal gate resistors for each DCB substrate, see Figure 7.1 and Figure 7.2a. The discrete resistors are used to synchronize the switching times of the distributed IGBT chips and to dampen oscillations between the separate gate loop segments. The temperature dependency of the overall internal gate resistance depends on both the on-chip resistance and the discrete resistors mounted on the DCB substrate. During calibration in double-pulses, the entire module is at a homogeneous temperature. Thus, the discrete resistors and the semiconductor chips are at the same temperature. During operation, losses heat up the semiconductor chips significantly compared to the baseplate temperature ϑ_{bp}. This causes a discrepancy between the calibration data and the measured switching times in continuous PWM operation.

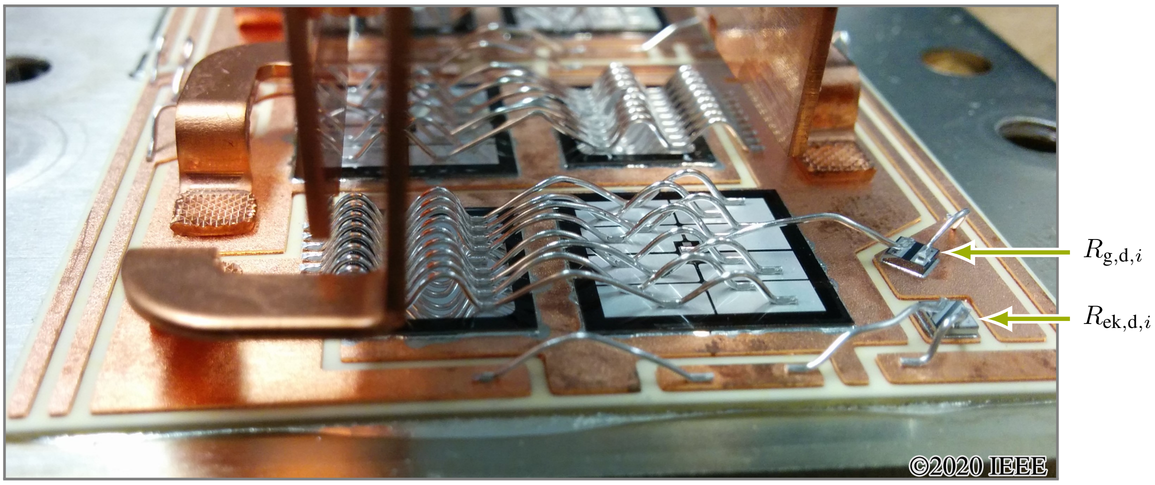
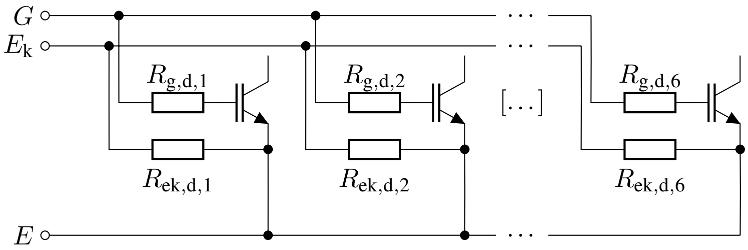
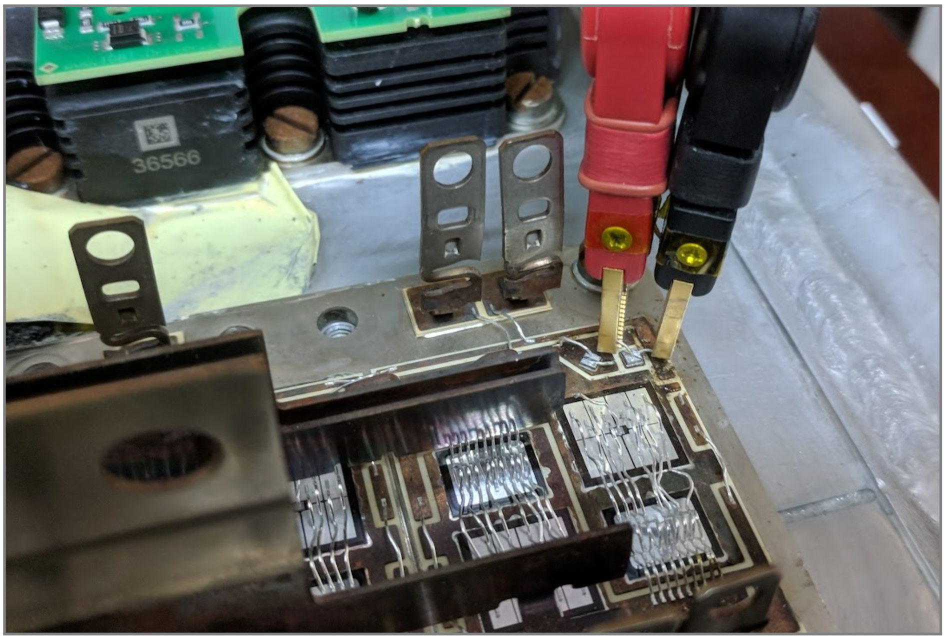


Figure 7.1: Photo of the discrete internal resistors mounted on each DCB substrate [103]

In order to estimate this effect, an IGBT module is opened and the bond wires are cut, see Figure 7.2b. The temperature dependency of the discrete resistors is measured. The results are shown in Figure 7.3. The measurement is done on the DCB substrate closest to the gate and Kelvin emitter terminals. The overall resistance of one DCB substrate is in the order of



(a) Schematic of the discrete internal resistors in the context of the module's gate loop [103]; collector path not shown



(b) Photo of the isolated discrete resistors $R_{\text{g,d},i}$ and $R_{\text{ek,d},i}$ being measured at different temperatures

Figure 7.2: Schematic of the gate loop and measurement setup

9 Ω [104], which includes the on-chip resistance of the IGBT chip in addition to $R_{\text{g,d},i}$ and $R_{\text{ek,d},i}$. Although the variation in the discrete resistors with temperature is small compared to the overall resistance of a DCB substrate, it will be shown that this deviation can cause a temperature estimation error of several kelvin at the end of this section.

Gate Driver Voltage The gate driver voltages are expected to have significant impact on most TSEPs. They vary with the switching frequency and the ambient temperature of the driver. In order to determine the size of these variations, the available driver, see Table 5.1, is placed in a laboratory oven. An RC element is attached externally, matching the load caused by the gate charge of the IGBT module.

The temperature and switching frequency of the driver is varied. Figure 7.4 shows the measured positive and negative gate driver voltage levels. The positive gate driver voltage shows remarkable stability at the nominal operating point in PWM at 1 kHz. It can be seen that there is a large voltage step between idle operation at 0 Hz and the nominal operating point. This effect has a significant impact when transferring calibration data acquired in double-pulse experiments to regular continuous PWM operation. In double-pulse experiments, the system is mostly idling and then loaded with a single double-pulse. The changing

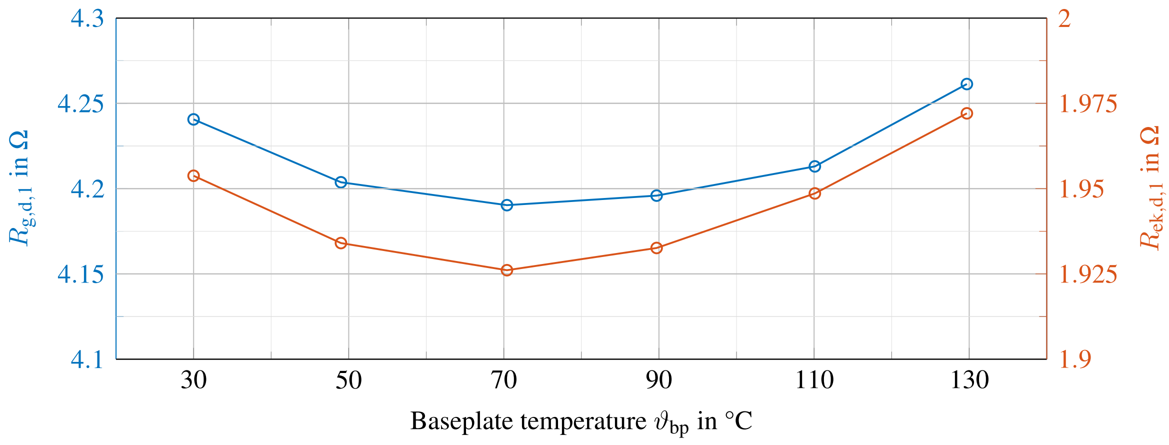


Figure 7.3: Measured resistance of $R_{g,d,1}$ and $R_{ek,d,1}$ depending on the baseplate temperature [103]

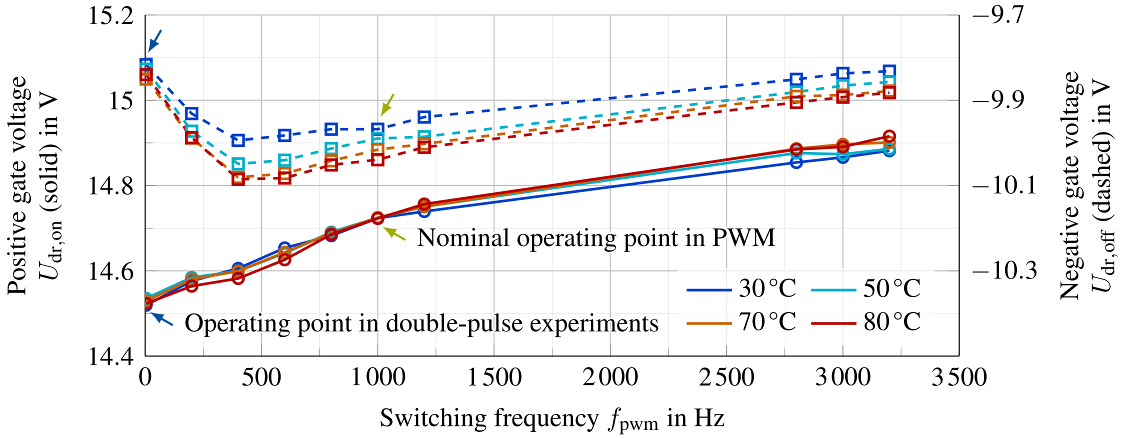


Figure 7.4: Measured gate driver voltages at different temperatures and switching frequencies [103]; matching scales; the matching drift in both voltage rails indicates a drifting ground potential; duty cycle fixed at 50 %; output loaded with 330 nF

positive gate driver voltage will impact switching times as well as the on-state voltage of the IGBT.

The positive and negative gate driver voltage change with the switching frequency. Interestingly, both drift by a similar amount. This indicates that the effects are not a typical drop or increase in supply voltage, but rather a shift in the virtual ground generated on the driver.

Duty cycle dependency The effects of the discrepancy between idle and continuous PWM operation could be mitigated by preloading the driver before executing a double-pulse. To investigate the feasibility of this strategy, the driver was mounted on an IGBT module and switched at nominal switching frequency without a load current. During these experiments, also the stability of the gate driver voltages with regard to the applied duty cycle was measured [89]. Trying to compensate the voltage step between idle and continuous PWM operation was discarded, as the duty cycle dependent gate driver voltage instabilities have been found to be even more significant, requiring an external stabilization of the voltage rails anyway.

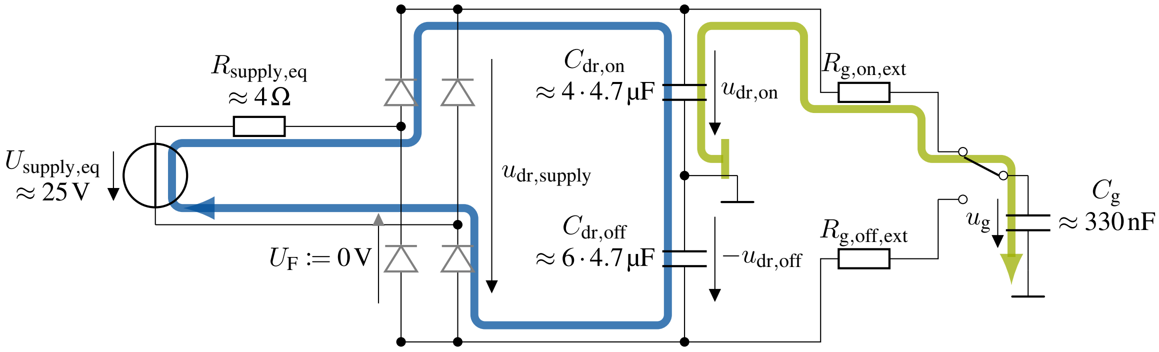


Figure 7.5: Schematic of the gate driver's supply; at turn-on, only $C_{\mathrm{dr,on}}$ is discharged (green); afterwards, both capacitors are recharged from the supply (blue); capacitor values measured on the PCB; voltage source equivalent estimated from measured time constant $\tau_{\mathrm{dr,supply}}$

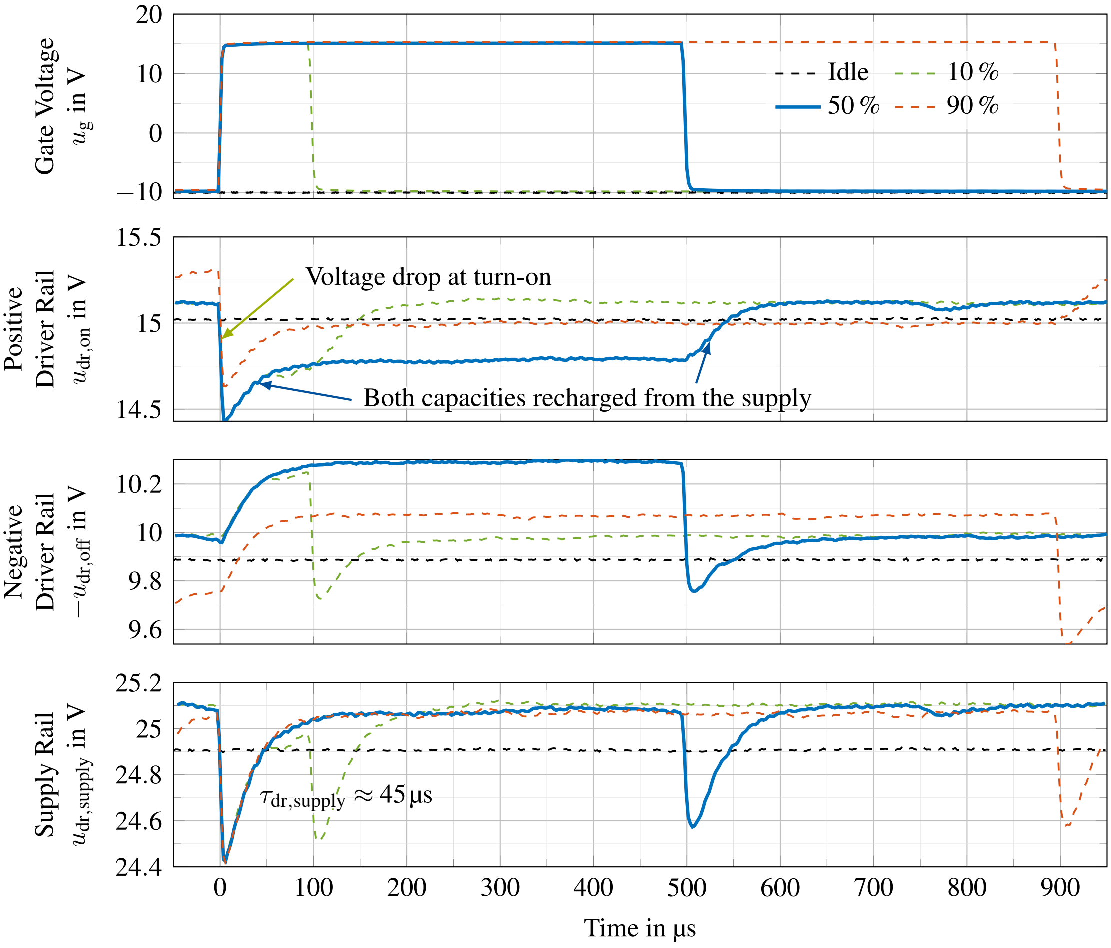


Figure 7.6: Gate driver voltage rails during PWM at varying duty cycles [89]; $u_{\mathrm{dr,off}}$ negated to match Figure 7.5

The driver uses a single supply voltage and generates a floating ground instead of a bipolar voltage supply [105]. Figure 7.5 shows a schematic of the gate driver's voltage supply. A transformer with a rectifier is used as input. As a simplification, this is represented by a Thévenin-equivalent DC voltage source, with the diodes neglected. The positive voltage rail $u_{\mathrm{dr,on}}$ and the negative voltage rail $u_{\mathrm{dr,off}}$ are decoupled by the capacitances $C_{\mathrm{dr,on}}$ and $C_{\mathrm{dr,off}}$. The ground level is not stiff, as it is formed by the middle connection between the positive and negative voltage capacitances. Additional, long-term stabilization circuits, which are acting over the course of several PWM periods, are neglected in this model.

When the IGBT is turned on, $C_{\mathrm{dr,on}}$ is discharged and $u_{\mathrm{dr,on}}$ drops. The negative supply $u_{\mathrm{dr,off}}$ does not change during this process. Afterwards, the overall voltage $u_{\mathrm{dr,supply}} = u_{\mathrm{dr,on}} - u_{\mathrm{dr,off}}$ is lower than steady-state and is recharged from the supply. The recharge current flows through both capacitances $C_{\mathrm{dr,on}}$ and $C_{\mathrm{dr,off}}$ in series. This leads to a recharging of the negative voltage rail capacitance $C_{\mathrm{dr,off}}$, even though it did not lose any charge. The result is a shifting of the virtual ground depending on the switch state of the IGBT.

The measured positive and negative gate driver voltage rails are depicted in Figure 7.6. The graphs show a fast voltage drop when the IGBT is turned on and the following slow charge phase of both capacitances. The time constant of the recharging process $\tau_{\mathrm{dr,supply}}$ is approximately 45 ns. The positive gate driver voltage also exhibits varying steady-state voltage levels when the switch is fully turned on, which affects on-state voltage measurements.

The positive and negative gate driver voltage rail is measured right before turn-on. The extracted levels of the positive and negative gate voltage rail vary significantly, see Figure 7.7. The variations are larger than 200 mV. They are especially high at very small or large duty cycles, when a switching process occurs before the recharging process of the driver capacitances has settled.

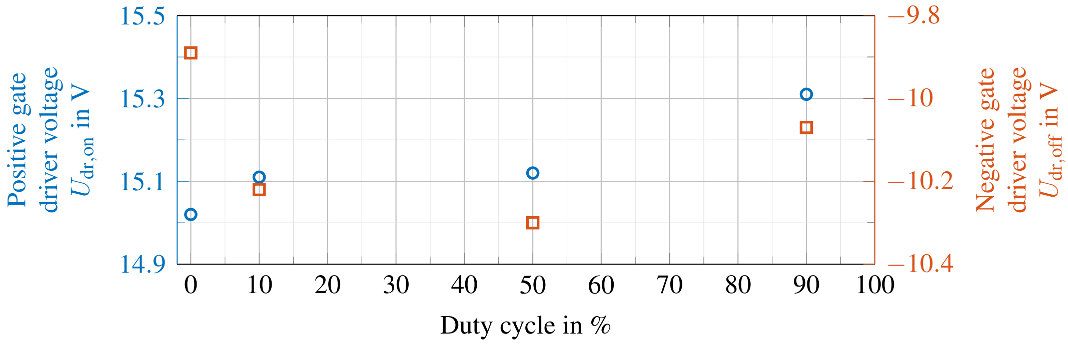


Figure 7.7: Positive and negative gate driver voltage levels before turn-on [103]

The observed variations in the gate driver voltage supplies of a commercial driver are expected to have significant impact on most TSEPs, e.g., switching times and on-state voltages. For the driver design for the SiC MOSFET module, the driver voltages will be stabilized.

7.2 Turn-on process system model

In this chapter, an analytical model of the turn-on process will be developed. It focuses on the charging process with respect to the gate loop. Here, the threshold voltage U_{th} and

Miller plateau voltage U_{M} are used as independent input parameters for the model. This system model will be extended by the underlying semiconductor characteristics of the threshold voltage $U_{\mathrm{th}} = f_1\left(\vartheta_{\mathrm{vj}}\right)$ and Miller plateau voltage $U_{\mathrm{M}} = f_2\left(\vartheta_{\mathrm{vj}}, I_{\mathrm{c}}\right)$ for a more detailed analysis in Section 9.3.

The model is shown in Figure 7.8. The gate driver power supply is modeled only by

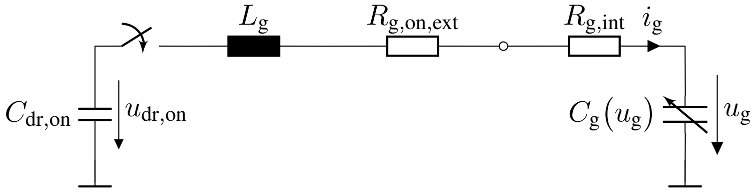


Figure 7.8: Model of the gate loop [103]

its decoupling capacitor $C_{\mathrm{dr,on}}$, precharged to the positive gate driver voltage $U_{\mathrm{dr,on}}$. It is assumed that the dominant part of the charge current is solely provided by this capacitance. The driver voltage is allowed to collapse during turn-on. The total gate loop resistance R_{g} is split into two parts, the external gate resistance $R_{\mathrm{g,on,ext}}$ and the internal gate resistance $R_{\mathrm{g,int}}$. These two components can have different temperatures. As described at the beginning of this section, the internal resistance itself is composed of the on-chip resistance of the six paralleled IGBT chips and the discrete gate resistors inside the module. The gate capacitance is modeled as a nonlinear capacitance C_{g} with respect to the gate voltage U_{g}. Gate loops are usually trimmed to switch the device as fast as possible, without causing oscillations of the gate loop. Therefore, the gate loop inductance L_{g} is expected to have a noteworthy impact on the switching behavior. Feedback due to the magnetic coupling between the collector-emitter path and the gate loop is not included. An evaluation of the feedback effect will be shown for the SiC device in Section 9.6. The parameters will be determined according to Table 7.1.

Table 7.1: Used sources or methods for parameter determination

Parameter		Method/Source
Driver gate capacitance	$C_{\mathrm{dr,on}}$	Driver datasheet, PCB
Gate loop inductance	L_{g}	Impedance analyzer
External gate resistor	$R_{\mathrm{g,on,ext}}$	Driver datasheet
Internal gate resistor	$R_{\mathrm{g,int}}$	Measured on DCB level
Gate capacitance	$C_{\mathrm{g}}\left(U_{\mathrm{g}}\right)$	Charge curve measurement
Gate driver voltage	$U_{\mathrm{dr,on}}, U_{\mathrm{dr,off}}$	Measurement

Gate capacitance The gate capacitance is measured using the setup in Figure 7.9. The gate is charged slowly with a 1 Hz triangular signal u_{sig}. Using a large charge resistor R_{charge}, the gate current i_{g} can be determined and integrated to the gate charge q_{g}. A large resistor is

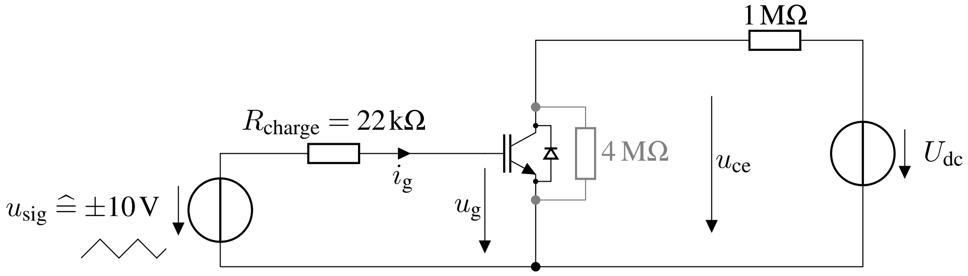


Figure 7.9: Gate charge measurement setup [106]; the voltage probe had a notable input resistance of 4 MΩ.

added to the collector to limit the current and the losses during the very slow switching processes [106]. Alternatively, a current limiter in the dc-link voltage source can be used [107]. The resulting gate charge measurement at ambient temperature for different collector-emitter voltage levels is depicted in Figure 7.10. The nonlinearity of the gate capacitance can be approximated by a piecewise linear function with $C_{\mathrm{g},1}$ and $C_{\mathrm{g},2}$. The voltage where the piecewise linear phases are switched is the flat-band voltage U_{fb}. The flat-band voltage U_{fb} that needs to be applied to the gate-emitter path changes with the collector-emitter voltage and the temperature. For subsequent investigations, U_{fb} is assumed constant. When the Miller plateau voltage U_{M} is reached, the collector-emitter voltage drops, keeping the gate voltage almost constant. Only the part until the Miller plateau is reached needs to be modeled for the planned investigation, as the voltage fall time is not considered in the TSEP analysis.

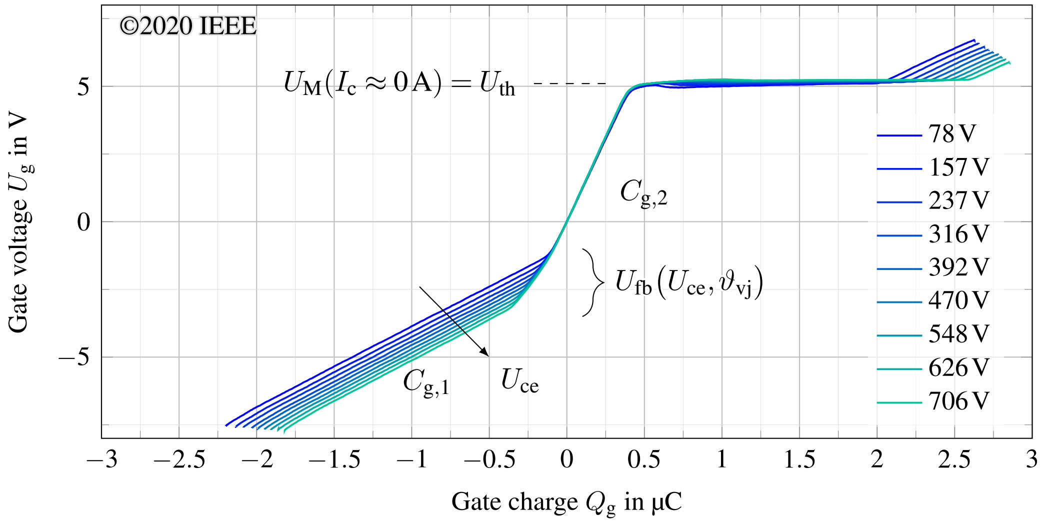


Figure 7.10: Measured gate charge curves at ambient temperature for different dc-link voltages U_{ce} [103]

Remark: At this point, only a short overview of the nonlinear effects of the gate charge profile is given. The nonlinear behavior of the gate capacitance and the flat-band voltage will be explained in detail in Section 8.1.3. The gate charge measurement setup and further effects relevant to SiC devices will be discussed in detail in the context of the SiC MOSFET models in Section 9.2.

Table 7.2: Parameters used for the the sensitivity analysis [103]; U_fb was chosen to match the behavior at the highest voltage measured in Figure 7.10, as it is most representative of typical operating conditions of the module.

$U_\text{dr,on,0}$	$U_\text{dr,off,0}$	R_g	$C_\text{dr,on}$	U_fb
15 V	−10 V	3 Ω	4 · 4.7 µF	−2.75 V
L_g	$C_\text{g,1}$	$C_\text{g,2}$	$i_\text{g}(t=0)$	$i_\text{g}(t=t_\text{fb})$
75 nH	337.5 nF	81.1 nF	0 A	8 A

Gate loop inductance Gate loops are generally trimmed to be as fast as possible. The parasitic gate loop inductance may have a noteworthy impact on the switching behavior. It can be assumed that a well-designed gate circuit has a damping $\zeta \geq 1$ [7]. Therefore, the largest expected gate loop inductance is

$$\max\left(L_\text{g}\right) = \frac{\left(R_\text{g,on,ext} + R_\text{g,int}\right)^2 C_\text{dr,on} C_\text{g}}{4\left(C_\text{dr,on} + C_\text{g}\right)}. \tag{7.1}$$

The gate loop inductance is measured using an impedance analyzer. The IGBT module is directly attached to the analyzer with its gate and Kelvin emitter contacts while the collector-emitter path is shorted. The impedance of the driver PCB is neglected, due to the small size compared to the extended size of the IGBT module. The inductance is evaluated at high frequencies, close to the resonant frequency of the gate loop. In the ranges where the inductive component could be identified in the gate loop impedance, a significant frequency dependency is observed. Whether this effect is caused by current displacement effects or the frequency dependency of the gate capacitance is unclear. Measurement details are listed in Appendix B. The estimated result are listed in Table 7.2.

7.2.1 Model equations

The model in Figure 7.8 leads to a linear differential equation of second order and an initial value problem [103]. The underlying differential equation is

$$u_\text{dr,on} = \dot{i}_\text{g} L_\text{g} + R_\text{g} i_\text{g} + u_\text{g}, \quad i_\text{g} = \dot{u}_\text{g} C_\text{g}. \tag{7.2}$$

The two capacitances $C_\text{dr,on}$ and C_g are not independent. Any charge sourced from one capacitance must be sunk into the other

$$u_\text{dr,on} = u_\text{dr,on}(t=0) - \frac{1}{C_\text{dr,on}} \int i_\text{g} \mathrm{d}t, \tag{7.3}$$

$$u_\text{g} = u_\text{g}(t=0) + \frac{1}{C_\text{g}} \int i_\text{g} \mathrm{d}t \tag{7.4}$$

$$\Leftrightarrow \int i_\text{g} \mathrm{d}t = C_\text{g}\left(u_\text{g} - u_\text{g}(t=0)\right). \tag{7.5}$$

Combining (7.5) and (7.3) allows the description of the differential equation with only one time-dependent capacitance voltage u_g

$$u_\mathrm{dr,on} = u_\mathrm{dr,on}(t=0) - \frac{C_\mathrm{g}}{C_\mathrm{dr,on}}\left(u_\mathrm{g} - u_\mathrm{g}(t=0)\right). \tag{7.6}$$

Using (7.6) to describe the left-hand side of (7.2) yields

$$u_\mathrm{dr,on}(t=0) - \frac{C_\mathrm{g}}{C_\mathrm{dr,on}}\left(u_\mathrm{g} - u_\mathrm{g}(t=0)\right) = u_\mathrm{g} + \dot{u}_\mathrm{g} C_\mathrm{g} R_\mathrm{g} + \ddot{u}_\mathrm{g} C_\mathrm{g} L_\mathrm{g}, \tag{7.7}$$

$$R_\mathrm{g} := R_\mathrm{g,on,ext} + R_\mathrm{g,int}. \tag{7.8}$$

As expected, the LCR circuit shown in Figure 7.8 can be described with a second order linear homogeneous differential equation.

> **Remark:** Usually, one would unite the two series capacitances $C_\mathrm{dr,on}$ and C_g, as they only represent one independent state. Here, this step is skipped in order to avoid translations of the starting and end conditions to less tangible values, e.g., the definition when the gate capacitance crosses the threshold voltage U_th becomes more complex if the capacitances were merged.

Assuming a critically damped or overdamped system $\zeta \geq 1$, the solution is given by

$$u_\mathrm{g} = A_1 \mathrm{e}^{\lambda_1 t} + A_2 \mathrm{e}^{\lambda_2 t} + A_3, \quad A_1, A_2, A_3, \lambda_1, \lambda_2 \in \mathbb{R}, \tag{7.9}$$

$$\lambda_{1,2} = -\frac{R_\mathrm{g}}{2L_\mathrm{g}} \pm \sqrt{\left(\frac{R_\mathrm{g}}{2L_\mathrm{g}}\right)^2 - \frac{C_\mathrm{g} + C_\mathrm{dr,on}}{L_\mathrm{g} C_\mathrm{g} C_\mathrm{dr,on}}}. \tag{7.10}$$

Initial values and boundary conditions are needed to determine the parameters A_1 to A_3. Before the turn-on process begins, the gate capacitance C_g is charged to the negative gate driver voltage $U_\mathrm{dr,off,0}$ and the gate driver capacitance is charged to the positive driver voltage $U_\mathrm{dr,on,0}$. At the beginning of the first phase, there is no current in the gate loop, while a current is present when transitioning to the second phase of the piecewise linear description. In order to transfer the solution to the second phase, a current $i_\mathrm{g}(t=0) > 0\,\mathrm{A}$ in the gate loop inductance is assumed, yielding the following conditions

$$u_\mathrm{dr,on}(t=0) \overset{!}{=} U_\mathrm{dr,on,0}, \tag{7.11}$$

$$u_\mathrm{g}(t=0) \overset{!}{=} U_\mathrm{dr,off,0}, \tag{7.12}$$

$$i_\mathrm{g}(t=0) \overset{!}{=} I_\mathrm{g,0} \quad \Leftrightarrow \quad \dot{u}_\mathrm{g} = \frac{I_\mathrm{g,0}}{C_\mathrm{g}}. \tag{7.13}$$

The gate capacitance is charged until the voltage of the gate driver's capacitance and the gate capacitance are balanced

$$\lim_{t\to\infty} u_\mathrm{g} \overset{!}{=} \frac{U_\mathrm{dr,on,0} C_\mathrm{dr,on} + C_\mathrm{g} U_\mathrm{dr,off,0}}{C_\mathrm{g} + C_\mathrm{dr,on}} \mathrel{\widehat{=}} A_3. \tag{7.14}$$

The three boundary conditions (7.12) to (7.14) are used to solve the parameters A_1 to A_3

in (7.9) with a computer algebra system (CAS)[1]

$$A_1 = \frac{C_{\mathrm{dr,on}} I_{\mathrm{g},0} + C_{\mathrm{g}} I_{\mathrm{g},0} + C_{\mathrm{dr,on}} C_{\mathrm{g}} U_{\mathrm{dr,on},0} \lambda_2 - C_{\mathrm{dr,on}} C_{\mathrm{g}} U_{\mathrm{dr,off},0} \lambda_2}{C_{\mathrm{g}} (\lambda_1 - \lambda_2) \left(C_{\mathrm{dr,on}} + C_{\mathrm{g}} \right)}, \tag{7.15}$$

$$A_2 = -\frac{C_{\mathrm{dr,on}} I_{\mathrm{g},0} + C_{\mathrm{g}} I_{\mathrm{g},0} + C_{\mathrm{dr,on}} C_{\mathrm{g}} U_{\mathrm{dr,on},0} \lambda_1 - C_{\mathrm{dr,on}} C_{\mathrm{g}} U_{\mathrm{dr,off},0} \lambda_1}{C_{\mathrm{g}} (\lambda_1 - \lambda_2) \left(C_{\mathrm{dr,on}} + C_{\mathrm{g}} \right)}, \tag{7.16}$$

$$A_3 = \frac{C_{\mathrm{dr,on}} U_{\mathrm{dr,on},0} + C_{\mathrm{g}} U_{\mathrm{g},0}}{C_{\mathrm{dr,on}} + C_{\mathrm{g}}}. \tag{7.17}$$

Figure 7.11 shows model predictions of the turn-on process for different gate loop inductances. The first phase uses $C_{\mathrm{g}}\left(u_{\mathrm{g}} < U_{\mathrm{fb}}\right) = C_{\mathrm{g},1}$ until the gate voltage u_{g} reaches the flat-band voltage U_{fb}, which is assumed constant. At the time t_{fb}, when the flat-band voltage is reached, the gate capacitance is changed to $C_{\mathrm{g}}\left(u_{\mathrm{g}} \geq U_{\mathrm{fb}}\right) = C_{\mathrm{g},2}$. The same underlying solution of the differential equation (7.9) can be used, but the parameters A_1 (7.15) to A_3 (7.17) must be reinitialized

$$U_{\mathrm{dr,on},0}^{(\text{phase two})} = u_{\mathrm{dr,on}}^{(\text{phase two})}(t = t_{\mathrm{fb}}) \overset{!}{=} u_{\mathrm{dr,on}}^{(\text{phase one})}(t = t_{\mathrm{fb}}), \tag{7.18}$$

$$U_{\mathrm{dr,off},0}^{(\text{phase two})} = u_{\mathrm{g}}^{(\text{phase two})}(t = t_{\mathrm{fb}}) \overset{!}{=} u_{\mathrm{g}}^{(\text{phase one})}(t = t_{\mathrm{fb}}), \tag{7.19}$$

$$I_{\mathrm{g},0}^{(\text{phase two})} = i_{\mathrm{g}}^{(\text{phase two})}(t = t_{\mathrm{fb}}) \overset{!}{=} i_{\mathrm{g}}^{(\text{phase one})}(t = t_{\mathrm{fb}}). \tag{7.20}$$

At the points where the gate voltage u_{g} crosses the threshold voltage U_{th} and the Miller plateau voltage U_{M}, it can be seen that the gate loop inductance can increase the switching times, as well as shorten them. This aspect is even more significant considering the current rise time, where start and end change simultaneously.

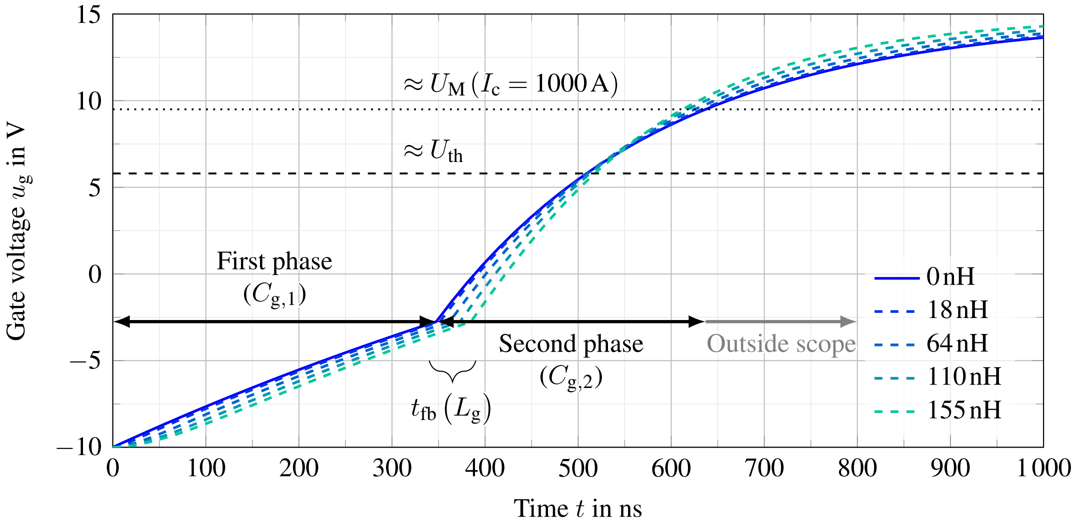


Figure 7.11: Exemplary turn-on processes for different gate loop inductances L_{g} [103]; used gate loop inductance is 75 nH; A_1 to A_3 are different in the first and second phase, as C_{g} changes

The dependencies of the switching times can be extracted from the time constants (7.10), the boundary conditions (7.11) to (7.14) and known semiconductor characteristics, which

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[1] The conditions (7.11) and (7.14) contain redundant information.

are shown in Figure 7.12. The dependencies are split into those tightly bound to the junction temperature on the right and those that are considered parasitic. The parasitic impacts depend on parameters that are either unknown during operation or whose acquisition would increase the complexity level of the system disproportionately.

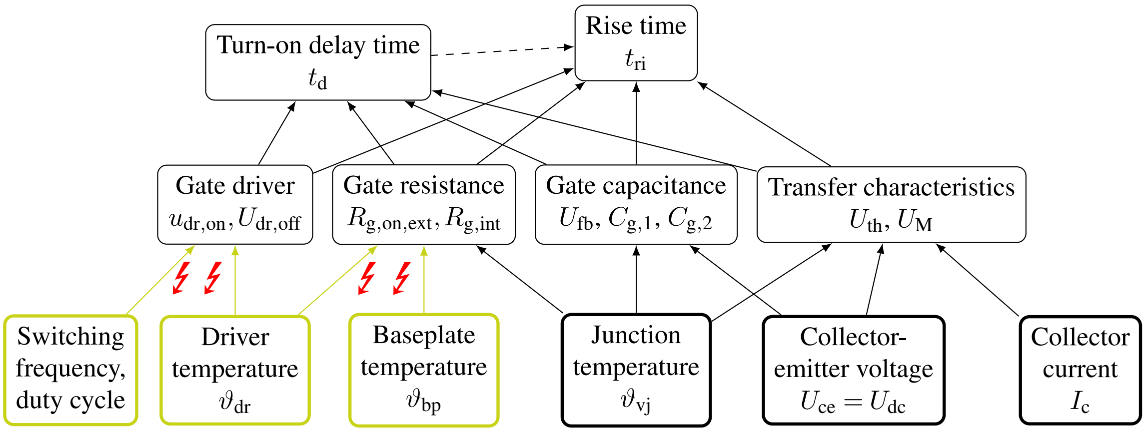


Figure 7.12: Direct and indirect dependencies of the switching times [103]; desired temperature dependencies of the semiconductor on the right; parasitic impacts on the left (green)

7.2.2 Sensitivity analysis

The first phase of the piecewise linear model uses the model (7.9) with $C_\mathrm{g,1}$ and zero current in the gate loop inductance. When the flat-band voltage is reached, the gate capacitance must be switched to $C_\mathrm{g,2}$ and the differential equation (7.9) must be reinitialized. At this point, a gate current i_g is flowing in the gate loop inductance.

The reinitialization requires the gate loop current i_g, the gate voltage u_g and driver voltage $u_\mathrm{dr,on}$ at the switching point. Therefore, the time when the two phases switch must be determined explicitly. Unfortunately, the second-order model equation (7.9) cannot be inverted for the time explicitly.

Instead, two edge cases will be evaluated. The first one only uses the large capacitance $C_\mathrm{g,1}$, while the second one only uses $C_\mathrm{g,2}$, see Figure 7.13. A third case is added to reflect that a gate current has already built up at the beginning of the second phase. In the following evaluations, the smallest and largest results of these three cases will be used. These two results will envelope the range of possible solutions. As will be shown at the end of this chapter, the determination of the range will be sufficient to draw the necessary conclusions.

The sensitivity $\frac{\partial t}{\partial x}$ of the switching time t towards a parameter x will be determined explicitly, based on the analytical solution shown in (7.9) and (7.15) to (7.17). Here, the same problem as before applies. The gate driver voltage (7.9) cannot be solved explicitly for the time. The *implicit function theorem* can be used to determine the sensitivity explicitly, without solving for the time. An analogy is that a small change in u_g due to the parameter x must

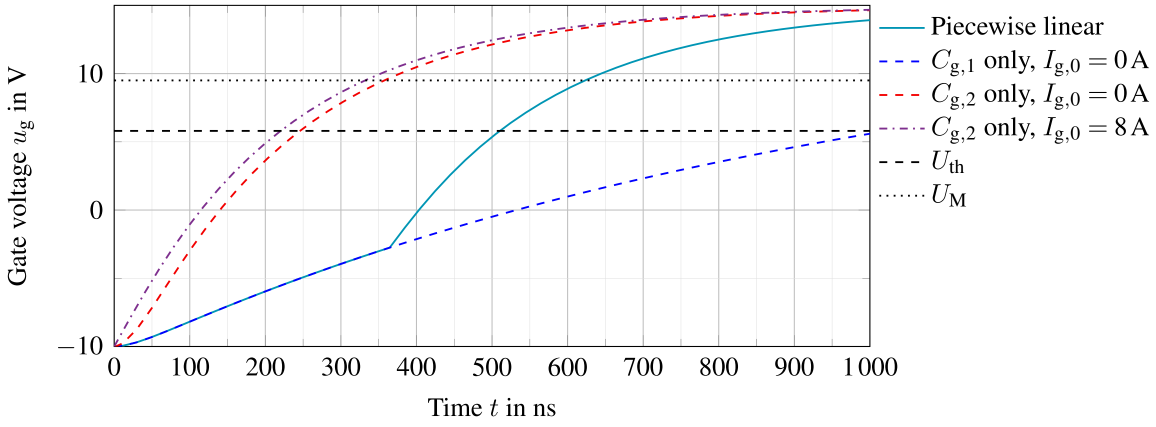


Figure 7.13: Edge cases used to envelope the range of the piecewise linear solution; third case added with L_g precharged to the largest gate current measured

be compensated by additional time to remain at the same voltage level

$$\frac{\partial u_g}{\partial x}\partial x + \frac{\partial u_g}{\partial t}\partial t \overset{!}{=} 0 \quad \Leftrightarrow \tag{7.21}$$

$$\frac{\partial t}{\partial x} = -\frac{\partial u_g}{\partial x}\left(\frac{\partial u_g}{\partial t}\right)^{-1} . \tag{7.22}$$

The results for (7.22) can be expressed explicitly, but are omitted in this work due to their complexity. Figure 7.14 depicts the shape of several sensitivities based on the presented LCR model and a simplified RC model with $L_g = 0$ nH. The results show the expected behavior. The time needed to reach a certain voltage increases approximately proportional with the gate resistance. The negative gate driver voltage $U_{dr,off}$ can be approximated by an offset, caused by the additional voltage that must be overcome. Changes in gate driver capacitance have little effect compared to the other effects. The investigation of the sensitivity towards the driver capacitance is added to evaluate whether TSEP calibration data may be transferred from one gate driver to another, e.g., due to a driver replacement during maintenance or when investigating the transferability of calibration data to other modules. In these cases, the high tolerances of capacitors must be accounted for, yet the impact is acceptable as long as the driver voltages are comparable between the gate drivers.

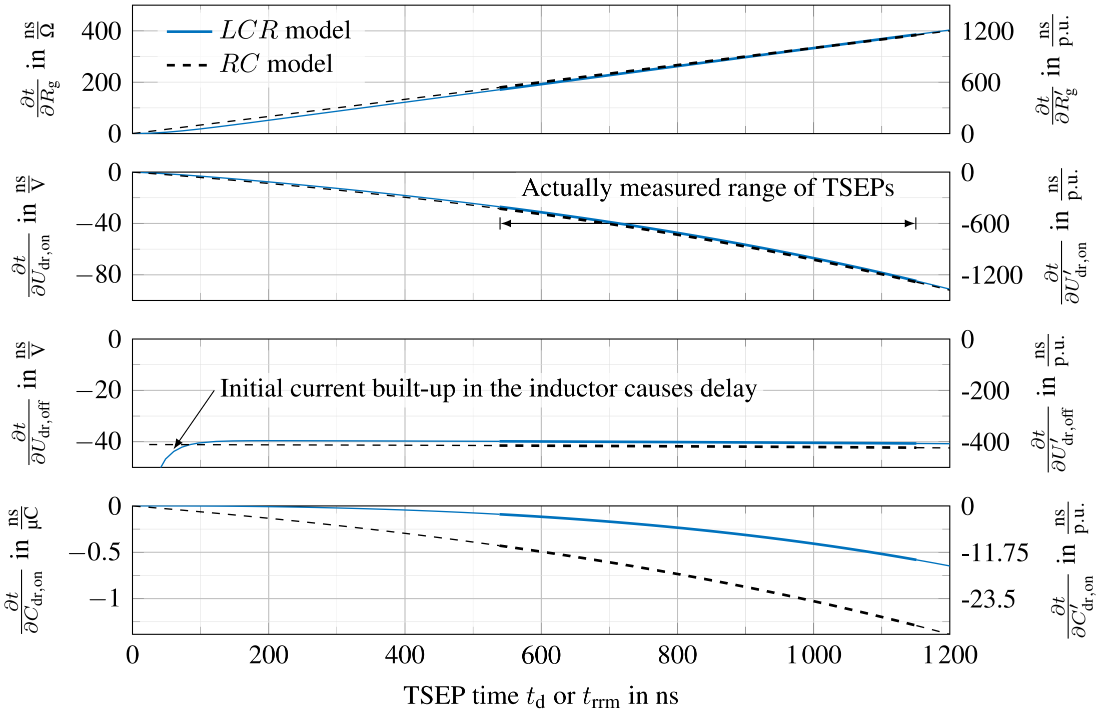


Figure 7.14: Sensitivities towards parasitic impacts of the gate loop; actual range of the TSEPs highlighted; normalized scale on the right-hand side; case with $C_{g,1}$ and $i_g(t=0) = 0\,A$ used, compare Table 7.2

7.3 Resulting temperature deviation

In the previous paragraphs, parasitic impacts have been identified. Their actual size has been measured on commercial hardware. The sensitivity of the two TSEPs, turn-on delay time t_d and the current rise time t_{ri}, towards each parasitic has been determined analytically.

The next step is the evaluation of the resulting temperature estimation deviation caused by each parasitic. These investigations will be repeated for several sets of input variables, i.e., using each TSEP individually or combined. First, for each set of input variables, an ANN will be trained on the calibration data, see Figure 7.15. The preprocessing will be described in a subsequent paragraph. The temperature predicted by this ANN will serve as reference, i.e., the "true" values. Figure 7.16 shows the results from this ANN trained on the current rise time t_{ri} alone as example.

Figure 7.15: Flowchart of the ANN training

Afterwards, the calibration data will be perturbed for each investigated parasitic impact. The size of the perturbation Δt is determined from the sensitivity towards the parasitic impact x and its expected size Δx using a first-order Taylor approximation

$$\Delta t = \frac{\mathrm{d}t_{\mathrm{TSEP}}}{\mathrm{d}x} \Delta x. \tag{7.23}$$

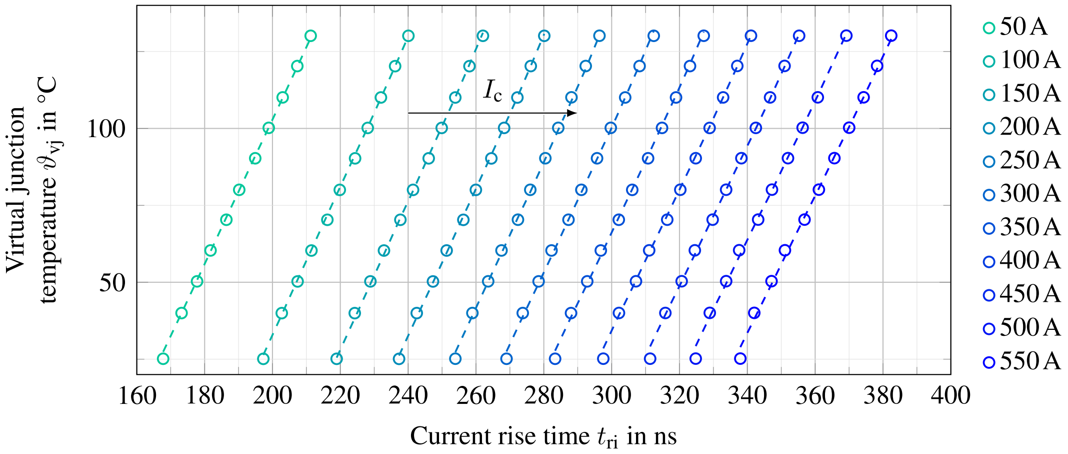


Figure 7.16: Example ANN fit of the current rise time alone [103]

The manipulated calibration data is then reevaluated in the previously determined ANN leading to a temperature deviation, see Figure 7.17.

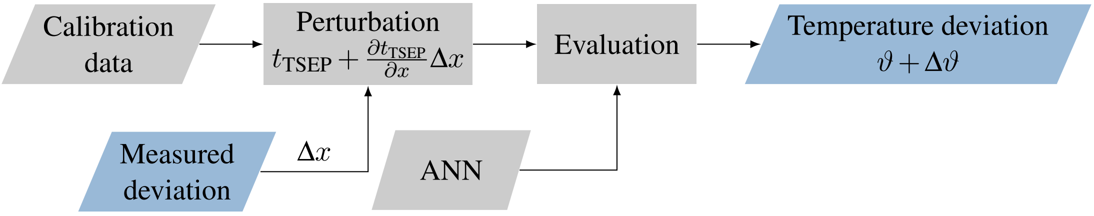


Figure 7.17: Flowchart of determining the temperature error caused by each parasitic

All investigated input combinations, parasitic impacts and resulting additional temperature deviations are listed in Table 7.3 and depicted in Figure 7.18 on a log scale. The values for the current and voltage sensors are extracted from the datasheets of the used sensors LEM LT 2005-S and TESTEC TT-SI 9002. The datasheets only state an "overall accuracy" and an offset. The probe offsets are depicted separately, as the offsets can be compensated to a large part before the inverter starts up. The used current probe has a nominal current of $I_{\mathrm{N}} = 2\,\mathrm{kA}$, which is twice the nominal current of the module. For a well-designed industrial setup it can be expected that the shown deviation caused by the current sensor is halved.

The TSEPs evaluated individually are shown using dashed lines. Especially the turn-on delay time t_{d} alone is susceptible to parasitic impacts leading to large deviations. The current rise time t_{ri} alone shows better robustness than the turn-on delay time. The observed variations in the gate driver voltages cause unfeasibly large temperature deviations if not stabilized. Therefore, a TSEP-based temperature estimation is not expected to be applicable, without a gate driver voltage stabilization.

The trivial approach of a combined TSEP evaluation using the two inputs $(t_{\mathrm{d}}, t_{\mathrm{ri}})$ is shown as a solid red line. Simply introducing additional TSEPs does not improve the system robustness. The additional temperature deviation is comparable to using the current rise time t_{ri} alone.

Table 7.3: Used input combinations and parasitic impact sources; resulting average temperature deviations, minimum deviation and maximum deviation; $^{\mathrm{a})}$ Combined TSEP evaluation; $^{\mathrm{b})}$ Combined and preprocessed TSEP evaluation;

Parasitic impact	TSEP combination				
	(t_{d})	(t_{ri})	$(t_{\mathrm{d}}, t_{\mathrm{ri}})^{\mathrm{a})}$	$\left(t_{\mathrm{d}}, \frac{t_{\mathrm{ri}}}{t_{\mathrm{d}}}\right)^{\mathrm{b})}$	
ΔI_{c}	(no dependency)	4.7 K	5.0 K	1.1 K	(current sensor accuracy)
$\Delta I_{\mathrm{c},0}$	(no dependency)	3.1 K	3.3 K	0.7 K	(current sensor offset)
ΔU_{dc}	23.9 K	6.3 K	5.1 K	2.3 K	(dc-link voltage sensor accuracy)
$\Delta U_{\mathrm{dc},0}$	0.9 K	0.2 K	0.2 K	0.1 K	(dc-link voltage sensor offset)
$\Delta U_{\mathrm{dr,on}}$	44.9 K (23.2 K, 66.7 K)	55.5 K (5.9 K, 105.1 K)	60.6 K (4.4 K, 116.7 K)	5.7 K (2.4 K, 9.0 K)	
$\Delta U_{\mathrm{dr,off}}$	20.8 K (33.4 K, 8.2 K)	0.2 K (0.1 K, 0.4 K)	2.7 K (4.5 K, 0.9 K)	2.2 K (3.5 K, 0.8 K)	
$\Delta C_{\mathrm{dr,on}}$	1.7 K (0.9 K, 2.5 K)	2.4 K (0.5 K, 4.3 K)	2.5 K (0.5 K, 4.5 K)	0.2 K (0.1 K, 0.3 K)	
$\Delta R_{\mathrm{g,on,ext}}$	9.8 K (8.8 K, 10.9 K)	1.7 K (1.5 K, 1.8 K)	1.2 K (1.1 K, 1.3 K)	1.0 K (0.9 K, 1.1 K)	
$\Delta R_{\mathrm{g,d},i}$	15.8 K (14.1 K, 17.5 K)	2.7 K (2.4 K, 3.0 K)	1.9 K (1.7 K, 2.1 K)	1.6 K (1.4 K, 1.8 K)	

7.3.1 Input preprocessing

So far, the ANN training process did not include any information about the parasitic impacts. One approach to incorporate these impacts would be to generate additional artificial calibration points that have been manipulated according to the expected deviations, see Figure 7.17. This approach would rely on the ANN's ability to include the expected deviations in its mapping. Another simple approach can be derived from the TSEPs sensitivities, see Figure 7.14. The deviation in the measured switching times due to a change in the positive gate driver voltage is almost proportional to the time elapsed. As a consequence, the ratio of the times $t_{\mathrm{rrm}} = t_{\mathrm{d}} + t_{\mathrm{ri}}$ and t_{d} should be unaffected by this parasitic impact

$$t^{(\mathrm{meas})} := t + \Delta t, \tag{7.24}$$

$$\Delta t \approx a \cdot t, \quad a \in \mathbb{R}, \tag{7.25}$$

$$\frac{t_{\mathrm{rrm}}^{(\mathrm{meas})}}{t_{\mathrm{d}}^{(\mathrm{meas})}} \approx \frac{t_{\mathrm{rrm}}\,(1+a)}{t_{\mathrm{d}}\,(1+a)} = 1 + \frac{t_{\mathrm{ri}}}{t_{\mathrm{d}}}. \tag{7.26}$$

The resulting sensitivity towards parasitic impacts is shown in Figure 7.18 in blue. This simple preprocessing (7.26) of the inputs reduces the sensitivity towards almost all investigated parasitic impacts significantly. The only exception is the sensitivity towards the negative gate driver voltage $U_{\mathrm{dr,off}}$. Here, the least affected TSEP is the current rise time t_{ri}, when used alone. This is due to the fact that a change in the negative gate driver voltage manifests approximately as a constant time deviation within the relevant time frame of TSEP measurements, see Figure 7.14. As a result, the current rise time is the best option to compensate

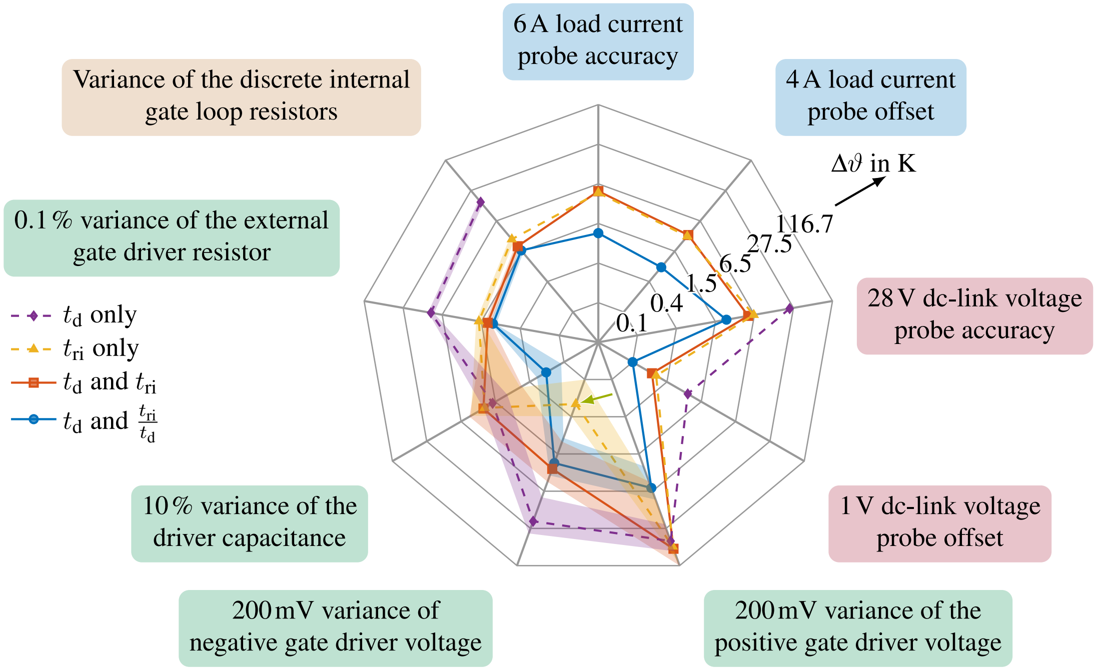


Figure 7.18: Additional temperature deviation caused by parasitic impacts [103]; log scale; current sensor (blue), voltage sensor (red), gate driver (green), module (brown); transparent areas mark range of the different edge cases, see Figure 7.13

variations in the negative gate driver voltage.

$$\Delta t \approx t + b, \quad a \in \mathbb{R}, \tag{7.27}$$

$$t_{\mathrm{ri}}^{(\mathrm{meas})} := t_{\mathrm{rrm}}^{(\mathrm{meas})} - t_{\mathrm{d}}^{(\mathrm{meas})} \tag{7.28}$$

$$\approx t_{\mathrm{rrm}} + b - t_{\mathrm{d}} - b, \tag{7.29}$$

$$t_{\mathrm{ri}}^{(\mathrm{meas})} \approx t_{\mathrm{rrm}} - t_{\mathrm{d}}. \tag{7.30}$$

Summary In this chapter, possible parasitic impacts on the measured switching times have been identified. Their actual size has been measured on commercially available hardware. An analytical model has been determined to assess the impact of each considered parasitic on the final TSEP-based temperature estimation. It could be shown that the positive gate driver voltage level has the greatest impact on the switching time measurements and the corresponding temperature estimation. The gate driver voltages show significant variations depending on the applied duty cycle, as well as between nominal continuous PWM operation and during double-pulse operation. Consequently, the gate driver voltages must be stabilized in order to apply TSEP-based temperature estimations and allow the transfer of TSEP calibration data from double-pulse experiments to continuous PWM operation.

Furthermore, a simple preprocessing was presented that uses the ratio of two measured switching times instead of their absolute values. With this preprocessing, the sensitivity of the TSEP-based temperature estimation towards most parasitic impacts could be reduced noticeably.

Part III

TSEP models for Si and SiC MOSFETs

8 On-state voltage

Estimating the temperature from a TSEP requires an accurate understanding of the temperature dependency of the TSEP. Typically, the changes in the characteristics of a power module with temperature are small by design. TSEPs with a cross-dependency on the current require models that are accurate with respect to the temperature and with respect to the current. Otherwise, an inadequately modeled current dependency can lead to a misinterpretation of a current-induced TSEP change as a temperature change.

In this chapter, a variety of models and factors relevant for the approximation of the on-state voltage will be described. Models and factors concerning the switching times during turn-on will be analyzed in Chapter 9. In a first step, the TSEPs are modeled without consideration of their temperature dependencies. These models depend on semiconductor parameters like the mobility, transconductance and the threshold voltage. In a second step, the temperature dependencies of these semiconductor parameters are discussed and combined with the previously described models.

The models are sourced from two different approaches. First, conventional models from literature on power semiconductors are summarized. These models aim to predict the semiconductor behavior from known geometry and semiconductor properties. Second, SPICE models are used. In the field of SPICE modeling, typically neither the geometry nor the semiconductor properties are known precisely. Instead, models are parameterized with assumptions and fitted to measurement data. SPICE models are expected to be sophisticated enough to model all relevant behavior of the TSEP, while not including too many details that have an insignificant impact. Nevertheless, to understand and extract the TSEP-relevant parts from SPICE models, a prior understanding of the conventional models is required.

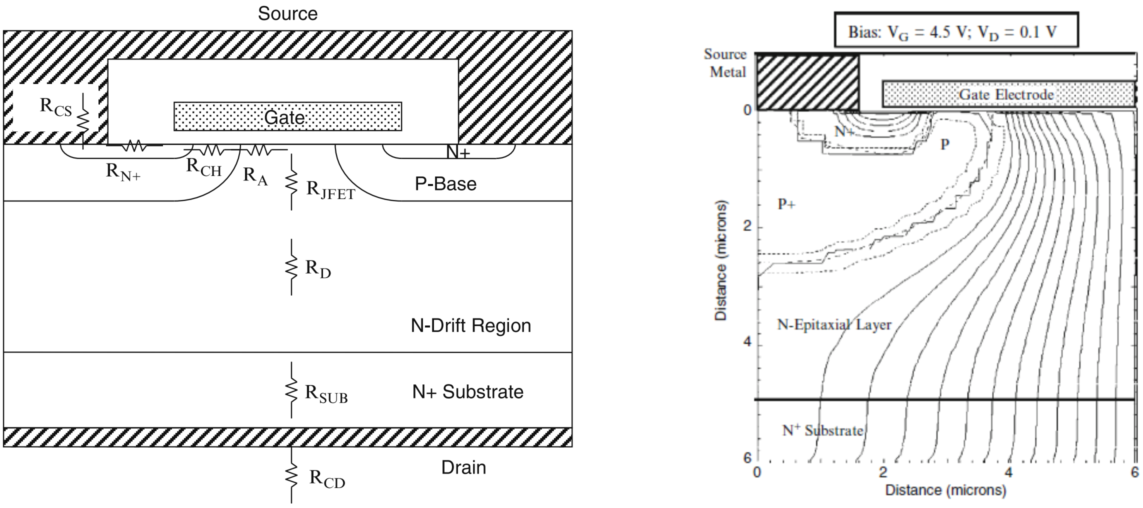
After a variety of modeling options has been introduced, each modeling option will be fitted to the SiC MOSFET devices under test. On-state voltage measurements and switching time measurements from 18 different units of the same switch are available. The inclusion of multiple examples in the fit comparison allows the assessment of the variation in the model performance across several switches.

The SiC MOSFET under test will be presented in Chapter 10. The 18 switches are sourced from seven modules used in the accelerated aging test and two generic modules. The acceleration tests will be presented in Chapter 14.

This Part is kept generic. The described effects and models are applicable to generic MOSFETs. They are not limited to either Si or SiC, although SiC-specific material properties and consequent effects are introduced in Section 8.5.

The goal of this comparison is the identification of the model details needed to reflect the current-dependent and the temperature-dependent behavior of the TSEPs and the assessment of which model details are not required for a TSEP-based temperature estimation.

MOSFET structure The on-state voltage drop of a MOSFET from drain to source can be modeled as a nonlinear resistance using the *Sun and Plummer Method* [108, 109]. The total resistance of the path $R_{\mathrm{ds,on}}$ can be described as a series resistance of the current path through the device, aggregating regions with similar geometries and material parameters. A typical cross-section of an n-channel D-MOSFET is shown in Figure 8.1.



(a) Structure (b) Current flow

Figure 8.1: Structure of a D-MOSFET with its resistive components [109] [1]

An electron current entering the MOSFET at the source contact will cause voltage drops at the metal contact (R_{CS}) and when passing through the highly doped N$^+$-region ($R_{\text{N+}}$). After this, the current will pass through the MOSFET channel (R_{CH}). At the junction between the channel and the n-drift region, the current exits the narrow channel, expanding in the accumulation zone (R_{A}), while simultaneously changing its direction. Between the top surface of the n-drift region at the gate insulator and the bottom edge of the p-base, the current is enclosed by p-doped regions on both sides. This geometry forms a parasitic JFET region, causing an additional resistance (R_{JFET}) [109, 110]. Below the p-base, the current spreads horizontally and passes through the n-drift region (R_{D}). Near the drain contact, the current passes through the highly doped N$^+$ substrate (R_{SUB}) and the metal contact (R_{CD}). The overall resistance can be described by

$$R_{\text{ds,on}} = \underbrace{R_{\text{CS}} + R_{\text{N+}}}_{\text{neglectable}} + R_{\text{CH}} + R_{\text{A}} + R_{\text{JFET}} + R_{\text{D}} + \underbrace{R_{\text{SUB}} + R_{\text{CD}}}_{\text{neglectable}} \quad [109]. \tag{8.1}$$

In the forward direction, the MOSFET is a unipolar device, meaning that only one type of carrier contributes to the current transport. Generally, the specific resistance ρ inside the structure of an n-channel MOSFET is given by

$$\rho = \frac{1}{\mu_{\text{n}} \cdot n \cdot e_0}, \tag{8.2}$$

where μ_{n} is the electron mobility, e_0 the elementary charge and n the density of electron carriers in the conduction band.

The resistances of the metal contacts R_{CS} and R_{CD} can be neglected for high-voltage devices [109, 111]. The resistance of the N$^+$-region, $R_{\text{N+}}$, can also be neglected due to the

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higher doping and the resulting low specific resistance [109]. Even though R_{SUB} also corresponds to a region with a high doping concentration, the resulting resistance depends on how thin the N^{+}-substrate can be manufactured. According to [109, 112], modern manufacturing processes for low-voltage Si MOSFETs generally allow R_{SUB} to be neglected in the device modeling. The resistances marked as neglectable in (8.1) are generally not considered in SiC SPICE models[2] [113, 114].

The remaining resistive components are

1. the channel resistance R_{CH},
2. the accumulation area contribution R_{A},
3. the JFET contribution R_{JFET}, and
4. the drift region contribution R_{D}.

During the course of this chapter, each of these contributions will be discussed separately.

Fundamental dependencies In order to achieve high breakdown voltages U_{br}, the thickness of the drift region W_{D} must be increased, while its doping concentration N_{D}^{+} must be reduced. The *ideal specific on-resistance of the drift region* [109] for unipolar drift regions can be estimated to be

$$W_{\text{D}} \propto \frac{U_{\text{br}}}{E_{\text{crit}}}, \quad N_{\text{D}}^{+} \propto \frac{\varepsilon E_{\text{crit}}^{2}}{U_{\text{br}}}, \tag{8.3}$$

$$R_{\text{D}} \propto \frac{W_{\text{D}}}{N_{\text{D}}^{+}} \propto \frac{U_{\text{br}}^{2}}{E_{\text{crit}}^{3}}. \tag{8.4}$$

This assumes a triangular electric field distribution without any carrier generation within the depletion region, a critical electrical field E_{crit} and an (absolute) permittivity ε of the Si or SiC material. If one considers the possible avalanche breakdown caused by the leakage current, the dependency increases to $R_{\text{ds,on}} \propto U_{\text{br}}^{2.5}$ [70, 108]. A manufacturer of power devices estimates the overall on-resistance to follow $R_{\text{ds,on}} \propto U_{\text{br}}^{2.4\dots2.6}$ [115]. The resistance of the drift region R_{D} is dominant for high-voltage Si MOSFETs [70, 111, 115]. The tenfold-higher critical electrical field of SiC compared to Si [69] allows a significant reduction in the drift region's thickness W_{D}, as well as increased doping concentrations N_{D}^{+}, thus reducing the relative contribution of R_{D}, see (8.4). As a consequence, the relative contribution of the other resistances, e.g., the channel resistance R_{CH}, becomes more relevant in SiC devices.

Trench MOSFET or U-MOSFET structure An important tool for reducing the overall resistance of a D-MOSFET as depicted in Figure 8.1a is increasing the cell density. Increasing the cell density increases the total available gate width and therefore reduces the channel resistance. Unfortunately, this also reduces the width of the vertical JFET region, enveloped by the p-base to the left and right. For a D-MOSFET with a given minimum gate contact width, there exists an optimal cell density which minimizes the summed resistance of these two effects [112, 116].

Figure 8.2a shows the structure of a trench MOSFET or U-MOSFET. Instead of a planar

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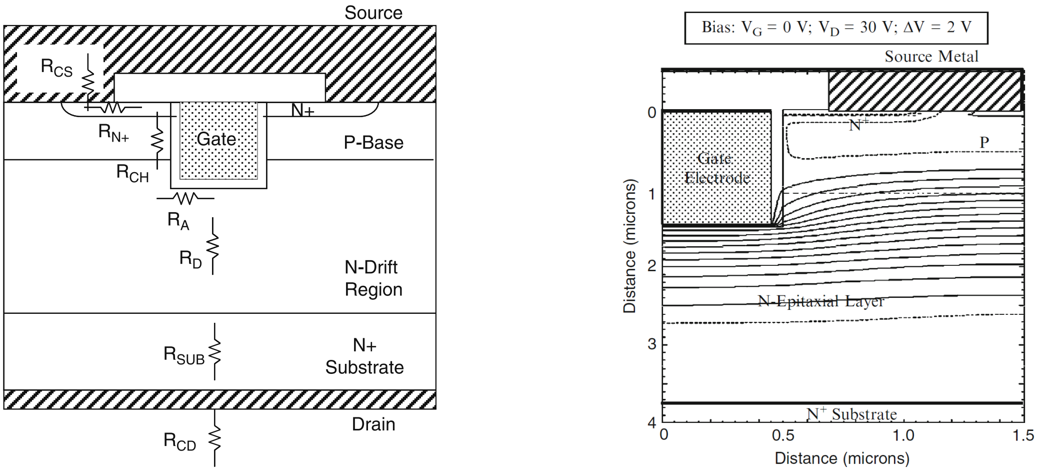
[2] Of course, this could also be caused by the fact that their contribution to the overall resistance cannot be separated from other effects considered in the fitting function, i.e., their resistance follows the same or similar physical behavior as the resistance of the drift region.



(a) Structure (b) Potential contour lines

Figure 8.2: Structure, resistive components and potential of a trench MOSFET [109][3]

gate electrode, the gate is implemented as a vertical trench. The two biggest advantages of the trench structure are the increased channel width and the absence of a JFET region [68].

A challenge of the trench MOSFET design is the high field strength occurring at the corner of the trench [117], which strains the gate insulator, see Figure 8.2b. According to the manufacturer, the p-base region extends far below the trench structure in this device, in order to relieve the stress on the thin gate insulator [117, 118], as shown in Figure 8.3. The module under test is an SiC trench MOSFET (or U-MOSFET), therefore a JFET region should not be expected. Nevertheless, the extended p-base region re-introduces a relevant JFET region in this device [119]. The relative contribution of the JFET region to the overall on-state voltage depends on the precise geometry, doping and cell density [68, 116, 120].

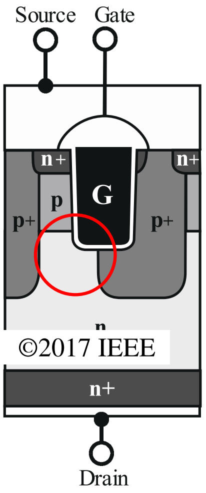


Figure 8.3: Sketch of the trench SiC MOSFET cell of the devices under test [119]; gate contact has rounded corners and is shielded by a deep, highly p-doped region; JFET region marked in red

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8.1 Channel resistance

The resistance of the metal-oxide semiconductor (MOS) channel is a highly complex topic. Therefore, the fundamentals of the channel resistance are introduced in this section and extended to cover further nonlinear details in Section 8.1.3. As not all aspects can be discussed in their full extend, [68, 69, 121] are recommended for further reading.

Remarks on notation Semiconductors are three-dimensional objects. Carrier density, current density, voltage and other quantities can vary in all three dimensions. Depending on the type of investigation, different relations of these quantities are useful. For example, analyzing the required chip area for a given load current may best be done with area-related quantities, while the analysis of the channel resistance can benefit from length-related quantities. Thus, new related quantities can be introduced. In this work, total quantities, concentration of quantities and quantities related to a length are used.

1. Total quantities use capital letters. For instance, charges and capacitances are denoted as a total charge Q or a total capacitance C.

2. Quantities related to a length are marked with a dash. In the analysis of the channel, the total charge Q will be denoted related to the channel length L_{ch}

   $$Q' := \frac{Q}{\mathrm{d}y} \mathrel{\widehat{=}} \frac{Q}{L_{\mathrm{ch}}}, \tag{8.5}$$

   where the channel/drain current flow is oriented in the y coordinate axis. The axis definitions are shown in Figure 8.4.

3. Carrier concentrations n or p are denoted in lower case.

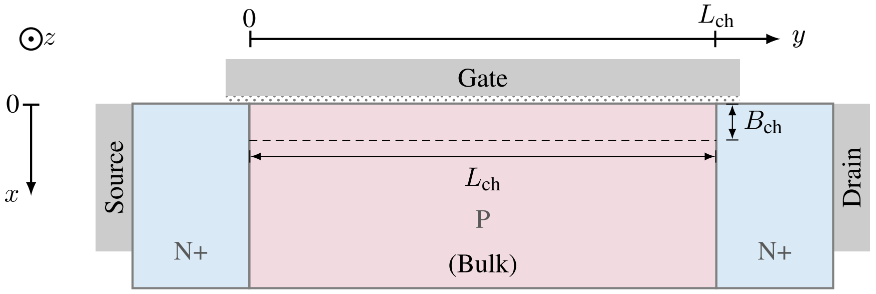

Figure 8.4: Used coordinate system and dimensions of the MOS channel; the channel has a depth of D_{ch} in z direction

8.1.1 Simple MOS channel model

The voltage drop across the MOS channel can be described by two key concepts. First, if the gate voltage U_{gs} is increased above the threshold voltage U_{th}, the concentration of minority carriers increases at the surface of the p-base, forming a conductive channel. According to [70, 109], the capacitance between the gate electrode and the channel can be assumed to be constant, leading to a free carrier charge Q_{ch} and resistance of the channel R_{CH}

$$Q_{\text{ch}} = ne_0 L_{\text{ch}} D_{\text{ch}} B_{\text{ch}} \quad \Leftrightarrow \quad \rho = \frac{L_{\text{ch}} B_{\text{ch}} D_{\text{ch}}}{Q_{\text{ch}} \mu_{\text{n}}} \tag{8.6}$$

$$Q_{\text{ch}} = C_{\text{ox}} \left(U_{\text{gs}} - U_{\text{th}} \right) \tag{8.7}$$

$$R_{\text{CH}} = \frac{L_{\text{ch}} \rho}{D_{\text{ch}} B_{\text{ch}}} \tag{8.8}$$

$$= \frac{L_{\text{ch}}^2}{\mu_{\text{n}} Q_{\text{ch}}} = \frac{L_{\text{ch}}^2}{\mu_{\text{n}} C_{\text{ox}} \left(U_{\text{gs}} - U_{\text{th}} \right)}. \tag{8.9}$$

The model depends on the channel length L_{ch} in the direction of the current flow and the total channel width B_{ch} perpendicular to the current flow direction, compare Figure 8.4. The channel has a depth of D_{ch} in z direction.

Let y be the position in the direction of current flow along the channel. If a current I_{d} flows between the drain and source, it will cause a voltage drop $U(y)$ along the channel, reducing the effective voltage between the gate electrode and the channel. The used electrical quantities are illustrated in Figure 8.5.

Assuming the gate oxide capacitance C_{ox} is voltage independent, the local resistance and voltage drop across the channel can be described as presented in [70]

$$\mathrm{d}R_{\text{CH}} = \frac{\rho(y)\,\mathrm{d}y}{B_{\text{ch}} D_{\text{ch}}} = \frac{\mathrm{d}y}{Q'_{\text{ch}}(y)\,\mu_{\text{n}}}, \quad Q_{\text{ch}} = \int_0^{L_{\text{ch}}} Q'_{\text{ch}}(y)\,\mathrm{d}y, \tag{8.10}$$

$$= \frac{L_{\text{ch}} \mathrm{d}y}{\mu_{\text{n}} C_{\text{ox}} \left(U_{\text{gs}} - U_{\text{th}} - U(y) \right)}, \quad C_{\text{ox}} = C'_{\text{ox}} L_{\text{ch}}, \tag{8.11}$$

$$= \frac{\mathrm{d}y}{\mu_{\text{n}} C'_{\text{ox}} \left(U_{\text{gs}} - U_{\text{th}} - U(y) \right)}, \quad \mathrm{d}U = I_{\text{d}} \mathrm{d}R_{\text{CH}}, \tag{8.12}$$

$$I_{\text{d}} = \mu_{\text{n}} C'_{\text{ox}} \left(U_{\text{gs}} - U_{\text{th}} - U(y) \right) \frac{\mathrm{d}U}{\mathrm{d}y}, \tag{8.13}$$

$$\int_0^{L_{\text{ch}}} I_{\text{d}} \mathrm{d}y = \int_0^{L_{\text{ch}}} \mu_{\text{n}} C'_{\text{ox}} \left(U_{\text{gs}} - U_{\text{th}} - U(y) \right) \frac{\mathrm{d}U}{\mathrm{d}y} \mathrm{d}y. \tag{8.14}$$

Equation (8.13) is a first-order nonlinear ordinary differential equation. It can be solved by *separation of variables*, or by *substitution* [122]. Here, y can be substituted by the inverse function of the voltage $U(y)$

$$y := U^{-1}\left(\tilde{U}\right), \quad \mathrm{d}y = \frac{\mathrm{d}U^{-1}\left(\tilde{U}\right)}{\mathrm{d}\tilde{U}} \mathrm{d}\tilde{U} = \left(\frac{\mathrm{d}U}{\mathrm{d}y} \right)^{-1} \mathrm{d}\tilde{U}, \tag{8.15}$$

$$\int_0^{L_{\text{ch}}} I_{\text{d}} \mathrm{d}y = \int_{\tilde{U}(y=0)}^{\tilde{U}(y=L_{\text{ch}})} \mu_{\text{n}} C'_{\text{ox}} \left(U_{\text{gs}} - U_{\text{th}} - \tilde{U} \right) \frac{\mathrm{d}U}{\mathrm{d}y} \left(\frac{\mathrm{d}U}{\mathrm{d}y} \right)^{-1} \mathrm{d}\tilde{U}, \tag{8.16}$$

$$\tilde{U}\left(y=0\right) := 0, \quad \tilde{U}\left(y=L_{\text{ch}}\right) =: U_{\text{ch}}, \tag{8.17}$$

$$I_{\text{d}} = \frac{\mu_{\text{n}} C'_{\text{ox}}}{L_{\text{ch}}} \left(\left(U_{\text{gs}} - U_{\text{th}} \right) U_{\text{ch}} - \frac{U_{\text{ch}}^2}{2} \right). \tag{8.18}$$

Equation (8.18) describes the current-voltage relationship of the channel, with the total voltage drop U_{ch} along the channel. Starting with $U(y) = 0$, the inverse of the voltage $U^{-1}\left(\tilde{U}\right)$

in (8.15) can only be defined if $U(y)$ is bijective. According to (8.12), $U(y)$ increases strictly for $\mathrm{d}R_{\mathrm{CH}} > 0\,\Omega$ and $I_{\mathrm{d}} > 0\,\mathrm{A}$. Therefore, the current-voltage relationship (8.18) is only valid up to

$$U_{\mathrm{ch}} < U_{\mathrm{gs}} - U_{\mathrm{th}} =: U_{\mathrm{ch,po}}, \tag{8.19}$$

which is also referred to as the pinch-off voltage $U_{\mathrm{ch,po}}$ [109].

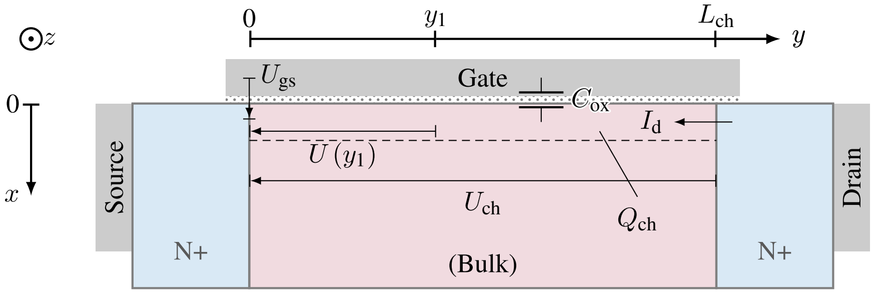

Figure 8.5: Definition of the electrical quantities; the source contact, gate contact, drain contact, and each of the interfaces between the n and p region are assumed equipotentials [4]

So far, the model cannot be used to calculate the current-voltage relationship for U_{ch} equal to or exceeding the pinch-off voltage $U_{\mathrm{ch,po}}$. According to (8.12), the channel resistance would approach infinity when U_{ch} approaches $U_{\mathrm{ch,po}}$. For simple models, it is assumed that the current saturates after reaching the pinch-off voltage and does not increase depending on the drain or channel voltage [69, 70, 109, 110]

$$I_{\mathrm{d}} = \begin{cases} \dfrac{\mu_{\mathrm{n}} C'_{\mathrm{ox}}}{L_{\mathrm{ch}}} \left(\left(U_{\mathrm{gs}} - U_{\mathrm{th}}\right) U_{\mathrm{ch}} - \dfrac{U_{\mathrm{ch}}^2}{2} \right), & \text{for } U_{\mathrm{ch}} < U_{\mathrm{ch,po}} \\ I_{\mathrm{d,sat}}, & \text{for } U_{\mathrm{ch}} \geq U_{\mathrm{ch,po}} \end{cases} \tag{8.20}$$

$$I_{\mathrm{d,sat}} = I_{\mathrm{d}}\left(U_{\mathrm{ch,po}}\right) = \frac{\mu_{\mathrm{n}} C'_{\mathrm{ox}}}{2L_{\mathrm{ch}}} \left(U_{\mathrm{gs}} - U_{\mathrm{th}}\right)^2, \tag{8.21}$$

$$I_{\mathrm{d,sat}} = \frac{K}{2} \left(U_{\mathrm{gs}} - U_{\mathrm{th}}\right)^2, \quad K := \frac{\mu_{\mathrm{n}} C'_{\mathrm{ox}}}{L_{\mathrm{ch}}}. \tag{8.22}$$

Equation (8.22) defines the transconductance K, which is often used when the internal geometry and semiconductor paramters are not know, i.e., when working with datasheet values.

If the drain or channel voltage is increased beyond the pinch-off voltage, the location where the carrier distribution (8.12) reaches zero occurs before the end of the channel. This, the effective channel length is shortened by a distance ΔL, reducing the associated voltage drop. A depletion layer forms in the shorting distance ΔL in the p-base and the n-drift region, compensating the remaining voltage. This usually leads to a small increase of I_{d} with the drain or channel voltage. An elaborated model with a gradual change in the charge distribution beyond the pinch-off voltage has already been presented by Shockley [110]. Further details of the modeling beyond the pinch-off voltage can be found in [68–70, 109].

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[4] Technically, using a one-dimensional approach is only valid if the equipotential lines are perpendicular to the current direction, which is not correct at the beginning and end of the channel. The resulting deviation can be accepted considering the small channel width B_{ch}. [110]

In the context of this work, the power module investigated will be operated well below the pinch-off voltage. Therefore, further modeling above this point is omitted.

Equation (8.18) leads to the first (simple) fit model I_d^* for I_d

$$I_\text{d}^* = a_0 \left(a_1 U_\text{ch} - \frac{U_\text{ch}^2}{2} \right), \quad a_0, a_1 \in \mathbb{R}. \tag{8.23}$$

During the course of this work, all fit models for a quantity x are denoted by x^*.

8.1.2 MOS structure band diagrams

The simple MOS channel model from Section 8.1.1 assumes that all charge in the channel contributes to its conductivity (8.7). This assumption may oversimplify the actual charge behavior and may have a notable impact on the on-state voltage model function (8.23). A more detailed analysis of the charge in the MOS channel will be presented in this section.

Section 8.1.2 to Section 8.1.4.2 will show that the charge of the gate channel can be split into two parts: free carriers that contribute to the conductivity and stationary carriers that form the space-charge region to the bulk. The latter type of carriers does not contribute to the conductivity. Since less charge contributes to the conductivity than expected from the simple model, the channel conductivity is smaller and decreases faster in the presence of a drain current. The underlying principles will be discussed in the following sections. Finally, the impact on the model function will be quantified. The sections are based on [68, 69, 121, 123].

Energy levels and band diagrams The energy-band diagram of a semiconductor is typically described using a subset of the following parameters

- the Fermi level E_F,
- the (lower) energy level of the conduction band E_c,
- the (upper) energy level of the valence band E_v, or
- the bandgap E_G.

Alternatively, the work function E_work, the electron affinity E_aff, the vacuum energy E_vac, and the bandgap of the material E_G can be used to define the energy diagram. The vacuum energy is the energy of a free electron at rest, infinitely far away from the material surface. The work function is the energy difference between the vacuum energy E_vac and the Fermi level E_F in the material

$$E_\text{work} = E_\text{vac} - E_\text{F}, \quad E_\text{work} \geq 0. \tag{8.24}$$

The electron affinity E_aff is the difference between the vacuum energy E_vac and (lower) energy level of the conduction band E_c in the material

$$E_\text{aff} = E_\text{vac} - E_\text{c}, \quad E_\text{work} \geq E_\text{aff} \geq 0. \tag{8.25}$$

The definitions are illustrated in Figure 8.6. The energy of a particle can be expressed by its

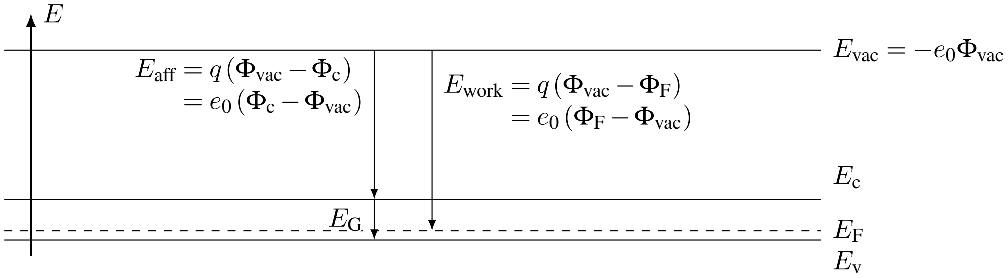


Figure 8.6: Illustration of band energy levels, work functions, electron affinity and the corresponding electric potentials; Here, $q = -e_0$

charge and an electric potential Φ

$$E = q\Phi \tag{8.26}$$

$$\Rightarrow E_{\text{work}} = q\Phi_{\text{vac}} - q\Phi_{\text{F}}, \tag{8.27}$$

$$E_{\text{aff}} = q\Phi_{\text{vac}} - q\Phi_{\text{c}}. \tag{8.28}$$

Energy diagrams in the context of semiconductors describe the energy levels of *electrons*, thus

$$q := -e_0 \tag{8.29}$$

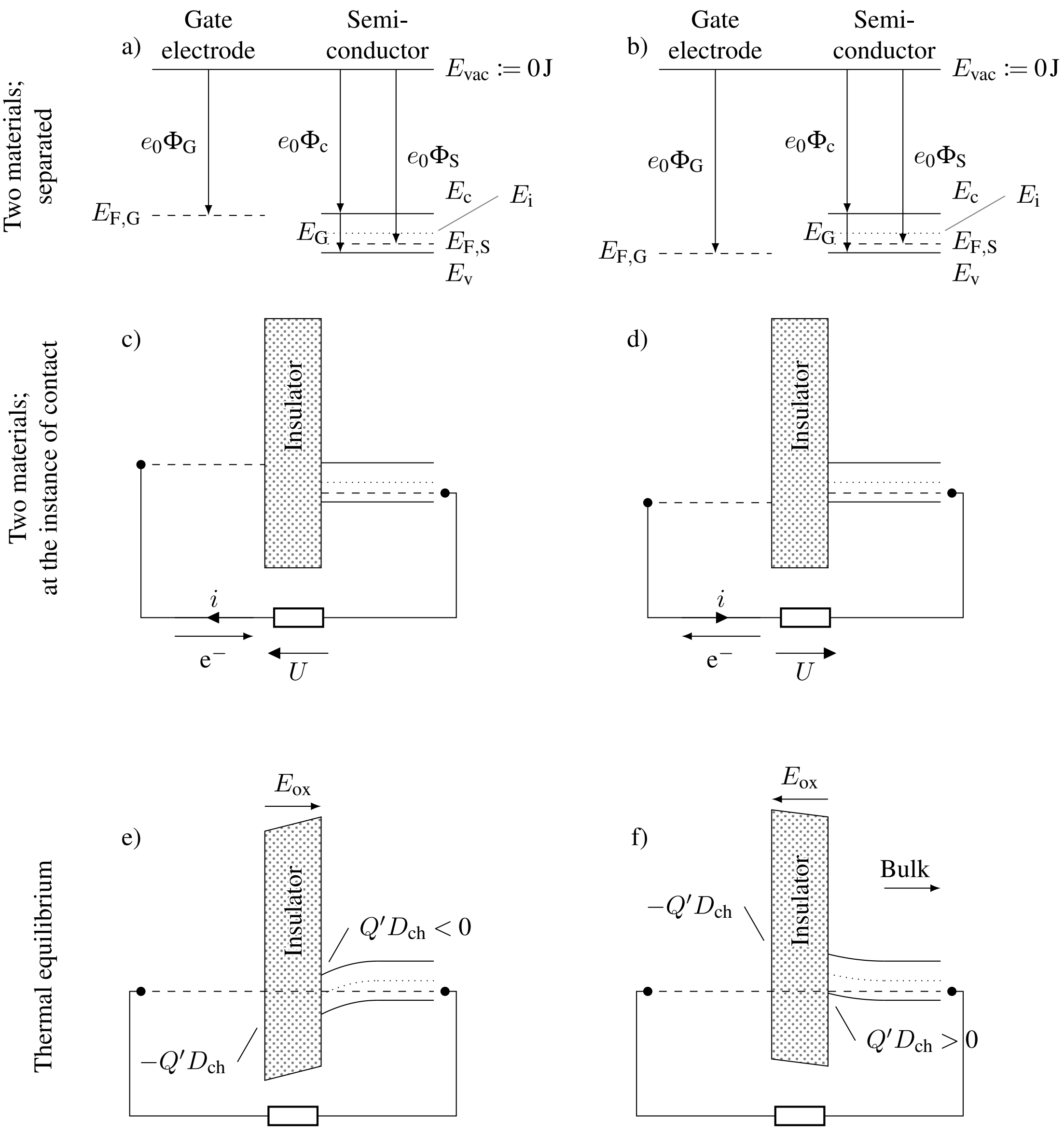
$$E_{\text{work}} = -e_0\Phi_{\text{vac}} - \left(-e_0\right)\Phi_{\text{F}} \quad \Leftrightarrow \quad \frac{E_{\text{work}}}{e_0} = \Phi_{\text{F}} - \Phi_{\text{vac}}, \tag{8.30}$$

$$E_{\text{aff}} = -e_0\Phi_{\text{vac}} - \left(-e_0\right)\Phi_{\text{c}} \quad \Leftrightarrow \quad \frac{E_{\text{aff}}}{e_0} = \Phi_{\text{c}} - \Phi_{\text{vac}}. \tag{8.31}$$

MOS structure The MOS structure consists of a semiconductor material, an insulator and a gate electrode. This work focuses an Si and SiC semiconductors only. The gate electrode can be made from different materials, e.g., aluminum or highly doped polysilicon. The insulator is simply assumed to have no leakage current, a permittivity ε_{ox} and a sufficiently large bandgap to prohibit any direct charge exchange between the gate electrode and the semiconductor.

A metal does not have a bandgap, so its Fermi level is sufficient to define its band structure in the context of this work. Different materials have different work functions, and therefore, different Fermi levels. The top row of Figure 8.7 shows the energy level diagram of a gate electrode material and a semiconductor that are completely isolated from each other. The diagrams on the left correspond to a gate electrode made from aluminum, while the diagrams on the right correspond to a gate electrode made from highly p-doped polysilicon. The semiconductor is p-doped silicon with an acceptor concentration of $N_{\text{A}}^{-} = 1.1 \cdot 10^{15}\,\frac{1}{\text{cm}^3}$.

Figure 8.7a shows the energy levels of a gate electrode material with a Fermi level higher than the semiconductor, while Figure 8.7b depicts those of an electrode material with a lower Fermi level. The intrinsic Fermi level E_{i} of the undoped semiconductor is marked in the middle of the bandgap. When the materials are connected with an ideal insulator to form a MOS structure, the differences in Fermi levels would remain. In a realistic device, a charge exchange is always possible externally, i.e., due to leakage currents or external circuitry. Thus, electrons will move from the material with the higher Fermi level to the material with



E_{vac}	vacuum energy	$E_{\mathrm{F,G}}$	Fermi level of the gate material
E_{v}	upper energy level of the valence band	$E_{\mathrm{F,S}}$	Fermi level of the semiconductor
E_{i}	Fermi level of the undoped semiconductor	Φ_{G}	work function of the gate material
E_{c}	lower energy level of the conduction band	Φ_{S}	work function of the semiconductor
q	$\widehat{=} - e_0$	Φ_{c}	electron affinity of the semiconductor

Figure 8.7: Energy levels of a gate material and a semiconductor; left hand side shows a gate electrode material (aluminum) with a smaller work function than the semiconductor; right hand side shows a gate electrode material (highly p-doped polysilicon) with a larger work function than the semiconductor; the top row shows the energy levels without any connection between the materials; the middle row shows the energy levels at the instance the materials have been contacted and no charge has shifted yet; the bottom row shows the thermal equilibrium where charge has moved, compensating the difference in Fermi levels [121]

Table 8.1: Parameters of the example materials used in this section [121]

	P-doped Silicon $N_A^- = 1.1 \cdot 10^{15}\,\frac{1}{\mathrm{cm}^3}$	Aluminum	Highly p-doped polysilicon
Work function E_{work} (or neg. Fermi level $-E_F$)	4.9 eV	4.1 eV	5.17 eV
Electron affinity E_{aff} (or neg. conduction band $-E_c$)	4.1 eV	-	-
Bandgap E_G	1.1 eV	-	-

the lower Fermi level. This process is illustrated in diagrams c and d of Figure 8.7, for the instance after the materials have been merged the first time.

> **Remark:** The fact that negatively charged particles (electrons) are used in the energy diagrams means that a positive voltage is oriented from a *lower* energy level to a *higher*.

The displacement of electrons leads to a surface charge $-Q'D_{\mathrm{ch}}$ at the electrode-insulator interface and a charge $Q'D_{\mathrm{ch}}$ close to the semiconductor-insulator interface. These charges cause an electric field E_{ox} in the insulator. Thermal equilibrium is reached when this field compensates the Fermi level difference. The thermal equilibrium is shown in diagrams e and f of Figure 8.7. The charge profiles are not included in Figure 8.7, but will be presented in Section 8.1.3.

8.1.2.1 Voltage bias

The band diagrams depicted in Figure 8.7 show the unbiased MOS structure. Depending on the applied gate voltage, the (biased) Fermi level at the surface will pass through multiple band diagram regions of the semiconductor. Figure 8.8 illustrates the used terminology [121] for the different locations of the biased Fermi level E_F with respect to the band diagram of the unbiased p-doped semiconductor. Besides the already established energy

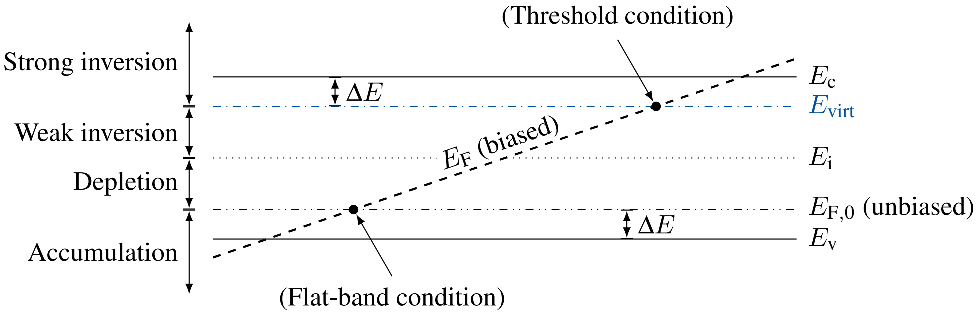


Figure 8.8: Charge conditions of a p-doped semiconductor depending on the biased Fermi level E_F; shown as reference for the used terminology; no other material present;

levels E_c, E_i, E_F and E_v, a virtual energy level E_{virt} is shown. This energy level is used as reference to define the transition between weak and strong inversion. At the virtual energy level E_{virt}, the difference between the Fermi level E_{F} and the conduction band E_{c} is the same size ΔE as the difference between the unbiased Fermi level $E_{\mathrm{F},0}$ and the valence band E_{v}. Details on the charge conditions and the marked conditions will be presented in the next paragraphs.

In a MOS structure, a voltage can be applied between the gate contact and the bulk. This bias introduces an additional difference between the Fermi levels of the gate contact material and the semiconductor. Consequently, free electrons will be transferred from one material to the other, until a new thermal equilibrium is reached. Figure 8.9 shows the band diagrams of a MOS structure with a gate voltage applied for the material combination depicted on the left-hand side of Figure 8.7. The diagrams corresponding to the material combination described on the right-hand side will be presented later.

The different surface charge conditions will be outlined in the following paragraphs. The descriptions are not ordered according to the figure, but first describe the effects when applying a positive gate voltage and then a negative. They start with a short-circuit as shown in Figure 8.9c, then for increasing gate-bulk voltage values, see Figure 8.9d to f. Afterwards, the effects of a negative gate-bulk voltage will be illustrated in accordance to Figure 8.9b and a.

The nomenclature used to describe different carrier concentrations in different semiconductor regions is listed in Table 8.2. For now, all doping atoms are assumed to be ionized, i.e., $N_{\mathrm{A}}^{-} = N_{\mathrm{A}}$. This assumption will be modified in Section 8.5.2.

Table 8.2: Nomenclature used for carrier concentrations

Electron concentration	n
Electron concentration in an n-doped region	n_{n}
Electron concentration in a p-doped region	n_{p}
Electron concentration in an unbiased p-doped region	n_{p0}
Hole concentration	p
Hole concentration in an n-doped region	p_{n}
Hole concentration in a p-doped region	p_{p}
Hole concentration in an unbiased p-doped region	p_{p0}
Acceptor doping atom concentration	N_{A}
Ionized acceptor doping atom concentration	N_{A}^{-}
Donator doping atom concentration	N_{D}
Ionized donator doping atom concentration	N_{D}^{+}
Intrinsic carrier concentration	n_{i}
Charge concentration	$q = \left(p + N_{\mathrm{D}}^{+} - n - N_{\mathrm{A}}^{-}\right) e_0$

Short circuit If the gate is shorted, i.e., Figure 8.9c, the band energy levels match those shown in Figure 8.7 on the right-hand side. The difference between the work function of a)

Negative voltage	
Applied gate voltage	$U_{\mathrm{gb}} < U_{\mathrm{fb}} < 0\,\mathrm{V}$
Surface charge condition	Accumulation
Surface carrier density	$p_{\mathrm{p}} > N_{\mathrm{A}}^{-} = p_{\mathrm{p0}}$

b)

Flat-band voltage	
Applied gate voltage	$U_{\mathrm{gb}} = U_{\mathrm{fb}} < 0\,\mathrm{V}$
Surface charge condition	Neutral/Flat band
Surface carrier density	$p_{\mathrm{p}} = N_{\mathrm{A}}^{-} = p_{\mathrm{p0}}$

c)

Thermal equilibrium/Short circuit	
Applied gate voltage	$U_{\mathrm{gb}} = 0\,\mathrm{V}$
Surface charge condition	Depletion
Surface carrier density	$p_{\mathrm{p}} < N_{\mathrm{A}}^{-}$

d)

Small positive gate voltage	
Applied gate voltage	$U_{\mathrm{th,b}} > U_{\mathrm{gb}} > 0\,\mathrm{V}$
Surface charge condition	Weak inversion
Surface carrier density	$p_{\mathrm{p}} < n_{\mathrm{i}} < n_{\mathrm{p}} < N_{\mathrm{A}}^{-} = p_{\mathrm{p0}}$

e)

Threshold voltage	
Applied gate voltage	$U_{\mathrm{gb}} = U_{\mathrm{th,b}}$
Surface charge condition	Beginning of strong inversion
Surface carrier density	$n_{\mathrm{p}} = N_{\mathrm{A}}^{-} = p_{\mathrm{p0}}$

f)

Positive voltage	
Applied gate voltage	$U_{\mathrm{gb}} > U_{\mathrm{th,b}}$
Surface charge condition	Strong inversion
Surface carrier density	$n_{\mathrm{p}} > N_{\mathrm{A}}^{-}$

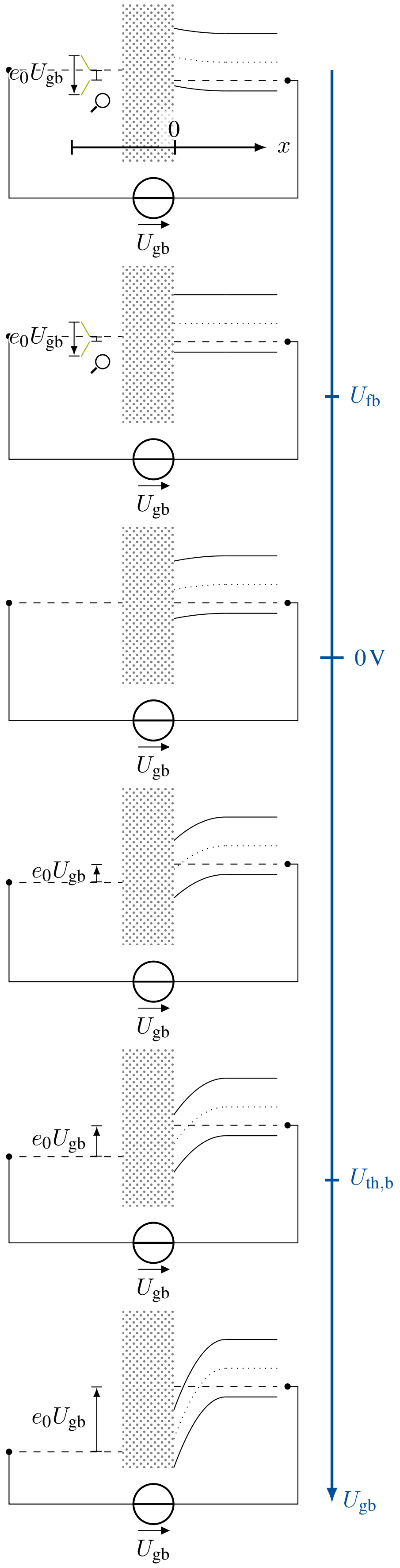


Figure 8.9: Applied gate voltage U_{gs}, surface charges and band diagrams [121]; example shown for a gate material with a larger work function than the semiconductor

the gate contact material and the doped semiconductor leads to a depletion of holes at the insulator semiconductor interface, or surface of the semiconductor. The concentration of holes p_p at the surface, i.e., $x=0$, is lower than the concentration of holes p_p0 in the unbiased bulk of the semiconductor, but the concentration is still larger than the intrinsic carrier concentration n_i

$$n_\mathrm{i} < p_\mathrm{p}\big|_{x=0} < p_\mathrm{p0} \mathrel{\widehat{=}} p_\mathrm{p}\big|_{x\to\infty}. \tag{8.32}$$

The x coordinate axis is oriented from the insulator semiconductor interface towards the bulk, as shown in Figure 8.9a. This definition matches Figure 8.4. For now, the concentration of holes p_p0 in the unbiased bulk of the semiconductor is assumed to be equal to the donator concentration N_A^-

$$p_\mathrm{p0} = N_\mathrm{A}^-. \tag{8.33}$$

In the example shown in Figure 8.7c, the Fermi level E_F at the surface of the semiconductor is lower than Fermi level E_i of the intrinsic semiconductor. Based on the mass-action law [121], the concentration of electrons n_p at the surface must be smaller than the intrinsic carrier concentration n_i and hole concentration p_p. Thus, (8.32) can be described more precisely

$$\text{Mass-action law [121]:} \quad np = n_\mathrm{i}^2, \tag{8.34}$$

$$E_\mathrm{F}\big|_{x=\to\infty} < E_\mathrm{F}\big|_{x=0} < E_\mathrm{i}, \tag{8.35}$$

$$\Rightarrow n_\mathrm{p}\big|_{x=0} < n_\mathrm{i} < p_\mathrm{p}\big|_{x=0} < p_\mathrm{p0}. \tag{8.36}$$

The semiconductor charge is in depletion at the surface.

> **Remark:** A different material combination could lead to an inversion layer already being formed in an unbiased state.

Small positive voltage When applying a small positive voltage U_gb, the Fermi level at the surface increases. At a certain voltage level, the Fermi level at the surface is larger than the Fermi level E_i of the intrinsic semiconductor, see Figure 8.9d.

$$E_\mathrm{F}\big|_{x=0} > E_\mathrm{i}. \tag{8.37}$$

In the example shown, see Figure 8.7d,, the small positive voltage U_gb is still smaller than the threshold voltage $U_\mathrm{th,b}$. In [69], the threshold voltage $U_\mathrm{th,b}$ is defined as the gate voltage required to bring the surface charge layer into strong inversion.

> **Remark:** It is important to note that the threshold voltage $U_\mathrm{th,b}$ of the MOS structure is referenced to the bulk instead of the source. A translation between this threshold voltage $U_\mathrm{th,b}$ and the typical threshold voltage of the device U_th, applied between the gate and source contact, will be introduced later.

Strong inversion begins when energy difference between the conduction band E_c and the Fermi level E_F at the surface becomes smaller than the energy difference between the Fermi level and the valence band E_v of the unbiased, doped semiconductor

$$0\,\mathrm{V} < U_\mathrm{gb} < U_\mathrm{th,b} \tag{8.38}$$

$$\Leftrightarrow (E_\mathrm{c} - E_\mathrm{F})\big|_{x=0} < (E_\mathrm{F} - E_\mathrm{v})\big|_{x\to\infty}. \tag{8.39}$$

The surface charge layer is weakly inverted

$$p_\mathrm{p}\big|_{x=0} < n_\mathrm{i} < n_\mathrm{p}\big|_{x=0} < p_\mathrm{p0}. \tag{8.40}$$

Threshold voltage As previously described, the threshold voltage $U_\mathrm{th,b}$ is defined as the gate-bulk voltage[5] required to bring the surface charge layer into strong inversion [69].

$$\text{Threshold condition [69]:}\quad n_\mathrm{p}\big|_{x=0} = p_\mathrm{p0} = N_\mathrm{A}^- \tag{8.41}$$

$$\Leftrightarrow (E_\mathrm{c} - E_\mathrm{F})\big|_{x=0} = (E_\mathrm{F} - E_\mathrm{v})\big|_{x\to\infty} \tag{8.42}$$

$$\Leftrightarrow U_\mathrm{gb} = U_\mathrm{th,b}. \tag{8.43}$$

The band diagram with the threshold voltage applied is outlined in Figure 8.9e and Figure 8.10 shows more details of this particular state.

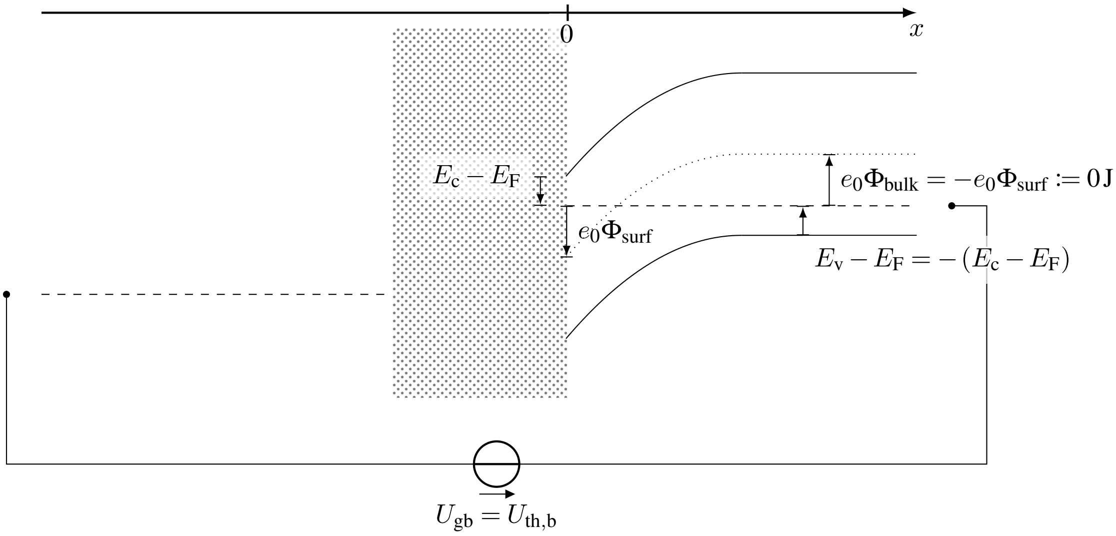


Figure 8.10: Band diagram when the threshold voltage is applied to the gate contact, $U_\mathrm{gs} = U_\mathrm{th}$ or $U_\mathrm{gb} = U_\mathrm{th,b}$, [121]; the intrinsic Fermi level E_i is chosen as the reference potential arbitrarily; x coordinate axis is oriented from the insulator semiconductor interface towards the bulk, as shown in Figure 8.4

Large positive voltage Increasing the gate voltage beyond the threshold voltage leads to a strong inversion, according to the definition of the threshold voltage (8.41). This is the typical state of the MOSFET when it is turned on

$$U_\mathrm{gb} > U_\mathrm{th,b} \tag{8.44}$$

$$\Leftrightarrow n_\mathrm{p}\big|_{x=0} > p_\mathrm{p0} = N_\mathrm{A}^-. \tag{8.45}$$

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[5] The threshold voltage is typically defined as a gate-source voltage instead of a gate-bulk voltage.

This case is illustrated in Figure 8.9f.

Flat-band voltage So far, the descriptions of the different surface charge conditions covered the application of a positive gate voltage. For the combination of gate material and semiconductor shown in Figure 8.9, the application of a small negative gate voltage will counteract the depletion of holes at the surface of the semiconductor. At a certain level of $U_{\mathrm{gs}} < 0\,\mathrm{V}$, the Fermi level difference between the gate contact material and the semiconductor is compensated precisely, which is defined as the *flat-band* condition [121]

$$\text{Flat-band condition [121]:}\quad p_{\mathrm{p}}\big|_{x=0} = p_{\mathrm{p0}} = N_{\mathrm{A}}^{-} \tag{8.46}$$

$$\Leftrightarrow (E_{\mathrm{F}} - E_{\mathrm{v}})\big|_{x=0} = (E_{\mathrm{F}} - E_{\mathrm{v}})\big|_{x\to\infty} \tag{8.47}$$

$$\Leftrightarrow U_{\mathrm{gb}} = U_{\mathrm{fb}}. \tag{8.48}$$

Large negative voltage Further increasing the amplitude of the negative gate voltage leads to an accumulation of holes, see Figure 8.9a

$$U_{\mathrm{gb}} < U_{\mathrm{fb}} \tag{8.49}$$

$$\Leftrightarrow p_{\mathrm{p}}\big|_{x=0} > p_{\mathrm{p0}} = N_{\mathrm{A}}^{-}. \tag{8.50}$$

Other material combinations The descriptions of the surface charge conditions used the example case of a gate material with a larger work function than the semiconductor. If the work function is smaller, the same cases occur, but the conditions for the unbiased system change.

Figure 8.11 shows the same diagrams as Figure 8.9 for a with a smaller work function than the semiconductor, as shown on the right-hand side of Figure 8.7. The surface charge conditions shown in Figure 8.11 are generally analogous to those shown for the other material combination in Figure 8.9, except for two differences. First, an accumulation layer is already formed at the interface between the semiconductor and the insulator if the gate-source path is shorted, see Figure 8.11b. Consequently, a positive gate-source voltage is required for the flat band condition, see Figure 8.11c. This shows, that the flat-band voltage U_{fb} for a semiconductor device can be positive or negativ. The actual flat-band voltage depends on the used materials, doping concentrations and semiconductor structure [121].

8.1.3 Nonlinear gate charge curve

The surface charge of the MOS structure passes through several charge conditions[6] when the gate voltage is changed from a negative to a positive voltage. The Q_{ch}-U_{gs} relationship changes depending on the surface charge condition, which can be expressed modeled with a piecewise function definition.

Depleted or weakly inverted surface layer When a gate voltage between the flat-band voltage and the threshold voltage is applied, the surface charge is layer is in depletion or weak inversion. In these cases, the concentration of holes and electrons is smaller than the

---

[6] accumulation, depletion, weak inversion, strong inversion

a)

Negative gate voltage	
Applied gate voltage	$U_{\mathrm{gb}} < 0\,\mathrm{V}$
Surface charge condition	Accumulation
Surface carrier density	$p_{\mathrm{p}} > N_{\mathrm{A}}^{-}$

b)

Thermal equilibrium/Short circuit	
Applied gate voltage	$U_{\mathrm{gb}} = 0\,\mathrm{V}$
Surface charge condition	Accumulation
Surface carrier density	$p_{\mathrm{p}} > N_{\mathrm{A}}^{-}$

c)

Flat-band voltage	
Applied gate voltage	$U_{\mathrm{gb}} = U_{\mathrm{fb}} > 0\,\mathrm{V}$
Surface charge condition	Neutral/Flat band
Surface carrier density	$p_{\mathrm{p}} = N_{\mathrm{A}}^{-} = p_{\mathrm{p0}}$

d)

Small positive gate voltage	
Applied gate voltage	$U_{\mathrm{th,b}} > U_{\mathrm{gb}} > 0\,\mathrm{V}$
Surface charge condition	Depletion
Surface carrier density	$n_{\mathrm{i}} < p_{\mathrm{p}} < N_{\mathrm{A}}^{-}$

e)

Threshold voltage	
Applied gate voltage	$U_{\mathrm{gb}} = U_{\mathrm{th,b}}$
Surface charge condition	Beginning of strong inversion
Surface carrier density	$n_{\mathrm{p}} = N_{\mathrm{A}}^{-}$

f)

Threshold voltage	
Applied gate voltage	$U_{\mathrm{gb}} > U_{\mathrm{th,b}}$
Surface charge condition	Strong inversion
Surface carrier density	$n_{\mathrm{p}} > N_{\mathrm{A}}^{-}$

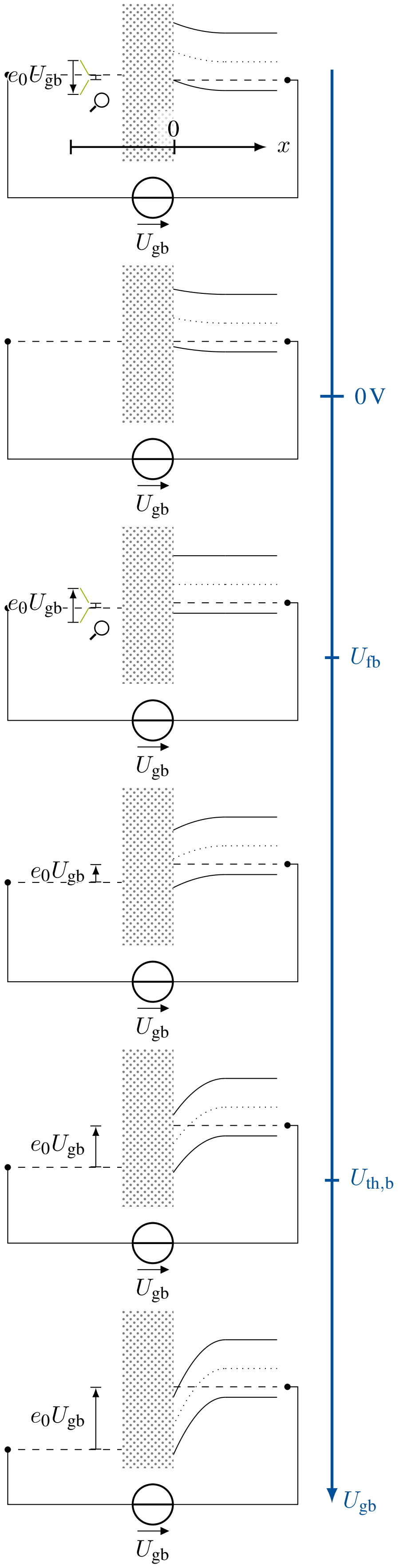


Figure 8.11: Applied gate voltage U_{gs}, surface charges and band diagrams [121]; example shown for a gate material with a smaller work function than the semiconductor

concentration of the ionized acceptor atoms N_A^- and the electric potential at the surface is higher than in the bulk

$$n_\mathrm{p}\big|_{x=0} < N_\mathrm{A}^-, \quad p_\mathrm{p}\big|_{x=0} < N_\mathrm{A}^-. \tag{8.51}$$

As the potential at the surface is larger than in the bulk, a depletion layer must from between the surface and the bulk, compensating the potential difference. Modeling the dependencies between the charge concentrations, electric field and electric potential can be done with the *depletion approximation* [121], which is also called approximation for an *abrupt junction* [69]. The depletion approximation assumes that the carrier concentrations are piecewise constant. In particular, the approximation assumes that a depletion layer forms from the surface towards the bulk with a width of b_sc, where the concentration of free carriers n_p and p_p is zero. Only the acceptor atoms remain in this region with an assumed homogenous concentration of N_A^-, although the depletion approximation can also be used to model other distributions of doping atoms [121]. Poisson's equation for electrostatics describes the relationship between the charge concentration q, electric field E and electric potential Φ

$$\text{Poisson's equation:} \quad \Phi = \int E \mathrm{d}x = \iint -\frac{q}{\varepsilon} \mathrm{d}x \mathrm{d}x. \tag{8.52}$$

The permittivity ε is assumed to be constant throughout each material. Applying Poisson's equation to the depletion assumption yields the charge, field and potential profiles shown in Figure 8.12. In the semiconductor, the constant charge density $q = -e_0 N_\mathrm{A}^-$ of the space-charge region leads to a linear electric field E and a parabolic electric potential Φ. The insulator is assumed to be charge free, thus the electric field inside E_ox is constant and the electric potential profile is linear. At the gate-insulator interface, a surface charge Q_s' layer forms. The width of this charge layer is not drawn to scale for better visibility. Assuming a material with infinite conductivity, the layer is infinitely small [121].

> **Remark:** The thickness of the inversion layer is significantly smaller than that of the space-charge region. Thus, it is typically modeled as Dirac delta function. This simplification will be used in the further course of this section and Figure 8.15, but will be reassessed in Section 8.1.4.1.

For Figure 8.12, the voltage in the bulk is defined as the 0 V reference and the electric potential Φ is substituted by a voltage U. According to the depletion approximation, there is no unbalanced charge for $x > b_\mathrm{sc}$. Therefore, this location has the same electric potential as inside the bulk

$$U(x) = \Phi(x) - \Phi(b_\mathrm{sc}), \tag{8.53}$$

$$\Phi(b_\mathrm{sc}) := 0\,\mathrm{V}, \quad E(b_\mathrm{sc}) := 0\,\frac{\mathrm{V}}{\mathrm{m}}. \tag{8.54}$$

The electric field E inside the semiconductor can be determined by integrating the charge from the voltage reference point $x = b_\mathrm{sc}$ to the desired location x. Since the direction of integration is opposed to the x coordinate, a negative sign occurs at the begging of the equation

$$E(x) = -\int_{b_\mathrm{sc}}^{x} -\frac{q}{\varepsilon_\mathrm{Si}} \mathrm{d}\tilde{x} = -\left[-\frac{q}{\varepsilon_\mathrm{Si}}\tilde{x}\right]_{b_\mathrm{sc}}^{x} = -\frac{q}{\varepsilon_\mathrm{Si}}\left(b_\mathrm{sc} - x\right), \quad 0 \le x \le b_\mathrm{sc}. \tag{8.55}$$

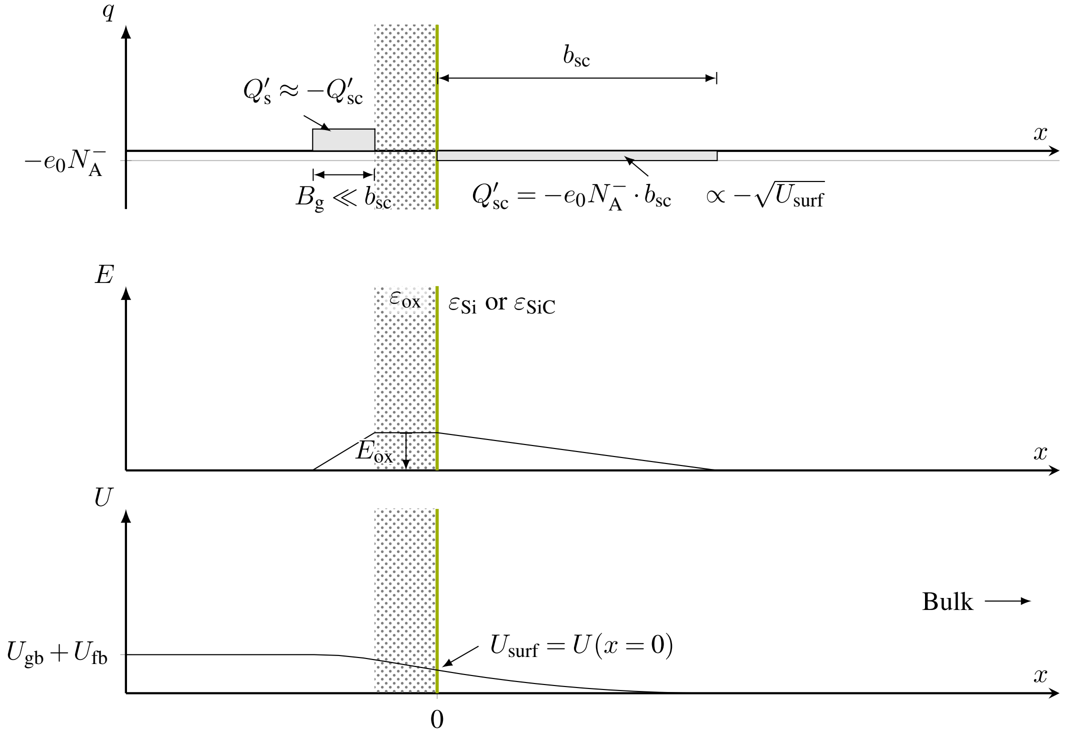


Figure 8.12: Relevant charge components of the MOS channel [121] in depletion or weak inversion; space charge Q'_{sc} is stationary; not drawn to scale; the width B_{g} of the charge layer at the gate-insulator interface is much smaller than the width of the space-charge region b_{sc}; insulator-semiconductor interface marked in green; electric potential in the bulk used as 0 V voltage reference

The descriptions in this this section use the permittivity $\varepsilon_{\mathrm{Si}}$ of a Si semiconductor. If a SiC semiconductor is used, the variable has to be substituted accordingly.

Poisson's equation (8.52) and (8.55) yield the voltage U

$$U(x) = -\int_{b_{\mathrm{sc}}}^{x} E(x)\,\mathrm{d}\tilde{x} = -\left[-\frac{q}{\varepsilon_{\mathrm{Si}}}\left(b_{\mathrm{sc}}\tilde{x} - \frac{\tilde{x}^2}{2}\right)\right]_{b_{\mathrm{sc}}}^{x}, \tag{8.56}$$

$$= \frac{q}{\varepsilon_{\mathrm{Si}}}\left(b_{\mathrm{sc}}x - b_{\mathrm{sc}}^2 - \frac{x^2}{2} + \frac{b_{\mathrm{sc}}^2}{2}\right), \tag{8.57}$$

$$= \frac{q}{\varepsilon_{\mathrm{Si}}}\left(-\frac{x^2}{2} + b_{\mathrm{sc}}x - \frac{b_{\mathrm{sc}}^2}{2}\right), \quad q = -e_0 N_{\mathrm{A}}^-,\ 0 \le x \le b_{\mathrm{sc}}. \tag{8.58}$$

At the surface, $x = 0$, the electric field E, the voltage U, and the total charge of the space-charge region Q'_{sc} are

$$E\big|_{x=0} = -\frac{q}{\varepsilon_{\mathrm{Si}}} b_{\mathrm{sc}} = \frac{e_0 N_{\mathrm{A}}^-}{\varepsilon_{\mathrm{Si}}} b_{\mathrm{sc}}, \tag{8.59}$$

$$U_{\mathrm{surf}} := U\big|_{x=0} = -\frac{q}{\varepsilon_{\mathrm{Si}}}\frac{b_{\mathrm{sc}}^2}{2} = \frac{e_0 N_{\mathrm{A}}^-}{\varepsilon_{\mathrm{Si}}}\frac{b_{\mathrm{sc}}^2}{2}, \tag{8.60}$$

$$Q'_{\mathrm{sc}} = q b_{\mathrm{sc}} D_{\mathrm{ch}} = -e_0 N_{\mathrm{A}}^- b_{\mathrm{sc}} D_{\mathrm{ch}}. \tag{8.61}$$

Equation (8.60) and (8.61) yield the typical square-root relationship between the charge density Q'_{sc} and the surface voltage U_{surf} of a depletion layer [69]

$$Q'_{\mathrm{sc}}(U_{\mathrm{surf}}) = -\sqrt{2\varepsilon_{\mathrm{Si}} N_{\mathrm{A}}^{-} e_0 U_{\mathrm{surf}}} D_{\mathrm{ch}}, \tag{8.62}$$

$$Q_{\mathrm{sc}}(U_{\mathrm{surf}}) = -\sqrt{2\varepsilon_{\mathrm{Si}} N_{\mathrm{A}}^{-} e_0 U_{\mathrm{surf}}} D_{\mathrm{ch}} L_{\mathrm{ch}}. \tag{8.63}$$

Strongly inverted channel When the channel is brought into strong inversion, the concentration of electrons at the surface is greater than the concentration of holes within the bulk of the semiconductor (8.45). The charge concentration can no longer be assumed to be fixed or bound to the concentration of the doping atoms.

Generally, the concentration of electrons or holes in a semiconductor can be determined by integrating the density of allowed states with their probability of being populated [121]. The latter follows the Fermi-Dirac distribution, which depends on the (local) voltage bias. Without going into detail, the electron concentration n_{p} and hole concentration p_{p} in a p-doped semiconductor can be described by Boltzmann's relationship [121]

$$n_{\mathrm{p}} = n_{\mathrm{p0}} \mathrm{e}^{\frac{U}{U_{\mathrm{T}}}}, \tag{8.64}$$

$$p_{\mathrm{p}} = p_{\mathrm{p0}} \mathrm{e}^{-\frac{U}{U_{\mathrm{T}}}}, \tag{8.65}$$

$$U_{\mathrm{T}} = \frac{k\vartheta}{e_0}, \tag{8.66}$$

where k is the Boltzmann constant, ϑ the temperature and U_{T} the *thermal voltage*. The voltage U is referenced to the electric potential in the bulk of the semiconductor. To keep consistency, the electron concentration n_{p0} and the hole concentration p_{p0} of the unbiased semiconductor must also be referenced to the bulk.

In this paragraph, the charge of free electrons Q'_{n} of the inversion layer will be quantified when a positive gate voltage greater than the threshold voltage is applied. the charge of the inversion layer depend exponentially on the surface voltage U_{surf} and their concentration decreases in the direction of the bulk.

The exponential voltage dependency of the charge of the inversion layer Q'_{n} is in strong contrast to the behaviour of the charge components Q'_{sc} of the space-charge region (8.62). Precisely determining the charge distribution of electrons requires solving Poisson's equation. As this is not explicitly possible [123], an approximation is used. The width of the inversion layer with relevant amounts of charge is in the order of several Debye lengths $L_{\mathrm{D}} = \sqrt{\frac{\varepsilon_{\mathrm{Si}} U_{\mathrm{T}}}{e_0 n_{\mathrm{p0}}}}$ and can be neglected when compared to the width of the space-charge region [68, 121]. The concepts of the depletion approximation are transferred and the inversion layer is modeled to have a constant electron concentration and the width B_{n}.

Figure 8.13 illustrates the resulting charge of the inversion layer Q'_{n} and the charge of the space-charge region Q'_{sc}. The channel is formed at the insulator-semiconductor interface.

The closed line integral of the electric field from the bulk to the gate contact, returning through the externally applied gate voltage, is used to determine the inversion layer charge Q'_{n}

$$0\,\mathrm{V} = \oint_L E \mathrm{d}L. \tag{8.67}$$

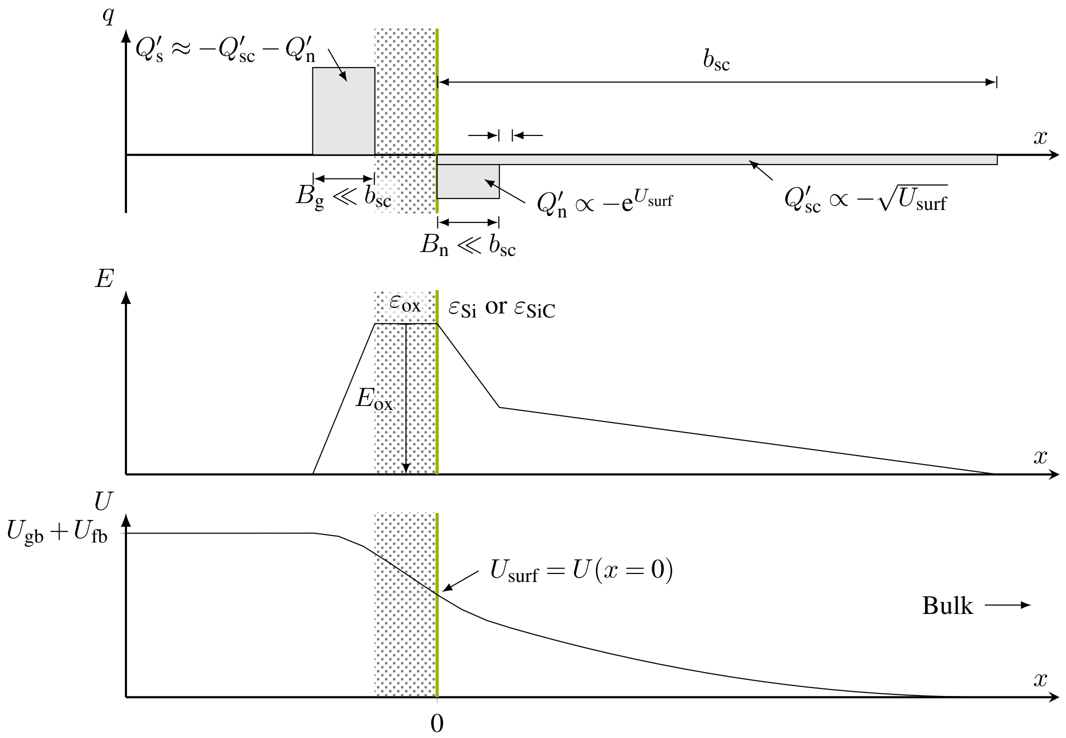


Figure 8.13: Charge components of the MOS channel in strong inversion [121]; space charge Q'_{sc} is stationary; not drawn to scale; the width B_{g} of the charge layer at the gate-insulator interface is much smaller than the width of the space-charge region b_{sc}; insulator-semiconductor interface marked in green; electric potential in the bulk used as 0 V voltage reference

The path of the line integral is also shown in Figure 8.14. In a MOS structure, the difference in Fermi levels between the gate material and the semiconductor leads to a charge being present in the unbiased state. Only when the flat-band voltage U_{fb} is applied, the charge becomes zero

$$U_{\mathrm{gb}} - U_{\mathrm{fb}} = -\int_{\infty}^{-\infty} E\,\mathrm{d}x = \int_{\infty}^{-\infty}\int_{\infty}^{-\infty} \frac{q}{\varepsilon}\,\mathrm{d}\tilde{x}\,\mathrm{d}x. \tag{8.68}$$

The contribution of the space-charge region to the electric field was already determined in (8.59) to (8.62). The inversion layer charge Q'_{n} and the charge within the gate contact Q'_{s} are modeled infinitely small using a Dirac delta function $\delta(x)$. The model concept is illustrated in Figure 8.15. Let the location $x = 0$ be located in the semiconductor, then

$$E\big|_{x=0} = -\int_{\infty}^{0} -\frac{q}{\varepsilon}\,\mathrm{d}x = \int_{b_{\mathrm{sc}}}^{0} \frac{-N_{\mathrm{A}}^{-} e_0}{\varepsilon_{\mathrm{Si}}}\,\mathrm{d}x + \int_{\infty}^{-\infty} \frac{Q'_{\mathrm{n}}}{D_{\mathrm{ch}}\varepsilon_{\mathrm{Si}}}\,\frac{\delta(x)}{1\,\mathrm{m}}\,\mathrm{d}x \tag{8.69}$$

$$= \frac{-Q'_{\mathrm{sc}} - Q'_{\mathrm{n}}}{D_{\mathrm{ch}}\varepsilon_{\mathrm{Si}}}, \quad Q = qbL_{\mathrm{ch}}D_{\mathrm{ch}},\ Q' = qbD_{\mathrm{ch}}. \tag{8.70}$$

At the insulator-semiconductor interface $x = 0$, the permittivity changes. The electric field $E\big|_{x=0^-}$ on the insulator side of the interface depends on the electric field on the semicon-

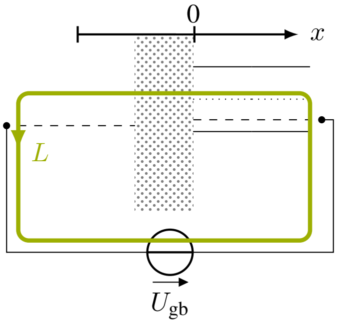


Figure 8.14: Path of the line integral; example shows the semiconductor in flat-band condition

ductor side $E\big|_{x=0}$ and the ratio of the permittivities

$$E_{\mathrm{ox}} = E\big|_{x=0^-} = \frac{\varepsilon_{\mathrm{Si}}}{\varepsilon_{\mathrm{ox}}} E\big|_{x=0} = \frac{-Q'_{\mathrm{sc}} - Q'_{\mathrm{n}}}{D_{\mathrm{ch}}\varepsilon_{\mathrm{ox}}}. \tag{8.71}$$

Knowledge of the electric field E_{ox} in the insulator and the already determined voltage contribution of the space-charge region (8.59) are sufficient to solve the closed line integral (8.67)

$$U_{\mathrm{gb}} - U_{\mathrm{fb}} = -\int_{\infty}^{-\infty} E\mathrm{d}x \tag{8.72}$$

$$= -\int_{b_{\mathrm{sc}}}^{0} E(x)\,\mathrm{d}x - \int_{0}^{-B_{\mathrm{ins}}} E_{\mathrm{ox}}\mathrm{d}x \tag{8.73}$$

$$= U_{\mathrm{surf}} + E_{\mathrm{ox}} B_{\mathrm{ins}}. \tag{8.74}$$

The term U_{surf} in (8.74) is due to the space-charge region. The inversion layer and the charge inside the gate material contact have no immediate impact on the voltage, as they are modeled infinitely small. The right term $E_{\mathrm{ox}}B_{\mathrm{ins}}$ can also be expressed by the charges using (8.71), which yields

$$U_{\mathrm{gb}} - U_{\mathrm{fb}} = U_{\mathrm{surf}} + \left(-Q'_{\mathrm{sc}} - Q'_{\mathrm{n}}\right) \frac{B_{\mathrm{ins}}}{D_{\mathrm{ch}}\varepsilon_{\mathrm{ox}}}. \tag{8.75}$$

The voltage at the surface U_{surf} can also be described by the charge Q'_{sc} of the space-charge region (8.62)

$$U_{\mathrm{surf}} = \frac{e_0 N_{\mathrm{A}}^-}{\varepsilon_{\mathrm{Si}}} \frac{b_{\mathrm{sc}}^2}{2} = \frac{{Q'_{\mathrm{sc}}}^2}{2\varepsilon_{\mathrm{Si}} N_{\mathrm{A}}^- e_0 D_{\mathrm{ch}}^2}, \tag{8.76}$$

$$U_{\mathrm{gb}} - U_{\mathrm{fb}} = \frac{{Q'_{\mathrm{sc}}}^2}{2\varepsilon_{\mathrm{Si}} N_{\mathrm{A}}^- e_0 D_{\mathrm{ch}}^2} + \left(-Q'_{\mathrm{sc}} - Q'_{\mathrm{n}}\right) \frac{B_{\mathrm{ins}}}{D_{\mathrm{ch}}\varepsilon_{\mathrm{ox}}}. \tag{8.77}$$

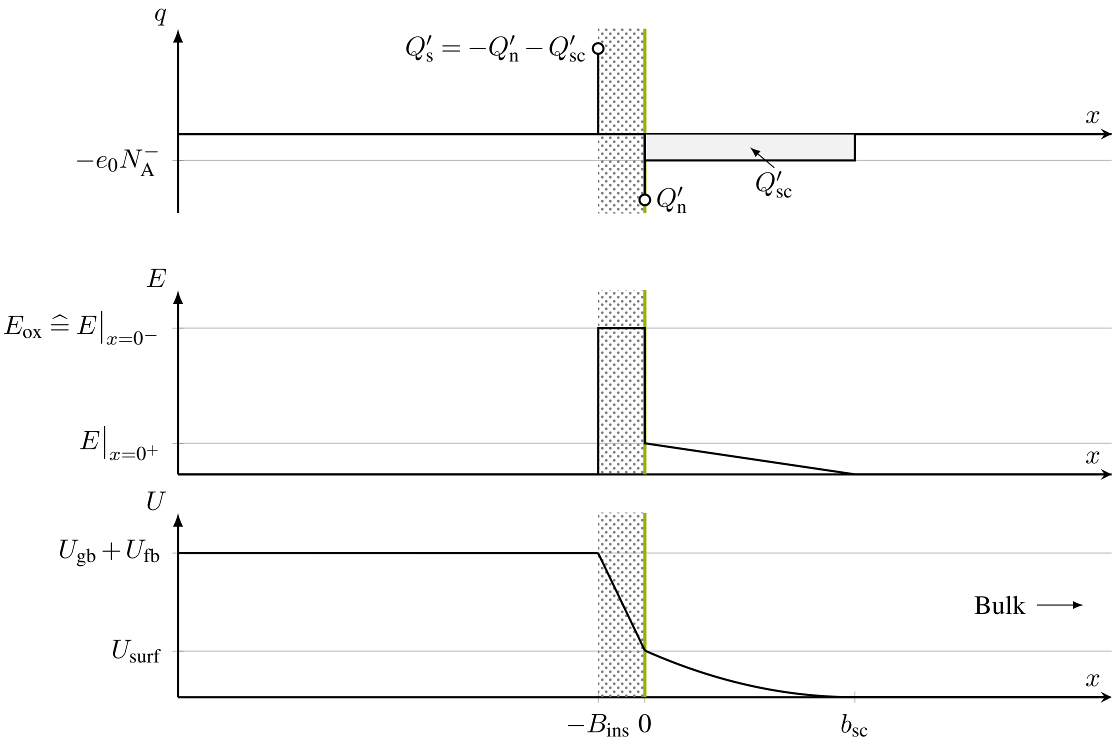


Figure 8.15: Modeling approach used to quantify the inversion layer charge Q_n; The inversion layer charge and the charge in the gate contact are modeled as Dirac delta pulses δ

Solving this equation for the free carrier charge Q'_n yields

$$Q'_\mathrm{n} = -\frac{D_\mathrm{ch}\varepsilon_\mathrm{ox}}{B_\mathrm{ins}}\left(U_\mathrm{gb} - U_\mathrm{fb}\right) + \frac{\varepsilon_\mathrm{ox}}{D_\mathrm{ch} B_\mathrm{ins}} \frac{{Q'_\mathrm{sc}}^2}{2\varepsilon_\mathrm{Si} N_\mathrm{A}^- e_0} - Q'_\mathrm{sc} \tag{8.78}$$

$$= -C'_\mathrm{ox}\left(U_\mathrm{gb} - U_\mathrm{fb}\right) + C'_\mathrm{ox} \frac{{Q'_\mathrm{sc}}^2}{2\varepsilon_\mathrm{Si} N_\mathrm{A}^- e_0} - Q'_\mathrm{sc}, \quad C'_\mathrm{ox} = \frac{D_\mathrm{ch}\varepsilon_\mathrm{ox}}{B_\mathrm{ins}}. \tag{8.79}$$

This can also be stated using the surface voltage U_surf (8.62)

$$U_\mathrm{gb} - U_\mathrm{fb} = U_\mathrm{surf} + \left(\sqrt{2\varepsilon_\mathrm{Si} N_\mathrm{A}^- e_0 U_\mathrm{surf}} D_\mathrm{ch} - Q'_\mathrm{n}\right) \frac{B_\mathrm{ins}}{D_\mathrm{ch}\varepsilon_\mathrm{ox}}, \tag{8.80}$$

$$Q'_\mathrm{n} = -C'_\mathrm{ox}\left(U_\mathrm{gb} - \overbrace{U_\mathrm{fb} - U_\mathrm{surf}}^{\text{corresponds to threshold voltage}}\right) \underbrace{+ \sqrt{2\varepsilon_\mathrm{Si} N_\mathrm{A}^- e_0 U_\mathrm{surf}} D_\mathrm{ch}}_{\text{immovable charge } -Q_\mathrm{sc}\text{, not contributing to conductivity}}. \tag{8.81}$$

Considering that Q'_n and Q'_sc are negative for an n-channel MOSFET, the square-root term reduces the amount of free charge. It describes the reduction of the free carrier charge in the channel due to the stationary charge bound in the space-charge region.

Gate charge curve on the surface level The different cases of the surface charge lead to different charge-voltage relationships at the surface. In depletion and weak inversion, the square-root relationship of the space-charge region dominates the relationship, while Boltzman's exponential relationship between voltage an charge concentration describes the most significant effects in accumulation and strong inversion. Thus, the relationship is nonlinear. Figure 8.16 shows an illustration of the gate charge components of the accumulation layer Q'_p, inversion layer Q'_n and space charge Q'_sc [121] and annotations of the surface-level carrier concentrations $n^{(\mathrm{surf})}$ and $p^{(\mathrm{surf})}$ depending on the surface voltage U_surf. The sum of the

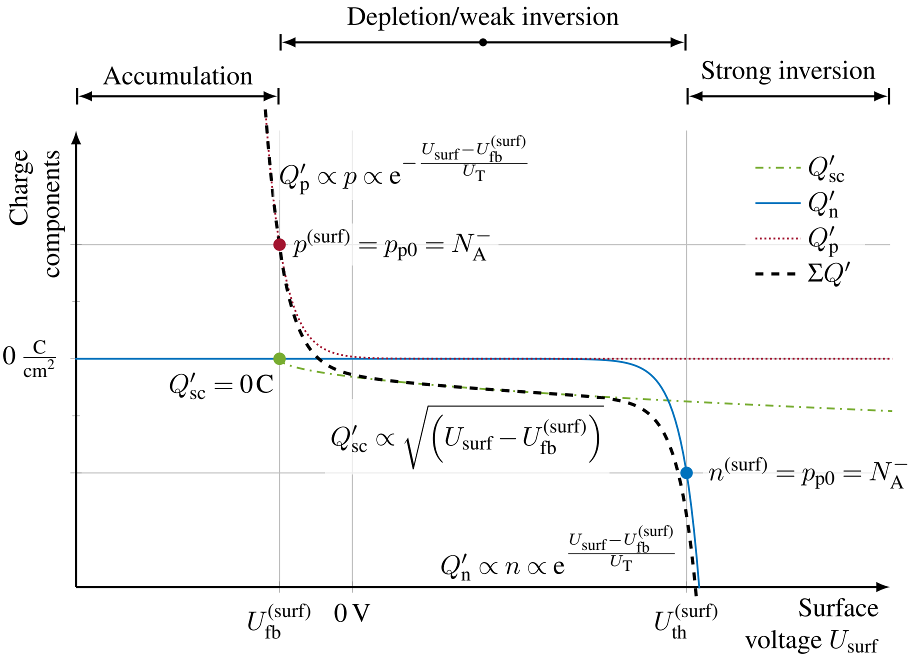


Figure 8.16: Illustration of the gate charge components of the accumulation layer Q'_p, inversion layer Q'_n and space charge Q'_sc for an n-channel MOSFET according to [121]; annotations of the surface-level carrier concentrations $n^{(\mathrm{surf})}$ and $p^{(\mathrm{surf})}$; sum of all components $\Sigma Q'$ dashed; proportional relationships assume a constant width of the accumulation or inversion layer as well a homogeneous charge concentration within; the relative size difference between the space charge Q'_sc and the free carrier charges Q'_p or Q'_n depends on the doping ratio N_A and the value of the gate oxide C_ox, and thus, cannot be quantified without detailed knowledge of the device; characteristic voltages U_th and U_fb noted as their value on the surface of the channel

charge components $\Sigma Q'$ has three distinct regions. When the surface of the semiconductor is in accumulation $p > N_\mathrm{A}^-$ or strong inversion $n > N_\mathrm{A}^-$, the sum of the charge components shows an exponential dependency on the surface voltage U_surf. In depletion or weak inversion, the free carriers are neglectable compared to the concentration of (ionized) doping atoms N_A^-, leading to a square-root relation between the sum of the charge components $\Sigma Q'$ and the surface voltage.

> **Remark:** The qualitative characteristics of this gate charge curve with regard to the surface voltage in Figure 8.16 can be related to the gate charge curve measured in Section 7.2, see Figure 7.10. Two aspects must be considered. First, the relationship between the gate-source voltage and the surface voltage is nonlinear, i.e., $U_\mathrm{surf} = f\left(U_\mathrm{gs}\right)$, see (8.81). Thus, the shapes of

> their characteristics are not identical. Second, the gate charge curve shown in Figure 7.10 was measured from the outside of the module. Hence, it also includes other capacitive components, e.g., the capacitance between the gate and source electrodes on the chip or the Miller capacitance in the semiconductor. Nevertheless, the smaller derivative of the charge with regard to the surface voltage in the depletion or weak inversion state $U_{\mathrm{fb}} \leq U_{\mathrm{gs}} \leq U_{\mathrm{th}}$ leads to a smaller effective capacitance, i.e., $C_{\mathrm{g},2}$ in Figure 7.10. The larger derivative of the charge in the accumulation or inversion state corresponds to the capacitance $C_{\mathrm{g},1}$ below the flat-band voltage U_{fb} or the capacitance beyond the threshold voltage.

For the simple MOS channel model (8.7), a constant capacitance C_{ox} between the gate contact and the channel was assumed. The simple model assumes that all charge created in the semiconductor contributes to its conductivity (8.7). The results (8.79) or (8.81) highlight an important aspect of the calculation of the I_{d}-U_{ch} characteristic of the channel. Compared to the assumption used in (8.7), less charge contributes to the channel conductivity, as the charge is provided by the stationary doping atoms in the space-charge region. Therefore, (8.18) overestimates the current I_{d} in general [121].

8.1.4 Extended MOS channel model

In the previous section, the impact of the stationary charge Q'_{sc} on the amount of free carriers in the channel Q'_{n} was quantified, see (8.79) or (8.81). In this section, the impact on the I_{d}-U_{ch} characteristic of channel will be calculated, leading to an extended model of the MOS channel. A drain current $I_{\mathrm{d}} > 0\,\mathrm{A}$ leads to a voltage drop across the channel, increasing the voltage U_{surf} at the surface. For simplicity, the voltage $U(y)$ in the channel will be assumed to be homogeneous and equal to the surface voltage U_{surf}. This voltage drop decreases the voltage difference between the gate and the channel, thereby reducing the amount of carriers and increasing the resistance of the channel. As a result, the conductivity of the channel drops faster with increasing drain current I_{d} than predicted by the simple model (8.7).

Figure 8.17 shows the depletion layers in the geometric MOSFET model when a drain current $I_{\mathrm{d}} > 0\,\mathrm{A}$ is present. The additional voltage drop also increases the voltage between the channel and the bulk, and therefore must also be compensated by the space-charge region. The space-charge region widens, increasing the amount of immovable charge not contributing to the channel conductivity.

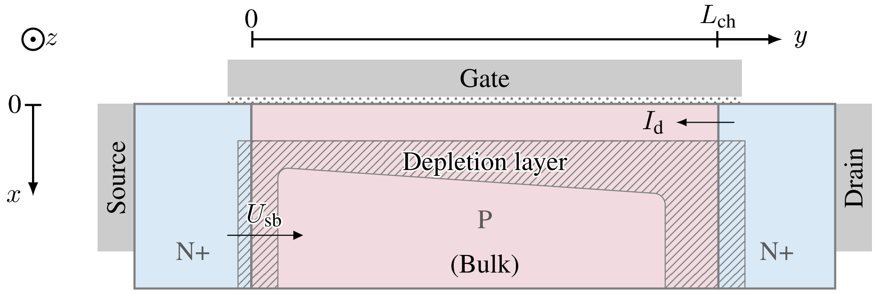


Figure 8.17: Depletion layer of a simple MOSFET model [121]; three depletion layers form, channel-to-bulk, source-to-bulk and drain-to-bulk

> **Remark:** At this point, a mapping issue needs to be addressed. In the simple MOS channel model (8.7), the source contact was used as the voltage reference. The more detailed description of the inversion layer charge Q_n (8.81) uses the bulk as reference. A (constant) built-in voltage difference U_sb between the n-doped source and the p-doped bulk exists, as their Fermi levels differ. This difference would need to be taken into account when combining models using the source and the bulk as reference. Since the models already assume a flat-band voltage of arbitrary size, the voltage difference between the source and the bulk will be modeled to be incorporated in the flat-band voltage for simplicity. Therefore, the gate-bulk voltage U_gs can be interchanged with the gate-source voltage U_gb and the difference caused by the source-bulk voltage U_sb accounted to the flat-band voltage
>
> $$U_\mathrm{gb} \mathrel{\widehat{=}} U_\mathrm{gs}, \quad \tilde{U}_\mathrm{fb} = U_\mathrm{fb} - U_\mathrm{sb}. \tag{8.82}$$

The voltage $\tilde{U}(y)$ describes the additional voltage of the channel due to the load current and the channel resistivity, referenced to the source contact. Thus, it can still be defined in the same way as in the simple MOS channel model

$$\tilde{U}(y=0) := 0, \quad \tilde{U}(y=L_\mathrm{ch}). \tag{8.83}$$

The resulting I_d-U_ch characteristic can be recalculated analogously to (8.10) to (8.18)

$$\int_0^L I_\mathrm{d} \mathrm{d}y = \int_{\tilde{U}(y=0)}^{\tilde{U}(y=L_\mathrm{ch})} -\mu_\mathrm{n} Q'_\mathrm{n}\left(\tilde{U}(y)\right) \mathrm{d}\tilde{U}, \quad \tilde{U}(y) \mathrel{\widehat{=}} U_\mathrm{surf}. \tag{8.84}$$

Substituting the charge Q_n according to (8.81) yields

$$\int_0^L I_\mathrm{d} \mathrm{d}y = \int_{\tilde{U}(y=0)}^{\tilde{U}(y=L_\mathrm{ch})} \mu_\mathrm{n} \left(C'_\mathrm{ox}\left(U_\mathrm{gs} - \tilde{U}_\mathrm{fb} - \tilde{U}(y)\right) - \sqrt{2\varepsilon_\mathrm{Si} N_\mathrm{A}^- e_0 \tilde{U}(y)} D_\mathrm{ch} \right) \mathrm{d}\tilde{U}, \tag{8.85}$$

$$\tilde{U}(y=0) := 0, \quad \tilde{U}(y=L_\mathrm{ch}) =: U_\mathrm{ch}, \quad U_\mathrm{gb} \mathrel{\widehat{=}} U_\mathrm{gs}, \tag{8.86}$$

$$\Leftrightarrow I_\mathrm{d} = \frac{\mu_\mathrm{n}}{L_\mathrm{ch}} \int_{0\,\mathrm{V}}^{U_\mathrm{ch}} \left(C'_\mathrm{ox}\left(U_\mathrm{gs} - \tilde{U}_\mathrm{fb} - \tilde{U}(y)\right) - \sqrt{2\varepsilon_\mathrm{Si} N_\mathrm{A}^- e_0 \tilde{U}(y)} D_\mathrm{ch} \right) \mathrm{d}\tilde{U}, \tag{8.87}$$

$$I_\mathrm{d} = \frac{\mu_\mathrm{n}}{L_\mathrm{ch}} \left(C'_\mathrm{ox}\left(\left(U_\mathrm{gs} - \tilde{U}_\mathrm{fb}\right) U_\mathrm{ch} - \frac{U_\mathrm{ch}^2}{2} \right) - \frac{2}{3}\sqrt{2\varepsilon_\mathrm{Si} N_\mathrm{A}^- e_0} D_\mathrm{ch} U_\mathrm{ch}^{1.5} \right). \tag{8.88}$$

The additional exponents of U_ch could be relevant when creating fit functions for experimental I-U characteristics of a channel. However, the model is already rather complex for the target application of this work. In practice, the additional terms may also be approximated by a factor $\alpha = 1.5$ in the quadratic voltage dependency [121]

$$I_\mathrm{d} = \frac{\mu_\mathrm{n} C'_\mathrm{ox}}{L_\mathrm{ch}} \left(\left(U_\mathrm{gs} - U_\mathrm{th}\right) U_\mathrm{ch} - \frac{\alpha U_\mathrm{ch}^2}{2} \right), \quad \alpha \approx 1.5 \quad [121]. \tag{8.89}$$

This new model will be added to the model function options for the channel.

> **Remark:** The core difference between the new model (8.89) and the simple model (8.18) is the increased weight α of the quadratic term. As a conse-

quence, fit models based on the simple model

$$I_{\mathrm{d}}^{*} = a_0 \left(a_1 U_{\mathrm{ch}} - \frac{U_{\mathrm{ch}}^2}{2} \right), \quad a_0, a_1 \in \mathbb{R} \tag{8.90}$$

are still valid, but the fit result for a_1 will differ from the expected value $a_1 \approx \left(U_{\mathrm{gs}} - U_{\mathrm{th}}\right)$ by a factor of $\alpha \approx 1.5$. It is important to keep this in mind when plausibility checking fit results against the threshold voltage from the datasheet and the applied gate voltage.

Remark: The steps between (8.88) and (8.89) are not elaborated in the investigated sources [68, 69, 121]. Consequently, there applicability to this work cannot be assessed in detail. The fit model comparison following in Section 8.7 will compare whether the simple MOS channel model (8.23) or the extended MOS channel model (8.90) leads to more precise on-state voltage fits. Since the term to the power of 1.5 (8.88) is eliminated in the fit model function (8.90), the comparison can only evaluate whether the introduction of the factor α in (8.89), or a_1 in (8.90), respectively, leads to more precise fits. Whether the improvement stems from the effects of the stationary charge bound in the space-charge region or another effect cannot be verified conclusively.

Remark: Equation (8.88) was determined by modeling the change in the space-charge region caused by the voltage drop $U\left(y, I_{\mathrm{d}}\right)$ along the channel. The same result can be derived using a model in which the additional voltage drop is modeled as change in the threshold voltage $U_{\mathrm{th}} := f\left(U\left(y, I_{\mathrm{d}}\right)\right)$, as a higher surface voltage $U_{\mathrm{th}}^{(\mathrm{surf})}$ is needed to initiate the formation of an inversion layer [121].

Remark: The charge concentrations use the simplification of the depletion assumption and a surface charge with zero width. Analytical solutions without these simplifications can be found in [68, 69], whereas [123] shows in detail that the solution may not be found explicitly.

8.1.4.1 Extended MOS channel model assuming a finite channel width

The extended MOS channel model described in Section 8.1.4 or by (8.88) was derived assuming that the inversion layer of the channel is infinitely thin, i.e., a Dirac delta pulse δ with regard to the x coordinate. This assumption lead to the graphs shown in Figure 8.15. Since the inversion layer charge is modeled as a Dirac delta pulse, the electric field E has a step at the location of the channel and the voltage profile U_{gb} only bends. Thus, no voltage is dropped across the channel and the space-charge region has to increase in width and charge proportional to $\sqrt{U_{\mathrm{surf}}}$, in order to compensate the potential difference between the surface of the channel and the bulk. The consequences of the zero-voltage drop across the channel are further investigated in this section.

Instead of assuming a channel with zero width, the channel will be modeled with a very small, but nonzero, width b_{n}. This allows a voltage drop to occur across the channel.

The central idea is illustrated in Figure 8.18 and may be compared to the previous model assumptions illustrated in Figure 8.15. When the applied gate voltage is increased from

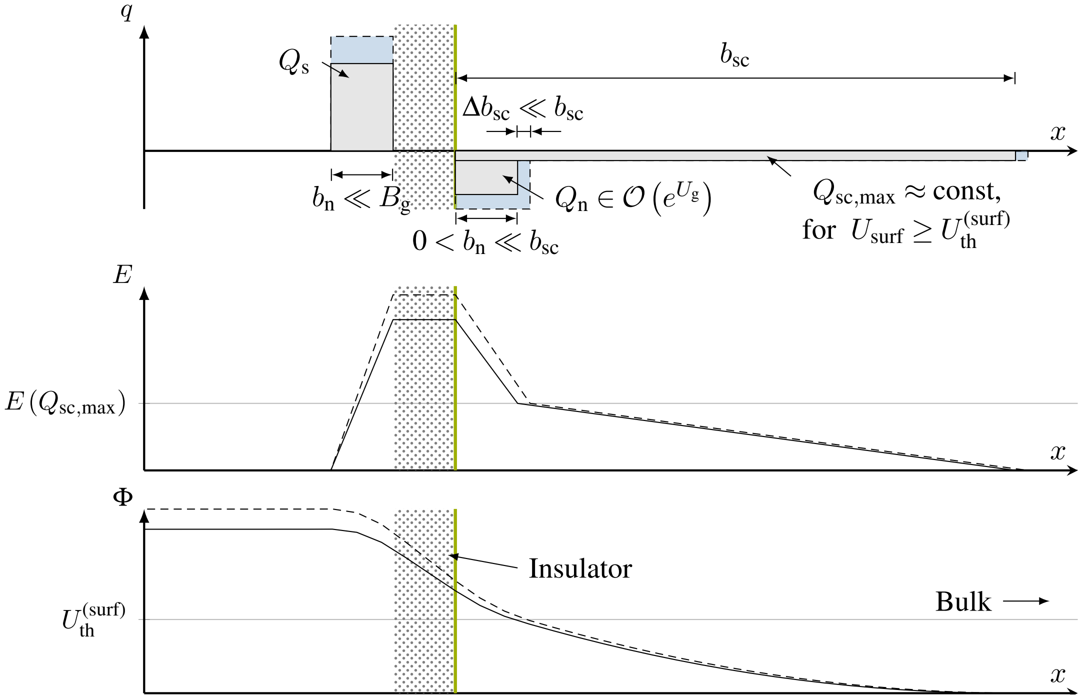


Figure 8.18: Charge components of the MOS channel assuming a finite channel width b_n instead of an infinitesimally small layer; free carrier concentration Q_n' contributes to the conductivity; space charge Q_sc' is stationary; channel width b_n not drawn to scale; the width of the inversion layer is much smaller than the space-charge region

zero, the surface voltage U_surf of the channel rises and the space-charge region increases in size according to the square-root relationship $b_\mathrm{sc} \propto \sqrt{U_\mathrm{surf}}$. Once the threshold surface voltage $U_\mathrm{th}^{(\mathrm{surf})}$ at the surface is reached, the channel begins to form. Any additional voltage increase at the surface of the semiconductor leads to a large increase of the average carrier concentration $\overline{n}_\mathrm{ch}$ in the channel and only a small increase of the channel width b_n. At the end of the channel $x = b_\mathrm{n}$, the entire additional voltage has dropped. At this location inside the semiconductor, the voltage level equals the surface threshold voltage level, due to the definition of the threshold voltage

$$U\Big|_{b_\mathrm{n}} \overset{!}{=} U_\mathrm{th}^{(\mathrm{surf})}. \tag{8.91}$$

The width of the space-charge region b_sc increases by the same amount as the channel width b_n. Thus, its relative change is neglectable. Furthermore, the change in space charge Q_sc' is also be neglectable, i.e., it would be constant for $U_\mathrm{gs} > U_\mathrm{th}$. Considering the new assumptions of the nonzero width of the channel, this results in a different relationship between the surface voltage and the concentration of free carriers of the inversion layer Q_n' and the resulting I_d-U_ch relationship, compared to the model assuming an infinitely small inversion layer that cannot cause a voltage drop.

Model calculations The resulting I_d-U_ch relationship will be quantified in this paragraph. The assumptions are

1. The channel width b_n is much smaller than the width of the space-charge region b_sc,

but is finite

$$0 < b_\mathrm{n} \ll b_\mathrm{sc}. \tag{8.92}$$

2. The charge in the channel is still assumed to be homogeneously distributed with an average electron concentration of $\overline{n}_\mathrm{ch}$. The size of $\overline{n}_\mathrm{ch}$ depends on how far the surface voltage U_surf is increased above the threshold voltage at the surface as well as the specific charge profile in the channel. For this modeling approach, the average electron concentration is only estimated to be smaller than the electron concentration at the surface $n^{(\mathrm{surf})}$ and larger than the concentration of the (ionized) doping atoms N_A^-

$$N_\mathrm{A}^- < \overline{n}_\mathrm{ch} < n^{(\mathrm{surf})} = \frac{n_\mathrm{i}^2}{N_\mathrm{A}^-}\mathrm{e}^{\frac{U_\mathrm{surf}-U_\mathrm{fb}}{U_\mathrm{T}}}, \tag{8.93}$$

$$Q'_\mathrm{n} = \overline{n}_\mathrm{ch} b_\mathrm{n} D_\mathrm{ch}. \tag{8.94}$$

Using these assumptions, the electric field profile can be recalculated analogously to (8.55). The electric field depends on the homogeneously distributed charges N_A^- and $\overline{n}_\mathrm{ch}$

$$E(x) = -\int_\infty^x -\frac{q}{\varepsilon}\mathrm{d}\tilde{x}, \quad 0 \le x \le b_\mathrm{sc}, E(b_\mathrm{sc}) = 0, \tag{8.95}$$

$$= \begin{cases} 0\frac{\mathrm{V}}{\mathrm{m}}, & b_\mathrm{sc} \le x, \\ \int_{b_\mathrm{sc}}^x \frac{-N_\mathrm{A}^- e_0}{\varepsilon_\mathrm{Si}}\mathrm{d}\tilde{x}, & b_\mathrm{n} \le x < b_\mathrm{sc}, \\ \int_{b_\mathrm{sc}}^x \frac{-N_\mathrm{A}^- e_0}{\varepsilon_\mathrm{Si}}\mathrm{d}\tilde{x} + \int_{b_\mathrm{n}}^x \frac{-\overline{n}_\mathrm{ch} e_0}{\varepsilon_\mathrm{Si}}\mathrm{d}\tilde{x}, & 0\,\mathrm{m} \le x < b_\mathrm{n}, \end{cases} \tag{8.96}$$

$$E(x) = \begin{cases} 0\frac{\mathrm{V}}{\mathrm{m}}, & b_\mathrm{sc} \le x, \\ \frac{-N_\mathrm{A}^- e_0}{\varepsilon_\mathrm{Si}}(x - b_\mathrm{sc}), & b_\mathrm{n} \le x < b_\mathrm{sc}, \\ \frac{-N_\mathrm{A}^- e_0}{\varepsilon_\mathrm{Si}}(x - b_\mathrm{sc}) + \frac{-\overline{n}_\mathrm{ch} e_0}{\varepsilon_\mathrm{Si}}(x - b_\mathrm{n}), & 0\,\mathrm{m} \le x < b_\mathrm{n}. \end{cases} \tag{8.97}$$

The latter two cases shown here correspond to the linear slopes of the electric field in the semiconductor, as shown in Figure 8.18. The calculations assume that the (ionized) doping atoms N_A^- are also present in the channel. The electric field at the surface of the semiconductor is

$$E\big|_{x=0} = \frac{N_\mathrm{A}^- e_0}{\varepsilon_\mathrm{Si}} b_\mathrm{sc} + \frac{\overline{n}_\mathrm{ch} e_0}{\varepsilon_\mathrm{Si}} b_\mathrm{n} \tag{8.98}$$

$$= \frac{-Q'_\mathrm{sc}}{\varepsilon_\mathrm{Si} D_\mathrm{ch}} + \frac{-Q_\mathrm{n}}{\varepsilon_\mathrm{Si} D_\mathrm{ch}}. \tag{8.99}$$

Integrating the electric field yields the surface voltage

$$U_{\mathrm{surf}} = -\int_{b_{\mathrm{sc}}}^{0} E \mathrm{d}x \tag{8.100}$$

$$\begin{aligned} &= -\int_{b_{\mathrm{sc}}}^{b_{\mathrm{n}}} \frac{-N_{\mathrm{A}}^{-} e_0}{\varepsilon_{\mathrm{Si}}} (x - b_{\mathrm{sc}}) \, \mathrm{d}x - \int_{b_{\mathrm{n}}}^{0} \frac{-N_{\mathrm{A}}^{-} e_0}{\varepsilon_{\mathrm{Si}}} (x - b_{\mathrm{sc}}) \, \mathrm{d}x \\ &\quad - \int_{b_{\mathrm{n}}}^{0} \frac{-\overline{n}_{\mathrm{ch}} e_0}{\varepsilon_{\mathrm{Si}}} (x - b_{\mathrm{n}}) \, \mathrm{d}x \end{aligned} \tag{8.101}$$

$$= -\int_{b_{\mathrm{sc}}}^{0} \frac{-N_{\mathrm{A}}^{-} e_0}{\varepsilon_{\mathrm{Si}}} (x - b_{\mathrm{sc}}) \, \mathrm{d}x - \int_{b_{\mathrm{n}}}^{0} \frac{-\overline{n}_{\mathrm{ch}} e_0}{\varepsilon_{\mathrm{Si}}} (x - b_{\mathrm{n}}) \, \mathrm{d}x \tag{8.102}$$

$$= -\left[\frac{-N_{\mathrm{A}}^{-} e_0}{\varepsilon_{\mathrm{Si}}} \left(\frac{x^2}{2} - b_{\mathrm{sc}} x \right) \right]_{b_{\mathrm{sc}}}^{0} - \left[\frac{-\overline{n}_{\mathrm{ch}} e_0}{\varepsilon_{\mathrm{Si}}} \left(\frac{x^2}{2} - b_{\mathrm{n}} x \right) \right]_{b_{\mathrm{n}}}^{0} \tag{8.103}$$

$$= \frac{N_{\mathrm{A}}^{-} e_0}{\varepsilon_{\mathrm{Si}}} \frac{b_{\mathrm{sc}}^2}{2} + \frac{\overline{n}_{\mathrm{ch}} e_0}{\varepsilon_{\mathrm{Si}}} \frac{b_{\mathrm{n}}^2}{2}. \tag{8.104}$$

As mentioned at the beginning of this section, the central idea of the model with a nonzero channel width is that the width of the space-charge region only increases by the width of the channel b_{n}. A reference width $B_{\mathrm{sc,th}}$ of the space-charge region is defined as its width when the threshold voltage is applied, i.e., when the inversion layer begins to form, i.e., $b_{\mathrm{n}} = 0$,

$$B_{\mathrm{sc,th}} := b_{\mathrm{sc}} \big(U_{\mathrm{gs}} = U_{\mathrm{th}} \big) , \tag{8.105}$$

$$b_{\mathrm{sc}} = B_{\mathrm{sc,th}} + b_{\mathrm{n}}, \quad b_{\mathrm{n}} \ll B_{\mathrm{sc,th}}. \tag{8.106}$$

Substituting (8.106) in (8.109) yields

$$U_{\mathrm{surf}} = \frac{N_{\mathrm{A}}^{-} e_0}{\varepsilon_{\mathrm{Si}}} \frac{\big(B_{\mathrm{sc,th}} + b_{\mathrm{n}} \big)^2}{2} + \frac{\overline{n}_{\mathrm{ch}} e_0}{\varepsilon_{\mathrm{Si}}} \frac{b_{\mathrm{n}}^2}{2}, \quad N_{\mathrm{A}}^{-} \ll \overline{n}_{\mathrm{ch}}, b_{\mathrm{n}} \ll B_{\mathrm{sc,th}} \tag{8.107}$$

$$\approx \frac{N_{\mathrm{A}}^{-} e_0}{\varepsilon_{\mathrm{Si}}} \frac{B_{\mathrm{sc,th}}^2}{2} + \frac{\overline{n}_{\mathrm{ch}} e_0}{\varepsilon_{\mathrm{Si}}} \frac{b_{\mathrm{n}}^2}{2} \tag{8.108}$$

$$\Leftrightarrow U_{\mathrm{surf}} = \underbrace{-Q'_{\mathrm{sc,max}} \frac{B_{\mathrm{sc,th}}}{2 \varepsilon_{\mathrm{Si}} D_{\mathrm{ch}}}}_{\text{independent of } U_{\mathrm{gs}} \text{ for } U_{\mathrm{gs}} > U_{\mathrm{th}}, \text{ assuming } 0 < b_{\mathrm{n}} \ll b_{\mathrm{sc}}} - Q'_{\mathrm{n}} \frac{b_{\mathrm{n}}}{2 \varepsilon_{\mathrm{Si}} D_{\mathrm{ch}}}. \tag{8.109}$$

In contrast to the extended MOS channel model of the previous section, Section 8.1.4, the charge bound in the space-charge region is constant, which will affect the I_{d}-U_{ch} relationship. In order to quantify this effect, the relationship between the externally applied gate voltage U_{gs} and the free carrier charge in the inversion layer Q'_{n} is determined in the same way as in (8.74)

$$U_{\mathrm{gb}} - U_{\mathrm{fb}} = -\int_{\infty}^{-\infty} E \mathrm{d}x \tag{8.110}$$

$$= -\int_{b_{\mathrm{sc}}}^{0} E(x) \, \mathrm{d}x - \int_{0}^{-B_{\mathrm{ins}}} E_{\mathrm{ox}} \mathrm{d}x \tag{8.111}$$

$$= U_{\mathrm{surf}} + E_{\mathrm{ox}} B_{\mathrm{ins}}, \quad E_{\mathrm{ox}} = \frac{\varepsilon_{\mathrm{Si}}}{\varepsilon_{\mathrm{ox}}} E\big|_{x=0} \tag{8.112}$$

$$= U_{\mathrm{surf}} + B_{\mathrm{ins}} \left(\frac{-Q'_{\mathrm{sc,max}}}{\varepsilon_{\mathrm{Si}} D_{\mathrm{ch}}} + \frac{-Q'_{\mathrm{n}}}{\varepsilon_{\mathrm{Si}} D_{\mathrm{ch}}} \right) \frac{\varepsilon_{\mathrm{Si}}}{\varepsilon_{\mathrm{ox}}} \tag{8.113}$$

$$= U_{\mathrm{surf}} + \frac{B_{\mathrm{ins}}}{\varepsilon_{\mathrm{ox}} D_{\mathrm{ch}}} \left(-Q'_{\mathrm{sc,max}} - Q'_{\mathrm{n}} \right). \tag{8.114}$$

For reference, this can also be expressed only by charges

$$U_{\mathrm{gb}} - U_{\mathrm{fb}} = -Q'_{\mathrm{sc,max}} \frac{B_{\mathrm{sc,th}}}{2\varepsilon_{\mathrm{Si}} D_{\mathrm{ch}}} - Q'_{\mathrm{n}} \frac{b_{\mathrm{n}}}{2\varepsilon_{\mathrm{Si}} D_{\mathrm{ch}}} + B_{\mathrm{ins}} \left(\frac{-Q'_{\mathrm{sc,max}}}{\varepsilon_{\mathrm{Si}} D_{\mathrm{ch}}} + \frac{-Q'_{\mathrm{n}}}{\varepsilon_{\mathrm{Si}} D_{\mathrm{ch}}} \right) \frac{\varepsilon_{\mathrm{Si}}}{\varepsilon_{\mathrm{ox}}} \tag{8.115}$$

$$= -Q'_{\mathrm{sc,max}} \left(\frac{B_{\mathrm{sc,th}}}{2\varepsilon_{\mathrm{Si}} D_{\mathrm{ch}}} + \frac{B_{\mathrm{ins}}}{\varepsilon_{\mathrm{ox}} D_{\mathrm{ch}}} \right) - Q'_{\mathrm{n}} \left(\frac{b_{\mathrm{n}}}{2\varepsilon_{\mathrm{Si}} D_{\mathrm{ch}}} + \frac{B_{\mathrm{ins}}}{\varepsilon_{\mathrm{ox}} D_{\mathrm{ch}}} \right). \tag{8.116}$$

Equation (8.116) can be solved for the free carrier charge in the inversion layer Q'_{n}

$$Q'_{\mathrm{n}} = -\left(U_{\mathrm{gb}} - U_{\mathrm{fb}} - U_{\mathrm{surf}} \right) \frac{\varepsilon_{\mathrm{ox}} D_{\mathrm{ch}}}{B_{\mathrm{ins}}} + Q'_{\mathrm{sc,max}}, \quad Q'_{\mathrm{n}}, Q'_{\mathrm{sc,max}} < 0 \tag{8.117}$$

$$= -C'_{\mathrm{ox}} \left(U_{\mathrm{gb}} - U_{\mathrm{fb}} - U_{\mathrm{surf}} \right) + \underbrace{Q'_{\mathrm{sc,max}}}_{\text{Constant instead of } \propto -\sqrt{U_{\mathrm{surf}}} \text{ in (8.81)}}. \tag{8.118}$$

In the MOS channel model that assumes an infinitely small channel width, the charge Q'_{sc} depends on the surface voltage, while this model predicts a constant charge that is independent of the voltage, once the threshold voltage is reached. The fact that only a constant charge $Q'_{\mathrm{sc,max}}$ does not contribute to the conductivity of the channel is the key difference of this modeling approach compared to (8.81).

Resulting I_{d}-U_{ch} relationship and fit model function The I_{d}-U_{ch} relationship can be determined analogously to (8.88) using (8.118), which yields

$$I_{\mathrm{d}} = \frac{\mu_{\mathrm{n}}}{L_{\mathrm{ch}}} \int_{0\,\mathrm{V}}^{U_{\mathrm{ch}}} \left(C'_{\mathrm{ox}} \left(U_{\mathrm{gs}} - U_{\mathrm{fb}} - \tilde{U}(y) \right) + Q'_{\mathrm{sc,max}} \right) \mathrm{d}\tilde{U}, \quad Q'_{\mathrm{sc,max}} < 0 \tag{8.119}$$

$$= \frac{\mu_{\mathrm{n}}}{L_{\mathrm{ch}}} \left(C'_{\mathrm{ox}} \left(\left(U_{\mathrm{gs}} - U_{\mathrm{fb}} \right) U_{\mathrm{ch}} - \frac{U_{\mathrm{ch}}^2}{2} \right) + Q'_{\mathrm{sc,max}} U_{\mathrm{ch}} \right), \tag{8.120}$$

$$= \frac{\mu_{\mathrm{n}} C'_{\mathrm{ox}}}{L_{\mathrm{ch}}} \left(\left(U_{\mathrm{gs}} \underbrace{- U_{\mathrm{fb}} - \frac{Q'_{\mathrm{sc,max}}}{C'_{\mathrm{ox}}}}_{\widehat{=}\, -U_{\mathrm{th}}} \right) U_{\mathrm{ch}} - \frac{U_{\mathrm{ch}}^2}{2} \right). \tag{8.121}$$

The resulting I_{d}-U_{ch} relationship is similar to the one in the simple MOS channel model shown in (8.18), as the fixed charge is already accounted for in the threshold voltage. The resulting fit model function is identical

$$I_{\mathrm{d}}^* = a_0 \left(a_1 U_{\mathrm{ch}} - \frac{U_{\mathrm{ch}}^2}{2} \right), \quad a_0, a_1 \in \mathbb{R}. \tag{8.122}$$

8.1.4.2 Conclusion to the extended MOS channel models

Three distinct models of the MOS channel have been presented.

1. The simple MOS channel model (8.18), which assumes all charge in the semiconductor, generated by the gate voltage, contributes to the channel conductivity,

$$I_\mathrm{d} = \frac{\mu_\mathrm{n} C'_\mathrm{ox}}{L_\mathrm{ch}} \left(\left(U_\mathrm{gs} - U_\mathrm{th}\right) U_\mathrm{ch} - \frac{U_\mathrm{ch}^2}{2} \right).$$

2. An extended MOS channel model, assuming an infinitesimally small inversion layer. In this model, the voltage drop in the channel caused by the load current I_d leads to an increasing amount of charge bound in the space-charge region, which does not contribute to the channel conductivity. As a result, the channel conductivity drops faster than predicted by the simple model if a drain current is present (8.88),

$$I_\mathrm{d} = \frac{\mu_\mathrm{n} C'_\mathrm{ox}}{L_\mathrm{ch}} \left(\left(U_\mathrm{gs} - U_\mathrm{th}\right) U_\mathrm{ch} - \frac{\alpha U_\mathrm{ch}^2}{2} \right), \quad \alpha \approx 1.5.$$

3. The extended MOS channel model was adapted by assuming a small but finite channel width b_n. This changes the results of the extended MOS channel model in such a way that the charge bound in the space-charge region is constant and independent of the voltage drop caused by the load current. The resulting I_d-U_ch relationship (8.121) matches the simple model in structure,

$$I_\mathrm{d} = \frac{\mu_\mathrm{n} C'_\mathrm{ox}}{L_\mathrm{ch}} \left(\left(U_\mathrm{gs} \underbrace{- U_\mathrm{fb} - \frac{Q'_\mathrm{sc,max}}{C'_\mathrm{ox}}}_{\widehat{=}\, -U_\mathrm{th}} \right) U_\mathrm{ch} - \frac{U_\mathrm{ch}^2}{2} \right).$$

The main difference between the two extended MOS models is due to the different assumptions of the charge distribution in the MOS channel. Figure 8.19 illustrates the resulting electric field and voltage profile in a MOS channel for different charge profile curvatures. The overall charge in the channel is kept equal for all cases. The blue dashed line corresponds to the MOS channel model with a finite width and homogenous charge distribution. Although this assumption is valid for a space-charge region where the charge distribution is defined by the doping concentration, the assumption is less applicable to thin layers in accumulation or strong inversion. The red dashed line corresponds to the MOS channel model based on the Dirac delta pulse assumption. The bottom graph shows the resulting voltage profiles. The overall voltage drop across the channel corresponds to the voltage at $x = 0$, which marks the semiconductor surface. The diagram shows that a higher curvature leads to a lower voltage drop across the channel. Which of the two extended MOS models provides better results depends on the curvature of the charge distribution in the channel of the MOSFET device under test. Considering Boltzmann's relationship, a high curvature is expected.

The final comparison of the models will be done by evaluating their fit accuracy using several measured power module units in Section 8.7. In the comparison, only the simple MOS channel model and the extended MOS channel model with the infinitesimal small channel width will be compared, as the model assuming the finite channel width is structural identical to the simple MOS channel model.

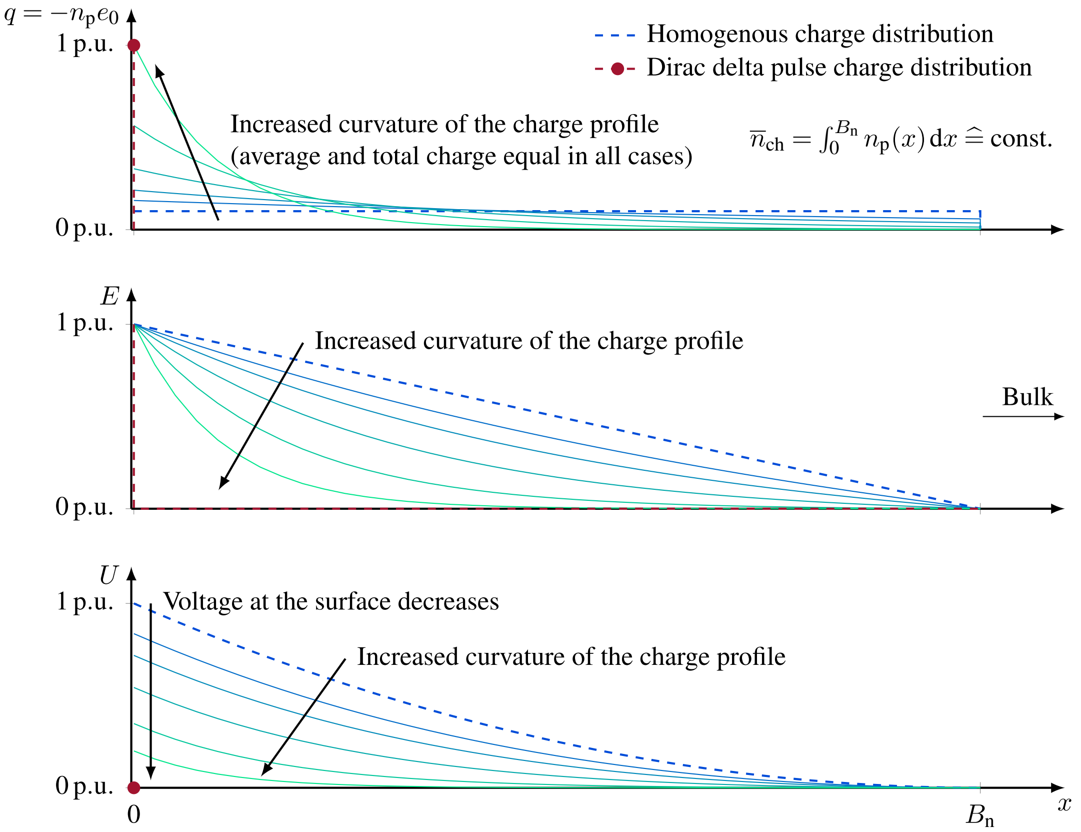


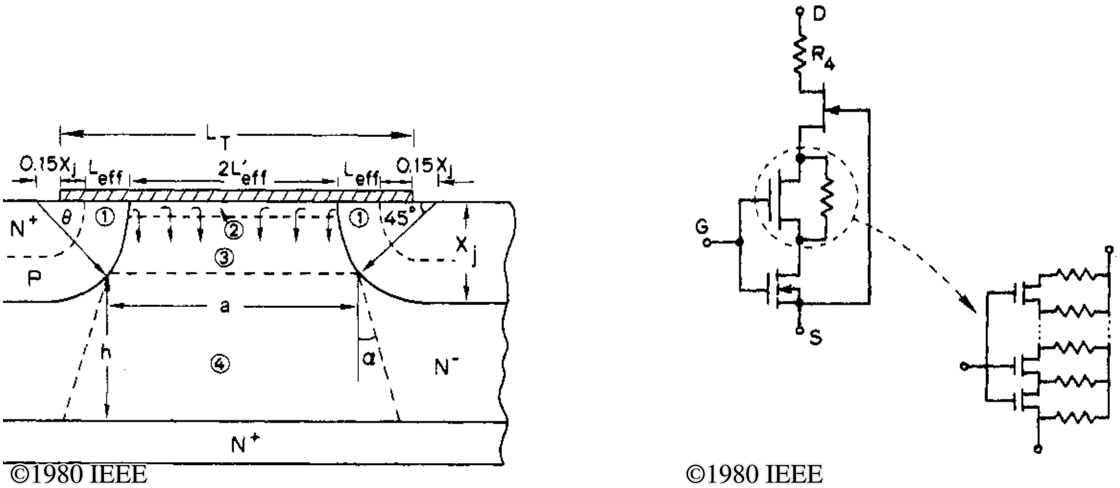
Figure 8.19: Illustration of the resulting electric field and voltage profile in a MOSFET channel depending on the charge profile curvature; average electron concentration of $\overline{n}_\mathrm{ch}$ and total charge Q'_n equal for all cases; arbitrary exponential functions chosen as examples, as the solution cannot be determined explicitly [123]

Deliberately neglected effects At high field strengths in the channel, the carrier mobility can saturate. This leads to the saturation of the transconductance [108]. According to [116], field-dependent channel mobility and concentration-dependent mobility play a minor role in high-voltage devices. As we can see in the datasheet [124], this effect does not seem to occur in the gate voltage regions relevant to this work.

8.2 Accumulation region

Figure 8.20 shows a current flow model and a circuit model of a D-MOSFET. The arrows shown in Figure 8.20a describe the electron flow. An electron flow starts at the source and passes through the channel, see Marker 1. The channel is formed in a p-doped region. Thus, the electron layer is referred to as an inversion layer. The gate electrode expands further than the channel and overlaps with the n-doped drain region of the MOSFET. The electron current leaves the channel and enters the drain region, see Marker 2. Since the region is already n-doped, the name of the electron layer changes to accumulation layer or region. Marker 3 marks the JFET region, which will be discussed in the next section.

The curvature of the arrows in Figure 8.20a, Marker 2, show that the current flow changes its direction in the accumulation region. Simply put, a portion of the electron current "immediately" flows downwards and is unaffected by the accumulation region, while other



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(a) Current flow

(b) Circuit model

Figure 8.20: Modeling the accumulation region as a parallel depletion-mode MOSFET at Marker (2) [108]

parts expand horizontally before flowing downwards. Of course, this process is gradual and in accordance with the electric field.

In [108], the accumulation region of a D-MOSFET is described as a depletion-type MOSFET, since the electron current runs through an n-doped region, parallel to the gate electrode. Figure 8.20b shows the circuit modeling approach using a depletion type MOSFET that is composed of an infinite number of infinitesimally small depletion type MOSFETs. The partitioning can be used to describe that the current gradually leaves the accumulation region in vertical direction while flowing horizontally. In practice, the accumulation region is modeled by assuming the entire current flows through the entire accumulation region, i.e., to the center of the region marked by Marker 2 in Figure 8.20a. Afterwards, the resulting accumulation region resistance of voltage drop is weighted with a factor between zero and one [68]. The concept will be elaborated using a trench MOSFET structure.

Figure 8.21 shows the structure of a trench MOSFET. The two edge cases of the current flow through the accumulation region are indicated by dashed lines.

According to [68], the resistance of the accumulation zone of a trench MOSFET can be modeled by two components. The first component describes the vertical current flow along the gate insulator between the bottom of the p-base and the bottom of the trench, see Figure 8.21. The second component describes the horizontal spreading of the current when it enters the drift region[7] [68]

$$R_\mathrm{A} = K_\mathrm{A} \frac{L_\mathrm{A,max}}{B_\mathrm{ch}\mu_\mathrm{n}C_\mathrm{ox}\left(U_\mathrm{gs} - U_\mathrm{th}^*\right)}, \quad L_\mathrm{A,max} = t_\mathrm{T} - x_\mathrm{JP} + \frac{W_\mathrm{T}}{2}, \tag{8.123}$$

$$0 \leq K_\mathrm{A} < 1. \tag{8.124}$$

The parameters are defined in Figure 8.21. This formula does not yet include the voltage drop U_ch caused by the drain current I_d and is therefore only valid for very low currents. The used threshold voltage U_th^* is not the same as the threshold voltage U_th of the channel, as it

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[7] The trench MOSFET shown does not have a JFET region.

describes the modeled depletion type MOSFET of the accumulation region. The coefficient K_{A} describes how the current spreads horizontally when entering the drift zone [108]. A coefficient of $K_{\mathrm{A}} = 0$ means that the current spreads away from the gate as soon as the current leaves the channel the end of the channel, while a coefficient of $K_{\mathrm{A}} = 1$ would correspond to the current flowing closely along the gate contact until it reachs the middle below the contact. The latter case is an edge case that is not reached. The coefficient can be determined by simulation and may be assumed to be $K_{\mathrm{A}} = 0.6$ for a trench MOSFET [68], while $K_{\mathrm{A}} = 0.3$ is suggested for a D-MOSFET [108].

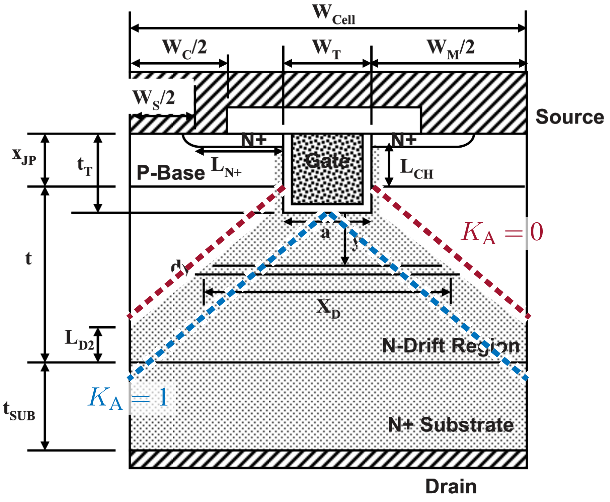

Figure 8.21: Simplified current flow model [68][8]; the red and blue dashed lines were added by the author

If one considers the voltage drop U_{ch} already caused by the channel resistance, (8.123) can be extended to

$$R_{\mathrm{A}} = K_{\mathrm{A}} \frac{L_{\mathrm{A,max}}}{B_{\mathrm{ch}} \mu_{\mathrm{n}} C_{\mathrm{ox}} \left(U_{\mathrm{gs}} - U_{\mathrm{th}}^{*} - U_{\mathrm{ch}} \right)}. \tag{8.125}$$

It can be seen that the resistance of the accumulation region R_{A} matches the behavior of the MOS channel (8.9). Therefore, the U_{a}-I_{d} characteristic of the accumulation region can be determined analogous to (8.18)

$$I_{\mathrm{d}} = K_{\mathrm{A}} \frac{B_{\mathrm{ch}} \mu_{\mathrm{n}} C_{\mathrm{ox}}}{L_{\mathrm{A,max}}} \left(\left(U_{\mathrm{gs}} - U_{\mathrm{th}}^{*} - U_{\mathrm{ch}} \right) U_{\mathrm{a}} - \frac{U_{\mathrm{a}}^{2}}{2} \right). \tag{8.126}$$

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8.3 JFET region

The JFET region of a D-MOSFET can be described using Figure 8.20a, Marker (3). The p-base shape is assumed to be circular, leading to a resistance of

$$R_{\text{JFET}} = \frac{2}{\mu_\text{n} N_\text{D}^+ e_0} \underbrace{\frac{1}{B_\text{ch}} \left(\frac{1}{\sqrt{1-\left(2X_\text{j}/L_\text{eff}\right)^2}} \tan^{-1}(0.414) \sqrt{\frac{L_\text{eff}+2X_\text{j}/L_\text{eff}}{L_\text{eff}-2X_\text{j}/L_\text{eff}}} - \frac{\pi}{8} \right)}_{\text{depends on the geometry only}} \quad [108]. \tag{8.127}$$

This description assumes that the drain current is zero. The required geometric parameters of the equation are defined in Figure 8.20a. Equation (8.127) is determined by defining the end of the JFET region at $\theta = 45°$ in Figure 8.20a.

The solution presented (8.127) does not include any shrinking of the JFET region due to the vertical voltage drop $U(y)$ caused by the drain current [110]. Assuming that the width of the channel B_geo changes with y, the overall voltage drop could be calculated analogous to that of the MOS channel (8.18).

$$\mathrm{d}R_{\text{JFET}} = \frac{\mathrm{d}y}{B_\text{ch}\mu_\text{n} N_\text{D}^+ e_0 \left(B_\text{geo}(y) - 2b_\text{sc}(U(y))\right)}, \quad \mathrm{d}U = I_\text{d}\mathrm{d}R, \tag{8.128}$$

$$b_\text{sc} = \sqrt{\frac{2\varepsilon_\text{Si}}{e_0 N_\text{D}^+}\left(U(y) - U_\text{g} + \frac{kT}{e_0}\ln\left(\frac{N_\text{D}^+}{n_i}\right)\right)}, \tag{8.129}$$

$$I_\text{d}\text{dy} = B_\text{ch}\mu_\text{n} N_\text{D}^+ e_0 \Big(\underbrace{B_\text{geo}(y)\,\mathrm{d}U}_{\text{mixed term}} - 2b_\text{sc}(U(y))\,\mathrm{d}U\Big). \tag{8.130}$$

The channel is assumed to be symmetrical. The width of the space-charge region b_sc is subtracted from the total available channel width B_geo on both sides. Equation (8.130) cannot be solved trivially without knowledge of the geometry, as the location-dependent and voltage-dependent terms cannot be separated. Due to the mixed term, any exponents of the load current could occur in the voltage drop across the JFET region, depending on the specific geometry.

If the width of the channel is constant, i.e., $B_\text{geo}(y) = B_\text{jfet}$, a solution for the U_jfet-I_d characteristic can be found in [69, 110]

$$I_\text{d} = I_0 \left(3\frac{U_\text{jfet}}{U_\text{po}} - 2\frac{\left(U_\text{jfet} + U_\text{base} - \frac{kT}{e_0}\ln\left(\frac{N_\text{D}^+}{n_i}\right)\right)^{\frac{3}{2}} - \left(U_\text{base} + \frac{kT}{e_0}\ln\left(\frac{N_\text{D}^+}{n_i}\right)\right)^{\frac{3}{2}}}{U_\text{po}^{\frac{3}{2}}} \right), \tag{8.131}$$

$$I_0 = \frac{\mu_\text{n} e_0^2 \left(N_\text{D}^+\right)^2 B_\text{jfet}^3 B_\text{ch}}{6\varepsilon_\text{Si} L_\text{jfet}}, \quad U_\text{po} = \frac{e_0 N_\text{D}^+ B_\text{jfet}^2}{2\varepsilon_\text{Si}}. \tag{8.132}$$

The length of the JFET region is L_jfet. The voltage U_base at the top of the JFET region can be used to include already existing voltage increases with regard to the source potential, i.e., the voltage drop across the channel and the accumulation region $U_\text{base} = U_\text{ch} + U_\text{a}$. These voltage drops can be interpreted as a negative voltage bias on the JFET gate. Equation (8.131) is valid up to the pinch-off voltage U_{po} of the channel.

It must be kept in mind that the terms occurring in (8.131) will be different if the width of the JFET region B_{jfet} changes, i.e., if the p-base has a circular shape, as shown in Figure 8.20a. In an ideal trench MOSFET, no JFET region would be expected, see Figure 8.2a. However, the manufacturer employs highly doped p-base regions below the bottom of the trench to reduce the voltage stress [118, 119], see Figure 8.3. Therefore, a JFET contribution is expected in the I-U characteristic.

8.4 Drift region

The drift region shown in Figure 8.21 is split into two parts. In the first part R_{D1}, the expansion of the current flow is assumed to follow a fixed 45° shape until it encounters the boundaries of the cell [68]. It is assumed that the drift region is thick enough that the horizontal cell boundaries are always reached. The second part R_{D2} describes a simple uniform current flow through the remaining drift region according to [68, 108]

$$R_{\text{D1}} = \frac{1}{\mu_{\text{n}} N_{\text{D}}^{+} e_0 2 B_{\text{ch}}} \ln\left(\frac{W_{\text{T}} + W_{\text{M}}}{W_{\text{T}}}\right) \tag{8.133}$$

$$R_{\text{D2}} = \frac{1}{\mu_{\text{n}} N_{\text{D}}^{+} e_0 B_{\text{ch}}} L_{\text{D2}}, \quad L_{\text{D2}} = t + x_{\text{JP}} - t_{\text{T}} - \frac{W_{\text{M}}}{2} \tag{8.134}$$

$$\begin{aligned} R_{\text{D}} &= R_{\text{D1}} + R_{\text{D2}} && (8.135) \\ &= \frac{1}{\mu_{\text{n}} N_{\text{D}}^{+} e_0} \underbrace{\frac{1}{B_{\text{ch}}} \left(\frac{1}{2} \ln\left(\frac{W_{\text{T}} + W_{\text{M}}}{W_{\text{T}}}\right) + L_{\text{D2}}\right)}_{\text{depends on the geometry only}}. && (8.136) \end{aligned}$$

In the context of this work, (8.136) shows that the resistance of the drift region or epitaxial layer can be interpreted as the resistance of a simple, doped semiconductor, depending on geometry, doping N_{D}^{+} and mobility μ_{n} only.

In this section, different regions of a generic trench MOSFET structure were described. Model fitting functions of the resistance or the voltage drop of each region were provided. They are mostly based on simple geometry, applied voltages and fundamental semiconductor properties. In the context of this work, only the structure of the terms (linear, quadratic, ...) of the region's model fitting functions are needed.

8.5 Semiconductor properties

In this section, the semiconductor properties required to model the behavior of an SiC MOSFET will be summarized. Special consideration is given to the temperature dependency of each property, in order to develop temperature-dependent fit models. Detailed discussions of the resulting differences between silicon and silicon carbide devices can be found in [68, 69].

Table 8.3 shows the fundamental properties of silicon and the most common type of silicon carbide in power semiconductors, 4H-SiC [68]. Generally, 4H-SiC has a better mobility than 6H-SiC with less anisotropy [69]. The intrinsic carrier concentration n_{i} in 4H-SiC is below that of Si by several orders of magnitude. While the intrinsic carrier concentration

Table 8.3: Fundamental material properties [68]

	Variable	Unit	Silicon	4H-SiC
Energy bandgap	E_G	eV	1.11	3.26
Critical electric field [69]	E_crit	$\frac{\mathrm{MV}}{\mathrm{cm}}$	0.3	2.8
Relative dielectric constant	ε_r		11.7	9.7
Vacuum permittivity	ε_0	$\frac{\mathrm{A \cdot s \cdot m}}{\mathrm{V}}$	$8.85 \cdot 10^{-12}$	
Thermal conductivity	λ	$\frac{\mathrm{W}}{\mathrm{cm \cdot K}}$	1.5	3.7
Electron affinity		eV	4.05	3.7
Density of states, conduction band	N_C	$\frac{1}{\mathrm{cm}^3}$	$2.8 \cdot 10^{19}$	$1.23 \cdot 10^{19}$
Density of states, valence band	N_V	$\frac{1}{\mathrm{cm}^3}$	$1.04 \cdot 10^{19}$	$4.58 \cdot 10^{18}$
Intrinsic carrier concentration [68] (at room temperature)	n_i	$\frac{1}{\mathrm{cm}^3}$	$1.4 \cdot 10^{10}$	$6.7 \cdot 10^{-11}$

in Si can reach that of typical doping levels[9] at a temperature of approximately 267 °C, in 4H-SiC this occurs at temperatures higher than 700 °C [68, 69]. Thus, SiC devices can be operated at much higher temperatures, although current packaging technologies are the limiting factor in practical applications today [69].

In the context of device modeling, the most important factors are the electron mobility μ_n and the concentrations of the *ionized* doping atoms N_D^+ and N_A^-. The following paragraphs will provide a short summary of the different material properties and their behavior with regard to temperature and other factors. At the end of this section, these properties will be summarized in Table 8.4 along with their temperature models.

Intrinsic carrier concentration The intrinsic carrier concentration n_i depends on the density of states in the conduction band N_C, the density of states in the valence band N_V and the size of the bandgap E_G [68]

$$n_\mathrm{i} = \sqrt{N_\mathrm{C} N_\mathrm{V}} \mathrm{e}^{-\frac{E_\mathrm{G}}{2k\vartheta}}. \tag{8.137}$$

It can be modeled by [68]

$$n_\mathrm{i}^* = a_0 \vartheta^{\frac{3}{2}} \mathrm{e}^{-\frac{a_1}{\vartheta}}, \quad a_0, a_1 > 0, \tag{8.138}$$

$$\frac{\mathrm{d}n_\mathrm{i}^*}{\mathrm{d}\vartheta} = \frac{a_0 \mathrm{e}^{\frac{-a1}{\vartheta}} \left(a_1 + 1.5\vartheta\right)}{\sqrt{\frac{\vartheta}{1\mathrm{K}}}} > 0. \tag{8.139}$$

The intrinsic carrier concentration increases with temperature [68]. The intrinsic carrier concentration in silicon exceeds the concentration for medium doping levels[10] at 267 °C, while the intrinsic carrier concentration in 4H-SiC is several orders of magnitude below

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[9] $10 \cdot 10^{15} \frac{1}{\mathrm{cm}}$

this [68].

Built-in potential The built-in potential of a p-N junction U_bi is a core aspect of bipolar devices. Even though the MOSFET is a unipolar device, its body diode is a bipolar device, and the built-in potential also impacts the threshold voltage U_th of the channel [68]

$$U_\mathrm{bi} = \frac{k\vartheta}{e_0} \ln\left(\frac{N_\mathrm{A}^- N_\mathrm{D}^+}{n_\mathrm{i}(\vartheta)^2}\right). \tag{8.140}$$

The temperature dependency of U_bi is dominated by the temperature dependency of the intrinsic carrier concentration n_i [70]. Inserting the model for n_i (8.138) yields

$$U_\mathrm{bi}^* = \frac{k\vartheta}{e_0}\left(\ln\left(\frac{N_\mathrm{A}^- N_\mathrm{D}^+}{\vartheta^3 a_0^2}\right) + \frac{2a_1}{\vartheta}\right) \tag{8.141}$$

$$U_\mathrm{bi}^* = a_0 + a_1\vartheta - a_2 \ln\left(\frac{\vartheta}{1\,\mathrm{K}}\right)\vartheta, \quad a_i > 0 \wedge a_1 < a_2 \ln(\vartheta), \tag{8.142}$$

$$\frac{\mathrm{d}U_\mathrm{bi}^*}{\mathrm{d}\vartheta} = a_0 - a_1\left(1 + \ln\left(\frac{\vartheta}{1\,\mathrm{K}}\right)\right) < 0. \tag{8.143}$$

> **Remark:** As stated in Section 1.2, the regression parameters a_i are reused between equations and are therefore *not* necessarily equal in each equation.

The voltages associated with the n and p regions of the junction, U_p and U_n, can be described similarly

$$U_\mathrm{bi} = U_\mathrm{n} + U_\mathrm{p} = \frac{k\vartheta}{e_0}\ln\left(\frac{N_\mathrm{D}^+}{n_\mathrm{i}(\vartheta)^2}\right) + \frac{k\vartheta}{e_0}\ln\left(\frac{N_\mathrm{A}^-}{n_\mathrm{i}(\vartheta)^2}\right), \tag{8.144}$$

following the same model as (8.142) and (8.143).

8.5.1 Dependencies of the carrier mobility

The mobility μ of a free carrier describes the dependency between the electrical field E and the average drift velocity v_d

$$v_\mathrm{d} = \mu E. \tag{8.145}$$

When a carrier moves through a crystal lattice, a multitude of scattering effects occur concurrently [68]. Scattering effects generally lower the mobility. In this section, several relevant scattering effects will be described briefly. Their impacts vary with external factors like the temperature, the electric field or the doping concentrations. Therefore, different scattering effects dominate for different temperatures, field strengths and materials.

This work cannot describe the details of the band structures, energy states and scattering statistics which are needed to do these models justice. Consequently, there will be model concepts which use rough assumptions or boundary conditions. More detailed descriptions of the scattering effects can be found in [125].

Temperature An increasing temperature usually increases the impact of scattering effects on the carrier mobility. Experimental data [68] has shown that the electron mobility μ_n at low doping concentrations can be modeled as

$$\mu_\mathrm{n}^{(\mathrm{Si})} = 1360\,\frac{\mathrm{cm}^2}{\mathrm{V}\cdot\mathrm{s}}\left(\frac{\vartheta}{300\,\mathrm{K}}\right)^{-2.42}, \tag{8.146}$$

$$\mu_\mathrm{n}^{(\mathrm{4H-SiC})} = 1140\,\frac{\mathrm{cm}^2}{\mathrm{V}\cdot\mathrm{s}}\left(\frac{\vartheta}{300\,\mathrm{K}}\right)^{-2.7} \tag{8.147}$$

$$\Rightarrow \quad \mu_\mathrm{n}^* = a_0\left(\frac{\vartheta}{T_\mathrm{ref}}\right)^{-a1}, \quad T_\mathrm{ref}, a_i > 0 \tag{8.148}$$

$$\frac{\mathrm{d}\mu_\mathrm{n}^*}{\mathrm{d}\vartheta} = -a_0\left(\frac{\vartheta}{T_\mathrm{ref}}\right)^{-a1}. \tag{8.149}$$

Doping concentration The concentration of stationary ionized atoms with a positive $\left(N_\mathrm{D}^+\right)$ or negative charge $\left(N_\mathrm{A}^-\right)$ increases with the doping concentration. Moving free carriers scatter at the ionized atoms, reducing their mobility. This effect is referred to as *Rutherford* or *Coulomb scattering*. Figure 8.22 depicts the measured mobility depending on the doping concentration [68]. There is an upper limit for low concentrations and a lower limit for high concentrations [68, 121]. This dependency shows that the mobility used to describe the on-state voltage of a MOSFET does not remain constant across regions with different doping concentrations. If the concentration of ionized doping atoms is assumed to change with temperature, i.e., $\frac{\mathrm{d}N_\mathrm{A}^-}{\mathrm{d}\vartheta} \neq 0$ or $\frac{\mathrm{d}N_\mathrm{D}^+}{\mathrm{d}\vartheta} \neq 0$, the related change in mobility must be accounted for when calculating the resulting resistivity of a semiconductor region.

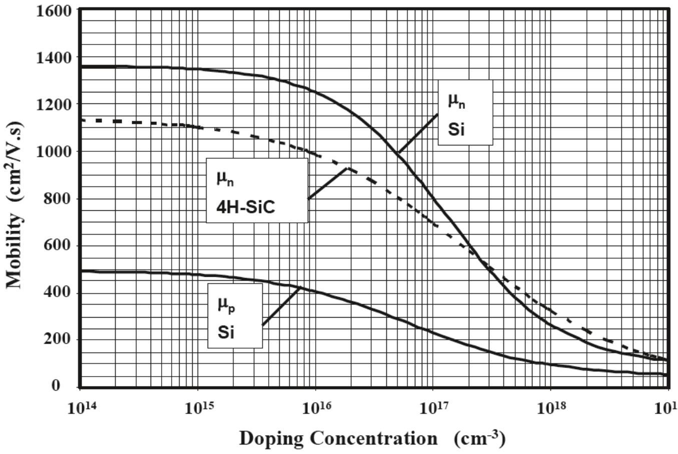

Figure 8.22: Mobility μ depending on the doping concentration [68][10]

Electrical field strength Equation (8.145) suggests a proportional increase in carrier velocity with the electric field strength. Nevertheless, saturation of the drift velocity $v_\mathrm{d,sat}$ at high field strengths $E > 1 \cdot 10^3\,\frac{\mathrm{V}}{\mathrm{cm}}$ was observed in experiments [68]. In the on-state of a

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MOSFET, this effect is relevant for the mobility in the MOSFET channel. This mobility can be described as

$$\mu = \frac{\mu_{\text{base}}}{\sqrt{1+\left(\frac{\mu_{\text{base}}E}{v_{\text{d,sat}}}\right)^2}}, \quad \mu \in \mathcal{O}\left(\frac{1}{E}\right), \tag{8.150}$$

$$v_{\text{d,sat,n}} = 1.434\cdot 10^7\,\frac{\text{m}}{\text{s}}\left(\frac{\vartheta}{1\,\text{K}}\right)^{-0.87} \quad [68]. \tag{8.151}$$

Combining (8.150) and (8.151) yields a temperature-dependent model of the electron mobility

$$\mu^*(\vartheta, E) = \frac{a_0}{\sqrt{a_1 E^2 \vartheta^{a_2}+1}}, \quad a_i > 0, E > 0, \tag{8.152}$$

$$\frac{\partial \mu^*}{\partial \vartheta} = -\frac{E^2\vartheta^{a_2-1}a_0a_1a_2}{2(E^2\vartheta^{a_2}a_1+1)^{3/2}} < 0, \tag{8.153}$$

$$\frac{\partial \mu^*}{\partial E} = -\frac{E\vartheta^{a_2}a_0a_1}{(E^2\vartheta^{a_2}a_1+1)^{3/2}} < 0. \tag{8.154}$$

Surface mobility In a MOSFET channel, the inversion layer is formed at the contact between the semiconductor and the insulator. The high carrier concentration at the surface rapidly decays moving inwards, with an effective layer thickness in the order of 100 Å[11] [68]. The narrow channel leads to frequent scattering of a laterally traveling carrier at surface defects and interface traps. Scattering at interface traps plays a major role in SiC devices [126], as the interface trap density is a hundred times higher than in Si [120]. These effects are further increased by the very strong electric fields normal to the surface E_{n} [121].

Even if the carrier concentration is assumed to be homogeneous in the channel, the electric field is not homogeneous, as the field strength at the top of the channel is higher than at the bottom. Consequently, the carriers at the top of the channel have a lower mobility than those at the bottom. The effective mobility of the channel is defined as [68]

$$\mu_{\text{n,eff}} = \frac{\int_0^{B_{\text{ch}}} \mu_{\text{n}}(y)\,n(y)\,\mathrm{d}y}{\int_0^{B_{\text{ch}}} n(y)\,\mathrm{d}y}, \tag{8.155}$$

reflecting the average mobility of the free electrons in the channel. The integrals are oriented from the surface towards the bulk, compare Figure 8.4, and average the mobility perpendicular ot the current flow. An analogous definition can be used for the effective electric field normal to the surface [121]

$$E_{\text{n,eff}} = \frac{\int_0^{b_{\text{sc}}} E(y)\,n(y)\,\mathrm{d}y}{\int_0^{b_{\text{sc}}} n(y)\,\mathrm{d}y} = -\frac{1}{\varepsilon}\left(Q_{\text{sc}} + \frac{Q_{\text{n}}}{2}\right). \tag{8.156}$$

Using the gate voltage dependency of the inversion layer charge Q_{n} (8.62) and space-charge

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[11] One Ångström equals 0.1 nm.

region charge Q_{sc}, a fit model for the effective electric field can be obtained

$$E^{*}_{\mathrm{n,eff}} = a_0 \left(U_{\mathrm{g}} - U_{\mathrm{th}}\right) + a_1, \quad a_i \in \mathbb{R}. \tag{8.157}$$

An appropriate empirical equation for the effective channel mobility is provided in [121]

$$\mu^{*}_{\mathrm{n,eff}} = \frac{a_0}{1 + \left(\frac{E_{\mathrm{n,eff}}}{a_1}\right)^{a_2}}, \quad a_i \in \mathbb{R}. \tag{8.158}$$

8.5.2 Special considerations for SiC

Most of the dependencies presented in the previous section were not limited to one specific material. Of course, the differences between silicon and silicon carbide in terms of power device operation are significant. The aim of the previous descriptions was to find fit model descriptions for different effects that are important when describing the MOSFET's electrical characteristics. As a consequence, quantitative differences between materials are usually not of concern. Quantitative comparisons between silicon and silicon carbide in power electronics can be found in [69]. There are, however, several differences that change the model behavior when applied to SiC devices.

Ionization degree of doping atoms All previous descriptions assume that all doping atoms are ionized, i.e., $N_{\mathrm{D}}^{+} = N_{\mathrm{D}}$ and $N_{\mathrm{A}}^{-} = N_{\mathrm{A}}$, having a corresponding ionization degree of $\xi = 1$. This assumption is valid for silicon devices operating at room temperature or higher, but is not correct for silicon carbide [127, 128]. Figure 8.23 shows the calculated ionization degree of a p-doped 4H-SiC semiconductor doped with aluminum as an example. It can be seen that the ionization degree of an SiC device can be significantly below 1 at typical operating temperatures. Also, a strong temperature dependency can be seen. The width of the space-charge regions at thermodynamic equilibrium is generally not affected, as the high electric field strengths cause the ionization of practically all doping atoms [69]. The channel can be assumed to be fully ionized due to the high electric field strength, while the electric field in the drift region is not sufficiently large to ionize all doping atoms [69]. Thus, The concentration of ionized donor atoms $N_{\mathrm{D}}^{+(\mathrm{Drift})}$ in the drift region is below the

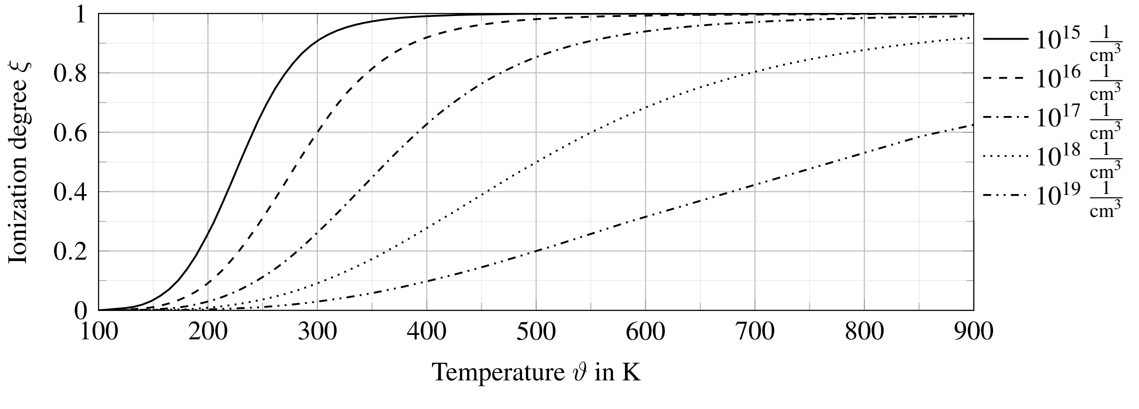

Figure 8.23: Ionization degree of 4H-SiC [127]; p-doped with aluminum at different doping concentrations; ionization energy $E_{\mathrm{Al}} = 200\,\mathrm{meV}$

concentration of the implanted donor atoms N_D and varies with temperature

$$N_\mathrm{D}^{+(\mathrm{Drift})} = \xi(\vartheta)\, N_\mathrm{D}{}^{(\mathrm{Drift})}, \quad \text{with } 0 \leq \xi(\vartheta) \leq 1. \tag{8.159}$$

As a consequence, the lowered specific conductance $\sigma = \xi(\vartheta)\, \mu N_\mathrm{D}{}^{(\mathrm{Drift})} e_0$ of the drift region needs to considered when determining the resistance of the drift region (8.136). Although the effect is less pronounced at low doping levels, even a 10 % change in the ionization degree can be important for TSEP-based temperature estimations.

8.6 SiC MOSFET SPICE models

In the previous sections, MOSFET models and material characteristics found in literature on power semiconductor devices were presented. Applying these models to power modules with confidential parameters is complex, but already performed elaborately in the creation of SPICE models.

In this section, typical models for SiC MOSFETs and the underlying subcomponents found in SPICE models will be presented. The models have already been fitted and tested against comparable devices, although typically focusing on aspects other than TSEPs [113]. The model terms used in the SPICE models will be summarized at the end of this section in Table 8.4. All models presented will focus on the on-state voltage in the linear region of the MOSFET, i.e., $U_\mathrm{ch} < U_\mathrm{g} - U_\mathrm{th}$. Model terms needed to describe the behavior at the saturation current or temperatures far above the maximum junction temperature, i.e., during a short circuit, will be neglected.

Appropriate SPICE models for MOSFETs or their subcomponents according to [108] can be found in [114, 129, 130]. In [113], a model for simulations outside the safe operating area, i.e., during short-circuit events, is presented. The self heating which occurs during a short circuit can reach approximately 1000 °C. Consequently, the model includes detailed temperature dependencies for the electron mobilities which have been validated experimentally with a comparable SiC MOSFET. The following key features are extracted from the SPICE model to describe the on-state voltage [113]:

1. a nonlinear temperature dependency of the threshold voltage

$$U_\mathrm{th}^* = \left(U_\mathrm{th,0} - \beta_\mathrm{th}\right) e^{-\varphi_\mathrm{th}(\vartheta - \vartheta_\mathrm{ref})} + \beta_\mathrm{th} \tag{8.160}$$

2. a bulk mobility model, allowing PTC and NTC behavior

$$\mu_\mathrm{n,bulk}^* = \mu_\mathrm{n,bulk,0} \left(\frac{\vartheta}{\vartheta_\mathrm{ref}}\right)^{-r + \alpha \frac{\vartheta}{\vartheta_\mathrm{ref}}} \tag{8.161}$$

3. a more detailed mobility model for the MOS channel, allowing PTC and NTC behavior

$$\mu_\mathrm{n,ch}^* = \mu_\mathrm{n,ch,0} \left(\frac{\vartheta}{\vartheta_\mathrm{ref}}\right)^{-m_\mathrm{ch,1} + m_\mathrm{ch,2} \exp\left(-m_\mathrm{ch,3} \frac{\vartheta}{\vartheta_\mathrm{ref}}\right)} \tag{8.162}$$

4. a combined term for the accumulation layer, JFET region and drift region, based on

the temperature dependency of the bulk mobility and the gate voltage, where each subcomponent $R_{\mathrm{D},i}$ has its own mobility term

$$R^*_{\mathrm{D},i}(\vartheta) = R_{\mathrm{ref},i}\left(\frac{\vartheta}{\vartheta_{\mathrm{ref}}}\right)^{-r_i+\alpha_{\mathrm{r}}\frac{\vartheta}{\vartheta_{\mathrm{ref}}}}, \tag{8.163}$$

$$U^*_{\mathrm{drift}} = I_{\mathrm{d}}\left(R^*_{\mathrm{D},0}(\vartheta) + R^*_{\mathrm{D},1}(\vartheta) + R^*_{\mathrm{D},2}(\vartheta)\left(1+\left(U_{\mathrm{g}}/U_2\right)\right)^{-\eta}\right). \tag{8.164}$$

The voltage U_2 is a regression parameter.

5. a channel model which considers nonlinearities of the gate capacitance (8.89) and the detailed mobility model

$$U^*_{\mathrm{ch}} = \frac{U_{\mathrm{g}} - U^*_{\mathrm{th}}(\vartheta)}{\alpha} - \sqrt{\left(\frac{U_{\mathrm{g}} - U^*_{\mathrm{th}}(\vartheta)}{\alpha}\right)^2 - \frac{I_{\mathrm{d}}}{\alpha K_0}\frac{\mu_{\mathrm{n,ch},0}}{\mu^*_{\mathrm{n,ch}}(\vartheta)}} \tag{8.165}$$

The final model of the on-state voltage is

$$U^*_{\mathrm{ds,on}} = U^*_{\mathrm{ch}} + U^*_{\mathrm{drift}}. \tag{8.166}$$

8.7 Model comparison with experimental data

In the previous section, different "physical" subcomponents that compose the on-state voltage were identified. For each subcomponent, several (mathematical) model variants were presented. The composition of the on-state voltage from a physical point of view and a (mathematical) model point of view is shown in Figure 8.24. The overall model is composed of the models of the subcomponents. Each subcomponent can depend on further subcomponents, therefore each model can depend on further models. A specific model for a subcomponent is called a variant.

The overall model of the on-state voltage is composed of a channel model U^*_{ch}, an accumulation layer model U^*_{a}, and a drift region model U^*_{drift}. These models use one of the several mobility model variants for the bulk $\mu_{\mathrm{n,bulk}}$ and another for the channel $\mu_{\mathrm{n,ch}}$.

$$U^*_{\mathrm{ds,on},k_0} = U^*_{\mathrm{ch},k_1}\left(\mu^*_{\mathrm{n,ch},k_2}, U^*_{\mathrm{th},k_6}\right) + U^*_{\mathrm{a},k_2}\left(\mu^*_{\mathrm{n,bulk},k_7}\right) + U^*_{\mathrm{drift},k_3}\left(\mu^*_{\mathrm{n,bulk},k_7}\right) + U^*_{\mathrm{t},k_4} \tag{8.167}$$

The indices k_1 to k_7 index the different model variants for each subcomponent, while k_0 indexes the resulting variant of the overall model $U^*_{\mathrm{ds,on},k_0}$ of the on-state voltage. The accumulation region and drift region always use the same mobility $\mu^*_{\mathrm{n,bulk},k_7}$. As a result, $(2\cdot 3\cdot 1)\cdot(2\cdot 2)\cdot 2 = 48$ distinct model variants of the on-state voltage U^*_{ch} are created. The overall model variants of the on-state voltage are also varied by including no resistance between chip and the module terminals or an ohmic resistance with linear temperature dependency U_{t}

In this section, the different model variants for each subcomponent will be listed and their ability to fit the on-state voltage will be assessed in terms of accuracy and model complexity. All model variants for the subcomponents are listed in Table 8.4. Their precise compositions are listed in Appendix C. In this section, each model variant will be fitted to 18 switches in

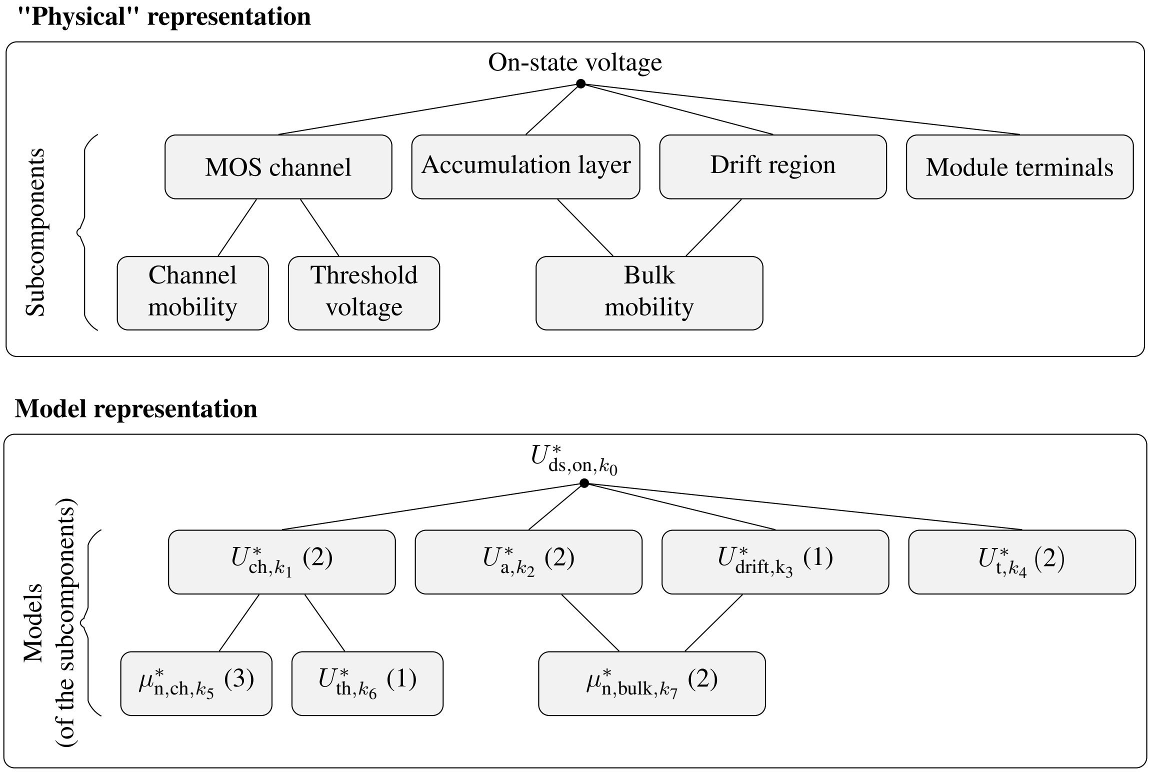

Figure 8.24: Composition of the on-state voltage from a physical point of view and a (mathematical) model point of view; the total number of available subcomponent models is listed in brackets

order to compare them and find a single model to be used in this work[12]. The modules and the measurement system will be presented in the next section, Chapter 10. The acceleration tests will be described in Chapter 14.

The model functions lead to nonlinear fit problems with many local minima. Suitable initial values for the fit parameters are needed to find a viable solution. Fundamental parameters can be estimated from the datasheet, e.g., $R_{\mathrm{ref},i}, U_{\mathrm{th},0}$ or K_0. Initial values of the mobilities' temperature dependencies are extracted from [113]. Each model variant is fitted over 100 times in order find lower local minima. For each run, each initial value is randomly varied by up to $\pm 50\,\%$. A tenth of the TSEP samples are excluded and kept as validation data. Each model variant is fitted until the best RMSD of the training data stagnates, while only the result with the lowest RMSD using the training data is kept, see *early stopping* in Section 4.2.1. The gate voltage U_{g} was considered constant and was determined by measurement while the system was idling[13].

The resulting fit metrics are depicted in Figure 8.25. Each model variant has 18 separate results, corresponding to the 18 fitted switches. The coefficient of determination R^2 is shown in the top graph. The middle and bottom graph show box plots of the achieved RMSD on the training and validation data for all 18 fitted switches. The evaluation will be performed based on the median observed RMSD using the *validation* data.

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[12] Measured on two individual modules and seven power module examples from the accelerated aging tests in their initial condition.

[13] Measured values of the actual gate voltage during the double-pulse experiments were available for the low-side switches only. Thus, this choice was made to keep consistency between the results of the high-side and low-side switches.

Table 8.4: Model variants for mobilities and voltage drops

	Variant ID	Model	Based on
Threshold voltage	1	$U^*_{\text{th}} = \left(U_{\text{th},0} - \beta_{\text{th}}\right) e^{-\varphi_{\text{th}}(\vartheta - \vartheta_{\text{ref}})} + \beta_{\text{th}}$	(8.160)
Bulk mobility	1	$\mu^*_{\text{n,bulk}} = \mu_{\text{n,bulk},0} \left(\frac{\vartheta}{\vartheta_{\text{ref}}}\right)^{-r_{\text{B}}}$	(8.148)
	2	$\mu^*_{\text{n,bulk}} = \mu_{\text{n,bulk},0} \left(\frac{\vartheta}{\vartheta_{\text{ref}}}\right)^{-r_{\text{B}} + \alpha \frac{\vartheta}{\vartheta_{\text{ref}}}}$	(8.161)
Channel mobility	1	$\mu^*_{\text{n,ch}} = \mu_{\text{n,ch},0} \left(\frac{\vartheta}{\vartheta_{\text{ref}}}\right)^{-r_{\text{ch}}}$	(8.148)
	2	$\mu^*_{\text{n,ch}} = \mu_{\text{n,ch},0} \sqrt{m_{\text{ch},4} \left(U_{\text{g}} - U^*_{\text{th}}(\vartheta)\right)^2 \vartheta^{m_{\text{ch},5}} + 1}^{\,-1}$	(8.150)
	3	$\mu^*_{\text{n,ch}} = \mu_{\text{n,ch},0} \left(\frac{\vartheta}{\vartheta_{\text{ref}}}\right)^{-m_{\text{ch},1} + m_{\text{ch},2} \exp\left(-m_{\text{ch},3} \frac{\vartheta}{\vartheta_{\text{ref}}}\right)}$	(8.162)
MOS channel	1	$U^*_{\text{ch}} = \left(U_{\text{g}} - U^*_{\text{th}}(\vartheta)\right) - \sqrt{\left(U_{\text{g}} - U^*_{\text{th}}(\vartheta)\right)^2 - \frac{2I_{\text{d}}}{K_0} \frac{\mu_{\text{n,ch},0}}{\mu^*_{\text{n,ch}}(\vartheta)}}$	(8.18)
	2	$U^*_{\text{ch}} = \frac{\left(U_{\text{g}} - U^*_{\text{th}}(\vartheta)\right)}{\alpha} - \sqrt{\left(\frac{U_{\text{g}} - U^*_{\text{th}}(\vartheta)}{\alpha}\right)^2 - \frac{2I_{\text{d}}}{\alpha K_0} \frac{\mu_{\text{n,ch},0}}{\mu^*_{\text{n,ch}}(\vartheta)}}$	(8.89)
Accumulation layer/ JFET region	1	$U^*_{\text{a}} = \left(U_{\text{g}} - U^*_{\text{th}}(\vartheta) - U^*_{\text{ch}}\right) - \sqrt{\left(U_{\text{g}} - U^*_{\text{th}}(\vartheta) - U^*_{\text{ch}}\right)^2 - \frac{2I_{\text{d}}}{K_{\text{A}} K_0} \frac{\mu_{\text{n,bulk},0}}{\mu^*_{\text{n,bulk}}(\vartheta)}}$	(8.126)
	2	$U^*_{\text{a}} = I_{\text{d}} \left(R^*_{\text{D},1}(\vartheta) + R^*_{\text{D},2}(\vartheta) \left(1 + U_{\text{g}}/U_2\right)^{-\eta}\right), \quad R^*_{\text{D},i}(\vartheta) = R_{\text{ref},i} \frac{\mu_{\text{n,ch},0}}{\mu^*_{\text{n,ch}}(\vartheta)}$	(8.165)
Epitaxial layer or drift region	1	$U^*_{\text{drift}} = I_{\text{d}} R_{\text{EPI},0} \frac{\mu_{\text{n,ch},0}}{\mu^*_{\text{n,ch}}(\vartheta)}$	(8.127), (8.164)
Interconnects (terminals to chip)	1	$U^*_{\text{t}} = 0$	
	2	$U^*_{\text{t}} = I_{\text{d}} R_{\text{t}} \left(1 + \alpha_{\text{t}} (\vartheta - \vartheta_{\text{ref}})\right)$	

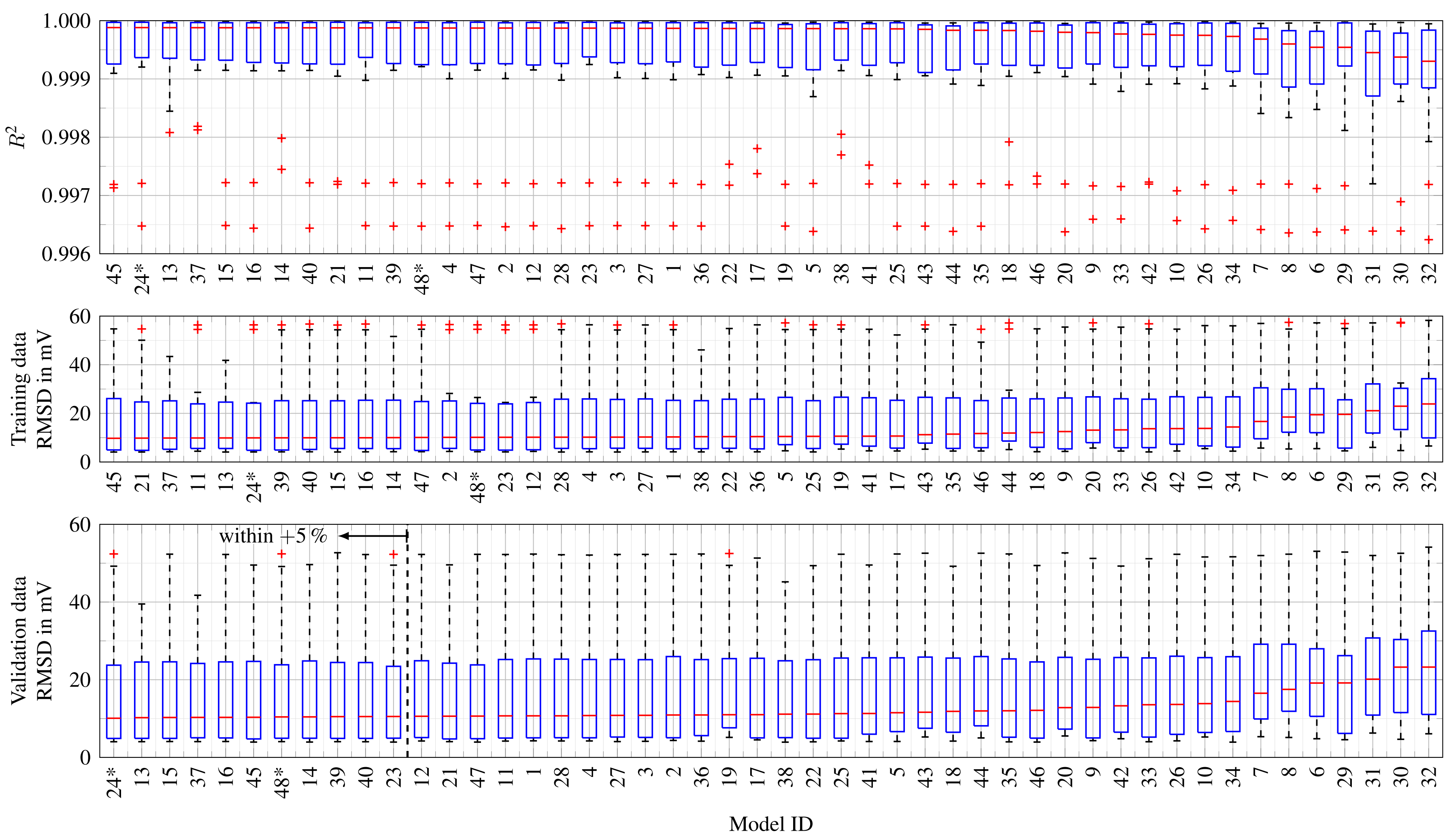

Figure 8.25: Fit metrics for the 48 model variants; box plots of the results from 18 switches; models sorted by their medians; * model based on the spice model (8.160) to (8.166)

In each plot, the models are sorted from best to worst. It can be seen that Model Variant 24 has the best median metrics, although the medians of the first eleven models are within $+5\,\%$ of that of Model Variant 24. Model Variant 24 is the model variant based on SPICE models presented in Section 8.6 without taking any resistance between the chips and the module terminals into account. Model Variant 48 is the same model variant except that it also incorporates an ohmic terminal resistance.

As an additional metric, Figure 8.26 shows the model RMSD compared to the number of fit parameters.

Even though Model Variant 24 has the lowest RMSD using the validation data, Model Variant 13 has significantly fewer fit parameters and less model complexity, while increasing the RMSD by only $1.5\,\%$. Interestingly, Model Variant 13 is composed of the most basic model variant listed in Table 8.4, expect for the MOS channel. Model Variant 13 is chosen as the modeling approach for the rest of this work and is composed of these subcomponent variants

$$U^*_{\text{th}} = \left(U_{\text{th},0} - \beta_{\text{th}}\right) e^{-\varphi_{\text{th}}(\vartheta - \vartheta_{\text{ref}})} + \beta_{\text{th}}, \tag{8.168}$$

$$\mu^*_{\text{n,bulk}} = \mu_{\text{n,bulk},0} \left(\frac{\vartheta}{\vartheta_{\text{ref}}}\right)^{-r_{\text{B}}}, \tag{8.169}$$

$$\mu^*_{\text{n,ch}} = \mu_{\text{n,ch},0} \left(\frac{\vartheta}{\vartheta_{\text{ref}}}\right)^{-r_{\text{ch}}}, \tag{8.170}$$

$$U^*_{\text{ch}} = \frac{\left(U_{\text{g}} - U^*_{\text{th}}(\vartheta)\right)}{\alpha} - \sqrt{\left(\frac{U_{\text{g}} - U^*_{\text{th}}(\vartheta)}{\alpha}\right)^2 - \frac{2I_{\text{d}}}{\alpha K_0} \frac{\mu_{\text{n,ch},0}}{\mu^*_{\text{n,ch}}(\vartheta)}}, \tag{8.171}$$

$$U^*_{\text{a}} = \left(U_{\text{g}} - U^*_{\text{th}}(\vartheta) - U^*_{\text{ch}}\right) - \sqrt{\left(U_{\text{g}} - U^*_{\text{th}}(\vartheta) - U^*_{\text{ch}}\right)^2 - \frac{2I_{\text{d}}}{K_{\text{A}} K_0} \frac{\mu_{\text{n,bulk},0}}{\mu^*_{\text{n,bulk}}(\vartheta)}}, \tag{8.172}$$

$$U^*_{\text{drift}} = I_{\text{d}} R_{\text{EPI},0} \frac{\mu_{\text{n,ch},0}}{\mu^*_{\text{n,ch}}(\vartheta)}, \tag{8.173}$$

$$U^*_{\text{t}} = 0. \tag{8.174}$$

Remark: Figure 8.26 states that Model Variant 13 has 12 regression parameters, while counting all parameters in (8.168) to (8.174) yields only 11

$$U_{\text{th},0},\ \beta_{\text{th}},\ \varphi_{\text{th}},\ \mu_{\text{n,bulk},0},\ r_{\text{B}},\ \mu_{\text{n,ch},0},\ r_{\text{ch}},\ \alpha,\ K_0,\ K_{\text{A}},\ R_{\text{EPI},0}. \tag{8.175}$$

This discrepancy has two sources.

First, the model is actually independent of $\mu_{\text{n,bulk},0}$ and $\mu_{\text{n,ch},0}$. These two parameters are redundant with respect to the transconductance K_0 and the reference resistance of the drift region $R_{\text{EPI},0}$. The transconductance K_0 is already proportional to $\mu_{\text{n,ch},0}$ and $R_{\text{EPI},0}$ is already proportional to $\mu^{-1}_{\text{n,bulk},0}$. Whenever K_0 or $R_{\text{EPI},0}$ are used in (8.171) to (8.173), they have to be divided by the reference mobility $\mu_{\text{n,bulk},0}$ or $\mu_{\text{n,ch},0}$ before the temperature dependent mobility model $\mu^*_{\text{n,bulk}}$ or $\mu^*_{\text{n,ch}}$ is inserted. These regression parameters are automatically eliminated during model construction already, leading to nine expected regression parameters in (8.168) to (8.174).

Second, each measured parameter $\tilde{x}$ is extended with an offset x_0 to account for sensor offsets. Here, the drain current I_{d}, the temperature ϑ and the

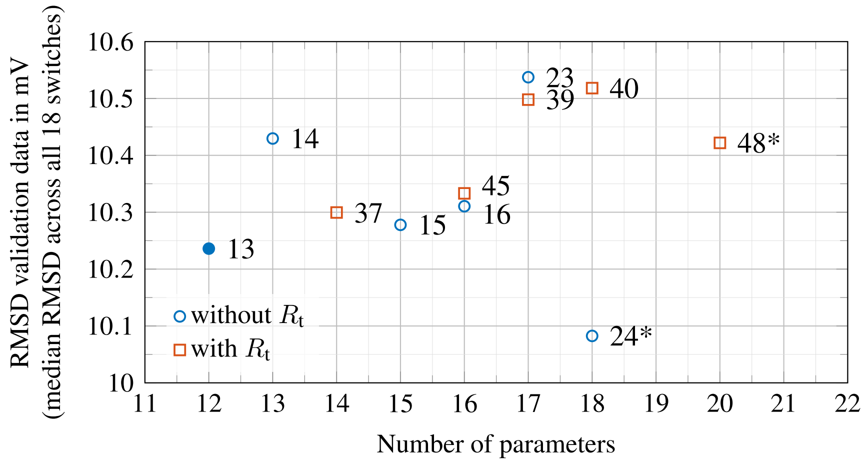

Figure 8.26: Comparison of the RMSD achieved using the validation data compared to the model variant parameters for model variants within +5 % of the model with the lowest RMSD

on-state voltage $U_{\text{ds,on}}$ itself are extended by an offset

$$I_{\text{d}} = \tilde{I}_{\text{d}} + I_{\text{d},0}, \tag{8.176}$$

$$\vartheta = \tilde{\vartheta} + \vartheta_0, \tag{8.177}$$

$$U_{\text{ds,on}} = \tilde{U}_{\text{ds,on}} + U_{\text{ds,on},0}. \tag{8.178}$$

These offsets are also considered regression parameters, as described in Section 4.1. The additional offsets add three regression parameters, resulting in the stated number of 12 regression parameters.

The values of the regression parameters (8.175), as well as their initial values, are listed in Appendix D for each of the 18 switches.

Figure 8.27 shows the fit result of the chosen model variant for a single module. It can be seen that the low-side switch has a significantly higher RMSD and a small discontinuity at 0 A. This is a trend that could be observed throughout all modules. Usually, the low side is expected to be less affected by EMI after switching, as the reference potential $U_{\text{DC}-}$ is bound more tightly to the PE potential via the Y-capacitors. Both ADC measurement circuits are designed in the same way. Possible causes for this behavior are the different commutation cells of the high side (smaller cell) and low side (larger cell) or the fact that only the low side has an oscilloscope attached, forming an additional grounding and EMI path.

8.7.1 Impact of the subcomponent variant choice

So far, the results for all model variants have been discussed separately. In this section, the impact of each subcomponent's model complexity will be investigated. Figure 8.28 shows the achieved RMSD using the validation data for each subcomponent when a specific subcomponent model variant is chosen. The variants of the other subcomponents are not considered as classification features and are united. Therefore, each box plot contains one half or one third of the total data set of 864 fit results.

When considering the bulk mobility and channel mobility, it can be seen that switching from the mobility model with only NTC behavior to a model with NTC and PTC behavior

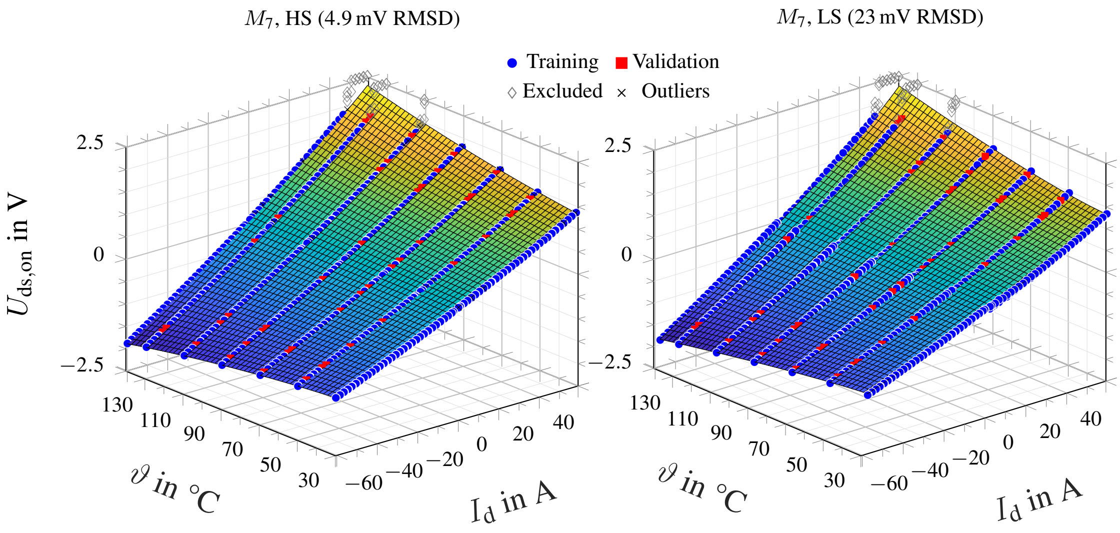

Figure 8.27: Fit result illustration for Model Variant 13 and Module M_7(surface plot); data binning used in training and validation data; data points are excluded (gray) when one of the ADC samples saturated at 2.5 V; details will be presented in Section 10.6; for more detailed plots, see Appendix L; No outliers present in these graphs

does not improve the fit quality of the validation data, see Marker I. Choosing a channel mobility model variant based on the saturation velocity of carriers severely reduces the fit precision, see Marker II. As expected, the MOS channel has a large impact on the fit precision. Using a more complex MOS channel model variant improves the fit results significantly, see Marker III. The differences between the model variants for the accumulation region are small, see Marker IV. Therefore, the exact modeling choice for this region has little impact. A reason for this may be that the impact of the accumulation region can also be covered by other model terms. Model Variant 1 of the accumulation layer has a similar form as the MOS channel models, while Model Variant 2 is similar to the model of the drift region, see Table 8.4. The inclusion of a terminal-to-chip resistance with PTC behavior does not improve the fit quality, see Marker V. For this module, the terminal resistance is either so small that it has no significant impact, or its modeled linear temperature dependency cannot be distinguished from the slightly nonlinear temperature dependency of the carrier mobility. For more details, see Appendix E.

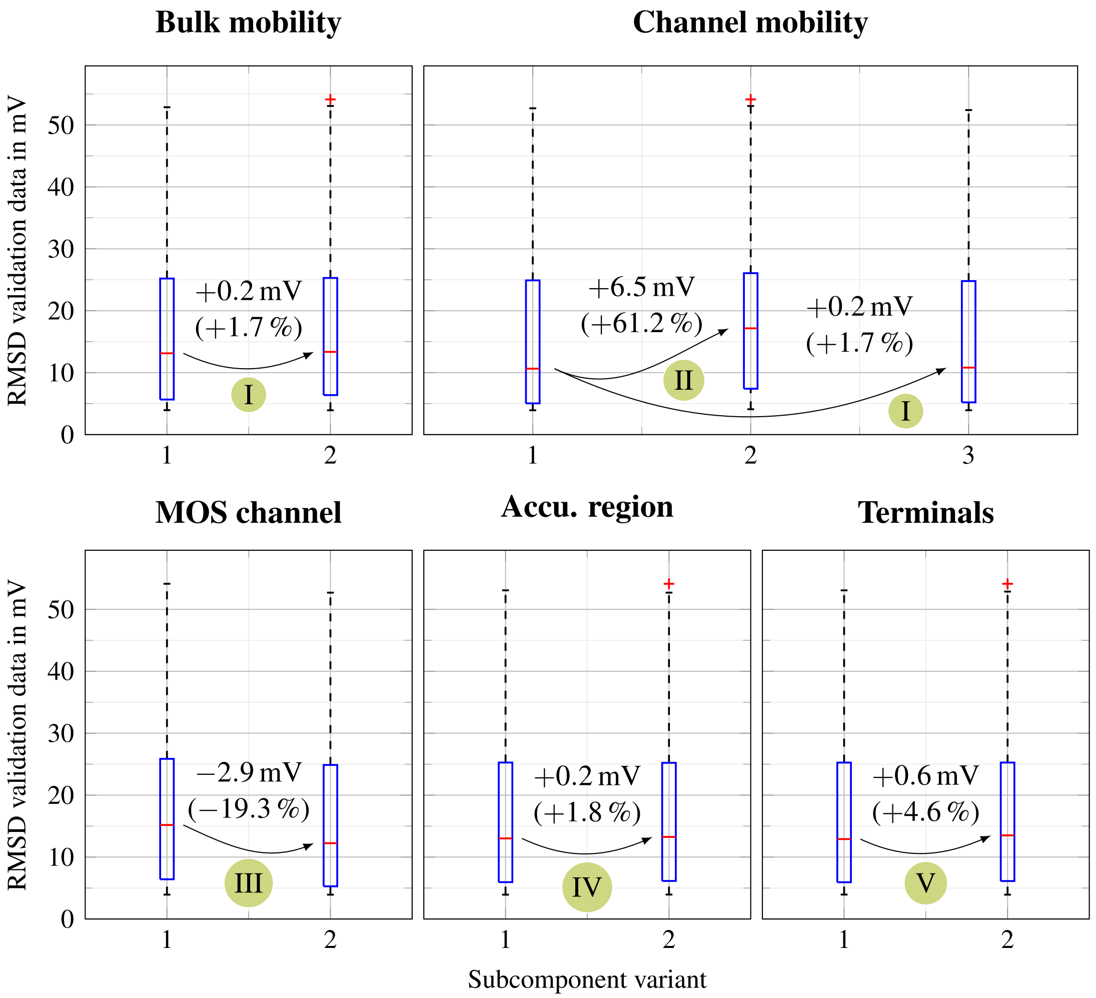

Figure 8.28: Fit RMSD when choosing a specific subcomponent model variant compared to all others; higher subcomponent ID generally means higher complexity; see Table 8.4 for model variant definitions

9 Turn-on times

The models of the turn-on delay time t_d and the time t_rrm until the overcurrent peak is reached require additional knowledge of the gate loop and other aspects of the power device structure beside the semiconductor's behavior. First, the semiconductor properties required concerning the threshold voltage are discussed and the gate charge curve is measured. Afterwards, systematic aspects like the gate loop inductance are added to the models. Finally, the different model variants for each model subcomponent are summarized and fitted to the measurement data of the 18 switches, in order to assess the level of detail which is required for TSEP-based temperature estimation.

9.1 Threshold voltage dependencies

The threshold voltage is one of the most relevant parameters with regard to the switching times. Beside the temperature, other parameters impact the threshold voltage leading to cross-dependencies on the dc-link voltage and the negative gate driver voltage. The underlying mechanisms of the semiconductor are summarized in this section.

9.1.1 Drain-induced barrier lowering

The device under test is a short-channel MOSFET and is therefore susceptible to drain-induced barrier lowering (DIBL) [120]. DIBL describes the lowering of the threshold voltage U_th at the gate contact when the drain-source voltage increases.

In Section 8.1.3, the nonlinear dependency between the applied gate voltage and the charge of the inversion layer Q_n (8.81) was presented. If a positive voltage is applied to the surface of the MOS channel in order to form the inversion layer, the space-charge in the bulk can be separated into two parts: the charge of the space-charge region and the charge of the free carriers in the inversion layer. The charge of the space-charge region is stationary and does not contribute to the conductivity of the channel.

Similarly, when a positive drain voltage U_ds is applied, a depletion layer forms at the p-n junction of the drain and the p-base. The location of the drain-induced depletion layer partly coincides with the location of the space-charge region between the MOS channel and the bulk [131]. In these parts, no gate voltage, or a lower gate voltage, is required to form the space-charge region between the MOS channel and the bulk.

Therefore, the amount of charge which needs to be induced by the gate voltage to fully form the gate-source space-charge region is lower than without an applied drain-source voltage [121]. Consequently, the threshold voltage that needs to be applied to the gate in order to form the inversion layer decreases with increasing drain voltage.

An alternative approach to explaining DIBL uses the changes in the conduction band when a drain voltage is applied. Figure 9.1 illustrates the conduction band along the channel for a short-channel and a long-channelMOSFET [121]. When a positive voltage is applied to the drain, the corresponding depletion layer expands into the p-base or MOS channel region.

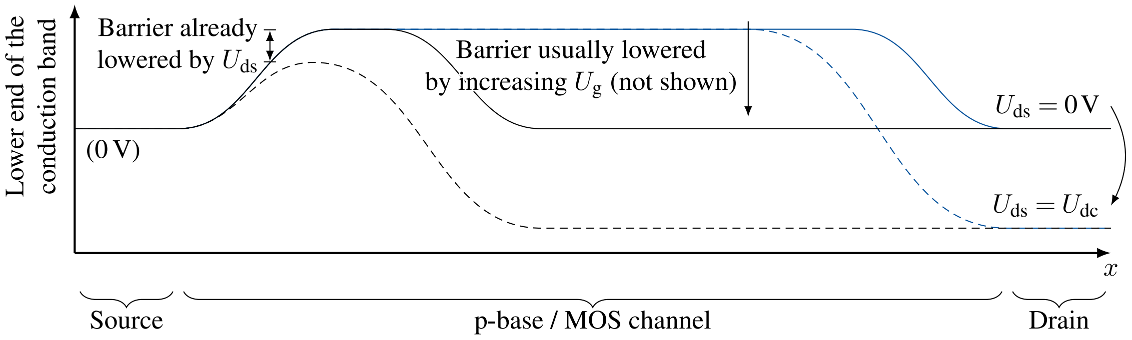

Figure 9.1: Conduction band along the channel of a short-channel (black) and a long-channel MOSFET (blue) at $U_{\mathrm{gs}} = 0$ [121]

For a short-channel MOSFET, this can cause barrier lowering of the conduction band in the p-base, thus decreasing the gate voltage needed to overcome the barrier for electrons moving from source to drain.

The quantitative description of this effect quickly leads to two-dimensional problems and complex terms [132, 133] and is usually approximated linearly [134–136]

$$U_{\mathrm{th}}(U_{\mathrm{ds}}) = U_{\mathrm{th},0} + \lambda_{\mathrm{DIBL}} U_{\mathrm{ds}}, \quad \lambda_{\mathrm{DIBL}} < 0. \tag{9.1}$$

Figure 9.2 depicts the drain-source voltage dependency of the threshold voltage published by the manufacturer for the device under test (DUT), which shows that a linear approximation is reasonable.

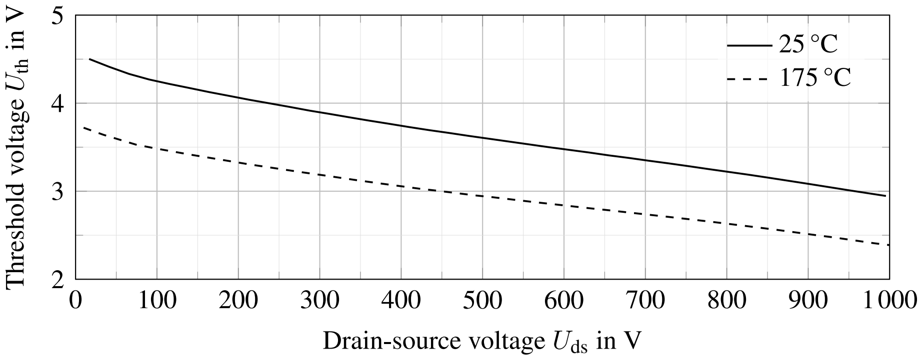

Figure 9.2: Typical dependence of threshold voltage on the drain-source voltage for the DUT [118]

9.1.2 Threshold voltage hysteresis

Point defects at the semiconductor to insulator contact can act as charge traps with regard to the Shockley-Read-Hall combinations [68]. According to [120], charge traps can be separated into two types. *Interface* traps are defined as traps in the semiconductor with an energy level within the bandgap of the semiconductor that can exchange carriers with the semiconductor's conduction and valence band. *Border* traps are defined as traps within the insulator, but still close to the semiconductor, with an arbitrary energy level. These are caused by different kinds of insulator defect [120]. Border traps can exchange charges with the semiconductor, but the corresponding time constants are very large compared to the switching periods of the device.

Beside their physical nature, interface and border traps can also be separated by their time constants. The time constants for interface traps to reach thermal equilibrium are within typical durations of a switching process and interface traps are fully reversible [120]. Border traps have long time constants and are associated with the *bias-temperature-instability* [137], increasing the threshold voltage of the device gradually during its lifetime [120].

The effects described in this section occur in Si and SiC, but their magnitude is neglectable in Si devices and significant in SiC devices [118]. Expectable magnitude ranges follow at the end of the section.

The thermal equilibrium of the amount of trapped charge varies depending on the applied gate voltage. Applying a negative gate voltage increases the number of holes trapped in the interface traps. The trapped charges act as a bias and shift the threshold voltage of the device, i.e., if a large number of holes are trapped in the MOS channel region, a lower voltage is required on the gate terminal to turn the device on.

Figure 9.3 illustrates the process of charge trapping in interface traps and the corresponding shift in the threshold voltage. Without a gate bias, i.e., $U_{\mathrm{g}} = 0\,\mathrm{V}$, the Fermi level E_{F} in the channel is close to the valence band, depending on its p-doping. The interface traps between the Fermi level and the conduction band are more likely to trap a hole. When a negative gate voltage is applied, an accumulation layer of holes forms and the Fermi level is pinned to the valence band [120].

When the gate voltage is increased to the threshold voltage, by definition the Fermi level moves close to the conduction band with the same distance it had to the valence band when the gate was unbiased. The change in the Fermi level therefore spans almost the entire bandgap. As a consequence, most interface traps are then below the Fermi level and start to capture electrons from the conduction band or emit holes into the valence band. The relaxation time of the interface traps is relevant compared to typical switching frequencies of SiC MOSFETs. Thus, the remaining positively charged interface traps act as an additional gate bias, lowering the gate voltage that must be applied to the outside terminal to form the inversion layer[1].

> **Remark:** At this point it needs to be discussed, whether the interface traps act like donator or acceptor doping atoms/molecules, i.e., whether they can be positively or negatively charged. According to [137], the dominant mechanism of the interface traps is "hole trapping". Thus, it can be assumed that the interface traps are either charged positively (trapped a hole) or neutrally (reemitted a trapped hole/recaptured an electron).

The time constant until thermal equilibrium is regained can be in the order of seconds at low currents [120]. It shortens with increased gate voltage and is inversely proportional to the drain current [120].

Before turn-off, the gate voltage is above the threshold voltage. The Fermi level of the channel is pinned to the conduction band. When the gate voltage is lowered to the threshold level, the Fermi level decreases only slightly. As a consequence, the perturbation of the Fermi level is small compared to the upward direction of the gate voltage and fewer traps

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[1] Forming the inversion layer is the definition of the threshold voltage, which is lowered as a consequence, see Section 8.1.2.

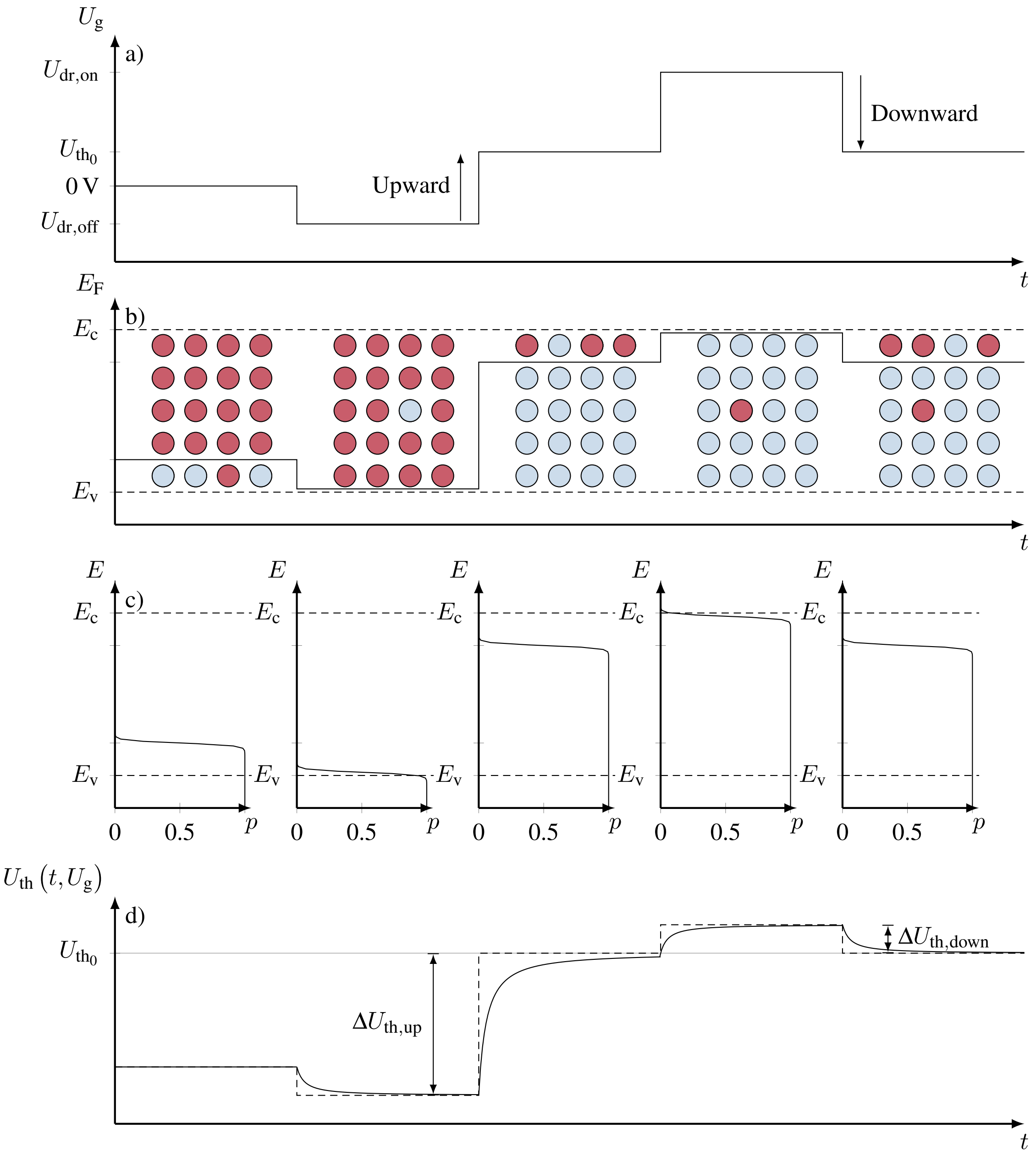

Figure 9.3: Interface traps and gate voltage hysteresis [120]: a) the applied gate voltage U_g is changed in the upward and downward directions; the threshold voltage stated in the datasheet U_{th_0} is measured with $U_{ds} = U_{gs} = U_{th}$ in the downward direction; b) Fermi level E_F and an illustration of the interface traps trapping holes $E > E_F$ (red); c) corresponding Fermi-Dirac statistics for $\vartheta = 300\,K$ and a bandgap of $E_G = 3.3\,eV$; d) steady-state and dynamic behavior of the effective threshold voltage; (time constants of the hysteresis illustrated according to a power function $\Delta U_{th} \propto t^{-a}$ [126], details follow in Section 9.3)

need regain thermal equilibrium [120]. The threshold voltage shift in the downward direction is small compared to the threshold voltage shift in the upward direction [120].

The resulting hysteresis of the threshold voltage leads to different threshold voltage measurements depending on the gate bias polarity before the measurement [120]. The datasheet values are measured in the downward direction [118]. As the time constants are inversely proportional to the drain current, the effect of the threshold voltage hysteresis at the nominal current of the devices is small [120].

The magnitude of the threshold voltage hysteresis is approximately proportional to the bandgap and the density of interface trap states within the bandgap [120]. The density of interface trap states depends on the manufacturing process and is approximately one hundred times larger in today's SiC than in Si [120]. The bandgap of SiC is three times larger than that of Si. As a result, the voltage hysteresis in SiC with today's manufacturing processes is expected to be in the range of 1 V to 10.7 V, whereas the effect in Si is expected to be below 36 mV [120].

9.1.3 Subthreshold conduction

Figure 9.1 shows the conduction band structure of a MOSFET when unbiased. If the gate voltage is increased, the conduction band plateau in the p-base, or MOS channel region, is lowered. At gate voltage levels slightly below the threshold voltage, the barrier for electrons being injected from the source into the p-base is small. Similar to BJT devices, a small diffusion current of electrons is generated that flows from the source into the p-base and can reach the drain [121]. The barrier from the drain to the p-base is assumed to be high, due to the applied drain-source voltage. In this region, the resulting subthreshold current increases exponentially with the gate voltage [121]. The relevant range of gate voltages for subthreshold conduction is between $U_{\mathrm{th}} - 0.2\,\mathrm{V}$ and the threshold voltage U_{th} [121].

9.2 Gate charge measurement

The nonlinear gate charge curve of the device under test is one of the key components for modeling the turn-on process. The previous discussions of the nonlinearities of the gate capacitance, see Section 8.1.3, were focused on describing the dependency between the applied gate voltage U_{g} and the resulting charge of the *inversion layer* Q_{n}, as this charge component is the defining quantity for channel conductivity.

Modeling the turn-on process must be done considering the total charge supplied from the gate driver to the gate-source terminals. In this context, the entire charge injected into the gate terminal is of interest, e.g., to model the time needed to reach the threshold voltage. On the one hand, this extends the gate-source capacitance C_{gs} to also include charge components from the gate electrode to the source electrode. On the other hand, the voltage-dependent gate-drain capacitance C_{gd} must still be accounted for. Figure 9.4 illustrates the additional capacitive components compared to the investigations done in Chapter 8.

The gate charge curve can be measured by applying a drain voltage to the device and slowly turning it on [138]. The gate current is passed through a shunt resistor for the purposes of measurement. Integrating the gate current yields the gate charge. The measurement setup is the same as was used for the IGBT gate charge curve measurement, see Figure 7.9. The (raw) signal waveforms are shown in Figure 9.5.

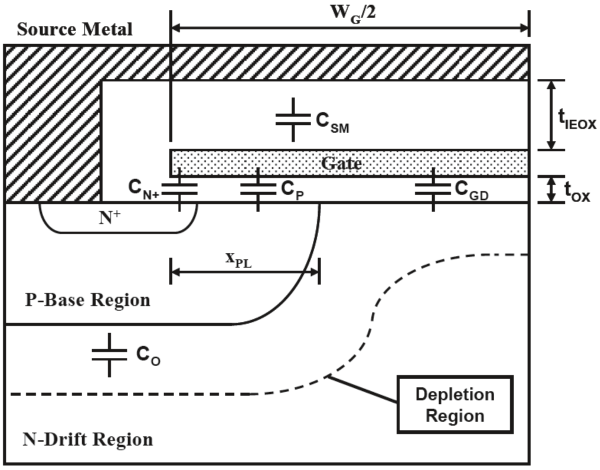

Figure 9.4: Capacitances within a MOSFET [68][3]

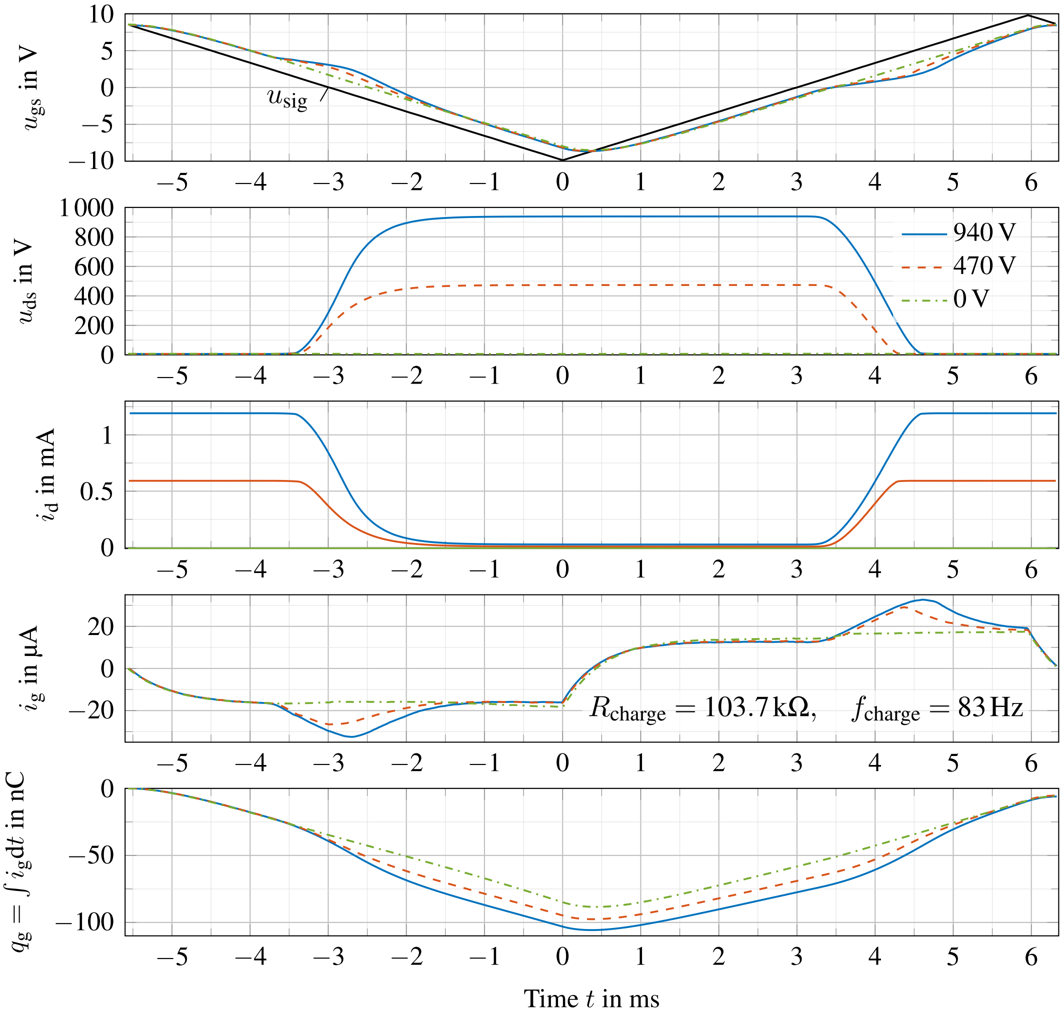

Figure 9.5: Signal waveforms of the SiC MOSFET gate charge measurement at different dc voltage levels and at 30 °C; see Figure 7.9 for setup definitions

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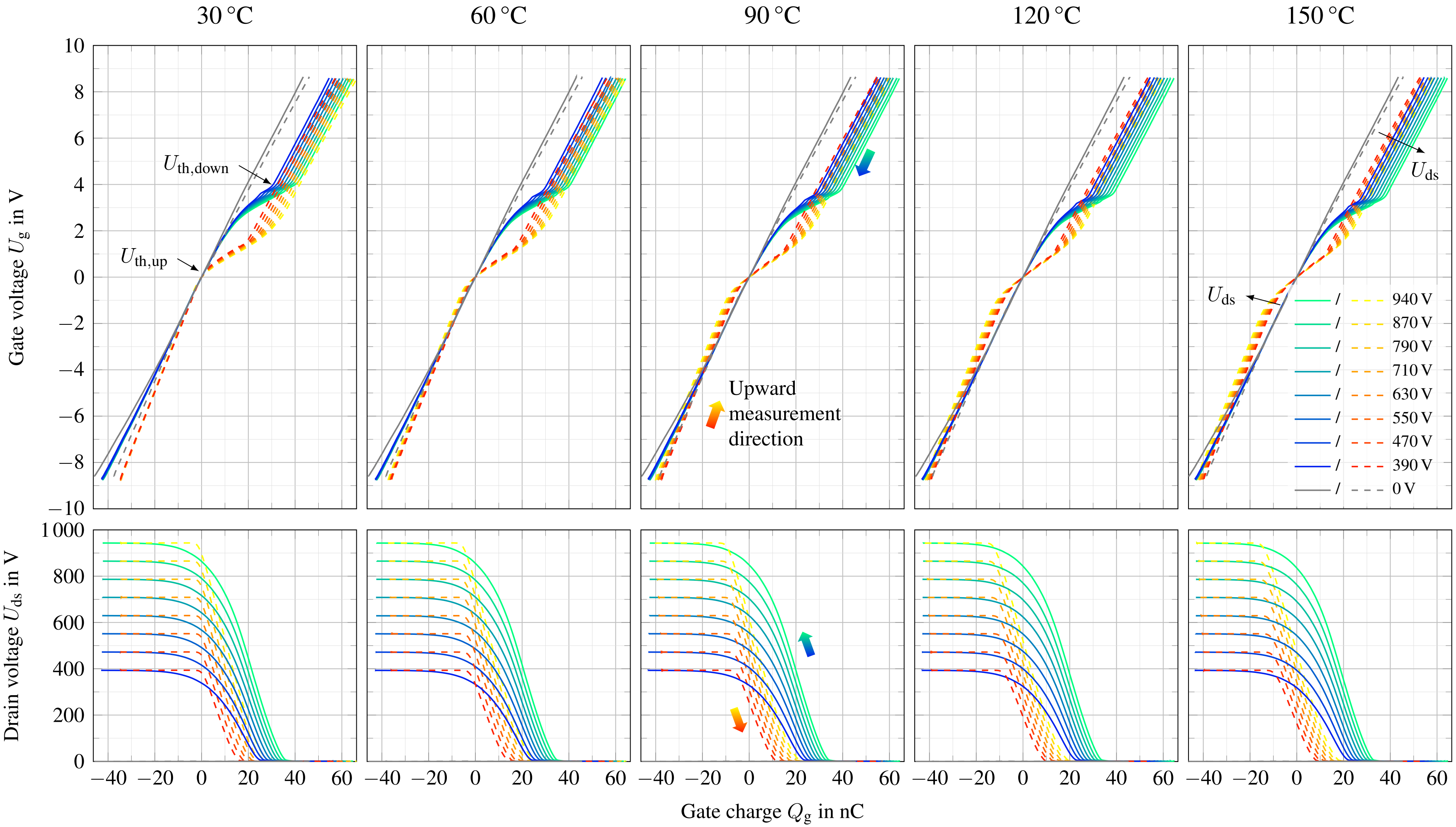

Figure 9.6: Gate charge curves at different temperatures and maximum drain voltages; measurement of the gate voltage in the upward direction shown as a dashed line; downward as a solid line; Module M_0 used

The resulting gate charge curves at different temperatures and dc-link voltages are shown in Figure 9.6. The integration of the gate current to give the gate charge introduces an integration constant, which was chosen such that the origin is at $U_g\big(Q_g = 0\,\mathrm{C}\big) = 0\,\mathrm{V}$. The graphs of the gate charge curve are different for the upward and downward directions, which is due to the aforementioned threshold voltage hysteresis. When comparing the results to datasheet values of the threshold voltage[2], the downward direction should be used.

In the upward direction, the expected Miller plateau can be clearly seen as a Miller ramp, which is caused by the drain-induced barrier lowering [118]. The shape of the Miller ramp in the downward direction is not as linear, since the drain-source voltage does not change so constantly. The measurement setup uses a very large drain resistor of $R_{\mathrm{d,dc}} = 1\,\mathrm{M\Omega}$ to limit the losses during the slow turn-on. During turn-off, or in the downward direction, the channel closes. The large drain resistor leads to a very low drain current, slowly charging the output capacitances of the MOSFETs. Thus, the waveform of u_{ds} with respect to time matches the step response of a first-order low-pass filter. In the upward direction, the channel turns on and basically shorts the drain to the source. This leads to the typical linear slope of U_{ds} with respect to the Miller capacitance. A measurement at $U_{\mathrm{ds}} = 0\,\mathrm{V}$ is shown for reference in gray. The setup was not changed for this measurement, so the drain and the source are not ideally shorted together, but rather connected via the $R_{\mathrm{d,dc}} = 1\,\mathrm{M\Omega}$ drain resistor and a 0 V dc-link power supply.

Comparison to literature The measured gate voltage in the upward direction $U_{\mathrm{th,up}}$ is remarkably low, as shown in Figure 9.6. In this paragraph, the measurement data acquired in the test setup is compared to similar studies found in literature.

In measurements conducted in [120], the gate and drain contact are shorted and the gate voltage is slowly increased from a negative value until a small, constant drain current flows. The constant current is controlled and held for a prolonged time by adjusting the gate and drain voltage. The required gate voltage is recorded and corresponds to the threshold voltage in the upward direction depending on the time $u_{\mathrm{th,up}}$. During the measurement, the applied gate voltage increases while the drain current is constant, as shown in Figure 9.7. The recovery of the threshold voltage is due to the interface traps emitting holes and progresses faster at higher drain currents [120]. The measurements presented in [120] suggest that threshold voltage levels as low as 0.5 V are to be expected in the upward direction, which

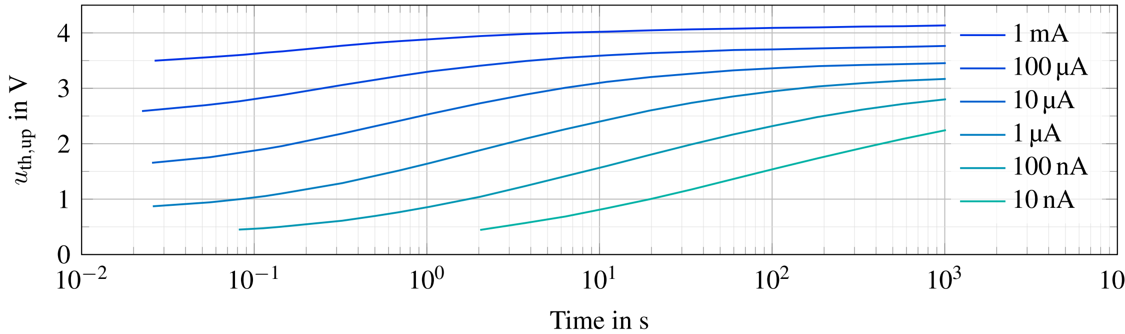

Figure 9.7: Threshold voltage measurements in the upward direction conducted in [120] at room temperature with $U_g = U_{\mathrm{ds}}$; A larger drain current decreases the recovery time of the threshold voltage

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[2] Datasheet values $U_{\mathrm{th}} =$ 3.5 V to 5.5 V at 25 °C; typically 4.5 V

matches the acquired data in the test setup given, as shown in Figure 9.6. In the setup given in this work, a large drain resistance determines the drain current. At its highest, the drain current is only

$$\max i_{\mathrm{d}} = 1.2\,\mathrm{mA}, \tag{9.2}$$

compare Figure 9.5. When the threshold voltage is reached in upward direction, almost the entire dc-link voltage is still blocked by the MOSFET, therefore the drain current will be orders of magnitude smaller at this point. Thus, the observed threshold voltage levels in the upward direction $U_{\mathrm{th,up}}$ well below 1 V in Figure 9.6 are plausible.

In addition to the effects of the threshold voltage hysteresis, the DIBL affects the measurement conducted in the context of this work. The measurements shown in Figure 9.7 are conducted with the drain and gate contacts shorted together. The measurements conducted in this work, see Figure 9.6, have a high drain-source voltage applied, lowering the threshold voltage due to the DIBL effect. The DIBL effect must be compensated in order to compare the measurements acquired here, see Figure 9.6, to those presented in [120], see Figure 9.7. Figure 9.8 shows the threshold voltage in the upward direction $U_{\mathrm{th,up}}$, extracted from the measurements conducted here, i.e., the measurements shown in Figure 9.6. The measurements are extrapolated to $U_{\mathrm{dc}} = 0\,\mathrm{V}$ with a linear regression to estimate the expected results if the gate and drain are shorted together. The extrapolation suggests a value of approximately 0.54 V at $U_{\mathrm{dc}} = 0\,\mathrm{V}$ for the setup used in this work, closely matching the results found in [120]. Using U_{dc} as a reference instead of the actually applied drain-source voltage U_{ds} is irrelevant for the extrapolation, as U_{dc} is proportional to the high level of U_{ds}. Therefore, the observed low levels of the threshold voltages in the upward direction presented in Figure 9.6 are plausible.

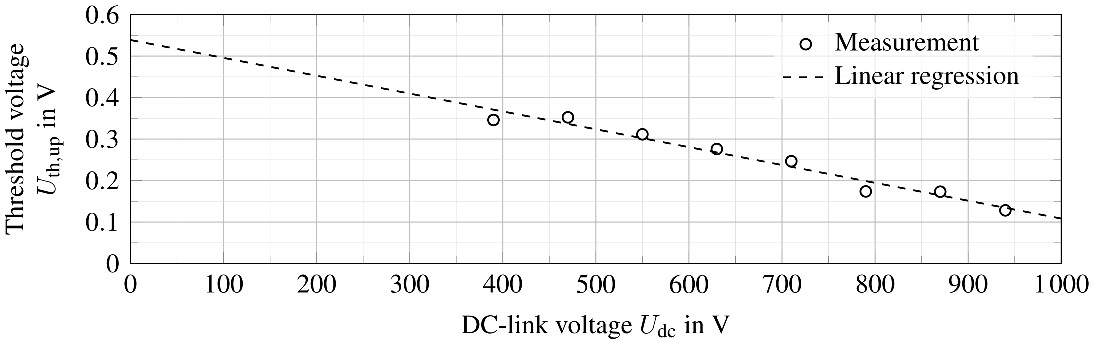

Figure 9.8: Extrapolation of the threshold voltage measurements presented in Figure 9.6 to $U_{\mathrm{dc}} = 0\,\mathrm{V}$ in order to compare against the results shown in [120]; measurements are extracted from Figure 9.6 at $\vartheta_{\mathrm{vj}} = 30\,^{\circ}\mathrm{C}$

9.2.1 Piecewise linear model

It can be seen from Figure 9.6 that the nonlinearities of the gate charge curve during turn-on can be modeled by a piecewise linear gate capacitance. The proposed linear approximation is shown in Figure 9.9. Three capacitances $C_i = \left(\frac{\mathrm{d}U_{\mathrm{g}}}{\mathrm{d}Q_{\mathrm{g}}}\right)^{-1}$ and two limits are needed to

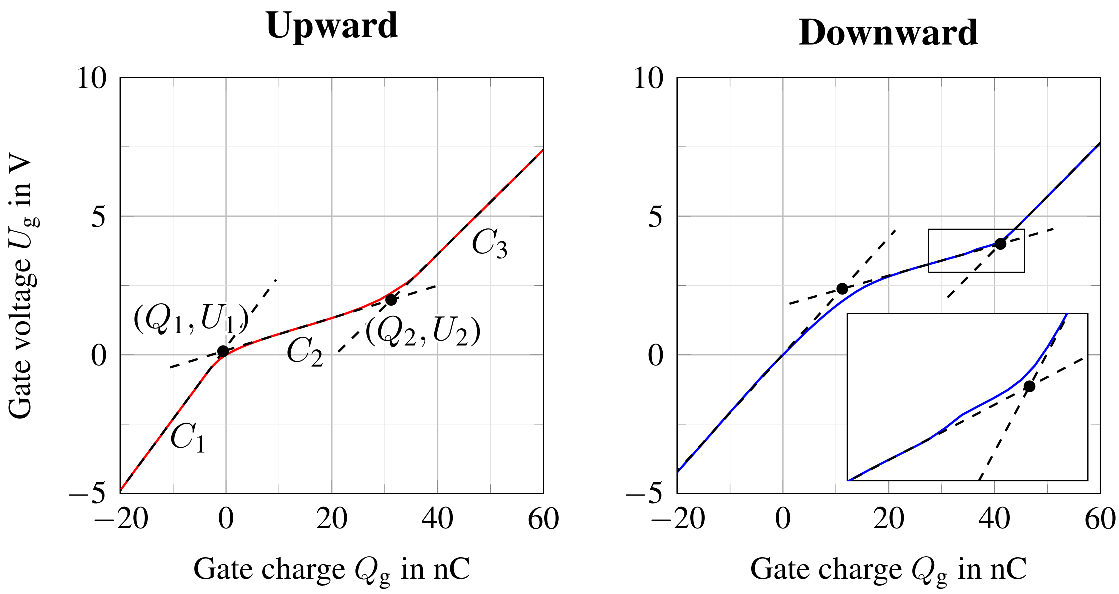

Figure 9.9: Measured gate charge curve in the upward and downward measurement directions with linear approximations at 30 °C and 940 V

define the approximation

$$U_g = \begin{cases} \dfrac{Q_g}{C_1} + U_1 - \dfrac{Q_1}{C_1} & \text{for } U_g \leq U_1, \\ \dfrac{Q_g}{C_2} + U_1 - \dfrac{Q_1}{C_2} & \text{for } U_1 < U_g \leq U_2, \\ \dfrac{Q_g}{C_3} + U_2 - \dfrac{Q_2}{C_3} & \text{for } U_g > U_2. \end{cases} \tag{9.3}$$

It should be noted that this modeled curve does not need to pass through the origin $\left(Q_g = 0\,\mathrm{C}, U_g = 0\,\mathrm{V}\right)$, as the first case transition happens close to the origin for the device under test.

> **Remark:** The voltage U_2 in the downward direction is similar to the threshold voltage in thermal equilibrium, although there are several factors contributing to U_2 being smaller than the threshold voltage given on the datasheet:
>
> - The voltage U_2 marks the intersection of the linear regressions. The voltage where the gradient of U_g begins to change is slightly higher, see the zoomed plot in Figure 9.9.
> - The fits and parameter determination for all measurements was automated. The small step in U_g when U_{ds} rises above $U_{ds} = U_g - U_{th}$ was not captured, leading to a deviation of around 50 mV, as can be seen in the zoomed plot in Figure 9.9.
> - The datasheet threshold voltage assumes the equality of U_{ds} and U_g, which is generally not fulfilled.
> - The drain current during the Miller ramp in the measurement is only $0.5\,\mathrm{mA} \leq I_d \leq 1.2\,\mathrm{mA}$, compared to the datasheet reference value of $I_d = 20\,\mathrm{mA}$.

Figure 9.10 depicts a selection of the extracted parameters needed to model the turn-on process. It can be seen that the gate capacitance C_1 below the threshold voltage shows almost no temperature dependency and only very little voltage dependency. The voltage U_1 at which the MOSFET begins to turn-on decreases with temperature and occurs at a more negative charge Q_1. The bottom graph includes U_2 for both measurement directions. The magnitude in the downward direction matches the expectations from the datasheet, except for the previously mentioned deviations.

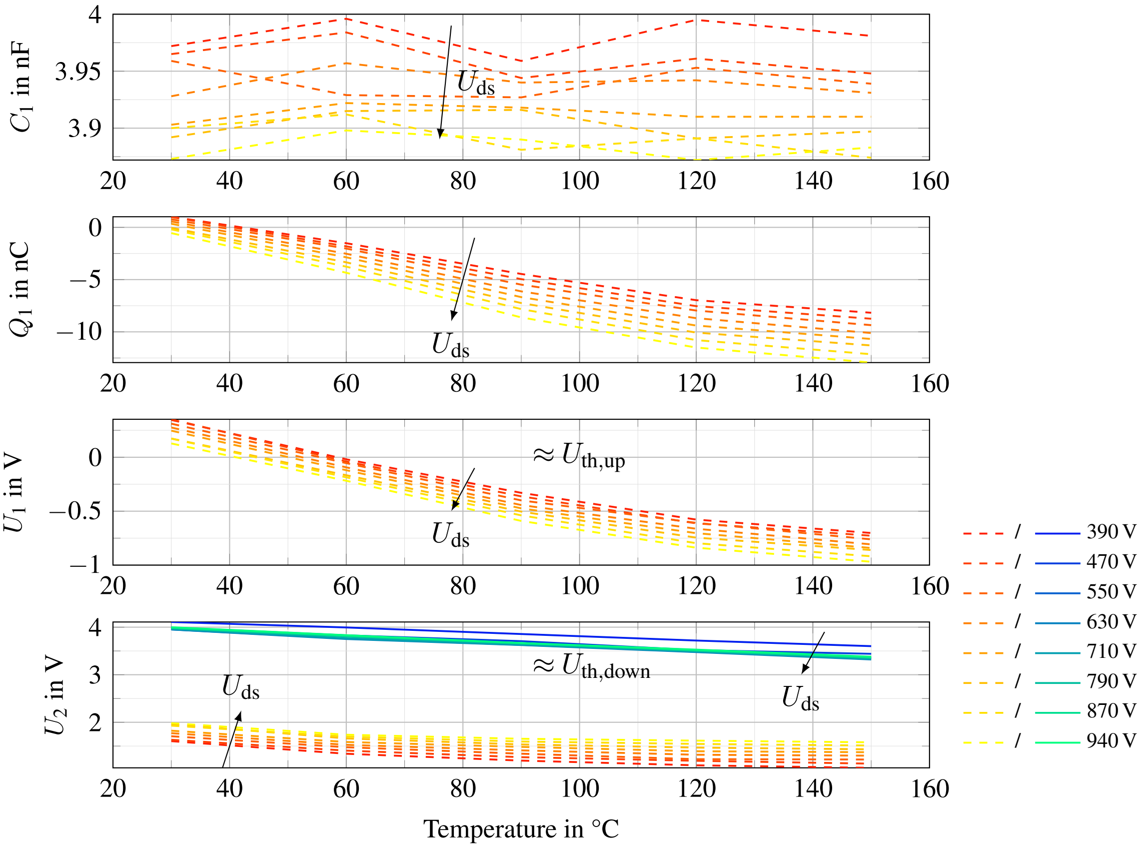

Figure 9.10: Extracted model parameters depending on the temperature and drain voltage; upward direction of the gate voltage shown as a dashed line, downward as solid

9.3 Gate loop modeling

In the previous section, the relevant semiconductor properties needed to model the turn-on process were presented. In this section, a model for the switching times t_{d} and t_{rrm} is created by including dependencies of the gate loop and the power module's structure.

During turn-on, the gate voltage is linear with regard to the gate charge before the drain voltage begins to decrease. Furthermore, the dependency on the dc-link voltage, as well as on the virtual junction temperature, is very small. The threshold voltage during turn-on $U_{\mathrm{th,up}}$ falls with an increasing temperature or dc-link voltage. In regular inverter operation, the dc-link voltage dependency will be a less significant due to the smaller dc-link voltage variation[4].

> **Remark:** The investigation of the gate charge curve was also done for IGBT modules, see [103] and Chapter 7. In that case, the slope of the gate voltage changes before reaching the threshold voltage. As a result, the turn-on process for IGBTs was modeled as a piecewise linear process with two consecutive phases. The following gate loop model is derived from the IGBT model described in [103] and adapted to an SiC MOSFET.

After reaching the threshold voltage, the MOSFET begins to turn on while its drain-source voltage stays constant[5]. This phase ends when the Miller plateau voltage, corresponding to the load current and reverse recovery current of the complementary body diode, is reached. The behavior after reaching the Miller plateau is not included in the model, as it is not required for the TSEPs considered.

Figure 9.11 shows the resulting model schematic of the gate loop during turn-on. It matches the model presented in Figure 7.8 for the gate loop modeling of the IGBT module, excluding the nonlinearity of the gate capacitance. Details of the parameters of this model were discussed in Chapter 7. In this section, the model will be extended by using semiconductor characteristics to form a temperature-dependent fit model for the measured switching times.

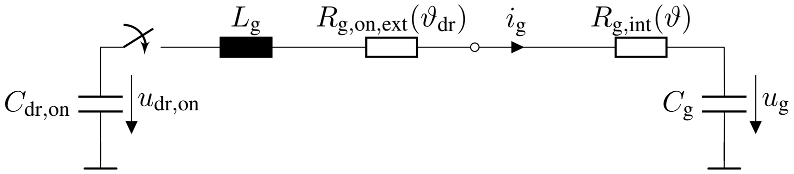

Figure 9.11: Schematic of the gate loop model during turn-on, before the drain voltage begins to decrease, adapted from Figure 7.8

Resistances The external resistor $R_{g,on,ext}$ is added to dampen oscillations during switching. For the device under test, the relevant parts of the internal resistance $R_{g,int}$ are composed of the on-chip resistances only. No additional discrete resistors are placed inside the module. While the internal resistance depends on the junction temperature, the resistance of the external gate resistor depends on the ambient temperature and load of the driver. The resistance as seen at the module terminals is the parallel resistance of two separate chips. The resistance of one chip is also dependent on the temperature distribution across the chip. Details of how the temperature distribution impacts the externally visible gate resistance will be presented in Section 9.5.

Threshold voltage Models for the threshold voltage without threshold voltage hysteresis were presented in Chapter 8. The models for the turn-on times use the same model (8.160) used for the on-state voltage. The effects of the threshold voltage hysteresis will be discussed separately in this section.

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[4] Although a typical application may reach dc-link voltage variations of ±20 %, the investigations shown in the previous section evaluated changes of $-100\,\%$ to $+18\,\%$ at a nominal dc-link voltage of 800 V.

[5] Assuming an inductive load

Current rise time During the current rise, a voltage approximately equal to the dc-link voltage is applied between the drain-source terminals. The gate needs to be charged until the saturation current of the MOSFET matches the load current

$$i_{\mathrm{d}} \overset{!}{=} I_{\mathrm{L}} = \frac{K}{2} \left(U_{\mathrm{M}} - U_{\mathrm{th}}(\vartheta, U_{\mathrm{ds}})\right)^2 \tag{9.4}$$

$$\Leftrightarrow \quad U_{\mathrm{M}} = \sqrt{\frac{2I_{\mathrm{L}}}{K}} + U_{\mathrm{th}}(\vartheta, U_{\mathrm{ds}})\,. \tag{9.5}$$

Generally, a dependency of the Miller plateau voltage U_{M} on the drain-source voltage U_{ds} is expected. The DIBL affects the threshold voltage of the MOSFET and thereby the Miller plateau voltage, see Section 9.1.1

$$U_{\mathrm{M}} = \sqrt{\frac{2I_{\mathrm{L}}}{K}} + U_{\mathrm{th},0}(\vartheta) + \lambda_{\mathrm{DIBL}}(\vartheta)\, U_{\mathrm{ds}}, \quad \lambda_{\mathrm{DIBL}} < 0. \tag{9.6}$$

As an indirect effect, this could also introduce a dependency on the current slope, as the current slope during turn-on causes the drain voltage to drop due to the stray inductance in the commutation loop. The transconductance K is proportional to the carrier mobility (8.22)

$$K \propto \mu_{\mathrm{n,ch}}(\vartheta)\,. \tag{9.7}$$

Technically, the nonlinearity of the gate capacitance would also affect the transconductance, see Section 8.1.3. As these effects can be approximated by a constant factor (8.89), they can be neglected here.

In [136], it is shown that the DIBL effect increases with temperature for DMOSFETs, which does not match the data presented in Figure 9.2. The precise characteristic should differ for different MOSFET structures and therefore cannot be directly transferred to a trench MOSFET [132, 133].

Threshold voltage hysteresis Generally, one would assume that a lower negative gate voltage would lead to longer turn-on delay times, as a larger voltage difference must be overcome in order to reach the threshold voltage. In [139, 140], it is shown that for a lower gate driver voltage, the turn-on delay time of an SiC MOSFET can actually be shorter. In this case, the turn-on delay time at $U_{\mathrm{dr,off}} = -10\,\mathrm{V}$ is approximately 15 ns shorter than at $U_{\mathrm{dr,off}} = -5\,\mathrm{V}$. The longer time needed for the gate voltage to rise from $U_{\mathrm{dr,off}}$ is offset by the effects of the reduced threshold voltage $U_{\mathrm{th,up}}$.

The behavior measured in [139] was determined using a module of the same type as the one used in this work, but with twice as many chips. Also, a larger external gate resistance $R_{\mathrm{g,pub}}$ is used in the publication. Scaling the time delay $t_{\mathrm{d,pub}}$ proportionally from [139] to fit the test setup used in this work provides a rough estimate for the expected impact

$$\frac{\partial t_{\mathrm{d}}}{\partial U_{\mathrm{dr,off}}} \approx \frac{\Delta t_{\mathrm{d,pub}}}{\Delta U_{\mathrm{g,pub}}} \cdot \frac{R_{\mathrm{g,tb}}}{R_{\mathrm{g,pub}}} \cdot \frac{n_{\mathrm{chips,tb}}}{n_{\mathrm{chips,pub}}} \tag{9.8}$$

$$= \frac{15\,\mathrm{ns}}{5\,\mathrm{V}} \cdot \frac{1.5\,\Omega + 2\,\Omega}{20\,\Omega + 1\,\Omega} \cdot \frac{2}{4} \tag{9.9}$$

$$= 250\,\frac{\mathrm{ps}}{\mathrm{V}}. \tag{9.10}$$

In the following section, the internal resistance of the gate driver used in this work will be estimated to be $R_{\mathrm{dr}} \approx 0.8\,\Omega$, but the value is unknown for the setup presented in [139]. Assuming that the gate driver resistance employed in [139] is not significantly higher, the actual sensitivity of the turn-on delay time t_{d} to the negative gate driver voltage $U_{\mathrm{dr,off}}$ will be slightly higher than estimated by (9.10). Considering an observed negative gate voltage variation in the order of 60 mV, the resulting deviation caused by the level of the negative gate voltage $U_{\mathrm{dr,off}}$ in conjunction with the threshold hysteresis effect will be neglected.

Another aspect to consider in this context is the time constant of the threshold voltage hysteresis. After applying a negative voltage to the gate, the interface traps start capturing holes. Technically, the hole-trapping process cannot be described by a time constant, as the behavior cannot be described as a simple first-order system. The time-dependent behavior of the traps consists of a superposition of traps at different energy levels. The behavior of the superposition depends on the individual time constants and the state density distribution, see *capture and emission time maps* [141]. A power function[6] is proposed to approximate the threshold voltage drift over time [126].

Figure 9.12 shows the threshold voltage of a matching SiC switch at 50 kHz switching frequency. The applied negative gate driver voltage is varied. It can be seen that the time needed to reach thermal equilibrium is relevant with regard to typical switching frequencies and that the process is faster at lower negative gate voltage, as more holes accumulate in the channel.

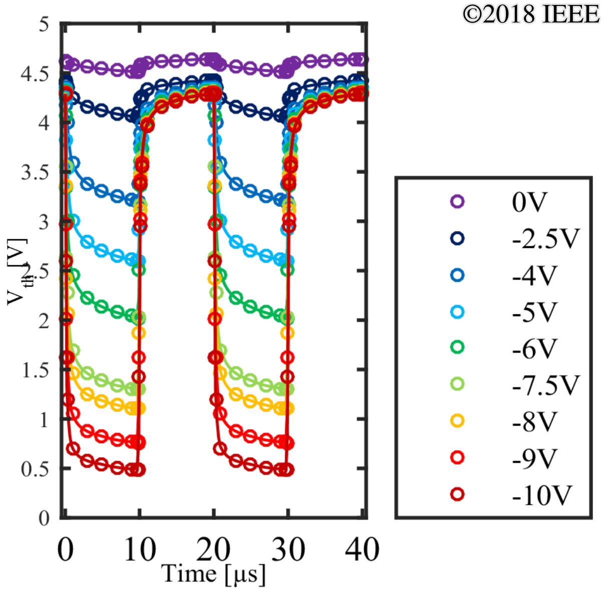

Figure 9.12: Threshold voltage plotted against time for different levels of the negative gate driver voltage [139]; negative gate voltage applied from 0 µs to 10 µs and from 20 µs to 30 µs, otherwise +15 V is applied; $u_{\mathrm{ds}} = 0.5\,\mathrm{V}$, $I_{\mathrm{d}} = 2\,\mathrm{mA}$, $\vartheta = 175\,°\mathrm{C}$; a negative gate voltage of $U_{\mathrm{dr,off}} = -5\,\mathrm{V}$ is used in this work

The TSEP calibration data used in this work is recorded after a 5 µs pulse of negative gate voltage. As can be seen in Figure 9.12, the lower level of threshold voltage hysteresis is still transient at this point. In continuous PWM operation, the duration of the off-pulse varies

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[6] $f(t) = at^b$

from 0 µs to 100 µs. Consequently, the calibration data concerning the turn-on delay time may not be directly transferable to continuous PWM operation with varying duty cycles.

The actual impact of the gate voltage hysteresis on the TSEP measurement also depends on several other factors. The TSEP circuitry and TDC cannot perfectly measure the turn-on delay time. When the threshold voltage of the device is reached, the drain current rises, inducing the voltage spike across the source inductance of the module. A certain level of this voltage is required to trigger the time measurement. The resulting trigger time delay will be discussed in Section 9.4. Thus, the gate voltage of the MOSFET has already risen at this point and the drain current is already high.

To estimate the impact of the gate voltage hysteresis on the measured turn-on delay time, these two aspects must be considered. The effects do not only depend on the threshold voltage at the beginning of the turn-on process, but also on how fast the threshold voltage recovers between turning on the MOSFET and reaching the trigger level of the measurement circuitry, see the positive voltage edge in Figure 9.12 at 10 µs. Figure 9.13 shows the measured recovery time after applying a positive gate voltage. As the recovery time at 15 V is within the order of typical turn-on delay times, the effect can be relevant for the TSEP measurement.

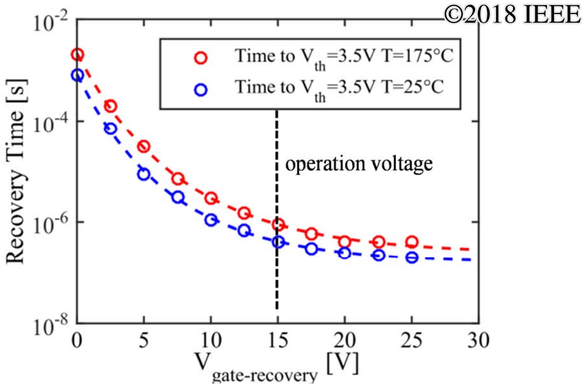

Figure 9.13: Recovery time from a −10 V negative gate voltage at different positive gate driver voltages [141]; drain current level unknown

However, the effects of the threshold voltage hysteresis are generally considered to be relevant mainly in the subthreshold region and less so at higher current levels [120]. In [142], the short circuit behavior of SiC devices is measured with different preapplied negative gate voltages. It is shown that the switching behavior changes significantly at a low positive gate driver voltage of 8 V, whereas no significant difference is measured at a high positive gate driver voltage of 18 V. All measurements are performed at very high currents, yet a significant impact of the threshold voltage hysteresis is observed at low positive gate voltage levels. Therefore, a high drain current alone does not seem to be sufficient to negate the effects of the gate voltage hysteresis. This observation is attributed to the faster recovery time at higher gate voltage levels [142].

Even though the results presented in [142] suggest only a small impact of the threshold voltage hysteresis on device operation at high driver voltages *and* high currents, comprehensive data with the required accuracy in the sub-ns range is not available.

Investigations on how the on-state voltage or the turn-on times are affected by the duration of the previous off-phase or the magnitude of the negative gate driver voltage could reveal further parasitic impacts on these TSEPs. Nevertheless, a quantified investigation of the effects of the threshold voltage hysteresis on the switching times at nominal load currents and gate driver voltages must be omitted at this point, due to the scope of this work. During continuous PWM operation, the duty cycle of the half-bridge under test will be fixed at 50 % in order to avoid possible effects caused by the time constant of the gate voltage hysteresis. Thus, these investigations should be conducted when applying the TSEPs to a typical PWM-operated inverter.

9.4 Turn-on time model components

As was done in Chapter 8 for the modeling of the on-state voltage, several aspects of the turn-on process will be listed at several levels of complexity. Afterwards, the fit accuracy using different model combinations and complexity levels will be evaluated to choose the details needed for an appropriate model of the switching times t_d and t_rrm.

Simple RC model One of the simplest models possible for modeling the turn-on process comprises a stiff voltage source $U_\mathrm{dr,on}$, a gate resistance R_g and a gate capacitance C_g only. The gate voltage against time together with the time t_RC needed to reach an arbitrary voltage U_lvl can be described by

$$u_\mathrm{g,RC}(t) = \left(U_\mathrm{dr,on} - U_\mathrm{dr,off}\right)\left(1 - e^{\frac{-t_\mathrm{RC}}{C_\mathrm{g}R_\mathrm{g}}}\right) + U_\mathrm{dr,off} \tag{9.11}$$

$$\Leftrightarrow \quad t_\mathrm{RC} = R_\mathrm{g}C_\mathrm{g}\ln\left(\frac{U_\mathrm{dr,on,0} - U_\mathrm{dr,off,0}}{U_\mathrm{dr,on,0} - U_\mathrm{lvl}}\right), \tag{9.12}$$

where $U_\mathrm{dr,on,0}$ and $U_\mathrm{dr,off,0}$ describe the gate voltages before and after turn-on.

RCL model Adding an inductance to the gate loop leads to a second-order system, see Chapter 7. Explicitly inverting the gate voltage model is not possible. For the purpose of modeling the turn-on time and the current rise time, the impact of the inductance can be modeled as a simple time delay T_delay preceding an RC model

$$t^*_\mathrm{RCL} = T_\mathrm{delay} + a_0 R_\mathrm{g}C_\mathrm{g}\ln\left(\frac{U_\mathrm{dr,on,0} - U_\mathrm{dr,off,0}}{U_\mathrm{dr,on,0} - U_\mathrm{lvl}}\right). \tag{9.13}$$

9.4.1 Trigger delay of the turn-on delay time

So far, the models presented include the semiconductor device and the gate loop only. Equation (9.13) describes the time t_RCL that is needed to reach a gate voltage of U_lvl. The analog front end used to generate the trigger signal for the time measurement requires a certain voltage U_trig on the induced voltage to be exceeded. This voltage is not reached exactly when the threshold voltage is reached, but delayed by a short time t_trig.

The additional time t_trig needed to reach a certain trigger level U_trig for the measurement system depends on the current slope waveform and the module's stray inductance [63, 97]. Combining the gate voltage waveform $u_\mathrm{g,RC}$ from (9.11), the saturation current characteristic

$I_\mathrm{d,sat}$ from (9.4), and the inductance L_ks results in

$$i_\mathrm{d} = \frac{K}{2}\left(\left(U_\mathrm{dr,on}-U_\mathrm{th}\right)\left(1-\mathrm{e}^{\frac{-t}{R_\mathrm{g}C_\mathrm{g}}}\right)\right)^2, \tag{9.14}$$

$$\frac{\mathrm{d}i_\mathrm{d}}{\mathrm{d}t} = \frac{K\left(U_\mathrm{dr,on}-U_\mathrm{th}\right)^2}{R_\mathrm{g}C_\mathrm{g}}\left(\mathrm{e}^{\frac{-t}{R_\mathrm{g}C_\mathrm{g}}}-\mathrm{e}^{\frac{-2t}{R_\mathrm{g}C_\mathrm{g}}}\right), \tag{9.15}$$

$$U_\mathrm{trig} \overset{!}{=} \frac{\mathrm{d}i_\mathrm{d}\left(t_\mathrm{trig}\right)}{\mathrm{d}t}L_\mathrm{ks} \tag{9.16}$$

$$\Rightarrow \quad t_\mathrm{trig} = R_\mathrm{g}C_\mathrm{g}\ln\left(\frac{1-\sqrt{1-4\gamma}}{2\gamma}\right), \tag{9.17}$$

$$\text{with } 0<\gamma = \frac{U_\mathrm{trig}R_\mathrm{g}C_\mathrm{g}}{L_\mathrm{ks}K\left(U_\mathrm{dr,on}-U_\mathrm{th}\right)^2} \leq \frac{1}{4}. \tag{9.18}$$

Equation (9.16) has two solutions. The solution in (9.18) corresponds to the first intersection during the rising edge of the voltage pulse. If γ rises above the upper limit listed in (9.18), the trigger level U_trig is larger than the maximum of the induced voltage pulse.

An interesting aspect of γ is the deliberate choice of a high trigger level U_trig, while staying below the maximum induced voltage in order to include the temperature dependencies of the transconductance K, the internal gate resistance $R_\mathrm{g,int}$, and the threshold voltage U_th in the turn-on delay time t_d measurement.

$$\gamma = U_\mathrm{trig}\frac{1}{L_\mathrm{ks}}\underbrace{\frac{R_\mathrm{g}C_\mathrm{g}}{K\left(U_\mathrm{dr,on}-U_\mathrm{th}\right)^2}}_{\text{semiconductor/driver properties}}, \quad g := K\left(U_\mathrm{dr,on}-U_\mathrm{th}\right)^2 \tag{9.19}$$

$$\frac{\mathrm{d}\gamma}{\mathrm{d}\vartheta_\mathrm{vj}} = \frac{\mathrm{d}\gamma}{\mathrm{d}R_\mathrm{g}}\frac{\mathrm{d}R_\mathrm{g}}{\mathrm{d}\vartheta_\mathrm{vj}} + \frac{\mathrm{d}\gamma}{\mathrm{d}g}\frac{\mathrm{d}g}{\mathrm{d}\vartheta_\mathrm{vj}}. \tag{9.20}$$

Hence, the choice of a higher trigger level can be used to increase the temperature sensitivity of this measurement, without introducing a significant load current dependency, as presented in [97].

The overall temperature sensitivity of γ depends on the device characteristics. The transfer characteristic $I_\mathrm{d,sat}\left(U_\mathrm{gs}\right)$ of the DUT is shown in Figure 9.14. The transfer characteristic

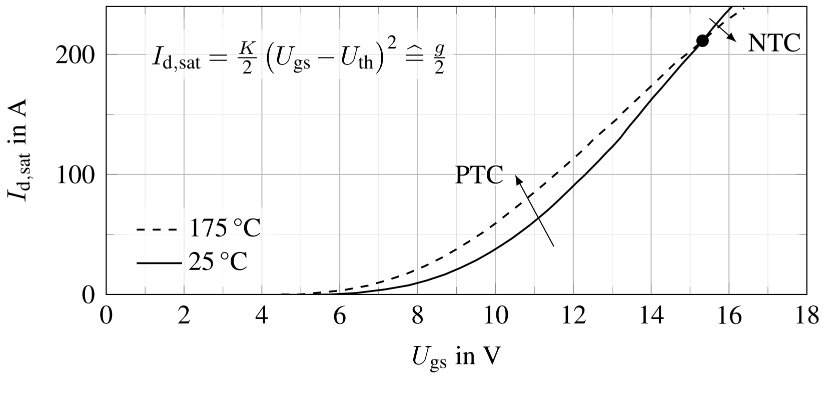

Figure 9.14: Transfer characteristic of the device under test FF23MR12W1M1B11 extracted from [124]

corresponds to $g/2$ in (9.19). Figure 9.14 shows that the denominator of (9.19) exhibits PTC behavior for $U_\mathrm{g} < 15.3\,\mathrm{V}$, counteracting the temperature dependency of the numerator [124]. A more detailed analysis of the devices transfer chararctersitic is presented in Appendix F.

With the chosen analog front end, see Figure 5.3, the trigger level U_trig of the PCB will vary proportional to the base-emitter threshold voltage of the BJT in the front end. Consequently, the measurement system would be more sensitive to the ambient temperature of the PCB. Therefore, the option of a higher trigger level is avoided and the trigger level U_trig is set as low as possible. This notwithstanding, the impact of the aforementioned semiconductor properties will still be captured inherently by the current rise time measurement.

The maximum of the current slope that can be reached is

$$\max\left(\frac{\mathrm{d}i_\mathrm{d}}{\mathrm{d}t}\right) = \frac{K\left(U_\mathrm{dr,on} - U_\mathrm{th}\right)^2}{4R_\mathrm{g}C_\mathrm{g}}, \quad \text{for } t = R_\mathrm{g}C_\mathrm{g}\ln(2)\,. \tag{9.21}$$

This would occur at a drain current of

$$i_\mathrm{d}\Big|_{\max\left(\frac{\mathrm{d}i_\mathrm{d}}{\mathrm{d}t}\right)} = \frac{K\left(U_\mathrm{dr,on} - U_\mathrm{th}\right)^2}{4} \,\widehat{=}\, \frac{I_\mathrm{d,sat}\left(U_\mathrm{g} = U_\mathrm{dr,on}\right)}{2}. \tag{9.22}$$

This current corresponds to one half of the saturation current after the device is fully turned on. Reaching this point is very unlikely during normal operation, considering the very high short-circuit currents of SiC MOSFETs. This is relevant when using the maximum of the induced voltage as a TSEP [43].

The results of the trigger delay t_trig (9.17) shown so far have been presented with regard to the semiconductor properties. For insights into the overall system, the equations will now be expanded.

Modeling the trigger delay can be simplified for low trigger voltages U_trig by relating the trigger level to the highest trigger level possible during a short-circuit event (9.21)

$$U_\mathrm{trig,max,sc} = \max\left(\frac{\mathrm{d}i_\mathrm{d}}{\mathrm{d}t}\right)L_\mathrm{ks}, \tag{9.23}$$

$$U_\mathrm{trig} \overset{!}{=} \frac{U_\mathrm{trig}}{U_\mathrm{trig,max,sc}}U_\mathrm{trig,max,sc} = \frac{U_\mathrm{trig}}{U_\mathrm{trig,max,sc}}L_\mathrm{ks}\frac{K\left(U_\mathrm{dr,on} - U_\mathrm{th}\right)^2}{4R_\mathrm{g}C_\mathrm{g}}. \tag{9.24}$$

Combining (9.24) with the definition of γ in (9.19) yields

$$\gamma = \frac{U_\mathrm{trig}}{4U_\mathrm{trig,max,sc}}. \tag{9.25}$$

This simple definition can be used to describe the trigger delay time (9.17) as

$$t_\mathrm{trig} = \underbrace{R_\mathrm{g}C_\mathrm{g}}_{:=\tau_\mathrm{g}}\ln\left(2\frac{1-\sqrt{1-\frac{U_\mathrm{trig}}{U_\mathrm{trig,max,sc}}}}{\frac{U_\mathrm{trig}}{U_\mathrm{trig,max,sc}}}\right), \quad 0 \leq \frac{U_\mathrm{trig}}{U_\mathrm{trig,max,sc}} \leq 1. \tag{9.26}$$

The resulting temperature dependency of the trigger delay is plotted in Figure 9.15. It can be seen that the trigger delay could be modeled linearly for small ratios $\frac{U_\mathrm{trig}}{U_\mathrm{trig,max,sc}}$. Considering that $U_\mathrm{trig,max,sc}$ corresponds to the maximum voltage that would occur in a short-circuit

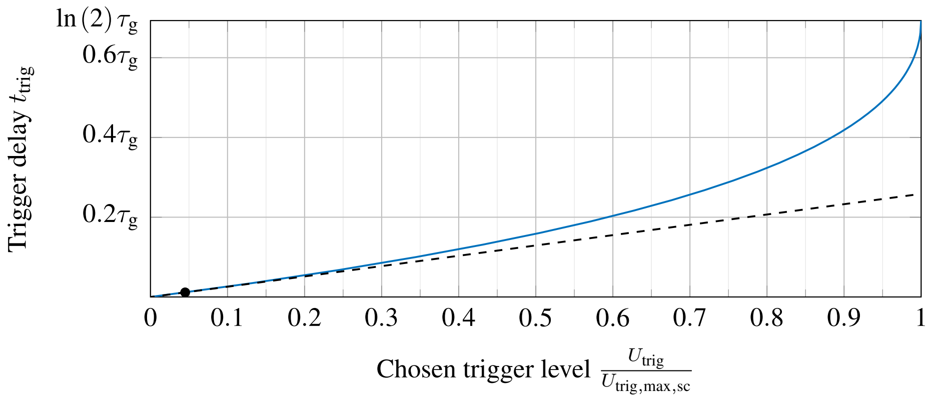

Figure 9.15: Resulting trigger delay depending on the chosen trigger level; linear approximation marked at the highest $\frac{U_{trig}}{U_{trig,max,sc}} \leq 0.043$ expected for the setup implemented

event, the ratio can be expected to be small. Even when using the maximum induced voltage $\max(u_{sk})$ at a low load current as $U_{trig,max,sc}$, see Figure 9.17 in Section 9.5, it can be estimated that the overall impact is small

$$\frac{U_{trig}}{U_{trig,max,sc}} < \frac{U_{trig}}{\max(u_{sk})} = \frac{1.4\,\mathrm{V}}{32.5\,\mathrm{V}} = 0.043 \tag{9.27}$$

$$\Leftrightarrow \quad t_{trig} < 0.011 \cdot \tau_g \approx 170\,\mathrm{ps}. \tag{9.28}$$

Of course, using the maximum induced voltage $\max(u_{sk})$ during regular operation from Figure 9.17 at a low load current instead of the maximum induced voltage during a short circuit $U_{trig,max,sc}$ significantly overestimates the effect and the trigger delay time t_{trig}.

Considering the very low temperature sensitivity of the turn-on times, even this small portion of the gate time constant can lead to deviations of several kelvin if left unaccounted for. Finally, the trigger delay time can be modeled linearly

$$t^*_{trig} = a_0 \frac{U_{trig}(\vartheta_{dr})}{U_{trig,max,sc}\left(K, \tau_g, U_{th}\right)} + a_1, \quad a_0, a_1 > 0\,\mathrm{s}. \tag{9.29}$$

9.4.2 Reverse recovery charge and overcurrent delay

The TSEP measurement circuit cannot inherently measure the current rise time of the turned-on MOSFET alone. The measurement always includes the time needed to reach the peak of the reverse recovery current, caused by the partner switch. Based on datasheet values, it can be expected that this additional elapsed time has a similar order as the current rise time itself [124]. Generally, the elapsed time changes with the load current, the current slope during turn-on, and the temperature of the body diode, or the partner switch.

Consequently, the first part of the *measured* current rise time depends on the temperature of the switch turning on, while the second part is likely to be impacted by the temperature of the complementary body diode turning off. The TSEP calibration data is acquired in double-pulse experiments at homogeneous module temperature only. During operation, the high-side and low-side switches can have different temperatures. A detailed investigation of the effects of a temperature difference between the high-side and low-side switches will be presented in Chapter 15.

Oscillations of the commutation loop, including C_{oss} of the MOSFETs, are superimposed onto reverse recovery of the body diode. During the rising edge of the overcurrent peak, the voltage across the body diode stays pinned to a very low value for the most part, before it rises during the falling edge [143]. Shortly before reaching the overcurrent peak, the body diode's forward voltage begins to rise [68], but the relative change in the drain-source voltage of the MOSFETs is low. As the output voltage of the half-bridge is not yet changing drastically, the oscillations of the commutation loop are expected to affect the switching behavior only after the TSEP measurement of the current rise time t_{ri} has been completed.

The effect of the diode turn-off can be incorporated into the model functions by adjusting the current level in the Miller plateau voltage (9.6) by using the maximum reverse recovery current I_{rrm}

$$U_{\mathrm{M}} = \sqrt{\frac{2\left(I_{\mathrm{L}} + I_{\mathrm{rrm}}\left(\vartheta_{\mathrm{DUT}}, \vartheta_{\mathrm{comp}}\right)\right)}{K(\vartheta)}} + U_{\mathrm{th},0}(\vartheta) + \lambda_{\mathrm{DIBL}}(\vartheta)\, U_{\mathrm{ds}}. \tag{9.30}$$

The maximum reverse current I_{rrm} mostly depends on the load current, the high level minority carrier lifetime and the carrier mobility [144]. Modeling the maximum reverse current I_{rrm} or the reverse recovery charge Q_{rr}, considering their temperature dependency, quickly becomes too complex for a fitting function [68, 145]. Based on [145], a simplified model of the reverse recovery charge is given by

$$Q_{\mathrm{rr}}^{*} = I_{\mathrm{L}} \tau_{\mathrm{HL},0} \left(\frac{\vartheta_{\mathrm{dut}}}{\vartheta_{\mathrm{ref}}}\right)^{a_1} + Q_{\mathrm{oss}}, \tag{9.31}$$

where Q_{oss} is the charge stored in the output capacity C_{oss} of the MOSFET. This model matches data published by the manufacturer [144] reasonably well, see Figure 9.16.

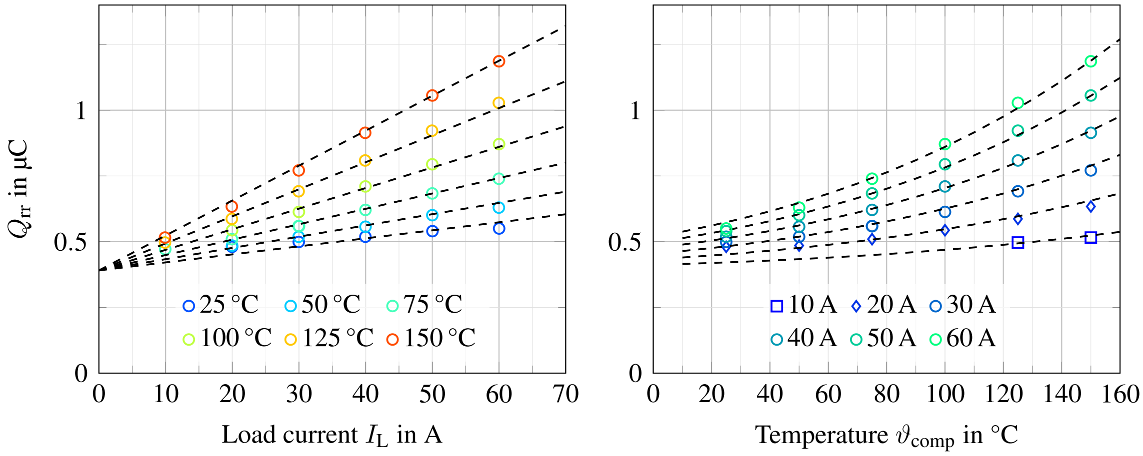

Figure 9.16: Fit model (9.31) validated with data published by the manufacturer [144]; only the body diode's temperature is varied while its switching partner was kept at a constant temperature; some data points could not be extracted at 10 A

A linear dependency on the current slope is reasonable according to the datasheet [124].

Thus, the maximum reverse recovery charge can be modeled as

$$Q_{\mathrm{rr}}^{*}=\left(I_{\mathrm{L}}a_0\left(\frac{\vartheta_{\mathrm{comp}}}{\vartheta_{\mathrm{ref}}}\right)^{a_1}\right)\left(1+a_2\frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t}\right)+Q_{\mathrm{oss}}. \tag{9.32}$$

Assuming a triangular shape of the recovery current curve, the reverse recovery charge Q_{rr} can be mapped to the peak reverse current I_{rrm}

$$I_{\mathrm{rrm}}=\frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t}\frac{t_{\mathrm{rr}}}{2},\quad I_{\mathrm{rrm}}\frac{t_{\mathrm{rr}}}{2}=Q_{\mathrm{rr}} \tag{9.33}$$

$$\Rightarrow I_{\mathrm{rrm}}=\sqrt{\frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t}Q_{\mathrm{rr}}} \tag{9.34}$$

$$\Rightarrow I_{\mathrm{rrm}}^{*}=\sqrt{\frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t}}\sqrt{\left(I_{\mathrm{L}}a_0\left(\frac{\vartheta_{\mathrm{comp}}}{\vartheta_{\mathrm{ref}}}\right)^{a_1}\right)\left(1+a_2\frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t}\right)+Q_{\mathrm{oss}}}\,. \tag{9.35}$$

Internal gate resistance The internal gate resistance R_{g} is expected to rise with temperature. The total internal gate resistance is composed of the metallic contact of the gate signal distribution above the gate insulator and the current path through the MOS channel and the p-base. Comparable studies suggest a linear temperature dependency [77]

$$R_{\mathrm{g,int}}^{*}=(a_0+a_1\vartheta)\,. \tag{9.36}$$

As it is unclear whether the dominant component in $R_{\mathrm{g,int}}$ is due to the signal distribution on top of the chip, which uses metallic conductors, or the path through the semiconductor, a mobility-based model will be investigated as well

$$R_{\mathrm{g,int}}^{*}=a_0\left(\frac{\vartheta}{\vartheta_{\mathrm{ref}}}\right)^{a_1}\,. \tag{9.37}$$

9.5 Gate loop inductance and driver resistance

In this section, the impact of the internal resistance of the gate driver on the turn-on process is estimated. In order to estimate the internal gate driver resistance, the gate loop inductance must also be determined. Therefore, this section investigates both aspects simultaneously. Additionally, the impact of the drain current feedback on the current rise time, due to the magnetic coupling between the drain-source path and the gate loop, is assessed.

The turn-on process of a module at different temperatures and at two different load currents, low and high, is plotted in Figure 9.17. The corresponding definitions are shown in Figure 9.18. Beside the fundamental temperature dependencies of u_{sk}, the temperature dependencies of the gate voltage at the module terminals $u_{\mathrm{g,t}}$, together with the output of the driver $u_{\mathrm{dr,out}}$, are also shown.

Gate terminal voltage Before the threshold voltage is reached, the gate terminal voltage $u_{\mathrm{g,t}}$ can be used to assess the temperature dependency of the internal gate resistance $R_{\mathrm{g,int}}$. If the internal gate resistance increases, the gate voltage at the terminals needs longer to rise as a result of the slower charging process. Simultaneously, the gate voltage at the terminals

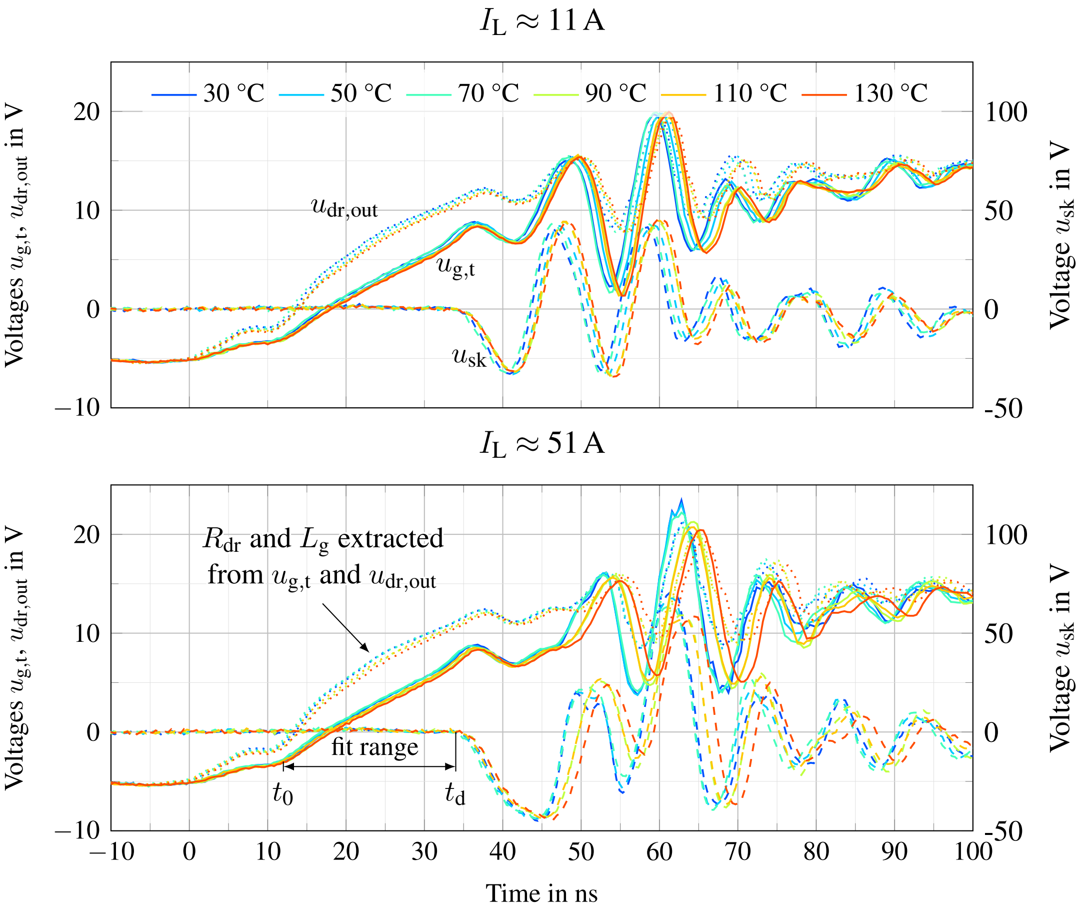

Figure 9.17: Turn-on process with gate voltage at the module terminal $u_{g,t}$, driver output $u_{dr,out}$ and induced voltage peak across the source inductance u_{sk}; voltage u_{sk} is scaled down 1:5; the load currents I_L vary between 10.5 A and 10.6 A and between 50.6 A and 50.8 A; Module M_4, LS in initial state

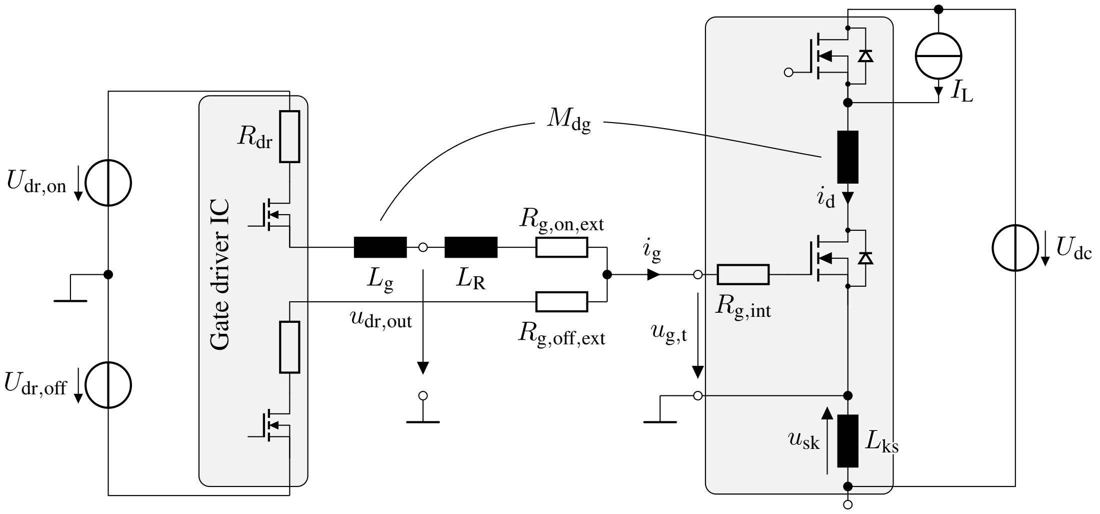

Figure 9.18: Schematic of the gate loop model used to investigate the gate loop inductance, driver resistance and the impact of the magnetic coupling between the drain current and the gate current; the gate driver's turn-off path is not considered

increases due to the additional voltage drop caused by the gate current

$$u_{\mathrm{g,t}} = U_{\mathrm{dr,off}} + \left(U_{\mathrm{dr,on}} - U_{\mathrm{dr,off}}\right)\left(1 - \mathrm{e}^{\frac{-t}{R_{\mathrm{g}}C_{\mathrm{g}}}}\right) + i_{\mathrm{g}}R_{\mathrm{g,int}}, \tag{9.38}$$

$$u_{\mathrm{g,t}} = U_{\mathrm{dr,off}} + \left(U_{\mathrm{dr,on}} - U_{\mathrm{dr,off}}\right)\left(1 - \mathrm{e}^{\frac{-t}{R_{\mathrm{g}}C_{\mathrm{g}}}}\right) + \frac{R_{\mathrm{g,int}}}{R_{\mathrm{g}}}\left(U_{\mathrm{dr,on}} - U_{\mathrm{dr,off}}\right)\mathrm{e}^{\frac{-t}{R_{\mathrm{g}}C_{\mathrm{g}}}}, \tag{9.39}$$

$$\text{with } R_{\mathrm{g}} = R_{\mathrm{g,int}} + R_{\mathrm{g,ext}} + R_{\mathrm{dr}}, \quad \text{assuming } L_{\mathrm{g}} = M_{\mathrm{dg}} = 0\,\mathrm{nH}. \tag{9.40}$$

Deriving (9.39) with respect to the internal gate resistance $R_{\mathrm{g,int}}$ is equal to deriving it with respect to the overall gate resistance R_{g}. Here, the latter leads to simpler equations, thus $R_{\mathrm{g,int}}$ is substituted by R_{g} first

$$\frac{\partial R_{\mathrm{g}}}{\partial R_{\mathrm{g,int}}} = 1 \quad \Rightarrow \quad \frac{\partial u_{\mathrm{g,t}}}{\partial R_{\mathrm{g,int}}} = \frac{\partial u_{\mathrm{g,t}}}{\partial R_{\mathrm{g}}}, \tag{9.41}$$

$$R_{\mathrm{g,int}} = R_{\mathrm{g}} - R_{\mathrm{g,ext}} - R_{\mathrm{dr}}, \tag{9.42}$$

$$u_{\mathrm{g,t}} = U_{\mathrm{dr,off}} + \left(U_{\mathrm{dr,on}} - U_{\mathrm{dr,off}}\right)\left[1 - \mathrm{e}^{\frac{-t}{R_{\mathrm{g}}C_{\mathrm{g}}}} + \frac{R_{\mathrm{g}} - R_{\mathrm{g,ext}} - R_{\mathrm{dr}}}{R_{\mathrm{g}}}\mathrm{e}^{\frac{-t}{R_{\mathrm{g}}C_{\mathrm{g}}}}\right]. \tag{9.43}$$

The gate inductance L_{g} and the magnetic coupling M_{dg} have not yet been considered. As a result, the sensitivity towards changes in the internal gate resistance $R_{\mathrm{g,int}}$ differs depending on the elapsed time

$$\frac{\partial u_{\mathrm{g,t}}}{\partial R_{\mathrm{g,int}}} = \frac{\partial u_{\mathrm{g,t}}}{\partial R_{\mathrm{g}}} = \frac{\left(U_{\mathrm{dr,on}} - U_{\mathrm{dr,off}}\right)\left(R_{\mathrm{g}} - R_{\mathrm{g,int}}\right)\overbrace{\left(R_{\mathrm{g}}C_{\mathrm{g}} - t\right)}^{\text{sign changes}}}{C_{\mathrm{g}}R_{\mathrm{g}}^{3}}\mathrm{e}^{\frac{-t}{C_{\mathrm{g}}R_{\mathrm{g}}}}, \tag{9.44}$$

$$\Rightarrow \quad \frac{\partial u_{\mathrm{g,t}}}{\partial R_{\mathrm{g,int}}} \begin{cases} > 0 & \text{for } t < R_{\mathrm{g}}C_{\mathrm{g}}, \\ < 0 & \text{for } t > R_{\mathrm{g}}C_{\mathrm{g}}, \\ = 0 & \text{for } t = R_{\mathrm{g}}C_{\mathrm{g}}. \end{cases} \tag{9.45}$$

Here, the time constant $R_{\mathrm{g}}C_{\mathrm{g}}$ occupies the range of 10 ns to 20 ns. The time period with positive sensitivity is likely to be masked by the voltage drop caused by the gate loop inductance.

Internal gate driver resistance The gate driver used has a short circuit current of 10 A at $U_{\mathrm{dr,on}} = 15\,\mathrm{V}$ [146]. The internal resistance of the gate driver can therefore be estimated to be $R_{\mathrm{dr}} \leq 1.5\,\Omega$, depending on the gate current. This places the driver resistance R_{dr} in the same range as the external gate resistance $R_{\mathrm{g,on,ext}}$ and the internal gate resistance of the module $R_{\mathrm{g,int}}$. The gate driver's output voltage $u_{\mathrm{dr,out}}$ in Figure 9.17 can be used to estimate R_{dr} and the gate loop inductance L_{g} when the following assumptions are made.

- The gate driver's supply voltage is stable during the turn-on process. This notwithstanding, the current gate driver voltage level $U_{\mathrm{dr,on}}$ is determined for the calculation before each turn-on process performed.
- The gate driver can be modeled as an ideal switch in series with a constant on-state resistance R_{dr}.
- The external gate resistor $R_{\mathrm{g,ext}}$ and the trace between the measurement locations

of $u_{\text{dr,out}}$ and $u_{\text{g,t}}$ do not include any inductance L_{R}. This assumption may lead to some deviations, depending on the relative size of L_{R} compared to the overall gate inductance L_{g}.

Although these assumptions lead to a simplified problem, the results can be used to estimate the gate driver's impact on the switching times and the gate loop inductance. Based on Figure 9.18, the positive gate driver voltage can be described as

$$U_{\text{dr,on}} = u_{\text{dr,out}} + R_{\text{dr}} i_{\text{g}} + L_{\text{g}} \frac{\mathrm{d}i_{\text{g}}}{\mathrm{d}t}, \tag{9.46}$$

$$i_{\text{g}} = \frac{u_{\text{dr,out}} - u_{\text{g,t}} - L_{\text{R}} \frac{\mathrm{d}i_{\text{g}}}{\mathrm{d}t}}{R_{\text{g,ext}}}, \quad L_{\text{R}} := 0\,\text{nH}. \tag{9.47}$$

Of course, this equation will not match the measured waveforms shown in Figure 9.17 perfectly. In each measured turn-on process, the best fit for R_{dr} and L_{g} is calculated between leaving the plateau at approximately 10 ns and reaching the turn-on delay time t_{d}, see Figure 9.17. The cost function E is defined in integrated form to reduce the impact of measurement noise

$$E' = u_{\text{dr,out}} + R_{\text{dr}} i_{\text{g}} + L_{\text{g}} \frac{\mathrm{d}i_{\text{g}}}{\mathrm{d}t} \tag{9.48}$$

$$E = \int_{t_0}^{t_{\text{d}}} \left(u_{\text{dr,out}} + R_{\text{dr}} i_{\text{g}}\right) \mathrm{d}t + L_{\text{g}} i_{\text{g}} + C, \quad C = -L_{\text{g}} i_{\text{g}}\big|_{t_0} \tag{9.49}$$

$$\left(R_{\text{dr}}, L_{\text{g}}\right) := \underset{R_{\text{dr}} \in \mathbb{R}, L_{\text{g}} \in \mathbb{R}}{\arg\min} \left(\int_{t_0}^{t_{\text{d}}} E^2 \mathrm{d}t\right). \tag{9.50}$$

Figure 9.19 shows the gate driver resistance $R_{\text{dr}} \approx 0.8\,\Omega$, estimated from approximately 20 000 turn-on process instances across eight different topological switches. The right plot

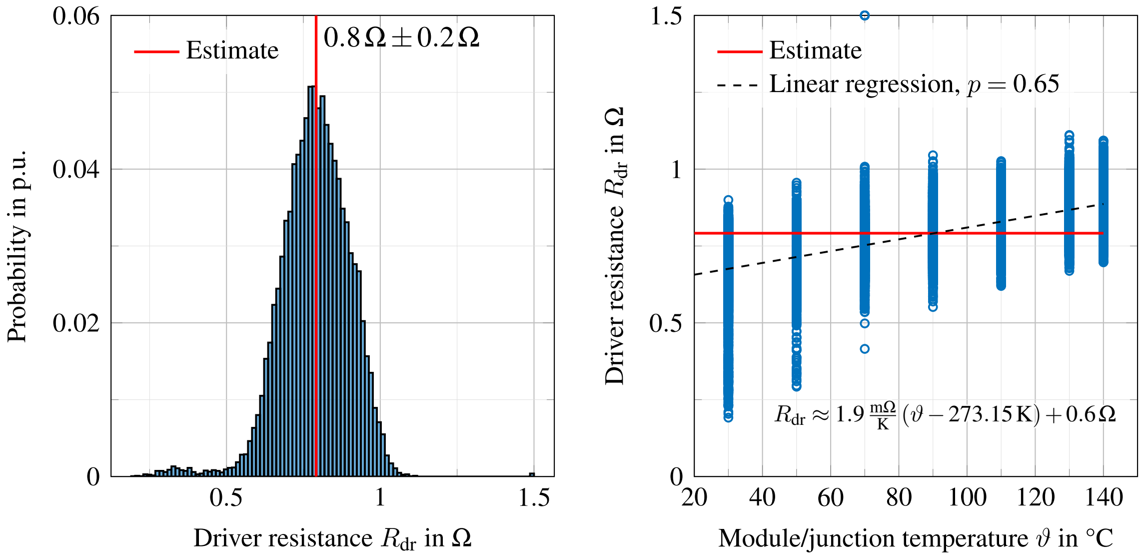

Figure 9.19: Estimated driver resistance R_{dr} and its temperature correlation based on more than 20 000 measurements across eight different topological switches; gate driver and PCB are not varied. Accuracies represent the 2.5 % to 97.5 % percentile of results; systematic errors and equipment accuracies are not included

depicts the correlation between the module's temperature during the double-pulse experiments and the estimated driver resistance. The Pearson correlation coefficient $p = 0.65$ corresponds to a moderate correlation between the module temperature and the driver resistance. This correlation is not desired and may hint at heat soaking from the module to the PCB through the module pins during the double-pulse experiments.

The same analysis is presented in Figure 9.20 for the estimated gate loop inductance $L_\mathrm{g} \approx 11.3\,\mathrm{nH}$. The inductance shows no correlation with the module's temperature, matching the expected behavior. In [71], the inductance of the gate loop inside the module is calculated to be 9.8 nH, supporting the estimated value. The largest inductance allowable to achieve at least a critically damped gate loop (7.1) is

$$\max\left(L_\mathrm{g}\right) = 18.5\,\mathrm{nH}. \tag{9.51}$$

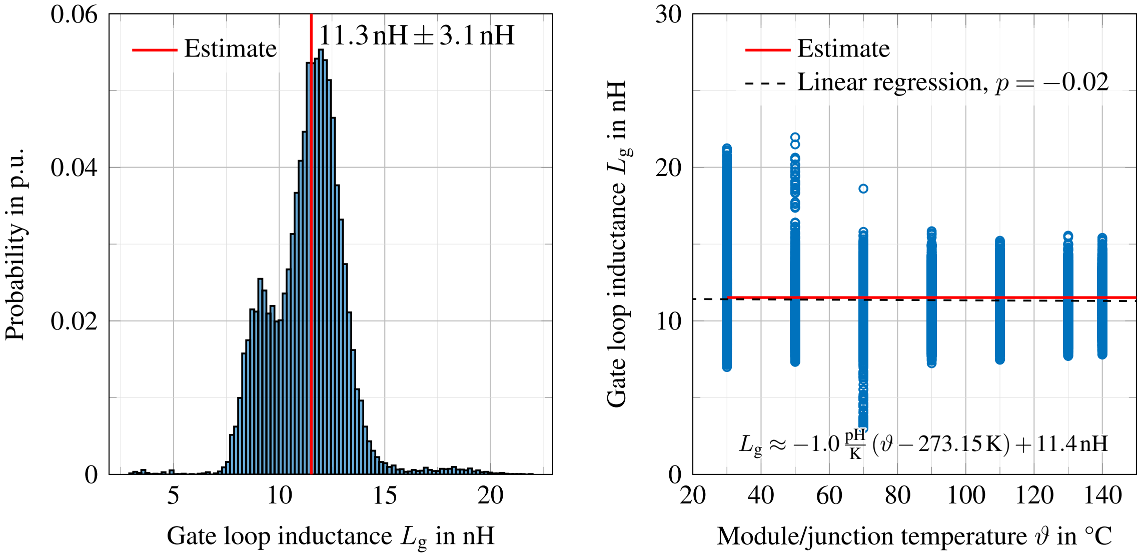

Figure 9.20: Estimated gate loop inductance L_g and its temperature correlation based on more than 20 000 measurements across eight different topological switches; gate driver and PCB are not varied; accuracies represent the 2.5 % to 97.5 % percentile of results; systematic errors or equipment accuracies not included

9.6 Drain current feedback

In this section, the impact of the drain current feedback due to the magnetic coupling M_dg between the drain-source current path and the gate loop is investigated. The differential equation of the gate loop includes an additional term

$$U_\mathrm{dr,on} = \frac{\mathrm{d}u_\mathrm{g}}{\mathrm{d}t} C_\mathrm{g} R_\mathrm{g} + M_\mathrm{dg} \frac{\mathrm{d}i_\mathrm{d}}{\mathrm{d}t} + u_\mathrm{g}. \tag{9.52}$$

The drain current can be described using the transconductance. Combined with (9.52) this yields

$$i_\mathrm{d} = \frac{K}{2}\left(u_\mathrm{g} - U_\mathrm{th}\right)^2 \tag{9.53}$$

$$\frac{\mathrm{d}i_\mathrm{d}}{\mathrm{d}t} = K\left(u_\mathrm{g} - U_\mathrm{th}\right)\frac{\mathrm{d}u_\mathrm{g}}{\mathrm{d}t} \tag{9.54}$$

$$\Rightarrow \quad U_\mathrm{dr,on} = \frac{\mathrm{d}u_\mathrm{g}}{\mathrm{d}t}\Big(\underbrace{C_\mathrm{g}R_\mathrm{g}}_{\tau_\mathrm{g}} + \underbrace{M_\mathrm{dg}K\left(u_\mathrm{g} - U_\mathrm{th}\right)}_{:=\Delta\tau_M}\Big) + u_\mathrm{g}. \tag{9.55}$$

The resulting differential equation is nonlinear. Even though the problem can be solved explicitly, this is avoided due to the complexity of the resulting function.

Instead, the additional term $\Delta\tau_M$ can be interpreted as a modulation of the expected gate loop time constant τ_g in a first-order system. In the relevant gate voltage range from U_th to U_M, the additional term $\Delta\tau_M$ can range between

$$U_\mathrm{th} \leq u_\mathrm{g}^\mathrm{(relevant)} \leq U_\mathrm{M}, \tag{9.56}$$

$$0 \leq \Delta\tau_M \leq M_\mathrm{dg}K\left(U_\mathrm{M} - U_\mathrm{th}\right). \tag{9.57}$$

Thus, minimum and maximum impacts on the switching times can be determined.

The magnetic coupling M_dg was extracted from finite-element-method (FEM) simulations of the same power module performed in [71]. Using datasheet values [147] for the transconductance K and the threshold voltage U_th, the resulting deviation range of τ_g can be estimated to be

$$\tau_\mathrm{g} = R_\mathrm{g}C_\mathrm{g} \approx 17.2\,\mathrm{ns}, \tag{9.58}$$

$$\max(\Delta\tau_M)\Big|_{u_\mathrm{g}=U_\mathrm{M}(I_\mathrm{N})} = M_\mathrm{dg}K\left(U_\mathrm{M} - U_\mathrm{th}\right). \tag{9.59}$$

The Miller plateau voltage U_M can be substituted by the nominal load current I_N using the dependency between the gate voltage and the saturation drain current (9.53), which yields

$$U_\mathrm{M} = \sqrt{\frac{2I_\mathrm{N}}{K}} + U_\mathrm{th}, \tag{9.60}$$

$$\max(\Delta\tau_M)\Big|_{u_\mathrm{g}} = M_\mathrm{dg}\sqrt{2I_\mathrm{N}K}, \approx 1.3\,\mathrm{ns} \tag{9.61}$$

$$\Rightarrow 0 < \frac{\tau_\mathrm{g} + \Delta\tau_M}{\tau_\mathrm{g}} - 1 < 8\,\%. \tag{9.62}$$

The parameters used are shown in Table 9.1. The deviation caused by the feedback from the drain current only applies during the current rise time and the error is below 8 %. Considering the low temperature dependency of the switching times, the resulting temperature error could be up to 15 K, see Appendix L.

The possible temperature deviation is significant. The investigated magnetic coupling M_dg between the drain current path and the gate current path is a fixed parameter "within" the power modul, i.e., it depends on the geometry within the module. Thus, the deviation introduced to the switching time by M_dg is constant, will be included in the initial cali-

Table 9.1: Parameters used for time constant modulation estimation

Transconductance	K	$\approx 5.6\,\frac{\mathrm{A}}{\mathrm{V}^2}$
Nominal current	I_N	$= 50\,\mathrm{A}$
Total gate resistance	R_g	$\approx 4.3\,\Omega$
Gate capacitance	C_g	$\approx 4\,\mathrm{nF}$
Magnetic coupling [71]	M_dg	$\approx 55\,\mathrm{pH}$

bration of the TSEPs and should not change significant during the useful lifetime of the module. Nevertheless, this emphasizes the severe impact a magnetic coupling between the load current and the gate loop can have on a switching-time-based temperature estimation, considering the load current flow outside the of the module. Consequently, it is essential to keep the geometry of the setup constant, i.e., fixed load current cables and fixed drivers. This also means, that the calibration of the switching times has to be done in an equivalent setup or the actual inverter setup itself.

9.7 Model comparison

In this section, multiple turn-on time model variants for t_d and t_rrm will be compared analogous to the model variants for the on-state voltage presented in Chapter 8. The measured turn-on delay t_d and the time t_rrm until the overcurrent peak is reached generally depend on the following factors:

1. a possible time delay T_delay or change in the charging time constant $R_\mathrm{g}C_\mathrm{g}$ caused by the gate loop inductance L_g,
2. the internal gate resistance $R_\mathrm{g,int}$,
3. the threshold voltage U_th,
4. a drain-induced barrier lowering λ_DIBL,
5. the transconductance K or channel mobility $\mu_\mathrm{n,ch}$,
6. the trigger delay t_trig,
7. the body diode's reverse recovery charge Q_rr.

The models[7] of the turn-on delay time t_d^* and the time t_rrm^* until the overcurrent peak models are composed of the following subcomponent models:

$$t_\mathrm{d}^* = t_\mathrm{charge}^*\left(U_\mathrm{th}^*, \tau_\mathrm{g}, U_\mathrm{dc}\right) + t_\mathrm{trig}^*\left(K^*, \tau_\mathrm{g}, U_\mathrm{th}^*\right), \tag{9.63}$$

$$t_\mathrm{rrm}^* = t_\mathrm{charge}^*\left(U_\mathrm{M}^*, U_\mathrm{th}^*, \tau_\mathrm{g}, U_\mathrm{dc}\right) + t_\mathrm{rr}^*\left(\vartheta, I_\mathrm{L}, U_\mathrm{dc}\right). \tag{9.64}$$

The trigger delay t_trig could not be included in the model of t_rrm, as no model of the current waveform during the overcurrent peak is available. Analogous to Chapter 8, several subcomponent variants must be considered, which are listed in Table 9.2. Not all subcom-

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[7] During the course of this work, all fit models of a quantity x are denoted by x^*.

Table 9.2: Model variants for different subcomponents of the turn-on times

	ID	Model	Based on
Drain-induced barrier lowering	1	$\lambda^*_{\mathrm{DIBL}} = 0$	
	2	$\lambda^*_{\mathrm{DIBL}} = \lambda_{\mathrm{DIBL}} \quad \text{(const)}$	(9.1)
	3	$\lambda^*_{\mathrm{DIBL}} = a_0\,(\vartheta - \vartheta_{\mathrm{ref}}) + a_1$	(9.1)
	4	$\lambda^*_{\mathrm{DIBL}} = a_0 \left(\frac{\vartheta}{\vartheta_{\mathrm{ref}}}\right)^{a_1}$	(9.1)
Threshold voltage	1	$U_{\mathrm{th}} = \left(U_{\mathrm{th,0}} - \beta_{\mathrm{th}}\right) e^{-\varphi_{\mathrm{th}}(\vartheta - \vartheta_{\mathrm{ref}})} + \beta_{\mathrm{th}} + \lambda^*_{\mathrm{DIBL}} U_{\mathrm{dc}}$	(8.160)
Channel mobility	1	$\mu^*_{\mathrm{n,ch}} = \mu_{\mathrm{n,ch,0}} \left(\frac{\vartheta}{\vartheta_{\mathrm{ref}}}\right)^{-r_{\mathrm{ch}}}$	(8.148)
	2	$\mu^*_{\mathrm{n,ch}} = \mu_{\mathrm{n,ch,0}} \left(\frac{\vartheta}{\vartheta_{\mathrm{ref}}}\right)^{-m_{\mathrm{ch,1}} + m_{\mathrm{ch,2}} \exp\left(-m_{\mathrm{ch,3}} \frac{\vartheta}{\vartheta_{\mathrm{ref}}}\right)}$	(8.162)
Gate time constant	1	$\tau^*_{\mathrm{g}} = a_0\,(1 + (\vartheta - \vartheta_{\mathrm{ref}})\,a_1)$	
	2	$\tau^*_{\mathrm{g}} = a_0 \left(\frac{\vartheta}{\vartheta_{\mathrm{ref}}}\right)^{a_1}$	(8.148)
Transconductance	1	$K^* = K_0 \mu^*_{\mathrm{n,ch}}$	(9.7)
Trigger delay	1	$t^*_{\mathrm{trig}} = 0$	
	2	$t^*_{\mathrm{trig}} = a_0\,(1 + (\vartheta - \vartheta_{\mathrm{ref}})\,a_1)$	(9.29)
	3	$t^*_{\mathrm{trig}} = a_0 \tau^*_{\mathrm{g}} + a_1$	(9.29)
	4	$t^*_{\mathrm{trig}} = a_0 \frac{\tau^*_{\mathrm{g}}}{K^* \left(U_{\mathrm{dr,on}} - U^*_{\mathrm{th}}\right)^2} + a_1$	(9.29)
Reverse recovery current	1	$I^*_{\mathrm{rrm}} = 0$	
	2	$I^*_{\mathrm{rrm}} = \sqrt{(a_0 I_{\mathrm{L}} + a_1) \cdot \left(\left(\frac{\vartheta}{\vartheta_{\mathrm{ref}}}\right)^{a_1} I_{\mathrm{L}} + Q_{\mathrm{oss}}\right)}$	(9.35)
	3	$I^*_{\mathrm{rrm}} = \sqrt{(a_0 I_{\mathrm{L}} + a_1) \cdot \left(\left(\frac{\vartheta}{\vartheta_{\mathrm{ref}}}\right)^{a_1} I_{\mathrm{L}}^{a_2} + Q_{\mathrm{oss}}\right)}$	(9.35)
Miller plateau voltage	1	$U^*_{\mathrm{M}} = \sqrt{\frac{2(I_{\mathrm{L}} + I^*_{\mathrm{rrm}})}{K^*}} + U^*_{\mathrm{th}}$	(9.30)
Charge time	1	$t^*_{\mathrm{charge}} = \tau^*_{\mathrm{g}} \ln\left(\frac{U_{\mathrm{dr,on}} - U_{\mathrm{dr,off}}}{U_{\mathrm{dr,on}} - U^*_{\mathrm{M}}}\right)$	(9.12)
	2	$t^*_{\mathrm{charge}} = \tau^*_{\mathrm{g}} \ln\left(\frac{U_{\mathrm{dr,on}} - U_{\mathrm{dr,off}}}{U_{\mathrm{dr,on}} - U^*_{\mathrm{M}}}\right) + T_{\mathrm{delay}}$	(9.13)

ponent variants listed in Table 9.2 are used in the models (9.63) and (9.64). The total number of model variants is 96, resulting from the different combinations of subcomponent model variants. Unfortunately, the fit results were not satisfactory and are not shown here. Most of the model variants resulted in RMSDs larger than the standard deviation of the measured data for t_{rrm} itself. Thus, the fits are less accurate than simply approximating the entire data with a constant. Consequently, these model variants cannot be validated with the acquired experimental data.

There are several possible causes for this.

1. The subcomponent models are faulty.
2. A significant influence was not considered and modeled.
3. An implementation error occurred.
4. The fit parameters were not initialized well enough to find a sufficiently small local minimum.
5. The measured data is not accurate enough to capture the modeled effects well enough, i.e., the measurement noise conceals small changes with temperature.
6. Several temperature and current sensitivities cancel each other out and the combined sensitivity of the effects is too small to be measured.

Reason 6 is unlikely, as the measured switching times can be fitted linearly with an RMSD of approximately 0.5 ns, which is significantly lower than the data's standard deviation of $\sigma \approx 25\,\mathrm{ns}$. The fit results will be shown at the end of this section. As the model variants could not be validated with experimental measurement data, a simplified approach must be applied. Reason 5 is assumed to be the most likely, due to the high noise levels seen in the data.

Nonlinearity of the calibration data In order to test whether any model behavior more complex than linear can be justified by the data, each available calibration data set was fitted with a curved surface for t_{rrm}

$$t^{*}_{\mathrm{rrm}} = t_0 + a_{\mathrm{I}} I_{\mathrm{L}}^{\alpha_{\mathrm{I}}} + a_{\vartheta} \vartheta^{\alpha_{\vartheta}}. \tag{9.65}$$

The time t_{rrm} until the overcurrent peak is reached was chosen for this investigation, as the turn-on delay time generally shows almost no current or temperature dependency. For a plane, both exponents α_{I} and α_{ϑ} would equal one. This test demonstrates whether nonlinear behavior of t_{rrm} could be identified at all with the given signal-to-noise ratio.

The resulting distributions of the exponents α_{I} and α_{ϑ} are plotted in Figure 9.21. The graphs on the right depict the fitted exponents for each topological switch using a different color or marker. Each switch was measured in up to four different stages of its expected lifetime. The results vary significantly, even for a single topological switch calibrated at different stages of its lifetime. As even this very simple modeling approach does not yield coherent results, even for a single topological switch, it is assumed that the accuracy or precision of the measured calibration data is not small[8] enough to validate the models, see Reason 5.

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[8] fine or sufficiently accurate

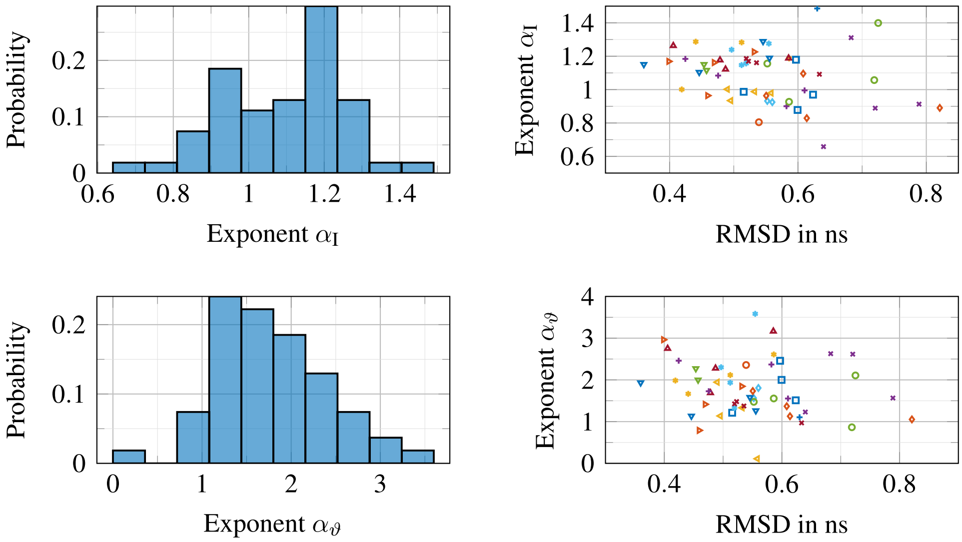

Figure 9.21: Resulting exponents for the temperature and current dependencies applied to 54 double-pulse calibration data sets; based on 14 topological switches; acquired at different stages of aging

Analysis of variance For further insight into the causes of the deviations, the root-mean-square deviations achieved by the fit together with the fitted exponents for current and temperature are depicted in an analysis of variance (ANOVA) shown in Figure 9.22. The data is categorized based on different factors that are suspected to lead to the varying results. If the chosen categorization is, or correlates with, the root cause, the variance within the subgroup should be smaller than the overall variance and the interquartile range could change.

Here, the fit results are grouped by module, by switch side or by aging level. The fit performance (RMSD) and exponents vary from module to module.

The measurements on the high side are generally more accurate than the low-side measurements. This matches the observations made regarding the on-state voltage measurement in Chapter 8. As the circuitry for the time measurement and on-state voltage measurement are independent of each other, EMI caused by the laboratory equipment attached only to the low side becomes more likely as the root cause[9].

The variance of the achieved RMSD does not change noteworthy depending on the age. Therefore, the aging of the device does not seem to impact the fit performance.

Simple linear plane approach An important aspect to consider is that even if the models employed lead to a good RMSD of the fit, this could solely be caused by a better fit to the measurement noise. The RMSD fit results achieved using the curved surface (9.65) compared to a plane are shown in Figure 9.23.

$$t^*_\mathrm{rrm} = t_0 + a_\mathrm{I} I_\mathrm{L} + a_\mathrm{T} T. \tag{9.66}$$

It can be seen that the two approaches lead to comparable median fit accuracy and comparable general RMSD distributions. At this point, a less complex model is preferred to avoid overfitting the problem and including too much noise. All further investigations will use a simple plane as the fit model for the switching times. Using a linear dependency for each

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[9] e.g., common-mode currents rushing through the probes and oscilloscope

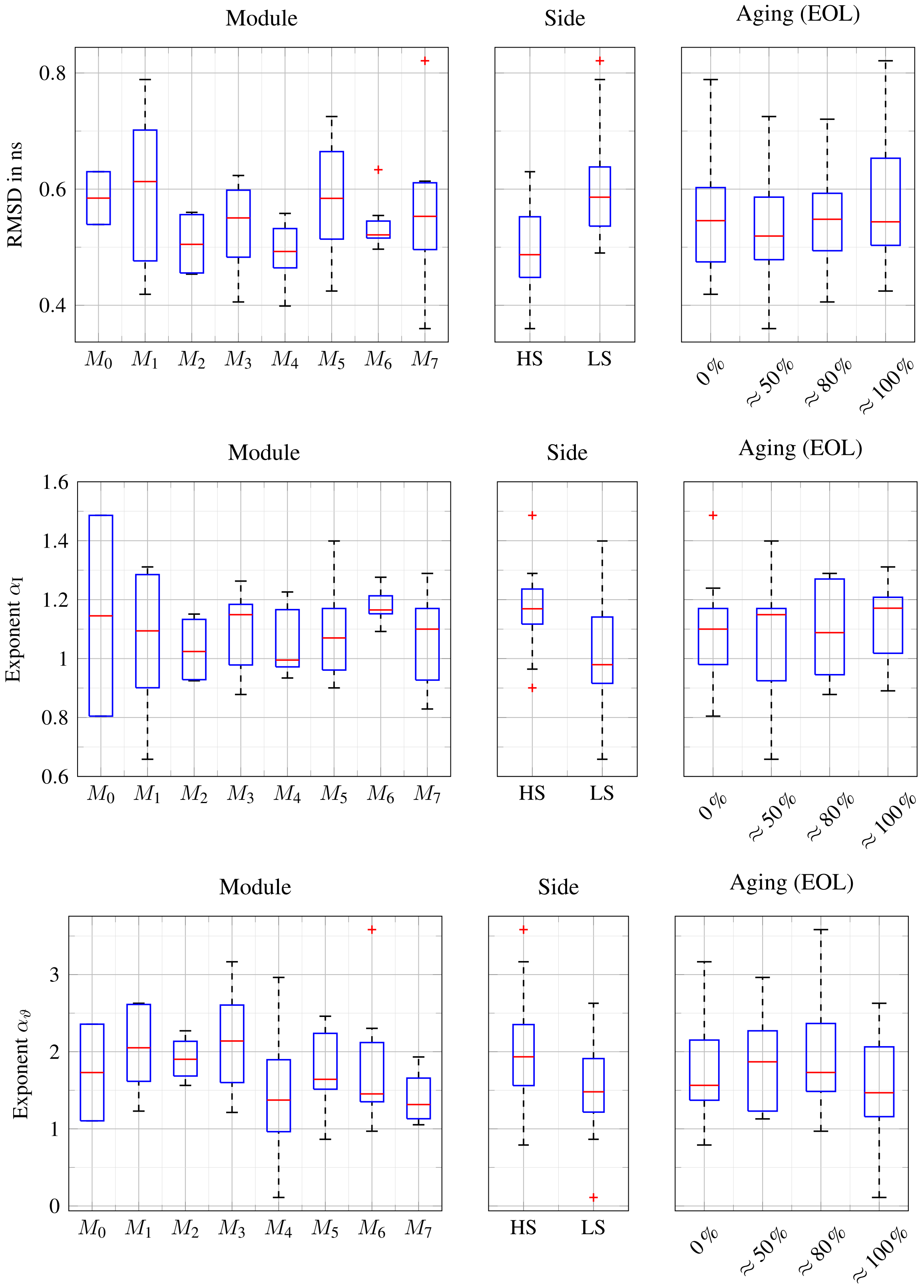

Figure 9.22: Fit performance and exponents when grouping the results by different aspects

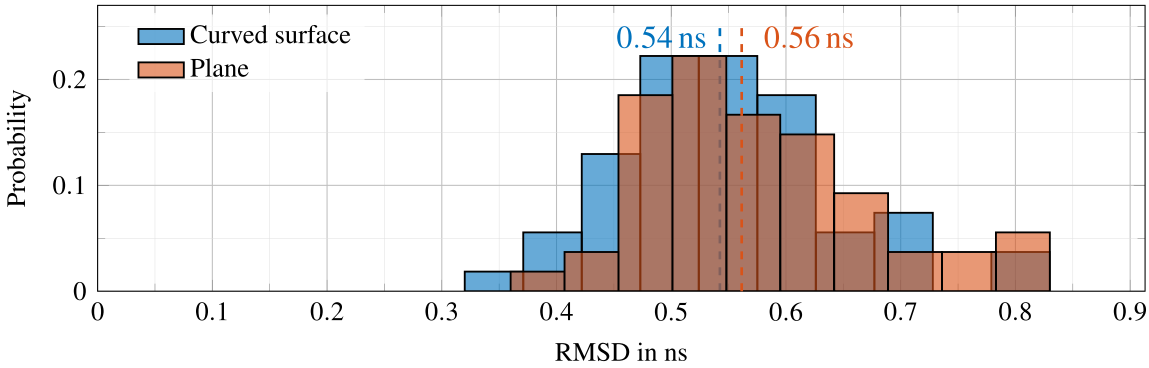

Figure 9.23: RMSD achieved using a linear model and a power-law model; median RMSD marked by dashed lines

dimension leads to a median RMSD of 0.56 ns.

Figure 9.24 shows measured data for two edge cases (switches) that resulted in highest exponent α_ϑ and one close to one. Comparing these two fit results shows no clearly preferable exponent α_ϑ, which supports the conclusion that the measured data is too inaccurate to justify the use of one model over another. More detailed plots can be found in Appendix L.

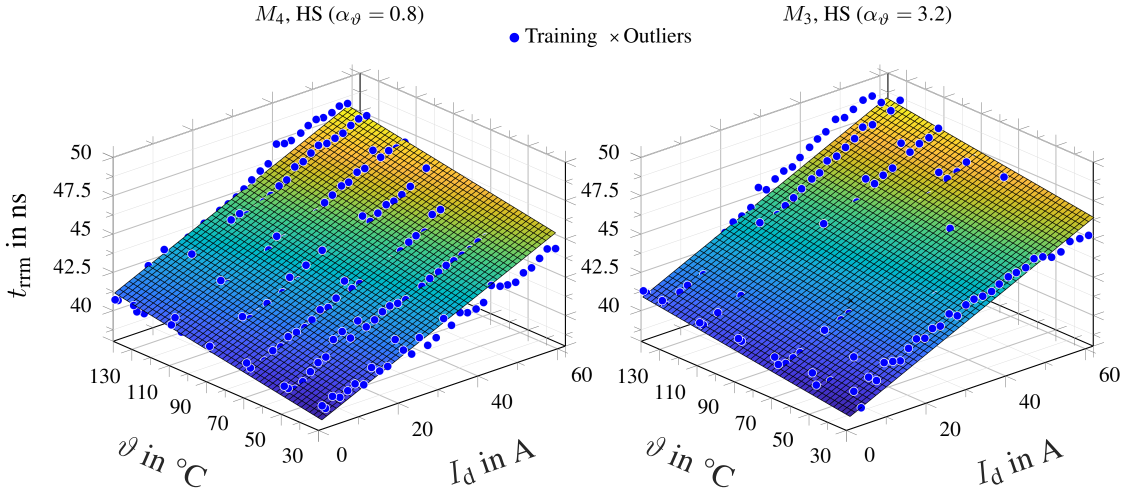

Figure 9.24: Example of the linear fit for the calibration data set with the smallest and largest exponent α_ϑ of the temperature dependency

Summary of the switching time model Modeling the switching times during turn-on requires an accurate representation of both the semiconductor properties and the gate loop. Detailed models of the threshold voltage and the gate capacitance were formed. The gate loop was modeled including the gate loop inductance.

The models have been fitted to the available TSEP calibration data from eight modules. The fits showed that the measurement noise of the switching times acquired here is too large to assess the suitability of different model complexities or even justify the use of any models more complex than a linear trend with temperature and current.

In the rest of this work, a simple linear model will be used for the switching times if needed.

Part IV

TSEP measurement system for SiC MOSFETs

10 TSEP measurement hardware for SiC MOSFETs

Most concepts of the measurement hardware needed to acquire TSEPs have been presented in Part II for the IGBT setup. In this chapter, further implementation details will be discussed for the specific application to fast-switching SiC MOSFETs.

An overview of the implemented TSEP measurement system and the half-bridge laboratory setup is shown in Figure 10.1. The acquisition of the on-state voltage $U_{\mathrm{ds,virt}}$ is more complex for SiC devices and will be discussed in Section 10.1. Only half-bridge HB2 is equipped with a TSEP measurement system. The module is mounted onto a high-power liquid cooler with a controlled fluid temperature ϑ_{a}. Half-bridge HB1 solely exists for regulating the load current i_{L} and has no measurement hardware equipment.

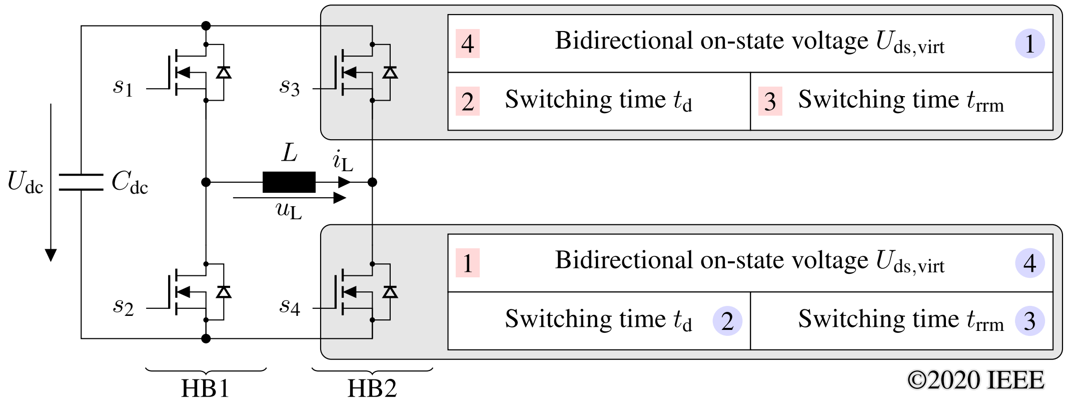

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Figure 10.1: Concept of the implemented TSEP measurement hardware and laboratory setup [99]; measurement sequence for the high side turning on in light red rectangles, for the low side in light blue circles

The top view of the TSEP measurement system is depicted in Figure 10.2. The measurement system is mounted on top of an SiC MOSFET module with brass solder-in sockets, see Figure 10.3. This contacting method allows repeated dismounting and remounting of the TSEP measurements system, even though the module uses single-use press-fit contacts. During the tests, several power modules will be analyzed, meaning the module used as HB2 will change. Figure 10.4 shows the TSEP measurement system mounted on a heat plate, which is the test bench for the double-pulse experiments.

The PWM test bench uses a liquid cooler. Seven modules are mounted on the cooler and the TSEP measurement system is moved from module to module for characterization. Figure 10.5 shows the liquid cooler with the modules and the TSEP measurement system.

The power module contains two chip per topological switch. The opened power module and the chip locations are shown in Figure 10.6.

Figure 10.7 shows the fundamental design aspects of one gate driver and the corresponding switch of the power module. Based on the findings in Chapter 7, a bipolar voltage supply

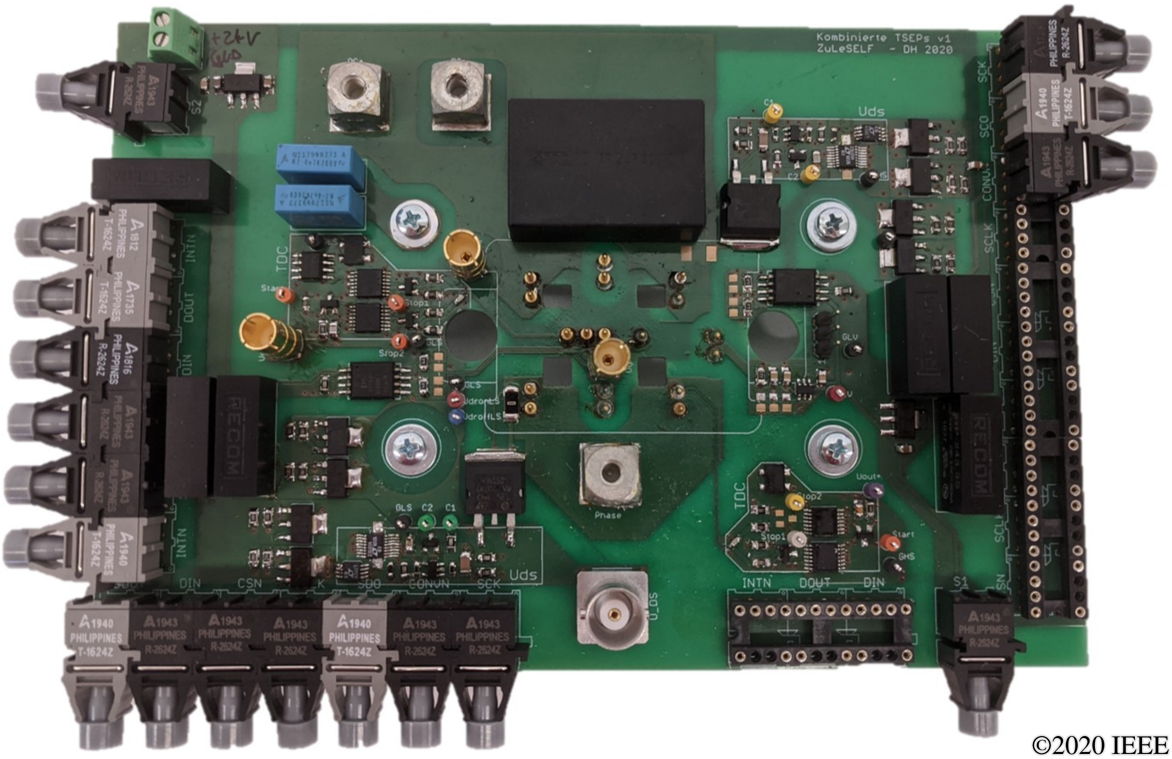

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Figure 10.2: Top view of the TSEP measurement system [67]

with a common ground reference was chosen. This improves the gate driver voltage stability compared to the commercial setup used in Chapter 7. For the laboratory setup, a base supply voltage of ±24 V was chosen and regulated to the desired voltage levels with a (low-dropout) linear voltage regulator (LDO). This improves the controllability of the supply rails for further investigations.

All measurements were done with the Kelvin source of the module as ground reference. The relevant voltages and currents are defined in Figure 10.7.

Table 10.1 summarizes key parameters of the power module under test and Table 10.2 summarizes the default parameters of the operation of the full-bridge setup, the gate drivers and the PWM modulation.

> **Remark:** Each switch in the power module is composed of two paralleled chips that are assumed to be identical to the chip used in the MOSFET IMZ120R045M1 [124], whose datasheet contains more details.

The duty cycle limits are not relevant for the laboratory setup, as the half-bridge under test HB2 is operated at a fixed duty cycle of $d_2 = 50\,\%$. Nevertheless, duty cycle limits must be chosen as a design limit for the on-state voltage measurement. If the conduction phase of a switch gets shorter, the measurement becomes unfeasible. With the chosen limits, the on-state voltage measurement must be conducted in less than 5 µs.

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[1] Assumes a thermal interface material between the case and heat sink according to the datasheet [147].

[2] Insertion inductance to the commutation loop for a load current switching between DC+ and DC- or vice versa.

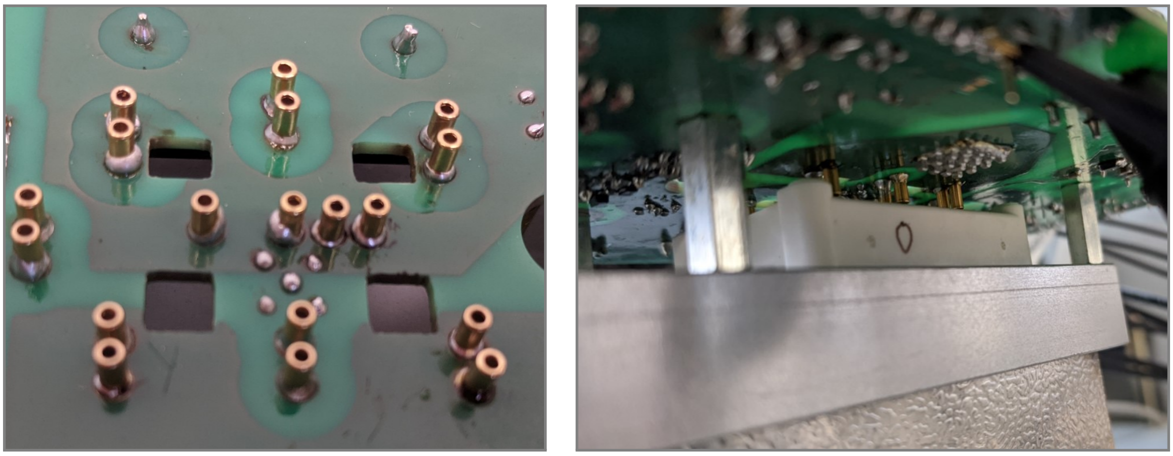

Figure 10.3: Module contacts on the PCB (left) and the TSEP measurement system mounted to a module on a heat plate (right)

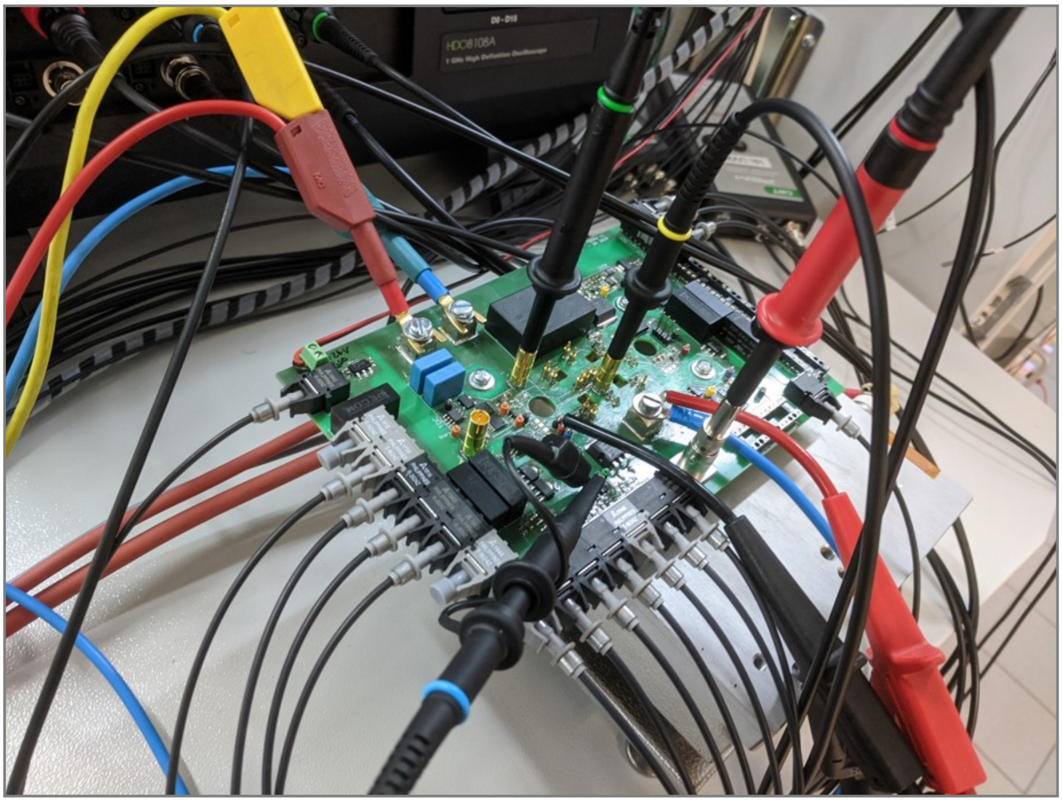

Figure 10.4: TSEP measurement system mounted to the a heat plate with probes attached

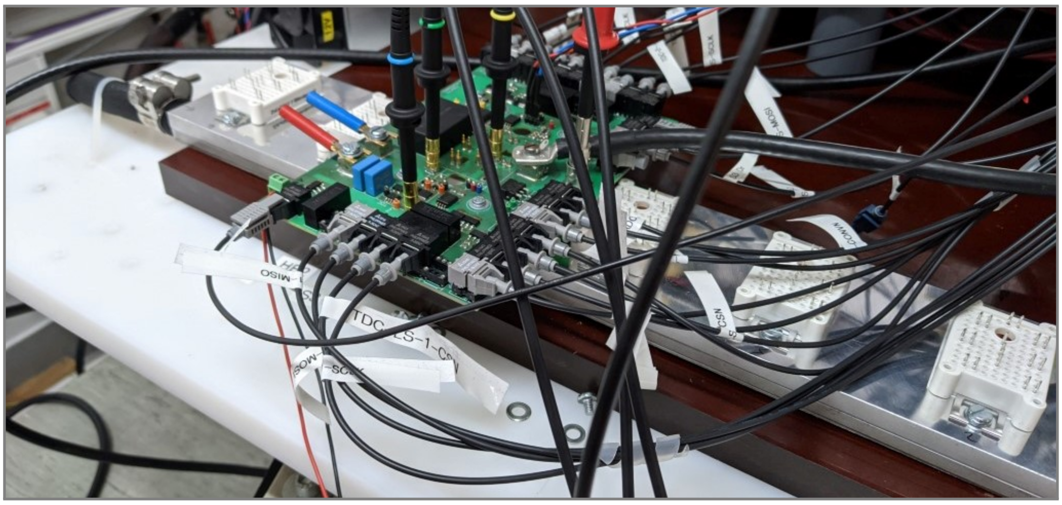

Figure 10.5: TSEP measurement system mounted on a module on the liquid cooler; HB1 not shown

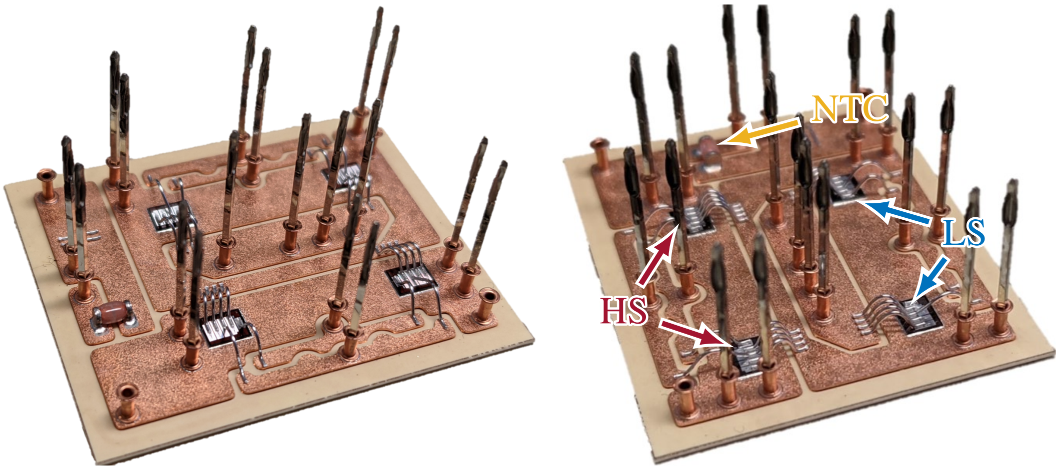

Figure 10.6: Opened power module with the silicone gel removed, showing chip locations and NTC placement

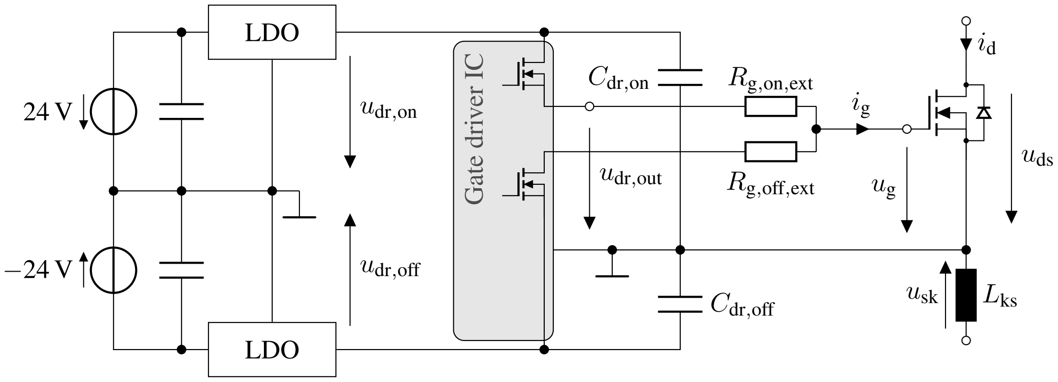

Figure 10.7: Driver design with stabilized gate driver voltages; SiC MOSFET of the power module on the right-hand side

Table 10.1: Key parameters of the power module under test FF23MR12W1M1B11 [147]; only the typical value is listed, for ranges see the datasheet

Nominal current	I_N	50 A
Breakdown voltage	U_br	1200 V
On-state resistance (25 °C)	$R_\mathrm{ds,on}$	23 mΩ
Threshold voltage	U_th	4.5 V
Internal gate resistance	$R_\mathrm{g,int}$	2 Ω
Max. virtual junction temperature during operation	$\vartheta_\mathrm{vj,max}$	150 °C
Thermal resistance, junction to heat sink[1]	$R_\mathrm{th,jh}$	0.8 $\frac{\mathrm{K}}{\mathrm{W}}$
Input capacitance	C_iss	3.68 nF
Output capacitance	C_oss	220 pF
Short circuit current	$I_\mathrm{d,sat}$	420 A
DC body diode current	I_sd	16 A
Body diode forward voltage (25 °C, 50 A)	U_f	4.6 V
Module stray inductance[2]	L_ds	9 nH
Transconductance (25 °C), see Appendix F	K	5.6 $\frac{\mathrm{A}}{\mathrm{V}^2}$

Table 10.2: Default parameters of the full-bridge setup and drivers

DC-link capacitance	C_dc	5 µF	Pos. driver voltage	$U_\mathrm{dr,on}$	15 V
Load inductance	L	225 µH	Neg. driver voltage	$U_\mathrm{dr,off}$	−5 V
Fluid temperature	ϑ_a	60 °C	Turn-on gate resistor	$R_\mathrm{g,on,ext}$	1.5 Ω
DC-link voltage	U_dc	800 V	Turn-off gate resistor	$R_\mathrm{g,off,ext}$	3.3 Ω
Switching frequency[3]	f_pwm	10 kHz	Pos. gate driver capacitance	$C_\mathrm{dr,on}$	14.1 µF
Interlock time[4]	T_D	300 ns	Neg. gate driver capacitance	$C_\mathrm{dr,off}$	14.1 µF
Duty cycle limits	$d \in (5\,\%, 95\,\%)$				

Modulation	Symmetrical, single-edged PWM; triangular carrier [148]
Voltage output	Unipolar voltage output; HB2 fixed at $d_2 = 50\,\%$
Gate Driver IC	Infineon EiceDRIVER 1EDI60H12AH [149]
ADC	LTC2310-14, 15 bit true bipolar input, sampling frequency of $2 \cdot 10^6\ \frac{1}{\mathrm{s}}$ [5] [150]
TDC	TDC7200, 55 ps resolution [98]

10.1 TSEP measurement sequence

The measurement of the four TSEPs t_d, t_rrm, $U_\mathrm{ds,on}^{(\mathrm{LS})}$ and $U_\mathrm{ds,on}^{(\mathrm{HS})}$ generally matches the descriptions in Part II. Measuring the switching times of SiC devices is more challenging due to the shorter switching times, greater current slopes and greater voltage slopes. The switching time measurement will use the voltage pulse induced across the module's parasitic inductance between the Kelvin source and source terminal u_sk. These contacts are all available on the PCB of the TSEP measurement system.

The on-state voltage must be acquired in a shorter time than for Si devices, due to the shorter conduction phases at the increased switching frequency of 10 kHz. Sufficiently fast ADCs are generally available. Unfortunately, the on-state voltage of the SiC MOSFETs is superimposed by oscillations caused by the commutation loop. All double-pulse experiments are conducted with 5 µs for the freewheeling period and the second pulse. This matches the worst case for the on and off times a switch may have during continuous PWM operation according to Table 10.2.

Figure 10.8 illustrates the entire TSEP acquisition sequence for the low-side switch in a double-pulse experiment. The switching signal of the half-bridge HB2 is defined as

$$s_\mathrm{HB2} = \begin{cases} 1 & \text{for } s_3 = 1 \wedge s_4 = 0, \\ -1 & \text{for } s_3 = 0 \wedge s_4 = 1, \\ 0 & \text{for } s_3 = 0 \wedge s_4 = 0. \end{cases} \tag{10.1}$$

The TSEP measurements are acquired in the following order.

1. Before the end of the freewheeling period, the on-state voltage of the high-side switch, or partner switch, is measured.
2. During turn-on, the measurements of both switching times t_d and t_rrm are taken.
3. At the beginning of the conduction phase of the second pulse, the on-state voltage of the low-side switch, or device under test, is measured.

Figure 10.9 shows measured turn-on and turn-off processes of the DUT at different temperatures and currents, extracted from the second on-pulse of double-pulse experiments. The dots marked in the drain-source voltage u_ds will be referenced later. The drain current has a pronounced reverse recovery current of one to two times the nominal current[6] as overshoot. The measurement at a low load current of 2 A leads a slow voltage rise of u_ds during turn-off, which is significantly affected by the output capacitances of the switches and the capacitance of the phase terminal to the dc link. The effect will be explained and analyzed more detailed in Chapter 11. The sum of these capacitances is referenced to as the node capacitance C_node. At turn-off, the drain voltage shows typical oscillations caused by the resonant circuit formed by the node capacitance and the commutation inductance.

Commutation loop oscillations The commutation loop oscillations must have settled before the on-state voltage measurement of the low-side switch can be acquired. During this

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[3] The switching frequency and dc-link voltage were specified by the project accompanying this work.

[4] The turn-on of a switch is delayed by T_D. The turn-off signal is issued unmodified.

[5] Operated at a sample frequency of $1.56 \cdot 10^6\ \frac{1}{\mathrm{s}}$, due to a serial peripheral interface (SPI) bus frequency limit of 50 MHz

[6] $I_\mathrm{N} = 50\,\mathrm{A}$

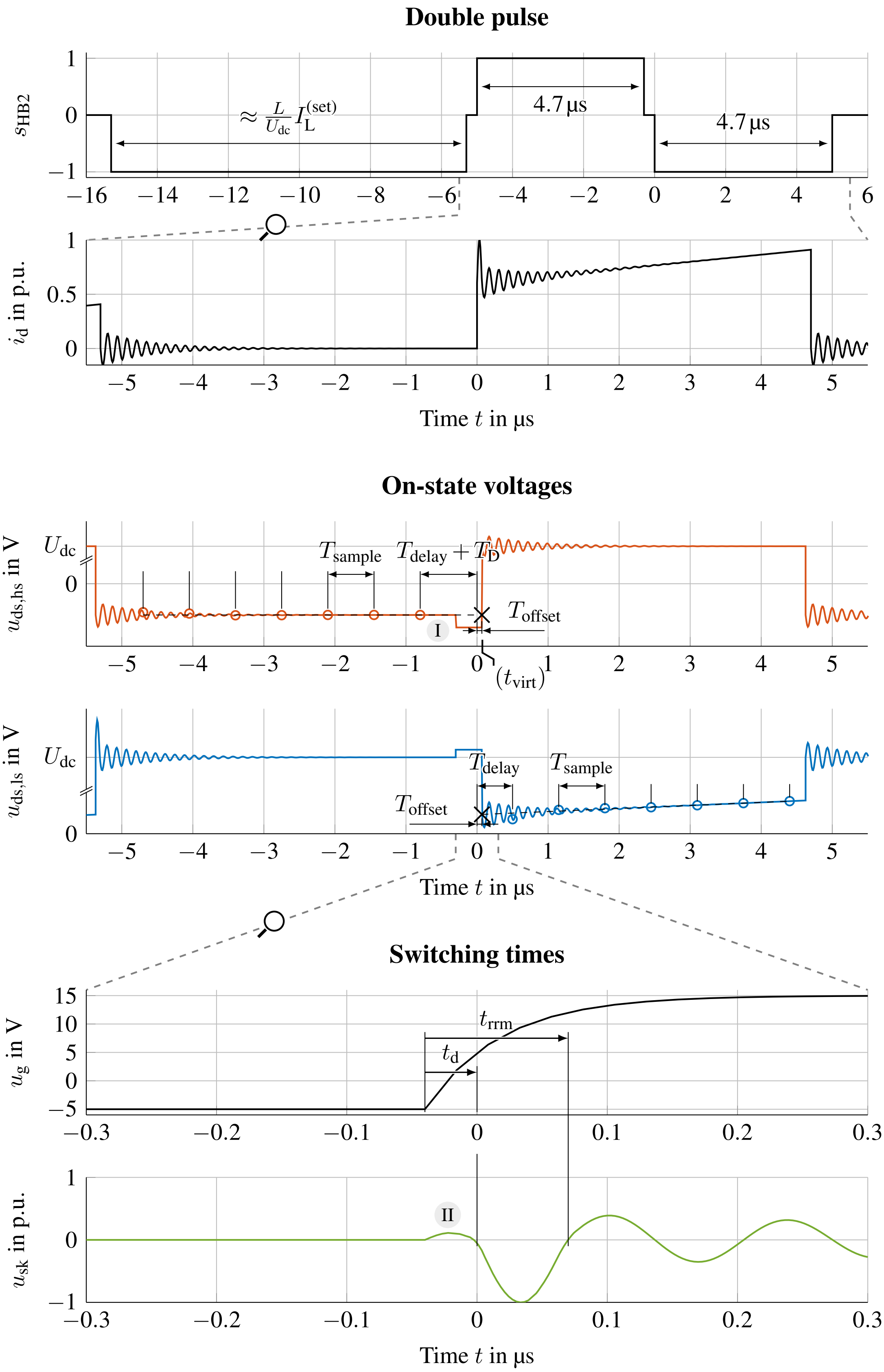

Figure 10.8: Measurement sequence during the turn-on of the low-side switch; current and voltage rise and fall times neglected; oscillations shown as illustration only

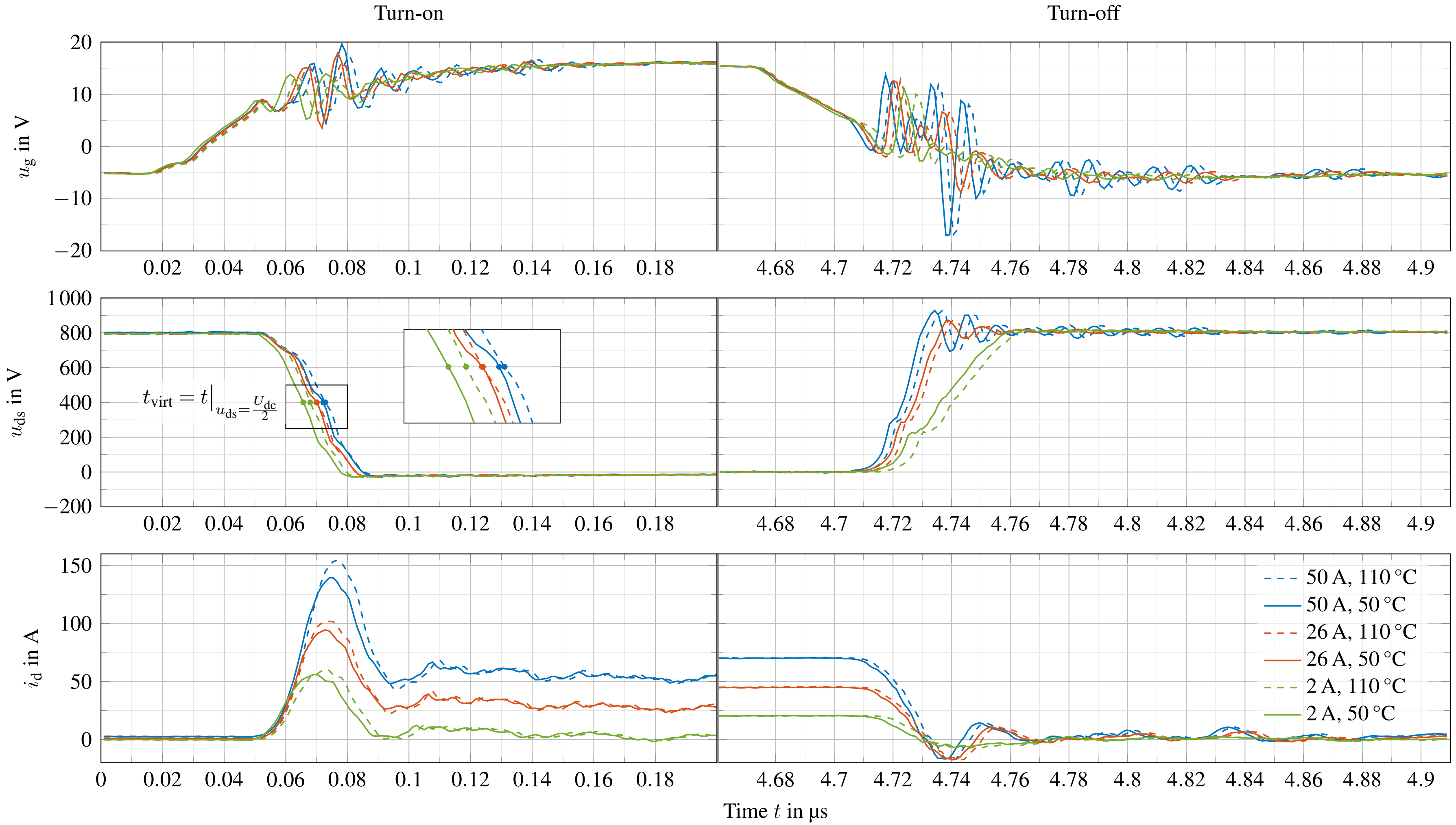

Figure 10.9: Example turn-on and turn-off processes of the DUT at different temperatures and currents; extracted from the second on-pulse of double-pulse experiments; $0.2\,\mu s < t < 4.66\,\mu s$ removed from the plot; t_{virt} definition examples marked by dots

waiting period, the load current i_L is rising, falling or staying constant, depending on the switch state of the other half-bridge, so the drain-source voltage is changing with

$$\left|\frac{\mathrm{d}u_\mathrm{ds}}{\mathrm{d}t}\right| = \left|\frac{\mathrm{d}i_\mathrm{d}}{\mathrm{d}t}\right| R_\mathrm{ds,on} \approx \begin{cases} \frac{U_\mathrm{dc}}{L} R_\mathrm{ds,on} = 81.8\,\frac{\mathrm{mV}}{\mathrm{\mu s}}, & s_\mathrm{HB1} \neq s_\mathrm{HB2}, \\ 0\,\frac{\mathrm{V}}{\mathrm{s}}, & s_\mathrm{HB1} = s_\mathrm{HB2}. \end{cases} \tag{10.2}$$

The oscillations need several micro seconds to settle. A possible load voltage increases the voltage slope for one switch and reduces it for the other. Measuring quickly after turn-on leads to noisy samples, while waiting too long lets the on-state voltage change depending on parameters that are not precisely known.

This issue is approached by the acquisition of multiple samples during the conduction phase. Assuming the voltage change of $u_\mathrm{ds,on}$ is linear, a linear regression can be used to calculate a virtual on-state voltage $U_\mathrm{ds,virt}(t_\mathrm{virt})$ at the time of turning on. As the regression is a linear least-squares problem, the result can be calculated explicitly without the need of an optimization routine on a possible real-time processing unit, see Section 4.1.

In the context of this work, the switching process is continuous and not a single point in time. Thus, a point in time t_virt has to be defined that represents the switching moment as reference. During turn-on, the drain-source voltage u_ds drops from the dc-link voltage U_dc to zero almost linearly. The center of this falling edge of u_ds during turn-on is used to define the time of turn on t_virt

$$t_\mathrm{virt} := t\Big|_{u_\mathrm{ds}=\frac{U_\mathrm{dc}}{2}}. \tag{10.3}$$

These points are marked in Figure 10.9. Details will be shown in Section 10.5.

Sample placement The last sample is placed as late as possible considering the conversion and readout times of the ADC. As many samples as feasible are placed equidistantly before the last sample with regard to the sampling frequency. The sampling interval given by the specified limits of the ADC is

$$T_\mathrm{sample} = 650\,\mathrm{ns}. \tag{10.4}$$

This allows the placement of seven ADC samples at the minimum duty cycle of 5 % that may be used for noise reduction and voltage slope compensation. An optimization of the used samples will be presented in Section 10.5. The measurement of the on-state of the switching partner in reverse direction before switching is done in the same way.

10.2 Hardware structure

The implemented analog and digital hardware blocks for one switch are shown in Figure 10.10. The switching time measurements are done with two separate TDCs, even though the TDCs are capable of measuring several consecutive times. Here, the minimum distance between the two stop events, i.e., the current rise time t_ri, was below the device

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[7] The four fiber optic transceivers needed for a round-trip SPI communication introduce a propagation delay of up to 120 ns [151], while the clock period of the SPI bus is only 20 ns. A 90 ns delay compensation was implemented in the SPI master to compensate the signal propagation delay.

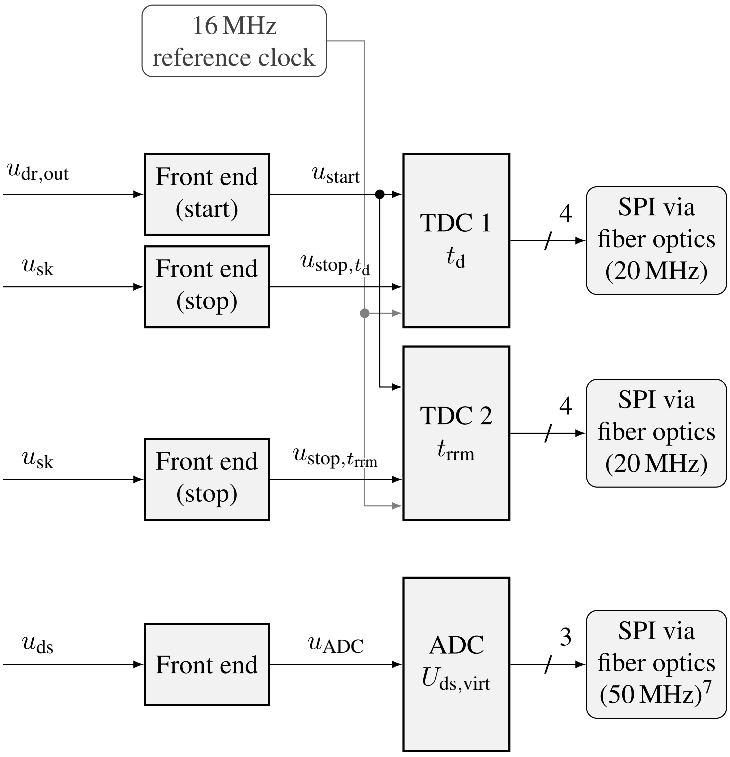

Figure 10.10: Block diagram of the TSEP measurement components implemented for each switch; for voltage definitions see Figure 10.7

specifications [98]. Better options are available, e.g., from LIDAR applications [152], but have higher cost than two TDCs from ultrasonic applications. The start trigger on CMOS level u_{start} is generated from the rising edge of driver output $u_{\text{dr,out}}$. The start trigger is supplied to both TDCs. One TDC captures the negative voltage spike on u_{sk} to measure the turn-on delay time t_d while the other TDC measures the positive voltage spike to capture t_rrm. In the laboratory setup, each IC has its own SPI bus, leading to a high number of signals to be managed and fiber optics to be used. Moving to an application, the SPI busses could be merged, reducing the total number of signals to be transmitted to six[8].

10.3 TDC front end

The new TDC configuration with two separate channels does not need a pulse train. The TDC front ends described in Part II can be simplified. They are summarized in Figure 10.11. At the beginning of the turn-on phase, a small voltage increase occurs on u_{sk} due to the gate current, see Figure 10.8, Marker II. The voltage divider at the input can be used to set the trigger level. The start trigger u_{start} and the stop trigger $u_{\text{stop},t_\text{rrm}}$ generate a falling edge, while the stop trigger $u_{\text{stop},t_\text{d}}$ has a rising edge. The output of the front ends are loaded with at least 3 pF input capacitance of the TDC.

The layout of the TDC front end is depicted in Figure 10.12. The signal path length for the voltage signal u_{sk} through the TDC front ends should be kept equal for both stop signal triggers. The reduced wave propagation speed through the dc-blocking capacitor in Figure 10.11c was not considered in the PCB layout. Figure 10.13 shows the measured

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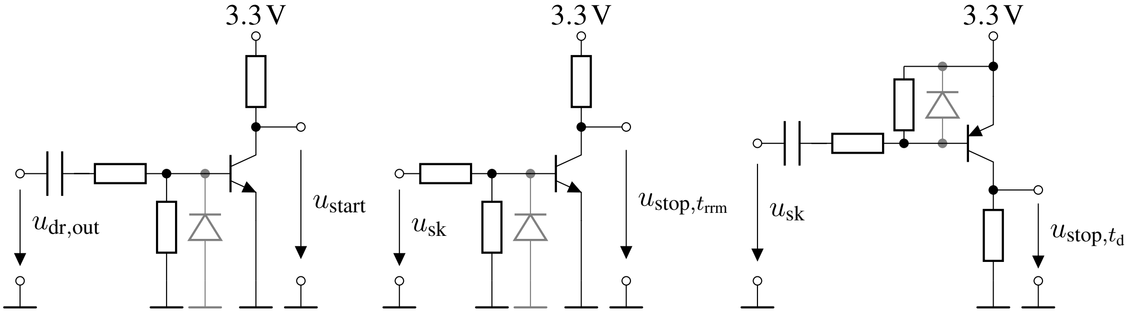
[8] SCLK, MISO, MOSI and three chip selects



(a) Start (b) Stop t_{rrm} (c) Stop t_{d}

Figure 10.11: TDC front ends; protective diode in gray; input capacitances used to decouple dc components if required

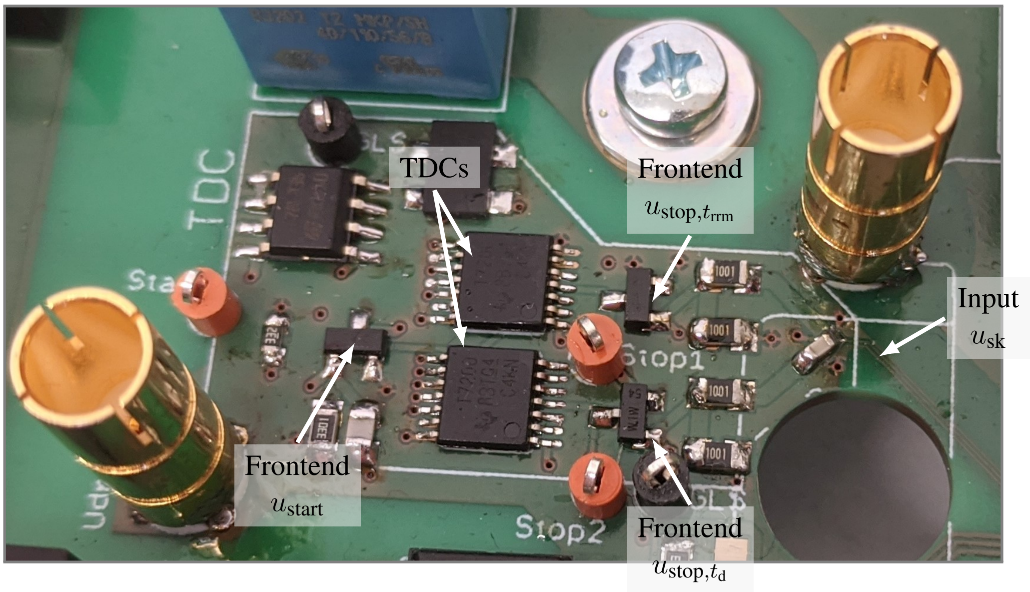


Figure 10.12: Photo of the TDC front end

trigger signals of the TDC front ends at a low load current I_{L}. A low load current is the worst-case scenario for the measurement due to smaller and shorter induced voltage pulses in u_{sk}.

The start trigger u_{start} is generated when the driver output rises. The signal has low noise, as the SiC MOSFET is not switching yet. The turn-on delay time trigger $u_{\mathrm{stop},t_{\mathrm{d}}}$ is generated from the negative pulse in u_{sk}. The trigger has a delay of approximately 4 ns. Afterwards, the measured signals are impacted by the switching transient of the SiC MOSFET via inductive and/or capacitive coupling. This is unproblematic for $u_{\mathrm{stop},t_{\mathrm{d}}}$, as the TDC ends its measurement after the trigger line has been high for 10 ns. The $u_{\mathrm{stop},t_{\mathrm{rrm}}}$ signal idles at high as designed. In the measurement shown in Figure 10.13, the falling edge of $u_{\mathrm{stop},t_{\mathrm{rrm}}}$ cannot be identified clearly, due to the EMI caused by the SiC MOSFET turning on. In fact, all measurement of t_{rrm} failed as long as the oscilloscope probes were attached. After removing the probes[9], the measurement of t_{rrm} was successful. Therefore, it is assumed that a

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[9] Teledyne LeCroy ZS1000, 1 GHz bandwidth, 0.9 pF input capacitance

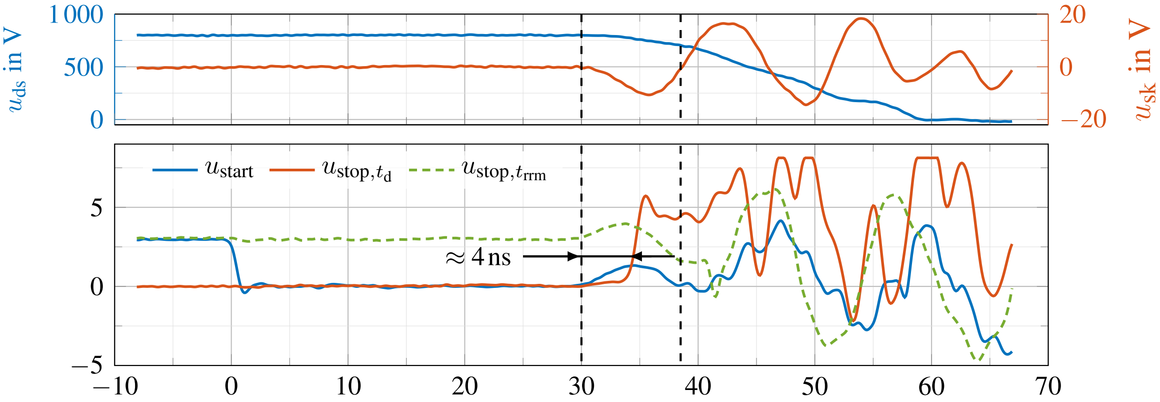

Figure 10.13: Measured TDC front-end trigger signals at a load current of $2\,A = 0.04 I_N$ [99]

relevant part of the high EMI observed here can be attributed to the measurement setup, see Appendix G. The TDC front end works as intended.

10.4 ADC front end

The ADC front end is based on the preliminary design for Si IGBTs, see Section 5.2.2. The ADC front end adapted to SiC MOSFETs is shown in Figure 10.14. A few changes have been introduced compared to the IGBT version. The active turn-off using a comparator in the signal stage was removed, as a passive limitation was sufficient and faster. The increased voltage slope of SiC MOSFETs causes an increased charging current. Reducing the size of C_1 and C_2 decreases this charging current. Additionally, the output capacities of the transistors Q_1 and Q_2 form a capacitive voltage divider with the capacitances C_1 and C_2. The corresponding crosstalk can be reduced by increasing the size of C_1 and C_2. Thus, these two aspects must be weighted against each other.

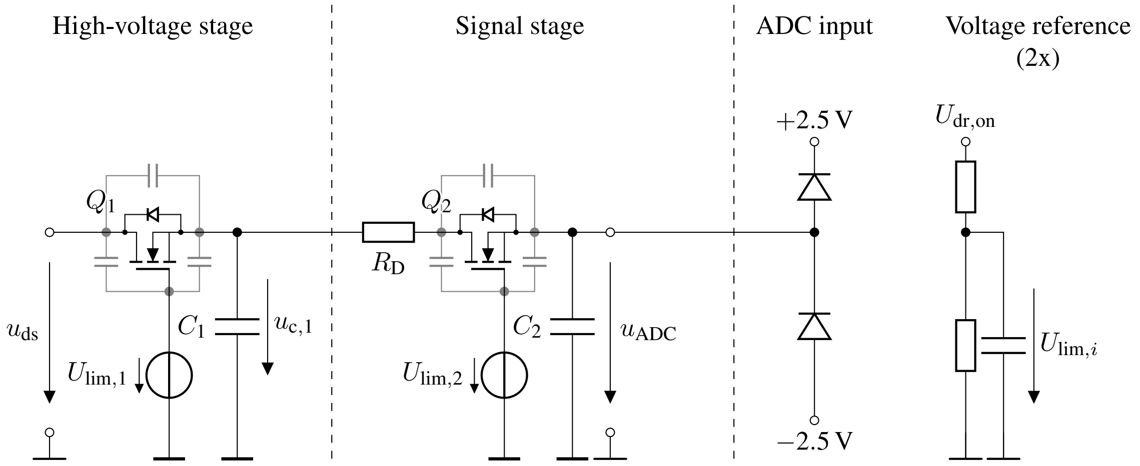

Figure 10.14: Schematic of the ADC front end [99]

10.4.1 Static behavior design

There are two critical design aspects that must be kept within the specifications of the used components. First, the SOA of the high-voltage MOSFET Q_1 allows a maximum current of 9 A. Second, the ADC's clamping diodes can withstand a 100 mA peak current without latch-up. Both limits can be breached during switching.

A passive current limiting resistor R_D is introduced to reduce both currents. The best charge current limitation could be achieved by placing R_D directly at the drain of Q_1, but this resulted in an unfeasible low-pass effect in conjunction with C_1 and C_2. Instead, R_D is placed between the first and the second limiter stage. The voltage limits $U_\mathrm{lim,1}$ and $U_\mathrm{lim,2}$ can be generated by a simple voltage divider with a large decoupling capacitor to stabilize the voltage during the transients.

Design First, the MOSFETs were chosen based on the design constraints and need an appropriately small threshold voltage and on-state resistance. The resistor, capacitances and voltage limits were chosen empirically in SPICE simulations, see Table 10.3. The minimum value for $C_2 = 47\,\mathrm{pF}$ is given by the input buffer capacitance requirement of the ADC [150]. The wide threshold range of Q_2 makes finetuning the voltage limit according to the ADC's supply limits difficult. The actual cut-off limit of the signal stage can be designed higher than the ADC's supply level to ensure nonblocking operation up to the desired upper limit. If the threshold voltage of Q_2 is small, R_D limits the current through the clamping diodes accordingly.

Table 10.3: Selected parameters of the ADC front end; note that the on-state resistances are listed for $U_\mathrm{g} = 10\,\mathrm{V}$ and are signficiantly higher at the lower gate-source voltages

C_1	C_2	$U_\mathrm{lim,1}$	$U_\mathrm{lim,2}$	R_D	Q_1	Q_2
1 nF	47 pF	9.9 V	4.9 V	10 Ω	IXTA3N150HV U_th =2.5 V to 5 V $R_\mathrm{ds,on}$ =7.3 Ω	IRLML0040TRPbF U_th =1 V to 2.5 V $R_\mathrm{ds,on}$ =56 mΩ

The static limiting behavior of the front end is shown in Figure 10.15. The residual current flowing into the analog front end at $U_\mathrm{ds} = U_\mathrm{dc} = 800\,\mathrm{V}$ was measured to be $I_\mathrm{ADC} < 3\,\mu\mathrm{A}$[10]. The ADC front end cannot block negative voltages due to the MOSFETs' Q_1 and Q_2 body diodes.

10.4.2 Dynamic behavior

The ADC front end needs to have a small low-pass filtering effect to allow the ADC voltage u_ADC to settle within the short conduction phase of the power module. The most challenging design aspect is the on-state resistance of the MOSFETs Q_1 and Q_2. They form a low-pass filter with the subsequent capacitances and their resistance changes with the voltages present at C_1 and C_2.

The frequency response of the front end was determined in SPICE simulations at different dc-voltage input levels. The results are shown in Figure 10.16. The low-pass effect is

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[10] The Ampere meter showed the smallest value it could measure.

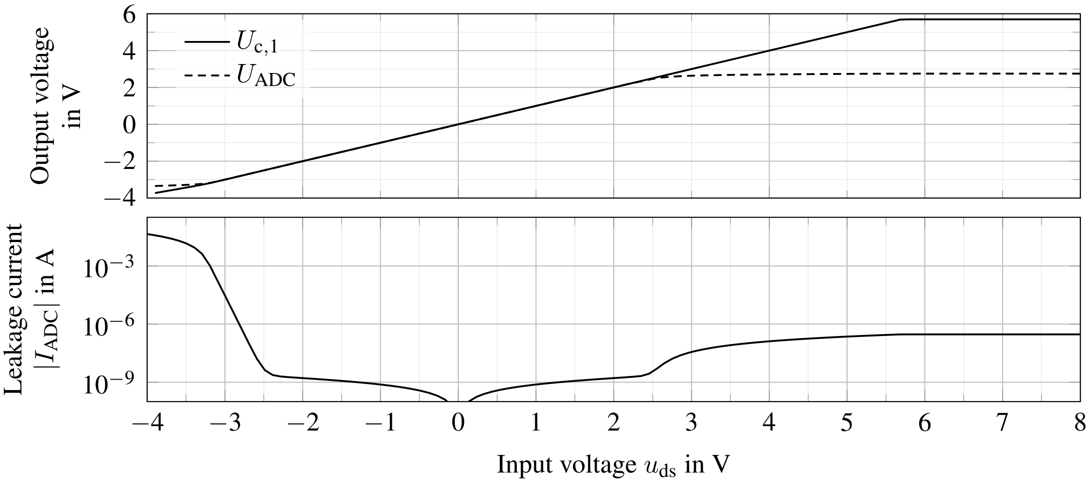

Figure 10.15: Simulated static characteristic of the ADC front-end voltage limiter

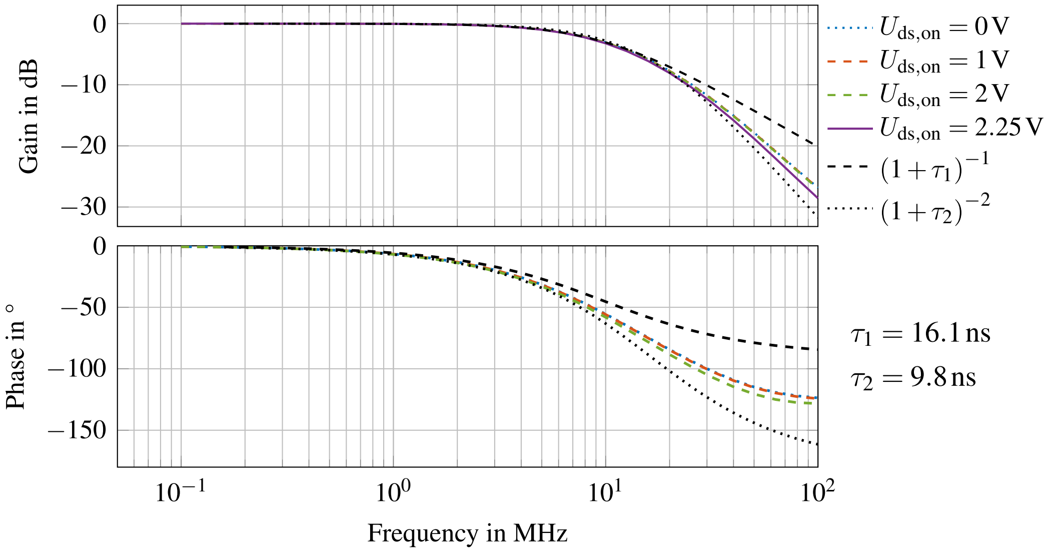

Figure 10.16: Simulated frequency response at different dc-levels $U_{ds,on}$ of u_{ds} [99]

approximated by two edge cases. A single limiter stage may be modeled as a first-order low-pass filter. Two stages can be modeled as an overdamped second-order system. Additionally, the output capacitances of the MOSFETs Q_1 and Q_2 add a feedthrough component with C_1 and C_2, lifting the phase and magnitude. Thus, the actual frequency response for a well-designed limiter is expected to be somewhere between a frist and second-order system.

The determined time constants τ_1 and τ_2 are listed in Figure 10.16, assuming the second-order system has a double pole. The two approximations envelop the actual characteristics well. They were determined such that the gain of $-3\,\text{dB}$, or $-6\,\text{dB}$ respectively, matches the simulated characteristic for low dc-voltage levels.

The ADC front end must follow a rise or fall of the on-state voltage of $81.8\,\frac{\text{mV}}{\mu\text{s}}$, see (10.2). A low-pass filter following a ramp will have a steady-state voltage offset ΔU. The voltage error of the ADC front end due to the slope of $u_{\mathrm{ds,on}}$ can be estimated to

$$\Delta U = u_{\mathrm{ds,on}} - u_{\mathrm{ADC}} \tag{10.5}$$

$$1.33\,\mathrm{mV} \approx \frac{\mathrm{d}u_{\mathrm{ds,on}}}{\mathrm{d}t} \cdot \tau_1 \leq \Delta U \leq \frac{\mathrm{d}u_{\mathrm{ds,on}}}{\mathrm{d}t} \cdot 2\tau_2 \approx 1.61\,\mathrm{mV}. \tag{10.6}$$

The resulting temperature estimation deviation at nominal current is in the order of 0.3 K. The error caused by the low-pass filtering effect is small and can be compensated to a large part, as the voltage slope is known from the samples taken, see Figure 10.8.

10.5 Current slope compensation

In the previous section, the static and dynamic behavior of the ADC front end was described. The designed front end is fast enough to follow the voltage slope of $u_{\mathrm{ds,on}}$. Furthermore, the system's behavior with regard to two other aspects must be investigated.

Shifts of the falling edge of u_{ds} First, the ADC samples are taken at fixed times, relative to the gate signal s_3 or s_4 sent to the gate driver to turn on. The time between the ADC samples and the falling edge of the drain-source voltage u_{ds} varies depending on the operating point, compare Figure 10.9. This changes the voltage-time integral applied to the load inductance, and therefore the drain current at the first samopling instant. The introduced error will be evaluated in this paragraph.

Double-pulse experiments were conducted at varying load current and temperature. The drain-source voltage was captured with an oscilloscope. In each double-pulse experiment, the time between the center of the falling edge of u_{ds} and the first sample $t_{\mathrm{sample,1}}$ was measured

$$\Delta T := t\Big|_{u_{\mathrm{ds}}=\frac{U_{\mathrm{dc}}}{2}} - t_{\mathrm{sample,1}} = T_{\mathrm{delay}} - T_{\mathrm{offset}}. \tag{10.7}$$

Figure 10.17 shows the determined time differences. It can be seen that the time between the edge in the drain-source voltage and the first sample $t_{\mathrm{sample,1}}$ varies only by ±5 ns. This

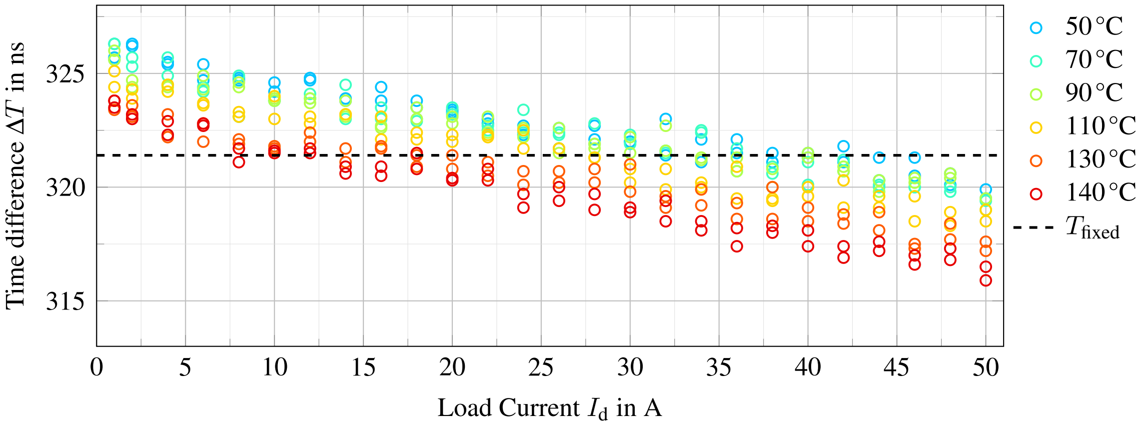

Figure 10.17: Determined delay between the falling edge of u_{ds} and the first sample [99]; approximation with a fixed time added; $U_{\mathrm{dc}} = 800\,\mathrm{V}$

time will be assumed to be constant $\Delta T = t_{\text{fixed}} = 321\,\text{ns}$. The residual error

$$\Delta I_{\text{d}} = \frac{U_{\text{dc}}}{L}\left(\Delta T - t_{\text{fixed}}\right) \approx \pm\frac{800\,\text{V}}{225\,\mu\text{H}} \cdot 5\,\text{ns} = \pm 18\,\text{mA} \tag{10.8}$$

is neglectable.

Linear regression Second, the on-state voltage slope during the conduction phase must be compensated. To investigate the effect, two sets of double-pulse experiments are recorded. One with freewheeling during the second pulse and one without. The experiment procedure is illustrated in Figure 10.18. During the second pulse, the left half-bridge is either kept in a high state or switched to a low state simultaneously. Thus, the load voltage U_{L} equals the dc-link voltage U_{dc} or is zero during the second pulse.

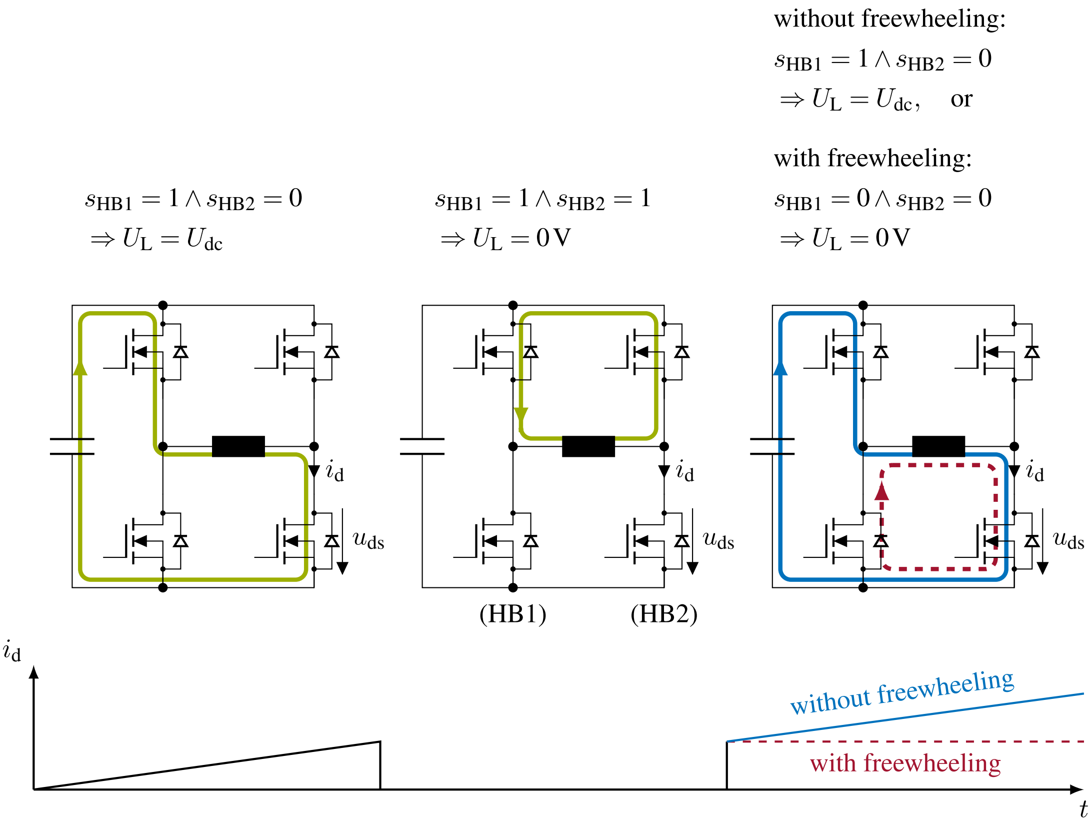

Figure 10.18: Illustration of the two different double-pulse experiments conducted in order to measure the on-state voltage with a voltage slope on $u_{\text{ds,on}}$ and without

The measured conduction phase, i.e., the second pulse of the double-pulse experiment, of one of the switches under test with and without freewheeling is shown in Figure 10.19. The upper graph depicts the drain current that either stays constant or rises according to the dc-link voltage and load inductance. In an application, this slope would also depend on the load voltage. The drain-source voltage is plotted in the middle graph. The bottom graph shows the on-state voltage u_{ADC} as measured behind the voltage limiter at the ADC for both cases.

Directly after turn-on, the on-state voltage cannot be sampled due to its strong oscillations.

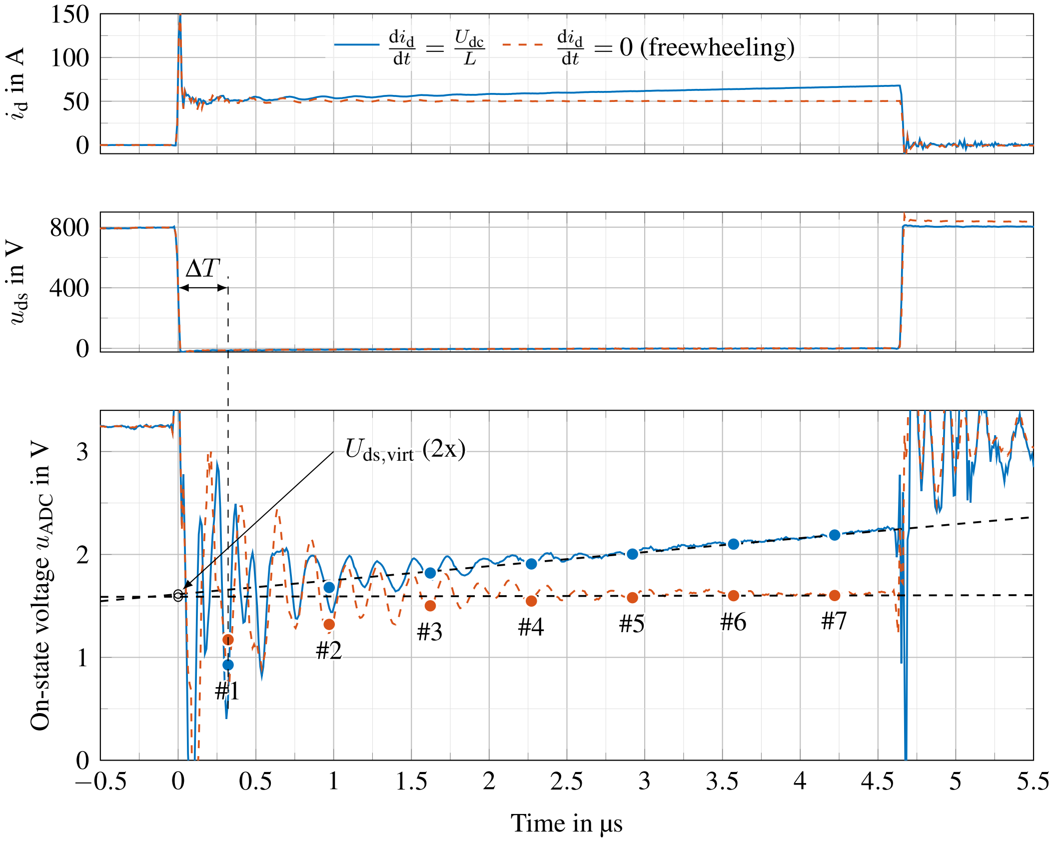

Figure 10.19: Conduction phase with (dashed red) and without (solid blue) freewheeling [99]; recorded ADC samples #1 to #7 as dots; linear regression of the last two samples in dashed black; $t = 0\,\mathrm{s}$ corresponds to $u_\mathrm{ds} = \frac{U_\mathrm{dc}}{2}$

Instead, the latter samples can be used to determine a linear regression of the on-state voltage and estimate a virtual on-state voltage $U_\mathrm{ds,virt}$ at the time when u_ds crosses $\frac{U_\mathrm{dc}}{2}$

$$t_\mathrm{virt} := t\big|_{u_\mathrm{ds}=\frac{U_\mathrm{dc}}{2}}, \tag{10.9}$$

$$U_\mathrm{ds,virt} = u_\mathrm{ADC}\left(t_\mathrm{virt}\right). \tag{10.10}$$

Using this virtual on-state voltage makes the measurement results less dependent on the dc-link voltage, load voltage and the switching state of the other half-bridge. Additionally, the virtual on-state voltage $U_\mathrm{ds,virt}$ is determined for the same time when the switching time measurements are conducted, thus improving the coherence of the four TSEPs that are to be combined.

Sample selection It must be determined which samples should be used for the regression. Using the first samples includes more noise while using only the latter samples decreases the number of available samples and increases the extrapolation error from those samples to the switching process.

In order to find the optimal selection of samples to be used, two sets of matching double-pulses were created for the high-side and low-side switch at the following operating points

$$\vartheta \in \{30\,°\mathrm{C}, 50\,°\mathrm{C}, 70\,°\mathrm{C}, \dots, 130\,°\mathrm{C}, 140\,°\mathrm{C}\}^{11}, \quad I_\mathrm{d} \in \{2\,\mathrm{A}, 4\,\mathrm{A}, 6\,\mathrm{A}, \dots, 60\,\mathrm{A}\}. \tag{10.11}$$

One set used freewheeling (FW) during the conduction phase, while the other set applied the dc-link voltage to the load during this phase, i.e., as shown in Figure 10.19 for one double pulse experiment. In each double-pulse experiment, the virtual on-state voltage $U_{\mathrm{ds,virt}}$ was determined for all possible start samples $n_{\mathrm{start}} = 1$ to $n_{\mathrm{start}} = 6$ and all possible stop samples $n_{\mathrm{end}} = 2$ to $n_{\mathrm{end}} = 7$. Discontinuous sample sets were not investigated. Independence of the dc-link voltage, load voltage and the switching state of the other half-bridge is achieved if there is no difference between the determined virtual on-state voltage with freewheeling $U^{(\mathrm{FW})}_{\mathrm{ds,virt}}$ and without freewheeling $U^{(\mathrm{no\ FW})}_{\mathrm{ds,virt}}$

$$\Delta U_{\mathrm{ds,virt}} = U^{(\mathrm{no\ FW})}_{\mathrm{ds,virt}} - U^{(\mathrm{FW})}_{\mathrm{ds,virt}} = 0\,\mathrm{V}. \tag{10.12}$$

The determined median deviation of $U_{\mathrm{ds,virt}}$and the root-mean-square deviation between the two cases are presented in Figure 10.20. The lowest RMSD can be achieved by using samples #4 to #7 for the high-side switch, or #5 to #7 for the low-side switch. Using later start samples increases the RMSD, validating the expected effect of the reduced number of samples and the increasing extrapolation error. The lowest dependency on the current slope is achieved by using only the last two samples #6 and #7.

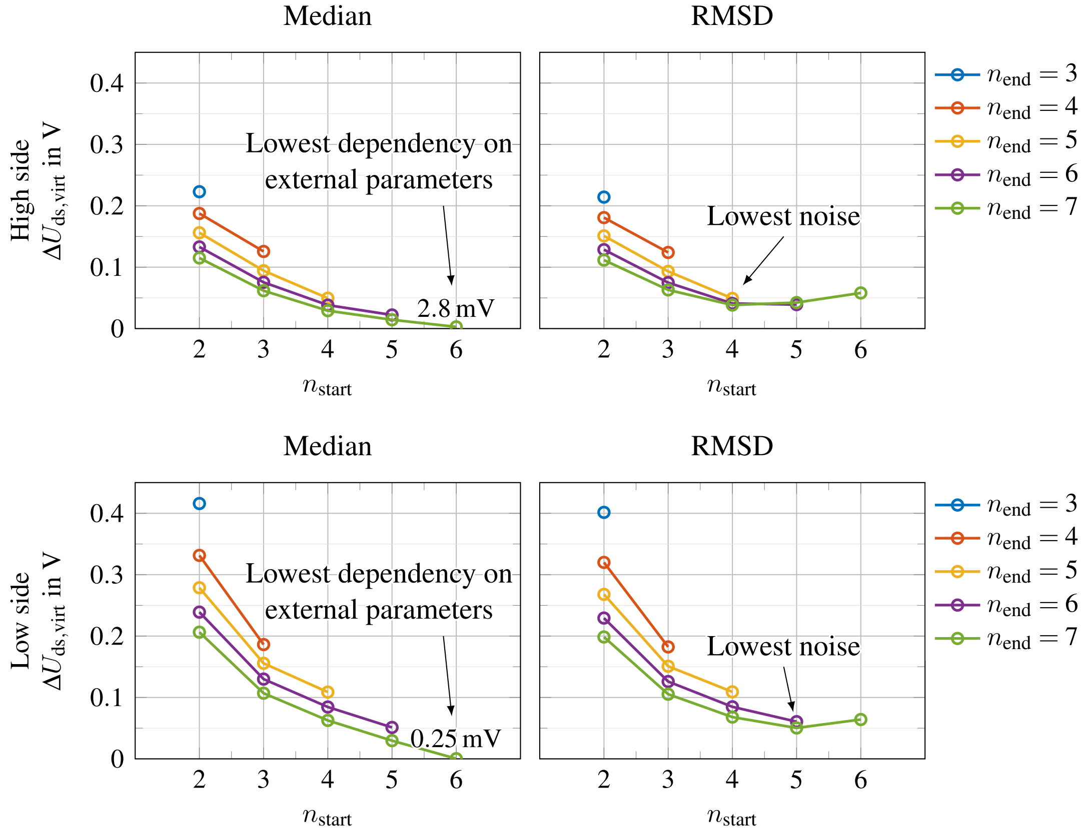

Figure 10.20: Median error and RMSD between the virtual on-state voltage $U_{\mathrm{ds,virt}}$ with and without freewheeling [99]; n_{start} is the first sample used for regression, n_{end} the last; results for $n_{\mathrm{start}} = 1$ have unacceptable error

One would expect the median error to approach zero with increasing start samples n_{start} and oscillate slightly around zero after a certain distance of the samples to the turn-on pro-

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[11] Note that the last temperature step is smaller.

cess is reached. While this expectation might be matched by the results of the high-side switch, it is unclear whether the median error of the low-side switch would move to negative values if more samples were available. This could be a hint that more time for the on-state measurements would be beneficial.

In the context of degradation detection, a zero-mean noisy signal is expected to be less impactful than a signal with an error correlating to the switching state of the other half-bridge, the load voltage or the dc-link voltage. Thus, only the samples #6 and #7 will be used for the calculation of all virtual on-state voltages $U_{\mathrm{ds,virt}}$ within this work.

The virtual on-state voltage of the partner switch, measured closely before turn-off, is also determined from the two last samples. In this case, these two samples are closest to the switching process. Nevertheless, the earlier samples can still be affected by the oscillations caused by the commutation loop if the duty cycle to the half-bridge is high, see Figure 10.8.

10.6 Double-pulse results

At this point, the TSEP measurement hardware and the required postprocessing of the virtual on-state voltage has been fully designed and specified. Now, the TSEP measurement system is validated in double pulse experiments.

The double-pulse experiments are conducted on a hot plate. The drain current and module temperature were varied in a wide range, see Table 10.4. The dc-link voltage was perturbed only slightly, to determine dc-link voltage sensitivities at the nominal operating point only.

Table 10.4: Default parameter sweep for double-pulse experiments

Module temperature	ϑ	$\in \{30\,°\mathrm{C}, 50\,°\mathrm{C}, 70\,°\mathrm{C}, \ldots, 130\,°\mathrm{C}, 140\,°\mathrm{C}\}$[12]
Drain current	I_{d}	$\in \{2\,\mathrm{A}, 4\,\mathrm{A}, 6\,\mathrm{A}, \ldots, 60\,\mathrm{A}\}$
DC-link voltage	U_{dc}	$\in \{780\,\mathrm{V}, 800\,\mathrm{V}, 820\,\mathrm{V}\}$

The intended operating range was up to $I_{\mathrm{d}} = \pm I_{\mathrm{N}} = \pm 50\,\mathrm{A}$. At very high currents and temperatures, outliers can be observed. This happens because the drain current rises during the second conduction phase of the double-pulse experiments, see Figure 10.21. If the on-state voltage reaches the ADC limits of $\pm 2.5\,\mathrm{V}$ when a sample is taken, the acquired sample saturates. This effect is severe in this application, as it impacts the determined linear regression for the slope correction. A small error in the last sample due to saturation leads to a large extrapolation error. The effect occurs outside the intended operating range, i.e., $I_{\mathrm{L}} > I_{\mathrm{N}} = 50\,\mathrm{A}$, and is therefore not critical.

The TSEP measurement results of the virtual on-state voltage of module M_0 are shown in Figure 10.22 and Figure 10.23. Module M_0 is an unmodified SiC MOSFET module used for fundamental investigations. Within this work, several other modules will be analyzed, i.e., during the accelerated aging tests. The TSEPs measured during double-pulse experiments for all modules are listed in Appendix L. The measured virtual on-state voltage before turn-off and after turn-on $U_{\mathrm{ds,virt}}$ matches expectations.

The switching times measured with the TSEP measurement system are plotted in Figure 10.24 and Figure 10.25. The noise is noticeably larger than in the on-state voltage

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[12] Note that the last temperature step is smaller.

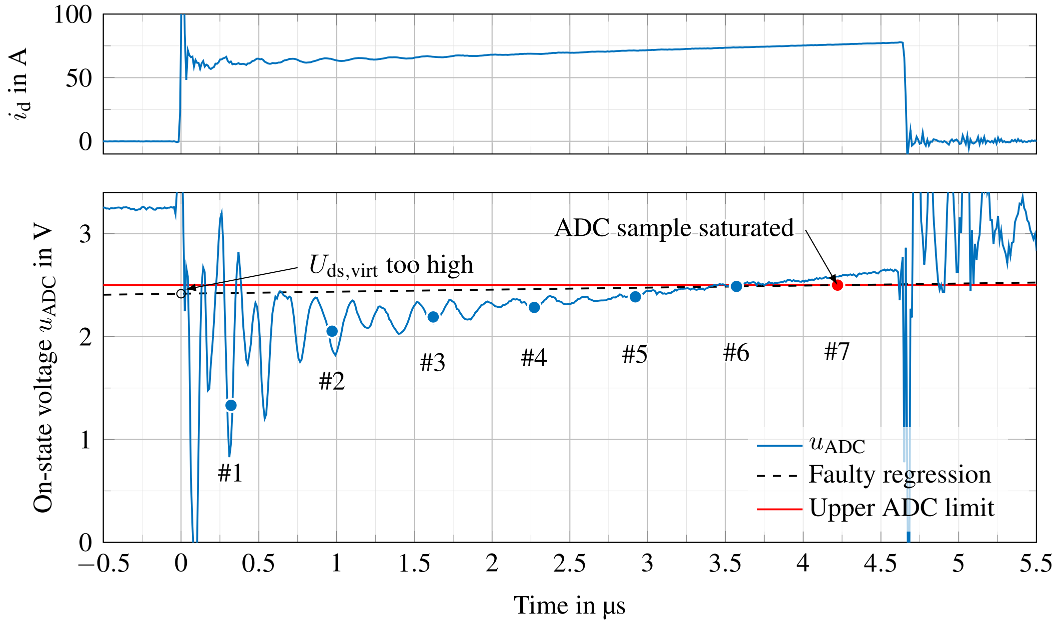

Figure 10.21: Example of the last sample saturating, causing a large extrapolation error in $U_{ds,virt}$; $I_L = 60\,A$, $\vartheta = 130\,°C$; the upper ADC limit is crossed at currents above $i_d = 73\,A$;

measurement. At currents below $5\,A \widehat{=} 0.1 I_N$ the switching time measurement seems to be unusable, as t_{rrm} decreases with current in this range. The current rise time t_{ri} or the time until the overcurrent peak is reached t_{rrm} shows the expected increase with the drain current. The turn-on delay time t_d is almost constant with regard to the drain current. Both switching times show PTC behavior, although the effect is very small for the turn-on delay time. Although PTC behavior is not impossible for the turn-on delay time, see Chapter 9, it was expected that the NTC behavior of the threshold voltage dominates the temperature dependency of the turn-on delay time.

The preprocessed variants of the switching times t_{ri} and $\frac{t_{rrm}}{t_d}$ are shown in Figure 10.26 to Figure 10.29. As expected from the results of Chapter 7, the behavior of the preprocessed variants is much more coherent and linear with regard to the current I_d. Nevertheless, the results are still not satisfactory with regard to the temperature sensitivity.

The current rise time t_{ri} and the ratio $\frac{t_{rrm}}{t_d}$ of the high-side switch only show a clearly identifiable temperature dependency at high currents. This could be due to the reverse recovery charge of the body diode of the partner switch. The temperature and current behavior of the reverse recovery charge was shown in Figure 9.16. For small currents, the reverse recovery charge is dominated by the constant charge contribution needed to change the voltage of the MOSFET's output capacitances C_{oss}. Only at high currents, a noticeable temperature dependency of the reverse recovery charge occurs.

The double-pulse calibration data of all modules is listed in Appendix L.

Summary of the TSEP measurement hardware for SiC MOSFETs The hardware for measuring the on-state voltage and switching times of SiC MOSFETs was presented. Design aspects and challenges were discussed. The sequence to acquire the four TSEP measurements in close succession during one turn-on process was shown.

The oscillations of the commutation loop make on-state voltage measurements right after

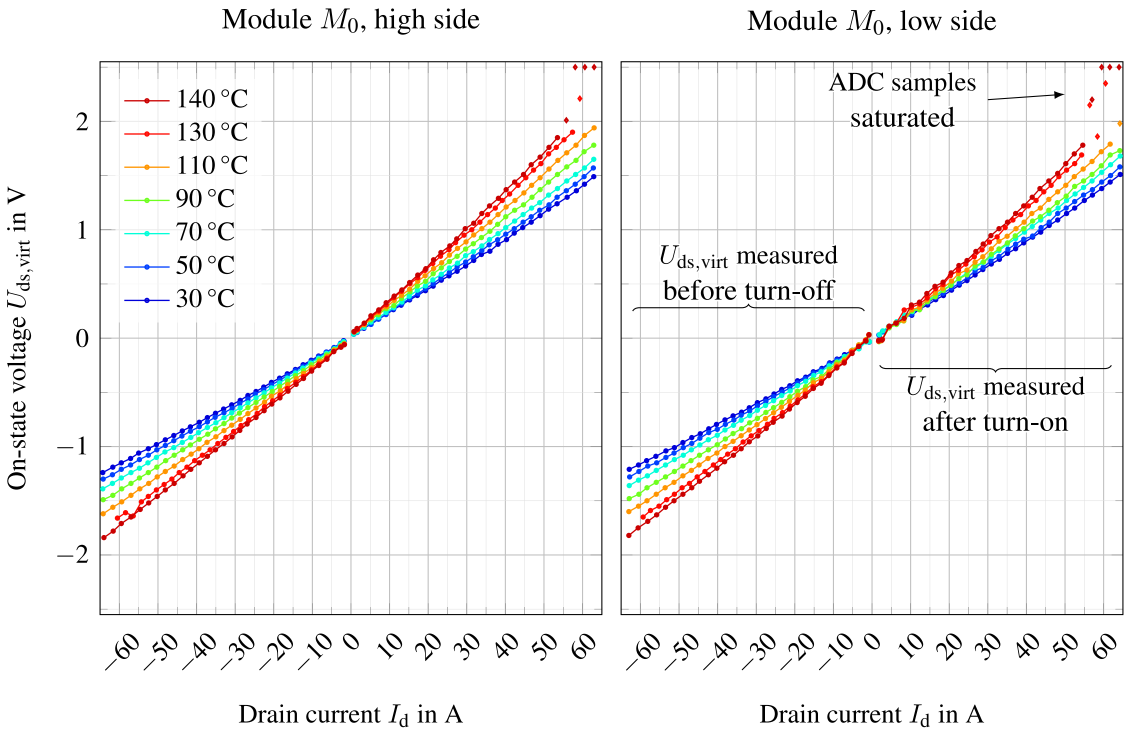

Figure 10.22: Double-pulse measurements of the virtual on-state voltage $U_{ds,virt}$ of module M_0 at $U_{dc} = 800\,V$; outliers marked as diamonds

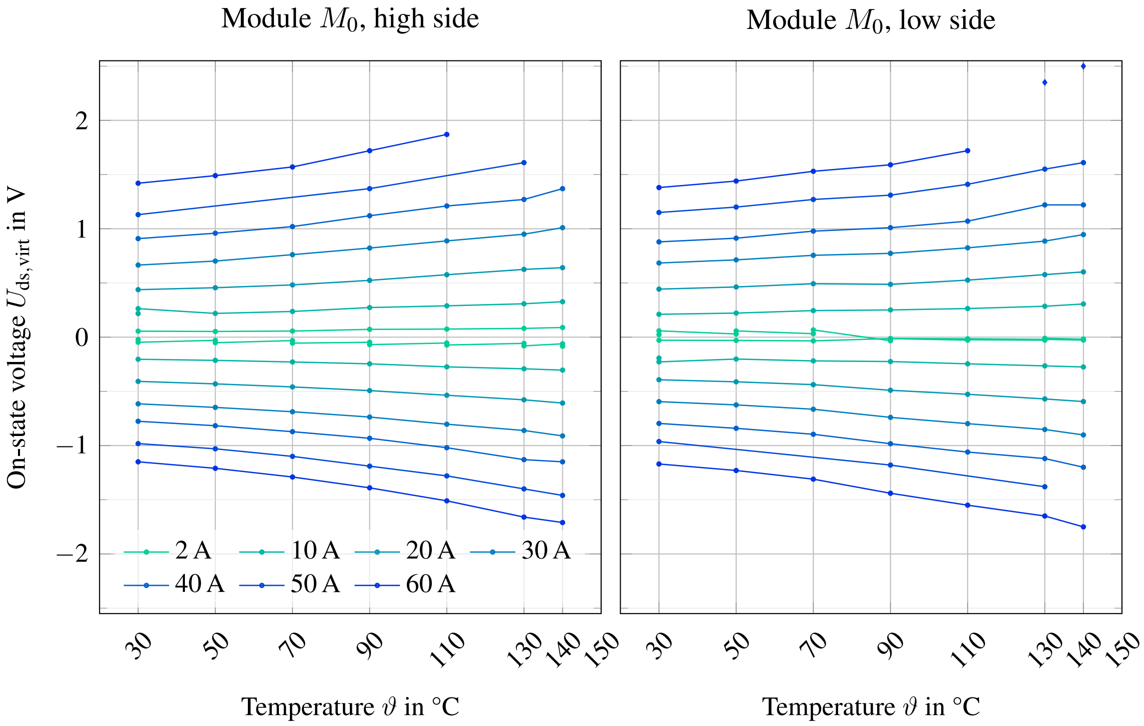

Figure 10.23: Double-pulse measurements of the virtual on-state voltage $U_{ds,virt}$ of module M_0 at $U_{dc} = 800\,V$; outliers marked as diamonds

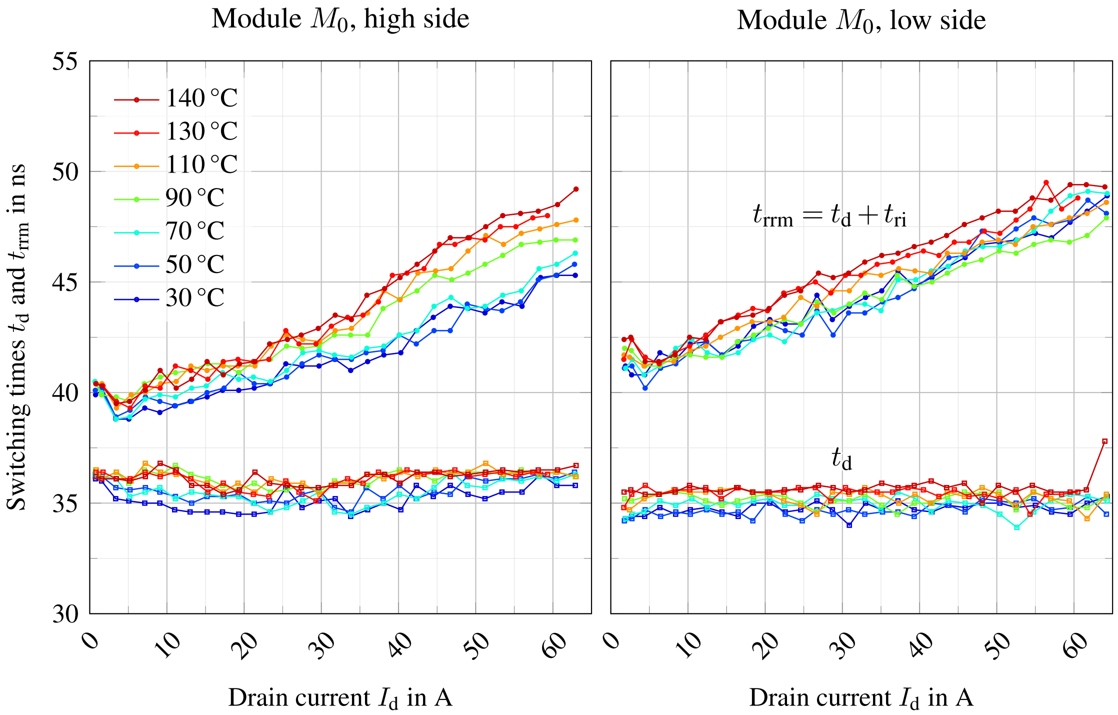

Figure 10.24: Double-pulse measurements of the switching times t_{d} and t_{rrm} of module M_0 at $U_{\mathrm{dc}} = 800\,\mathrm{V}$; outliers marked as diamonds

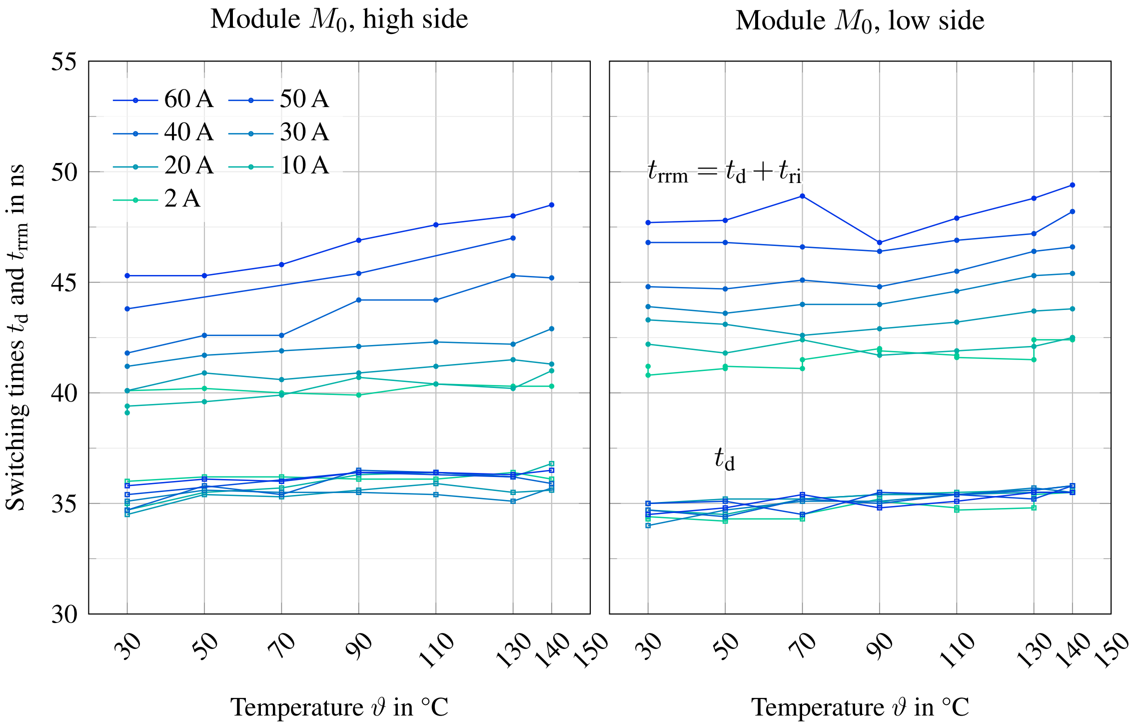

Figure 10.25: Double-pulse measurements of the switching times t_{d} and t_{rrm} of module M_0 at $U_{\mathrm{dc}} = 800\,\mathrm{V}$; outliers marked as diamonds

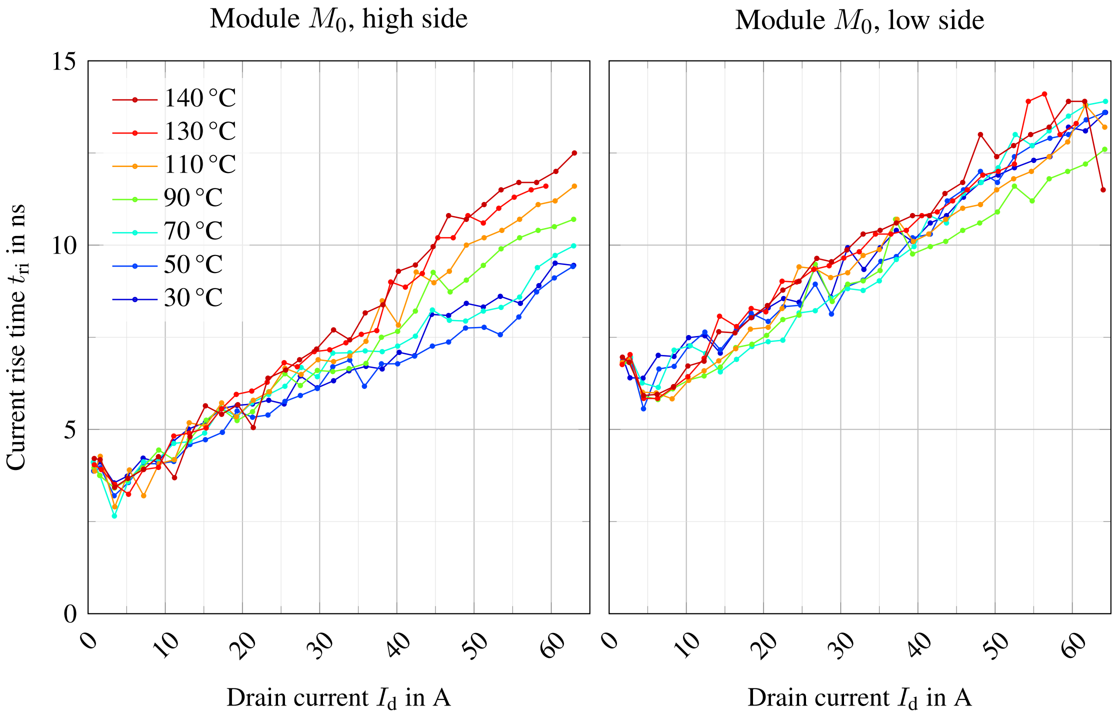

Figure 10.26: Switching times t_d and t_{rrm} preprocessed into the current rise time t_{ri} at $U_{dc} = 800\,V$

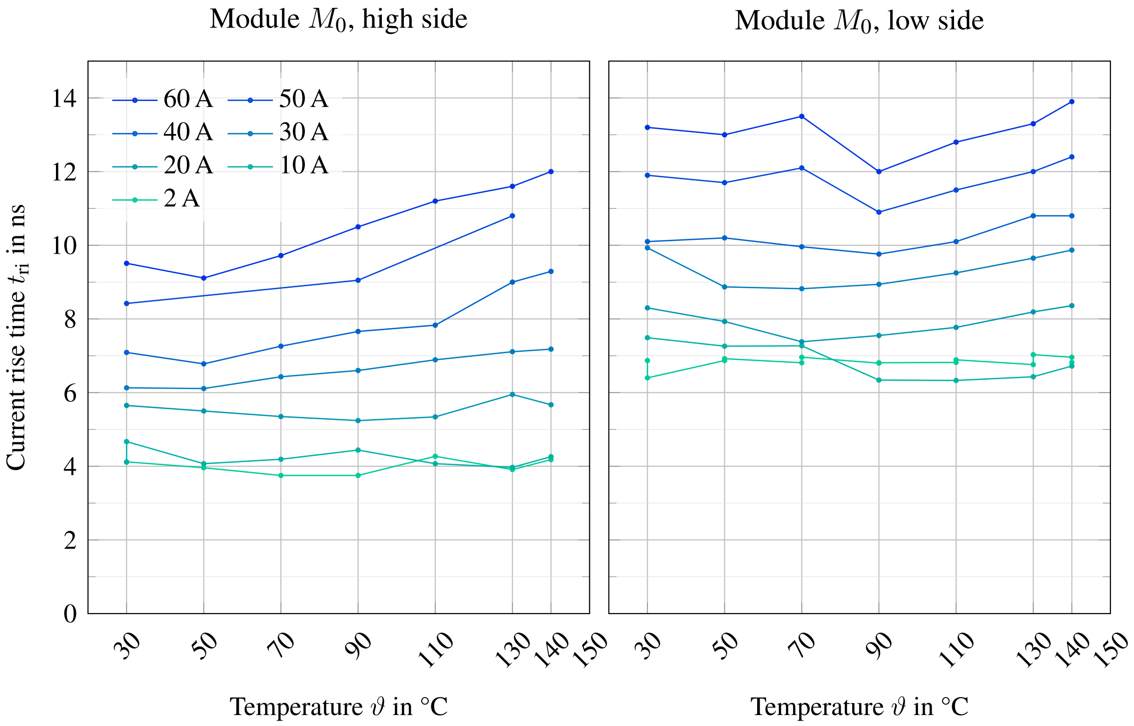

Figure 10.27: Switching times t_d and t_{rrm} preprocessed into the current rise time t_{ri} at $U_{dc} = 800\,V$

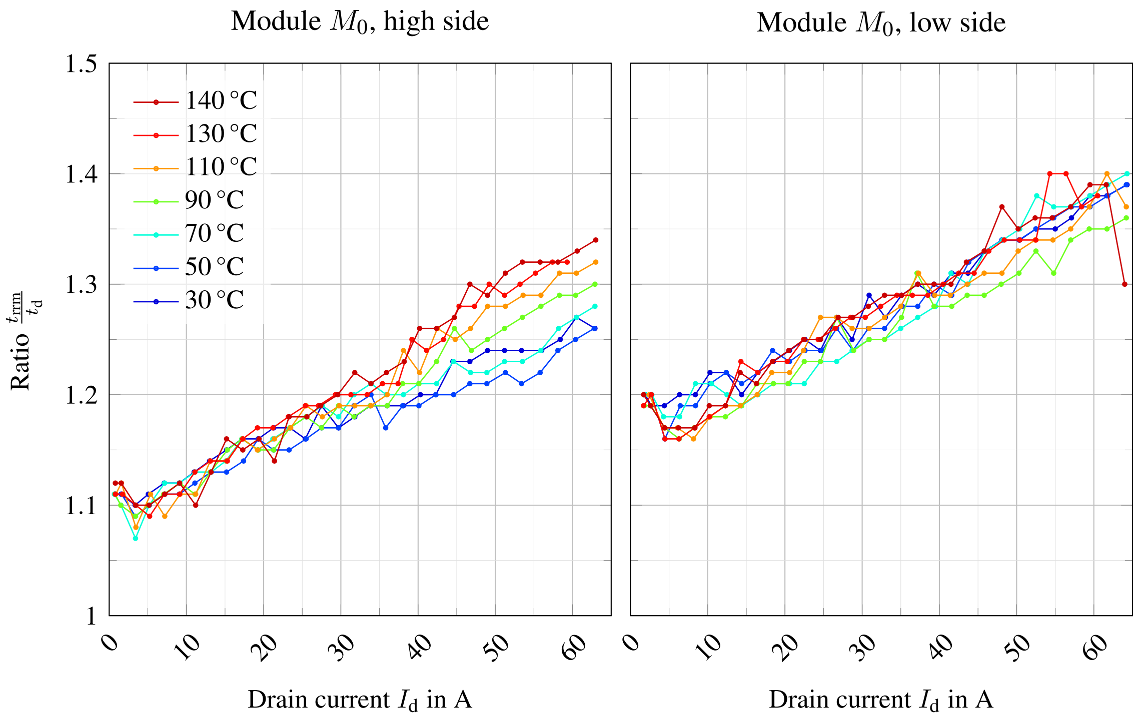

Figure 10.28: Switching times t_{d} and t_{rrm} preprocessed into the ratio $\frac{t_{\mathrm{rrm}}}{t_{\mathrm{d}}}$ at $U_{\mathrm{dc}} = 800\,\mathrm{V}$

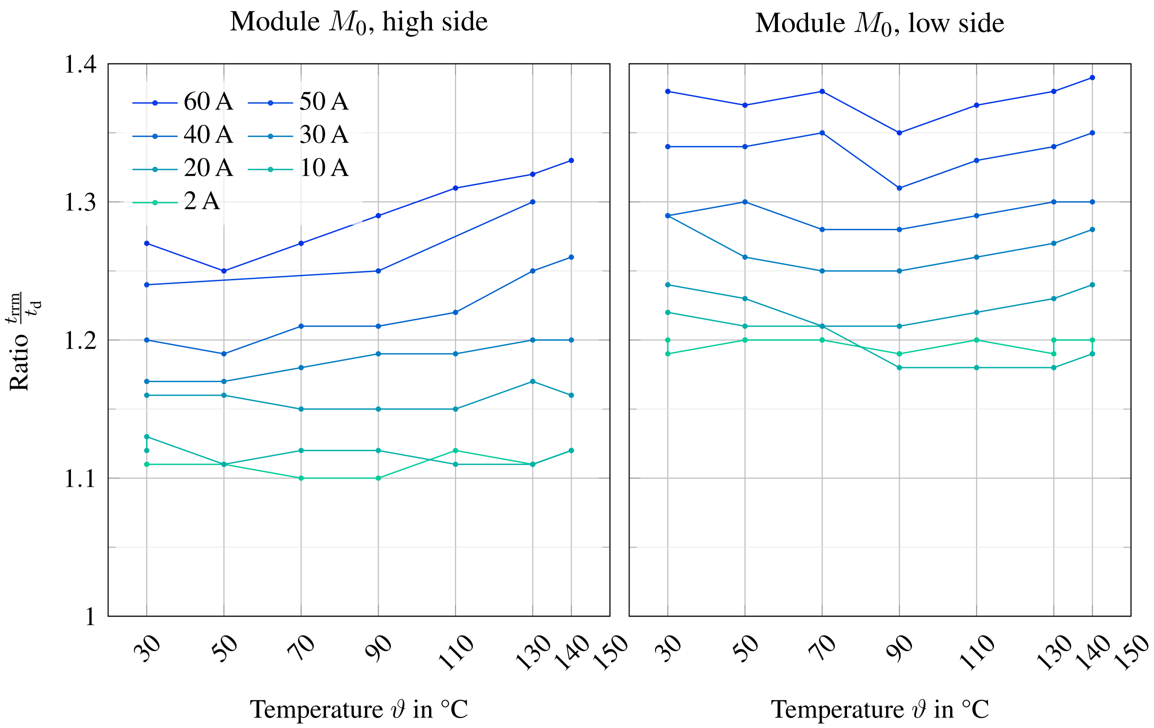

Figure 10.29: Switching times t_{d} and t_{rrm} preprocessed into the ratio $\frac{t_{\mathrm{rrm}}}{t_{\mathrm{d}}}$ at $U_{\mathrm{dc}} = 800\,\mathrm{V}$

turn-on impossible, while the possible voltage slope on the drain-source voltage modifies the on-state voltage measurement depending on the dc-link voltage, the load voltage and the switching state of the other half-bridge. A possible solution to this issue was presented, namely taking samples after the oscillations have settled and extrapolating backwards to determine a virtual on-state voltage $U_{\mathrm{ds,virt}}$. The virtual on-state voltage $U_{\mathrm{ds,virt}}$ represents the on-state voltage the SiC MOSFET would have had at the moment of turn-on, before the on-state voltage changes due to the slope.

The TSEP-measurement system was operated in double-pulse experiments for a wide variety of temperatures and load currents. While the on-state voltage measurements $U_{\mathrm{ds,virt}}$ exhibited accurate and expected behavior, the switching time measurements showed a high noise level and a low temperature dependency. In fact, the investigated SiC MOSFET shows almost no sensitivity of the turn-on time towards the temperature of the MOSFET turning-on, which will be measured and analyzed in Chapter 15.

11 Turn-on current estimation

The TSEPs analyzed in this work generally show a significant sensitivity towards the load current. Therefore, knowing the current I_{ton} at the moment the switch under test is turned on is essential for accurate temperature estimation. In continuous PWM operation, the instantaneous current I_{ton} at turn-on differs noticeably from the average value $\overline{I}$ due to the inverter's current ripple.

During operation, the current is measured by the inverter's sensors, which are typically designed for machine control. Usually, one current sample is taken from the sensor each PWM period. Depending on the ADC type used, i.e., successive-approximation ADC or sigma-delta ADC, the sensor provides a single measurement taken in the middle of the PWM period or the average of the instantaneous current across the PWM period. When using additional filters, either simple low-pass filters or sinc filters, information from the previous PWM periods is included in the latest sampled current measurement.

The setup employed uses a current transducer with a sigma-delta ADC. The bitstream is averaged over one PWM period. No low-pass or sinc filter is implemented, in order to avoid including historical data in the measurement values.

In this chapter, a model of the current waveform during one PWM period is developed. Unlike other models [153, 154], this model is not designed to determine the overall current ripple, but rather the instantaneous current I_{ton} at turn-on. For the most part, I_{ton} depends on the duty cycles, the load voltage and the load inductance. The varying locations of a turn-on process within the PWM period will be shown for a full-bridge setup. Furthermore, the instantaneous current is affected by non-ideal switching behavior. The following factors are considered in the model:

1. the effects of the interlock times
2. a well-known load voltage, i.e., an ohmic voltage drop
3. the impact of the node capacitance on the voltage rise time
4. a small phase shift between the carriers of the two half-bridges

The model will be developed incrementally, starting with a simplified setup. The necessary model parameters will be determined by measurement or extracted from datasheets. Finally, the model accuracy will be validated using additional experimental data. This validation will be performed in Section 11.3 after modeling all effects.

11.1 Initial current model

Figure 11.1 shows the extended model of the full-bridge setup. The switching signals s_1 to s_4 are "one" if the MOSFET is turned on and "zero" if the MOSFET is turned off. The actual output voltages of the half-bridges $u_{\mathrm{HB},1}$ and $u_{\mathrm{HB},2}$ depend on the interlock time T_{D}, the node capacitance C_{node} and, to a small degree, the on-state resistances $R_{\mathrm{ds,on}}$ of the MOSFETs.

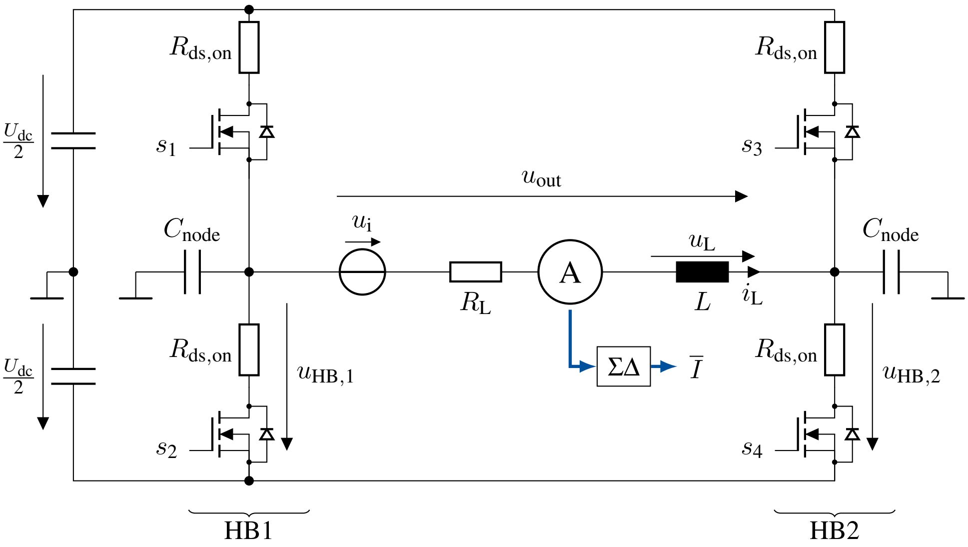

Figure 11.1: Full-bridge model and definitions; extended model

The node capacitance is a virtual, aggregated capacitance that models all capacitances that must be charged when the voltage of the half-bridge's phase terminal changes. Typical contributors are not only the output capacitances C_{oss} of the high-side and low-side switches of the half-bridge, but also the capacitance between the copper plane of the phase potential on the DCB substrate and the cooler. Furthermore, the capacitance of the load and load cables add to the node capacitance.

> **Remark:** Although this is a work on TSEPs and the details of the on-state voltage drops, together with the switching times, have been analyzed in detail in Part III, the level of detail used for the current model will be greatly reduced. The on-state voltage drops will be modeled as a constant resistor $R_{\mathrm{ds,on}}$ and the turn-on and turn-off delay times will be modeled as constants.

Base cases For now, the node capacitance C_{node}, the load resistance R_{L}, the load voltage u_{i} and the on-state resistances $R_{\mathrm{ds,on}}$ of the MOSFETs are all considered to be zero. The initial model is shown in Figure 11.2. This simple model results in four base cases for the

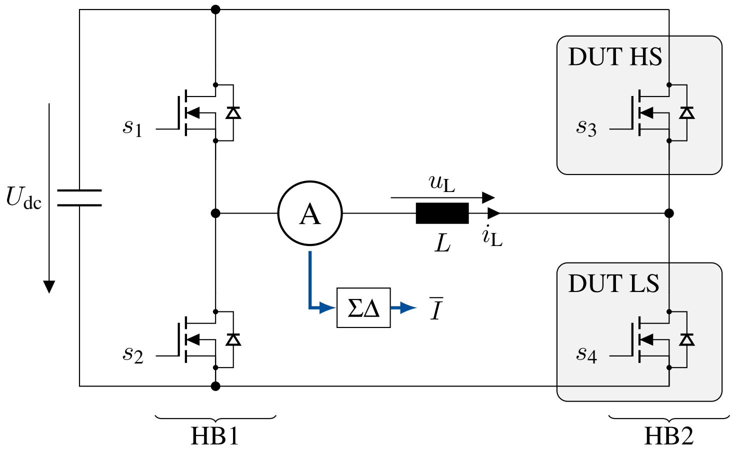

Figure 11.2: Full-bridge model and definitions; initial model

instantaneous current I_{ton}, which depend on two conditions. First, depending on which half-bridge has the larger duty cycle, the current slopes may occur before or after the turn-on process of the switches under test. Second, the effects of the interlock time T_{D} will cause a current deviation depending on the current direction. Edge cases, i.e., when the current waveform crosses 0 A during the period, are not included in the model.

Figure 11.3 shows these four base cases. For each case, the three top graphs show the switching signals of the half-bridges and the resulting output voltage u_{out} of the full-bridge. The effects caused by the interlock time are marked in gray.

The bottom graphs show the instantaneous current i_{L}, the average current $\overline{I}$ in the illustrated period and markers when the switches under test are turned on. The instantaneous currents at turn-on are $I_{\text{ton,HS}}$ and $I_{\text{ton,LS}}$. The instantaneous current at the midpoint of the PWM period I_{mid} equals the average current $\overline{I}$ if the current waveform during a PWM period is centrosymmetric with regard to the midpoint of the period. In the course of this chapter, several effects that introduce asymmetry into the current waveform, leading to a discrepancy between the average current value $\overline{I}$ and the instantaneous current at the midpoint of the PWM period I_{mid}, will be discussed.

Without the effects of the interlock time, i.e., $T_{\text{D}} = 0\,\text{s}$, the differences between the instantaneous currents at turn-on and at the midpoint of the PWM period depend only on the switching signals

$$I_{\text{ton,HS}} = \begin{cases} I_{\text{mid}} & \text{for } s_1 \geq s_2 \\ I_{\text{mid}} + \Delta I & \text{for } s_1 < s_2 \end{cases}, \quad T_{\text{D}} = 0\,\text{s}, \tag{11.1}$$

$$I_{\text{ton,LS}} = \begin{cases} I_{\text{mid}} & \text{for } s_1 \geq s_2 \\ I_{\text{mid}} - \Delta I & \text{for } s_1 < s_2 \end{cases}. \tag{11.2}$$

When considering the interlock time, i.e., $T_{\text{D}} > 0$, the cases become more complex. In addition to the cases shown, the turn-on process can occur during the current slopes, as marked by the red and blue dots in Figure 11.3. A current deviation of ΔI_{slope} between the current at the midpoint of the PWM period I_{mid} and the instantaneous currents at turn-on $I_{\text{ton,LS}}$ and $I_{\text{ton,HS}}$ occurs.

Turn-on moment The current waveform can be determined by integrating the voltage u_{L} across the load inductance L

$$i_{\text{L}} = \int \frac{u_{\text{L}}}{L} \text{d}t = \int \frac{u_{\text{HB,1}} - u_{\text{HB,2}}}{L} \text{d}t. \tag{11.3}$$

The waveform of the output voltage u_{L} and the points in time $t_{\text{on,HS}}$ and $t_{\text{on,LS}}$ when the turn-on occurs are needed to determine the instantaneous currents $I_{\text{ton,HS}}$ and $I_{\text{ton,LS}}$ at turn-on.

In the given test setup, the interlock times are implemented as follows. The turn-off signal is scheduled without any modification. Then the interlock time T_{D} must pass before the other switch is turned on. Therefore, the effects of the interlock times are not centered around the ideal switching time, but always occur subsequently. The times at which the high-side and

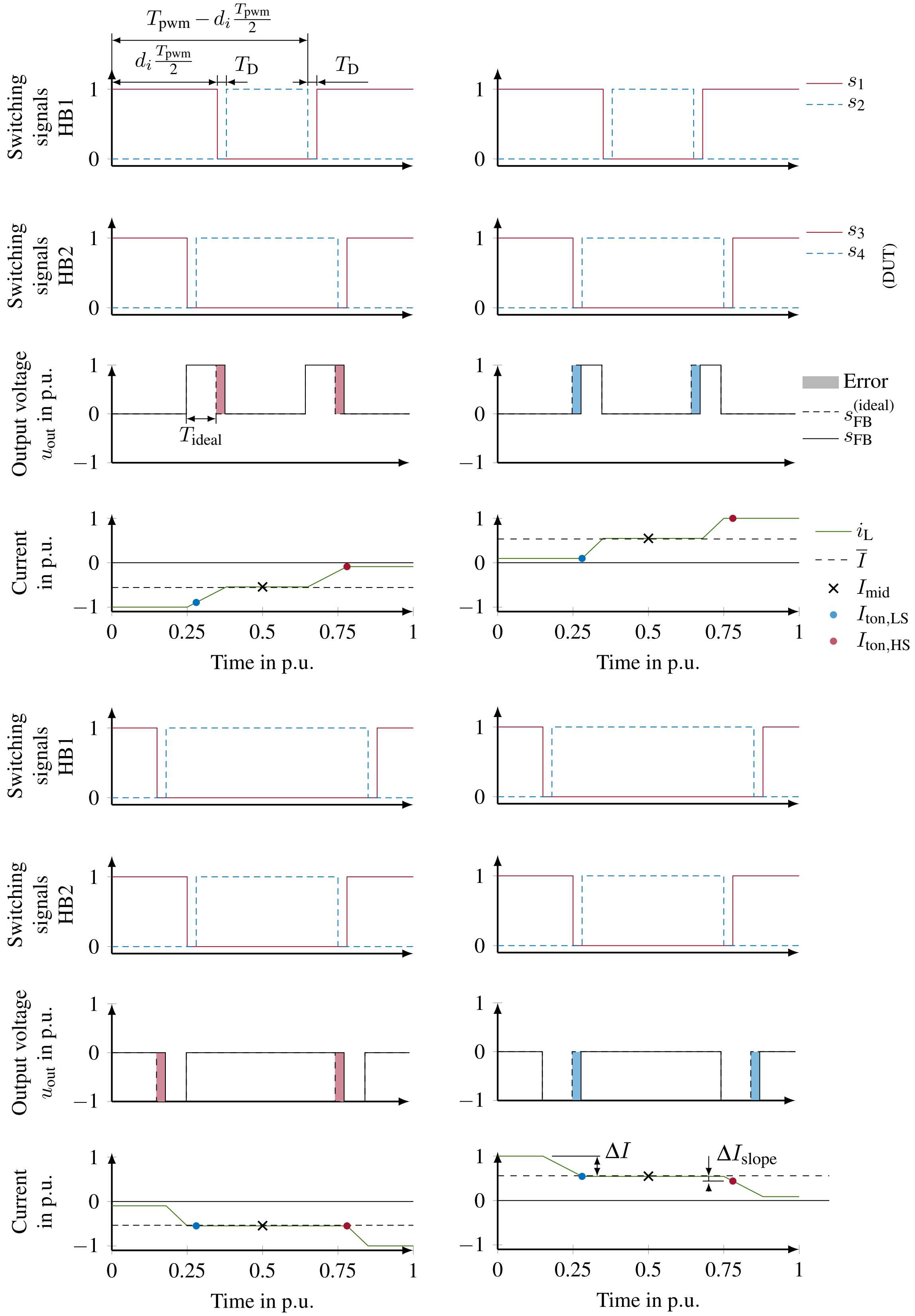

Figure 11.3: Current ripple in one PWM period for different current polarities and duty cycle conditions; the initial current model is used; red error areas are positive voltage-time integral errors, blue negative

low-side switches turn on and off can be described independent of the current polarity

$$t_{\text{off,HS}} = d_i \cdot \frac{T_{\text{pwm}}}{2}, \qquad t_{\text{off,LS}} = T_{\text{pwm}} - d_i \cdot \frac{T_{\text{pwm}}}{2}, \tag{11.4}$$

$$t_{\text{on,LS}} = d_i \cdot \frac{T_{\text{pwm}}}{2} + T_{\text{D}}, \qquad t_{\text{on,HS}} = T_{\text{pwm}} - d_i \cdot \frac{T_{\text{pwm}}}{2} + T_{\text{D}}, \tag{11.5}$$

$$I_{\text{ton,HS}} = i_{\text{L}}\left(t_{\text{on,HS}}\right), \qquad I_{\text{ton,LS}} = i_{\text{L}}\left(t_{\text{on,LS}}\right). \tag{11.6}$$

The output voltage depends on the applied duty cycles $d_1(s_1, s_2)$ of half-bridge HB1 and $d_2(s_3, s_4)$ of half-bridge HB2. The current at the midpoint of the PWM period I_{mid} forms the starting point for all the following calculations.

Assuming symmetrical, single-edged PWM [148], the current step ΔI between the current plateau and the currents at the beginning and end of the PWM period can be described for the ideal case as

$$T_{\text{ideal}} = (d_1 - d_2)\frac{T_{\text{pwm}}}{2}, \quad T_{\text{D}} = 0\,\text{s} \tag{11.7}$$

$$\Delta I_{\text{ideal}} = (d_1 - d_2)\frac{T_{\text{pwm}}}{2}\frac{U_{\text{dc}}}{L}. \tag{11.8}$$

Taking the interlock time into account, i.e., $T_{\text{D}} > 0\,\text{s}$, leads to a current-dependent error in the voltage-time integral applied to the load inductance. Neither the node capacitance C_{node} nor the switching time delay have been considered so far. Consequently, the output voltages of the half-bridges jump instantaneously, either at the beginning of the interlock time or at the end. The voltage-time integral of the first and second voltage pulses in the output voltage waveform u_{out} can be determined according to the applied duty cycles and the current polarity

$$U_{\text{dc}}T_1 = U_{\text{dc}}\left[t_{\text{off,HS}}^{(\text{HB1})} + H\left(-\bar{I}\right)T_{\text{D}} - \left(t_{\text{off,HS}}^{(\text{HB2})} + H\left(\bar{I}\right)T_{\text{D}}\right)\right] \tag{11.9}$$

$$= U_{\text{dc}}\left[d_1\frac{T_{\text{pwm}}}{2} - d_2\frac{T_{\text{pwm}}}{2} - \text{sgn}\left(\bar{I}\right)T_{\text{D}}\right] \tag{11.10}$$

$$= U_{\text{dc}}\left[T_{\text{ideal}} - \text{sgn}\left(\bar{I}\right)T_{\text{D}}\right], \tag{11.11}$$

$$U_{\text{dc}}T_2 = U_{\text{dc}}\left[T_{\text{ideal}} - \text{sgn}\left(\bar{I}\right)T_{\text{D}}\right], \tag{11.12}$$

with the Heavyside function

$$H(x) = \begin{cases} 0 & \text{for } x < 0 \\ 1 & \text{for } x \geq 0 \end{cases}. \tag{11.13}$$

The voltage-time integral Φ can be used to determine the current step between the current at the midpoint of the PWM period I_{mid} and the outer currents beyond the current slopes

$$\Delta I = \frac{\Phi}{L} = \frac{U_{\text{dc}}T}{L}, \tag{11.14}$$

$$\Delta I = \Delta I_1 = \Delta I_2 = \frac{U_{\text{dc}}}{L}\left(T_{\text{ideal}} + \text{sgn}\left(\bar{I}\right)T_{\text{D}}\right). \tag{11.15}$$

In the case of symmetrical, single-edged PWM modulation, the first and second current steps ΔI_1 and ΔI_2 have the same magnitude.

Current deviation due to duty cycle and interlock time Equation (11.3) represents a linear system. If the voltage u_{L} across the load inductance is a sum of multiple voltages, the impact of each voltage source can be determined separately. This allows the stepwise extension of the model for each impact considered. Let the instantaneous currents at turn-on be defined as the current plateau I_{mid}, modified by a current error $\Delta I_{\mathrm{ton}}^{(d_1,d_2,T_{\mathrm{D}})}$ depending on the applied duty cycles and the interlock time

$$I_{\mathrm{ton,HS}} \coloneqq I_{\mathrm{mid}} + \Delta I_{\mathrm{ton,HS}}^{(d_1,d_2,T_{\mathrm{D}})}, \tag{11.16}$$

$$I_{\mathrm{ton,LS}} \coloneqq I_{\mathrm{mid}} + \Delta I_{\mathrm{ton,LS}}^{(d_1,d_2,T_{\mathrm{D}})}. \tag{11.17}$$

This definition of I_{ton} allows the extension of the model by incorporating additional effects that have not yet been taken into account

$$I_{\mathrm{ton}} = I_{\mathrm{mid}} + \Delta I_{\mathrm{ton}}^{(d_1,d_2,T_{\mathrm{D}})} + \Delta I^{(\text{Impact } 2)} + \ldots + \Delta I^{(\text{Impact } n)}. \tag{11.18}$$

The resulting deviations between the instantaneous current values, $I_{\mathrm{ton,HS}}$ and $I_{\mathrm{ton,LS}}$, and the current at the midpoint of the PWM period I_{mid} can be extracted from Figure 11.3 and (11.15). The results are summarized in Table 11.1.

Table 11.1: Current adjustments from the sensor measurement to the instantaneous current; initial model

	Current polarity	Voltage polarity	Condition	$\Delta I_{\mathrm{ton}}^{(d_1,d_2,T_{\mathrm{D}})}$
HS	$\overline{I} \gg 0$	$\overline{u}_{\mathrm{HB1}} \geq \overline{u}_{\mathrm{HB2}}$	$d_1 \geq d_2$	$\frac{U_{\mathrm{dc}}}{L}\left(T_{\mathrm{ideal}} - T_{\mathrm{D}}\right)$
		$\overline{u}_{\mathrm{HB1}} < \overline{u}_{\mathrm{HB2}}$	$d_1 < d_2$	$-\frac{U_{\mathrm{dc}}}{L}\left(T_{\mathrm{D}}\right)$
	$\overline{I} \ll 0$	$\overline{u}_{\mathrm{HB1}} \geq \overline{u}_{\mathrm{HB2}}$	$d_1 \geq d_2 - \frac{2T_{\mathrm{D}}}{T_{\mathrm{pwm}}}$	$\frac{U_{\mathrm{dc}}}{L}\left(T_{\mathrm{ideal}} + T_{\mathrm{D}}\right)$
		$\overline{u}_{\mathrm{HB1}} < \overline{u}_{\mathrm{HB2}}$	$d_1 < d_2 - \frac{2T_{\mathrm{D}}}{T_{\mathrm{pwm}}}$	0
LS	$\overline{I} \gg 0$	$\overline{u}_{\mathrm{HB1}} \geq \overline{u}_{\mathrm{HB2}}$	$d_1 \geq d_2 + \frac{2T_{\mathrm{D}}}{T_{\mathrm{pwm}}}$	$-\frac{U_{\mathrm{dc}}}{L}\left(T_{\mathrm{ideal}} - T_{\mathrm{D}}\right)$
		$\overline{u}_{\mathrm{HB1}} < \overline{u}_{\mathrm{HB2}}$	$d_1 < d_2 + \frac{2T_{\mathrm{D}}}{T_{\mathrm{pwm}}}$	0
	$\overline{I} \ll 0$	$\overline{u}_{\mathrm{HB1}} \geq \overline{u}_{\mathrm{HB2}}$	$d_1 \geq d_2$	$-\frac{U_{\mathrm{dc}}}{L}\left(T_{\mathrm{ideal}}\right)$
		$\overline{u}_{\mathrm{HB1}} < \overline{u}_{\mathrm{HB2}}$	$d_1 < d_2$	0

The current polarity changes whether the interlock time affects the first or second switching process of the half-bridge, thereby shifting the boundaries of the cases with regard to the duty cycles. The full-bridge inverter setup on the test setup has no load voltage, and therefore drives very small duty cycle differences. Generally, the effects of the interlock time are expected to become less relevant at higher duty cycles, but it is important to bear in mind that the current step introduced by the interlock time is constant

$$\left|\Delta I_{T_{\mathrm{D}}}\right| = \frac{U_{\mathrm{dc}}}{L} T_{\mathrm{D}} \approx \frac{800\,\mathrm{V} \cdot 300\,\mathrm{ns}}{225\,\mu\mathrm{H}} = 1.1\,\mathrm{A} \approx 0.02 I_{\mathrm{N}}. \tag{11.19}$$

All test setup parameters are summarized in Table 10.2. For TSEP-based temperature estimations, a 2 % step in the current can be significant. The impact of the current error increases at smaller currents. Using the current rise time $t_{\text{ri}}\left(\vartheta, I_{\text{ton,LS}}\right)$ as a TSEP, the current sensitivity of the temperature estimation is approximately in the range of $\frac{\partial \vartheta_{\text{vj}}}{\partial I_{\text{ton,LS}}} = 0.9\,\frac{\text{K}}{\text{A}}$ to $2.75\,\frac{\text{K}}{\text{A}}$ at nominal current, see Appendix L.

Including a load resistance and on-state resistance The previous definition of the instantaneous currents (11.16) and (11.17) can be extended using the impacts of an ohmic voltage drop $\Delta I_{\text{ton}}^{(R)}$

$$I_{\text{ton,HS}} := I_{\text{mid}} + \Delta I_{\text{ton,HS}}^{(d_1,d_2,T_{\text{D}})} + \Delta I_{\text{ton,HS}}^{(R)}, \tag{11.20}$$

$$I_{\text{ton,LS}} := I_{\text{mid}} + \Delta I_{\text{ton,LS}}^{(d_1,d_2,T_{\text{D}})} + \Delta I_{\text{ton,LS}}^{(R)}. \tag{11.21}$$

For simplicity, the ohmic voltage drop is modeled as constant during the PWM period $U = R\overline{I}$, using the average current measurement from the inverter sensor $\overline{I}$. This simplification should have little impact at high load current, where the current ripple is small compared to the load currents. At low load currents, the error made by this simplification increases, as the current ripple becomes more relevant compared to the load current.

The current deviation between the midpoint of the PWM period and the instantaneous turn-on currents caused solely by an ohmic voltage drop can be described as

$$\Delta I_{\text{ton,HS}}^{(R)} = -\left(\frac{T_{\text{pwm}}}{2} - t_{\text{on,HS}}\right)\frac{R\overline{I}}{L} = \left(d_i - 1\right)\frac{T_{\text{pwm}}}{2}\frac{R\overline{I}}{L} - \frac{T_{\text{D}}R\overline{I}}{L}, \quad i \in \{1,2\} \tag{11.22}$$

$$\Delta I_{\text{ton,LS}}^{(R)} = -\left(t_{\text{on,LS}} - \frac{T_{\text{pwm}}}{2}\right)\frac{R\overline{I}}{L} = \left(d_i - 1\right)\frac{T_{\text{pwm}}}{2}\frac{R\overline{I}}{L} - \frac{T_{\text{D}}R\overline{I}}{L}. \tag{11.23}$$

The effects are symmetrical and independent of the switching state of the other half-bridge. The on-state resistance $R_{\text{ds,on}}$ of the MOSFETs can be easily incorporated into the model by assuming that the voltage drop across the on-state resistance is part of the load, while the MOSFETs are conducted without losses

$$R = R_{\text{L}} + 2R_{\text{ds,on}}, \tag{11.24}$$

$$U_{\text{ds,on}} = 0\,\text{V}. \tag{11.25}$$

The laboratory setup has a total resistance R of approximately $100\,\text{m}\Omega$, causing up to 0.56 A difference at I_{N}. This value was determined from multiple measurements of the current slope during the central current plateau, see Figure 11.4.

Preliminary experimental validation A preliminary experimental validation of the model showed that the measured and predicted current steps within a PWM period match in their order of magnitude, but the measurement also revealed a key difference between the model shown Figure 11.3 and the laboratory setup, which will be discussed in this paragraph.

Figure 11.4 depicts the measured load current during one PWM period of the full-bridge setup. The applied duty cycles in this period are known. The duration of the current slopes is too short to be visible in this measurement, but the resulting current step can be extracted from the remaining three regions, see the orange lines.

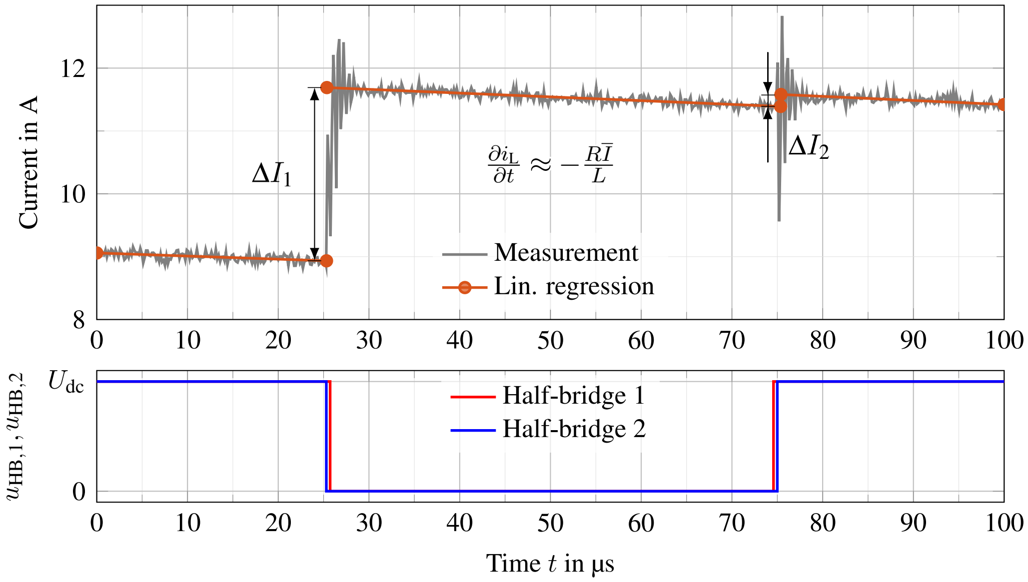

Figure 11.4: Measured load current during one PWM period; extracted from a 1 Hz load signal; applied duty cycles were recorded; the bottom graph shows the expected switching signals of both half-bridges without considering a phase shift; predicted effects of the interlock times are included in the switching signals

A symmetrical, single-edged PWM waveform with no carrier shifts is assumed for the initial current model. Contradicting the expectations, the observed first I_1 and second I_2 current steps in the PWM period are not of the same size.

A large number of measurements at load current levels of $\overline{I} \in (-I_N, +I_N)$ are available. It can be seen that the sums of the expected current steps match the sum of the measured current steps. Several other waveform examples are shown in Appendix H. A detailed analysis of the data follows in Section 11.2.4. The difference between the first and second current step, while maintaining the sum of the current steps, clearly indicates a phase shift between the carriers of the half-bridges.

11.2 Extended current model

The preliminary experimental validation revealed significant discrepancies between the basic model presented in Section 11.1 and the measurement. Here, the model will be extended to incorporate two further effects. First, the effects of the node capacitance on the output voltage are considered [153, 154]. Second, the effects of a carrier shift between the switching signals of the two half-bridges are considered. Additionally, the turn-on delay times and turn-off delay times are considered in the model, but their effect is small compared to the other effects. Jitter is not considered.

11.2.1 Effects of the node capacitance

Figure 11.5 shows the drain-source voltage $u_{ds}^{(LS)}$ of the low-side switch during the interlock time for different load currents being sourced from the phase terminal, i.e., $\overline{I} < 0\,\mathrm{A}$.

The switching process of the half-bridge begins with the turn-off of the high-side switch

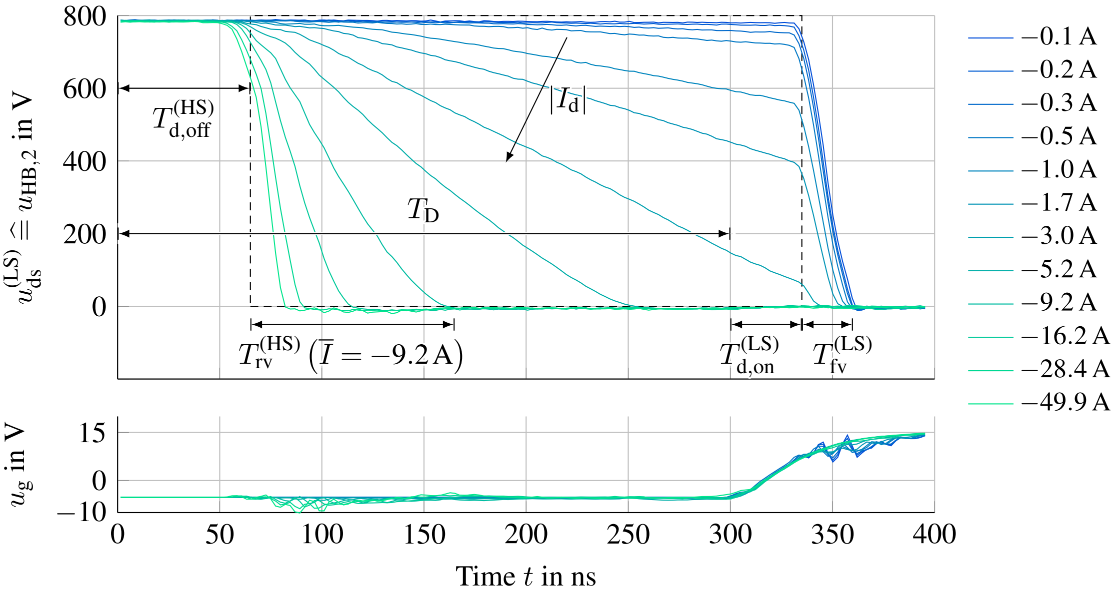

Figure 11.5: Examples of the output voltage of half-bridge during the interlock times at different load currents; $t = 0$ marks the beginning of the turn-off process of the high-side switch

at $t = 0\,\mathrm{s}$. A turn-off delay $T_{\mathrm{d,off}} \approx 65\,\mathrm{ns}$ occurs before the voltage of the low-side switch begins to fall/high-side switch begins to rise, due to the time needed to discharge the gate capacitance. The level of detail of the current model must be reduced significantly compared to the level of detail used in the TSEP descriptions. Therefore, the turn-on delay $T_{\mathrm{d,on}}$ and turn-off delay $T_{\mathrm{d,off}}$ are modeled as constants in this chapter.

After the high-side switch has turned off, the load current begins to charge (or discharge) the node capacitance C_{node}. The output voltage of the half-bridge changes continuously according to the state of charge of C_{node}. Even though the voltage dependency of the output capacitance of the switches C_{oss} is nonlinear, the voltage error caused by the charging process can be described with a linear change in output voltage due to symmetry effects. See Appendix I for details. The charging of the node capacity only occurs if the load current polarity leads to a current commutation to the partner switch's body diode.

The incorrectly output voltage-time integral caused by the charging of C_{node} increases with decreasing current. If the charging process is not finished before the low-side switch turns on, see Figure 11.5 at approximately 335 ns, the remaining charge is discharged through the low-side switch, thereby limiting the maximum voltage rise time $T_{\mathrm{rv}}^{(\mathrm{HS})}$ to a maximum duration of $\max(T_{\mathrm{rv}}) = T_{\mathrm{D}} + T_{\mathrm{d,on}} - T_{\mathrm{d,off}}$. Here, this occurs at load currents $\overline{I}$ smaller than approximately 2 A.

For now, the charge is estimated to be $\Delta Q_{\mathrm{node}} = 587\,\mathrm{nC}$ from the output capacitances stated in the datasheets, see Appendix I. The load current $\overline{I}$ is assumed to be constant. The voltage rise time $T_{\mathrm{rv}}^{(\mathrm{HS})}$ of the high-side switch necessary to fully change the output voltage of the phase terminal from U_{dc} to 0 V or vice versa can be described by the total charge

ΔQ_{node} required to achieve this

$$\Delta Q_{\text{node}} = C_{\text{node}}\left(U_{\text{dc}} - 0\,\text{V}\right), \tag{11.26}$$

$$T_{\text{rv}} \approx \begin{cases} \dfrac{\Delta Q_{\text{node}}}{\overline{I}} & \text{for } \overline{I} \geq \dfrac{\Delta Q_{\text{node}}}{T_{\text{D}} + T_{\text{d,on}} - T_{\text{d,off}}} \approx 2\,\text{A}, \\ T_{\text{D}} + T_{\text{d,on}} - T_{\text{d,off}} & \text{for } \overline{I} < \dfrac{\Delta Q_{\text{node}}}{T_{\text{D}} + T_{\text{d,on}} - T_{\text{d,off}}}, \end{cases} \tag{11.27}$$

The largest impact this effect can have on the load is

$$\max \Delta I^{(T_{\text{rv}})} = \frac{U_{\text{dc}}}{L}\left(T_{\text{D}} + T_{\text{d,on}} - T_{\text{d,off}}\right) \approx 1\,\text{A}. \tag{11.28}$$

The values used to estimate these results are listed in Table 11.2.

Table 11.2: Values used for magnitude estimations

U_{dc}	L	T_{D}	$T_{\text{d,on}}$	$T_{\text{d,off}}$	T_{fv}	ΔQ_{node}	T_{pwm}
800 V	225 µH	300 ns	35 ns	65 ns	20 ns	587 nC	100 µs

The resulting error Φ of the voltage-time integral can be separated into two cases, depending on whether or not the charging process of C_{node} has finished before the low-side switch is turned on

$$\max\left(T_{\text{rv}}\right) = T_{\text{D}} + T_{\text{d,on}} - T_{\text{d,off}}, \tag{11.29}$$

$$\Phi = U_{\text{dc}}\frac{T_{\text{rv}}}{2} = \begin{cases} \dfrac{U_{\text{dc}}\Delta Q_{\text{node}}}{2\overline{I}} & \text{for } \max\left(T_{\text{rv}}\right)\overline{I} \geq Q_{\text{node}}, \\ U_{\text{dc}}\max\left(T_{\text{rv}}\right) - \dfrac{\overline{I}\max\left(T_{\text{rv}}\right)^2}{2Q_{\text{node}}} & \text{for } \max\left(T_{\text{rv}}\right)\overline{I} < Q_{\text{node}}. \end{cases} \tag{11.30}$$

Impact of the turn-on and turn-off delay times The turn-on and turn-off delay times lead to an error in the voltage-time integral applied to the load inductance. The resulting current error can be estimated to

$$\Delta I^{(T_{\text{d,off}})} = \frac{U_{\text{dc}}}{L}T_{\text{d,off}} \approx 231\,\text{mA}, \tag{11.31}$$

$$0 \leq \Delta I^{(T_{\text{d,on}})} \leq \frac{U_{\text{dc}}}{L}\left(T_{\text{d,on}} + \frac{T_{\text{fv}}}{2}\right) \approx 160\,\text{mA}. \tag{11.32}$$

Although these two effects are small compared to the other discussed effects, and only the difference between the turn-on and turn-off delay time is relevant, integrating them into the current model with fixed times $T_{\text{d,on}}$ and $T_{\text{d,off}}$ does not increase the model complexity notably.

11.2.2 Carrier phase shift

Beside the effects of the interlock time and the node capacitance, the generated switching signal has a propagation delay T_{p}, delaying both edges of the switching signal. This propagation delay leads to a carrier shift between the half-bridges. The propagation delay of the half-bridge under test HB2 is defined to be zero

$$T_{\mathrm{p}} = T_{\mathrm{p}}^{(\mathrm{HB1})} - T_{\mathrm{p}}^{(\mathrm{HB2})}, \quad T_{\mathrm{p}}^{(\mathrm{HB2})} := 0\,\mathrm{s}. \tag{11.33}$$

The propagation delay of the half-bridge HB1 T_{p} is assumed to be small compared to a PWM period $T_{\mathrm{p}} \ll T_{\mathrm{pwm}}$.

The propagation delay affects the switching moments of half-bridge HB1 according to (11.4) and (11.5)

$$t_{\mathrm{off,HS}}^{(\mathrm{HB1})} = d_1 \cdot \frac{T_{\mathrm{pwm}}}{2} + T_{\mathrm{p}}, \qquad t_{\mathrm{off,LS}}^{(\mathrm{HB1})} = T_{\mathrm{pwm}} - d_1 \cdot \frac{T_{\mathrm{pwm}}}{2} + T_{\mathrm{p}}, \tag{11.34}$$

$$t_{\mathrm{on,LS}}^{(\mathrm{HB1})} = d_1 \cdot \frac{T_{\mathrm{pwm}}}{2} + T_{\mathrm{D}} + T_{\mathrm{p}}, \qquad t_{\mathrm{on,HS}}^{(\mathrm{HB1})} = T_{\mathrm{pwm}} - d_1 \cdot \frac{T_{\mathrm{pwm}}}{2} + T_{\mathrm{p}} + T_{\mathrm{D}}. \tag{11.35}$$

The errors in the first and second current steps can be determined from the additional voltage-time integral

$$\Delta I_1^{(d_1,d_2,T_{\mathrm{D}})} + \Delta I_1^{(T_{\mathrm{p}})} = \frac{U_{\mathrm{dc}}}{L}\left(d_1\frac{T_{\mathrm{pwm}}}{2} - d_2\frac{T_{\mathrm{pwm}}}{2} + \mathrm{sgn}\left(\bar{I}\right)T_{\mathrm{D}} + T_{\mathrm{p}}\right) \tag{11.36}$$

$$\Delta I_1^{(T_{\mathrm{p}})} = \frac{U_{\mathrm{dc}}}{L}T_{\mathrm{p}}, \tag{11.37}$$

$$\Delta I_2^{(T_{\mathrm{p}})} = -\frac{U_{\mathrm{dc}}}{L}T_{\mathrm{p}}. \tag{11.38}$$

The resulting errors in the current steps can be interpreted as a differential-mode error between the two steps. The size of the propagation delay will be determined in Section 11.2.4.

11.2.3 Model definitions

The effects of the interlock time T_{D}, the node capacitance C_{node}, the turn-on delay $T_{\mathrm{d,on}}$, the turn-off delay $T_{\mathrm{d,off}}$, and the propagation delay T_{p} are illustrated in Figure 11.6. The top graph, Figure 11.6a, shows the effects on the output voltage, assuming that the average of the output voltage is positive, i.e., $d_1 \gg d_2$. The voltage-time errors Φ are drawn for both load current polarities. The ideal output voltage $u_{\mathrm{out}}^{(\mathrm{ideal})}$ is shown by a dashed line for reference.

The deviation between the modeled output voltage $u_{\mathrm{out}}^{(\mathrm{extended})}$ and the ideal output voltage $u_{\mathrm{out}}^{(\mathrm{ideal})}$ can be positive or negative. The errors in the voltage-time integral caused by different effects and their magnitudes Φ_i are summarized in Table 11.3. Similar to the initial current model, see Section 11.1, the total resulting deviation of the first $\Delta I_1^{(\mathrm{extended})}$ and second $\Delta I_2^{(\mathrm{extended})}$ current steps of the extended current model can be determined from Figure 11.6 and Table 11.3. The resulting instantaneous turn-on currents for the low-side and high-side switches are summarized in Table 11.4, with

$$I_{\mathrm{ton,HS}}^{(\mathrm{extended})} = I_{\mathrm{mid}} + \Delta I_{\mathrm{ton,HS}}^{(\mathrm{extended})}, \tag{11.39}$$

$$I_{\mathrm{ton,LS}}^{(\mathrm{extended})} = I_{\mathrm{mid}} + \Delta I_{\mathrm{ton,LS}}^{(\mathrm{extended})}. \tag{11.40}$$

In two cases of the bottom graph[1], the turn-on process of a switch is already occurring

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[1] Low-side and high-side switch turning on at $\bar{I} \ll 0$ and $d_1 < d_2$

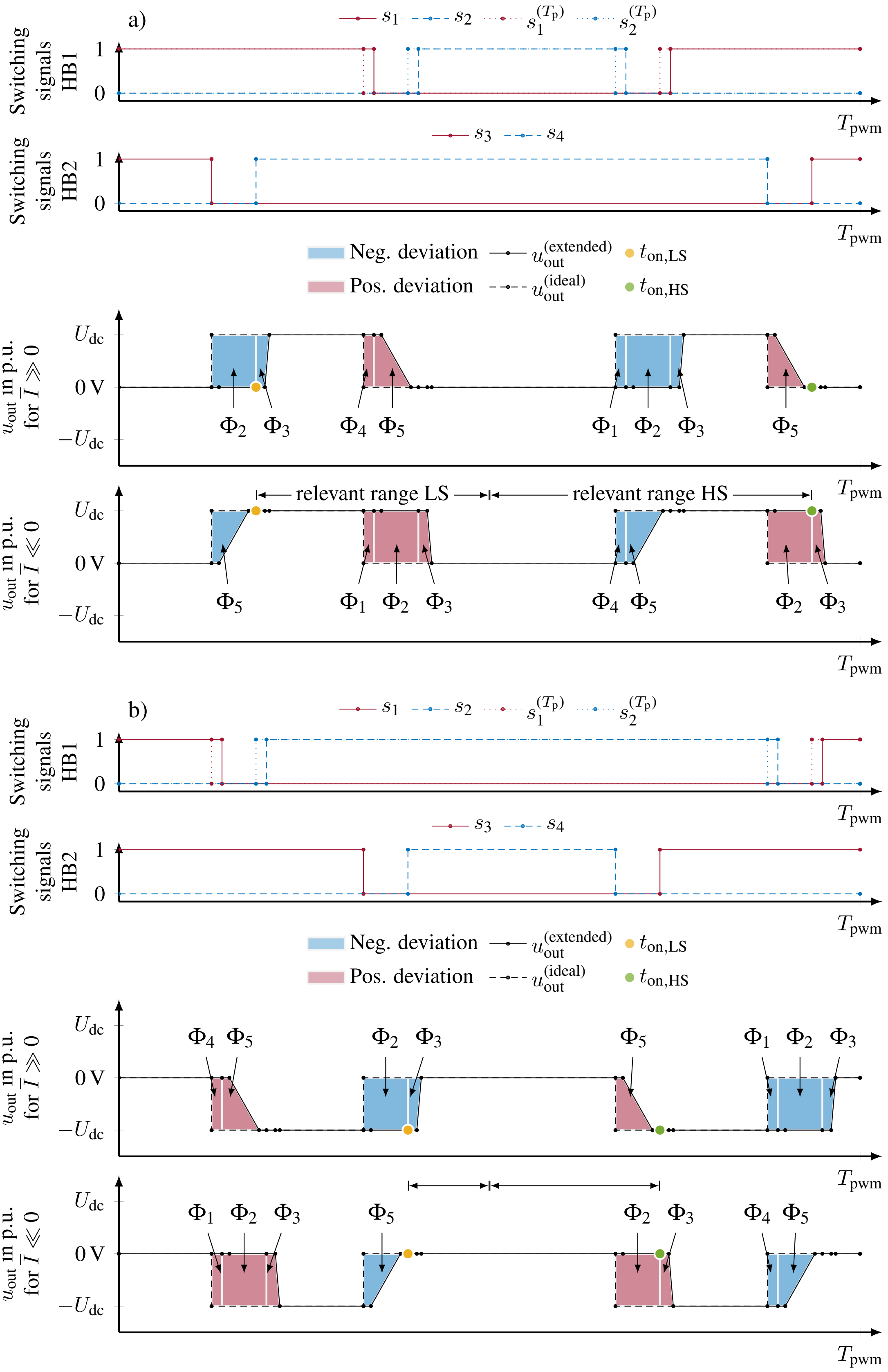

Figure 11.6: Error in the output voltage of the full-bridge; a) positive output voltage $\overline{u}_\mathrm{HB1} > \overline{u}_\mathrm{HB2}$; b) negative output voltage $\overline{u}_\mathrm{HB1} < \overline{u}_\mathrm{HB2}$; effects not drawn to scale

Table 11.3: Impacts on the voltage-time integral and their magnitudes

Factor	Voltage-time integral
Ideal case	$\Phi_{\text{ideal}} = (d_1 - d_2)\,\frac{T_{\text{pwm}}}{2} U_{\text{dc}}$
Propagation delay	$\lvert\Phi_1\rvert = T_{\text{p}} U_{\text{dc}}$
Interlock time	$\lvert\Phi_2\rvert = T_{\text{D}} U_{\text{dc}}$
Turn-on delay	$\lvert\Phi_3\rvert = \left(T_{\text{d,on}} + \frac{T_{\text{fv}}}{2}\right) U_{\text{dc}}$
Propagation delay	$\lvert\Phi_4\rvert = T_{\text{p}} U_{\text{dc}}$
Turn-off delay and node capacitance	$\lvert\Phi_5(\overline{I})\rvert = \begin{cases} U_{\text{dc}} T_{\text{d,off}} + \dfrac{U_{\text{dc}} Q_{\text{node}}}{2\overline{I}}, & \text{for } \max(T_{\text{rv}})\,\overline{I} \geq Q_{\text{node}} \\ U_{\text{dc}} T_{\text{d,off}} + U_{\text{dc}} \left(\max(T_{\text{rv}}) - \dfrac{\overline{I} \max(T_{\text{rv}})^2}{2 Q_{\text{node}}}\right), & \text{for } \max(T_{\text{rv}})\,\overline{I} < Q_{\text{node}} \end{cases}$

during the central plateau of the output voltage and no current step exists between the current at the midpoint of the PWM period I_{mid} and the instantaneous turn-on currents I_{ton}. In all other cases, the voltage-time integrals Φ_i between the turn-on moment and the midpoint of the PWM period must be accounted for. Special attention should be paid to the duty cycle conditions of the cases. If the propagation delay T_{p} is large compared to the ideal width of the output voltage pulses T_{ideal}, a case can occur where the first and second current steps have opposite signs. Consequently, this is an edge case, where one turn-on process of half-bridge HB2 occurs after its corresponding current step and one turn-on process occurs before its corresponding current step. The case decisions for the high-side and low-side switch can differ. This is reflected by the different boundary conditions of the duty cycles for the high-side and low-side current corrections in Table 11.4.

11.2.4 Estimating nonideal switching parameters

The extended current model developed requires the propagation delay T_{p}, as well as the node capacitance C_{node}, as parameters. In this section, these parameters are determined from measured current steps during PWM periods, as shown in Figure 11.4. The basis for these measurements is formed by the overall current steps ΔI_1 and ΔI_2, not the current steps between the current at the midpoint of the PWM period I_{mid} and the instantaneous current at turn-on $\Delta I_{\text{ton,HS}}^{(\text{extended})}$ or $\Delta I_{\text{ton,LS}}^{(\text{extended})}$, see Figure 11.7

Measurement A low-frequency load current, with an amplitude matching the nominal current of the power modules, is applied to the load. During the measurement, the duty cycles d_1 and d_2 are recorded in the gate driver control unit on a firmware level. These recorded values are unaffected by external influences like propagation delays or measurement noise.

Additionally, a current probe and an oscilloscope are attached to the load to measure the current waveforms during the PWM periods, as shown in Figure 11.4. The oscilloscope and the control unit's duty cycle data are synchronized. For each measurement, the expected current steps based on the initial current model, $\Delta I_1^{(\text{ideal})}$ and $\Delta I_2^{(\text{ideal})}$, are calculated. From the oscilloscope measurement, the actual current steps, $\Delta I_1^{(\text{meas})}$ and $\Delta I_2^{(\text{meas})}$, are determined. The differences between the expected current steps and the measured current steps are plot-

Table 11.4: Voltage-time error for the full-bridge; extended model

	Current polarity	Condition	$\Delta I_{\text{ton}}^{(\text{extended})}$
$\Delta I_{\text{ton,HS}}^{(\text{extended})}$	$\overline{I} \gg 0$	$(1-d_1)\frac{T_{\text{pwm}}}{2}+T_{\text{D}}+T_{\text{p}} \leq (1-d_2)\frac{T_{\text{pwm}}}{2}$	$\frac{1}{L}\left(U_{\text{dc}}T_{\text{ideal}}-\lvert\Phi_1\rvert-\lvert\Phi_2\rvert-\lvert\Phi_3\rvert+\left\lvert\Phi_5\left(\overline{I}\right)\right\rvert\right)$
		$(1-d_1)\frac{T_{\text{pwm}}}{2}+T_{\text{D}}+T_{\text{p}} > (1-d_2)\frac{T_{\text{pwm}}}{2}$	$\frac{1}{L}\left(\left\lvert\Phi_5\left(\overline{I}\right)\right\rvert\right)$
	$\overline{I} \ll 0$	$(1-d_1)\frac{T_{\text{pwm}}}{2}+T_{\text{p}} \leq (1-d_2)\frac{T_{\text{pwm}}}{2}+T_{\text{D}}$	$\frac{1}{L}\left(U_{\text{dc}}T_{\text{ideal}}+\lvert\Phi_2\rvert-\lvert\Phi_4\rvert-\left\lvert\Phi_5\left(\overline{I}\right)\right\rvert\right)$
		$(1-d_1)\frac{T_{\text{pwm}}}{2}+T_{\text{p}} > (1-d_2)\frac{T_{\text{pwm}}}{2}+T_{\text{D}}$	$\frac{1}{L}\left(\lvert\Phi_2\rvert\right)$
$\Delta I_{\text{ton,LS}}^{(\text{extended})}$	$\overline{I} \gg 0$	$d_1\frac{T_{\text{pwm}}}{2}+T_{\text{p}} \geq d_2\frac{T_{\text{pwm}}}{2}+T_{\text{D}}$	$\frac{1}{L}\left(U_{\text{dc}}T_{\text{ideal}}-\lvert\Phi_2\rvert-\lvert\Phi_3\rvert+\lvert\Phi_4\rvert+\left\lvert\Phi_5\left(\overline{I}\right)\right\rvert\right)$
		$d_1\frac{T_{\text{pwm}}}{2}+T_{\text{p}} < d_2\frac{T_{\text{pwm}}}{2}+T_{\text{D}}$	$-\lvert\Phi_3\rvert$
	$\overline{I} \ll 0$	$d_1\frac{T_{\text{pwm}}}{2}+T_{\text{D}}+T_{\text{p}} \geq d_2\frac{T_{\text{pwm}}}{2}$	$\frac{1}{L}\left(U_{\text{dc}}T_{\text{ideal}}+\lvert\Phi_1\rvert+\lvert\Phi_3\rvert\right)$
		$d_1\frac{T_{\text{pwm}}}{2}+T_{\text{D}}+T_{\text{p}} < d_2\frac{T_{\text{pwm}}}{2}$	0

ted in Figure 11.8. The results show that the first step is generally larger than expected,

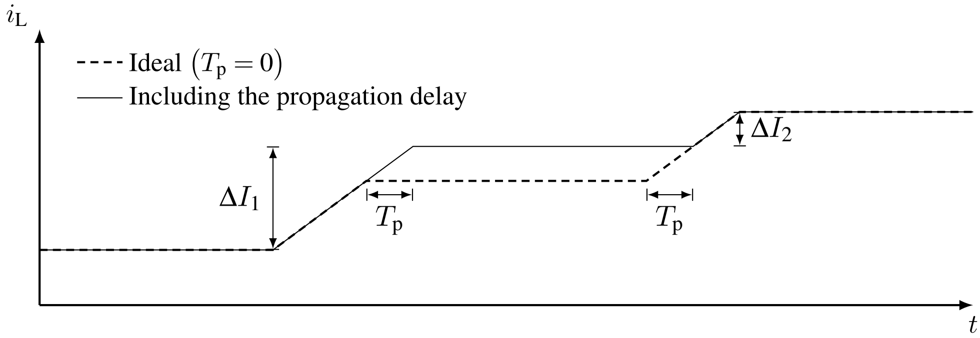

Figure 11.7: Definition of the current steps ΔI_1 and ΔI_2 used to estimate nonideal switching parameters

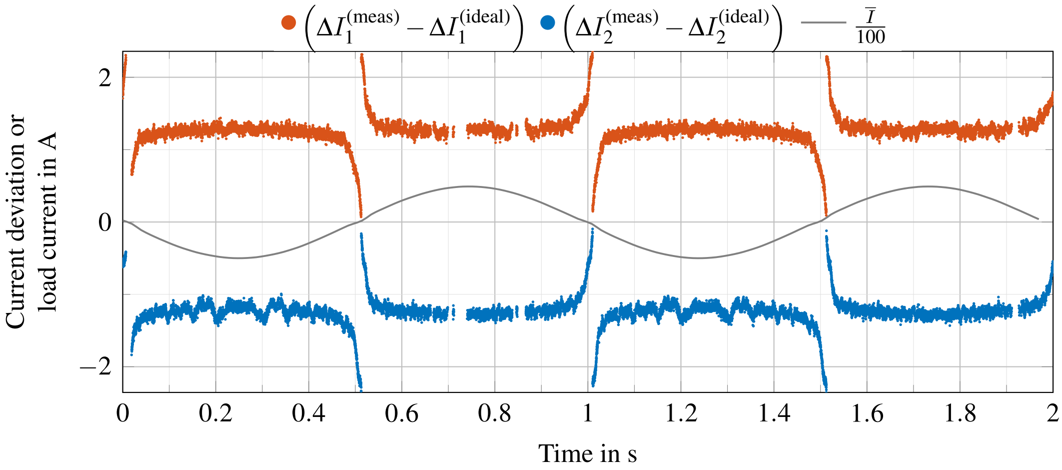

Figure 11.8: Current step differences between the measured current steps and the expected current steps using the initial current model; a 1 Hz load current at a switching frequency of 10 kHz is applied

while the second step is generally smaller than expected. The size differences in both steps are in the same order of magnitude. It can be assumed that a positive propagation delay $T_p > 0\,\mathrm{s}$ affects half-bridge HB1.

Value extraction Before extracting the required parameters from the measurement data, the data is preprocessed. The carrier shift, or propagation delay of the half-bridge HB1, affects the size of the first and second current steps with an opposite sign. All other effects impact both current steps in the same way. Therefore, the current steps ΔI_1 and ΔI_2 can be described as a common-mode component and a differential-mode component

$$\Delta I_{\text{cm}} := \frac{\Delta I_1 + \Delta I_2}{2}, \tag{11.41}$$

$$\Delta I_{\text{dm}} := \frac{\Delta I_1 - \Delta I_2}{2}. \tag{11.42}$$

According to Figure 11.6 and Table 11.3, the common-mode component can be described as

$$\begin{align}
\Delta I_{\mathrm{cm}} &= \frac{1}{L}\Big(U_{\mathrm{dc}}T_{\mathrm{ideal}} - \operatorname{sgn}\left(\bar{I}\right)|\Phi_2| - \operatorname{sgn}\left(\bar{I}\right)|\Phi_3| + \overbrace{\frac{|\Phi_4|}{2} - \frac{|\Phi_1|}{2}}^{\text{effects of } T_{\mathrm{p}} \text{ are eliminated}} + \operatorname{sgn}\left(\bar{I}\right)\left|\Phi_5\left(\bar{I}\right)\right|\Big) \tag{11.43}\\
&= \frac{U_{\mathrm{dc}}}{L}\left(T_{\mathrm{ideal}} - \operatorname{sgn}\left(\bar{I}\right)\left(T_{\mathrm{D}} + T_{\mathrm{d,on}} + \frac{T_{\mathrm{fv}}}{2} - T_{\mathrm{d,off}} - \frac{\Delta Q_{\mathrm{node}}}{2\bar{I}}\right)\right), \quad \bar{I} > 2\,\mathrm{A}. \tag{11.44}
\end{align}$$

This equation simply states, that all effects described, except for the effects of the propagation delay T_{p}, affect the first and second current step with the same value and polarity. For simplicity, the case where the node capacitance has not fully changed its charge state when the turn-on process begins is excluded. The impact of the propagation delays, Φ_1 and Φ_4, is eliminated in the common-mode representation of the currents (11.44).

The differential mode is given by

$$\begin{align}
\Delta I_{\mathrm{dm}} = \frac{1}{2L}\big(&-\operatorname{sgn}\left(\bar{I}\right)|\Phi_2| - \operatorname{sgn}\left(\bar{I}\right)|\Phi_3| + |\Phi_4| + \operatorname{sgn}\left(\bar{I}\right)\left|\Phi_5\left(\bar{I}\right)\right| \tag{11.45}\\
&+ |\Phi_1| + \operatorname{sgn}\left(\bar{I}\right)|\Phi_2| + \operatorname{sgn}\left(\bar{I}\right)|\Phi_3| - \operatorname{sgn}\left(\bar{I}\right)|\Phi_5|\big) \notag\\
= \frac{U_{\mathrm{dc}}}{L}\frac{T_{\mathrm{p}}}{2}&. \tag{11.46}
\end{align}$$

The effects of the propagation delay T_{p} are the only modeled effects visible in the differential mode. Based on (11.44) and (11.46), the propagation delay T_{p} and the difference ΔT_{D} between the set interlock time T_{D} and the effective floating time of the phase terminal can be determined

$$\begin{align}
T_{\mathrm{p}} &= \frac{2\Delta I_{\mathrm{dm}}L}{U_{\mathrm{dc}}} \tag{11.47}\\
\Delta T_{\mathrm{D}} &:= \left(T_{\mathrm{D}} + T_{\mathrm{d,on}} + \frac{T_{\mathrm{fv}}}{2} - T_{\mathrm{d,off}} - \frac{\Delta Q_{\mathrm{node}}}{\bar{I}}\right) - T_{\mathrm{D}} \tag{11.48}\\
&= T_{\mathrm{d,on}} + \frac{T_{\mathrm{fv}}}{2} - T_{\mathrm{d,off}} - \frac{\Delta Q_{\mathrm{node}}}{\bar{I}} \tag{11.49}\\
&= \frac{U_{\mathrm{dc}}T_{\mathrm{ideal}} - \Delta I_{\mathrm{cm}}L}{U_{\mathrm{dc}}\operatorname{sgn}\left(\bar{I}\right)} \tag{11.50}\\
&= \left(T_{\mathrm{ideal}} - \frac{\Delta I_{\mathrm{cm}}L}{U_{\mathrm{dc}}}\right)\operatorname{sgn}\left(\bar{I}\right). \tag{11.51}
\end{align}$$

The current step data shown in Figure 11.8 is mapped to their corresponding common-mode and differential-mode components, according to (11.41) and (11.42). Then, the propagation delay T_{p} and the difference ΔT_{D} between the interlock time and the effective floating time of the phase terminal are determined according to (11.47) and (11.51). The results are shown in Figure 11.9. For currents below 10 A, a significant difference between the effective floating time of the half-bridge and the expected effect of the interlock time can be seen. At current levels below $\bar{I} \approx 2\,\mathrm{A}$, the effects of the node capacitance necessitate a switch to the

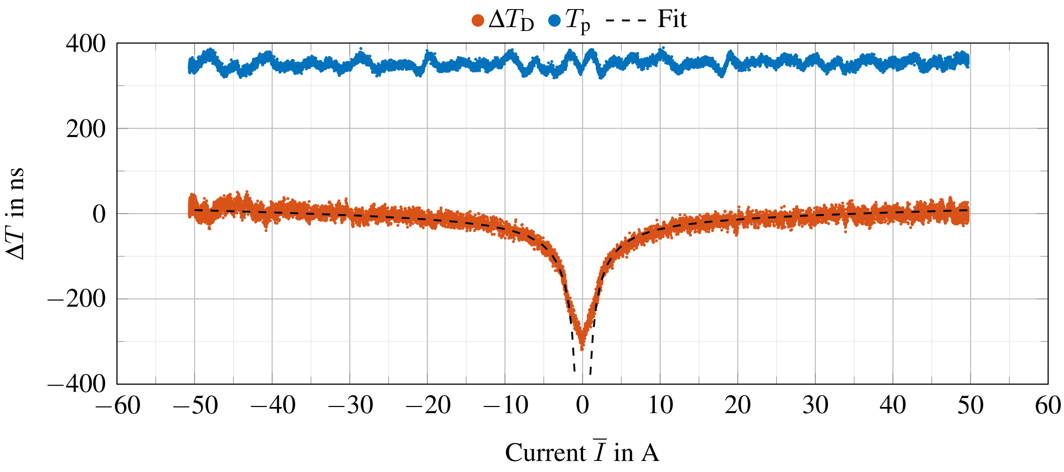

Figure 11.9: Estimated parameters from the current step differences between the measured current steps and the expected current steps using the initial current model

case where the node capacitance has not fully changed its charge stage before the turn-on process at the end of the interlock time begins. This is reflected by a changing curve shape of ΔT_D in Figure 11.9. The smallest value of ΔT_D should be limited by $\Delta T_\mathrm{D} \approx -T_\mathrm{D} = -300\,\mathrm{ns}$, which is when the second switch turns on after the interlock time. This limitation can clearly be seen in the results.

The propagation delay T_p of half-bridge HB1 can be estimated to be

$$T_\mathrm{p} \approx 352\,\mathrm{ns} \mathrel{\widehat{=}} 0.0035 T_\mathrm{pwm}. \tag{11.52}$$

Although this phase shift accounts for only 0.35 % of the duration of the PWM period, a significant current error arises if it is not accounted for

$$\Delta I \approx T_\mathrm{p} \frac{U_\mathrm{dc}}{L} = 1.3\,\mathrm{A} \mathrel{\widehat{=}} 2.6\,\% I_\mathrm{N}. \tag{11.53}$$

Figure 11.9 also shows a fit for ΔT_D to estimate the node charge $Q_\mathrm{node}\,(U_\mathrm{dc} = 800\,\mathrm{V})$, using the fit model and results

$$\Delta T_\mathrm{D}^{*} = -\frac{Q_\mathrm{node}}{2\left|\overline{I}\right|} + a\left|\overline{I}\right| + b, \quad \left|\overline{I}\right| > 2\,\mathrm{A} \tag{11.54}$$

$$Q_\mathrm{node} = 753.3\,\mathrm{nC}, \quad a = 0.35\,\frac{\mathrm{ns}}{\mathrm{A}}, \quad b = -1.6\,\mathrm{ns}. \tag{11.55}$$

The node charge is greater than assumed from the output capacitances of the MOSFETs, see Table 11.2. This is expected, as the capacitance between the DCB substrate and the cooler, as well as any capacitances of the load or load cables are neglected. The linear dependency on the current accounts for changes in the difference between the turn-on delay time $T_\mathrm{d,on}$ and the turn-off delay time $T_\mathrm{d,off}$ depending on the load current (11.49)

$$a\left|\overline{I}\right| + b \mathrel{\widehat{=}} T_\mathrm{d,on}\left(\overline{I}\right) + \frac{T_\mathrm{fv}\left(\overline{I}\right)}{2} - T_\mathrm{d,off}\left(\overline{I}\right). \tag{11.56}$$

The results for a and b in (11.55) match the expectations based on the TSEP measurement results given in Chapter 10 and are within 7 ns of the preliminary estimated times at a current of $\overline{I} = 0.5 I_\mathrm{N} = 25\,\mathrm{A}$, see Table 11.2.

11.2.5 Difference between the average current and the current at the midpoint of the PWM period

The starting point of the extended model is the current I_mid at the midpoint of the PWM period. In the given test setup, only the average current $\overline{I}$ of the PWM period is available. Before the model can be applied, the effects of the current waveform asymmetry on the average current $\overline{I}$ and the current I_mid at the midpoint of the PWM period must be determined. As described at the beginning of this chapter, both values are equal as long as the waveform is centrosymmetric with regard to the midpoint of the PWM period. There are two effects in the extended model that lead to asymmetry of the current waveform, namely the effects of the interlock time and the propagation delay.

Impact of the interlock times The ideal switching moments are symmetrically placed around the midpoint of the PWM period. The interlock times are always appended to the ideal switching moment, therefore introducing current waveform asymmetry.

This effect is depicted in Figure 11.10. The illustration is based on the initial current model for a positive current $\overline{I} \gg 0$ and a positive output voltage $u_\mathrm{out} > 0$ of the full-bridge, see Figure 11.3. The interlock time delays the start of each output voltage pulse by T_D. The resulting reduction in the current steps ΔI does not affect the symmetry, while the delay of the second pulse leads to asymmetry.

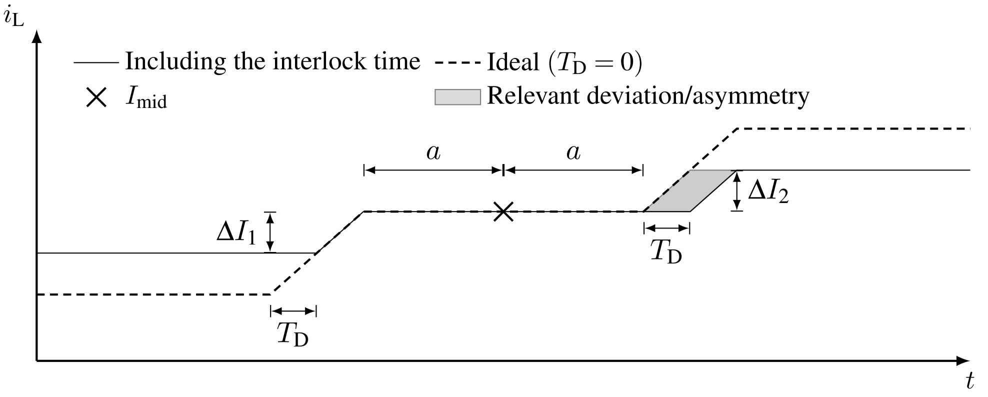

Figure 11.10: Impact of the effects of the interlock time on the symmetry of the current waveform for a positive current; not to scale

The difference between the average current value $\overline{I}$ and the current at the midpoint I_mid is given by

$$
\begin{aligned}
\overline{I} &= \frac{1}{T_\mathrm{pwm}} \int\limits_0^{T_\mathrm{pwm}} (i_\mathrm{L})\,\mathrm{d}t, \quad I_\mathrm{mid} = i_\mathrm{L}\Big|_{\frac{T_\mathrm{pwm}}{2}} && (11.57)\\
&= \frac{1}{T_\mathrm{pwm}} \left(I_\mathrm{mid} T_\mathrm{pwm} - \Delta I_2 T_\mathrm{D}\right), && (11.58)\\
\overline{I} - I_\mathrm{mid} &= -\Delta I_2 \underbrace{\frac{T_\mathrm{D}}{T_\mathrm{pwm}}}_{\approx 0.3\,\%}. && (11.59)
\end{aligned}
$$

The resulting difference between the average current $\overline{I}$ and the current I_mid at the midpoint of the PWM period depends on the current step ΔI_2 and the ratio of the interlock time and the PWM period. In the given test setup, the relative length of the interlock time is only approximately 0.3 % of the PWM period. The effects of the interlock-time-dependent asymmetry are neglected.

Impact of the propagation delay The impact of the propagation delay T_p, or a carrier shift, is much greater than the effects of the interlock times, see Figure 11.11. The symmetry difference between the steps ΔI_1 and ΔI_2 leads to the lifting of the central plateau. This change lasts for the entire duration of the plateau, which is much longer than the effects of the interlock times shown in Figure 11.10. The discrepancy between the average current and

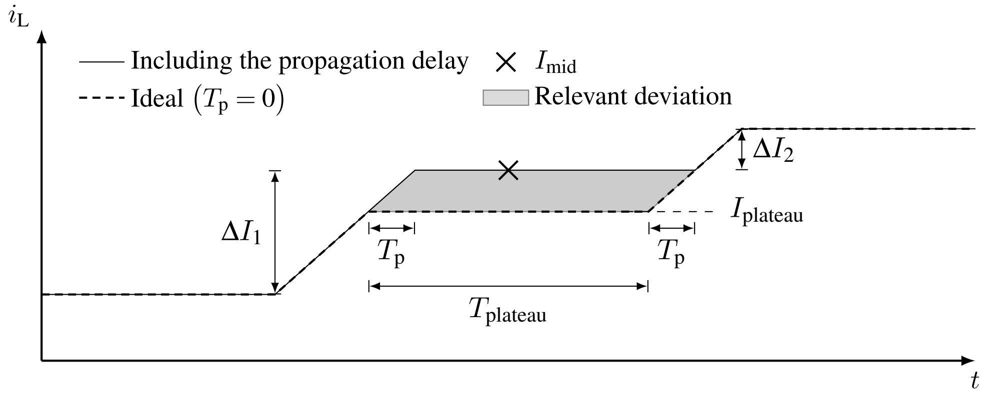

Figure 11.11: Impact of the propagation delay T_p on the symmetry of the current waveform for a positive current; not to scale

the current at the midpoint is

$$\overline{I} = \frac{1}{T_{\mathrm{pwm}}} \int_{0}^{T_{\mathrm{pwm}}} (i_{\mathrm{L}})\,\mathrm{d}t, \quad I_{\mathrm{mid}} = i_{\mathrm{L}}\big|_{\frac{T_{\mathrm{pwm}}}{2}} \tag{11.60}$$

$$\overline{I} = \frac{1}{T_{\mathrm{pwm}}} \left(I_{\mathrm{plateau}} T_{\mathrm{pwm}} + \left(I_{\mathrm{mid}} - I_{\mathrm{plateau}}\right) T_{\mathrm{plateau}}\right), \tag{11.61}$$

$$I_{\mathrm{plateau}} = I_{\mathrm{mid}} + \frac{\Delta I_2}{2} - \frac{\Delta I_1}{2} = I_{\mathrm{mid}} - T_{\mathrm{p}} \frac{U_{\mathrm{dc}}}{L}, \tag{11.62}$$

$$T_{\mathrm{plateau}} = \min(d_1, d_2) T_{\mathrm{pwm}} + T_{\mathrm{D}}, \tag{11.63}$$

$$\overline{I} = I_{\mathrm{mid}} - T_{\mathrm{p}} \frac{U_{\mathrm{dc}}}{L} + T_{\mathrm{p}} \frac{U_{\mathrm{dc}}}{L} \frac{\min(d_1, d_2) T_{\mathrm{pwm}} + T_{\mathrm{D}}}{T_{\mathrm{pwm}}}, \tag{11.64}$$

$$\overline{I} - I_{\mathrm{mid}} = \left(\min(d_1, d_2) - 1 + \frac{T_{\mathrm{D}}}{T_{\mathrm{pwm}}}\right) T_{\mathrm{p}} \frac{U_{\mathrm{dc}}}{L}. \tag{11.65}$$

Assuming that the lowest duty cycle is $d_1 = 50\,\%$, the propagation delay $T_{\mathrm{p}} = 352\,\mathrm{ns}$ determined for this setup causes a discrepancy between the average current and the current at the midpoint of approximately
$\overline{I} - I_{\mathrm{mid}} = -0.6\,\mathrm{A}$.

11.2.6 Model application

The average current $\overline{I}$ is acquired once per PWM period using the inverter sensor (ΣΔ). For each measurement, the following correction steps are needed to determine the instantaneous turn-on current for one switch.

1. Correct the discrepancy between the average current $\overline{I}$ and the current I_{mid} at the midpoint of the PWM period.
2. Determine the correction case, depending on the duty cycles and the load current polarity, according to Table 11.4.
3. Add the current steps $\Delta I_{\mathrm{ton}}^{(\mathrm{extended})}$ to I_{mid}, according to Table 11.4, to account for the following effects:
   a) applied duty cycles,
   b) interlock times,
   c) turn-on delay, turn-off delay and voltage fall time after turn-on,
   d) charging of the node capacitance,
   e) carrier phase shift or propagation delay
4. Add the current difference $\Delta I_{\mathrm{ton}}^{(R)}$, according to (11.22) and (11.23), to compensate the effects of an ohmic load and the on-state resistance of the semiconductors

The test setup employed does not have a load voltage u_{i} beside the ohmic voltage drop, see Figure 11.1. If the current model concepts were applied to an electrical machine, the model could be expanded to incorporate the current deviation caused by the load voltage u_{i}.

11.3 Experimental validation

The measurement and fit results shown in Figure 11.9 have already validated the fact that the extended current model is capable of describing the sizes of the first and second current steps of the PWM periods. Unfortunately, the turn-on moment can also occur during the current slopes. Another experiment is conducted, where the predicted instantaneous current at turn-on $I_{\mathrm{ton,LS}}$ of the extended model is compared to a measurement.

The experimental setup is shown in Figure 11.12. The full-bridge is operated in PWM mode, while an additional high-bandwidth current transducer and an oscilloscope are attached to the load. The gate signal s_4 is used to trigger an oscilloscope sample of the load current right at the turn-on $t_{\mathrm{on,LS}}$ of the DUT. The current measured by the oscilloscope $I_{\mathrm{scope}}\left(t_{\mathrm{on,LS}}\right)$ serves as a reference for the actual instantaneous current at turn-on.

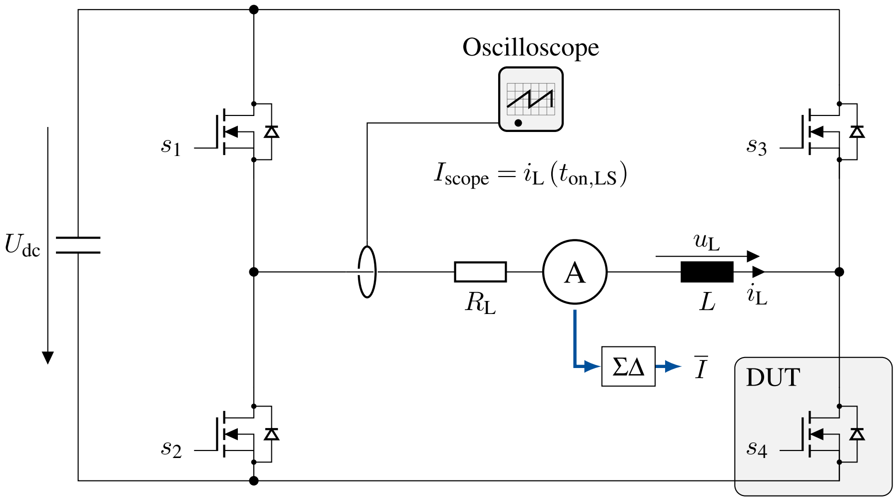

Figure 11.12: Experimental setup; the oscilloscope is set up to sample the load current i_{L} right at the turn-on moment $t_{\mathrm{on,LS}}$ of the low-side switch of the half-bridge HB2. The gate signal s_4 is used as a trigger. A 10 MHz current transducer is used as a probe.

Figure 11.13 depicts the measured average current $\overline{I}$ acquired from the inverter sensor, the instantaneous turn-on current measured by the oscilloscope I_{scope}, together with the instantaneous turn-on current $I_{\mathrm{ton,LS}}$ predicted by the model. The top graph shows that the relative current difference between the average current and the instantaneous current is generally small. Nevertheless, this deviation leads to a notable temperature estimation error when using TSEPs. The bottom graph depicts the deviations of the average current measurement $\overline{I}$ and the predicted instantaneous current $I_{\mathrm{ton,LS}}$ from the oscilloscope value I_{scope}. It can be seen that the deviation can be reduced by a factor of three to six. When the current is near zero, the predicted current is discontinuous. Edge cases close to a current of zero were excluded from the model.

The TSEP-based temperature estimation, using the current rise time $t_{\mathrm{ri}}\left(\vartheta, I_{\mathrm{ton,LS}}\right)$, has an approximate current sensitivity of $\frac{\partial \vartheta_{\mathrm{vj}}}{\partial I_{\mathrm{ton,LS}}} \approx 0.9\,\frac{\mathrm{K}}{\mathrm{A}}$ to $2.75\,\frac{\mathrm{K}}{\mathrm{A}}$ at nominal current, see Appendix L. As a result, using the average current $\overline{I}$ can lead to a temperature estimation deviation of up to 4 K. When using the model-corrected current $I_{\mathrm{ton,LS}}$, the temperature deviation is approximately 1.5 K.

It should be noted that the current differences plotted on the bottom graph of Figure 11.13

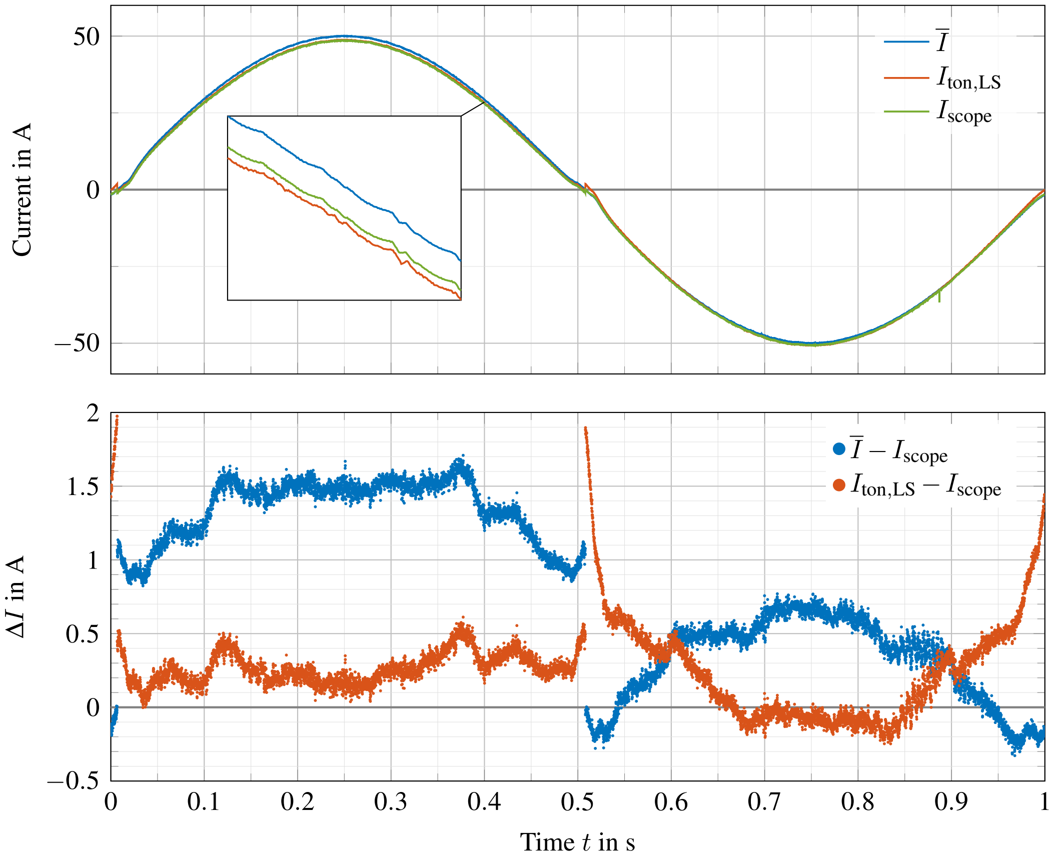

Figure 11.13: Average current measurement provided by the inverter sensor $\overline{I}$ compared to the instantaneous current at turn-on $I_{\mathrm{ton,LS}}$, determined using the extended current model; the instantaneous current at turn-on is also measured with a current transducer and an oscilloscope I_{scope} right before turn-on;

are already considerably below the guaranteed accuracy of the inverter's current sensor[2] and the oscilloscope's probe[3].

11.3.1 Further possible improvements

The measurement results acquired during a negative load current $t > 0.5\,\mathrm{s}$ and depicted in Figure 11.13 show that the instantaneous current $I_{\mathrm{ton,LS}}$ predicted by the model in fact increases the deviation from the actual value I_{scope}, compared to using the unmodified average value $\overline{I}$. This is most likely caused by one of the following model limitations.

First, the model does not include those cases where the load current crosses 0 A during one PWM period. Therefore, all instantaneous current predictions at very low currents are imprecise.

Second, a limit occurs at very low output voltages $\overline{u}_{\mathrm{out}}$. In Figure 11.6, the switching processes of one half-bridge are disjointed from the switching processes of the other half-bridge. At very low output voltages, i.e., if both half-bridges are switched at 50 % duty cycle, the voltage-area deviations drawn in blue and red in Figure 11.6 can overlap. The effects of the positive deviations can superimpose the effects of the negative deviations, as

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[2] LEM LT 100-S/SP30, accuracy of ±0.5 A

[3] Keysight N2781B, accuracy of ±0.8 A using two windings

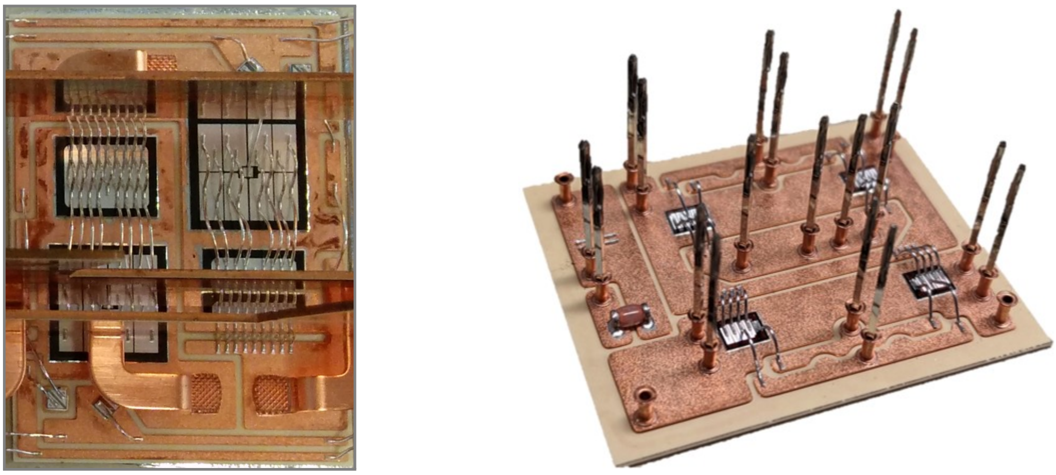
they originate from separate half-bridges. More specifically, the voltage-area deviations at the beginning of the first pulse and at the end of the second pulse originate from the half-bridge with the larger duty cycle. The voltage deviations at the end of the first pulse and the beginning of the second pulse originate from the half-bridge with the smaller duty cycle. This description of this edge case excludes the effects of the propagation delay.

If very small duty cycle differences occur between the half-bridges, the turn-on moments of one switch may occur during a voltage-time error area of the other half-bridge. Thus the current corrections made by the model can be incomplete or even increase the error.

These additional edge cases could be considered in further model refinements, but are omitted in this work. Aside from operating points with very small currents, the remaining current errors shown in Figure 11.13 are within acceptable levels for a TSEP-based temperature estimation.

12 Thermal characterization

The thermal impedance stated in the datasheets of power modules usually only includes the impedance between the junction and the case, i.e., the bottom side of the DCB substrate The thermal coupling between different switches and to the NTC temperature sensor strongly depend on the external cooling setup. Thermal coupling between the switches is expected to be less relevant for liquid cooling systems compared to air cooled systems. For liquid cooled systems, [39] states that noticeable thermal coupling between chips can be expected when the distance d between chips is smaller than $d \approx 0.6 \cdot \sqrt{A}$, with the chip area A. Consequently, relevant thermal coupling is expected when using larger IGBT modules [155] with densely placed chips and anti-parallel diodes, see Figure 12.1a. Thermal coupling between the high-side and low-side switches is expected to be low for the used SiC MOSFET module, as the distance between chips is much larger than the described limit, see Figure 12.1b.



(a) IGBT module, single DCB substrate

(b) SiC MOSFET module under test [99]

Figure 12.1: DCB substrates of the Si IGBT Primepack module and the SiC MOSFET module

The dynamic thermal behavior of a power module can be modeled by the mutual thermal impedance matrix $\boldsymbol{z}_{\text{th}}$ [155–158] for m temperature locations ϑ_k and n power sources p_j

$$\begin{bmatrix} \vartheta_1 \\ \vartheta_2 \\ \vdots \\ \vartheta_m \end{bmatrix} = \begin{bmatrix} z_{\text{th},1,1} & z_{\text{th},1,2} & \cdots & z_{\text{th},1,n} \\ z_{\text{th},2,1} & z_{\text{th},2,2} & \cdots & z_{\text{th},2,n} \\ \vdots & \vdots & \ddots & \vdots \\ z_{\text{th},m,1} & z_{\text{th},m,2} & \cdots & z_{\text{th},m,n} \end{bmatrix} \cdot \begin{bmatrix} p_1 \\ p_2 \\ \vdots \\ p_n \end{bmatrix} + \begin{bmatrix} \vartheta_{\text{ref},1} \\ \vartheta_{\text{ref},2} \\ \vdots \\ \vartheta_{\text{ref},m} \end{bmatrix} . \tag{12.1}$$

If modeled in the frequency domain, each element $z_{\text{th},k,j}$ can be a transfer function with several time constants. The transfer function describes the temperature increase $\Delta\vartheta_k$ in a location, caused by a power p_j. This description does not require the power p_j to actually flow between the reference location of ϑ_{ref} and the location of the modeled temperature ϑ_k. Depending on the cooling system and the orientation of the coolant flow, the thermal coupling between two points does not have to be identical in both directions, i.e., $z_{\text{th},k,j} \neq z_{\text{th},j,k}$ is possible.

The high-side and low-side switches of the module are composed of two separate semiconductor chips each. Both switches are modeled as a single loss source p_{HS} or p_{LS} and a single temperature location $\vartheta_{\text{vj,HS}}$ or $\vartheta_{\text{vj,LS}}$. This model predicts the virtual junction temperatures. The resulting thermal model is

$$\begin{bmatrix} \vartheta_{\text{vj,HS}} \\ \vartheta_{\text{vj,LS}} \\ \vartheta_{\text{NTC}} \end{bmatrix} = \begin{bmatrix} z_{\text{th,HS,HS}} & z_{\text{th,LS,HS}} \\ z_{\text{th,HS,LS}} & z_{\text{th,LS,LS}} \\ z_{\text{th,HS,NTC}} & z_{\text{th,LS,NTC}} \end{bmatrix} \cdot \begin{bmatrix} p_{\text{HS}} \\ p_{\text{LS}} \end{bmatrix} + \begin{bmatrix} \vartheta_{\text{a}} \\ \vartheta_{\text{a}} \end{bmatrix}. \tag{12.2}$$

The indices of the thermal impedance can be interpreted as $z_{\text{th,<power source>,<temperature location>}}$, which in particular means that $z_{\text{th,HS,HS}}$ and $z_{\text{th,LS,LS}}$ are the self-heating thermal impedances. The NTC sensor temperature is kept as an independent temperature, predicted by the model. This enables its use in temperature observer models in conjunction with the temperature measurement provided by the NTC sensor[1]. No additional measurements are needed to determine the thermal coupling to the NTC sensor, as the NTC sensor is already evaluated by the TSEP measurement system. The temperature of the cooling liquid ϑ_{a} is controlled in the test setup. It is constant and chosen as reference.

> **Remark:** An alternative to using the NTC sensor temperature as an independent temperature is the its use as temperature reference. The corresponding thermal model would be
>
> $$\begin{bmatrix} \vartheta_{\text{vj,HS}} \\ \vartheta_{\text{vj,LS}} \end{bmatrix} = \begin{bmatrix} z^{(\text{ntc})}_{\text{th,HS,HS}} & z^{(\text{ntc})}_{\text{th,LS,HS}} \\ z^{(\text{ntc})}_{\text{th,HS,LS}} & z^{(\text{ntc})}_{\text{th,LS,LS}} \end{bmatrix} \cdot \begin{bmatrix} p_{\text{HS}} \\ p_{\text{LS}} \end{bmatrix} + \begin{bmatrix} \vartheta_{\text{NTC}} \\ \vartheta_{\text{NTC}} \end{bmatrix}, \tag{12.3}$$
>
> which has only two independent temperatures and four transfer functions.

12.1 Thermal impedance measurement

The individual thermal impedance components z_{th} are measured as described in [156, 159] by heating one of the switches with a constant current and waiting for the thermal steady state. Then the current is quickly turned off, causing the system to cool down. The cool-down curve corresponds to the step response of the thermal impedance to a negative power step. A simple virtual junction temperature measurement using the body diode's forward voltage at low currents is done during cool down. Applying a positive power step using a load current or switching losses would require constant adjustments, as the losses are temperature dependent due to the changing forward voltage of the body diode [159]. Only

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[1] It also allows plausibility checks by comparing the predicted NTC sensor temperature with its measured value to validate the temperature model.

a single column in $\boldsymbol{z}_{\text{th}}$ will affect the measured temperatures, as all but one power source p_j are zero. The procedure is then repeated with the other switch being heated.

Preparation Prior to the z_{th} measurements, the forward voltage of both body diodes is measured with a current of $I_{\text{meas}} = 100\,\text{mA}$ at temperatures relevant to the operation of the power module. The self heating is neglected. Figure 12.2 shows the measured voltages and a linear fit. Both voltages show high linearity and have the same sensitivity towards the temperature, which is expected.

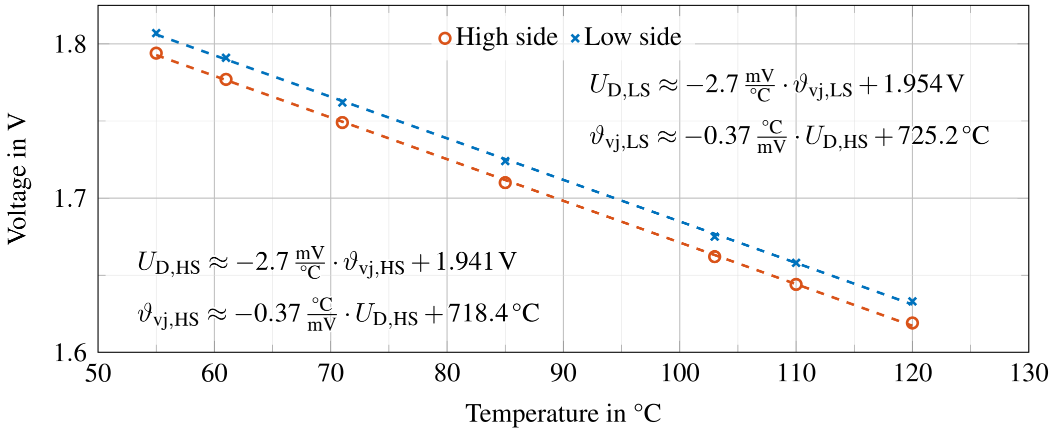

Figure 12.2: Measured forward voltage of the body diodes at $I_{\text{meas}} = 100\,\text{mA}$ depending on the temperature; self heating neglected; linear fit results (dashed) added

Measurement The module is mounted on the liquid cooler, see Figure 12.3. The liquid cooling system is set to the same temperature and flow rate as will be used during all PWM measurements. Variations in cooling temperature or flow rates are not considered. The gate-source connections of the MOSFETs are shorted. One of the switches is heated with a high current I_{heat} through its body diode generating the losses P_{heat}. The use of the body diode instead of the MOSFET channel is acceptable according to AQG 324 [5]. A schematic of

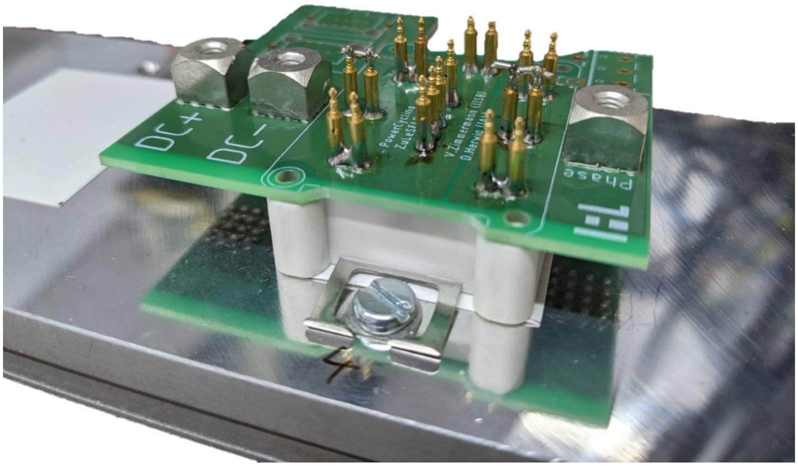

Figure 12.3: Module mounted on the liquid cooler; adapter board for thermal impedance measurement mounted; gate-source path shorted

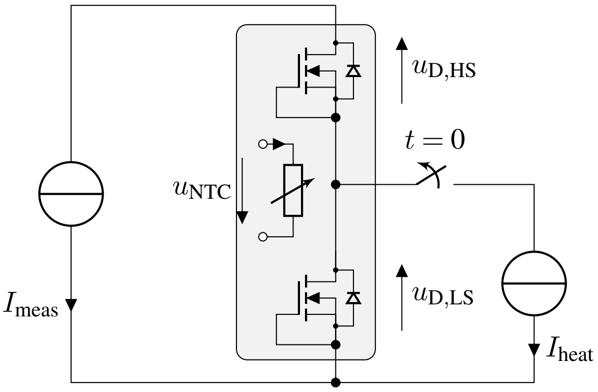

Figure 12.4: Basic schematic of the experimental setup when heating the low-side switch; the opening of the switch is used to define $t = 0$; the temperature of the module's NTC sensor is also recorded

the experiment is depicted in Figure 12.4. After two minutes of heating, the heating current is turned off and the body diode voltages $u_{\mathrm{D,LS}}$ and $u_{\mathrm{D,HS}}$ as well as the voltage of the NTC sensor circuit are recorded. The experiment is repeated for the other switch. The parameters of the experiment are summarized in Table 12.1 for a single thermal interface material (TIM).

Table 12.1: Parameters of the cool-down response measurement

		Single TIM	Double TIM
Heating current	I_{heat}	16 A	
Measurement current	I_{meas}	100 mA	
Self-heating[2]		$\approx 1.8\,\mathrm{V} \cdot 100\,\mathrm{mA} \cdot 0.8\,\frac{\mathrm{K}}{\mathrm{W}} = 0.144\,\mathrm{K}$	
Injected losses (HS)	P_{heat}	48.34 W	48.35 W
Injected losses (LS)	P_{heat}	48.37 W	48.37 W
Fluid temperature	ϑ_{a}	60 °C	
Recorded cool-down time		198 s	
Sample frequency		$250 \cdot 10^3\ 1/\mathrm{s}$	

---

[2] The thermal resistance of $0.8\,\frac{\mathrm{K}}{\mathrm{W}}$ assumes a TIM between the case and heat sink according to the datasheet [147].

12.2 Fitting self heating and cross couplings

The resulting cool-down response $z_{\text{th}}^{(\text{cd})}$ of the system is fitted with a Foster model, as it is well suited for fitting measured data [160]

$$z_{\text{th}} = \sum_{i=1}^{n} R_{\text{th},i} \cdot \left(1 - \mathrm{e}^{-\frac{t}{\tau_i}}\right), \tag{12.4}$$

$$z_{\text{th}}^{(\text{cd})} = \sum_{i=1}^{n} R_{\text{th},i} \cdot \mathrm{e}^{-\frac{t}{\tau_i}}, \tag{12.5}$$

$$\vartheta_{\text{vj}} = z_{\text{th}}^{(\text{cd})} P_{\text{heat}} + \vartheta_{\text{a}}. \tag{12.6}$$

Usually, $n = 4$ four elements are used to model the self heating z_{th} from the junction of the heated switch to the case or heat sink. Only one or two elements are suggested to model the cross coupling between the switches and to the NTC sensor with regard to the real-time requirements of thermal models in an inverter [159]. Here, the thermal model is calculated offline as laboratory reference. Therefore, a higher number of Foster elements is not critical. The entire liquid cooling system is included in the fit and is likely to have much smaller time constants than the junction-to-case thermal impedance. Additional Foster elements may be appropriate to approximate these different time constant ranges [161].

Figure 12.5 shows the measured cooling curves of the heated switch (high side), the unheated switch (low side) and the NTC sensor. For now, only the blue curves are relevant. The red curves will be discussed further in the section. The measured data is fitted with a varying number of Foster elements. Below each cool-down curve, the deviation between the measured data and the fit $\Delta\vartheta_{\text{vj}}$ is shown. Approximately 5 ms after turning off the heating current, the current in the body diode has settled to the level of the measurement. Therefore, the temperature between 0 ms to 5 ms is unknown. Each measurement showed a glitch in all measured voltages between 50 ms to 100 ms. This time span was excluded from the fit.

The dotted blue lines show the fit results for Foster models with four to six elements. The fits for the heated switch match the measurement very closely. A reduction in the deviation $\Delta\vartheta_{\text{vj}}$ can be observed after introducing a fifth Foster element, while the introduction of a sixth element leads to almost no change. In general, it can be seen that the fits match the cool-down behavior of the heated switch very closely. The applied heating power is comparable to the losses in continuous PWM operation at nominal current.

The dotted blue fit results for the cross coupling to the unheated low-side switch and the NTC sensor show noticeable deviation at the beginning and the end. Especially the deviation between the model prediction at the end of the measurement and the fluid temperature of $\vartheta_{\text{a}} = 60\,^{\circ}\text{C}$ leads to deviations in the estimated thermal resistance R_{th} of the cross couplings. A large deviation can also be observed in the range of 0.2 s to 1 s, which is a relevant range when loading the module with a low-frequency load current. In the further chapters, the continuous PWM operation will be done at a fundamental frequency of 1 Hz, so this effect will be relevant.

Fit model adjustments The noticeable deviations of the Foster model in the cross couplings is inherent to the Foster model. The measured temperature shows an approximate delay of 0.3 s before a change in temperature can be noted, but the derivative of the time

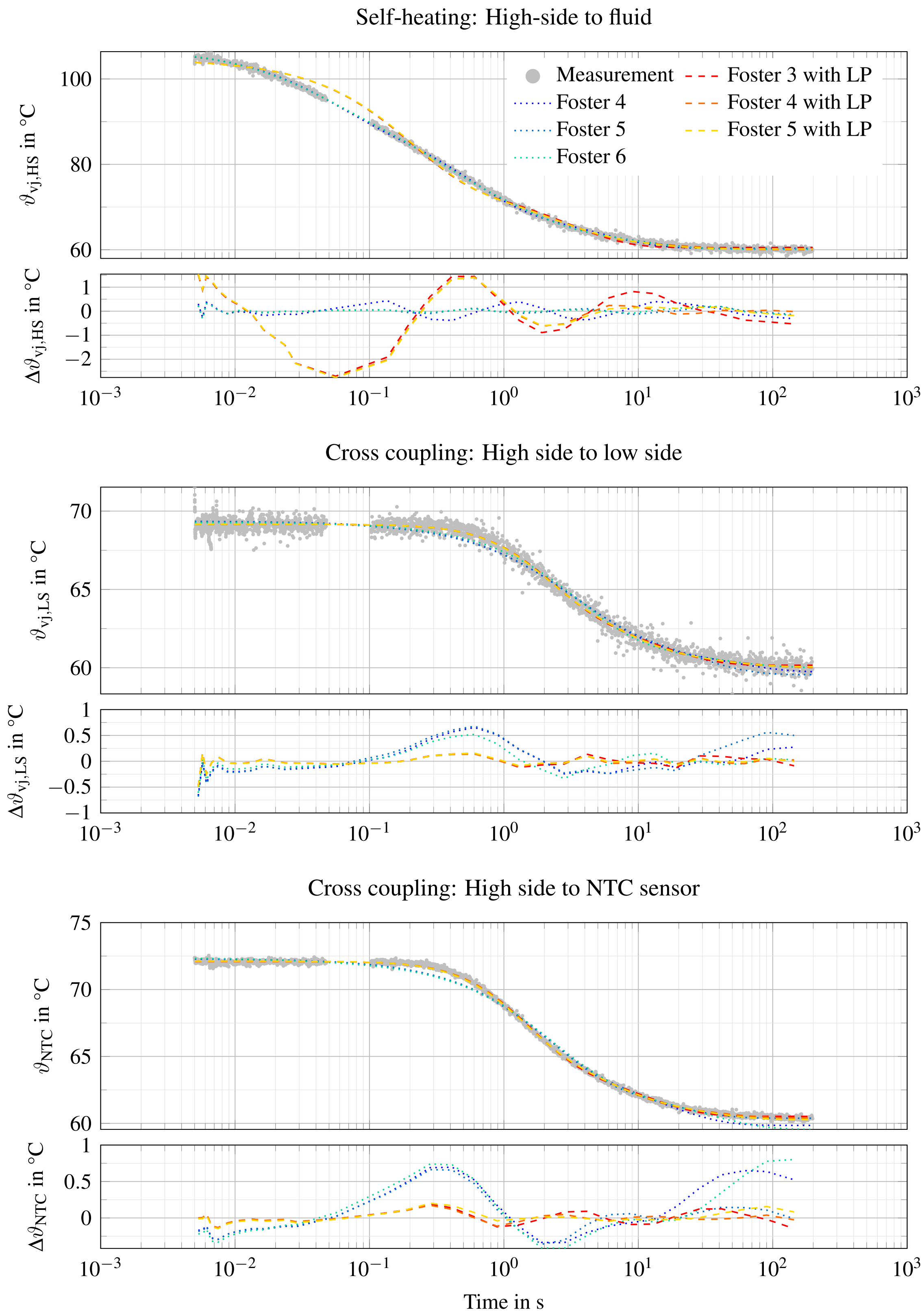

Figure 12.5: Cool-down behavior of a heated switch (HS) and the cross coupled switch (LS) and the NTC [99]; fit results for regular Foster models (blue) and adjusted Foster models with a prepended low-pass filter (LP) (red); a moving average filter was applied to the deviation $\Delta\vartheta_{\mathrm{vj}}$ for clarity; only 32 thousand measurement samples of 50 000 000 plotted

response of the Foster model cannot be zero.

$$z_{\text{th}}^{(\text{cd})} = \sum_{i=1}^{n} R_{\text{th},i} \cdot \text{e}^{-\frac{t}{\tau_i}}, \tag{12.7}$$

$$\left.\frac{\text{d}z_{\text{th}}^{(\text{cd})}}{\text{d}t}\right|_{t=0} = -\sum_{i=1}^{n} \frac{R_{\text{th},i}}{\tau_i} < 0. \tag{12.8}$$

A Cauer model would be better suited to reflect this behavior, but is very difficult to fit from a time series measurement. As an alternative to using a Cauer model, a low-pass filter is introduced in series with the model, see Figure 12.6, enabling the model to start with a derivative of zero. If only a single Foster element is used in conjunction with the low-pass filter, the adapted model is equal to a Cauer model with two elements.

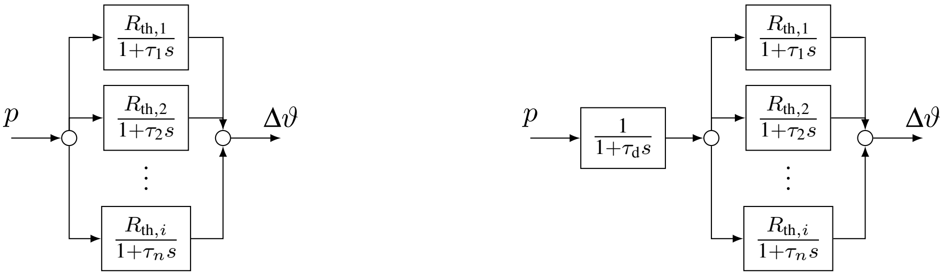

Figure 12.6: Regular Foster model $Z_{\text{th}}(s)$ (left) and adapted Foster model $Z_{\text{th,d}}(s)$ (right); a delay was prepended to better fit cross couplings [99]

The resulting time response during cool down can still be described with simple terms and fitted as

$$z_{\text{th,d}}^{(\text{cd})} = \sum_{i=1}^{n} \frac{R_{\text{th},i}}{\tau_\text{d} - \tau_i} \left(\tau_\text{d}\text{e}^{-\frac{t}{\tau_\text{d}}} - \tau_i\text{e}^{-\frac{t}{\tau_i}}\right), \tag{12.9}$$

$$\left.\frac{\text{d}z_{\text{th,d}}^{(\text{cd})}}{\text{d}t}\right|_{t=0} = \sum_{i=1}^{n} \frac{R_{\text{th},i}}{\tau_\text{d} - \tau_i} \left(-\frac{\tau_\text{d}}{\tau_\text{d}} + \frac{\tau_i}{\tau_i}\right) = 0. \tag{12.10}$$

$$\tag{12.11}$$

For simplicity, the prepended low-pass filter has unity-gain. The fit results of the adjusted Foster models are also shown in Figure 12.5. The introduced low-pass filter significantly improves the fit quality for the cross coupling between the switches and to the NTC sensor. For the fitting of the self heating, the adjusted model generates larger deviations. The introduced low-pass filter can also be seen as time delay before a temperature change of the heated chip translates to a different location on the DCB substrate, which is not the case for the heated switch.

Based on the deviations $\Delta\vartheta_{\text{vj}}$ shown in Figure 12.5, a regular Foster model with five elements is chosen to model the thermal impedance from a heated switch to the fluid and a Foster model with three elements and an additional low-pass filter is chosen to model the cross coupling between the switches and to the NTC sensor. The introduction of a low-pass filter increases the number of states by one. Still, this option should be considered, as it can reduce the number of subsequent Foster elements.

12.3 Experimental setups and results

The thermal characterization is done twice. A single layer of TIM between the module and the cooler is used as the reference setup. The thermal impedance is measured and fitted. Afterwards, a second layer of TIM is added to increase the thermal resistance between the junction and ambient $R_{\mathrm{th,ja}}$ of both switches, see Figure 12.3 and Figure 12.7. The thermal resistance R_{th} between a power source and a temperature location is defined as the steady-state thermal impedance

$$R_{\mathrm{th}} := \sum_{i=1}^{n} R_{\mathrm{th},i} = \lim_{t\to\infty} z_{\mathrm{th}} \mathrel{\widehat{=}} \lim_{t\to 0^+} z_{\mathrm{th}}^{(\mathrm{cd})}. \tag{12.12}$$

These two setups will be used in Section 13 to assess whether the TSEP measurement system can be used to detect the increase in thermal resistance.

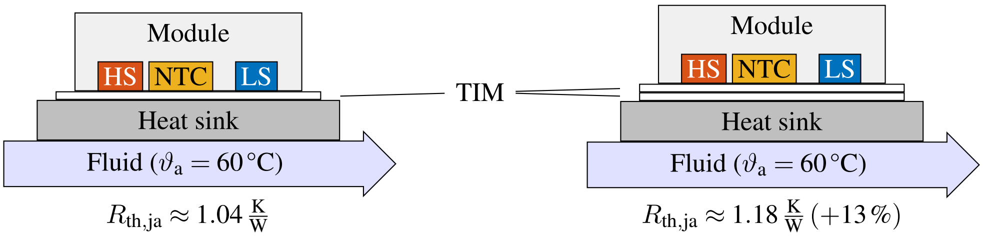

Figure 12.7: Reference setup with a single layer of TIM (left) and a double layer of TIM (right), increasing the thermal resistance [99]

Fit results Figure 12.8 shows the measured cooldown curves and the temperature predictions of the corresponding fits. Each switch is heated with both a single and a double layer of TIM. The thermal resistances can be preliminary assessed from the graph. It corresponds to the temperature increase at $t = 0$

$$R_{\mathrm{th}} \mathrel{\widehat{=}} \frac{\Delta\vartheta}{P_{\mathrm{heat}}} = \frac{1}{P_{\mathrm{heat}}} \lim_{t\to 0^+} (\vartheta - \vartheta_{\mathrm{a}}). \tag{12.13}$$

Adding the second TIM layer increases the measured temperature for of both switches and the NTC sensor, while the injected losses P_{heat} are matching. Due to the location of the NTC, see Figure 12.1, the measured temperature of the NTC sensor is higher if the high-side switch is heated.

The datasheet of the power module provides a four-element Foster model describing the thermal impedance between the junction and the case [147]. One of its time constants is too small to be measured with this setup, due to the settling time of the measurement current of 5 ms. To circumvent this issue, the first Foster element of both fitted self-heating thermal impedances $z_{\mathrm{th,LS,LS}}$ and $z_{\mathrm{th,HS,HS}}$ is predefined as $R_{\mathrm{th},1} = 47\,\frac{\mathrm{mK}}{\mathrm{W}}$ and $\tau_1 = 497\,\mu\mathrm{s}$ to match the datasheet values. This element accounts for an approximate temperature increase of 2 K at nominal current. By definition, the impact of this time constant has decayed before the measurement data for the fitting procedure is available.

A summary of the estimated parameters is shown in Table 12.2. More details can be found in Appendix J. The thermal resistances of the high-side and low-side switch to ambient show an increase of 12.4 % to 14.7 % when the second TIM layer is added. The module's end of

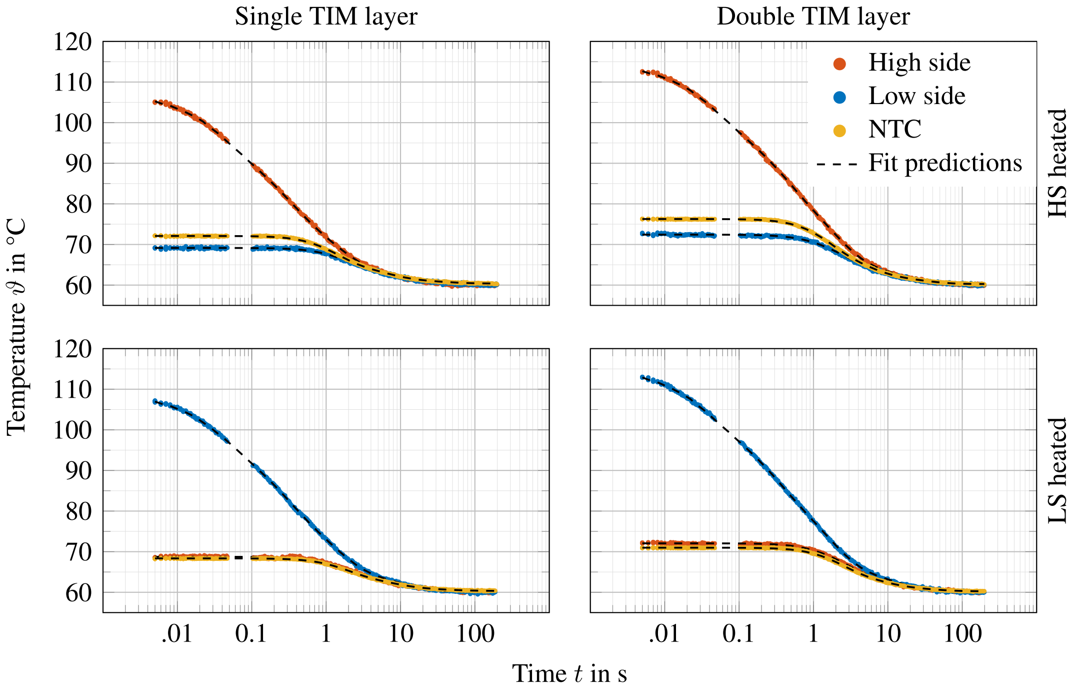

Figure 12.8: Measured temperatures during cool down [99]; either the high-side (top) or low-side (bottom) switch was heated; the right side shows measurements with an additional TIM layer between the module and the cooler, increasing z_{th}; only 100 points plotted per decade out of 50 000 000 samples

life (EOL) is defined as an increase of 20 % in AQG 324 [5]. Thus, the additional TIM layer can be used to emulate significant aging of the chip solder without breaching the end of life of the module. The observed changes in the cross-coupling thermal impedances are not directly transferable to real chip solder degradation, as the additional emulated thermal impedance occurs between the case and the cooler, while an actual solder degradation increases the thermal impedance between the chip and the DCB substrate, see [4] for further details.

> **Remark:** The cross couplings $R_{\mathrm{th,HS,LS}}$ and $R_{\mathrm{th,LS,HS}}$ are approximately one fifth of the switches' R_{th} to the fluid. This would indicate a significant cross coupling between the chips, even though no significant cross coupling is expected based on the wide distance between the chips. This discrepancy between the parameters and the expectations is due to the choice of the fluid temperature as reference. Thus, the cross-coupling coefficients also include the temperature increase of the baseplate. If the NTC sensor temperature had been chosen as reference, the cross-coupling coefficients would be smaller.

Figure 12.9 to Figure 12.11 show the thermal impedances in the frequency domain. Figure 12.12 to Figure 12.14 shows the same thermal impedances in the time domain. It can be seen that the thermal impedance for low frequencies is generally larger than the datasheet values. This is expected, as the measured thermal path also includes the heat sink and the heat transfer into the fluid, while the thermal impedance in the datasheet stops at the heat sink and has better thermal interface material. For higher frequencies, the thermal impedance is lower, which can be attributed to the larger thermal capacitance.

The changes in the cross coupling do not reflect the effects of chip solder degradation properly, as the TIM layer is introduced below the DCB substrate and not between the chip and the DCB substrate Therefore, the observed changes may not be transferable to real solder degradation. The coupling between the chips and the NTC sensor show a noticeable change in the phase at 0.2 Hz. A detailed investigation using an active gate driver to modulate the semiconductor losses and track the phase shift of the thermal transfer function from the junction to the NTC sensor is presented in [4].

Table 12.2: Summary of the basic parameters of the determined thermal impedances; time constants and individual Foster elements listed in Appendix J

	$R_{\text{th,HS,HS}}$ in $\frac{\text{K}}{\text{W}}$	$R_{\text{th,LS,LS}}$ in $\frac{\text{K}}{\text{W}}$	$R_{\text{th,HS,LS}}$ in $\frac{\text{K}}{\text{W}}$	$R_{\text{th,LS,HS}}$ in $\frac{\text{K}}{\text{W}}$	$R_{\text{th,HS,NTC}}$ in $\frac{\text{K}}{\text{W}}$	$R_{\text{th,LS,NTC}}$ in $\frac{\text{K}}{\text{W}}$
Single TIM	1.02	1.05	0.19	0.18	0.24	0.17
Double TIM	1.17	1.18	0.26	0.25	0.33	0.22
	(+14.7 %)	(+12.4 %)				

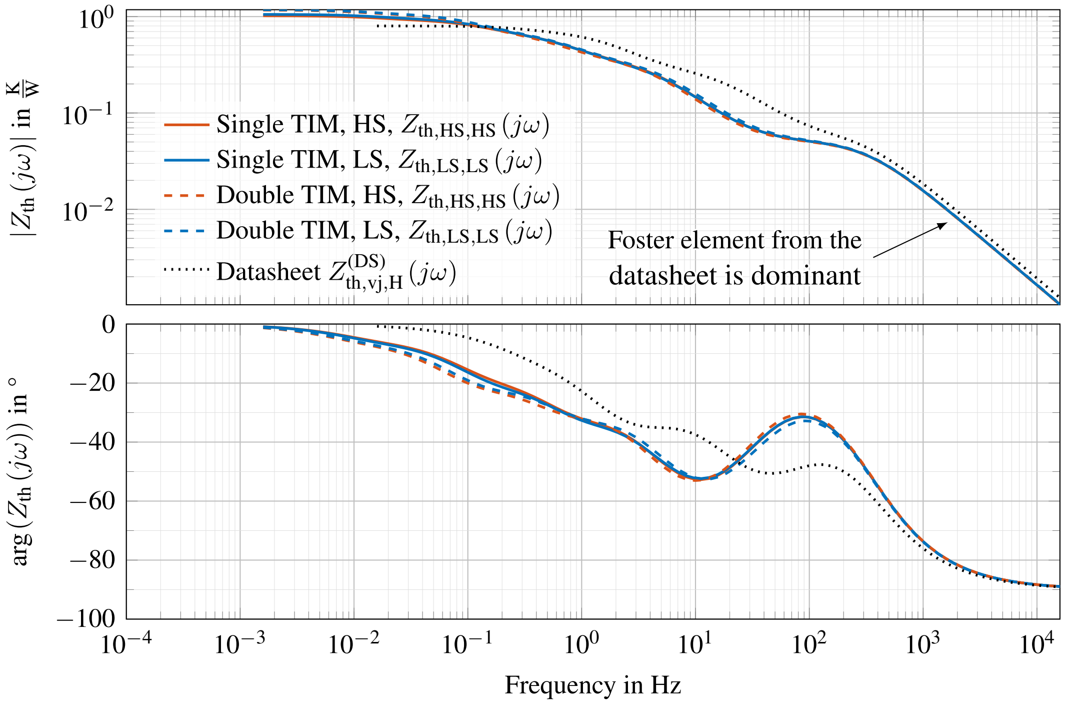

Figure 12.9: Estimated thermal impedance $Z_{\text{th}}(j\omega)$ from the heated switches to the fluid (ambient temperature) in the frequency domain

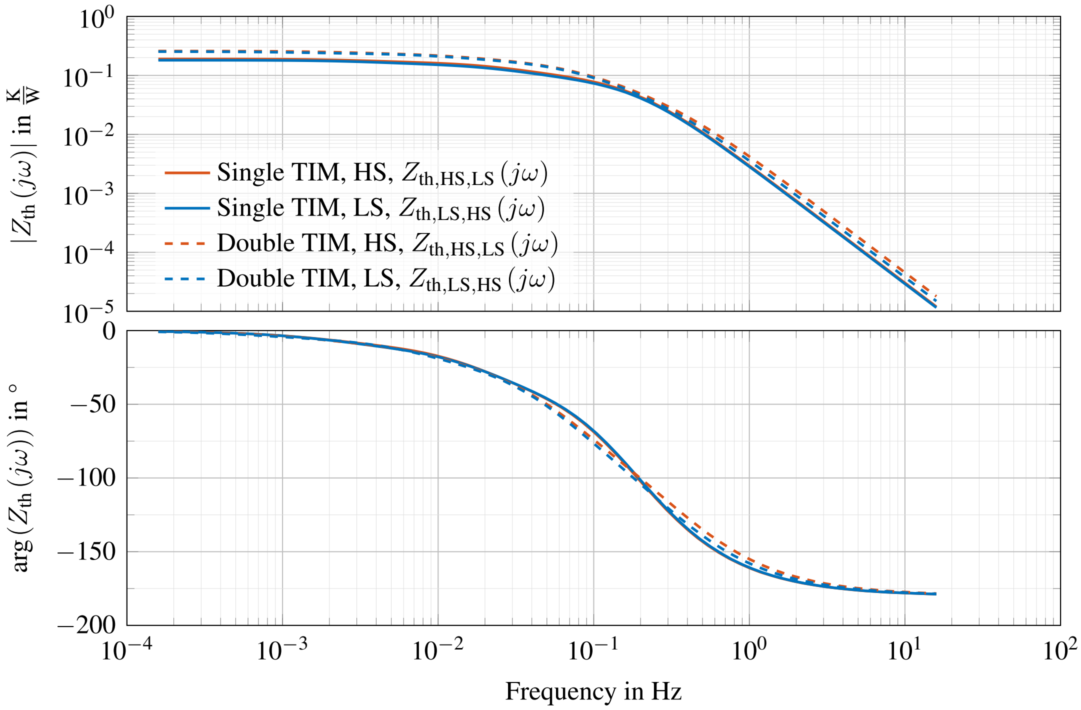

Figure 12.10: Estimated thermal impedance $Z_{\mathrm{th}}(j\omega)$ from the heated switches to the partner switch (cross coupling) in the frequency domain

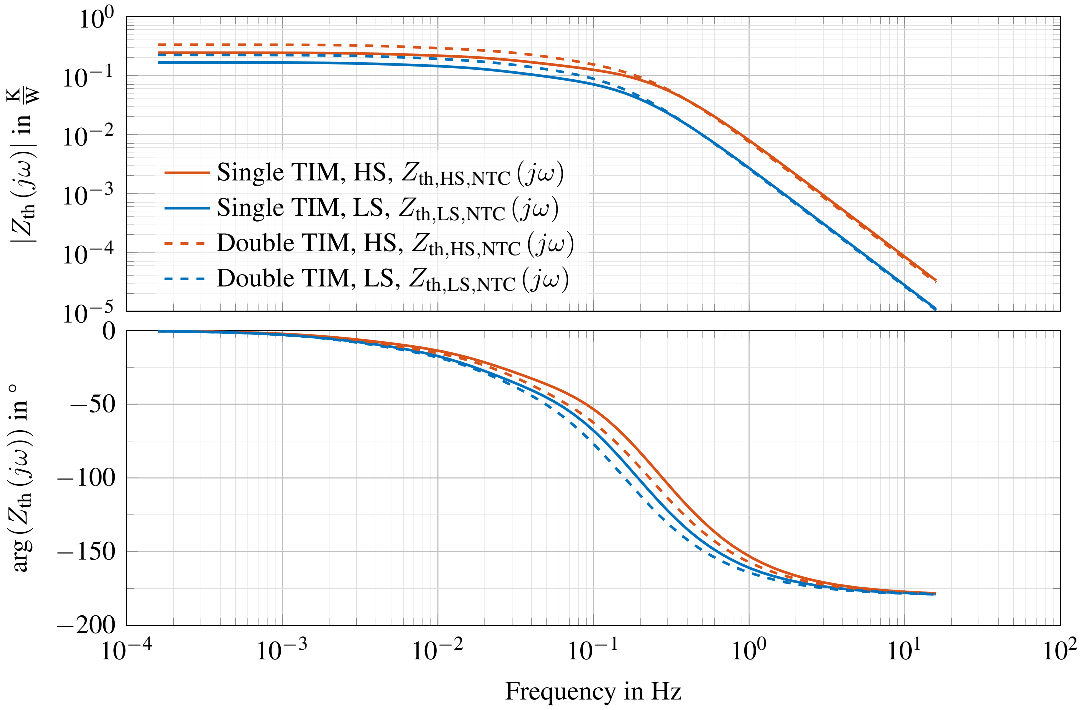

Figure 12.11: Estimated thermal impedance $Z_{\mathrm{th}}(j\omega)$ from the heated switches to the NTC (cross coupling) in the frequency domain

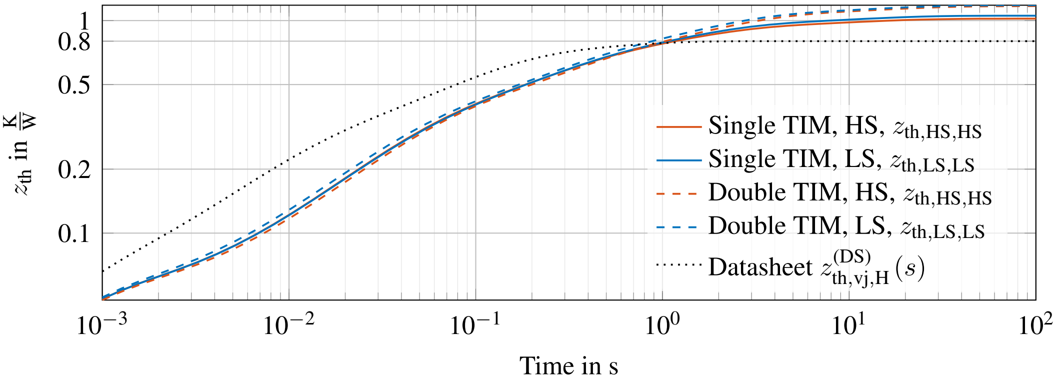

Figure 12.12: Estimated thermal impedance z_{th} from the heated switches to the to the fluid (ambient temperature) in the time domain

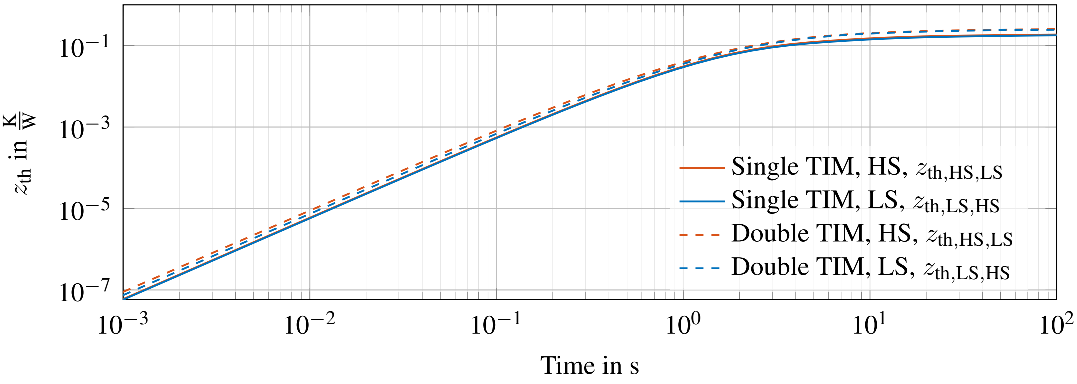

Figure 12.13: Estimated thermal impedance z_{th} from the heated switches to the partner switch (cross coupling) in the time domain

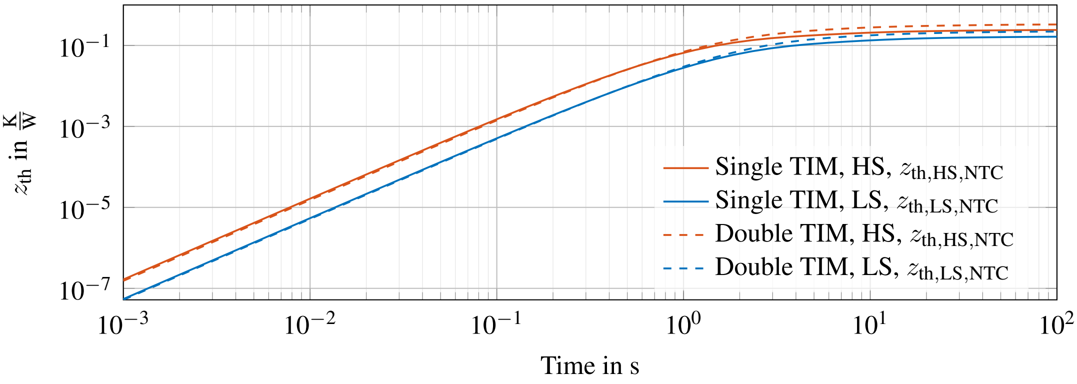

Figure 12.14: Estimated thermal impedance z_{th} from the heated switches to the NTC (cross coupling) in the time domain

12.4 Loss model

In the previous section, the determination of the thermal impedance of the module and the test setup was presented. A loss model is required to predict the junction temperature using the measured thermal impedance. The losses consist of switching losses p_{sw} and conduction losses p_{c}. The conduction losses can be determined directly from the measured on-state voltage of the TSEP measurement system.

Switching loss measurements in [162, 163] have shown that the bandwidth of the available Rogowski coils is too small to capture the overcurrent peak accurately. Hence, the switching losses will be estimated from a fit model developed in [162, 163]. This switching-loss model was determined for a matching SiC module and a specially designed calibration setup. In the calibration setup, a high-bandwidth shunt resistor was inserted into the commutation loop for a high-bandwidth measurement of the commutation current. The used dc-link capacitor is equal to the one used for the TSEP measurements, and the PCB layouts are similar. The model includes dependencies on the load current, the dc-link voltage and the junction temperature.

Having a shunt resistor within the commutation loop of the TSEP measurement system was not intended during the design stage and cannot be retrofitted easily. Using the measured switching losses from another module, driver and commutation loop introduces deviations, especially due to changes in the threshold voltage of the module. Therefore, inaccuracies in the assumed switching losses will occur. The impact of these inaccuracies will be assessed at the end of this section.

The switching-loss model, sourced from [162, 163], uses a reference switching-loss energy E_{ref} at a reference operating point, which is scaled with second-order polynomials for each dependency

$$E_{\mathrm{sw}}^{*} = E_{\mathrm{ref}} \cdot f_1\left(R_{\mathrm{g,on,ext}}\right) \cdot f_2\left(U_{\mathrm{dc}}\right) \cdot g\left(I_{\mathrm{L}}, \vartheta\right), \tag{12.14}$$

$$f_i\left(x\right) = a_{i,2}x^2 + a_{i,1}x + a_{i,0}, \tag{12.15}$$

$$g\left(x,y\right) = c_{20}x^2 + c_{11}xy + c_{02}y^2 + c_{10}x + c_{01}y + c_{00}. \tag{12.16}$$

The fit parameters for the turn-on losses $E_{\mathrm{sw,on}}$ and turn-off losses $E_{\mathrm{sw,off}}$ are listed in Appendix K. Reverse recovery losses within the body diode are neglected.

On-state voltage measurement incorporation During operation, the average estimated conduction losses $\overline{P}_{\mathrm{c}}$ are based on the measured on-state voltage $U_{\mathrm{ds,virt}}$, the sampled load current I_{L} and the duty cycle d_2. The required quantities are illustrated in Figure 12.15 for the low-side switch of half-bridge HB2 (DUT). In the given setup, the on-state voltage is measured directly after turn-on $U_{\mathrm{ds,virt,turnon}}$ and directly before turn-off[3] $U_{\mathrm{ds,virt,turnoff}}$. These measurements can be averaged resulting in a more accurate estimate of the average voltage during the conduction phase. The aim of the loss model and temperature model is to serve as reference to evaluate the TSEP-based temperature estimation. There is almost no load in the given laboratory setup, leading to small current ripple even at nominal current. The conduction losses will be estimated using the average current from the inverter sensor

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[3] Technically, this measurement is done as part of the TSEP measurement set of the partner switch, but can be used for the thermal model as well.

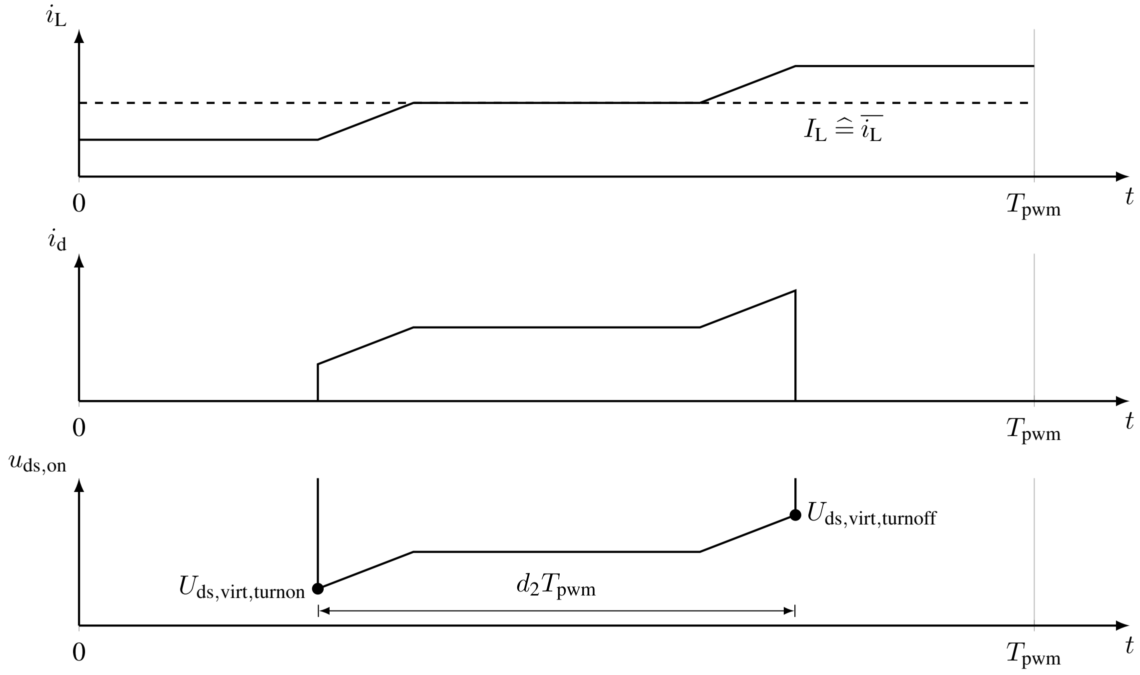

Figure 12.15: Illustration of the quantities used to estimate the conduction losses during PWM operation

$I_\mathrm{L} \widehat{=} \overline{i_\mathrm{L}}$ and the mean of measured on-state voltages

$$\overline{P}_\mathrm{c} = I_\mathrm{L} \frac{U_\mathrm{ds,virt,turnon} + U_\mathrm{ds,virt,turnoff}}{2} d_2. \tag{12.17}$$

As current ripple is neglected here, the conduction losses will be underestimated.

An average model of the switching and conduction losses is used

$$\overline{P}_\mathrm{sw} = \frac{E_\mathrm{sw}}{T_\mathrm{pwm}} = \frac{E_\mathrm{sw,on} + E_\mathrm{sw,off}}{T_\mathrm{pwm}}. \tag{12.18}$$

Temperature waveforms Figure 12.16 shows the estimated self heating of a switch during a PWM period for a simplified case. The conduction losses are approximated by assuming that the SiC MOSFET is an ideal resistor of $R_\mathrm{ds,on} = 23\,\mathrm{m\Omega}$ at nominal current and a fixed duty cycle of $d = 50\,\%$. The thermal model of the single-TIM setup in Chapter 12 is used. The investigations in the further sections will always use a duty cycle $d_2 = 50\,\%$ for the module under test only. It can be seen that the largest expected thermal ripple during a PWM period is less than 0.4 K. Temperature ripple within a PWM period will be neglected.

Figure 12.17 shows the waveforms of the switching energies, losses and temperature increase in the junction during a fundamental period of the output current in quasi-steady state. The depicted waveforms show a simplified example to assess the expected range of the losses and temperatures. Current ripple was not included. The example shows the low-side switch while the load current i_L flows into the half-bridge. Below approximately 33 A, the switching losses become more significant than the conduction losses. The total switching losses are also shown assuming a 10 % deviation of the predicted losses. A virtual junction temperature increase of approximately 30 K is expected. The assumed tolerance in the switching losses could cause a temperature deviation of ±1 K at nominal current.

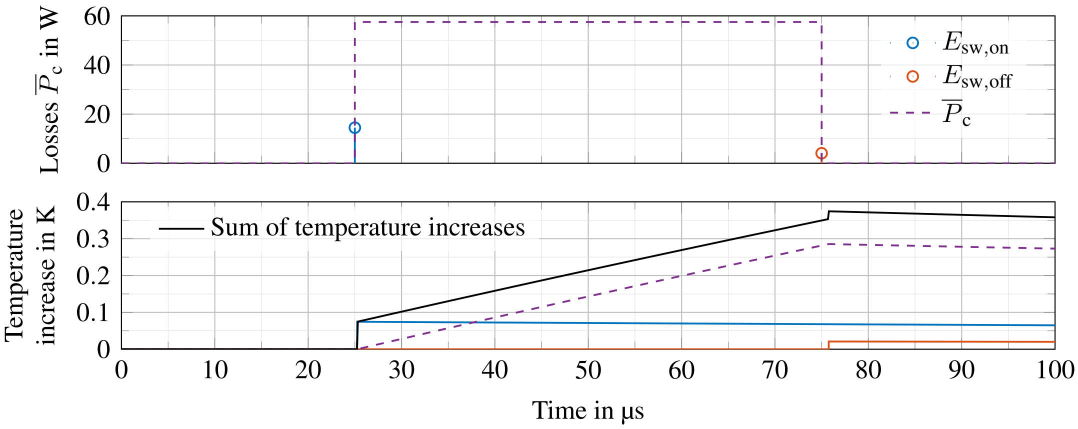

Figure 12.16: Expected switching energies, conduction losses and resulting temperature increase in the junction during a single PWM period at 50 % duty cycle and nominal current; the temperature increases are shown per component and must be summarized to get the overall temperature increase.

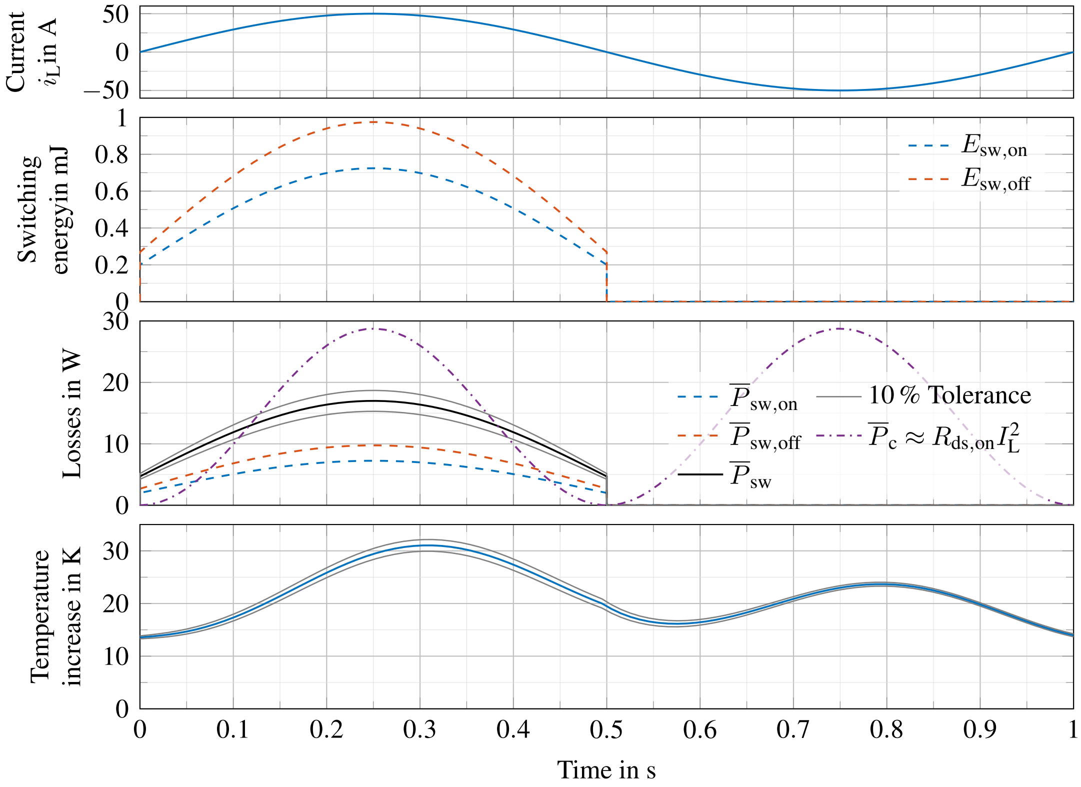

Figure 12.17: Expected switching energies, losses and resulting temperature increase of the low-side switch during a fundamental period at 50 % duty cycle and nominal current; ranges of the switching losses and the resulting virtual junction temperature in gray; a 10 % tolerance in switching losses is assumed

12.5 TSEP evaluation in continuous PWM operation

In the previous sections, PWM-specific aspects of a TSEP-based temperature evaluation have been discussed. In this section, a power module will be operated in PWM with a low-frequency load current. The current has an amplitude equal to the nominal current of the module. The low frequency was chosen to cause a high temperature swing on the junction temperature of the module.

During continuous PWM operation, the four TSEPs t_d, t_rrm, $U_\mathrm{ds,virt,turnon}$ and $U_\mathrm{ds,virt,turnoff}$ are recorded for both switches. The extended current model, see Section 11.2, is used to determine the instantaneous current during turn-on of both switches from the scalar inverter current sensor measurements. Afterwards, the virtual junction temperature for both switches is determined from the TSEPs and the inverter sensor readings using an ANN, as presented in Chapter 6. The estimated temperature is compared to the virtual junction temperature predicted by the thermal model of the power module and the test setup, see Chapter 12.

The measurements are presented in Figure 12.18. The virtual on-state voltage $U_\mathrm{ds,virt}$ exhibits some harmonics in the measurements done right after turn-on of a switch. The measurements right before turn-off (dashed) show a very smooth response to the average of the load current $\bar{i}_\mathrm{L}$ in each PWM period. These measurement results validate the accuracy of the ADC front end.

The measured switching times show little noise. The turn-on delay time of the high side is higher, as the trigger level was designed to be approximately 2.1 V instead of approximately 1.4 V on the low side[4]. The trigger level was increased due to higher EMI on the high-side TDC front end. The increased trigger level increases the measured turn-on delay time t_d by approximately 5 %.

The turn-on delay time is reduced at higher currents. This is probably caused by NTC behavior of the turn-on delay time in conjunction with the increased junction temperature. It must be noted that this is in contrast to the observed, slight PTC behavior of the turn-on delay time during double-pulse experiments, see Section 10.6. This might be a hint that heat soaks up from the hot plate to the TSEP measurement system during double-pulse experiments, while in continuous PWM operation the module's baseplate temperature stays close to the cooler's temperature.

The temperature estimation uses an ANN with a single hidden layer of six neurons and a hyperbolic tangent sigmoid as the activation transfer function, as described in Section 4.2

$$\vartheta := f_\mathrm{ANN}\left(U_\mathrm{ds,virt,turnon},\, U_\mathrm{ds,virt,turnoff},\, t_\mathrm{rrm}-t_\mathrm{d},\, \frac{t_\mathrm{rrm}}{t_\mathrm{d}},\, I_\mathrm{ton},\, U_\mathrm{dc}\right). \tag{12.19}$$

The switching times are preprocessed before usage, i.e., $\frac{t_\mathrm{rrm}}{t_\mathrm{d}}$ and $t_\mathrm{rrm}-t_\mathrm{d}$ are used as inputs. The ANN is trained on the previously acquired SiC MOSFET double-pulse calibration data using the concepts described in Chapter 6. This approach neglects one important effect. During calibration, the high side and low side are at the same temperature. During continuous PWM operation a temperature difference occurs. This temperature difference impacts t_rrm due to the reverse recovery current of the body diode. For now, the deviations caused by this effect are ignored. The resulting temperature error will be analyzed in Chapter 15.

The TSEP-based temperature estimation of the virtual junction temperature ϑ_vj is plotted in the fourth graph in Figure 12.18. It can be compared to the expected junction temperature

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[4] The magnitude of the (negative) induced voltage spike $|u_\mathrm{sk}|$ is approximately 43 V.

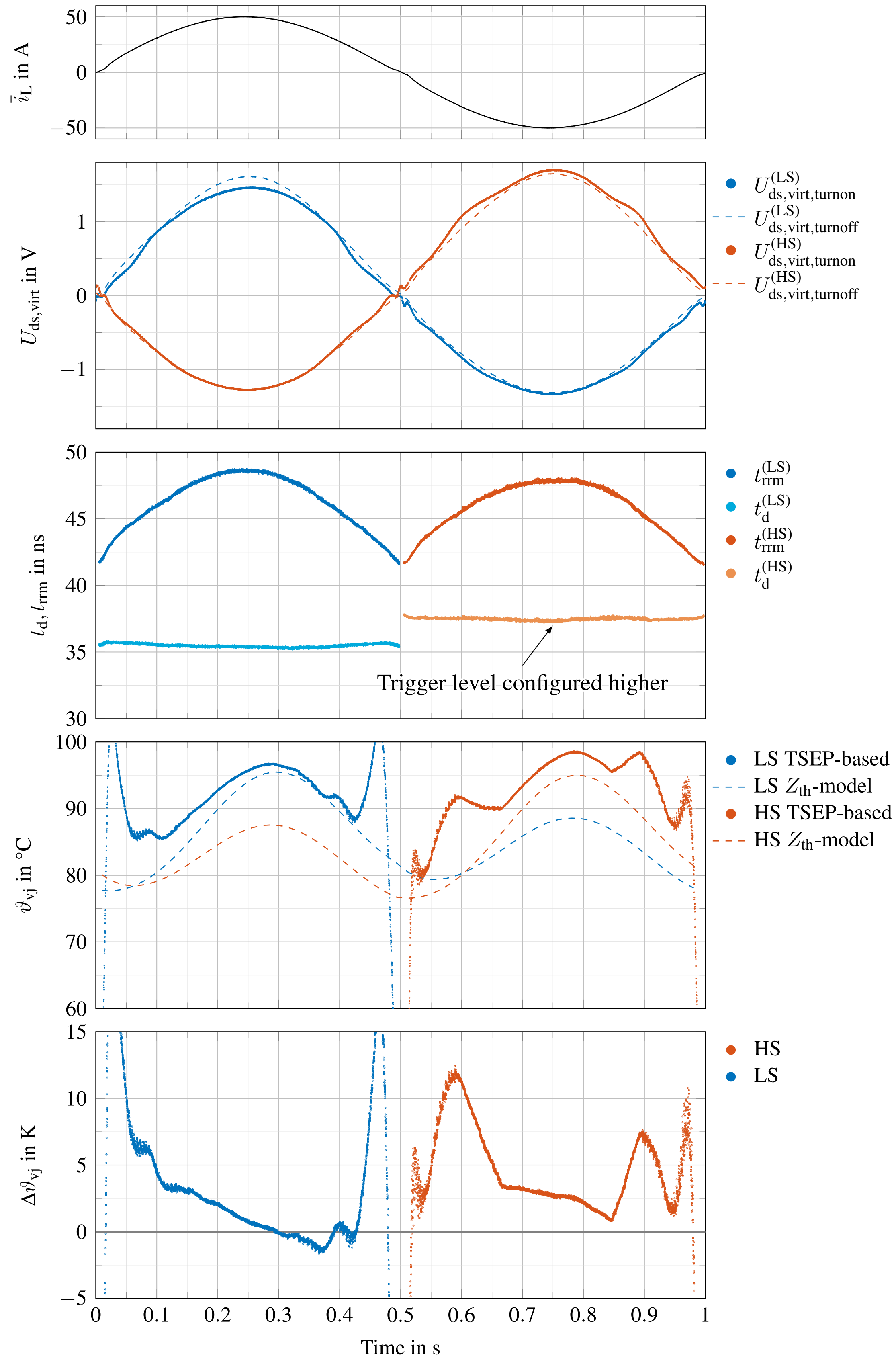

Figure 12.18: Acquired TSEPs during continuous PWM operation and the TSEP-based temperature evaluation

based on the thermal model of the system. The difference $\Delta\vartheta_{\mathrm{vj}} = \vartheta_{\mathrm{vj}}^{(\mathrm{TSEPs})} - \vartheta_{\mathrm{vj}}^{(Z_{\mathrm{th}}\text{-Model})}$ is plotted in the bottom graph. At high currents, the TSEP-based temperature estimation is close to the expected temperature. At low currents the deviation increases significantly.

The deviations at low currents are expected due to the low temperature sensitivity of the TSEPs at low currents, leading to a small signal-to-noise ratio. Considering the amount of possible parasitic effects presented in this work, see Chapter 7, the impact of current estimation deviations, see Chapter 11, the measurement challenges for fast-switching SiC devices and the low sensitivity of TSEPs in general, the TSEP-based virtual junction temperature estimation is satisfactorily close to the expected value.

13 Emulated solder degradation

In this chapter, it will be assessed whether an increase in thermal resistance can be detected using the TSEP measurement system. The thermal impedance between the semiconductor and the cooling system is increased by adding an additional TIM layer between the module and the liquid cooler. Details of the setup and the thermal characterization were shown in Chapter 12.

A degradation of the chip solder is emulated in this test. Compared to a real chip solder degradation, the emulated increase in the thermal impedance is located below the case of the module, while an actual chip solder degradation increases the thermal resistance between the chips and the DCB substrate. Consequently, the thermal coupling between the chips and the modul NTC is not reflected perfectly.

As before, the module was loaded with a 1 Hz load current until it reached quasi-steady state while the TSEPs were measured. Figure 13.1 shows the resulting TSEP-based temperature estimation with a single and a double layer of TIM. The expected junction temperature is shown in dashed as reference. The TSEPs are evaluated with the same ANN as used in

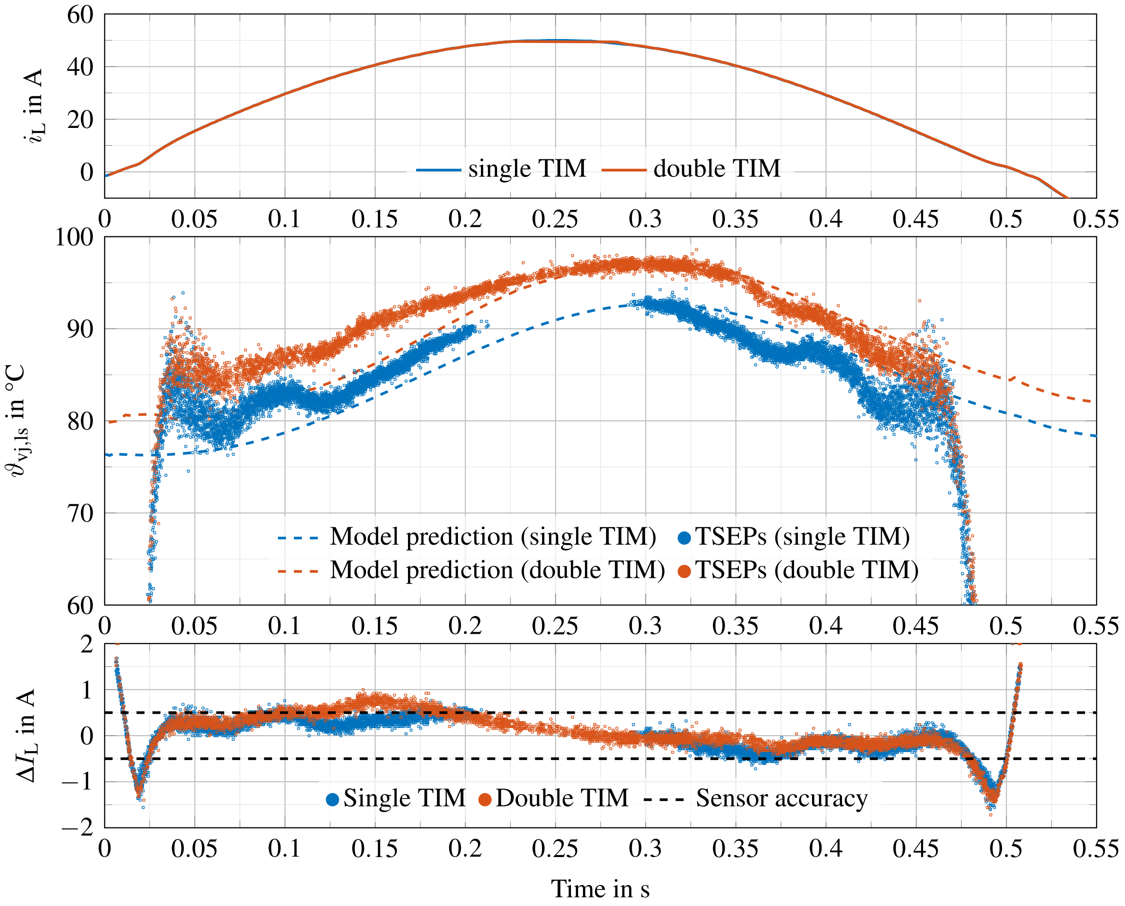

Figure 13.1: TSEP-based temperature estimation with and without and additional TIM layer

(12.19), Section 12.5 The TSEP-based temperature estimation is close to the temperature predicted by the thermal impedance model, especially at high currents. At low currents the deviation increases, as the temperature sensitivity approaches zero.

The most important aspect of this result is the temperature offset between the single TIM and the double TIM case. The TSEP measurement reflects the expected temperature increase well. Both cases can be clearly separated. Thus, the TSEP measurement system is capable of detecting an emulated degradation of the thermal resistance between the chips and the cooler.

Source of the deviation In the previous sections, numerous parasitic impacts on the measurements have been presented and discussed. However, one of the most important source of deviations is the accuracy of the instantaneous current estimation at turn-on. The bottom graph of Figure 13.1 shows a conceived current measurement deviation ΔI_{L} that was needed to cause the temperature deviation between the TSEP measurement and the model prediction in the middle graph. Instead of using sensitivities, the deviation ΔI_{L} was determined by simply perturbating the current input to the TSEP evaluation ANN until the the results of the ANN $\vartheta_{\mathrm{vj,ls}}^{(\mathrm{ANN})}$ matched the temperature predicted by the model $\vartheta_{\mathrm{vj,ls}}^{(Z_{\mathrm{th}}\text{-model})}$

$$\vartheta_{\mathrm{vj,ls}}^{(\mathrm{ANN})}\left(U_{\mathrm{dc}},\underbrace{I_{\mathrm{L}}+\Delta I_{\mathrm{L}}}_{\text{perturbated}},U_{\mathrm{ds,virt,turnon}},U_{\mathrm{ds,virt,turnoff}},\frac{t_{\mathrm{rrm}}}{t_{\mathrm{d}}},t_{\mathrm{rrm}}-t_{\mathrm{d}}\right)\overset{!}{=}\vartheta_{\mathrm{vj,ls}}^{(Z_{\mathrm{th}}\text{-model})}. \qquad (13.1)$$

All other inputs were kept constant.

A correlation between the corresponding current error ΔI_{L} and the slope of the load current is visible. While the load current is increasing, the error is positive and at a steady level of approximately 0.5 A. While the load current is decreasing, the error is negative and at a steady level of approximately -0.4 A. This indicates that the extended current model or the loss model could be improved further, see Section 11.2 and Section 12.4.

Almost the entire deviation could be accounted to a current estimation deviation of ± 0.5 A, which is within the accuracy level of the current sensor. Whether the temperature deviation is actually caused by the current sensor deviation, a deviation in the estimated instantaneous turn-on current or a parasitic impact cannot be determined conclusively. Nevertheless, these results show that these kind of deviations in the temperature estimation are to be expected in TSEP-based systems for SiC devices.

14 Accelerated aging tests

In Chapter Chapter 13, it has been validated that the TSEP measurement system can detect emulated degradation of the chip solder. In addition to these tests, accelerated aging tests are conducted. These tests should generate more realistic degradation of the modules. The specific type of the test performed, i.e., power-cycling tests, will be presented in Section 14.1.

Several modules are aged under test conditions likely to cause degradation of the chip-near interconnects. During the course of the accelerated aging tests, the modules are periodically dismounted from the power-cycling test bench and analyzed with the TSEP measurement system. Each time, the TSEPs are measured in double-pulse experiments and in continuous PWM operation. The aim is to validate whether or not the TSEP measurement system can detect realistic degradation effects of the chip-near interconnects before the module reaches its end of life (EOL).

14.1 Test selection

In accelerated aging tests, a physical stress is applied which is typically much higher than the stresses occurring during the regular life cycle of the module, in order to accelerate the aging process. This physical stress usually induces multiple types of degradation within the module simultaneously. Therefore, the type and parameters of the stress must be selected carefully to primarily generate the degradation mechanism to be investigated. Table 14.1 shows the relationship between several testing methods and the predominantly stressed components. Details of the test methods listed are described in [7]. This work focuses on thermomechanical degradation of the chip-near interconnects, see Figure 2.1. A power-cycling test (PC_{sec}) is chosen as accelerated aging test, as it predominantly stresses the bond wire connections and the chip solder.

In a PC_{sec}, the semiconductors are heated by a high load current for several seconds, followed by a cool-down phase. The semiconductors themselves are not switched. A constant gate voltage is applied to turn on the devices. The duration of one load cycle may range from 1 s to 15 s [6]. The heating current is turned off before the temperature increase soaks through the rest of the module. This generates a high temperature swing of the semiconductor and the chip-near interconnects, while the system solder experiences a much lower temperature swing. In comparison, a smaller current is applied over a longer time span of 1 min to 15 min in thermal cycling tests PC_{min} [6], thus, allowing the system solder temperature to follow the thermal cycle.

Apart from the standards *ECPE guideline AQG324 - Qualification of power modules for use in power electronics converter units in motor vehicles* [5] and *IEC 60749-34 - Semiconductor devices - Mechanical and climatic test methods - Part 34: Power cycling* [6] applied here, it is also possible to substitute and use a different method to generate losses within the semiconductor. Instead of using a high heating current, the semiconductors can be turned on and off with high switching losses. The smaller heating current reduces the stress on the bond wire connections while the switching losses keep the temperature swing of the semi-

Table 14.1: Applied test method and corresponding predominantly stressed components [7]; selected test method in bold

	Stressed component										
Test	Spatial defect in the semiconductor	Surface defect of the semiconductor	**Bond connection**	Housing	Electrical connection	Electrical stability	Gate oxide	Corrosion	Passivation	Insulation	**Internal solder layers**
High temperature reverse bias (HTRB)	✓	✓				✓			✓	✓	
High temperature gate stress (HTGS)						✓	✓				
High humidity, high temperature reverse bias (H3TRB)		✓				✓		✓	✓	✓	
Thermal shock test (TST)			✓	✓	✓					✓	✓
Thermal cycling ($\mathrm{PC}_{\mathrm{min}}$)			✓	✓	✓					✓	✓
Power-cycling ($\mathrm{PC}_{\mathrm{sec}}$)			**✓**								**✓**
Vibration			✓	✓	✓					✓	✓

conductor chip constant, thereby shifting the predominantly caused failure type towards the chip solder. Of course, this strategy can also be reversed by using an increased heating current for a shorter time, which would shift the stress towards the bond wire connections. A corresponding shift in predominant cause of failure was shown in [10], where modules were aged in a typical power-cycling test without switching losses and using an AC test bench where the modules were operated in PWM. The modules aged in continuous PWM operation exhibited fewer bond wire lift-offs or heel cracks as the main cause of failure.

Control strategy During the $\mathrm{PC}_{\mathrm{sec}}$ tests conducted, the heating current I_{heat}, the heating phase duration t_{on} and the cool-down phase duration t_{off} are kept constant. Any degradation of the chip solder generated during the $\mathrm{PC}_{\mathrm{sec}}$ tests further increases the thermal resistance of the semiconductor, and therefore increases the temperature swing. Furthermore, the increased temperature generally raises the losses due to the typical PTC behavior at high currents. Consequently, the module degradation accelerates due to the aging itself. This aspect of the tests is acknowledged and considered in the standards [5, 6]. The implications of using this control strategy compared to other methods, e.g., controlling a constant temperature swing or controlling constant loss levels, are discussed in detail in [164].

14.2 Description of the test bench

A total of seven modules M_1 to M_7 are used in the tests. The test procedure for two modules differs from that applied to the others. Module M_5 is randomly selected as a reference module. It goes through the same processing steps, e.g., mounting, dismounting, transporting or measurements, as the other modules, but no heating current is applied during the tests. It is still mounted, moved and analyzed with the TSEP measurement system. Module M_2 is removed from the tests after approximately one half of its expected lifetime for investigations outside the scope of this work. A list of all modules used within this work and their purposes is provided in Table L.1. A photo of the test bench is shown in Figure 14.1.

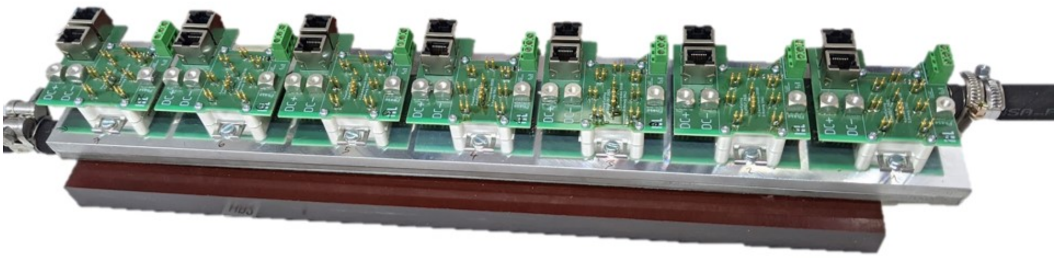

Figure 14.1: Photo of the power-cycling test bench with module M_7 (left) to M_1 (right); fluid inlet on the left; the PCBs provide contacts for a load current, gate voltage application and read-outs

The modules are aged for a predetermined number of accelerated aging cycles at the Fraunhofer IISB. Then, the modules are dismounted and sent to the author for TSEP analysis. Afterwards, the modules are sent back to the Fraunhofer IISB. Further accelerated aging cycles and TSEP analysis cycles follow. Details of the test procedure will be presented in Section 14.3.1.

The aging tests are conducted based on the standards [5] and [6]. The standards cannot be followed precisely, as they do not permit the periodic dismounting and remounting of the modules, which is needed for TSEP analysis. Thermal paste is used as TIM during the accelerated aging phases at the Fraunhofer IISB. During the TSEP measurements, a nonadhesive silicone sheet [165] is used to improve the reproducibility of results between analysis cycles. Nevertheless, the thermal conductivity of this silicone sheet depends on the applied pressure. Thus, variations between the analysis cycles are still expected, as the pressure on the silicone sheet is defined by the spring tabs of the module casing, which is not assumed to be designed for repeated remounting with defined force levels, see Figure 14.2.

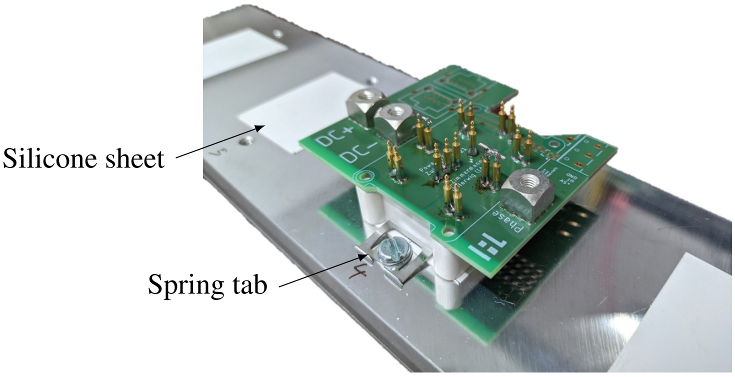

Figure 14.2: Photo of the silicone sheet and spring tabs; setup used for TSEP measurements only; photo taken during thermal characterization; (gates are not shorted during the power cycling)

14.3 Power-cycling tests

The basic thermal profile of a $\mathrm{PC_{sec}}$ for two switches, one at the inlet and the other at the outlet of the cooler, is illustrated in Figure 14.3. In these examples, a high heating current is applied for $t_{\mathrm{on}} = 3\,\mathrm{s}$, followed by a cool-down phase of $t_{\mathrm{off}} = 6\,\mathrm{s}$. The virtual junction temperature of the switches considered rises and settles at ϑ_{max}. At the end of the cool-down phase, the virtual junction temperature settles at ϑ_{min}, resulting in a temperature swing of

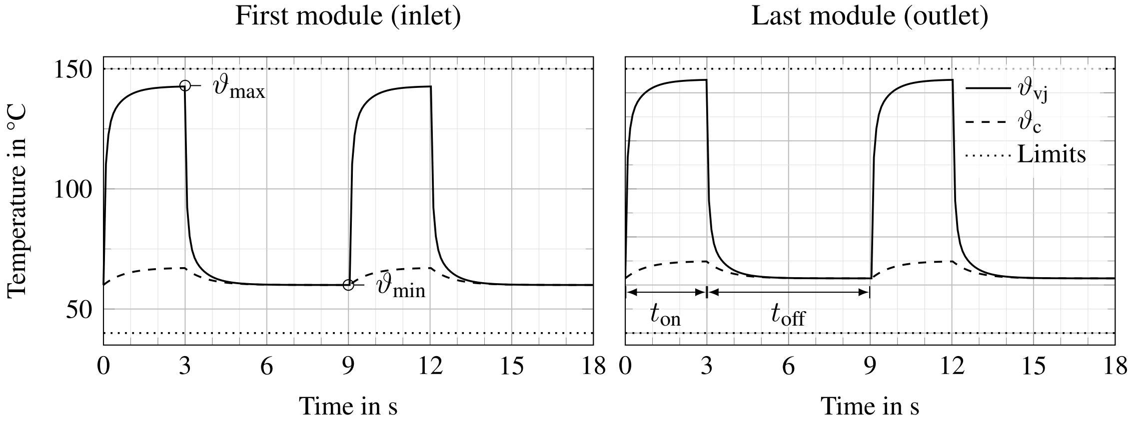

Figure 14.3: Illustration of the thermal load profile during a $\mathrm{PC_{sec}}$, estimated before the tests; virtual junction temperature ϑ_{vj}, heat-sink temperature below the module ϑ_{c}, and acceptable limits for ϑ_{vj} for all modules included in the test

$$\Delta\vartheta_{\mathrm{vj}} = \vartheta_{\mathrm{max}} - \vartheta_{\mathrm{min}}. \tag{14.1}$$

The temperature ϑ_{c} of the cooler below the module cases increases due to the losses. The product qualification report for the modules under test [166] rates them for 25 000 cycles in $\mathrm{PC_{sec}}$ tests with an 80 K temperature swing $\Delta\vartheta_{\mathrm{vj}}$. Therefore, the target temperature swing in the $\mathrm{PC_{sec}}$ tests conducted is also set to 80 K. During the course of this chapter, the EOL of the modules is assumed to occur at approximately 25 000 cycles.

The limits of the test parameters $\Delta\vartheta_{\mathrm{vj}}, \vartheta_{\mathrm{min}}, \vartheta_{\mathrm{max}}$ and ϑ_{c} are defined in [6] and listed in Table 14.2 for reference. At first glance, the parameters set by the standard are not coherent in itself and cannot be fulfilled simultaneously, i.e., the difference between the minimum and maximum virtual junction temperature does yield a permissible temperature swing

Table 14.2: Test parameter limits according to [6]

Temperature swing	$\Delta\vartheta_{\mathrm{vj}}^{(\mathrm{ISO})}$	80 K (75 K, 85 K)
Minimum virtual junction temperature	$\vartheta_{\mathrm{min}}^{(\mathrm{ISO})}$	45 K (40 K, 50 K)
Maximum virtual junction temperature	$\vartheta_{\mathrm{max}}^{(\mathrm{ISO})}$	150 K (140 K, 150 K)
Maximum case temperature increase	$\Delta\vartheta_{\mathrm{c}}^{(\mathrm{ISO})} = (\vartheta_{\mathrm{c}} - \vartheta_{\mathrm{a}})$	30 K

$$\vartheta_{\mathrm{max}}^{(\mathrm{ISO})} - \vartheta_{\mathrm{min}}^{(\mathrm{ISO})} = 105\,\mathrm{K}\,(90\,\mathrm{K}, 110\,\mathrm{K}) \neq \Delta\vartheta_{\mathrm{vj}}^{(\mathrm{ISO})}. \tag{14.2}$$

Accordingly, the stated values of the minimum $\vartheta_{\min}^{(\mathrm{ISO})}$ and maximum $\vartheta_{\max}^{(\mathrm{ISO})}$ junction temperature are understood as limits that may not be breached by any of the modules mounted on the cooler. The temperature of the modules increases during testing due to the losses being transported from the fluid inlet to the outlet. This must be accounted for, so that all modules stay within the temperature limits defined in Table 14.2 [6].

The waveforms illustrated in Figure 14.3 are estimations prepared beforehand. The final parameters are set empirically at the beginning of the $\mathrm{PC}_{\mathrm{sec}}$ and are listed in Table 14.3[1].

Table 14.3: Parameters used during the $\mathrm{PC}_{\mathrm{sec}}$

Duration of the heating phase	t_{on}	3 s
Duration of the cool-down phase	t_{off}	6 s
Heating current	I_{heat}	$50\,\mathrm{A} \mathrel{\widehat{=}} I_{\mathrm{N}}$
Fluid temperature	ϑ_{a}	60 °C

The virtual junction temperature is measured using a small measurement current passed through the body diodes during the cool-down phase [8], analogous to Chapter 12.

Failure criteria A module is defined as failed if its on-state voltage rises by 5 % of its initial value or if its thermal resistance rises by 20 % [5]. Whether the increase in the on-state voltage is caused by degradation of the bond wire connections or if it is due to an increased temperature arising from solder degradation is not relevant for the decision.

The on-state voltage $U_{\mathrm{ds,on}}$ is measured at the end of the conduction phase and the heating current I_{heat} is constant, therefore the losses at this moment are known. The thermal resistance is monitored during the tests based on the measured temperature swing and the losses according to

$$R_{\mathrm{th}} := \frac{\vartheta_{\max} - \vartheta_{\min}}{U_{\mathrm{ds,on}} I_{\mathrm{heat}}}. \tag{14.3}$$

This technique, or definition, requires the junction temperature to have settled at $\vartheta_{\max}$ or $\vartheta_{\min}$ before switching the heating current. The heat-sink temperature ϑ_{c} below the modules changes during the heating phase, which is included in the temperature swing. The thermal resistance of the entire cooling system is included in the thermal resistance determined, as it affects the minimum and maximum junction temperatures. Consequently, the choice of the external cooling system affects the threshold at which the thermal resistance failure criterion is reached. This issue is addressed indirectly in [6] by defining limits for the maximum acceptable increase in the heat-sink temperature ϑ_{c}.

> **Remark:** Requirements for the TIM between the modules and the cooler are not defined directly. Instead, the maximum case temperature increase $\Delta\vartheta_{\mathrm{c}}^{(\mathrm{ISO})}$ defines the portion of the temperature swing $\Delta\vartheta_{\mathrm{vj}}$ that may occur between the cooler and the case. A maximum thermal resistance of the ambient-to-case transition $R_{\mathrm{th,ca}}$ compared to the thermal resistance from the junction to the

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[1] Figure 14.3 was adapted afterwards to coincide with the empiric parameters.

case $R_{\text{th,jc}}$ can be deducted

$$\frac{\Delta\vartheta_{\text{c}}^{(\text{ISO})}}{\Delta\vartheta_{\text{vj}}^{(\text{ISO})} - \Delta\vartheta_{\text{c}}^{(\text{ISO})}} \overset{!}{>} \frac{R_{\text{th,ca}}}{R_{\text{th,jc}}}, \tag{14.4}$$

$$\Leftrightarrow \quad R_{\text{th,ca}} < R_{\text{th,jc}} \frac{\Delta\vartheta_{\text{c}}^{(\text{ISO})}}{\Delta\vartheta_{\text{vj}}^{(\text{ISO})} - \Delta\vartheta_{\text{c}}^{(\text{ISO})}} = R_{\text{th,jc}} \frac{30\,\text{K}}{80\,\text{K} - 30\,\text{K}} \tag{14.5}$$

$$\approx 0.6 R_{\text{th,jc}} = 0.375 \underbrace{\left(R_{\text{th,ca}} + R_{\text{th,jc}}\right)}_{=R_{\text{th,ja}}}. \tag{14.6}$$

The thermal resistance of the TIM and the heat-sink-to-ambient must be smaller than 60 % of the modules thermal resistance $R_{\text{th,jc}}$ from the junction to the case, or smaller than 37.5 % of the thermal resistance $R_{\text{th,ja}}$ between the junction and ambient, i.e., the fluid of the heat sink. This degree of freedom may lead to types of changes.

First, allowing the case temperature increase to rise to its maximum value of 30 K limits the temperature difference between the junction and the case to 50 K instead of 80 K. Although the junction itself always swings by 80 K, this limits the temperature gradient between the junction and the case. The different degradation mechanisms occurring simultaneously within the module may change. Consequently, the choice of a TIM with very low thermal resistance or the maximum permissible thermal resistance may change the resulting extent and characteristic of the module degradation.

Second, one failure criterion is defined as a 5 % increase in thermal resistance. The thermal resistance is defined by the temperature swing of the junction between ϑ_{max} and ϑ_{min} and the losses (14.3). At the end of the cooling phase, the temperature difference between the junction ϑ_{min} and the case ϑ_{c} can be assumed to be small. Thus, the thermal resistance used for the failure criterion includes, or is at least significantly influenced by, the thermal resistance of the TIM. Choosing a TIM with a high thermal resistance decreases the *relative* contribution of degradation effects within the module to the overall thermal resistance used as failure metric.

During the tests, thermal paste according to the datasheet [147] is used.

14.3.1 Test procedure employed

The PC_{sec} aging cycles are performed by the Fraunhofer IISB. For each TSEP measurement, the PC_{sec} is halted, the modules are dismounted from the liquid cooler at the Fraunhofer IISB and sent to the author for the TSEP measurements. A TSEP analysis is done before the tests started, after 50 % EOL, after 80 % EOL and after each switch meets at least one of the failure criteria, see Table 14.4. The final cycle count varies between the switches, therefore the last TSEP analysis is done at differing cycle counts. The four TSEP measurements split the PC_{sec} into three segments.

The interruption of the PC_{sec} and the remounting of the modules lead to discontinuities in the testing parameters that will be discussed in this section. Figure 14.4 shows the first aging sequence and the first remounting of the modules. The graph includes the on-state voltage

Table 14.4: Timing of the TSEP analysis

Approximately reached EOL	Cycles n_{cycle}	Comment
0 %	0	Initial measurement of the new modules
50 %	12 500	M_2 removed afterwards for use in another project
80 %	20 000	
100 %	24 077 to 30 718	Power cycling continued until one EOL criterion is met for every switch

$u_{\text{ds,on}}$ at ϑ_{max}, the measured temperature swing $\Delta\vartheta_{\text{vj}}$ and the applied gate voltages u_{g}. Only three modules are shown for clarity.

In the very beginning, the on-state voltage and temperature swing differ for each switch. The two main reasons for this are the differences in the threshold voltage and the varying thermal resistance between a module and the cooler, caused by differences in the mounting and the thermal paste. The temperature difference seen in the cooling fluid between the inlet and outlet was in the range of 2 K to 3 K. During the first 500 cycles, the gate voltage u_{g} of each switch was adjusted so that the temperature swing $\Delta\vartheta_{\text{vj}}$ of each switch was close to 80 K. After the first 500 cycles, the gate voltage u_{g} is kept constant and any increase in the temperature swing due to aging is accepted as part of the testing strategy. Changes due to the thermal paste moving and redistributing itself during the first thermal cycles are expected to have decayed at this point.

Remounting procedure After 12 500 cycles, the first PC_{sec} segment ends and the modules are dismounted from the cooler of the PC_{sec} test bench and sent to the author for the first time. After the TSEP analysis, the modules are sent back to continue the power-cycling. Stress caused by the transport or the TSEP analysis is not included in the PC_{sec} test results, as the temperature swing during this regular continuous PWM operation is small compared to that of the PC_{sec}.

It can be seen in Figure 14.4 that the temperature swings of each switch change drastically after remounting the modules. This is most likely caused by the changes in the mounting pressure and the reapplication of fresh thermal paste. After 13 800 cycles, the testing is halted and the gate voltages are reinitialized. The gate voltages are adjusted until the temperature swing $\Delta\vartheta_{\text{vj}}$ of each switch matches the temperature swing right before the modules were dismounted. This strategy for reinitialization was chosen because it keeps the thermal stress at the chip-near interconnects as consistent as circumstances allow.

Reinitialization of the EOL criteria The EOL criteria are defined as relative changes in the on-state voltage or in the thermal resistance of the switches. After remounting, the value of the on-state voltage may jump, due to the changed thermal and electrical conditions. It changes independently of the actual degradation of the module, making the direct application of the EOL criteria unfeasible.

Usually, the on-state voltage is normalized to give a persistent voltage reference $U_{\text{ds,on,ref}}$, i.e., the on-state voltage at the beginning of the PC_{sec}. In order to separate voltage changes

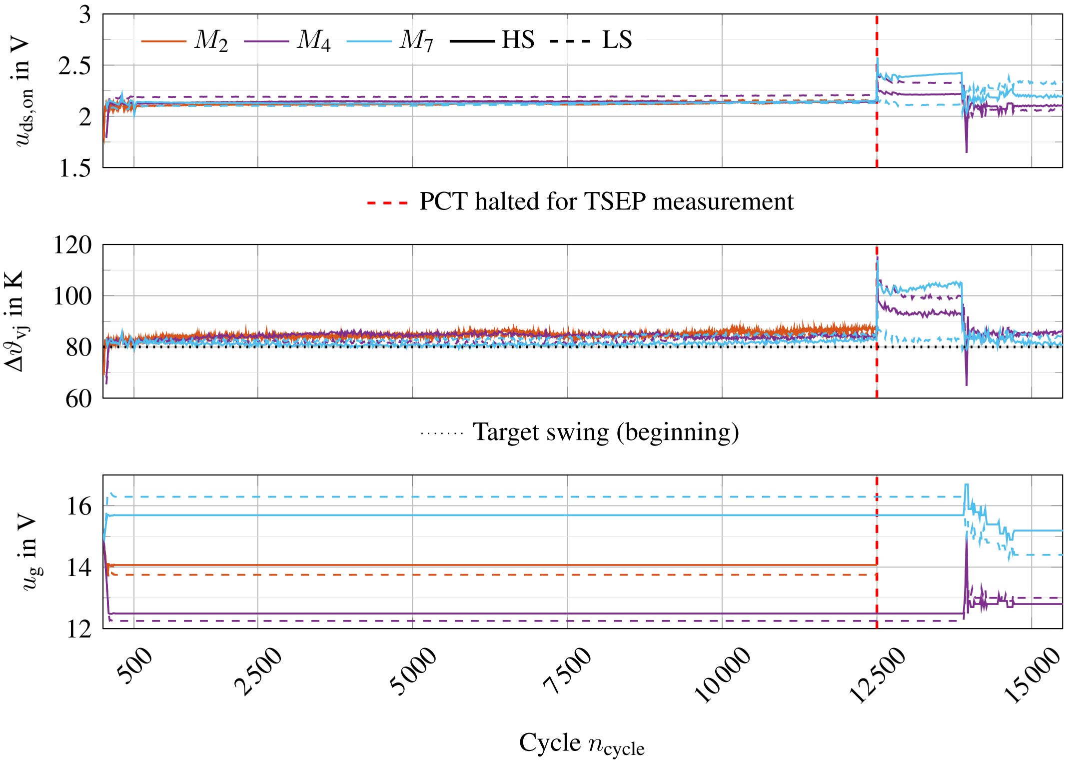

Figure 14.4: First aging sequence and first remounting procedure; only three modules plotted as examples

due to the degradation and the remounting, the reference voltage used for normalization is also reinitialized. First, the phase after remounting when the thermal paste is settling, or the gate voltages are still being adjusted, is masked. Then, the reference voltage is recalculated such that the normalized on-state voltage after settling equals the normalized on-state voltage before remounting

$$u'_{\mathrm{ds,on}} := \frac{u_{\mathrm{ds,on}}}{U_{\mathrm{ds,on,ref}}} \tag{14.7}$$

$$u'_{\mathrm{ds,on}}\Big|_{n_{\mathrm{cycle}}\approx 13\,000} \overset{!}{=} u'_{\mathrm{ds,on}}\Big|_{n_{\mathrm{cycle}}=12\,500} \tag{14.8}$$

$$\Leftrightarrow \quad U_{\mathrm{ds,on,ref}}\Big|_{n_{\mathrm{cycle}}\approx 13\,000} = U_{\mathrm{ds,on,ref}}\Big|_{n_{\mathrm{cycle}}=12\,500} \frac{u_{\mathrm{ds,on}}\Big|_{n_{\mathrm{cycle}}\approx 13\,000}}{u_{\mathrm{ds,on}}\Big|_{n_{\mathrm{cycle}}=12\,500}}. \tag{14.9}$$

The process is illustrated for the high-side switch of module M_4 in Figure 14.5. This procedure is applied to each switch individually after every remounting during the $\mathrm{PC}_{\mathrm{sec}}$.

14.3.2 Power-cycling test results

Figure 14.6 shows the overall course of the $\mathrm{PC}_{\mathrm{sec}}$ for the six aged modules with two topological switches each. Module M_5 is not included, as it was not aged during the tests. The diagram includes the on-state voltage $u_{\mathrm{ds,on}}$, the thermal resistance $r_{\mathrm{th}} \mathrel{\widehat{=}} R_{\mathrm{th}}(t)$, the temperature swing $\Delta\vartheta_{\mathrm{vj}}$, and the applied gate voltage u_{g}. For the on-state voltage and the thermal resistance, plots using the normalized values for evaluating the EOL criteria are also in-

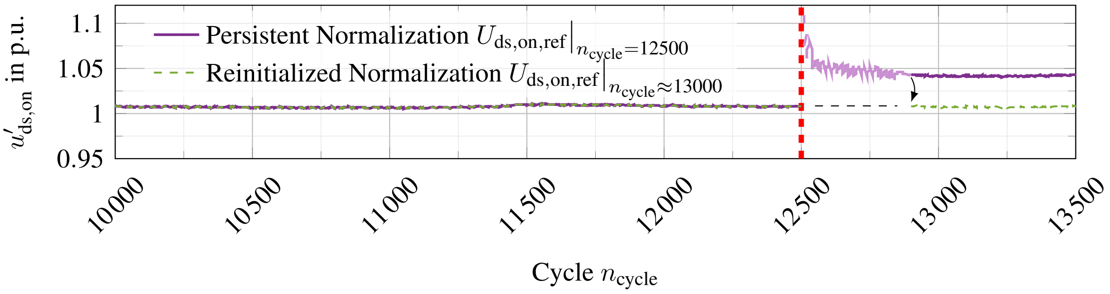

Figure 14.5: Reinitialization of the normalization; masked cycles marked by lighter colors; with the persistent normalization, the EOL criterion is almost reached after remounting, even though the module did not degrade correspondingly

cluded. The masked periods for reinitialization are marked by lighter colors in the measured values and as gaps in the plots of the normalized values, see Marker I. In addition to the steps caused by remounting, a fault in the cooling system at approximately 16 000 cycles had to be masked, see Marker II.

All switches reached the EOL criterion of a 5 % increase in $u_{\mathrm{ds,on}}$ first. Module M_1 shows a faster increase in $u_{\mathrm{ds,on}}$ than the rest of the modules, even though it does not show any notable difference in temperature swing $\Delta\vartheta_{\mathrm{vj}}$ or r_{th}. This could indicate degradation of the bond connection, including reconstruction of the metallization.

14.4 TSEP analysis results

Each switch was measured with the TSEP measurement system at four different stages during the accelerated aging tests, see Table 14.4. This includes double-pulse experiments and regular continuous PWM operation under load. The aim is to validate whether the TSEP measurement system is capable of detecting bond connection degradation and solder degradation. The double-pulse experiments should not be affected noticeably by changes in the thermal impedance of the switches, as the self heating is neglectable. Therefore, the TSEP results in double-pulse experiments depend only on the degradation of the bond connections. In continuous PWM operation, both types of degradation should affect the TSEPs. Consequently, the TSEP analysis is split into results obtained in double-pulse experiments and in continuous PWM operation.

14.4.1 Double-pulse experiments

The amount of data acquired in double-pulse experiments is too large to display and assess trivially. The investigations in this section will focus on data trends, histograms, and similar evaluation methods to condense the data to more comprehensible sizes. All TSEPs measured in double-pulse experiments for all modules, switches and aging stages are listed in Appendix L.

During the double-pulse experiments, the modules are mounted on a large heat plate. The losses generated within the semiconductors are neglectable, thus the semiconductors and the NTC sensor have the same temperature. During the double-pulse experiments, the NTC sensor temperature is used as temperature reference for the low-side and high-side switches.

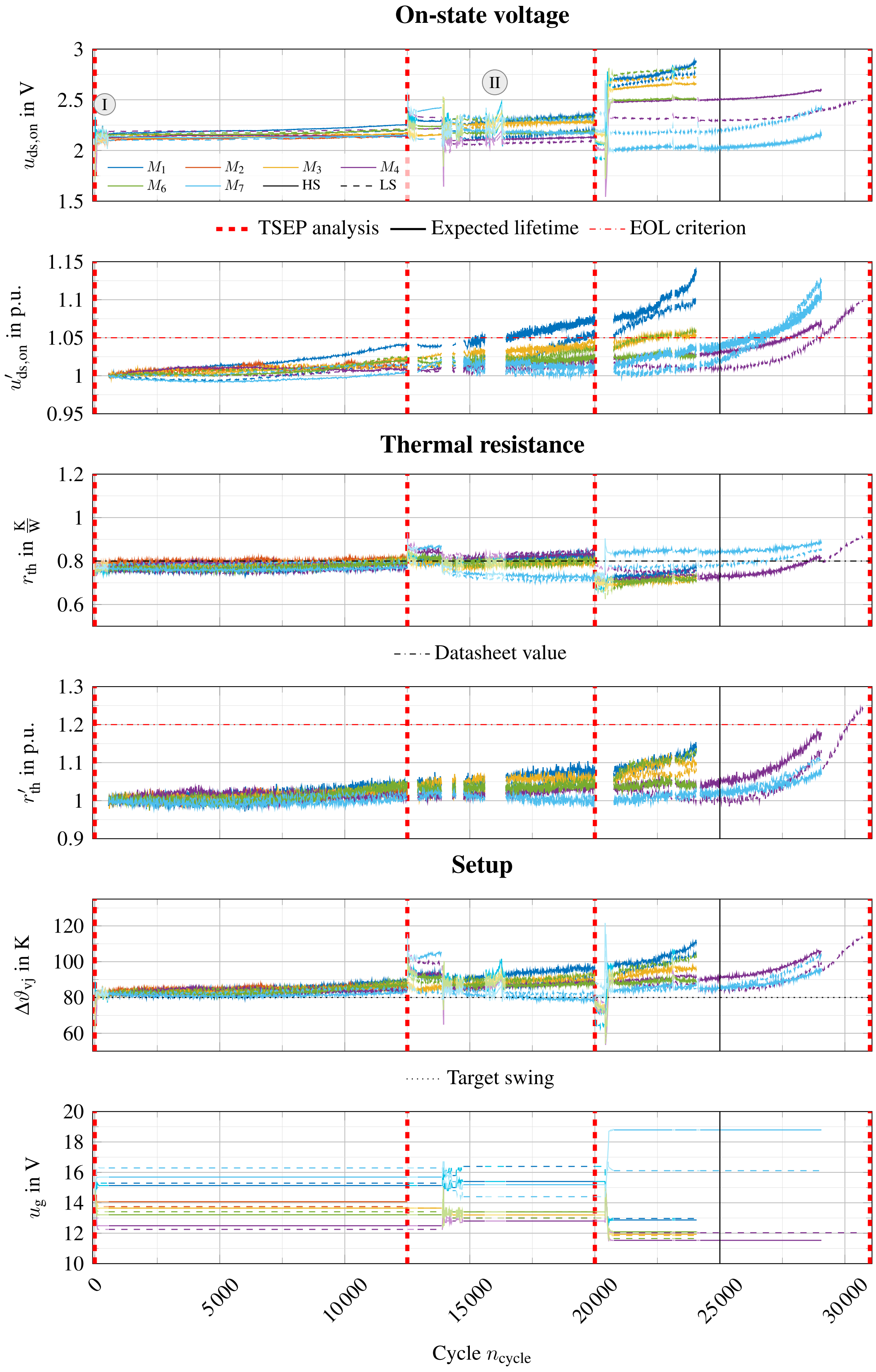

Figure 14.6: Overview of the PCT; unused recalibration data masked by lighter colors

On-state voltage The on-state voltage depends on the drain current, the junction temperature and the degradation of the module. In order to plot these dependencies, a normalized on-state voltage is introduced

$$U'_{\text{uncompensated}}\left(I_{\text{d,sp}},\vartheta_{\text{sp}}\right) := \frac{U_{\text{ds,virt,turnon}}\left(I_{\text{d,sp}},\vartheta_{\text{sp}}\right)}{U_{\text{ds,virt,turnon}}\left(I_{\text{d,sp}},\vartheta_{\text{sp}}\right)\big|_{n_{\text{cycle}}=0}}. \tag{14.10}$$

The on-state voltages measured after the module has been exposed to aging stress are normalized to the on-state voltage measured in the initial state of the module at $n_{\text{cycle}} = 0$. This is done for every set point of the load current and the temperature $\left(I_{\text{d,sp}},\vartheta_{\text{sp}}\right)$, to evaluate changes in the TSEPs independent of the set point. An example for the normalization $U'_{\text{uncompensated}}$ is depicted in Figure 14.7 for the last aging stage only. These results show expected behavior. At low currents, the signal-to-noise ratio is low and the determined normalized on-state voltage $U'_{\text{uncompensated}}$ exhibits large variations. With increasing current, the variance becomes smaller.

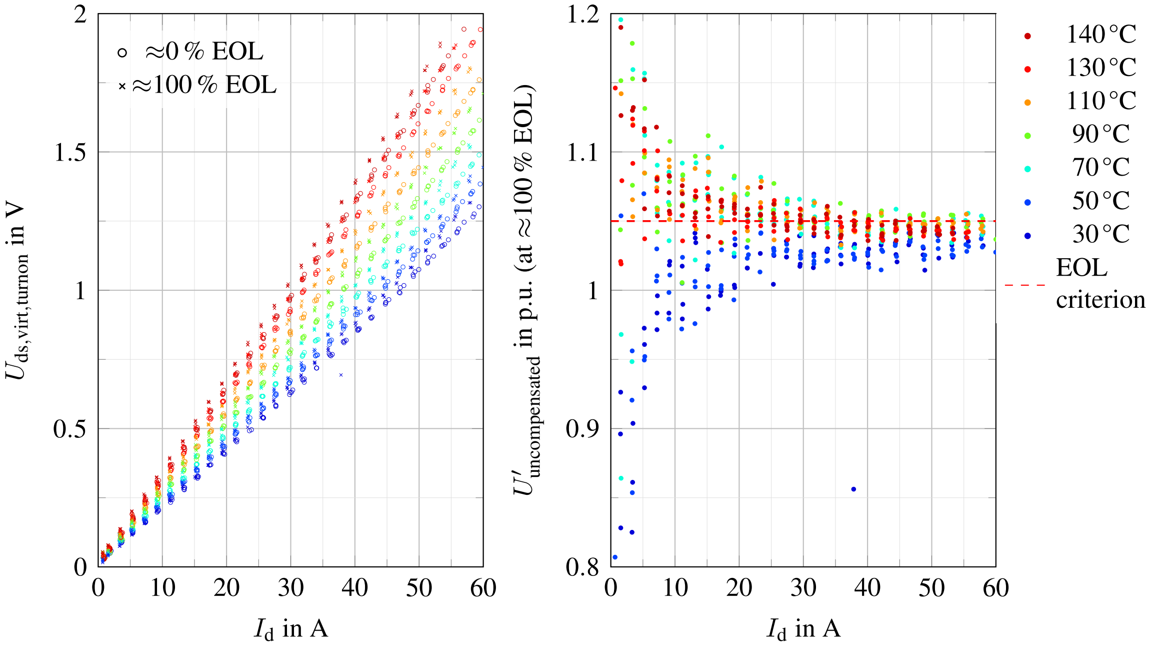

Figure 14.7: Example of the normalization for the high-side switch in module M_3 for the final aging stage only

Histograms of $U'_{\text{uncompensated}}$ for each aging stage are generated in order to assess how their distribution shifts in correlation with the aging stage. The resulting histograms for $U'_{\text{uncompensated}}$ are shown in the left diagram of Figure 14.8. The histograms of $U'_{\text{uncompensated}}$ suggest an increase in the on-state voltage of approximately 7 % compared to the module's initial state. This result is not quite accurate and must be corrected.

Current correction During the double-pulse experiments, the set points are kept equal. Nevertheless, the actually applied currents I_{d} deviate slightly from the set points $I_{\text{d,sp}}$ by approximately 2 %. The observable deviations change in each aging step, as the test bench is rebuilt for each TSEP analysis cycle. The actually applied currents are monitored with an oscilloscope during the experiments and are included in the calibration data sets. This

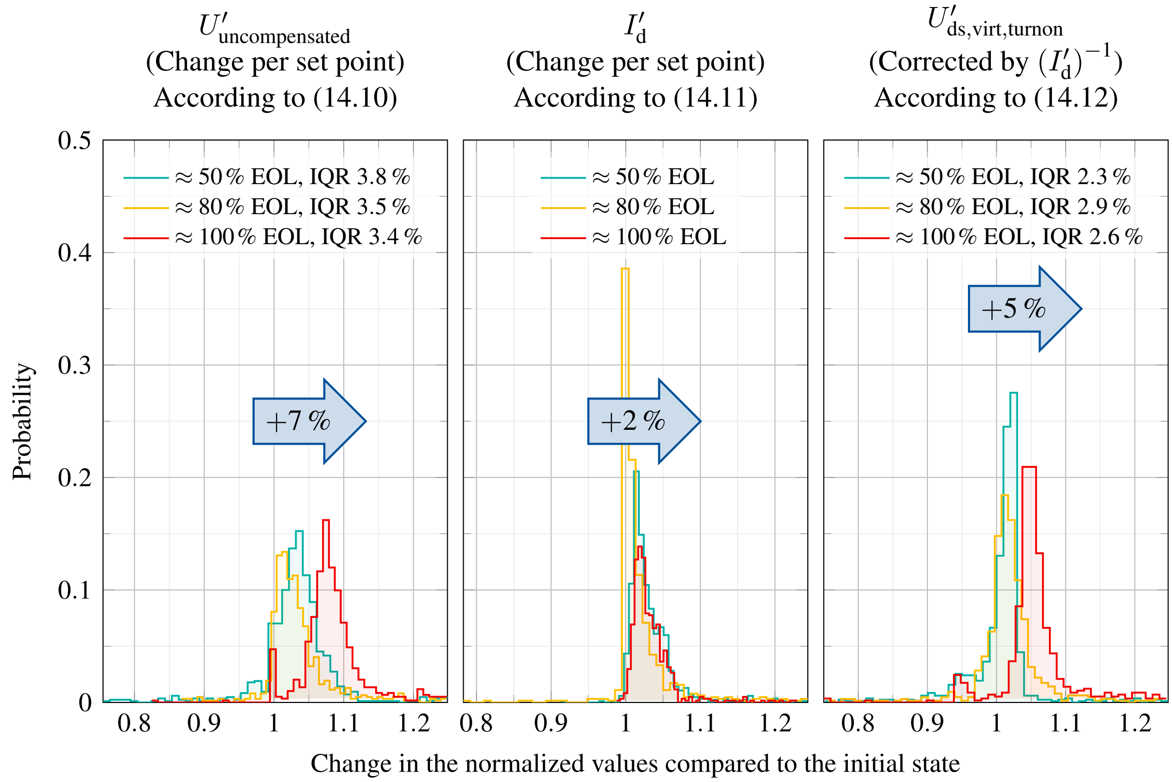

Figure 14.8: Normalized on-state voltage referenced to the initial measurement before the aging tests (left), distribution of the normalized switched currents (middle) and current-corrected normalized on-state voltage (right); 1 % bin width; interquartile range (IQR) from 25 to 75 %; high-side switch of module M_7

directly translates into a misassessment of the change in the on-state voltage if not accounted for. Since the deviations of the currents are small, the measured on-state voltages at each set point are scaled proportionally with the relative change in the applied switching current

$$I'_\mathrm{d}\left(I_\mathrm{d,sp},\vartheta_\mathrm{sp}\right) := \frac{I_\mathrm{d}\left(I_\mathrm{d,sp},\vartheta_\mathrm{sp}\right)}{I_\mathrm{d}\left(I_\mathrm{d,sp},\vartheta_\mathrm{sp}\right)\big|_{n_\mathrm{cycle}=0}}, \tag{14.11}$$

$$U'_\mathrm{ds,virt,turnon}\left(I_\mathrm{d,sp},\vartheta_\mathrm{sp}\right) = U'_\mathrm{uncompensated}\left(I_\mathrm{d,sp},\vartheta_\mathrm{sp}\right) I'^{-1}_\mathrm{d}\left(I_\mathrm{d,sp},\vartheta_\mathrm{sp}\right). \tag{14.12}$$

Thus, definition (14.10) is obsolete and is substituted by (14.12).

A significant portion of the deviations at low currents in Figure 14.7 can be explained by variations in the applied current, rather than the measured voltage. The current-corrected $U'_\mathrm{ds,virt,turnon}$ shows a smaller interquartile range and a more likely drift of the on-state voltage by approximately 5 %.

The concept of the current correction is also applied to $U'_\mathrm{ds,virt,turnoff}$. The normalized current rise time t'_ri was not current corrected, as a simple proportional scaling is not appropriate. No drift is expected in the current rise time due to aging in double-pulse experiments, therefore the missing current compensation is not critical. The additional variation in the TSEPs due to the current variation is accepted.

In the further course of this chapter, the normalized TSEPs and their corresponding data sets S will be used. A summary of all data sets is given in Table 14.5. The union of all

Table 14.5: Definitions of the used normalized TSEPs and data sets

	Data set	Elements
Normalized virtual on-state voltage:		
After turn-on, high-side switch	$S_{U'^{(\mathrm{HS})}_{\mathrm{ds,virt,turnon}}}$	$U'^{(\mathrm{HS})}_{\mathrm{ds,virt,turnon}}$
After turn-on, low-side switch	$S_{U'^{(\mathrm{LS})}_{\mathrm{ds,virt,turnon}}}$	$U'^{(\mathrm{LS})}_{\mathrm{ds,virt,turnon}}$
Before turn-off, high-side switch	$S_{U'^{(\mathrm{HS})}_{\mathrm{ds,virt,turnoff}}}$	$U'^{(\mathrm{HS})}_{\mathrm{ds,virt,turnoff}}$
Before turn-off, low-side switch	$S_{U'^{(\mathrm{LS})}_{\mathrm{ds,virt,turnoff}}}$	$U'^{(\mathrm{LS})}_{\mathrm{ds,virt,turnoff}}$
Union of all voltages	$S_{U_{\mathrm{ds,virt}}}$	$U'_{\mathrm{ds,virt}}$
Normalized switching times:		
Turn-on delay time, high-side switch	$S_{t'^{(\mathrm{HS})}_{\mathrm{d}}}$	$t'^{(\mathrm{HS})}_{\mathrm{d}}$
Turn-on delay time, low-side switch	$S_{t'^{(\mathrm{LS})}_{\mathrm{d}}}$	$t'^{(\mathrm{LS})}_{\mathrm{d}}$
Reaching the overcurrent peak, high-side switch	$S_{t'^{(\mathrm{HS})}_{\mathrm{rrm}}}$	$t'^{(\mathrm{HS})}_{\mathrm{rrm}}$
Reaching the overcurrent peak, low-side switch	$S_{t'^{(\mathrm{LS})}_{\mathrm{rrm}}}$	$t'^{(\mathrm{LS})}_{\mathrm{rrm}}$
Current rise time, high-side switch	$S_{t'^{(\mathrm{HS})}_{\mathrm{ri}}}$	$t'^{(\mathrm{HS})}_{\mathrm{ri}}$
Current rise time, low-side switch	$S_{t'^{(\mathrm{LS})}_{\mathrm{ri}}}$	$t'^{(\mathrm{LS})}_{\mathrm{ri}}$

measured voltages is used to further aggregate the data and assess changes in the on-state voltage independent of the specific measurement setup

$$S_{U_{\mathrm{ds,virt}}} := S_{U'^{(\mathrm{HS})}_{\mathrm{ds,virt,turnon}}} \cup S_{U'^{(\mathrm{LS})}_{\mathrm{ds,virt,turnon}}} \cup S_{U'^{(\mathrm{HS})}_{\mathrm{ds,virt,turnoff}}} \cup S_{U'^{(\mathrm{LS})}_{\mathrm{ds,virt,turnoff}}} . \tag{14.13}$$

TSEP results The relative changes in all aged modules were united for the following investigations. Figure 14.9 depicts histograms of the normalized TSEPs for each aging stage of the high-side switches. Figure 14.10 displays the same data for all aged low-side switches. The results show a clear increase in the measured on-state voltage, matching the expected increase of 5 %. Furthermore, the measured switching times or their preprocessed variants show almost no change, as is to be expected. Therefore, the TSEP measurement system is capable of detecting bond connection degradation. The histograms for the reference module are shown in Appendix N.

The results from the histograms are summarized further. Figure 14.11 depicts the change in the median of the normalized TSEPs depending on the approximately reached percentage of the EOL, based on the same data. Only one reference module was used, thus the amount of reference data is much smaller compared to the available data for the aged modules. In order to improve the precision of the reference data, the unionized data set including all voltage measurements $S_{U_{\mathrm{ds,virt}}}$ according to (14.13) was used.

The on-state voltage of the aged modules shows a steady increase in its median by up to

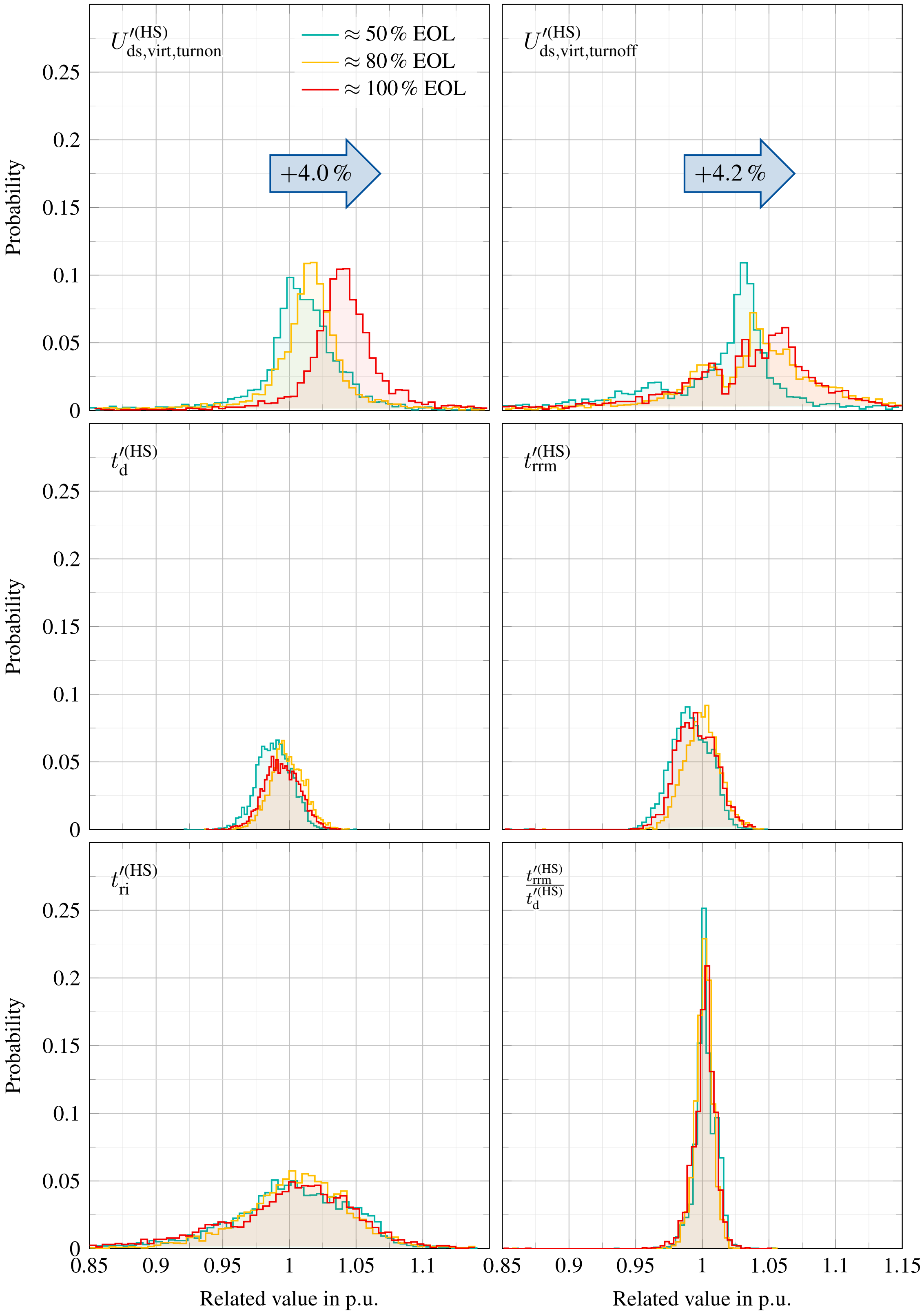

Figure 14.9: Histograms of the normalized TSEPs of the aged high-side switches depending on the approximately reached EOL; for the on-state voltages $U_{ds,virt,turnon}$ and $U_{ds,virt,turnoff}$, the change in the median between the initial state and ≈100 % EOL is shown; data set includes all samples at all currents and temperatures

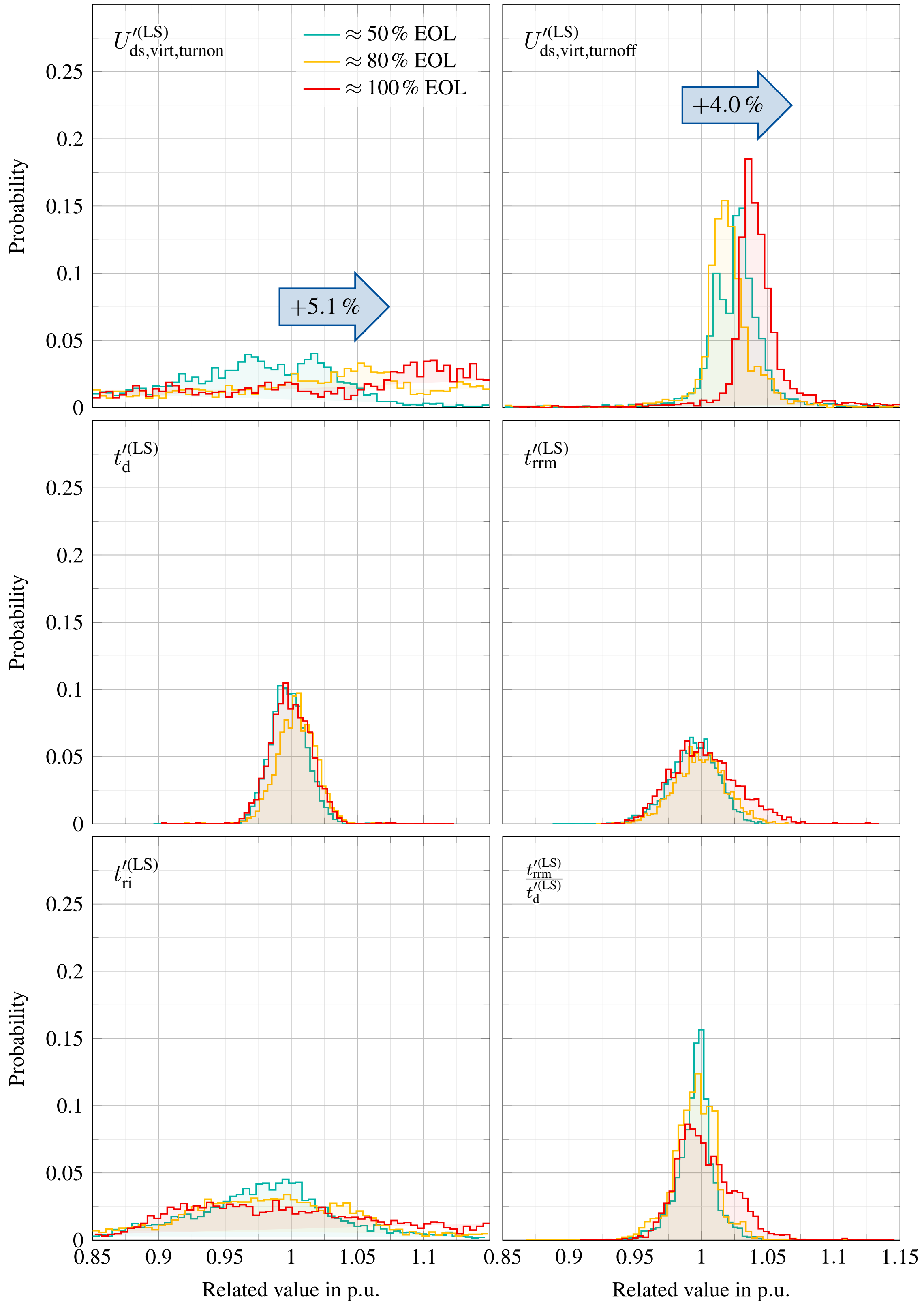

Figure 14.10: Histograms of the normalized TSEPs of the aged low-side switches depending on the approximately reached EOL; for the on-state voltages $U_{ds,virt,turnon}$ and $U_{ds,virt,turnoff}$, the change in the median between the initial state and ≈100 % EOL is shown; data set includes all samples at all currents and temperatures

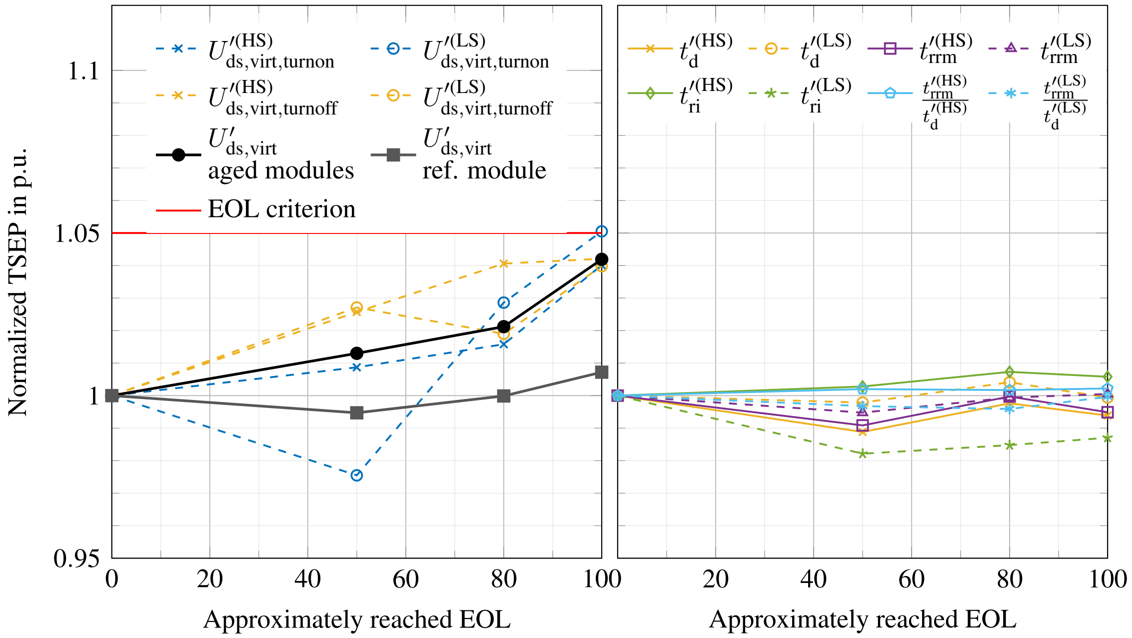

Figure 14.11: Median of the normalized TSEPs depending on the approximately reached EOL; the median of $U'_{ds,virt}$ is shown across all measurements of all aged modules combined and for the reference module alone. For these calculations, the union of all voltages $S_{U_{ds,virt}}$ is used

$+4.2\,\%$, while the reference module varies by around $\pm 0.7\,\%$. The behavior of the aged modules can be clearly distinguished from the behavior of the reference module.

The measured increase in the on-state voltage using the TSEP measurement system is smaller than those observed during the course of the PC_{sec}, as shown in Figure 14.6. During the PC_{sec}, the degradation of the thermal impedance of the switches, in conjunction with the high heating current, increases the maximum junction temperature of the switches. Thus, the on-state voltage during PC_{sec} increases due to the bond connection degradation and the increased temperature concurrently. In all the TSEP measurements in double-pulse experiments, the junction temperature was controlled and did not change between aging stages.

The switching times exhibit no significant trend depending on the stage of aging, see Figure 14.11. This validates the assertion that the switching times are not significantly affected by changes in the bond connections or the *electric* degradation of the solder[2].

Reduced precision of the low side The on-state voltage measurement $U'_{ds,virt,turnon}$ of the low-side switches in Figure 14.10 shows significantly larger deviations than all other on-state voltage measurements. This discrepancy between the high side and low side is traced back to the measurement accuracy difference between the high-side and low-side measurements. Figure 14.12 and Figure 14.13 show the measured on-state voltage $U_{ds,virt,turnon}$ for both sides, for all modules, and stages of aging. It can be seen that the high-side measurements include far less noise than the low-side measurements. The bottom graphs depict the normalized on-state voltage $U'_{ds,virt,turnon}$ at the end of the aging tests, i.e., at 100 % EOL.

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[2] It is not expected that an increase of the electric resistance due to solder degradation impacts the switching times, while a temperature increase resulting from the increased thermal resistance is expected to be reflected in the switching times. The latter cannot be investigated in double-pulse experiments due to the absence of relevant losses.

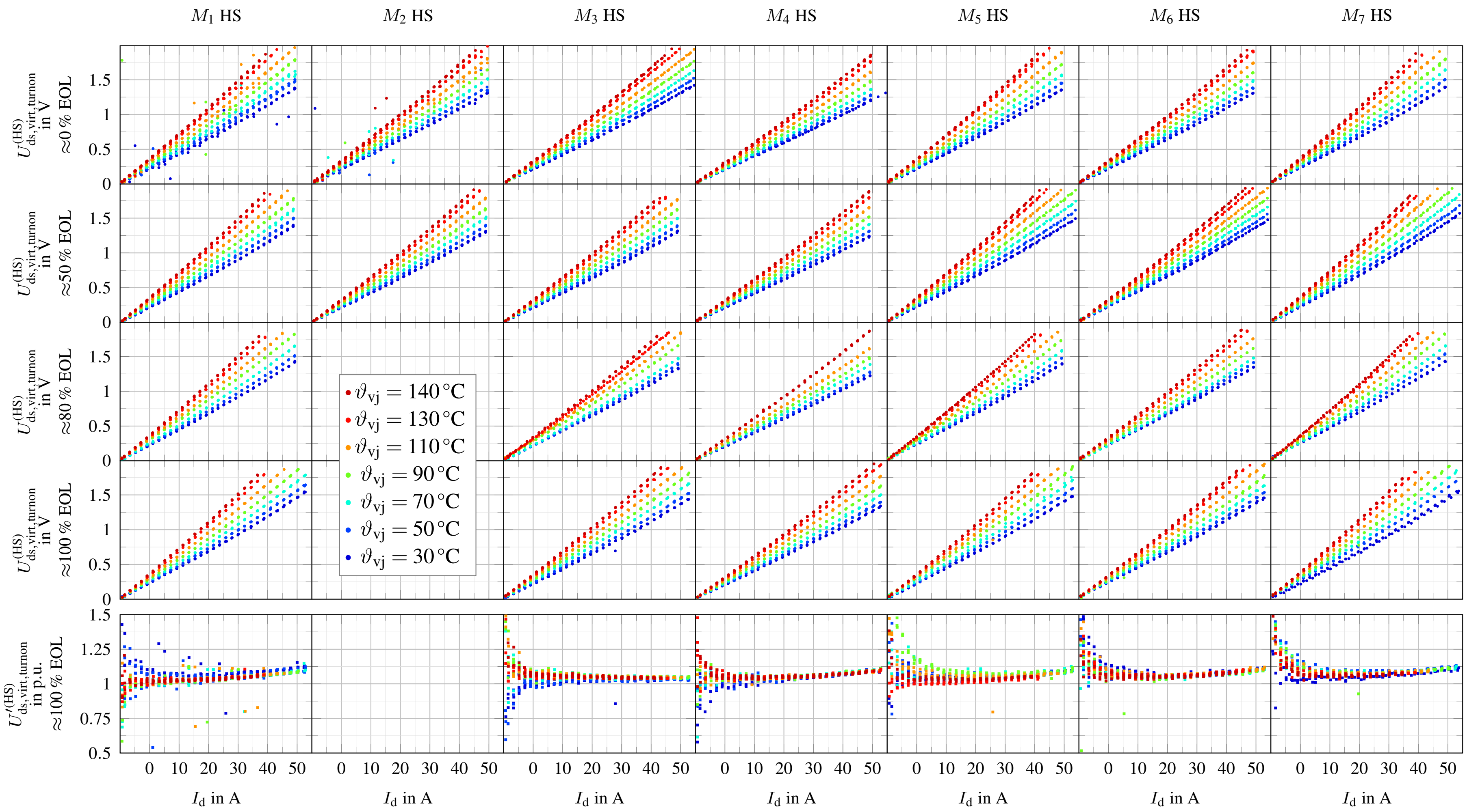

Figure 14.12: Measured on-state voltages of the aged high-side switches depending on the approximately reached EOL in double-pulse experiments; the change in the normalized on-state voltage $U'_{\mathrm{ds,virt,turnon}}$ between the initial state and ≈100 % EOL is shown

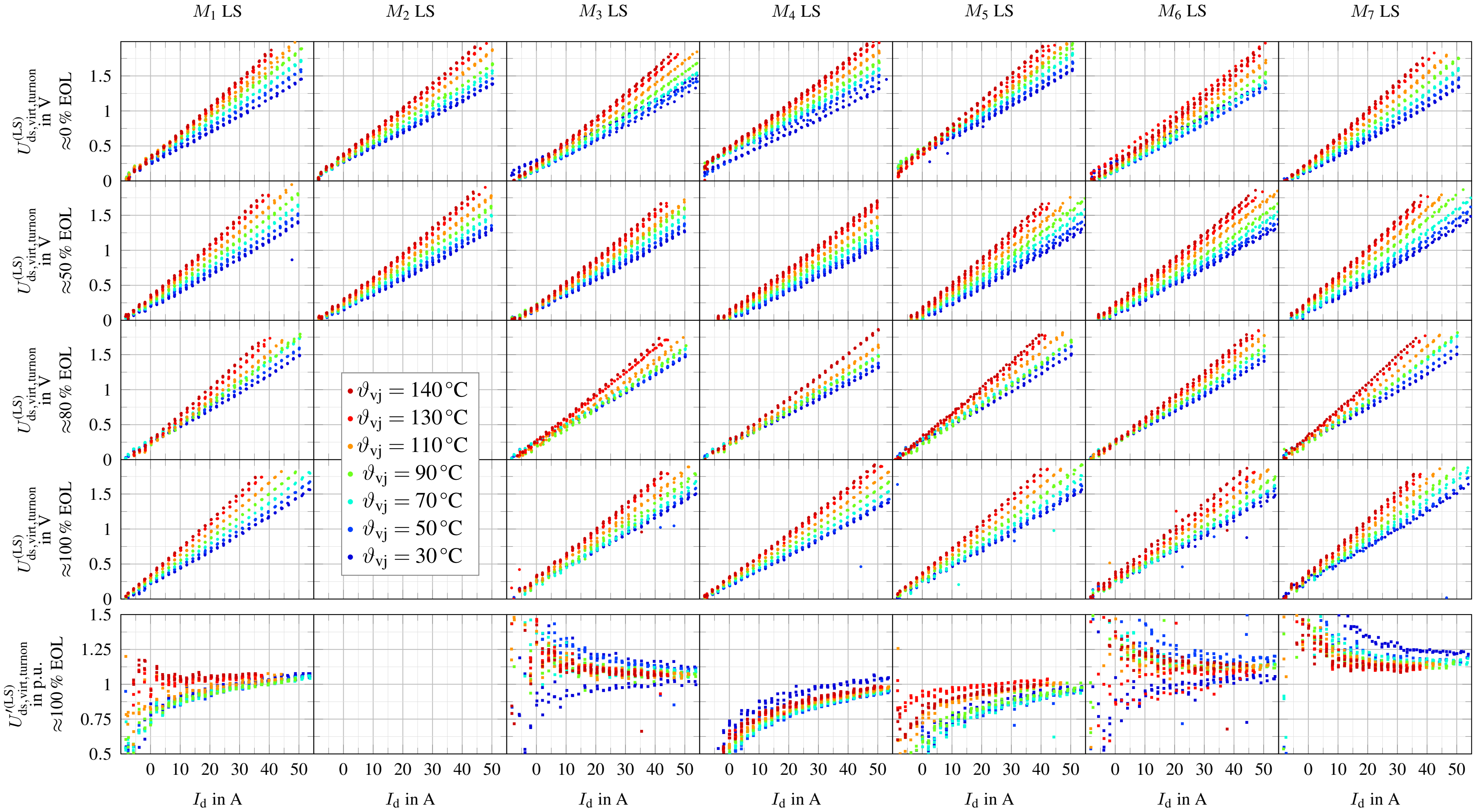

Figure 14.13: Measured on-state voltages of the aged low-side switches depending on the approximately reached EOL in double-pulse experiments; the change in the normalized on-state voltage $U'_{\mathrm{ds,virt,turnon}}$ between the initial state and ≈100 % EOL is shown; Note that the U-I characteristics do not pass through the origin

While this normalized voltage has a very similar characteristic for all high-side switches of the modules, the normalized voltage for the low-side switches varies widely. The low-side measurements do not seem to pass through the origin $U_{\mathrm{ds,virt,turnon}}\left(I_{\mathrm{d}}=0\,\mathrm{A}\right)=0\,\mathrm{V}$ reliably. It is assumed that this effect is largely caused by the external measurement equipment, i.e., the oscilloscope that is only connected to the low side. Nonetheless, the trend of the on-state voltage increase caused by the aging is still clearly visible in Figure 14.10.

14.4.2 Continuous PWM operation

All modules have been analyzed with the TSEP measurement system in continuous PWM operation at the four aging stages. A low-frequency load current of 1 Hz and $\hat{I}_{\mathrm{L}}=I_{\mathrm{N}}=50\,\mathrm{A}$ is applied to cause a large temperature swing of the junction temperature. This load is applied until thermal quasi steady-state is reached. Then, the TSEPs are recorded for several fundamental periods of the load current. This procedure is repeated for every module in every aging stage.

An example of the measured TSEPs for module M_7 in the initial and final aging states only is plotted in Figure 14.14. It can be seen that the applied load current waveform shows little deviation across the aging stages. As expected, the overall change in TSEPs is comparatively small, but an increase in the on-state voltage is clearly visible for all four types of on-state voltage measurement. The switching times t_{d} and t_{rrm} and their preprocessed variants t_{ri} and $\frac{t_{\mathrm{rrm}}}{t_{\mathrm{d}}}$ show a change, but whether this change is significant or not cannot be determined from this graph alone. The NTC sensor temperature rises with the aging stage. As before, histograms of normalized TSEPs will be generated and evaluated.

TSEP normalization The overall changes are small and need to be assessed across multiple modules. Thus, the TSEPs will be normalized, similar to the approach presented in Section 14.4. The value of each variable in the initial state 0 % EOL is used as a reference. The on-state voltages are current-corrected. For the NTC sensor temperature, its temperature increase with respect to the cooling liquid is used as a variable

$$\Delta\vartheta_{\mathrm{NTC}}:=\vartheta_{\mathrm{NTC}}-\vartheta_{\mathrm{a}},\quad \vartheta_{\mathrm{a}}=60\,^{\circ}\mathrm{C}. \tag{14.14}$$

Figure 14.15 shows the normalized PWM measurement for the aged module M_7. The zero crossings of the load current occur at approximately 0 s, 0.5 s and 1 s. At low load currents, the signal-to-noise level increases for all measured TSEPs. A clear, increasing trend of the on-state voltages with aging can be seen at high currents.

The measurements of the switching times t'_{d} and t'_{rrm} show a high noise level which makes interpreting the results difficult. The preprocessed variants t'_{ri} and $\frac{t_{\mathrm{rrm}}}{t_{\mathrm{d}}}'$ exhibit a significantly lower noise level but an increase with aging can be discerned.

The temperature difference between the NTC sensor measurement and the cooling fluid $(\Delta\vartheta_{\mathrm{NTC}})$ shows an increase of approximately $+30\,\%$ during the aging process, which is higher than expected from the determined increase in the on-state voltage. The measurement results in continuous PWM operation for all modules M_1 to M_7 and all aging stages are listed in Appendix M.

The results for the nonaged reference module M_5 are shown in Figure 14.16. All TSEPs show noticeably less change compared to those of the aged module M_7. The high-side on-state voltage measurements change especially little. As before, the preprocessed variants of the switching times t'_{ri} and $\frac{t_{\mathrm{rrm}}}{t_{\mathrm{d}}}'$ exhibit significantly less noise and are close to unity.

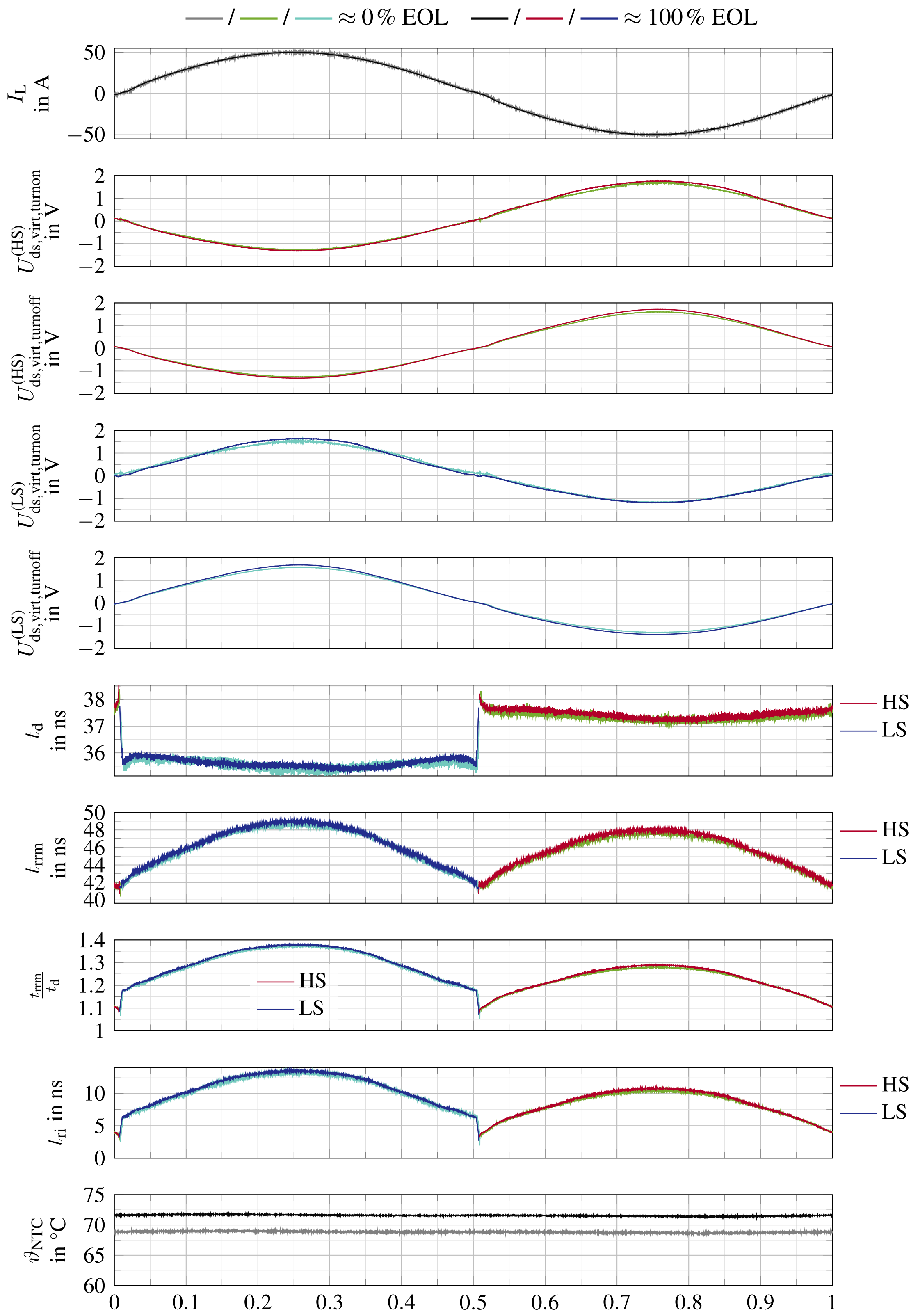

Figure 14.14: Example of the measured TSEPs of module M_7 during continuous PWM operation; results shown for the initial state (lighter colors) and the last aging stage (darker colors); the switching times of the high side and low side are shown on the same graphs, as their times of occurrence form disjointed sets

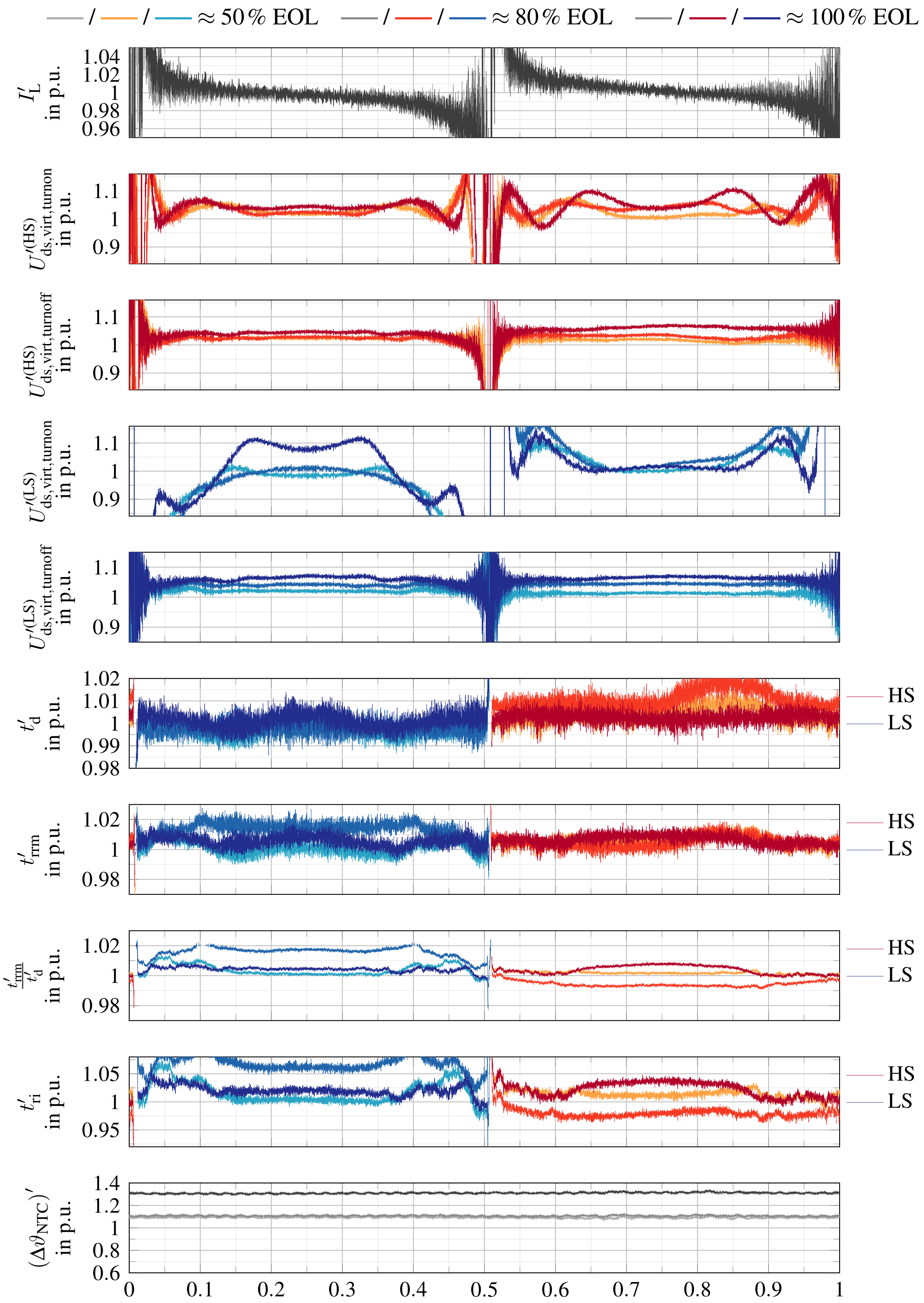

Figure 14.15: Example of the normalized TSEPs of module M_7 during continuous PWM operation; colors darken with the aging progression; the switching times of the high side and low side are shown on the same graphs, as their times of occurrence form disjointed sets

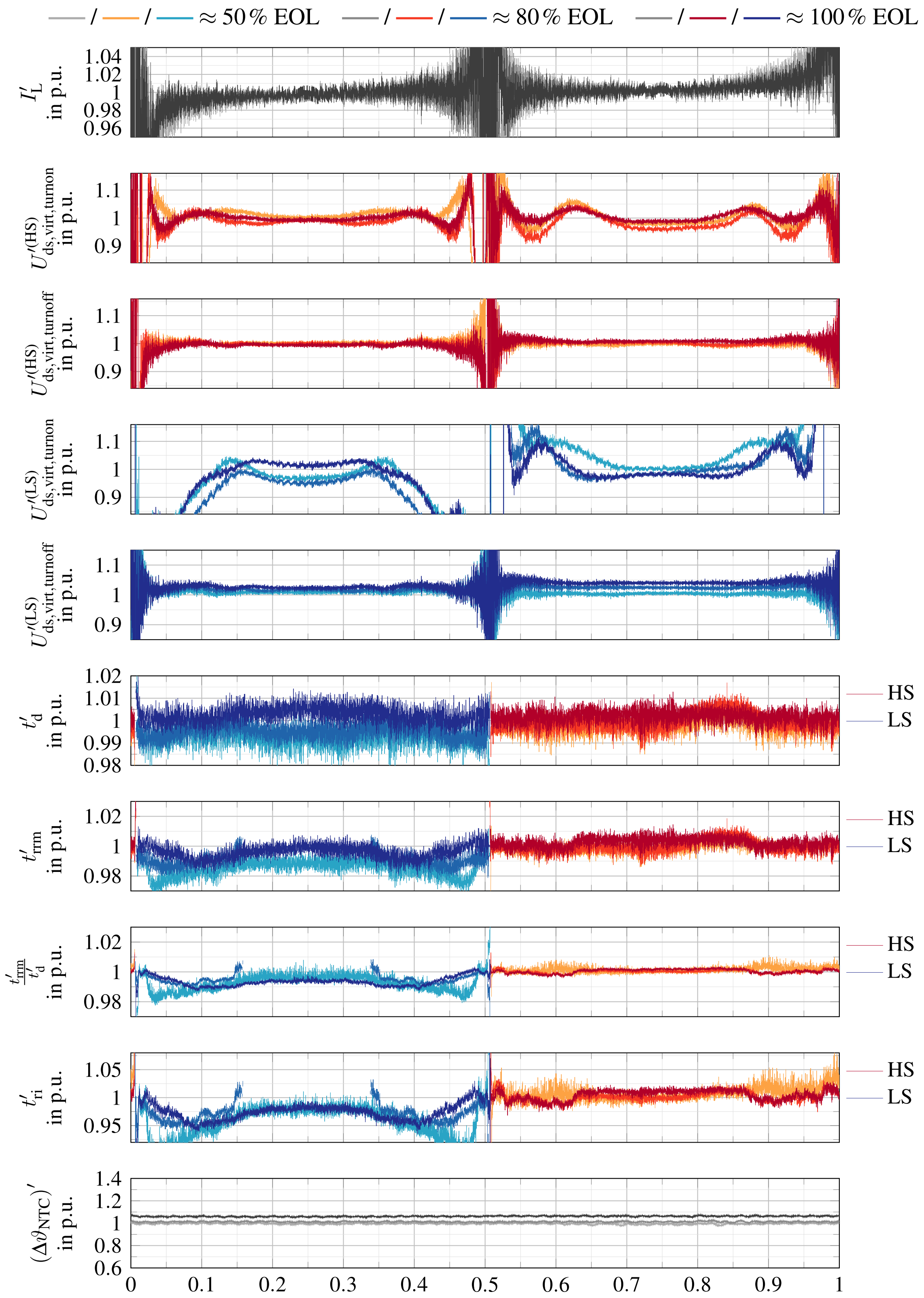

Figure 14.16: Example of the normalized TSEPs of the reference module M_5 during continuous PWM operation; colors darken with the aging progression; the switching times of the high side and low side are shown on the same graphs, as their times of occurrence are disjoint set

The NTC sensor temperature increase above ambient of module M_5 $(\Delta\vartheta_{\text{NTC}})'$ shows an increase of $+6\,\%$. As this module was not aged, this increase shows how much the thermal resistance of the test bench may have changed over the course of the PCT due to the repeated remounting.

14.4.2.1 TSEP shift due to the aging

Histograms of the normalized TSEPs, measured during continuous PWM operation, are depicted in Figure 14.17 and Figure 14.18. The on-state voltages show a clear increase with the aging stage. The results are less consistent than during double-pulse experiments and the measured increase in the on-state voltage is smaller. The measured switching times show no clearly identifiable trend with aging.

In continuous PWM operation, the varying thermal resistances of the modules, in conjunction with the losses, lead to more distinct differences between the modules than seen in double-pulse experiments. Several distinct peaks can be seen in the on-state voltage of the low side $U'^{(\text{LS})}_{\text{ds,virt,turnoff}}$. This demonstrates that in continuous PWM operation, the differences between each module and switch are more pronounced than in double-pulse experiments. To support this deduction, Figure 14.19 shows the corresponding histograms of the NTC sensor temperature increase $(\Delta\vartheta_{\text{NTC}})'$. The temperature increase in the NTC sensor shows many distinct peaks, even within each aging stage. It is likely that each individual peak corresponds to a specific module, TIM sheet, mounting pressure and module degradation.

As a consequence, the degradation detection in continuous PWM operation must be assessed on a per-switch basis. For each switch, the median of each TSEP for each aging stage was determined. The results are shown as gray dots in Figure 14.20. Additionally, the figure includes box plots of the medians of the normalized TSEPs during continuous PWM operation[3]. As before, a clear trend can be seen in the measured on-state voltages. The switching times show no clear trend with aging. Although the expected relative change in the measured switching times t'_{d} and t'_{rrm} is small, a noticeable increase in the current rise time t'_{ri} is expected but not seen.

The normalized temperature difference between the NTC sensor measurement and the cooling fluid $(\Delta\vartheta_{\text{NTC}})'$ shows an increase of 11.8 % in the final aging stage compared to the initial state, see Figure 14.20. This increase should be approximately proportional to the increased losses of the module, due to the degraded bond connections. The solder degradation should not affect $(\Delta\vartheta_{\text{NTC}})'$ directly, as the degradation of the chip solder occurs between the DCB substrate and the chip. Therefore, it should not impact the cross coupling between the chips and the NTC sensor. Of course, the resulting increase in junction temperature would increase the losses, which would increase $(\Delta\vartheta_{\text{NTC}})'$ indirectly. As the increase in $(\Delta\vartheta_{\text{NTC}})'$ is much larger than expected based on the increase in $\left(U_{\text{ds,virt}}\right)'$, degradation of the module mounting between the aging steps can be assumed.

Based on the increase in $(\Delta\vartheta_{\text{NTC}})'$ of the reference module M_5 in the final aging stage, see Figure 14.16, it is possible that an increase of around 6 % can be attributed to the specific test conditions alone, i.e., the repeated remounting of the modules. In the setup used, the temperature and flow rate of the cooling liquid were tightly controlled and known. Whether the module NTC can be used in an application must be evaluated carefully with regard to changes in the coolant temperatures, flow rate and degradation of the cooling system.

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[3] Yes, the red line on the box plots represents the median of the medians.

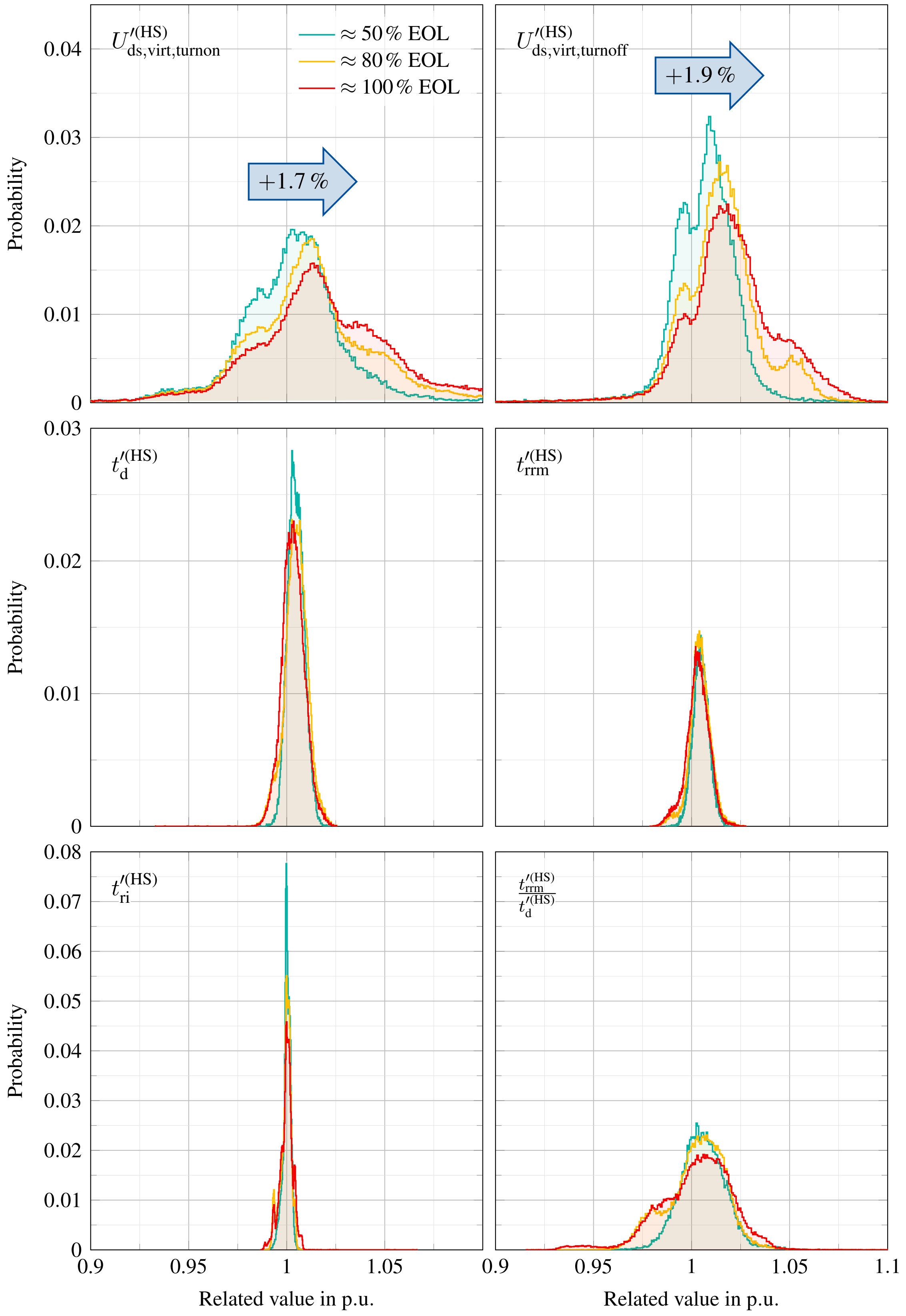

Figure 14.17: Histograms of the normalized TSEPs of the aged high-side switches depending on the approximately reached EOL during continuous PWM operation; bin width 0.1 %; for the on-state voltages $U_{\mathrm{ds,virt,turnon}}$ and $U_{\mathrm{ds,virt,turnoff}}$, the change in the median between the initial state and ≈100 % EOL is shown

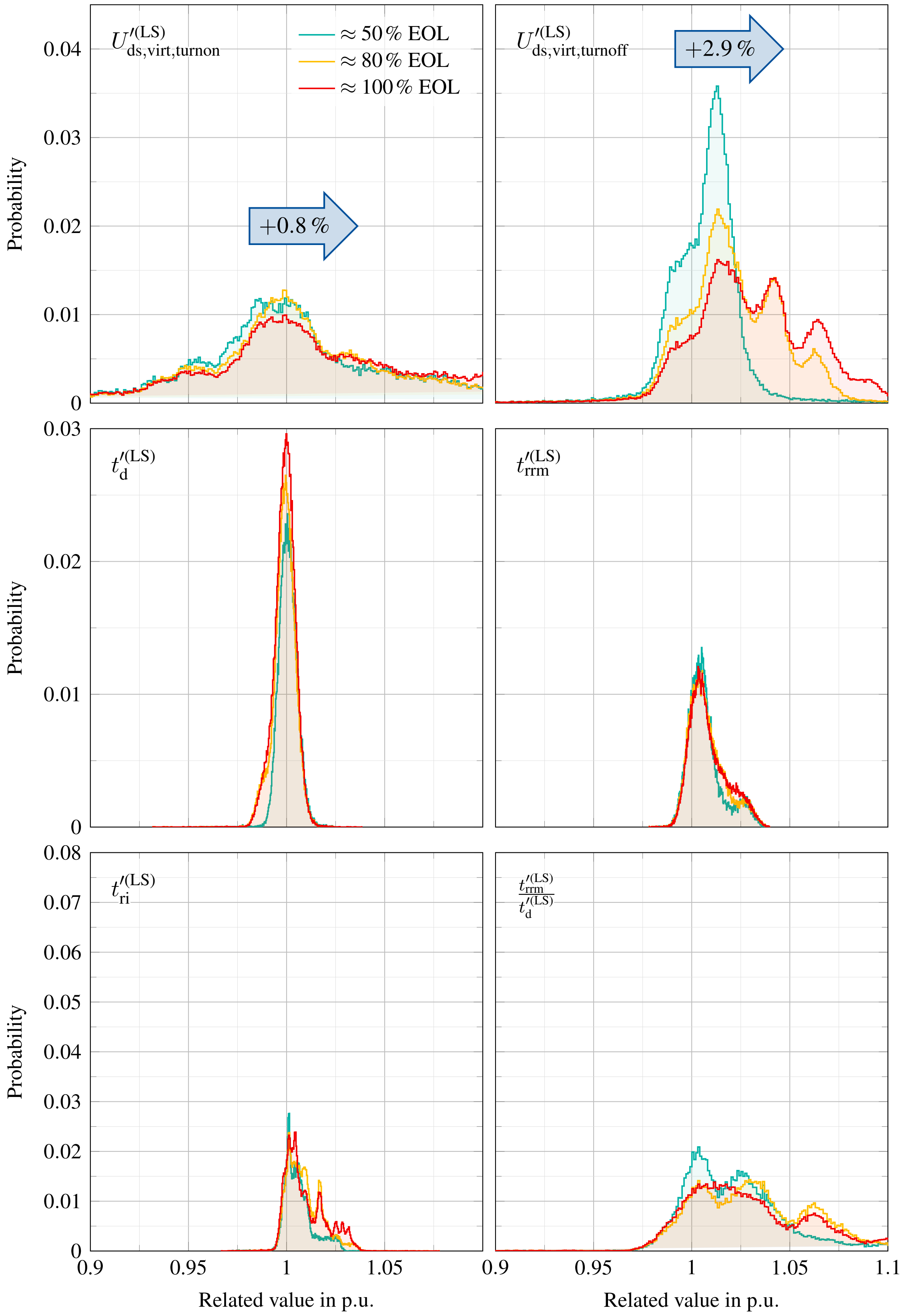

Figure 14.18: Histograms of the normalized TSEPs of the aged low-side switches depending on the approximately reached EOL during continuous PWM operation; bin width 0.1 %; for the on-state voltages $U_{ds,virt,turnon}$ and $U_{ds,virt,turnoff}$, the change in the median between the initial state and ≈100 % EOL is shown

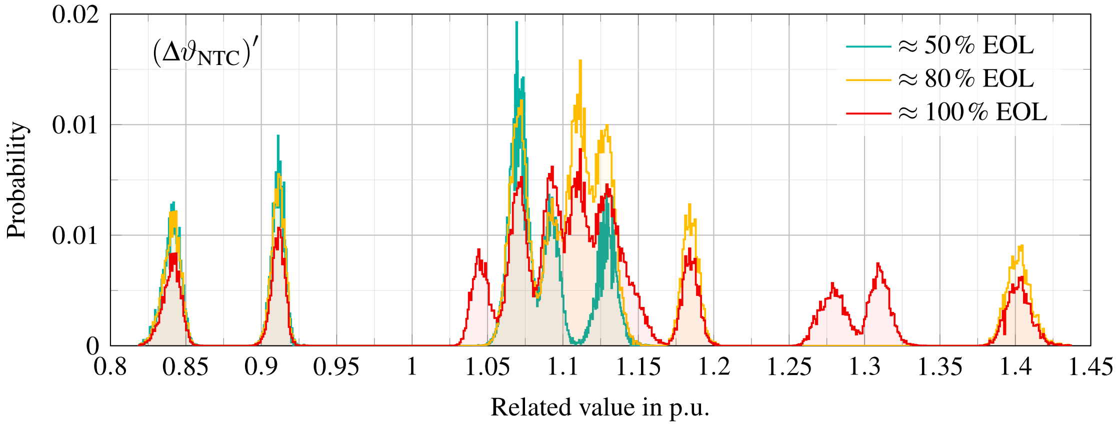

Figure 14.19: Histogram of the normalized NTC sensor temperature of all PWM measurements united; the varying positions of the peaks indicate changes in the thermal resistance between the case and the heat sink

14.4.2.2 Conclusion

The TSEP measurement system was used to monitor fourteen switches during accelerated aging tests by measuring their behavior at three different stages of aging. The TSEP analysis consists of measurements performed in double-pulse experiments and in continuous PWM operation under load.

In the double-pulse experiments, the aging could be clearly identified in the measured on-state voltages. As expected, no change in the switching time was observed, as no significant self heating occurs during double-pulse experiments.

In continuous PWM operation, the TSEP measurements become less precise. Even though the thermal connection between the modules and the cooler was as controlled as possible, large variances in the thermal resistance due to changing mounting pressure[4] and state of the TIM layer were observed. A change in the measured switching times was expected in continuous PWM operation. Given the changing mounting conditions, the high noise levels of these measurements and the limited number of TSEP analyzes, a trend could not be identified in the switching times in continuous PWM operation. Still, the degradation-dependent increase in the on-state voltage could be identified in double-pulse experiments and in continuous PWM operation.

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[4] The module cannot be mounted with a controlled torque on the mounting screws, but instead uses a built-in spring-tab mechanism, Figure 14.2, that may not be designed for the repeated remounting occuring during the aging tests.

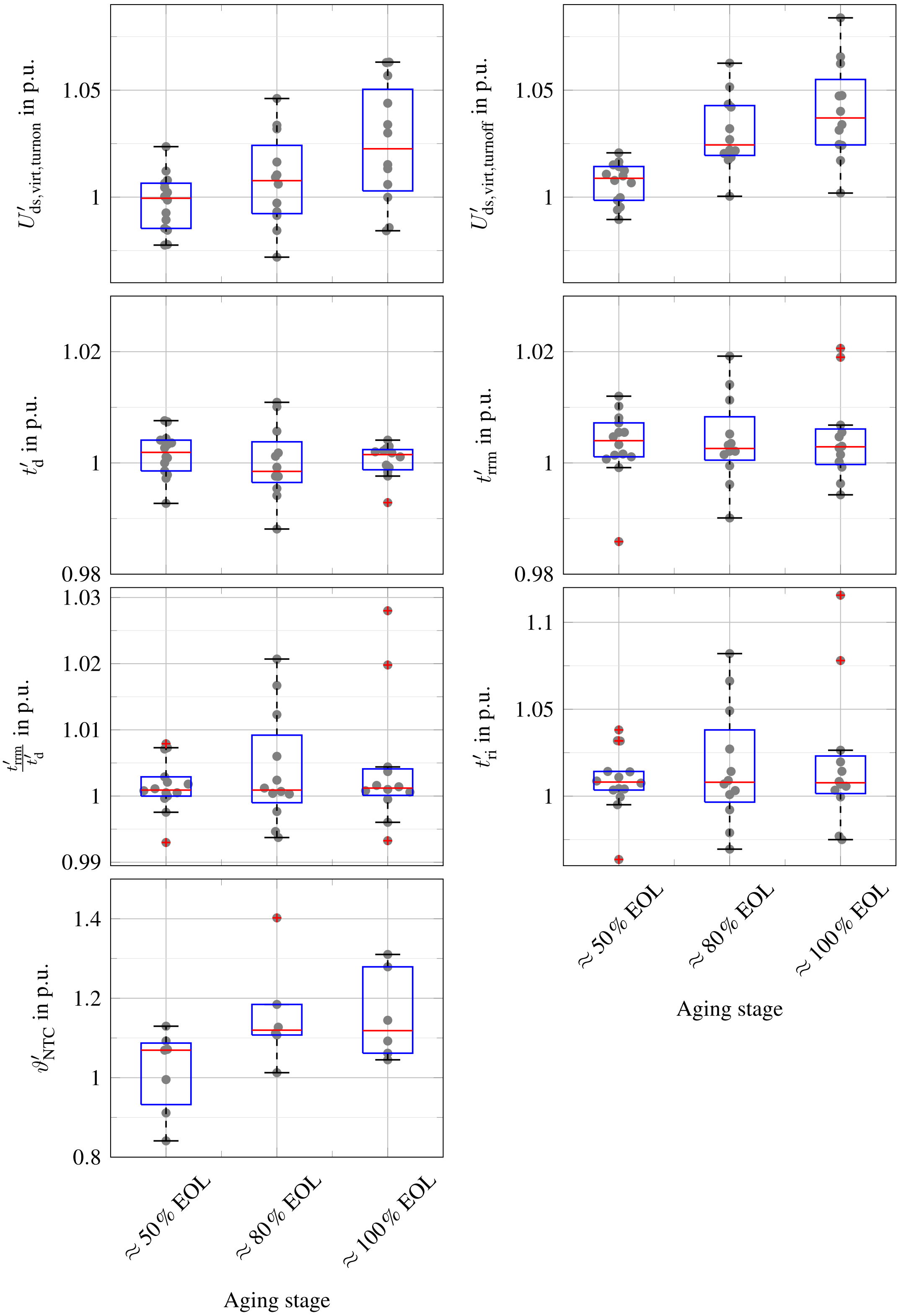

Figure 14.20: Boxplots of the normalized TSEPs of the aged switches depending on the approximately reached EOL during continuous PWM operation; based on the median change of each switch individually (gray dots);

15 Current rise time at unequal junction temperatures

In Chapter 9, the measurable time t_{rrm} until the peak of the reverse recovery current is reached, and also the turn-on delay time t_{d}, were modeled. The TSEP measurement system can only measure the time until the overcurrent peak is reached. As a result, the measured time also depends on the body diode behavior of the partner switch, and therefore its temperature. Double-pulse experiments are usually conducted on a hot plate with a known temperature. The junction temperature is assumed to be equal to the hot plate temperature. Both switches have the same temperature, which is not true during continuous PWM operation.

In this chapter, a test setup will be presented for the investigation of TSEPs in double-pulse experiments with a temperature difference between the high-side and low-side switches. The measurement procedure will be explained and the calibration data assessed. The aim is to determine the deviation of the current rise time $t_{\mathrm{ri}} = t_{\mathrm{rrm}} - t_{\mathrm{d}}$ caused by the temperature difference between the switches when using TSEP calibration data gathered only at homogeneous temperatures and applying these to continuous PWM operation without regard to the temperature difference between the switches.

Test hardware The test setup is similar to a hot plate that is split between the low-side and high-side switches. The two sides can be independently heated with resistors or cooled with fans. The setup is shown in Figure 15.1. The chip locations in the module are marked in Figure 10.6. The TSEP measurement PCB will be mounted on top of the hot plates, holding the module in place. It should be noted that this setup is only possible here because all high-side and all low-side chips in the module are located on different sides of the DCB substrate. The high-side and low-side chips of the IGBT module discussed in Part II are placed in a checkered pattern, making this approach impractical for them.

The module is placed symmetrically over the gap with regard to the chip locations[1]. The two hot plates are controlled at different temperatures. The module DCB acts as a thermal bridge between the two hot plates. A thermal power flow occurs across the module, reducing the temperature difference, see Figure 15.2. The challenging aspect of this setup is the determination of the junction temperature references. Due to the thermal power P flowing across the module, the junction temperature of the chips cannot be assumed to match the hot plate temperatures anymore.

Experimental procedure The experimental procedure will take advantage of the slow thermal time constant compared to the duration of double-pulse experiments. A schematic of the setup is shown in Figure 15.3. It will switch between two states. First, the high dc-link voltage U_{dc} will be applied as usual to the DUT and double-pulse experiments will be conducted. Second, the dc-link voltage source will be turned off and a small voltage source

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[1] The chips are not located symmetrically in the module.

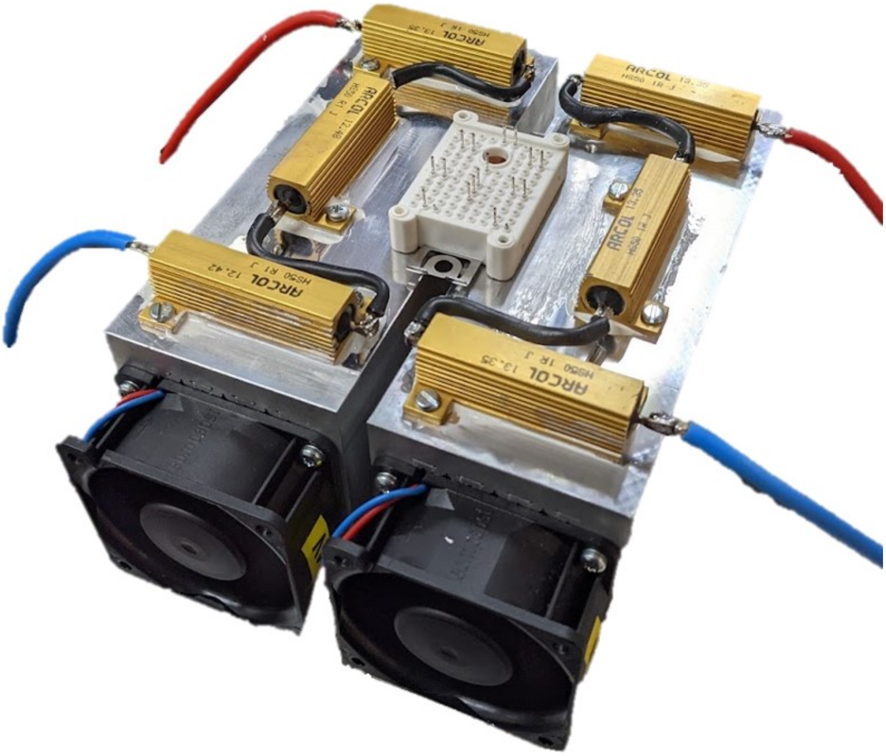

Figure 15.1: Photo of the test setup for calibrating TSEPs with a temperature difference between high side and low side

with a current regulator is used to inject a defined current I_{meas} through the body diodes of the SiC MOSFETs. The setup is shown in Figure 15.3.

The IGBT Primepack module used in Part II is used as an auxiliary switch, as it is available and has short-circuit protection. During the double-pulse phase, the setup continuously cycles through the desired operating points. A temperature measurement via the body diodes is acquired intermittently every 10 s, as the temperature changes slowly in this setup[2]. The junction temperature in between the measurements is interpolated linearly.

The MOSFET gate drivers are not turned off during the temperature measurement. The negative MOSFET gate driver voltage $U_{\text{dr,off}} = -5\,\text{V}$ is still applied. This impacts the body diode's voltage during the temperature measurement phase, as the channel is not completely closed above $U_{\text{dr,off}} \approx -7\,\text{V}$ for the given device [140]. Therefore, the body diode's forward voltages at the low measurement current I_{meas} are recalibrated analogous to Chapter 12 with the negative gate driver voltage applied. During the temperature measurement phase of the procedure, the TSEP measurement system is used to acquire the body diode's forward voltage.

The second half-bridge of the original full-bridge setup, presented in Chapter 10, was removed, as the measurement current I_{meas} would otherwise flow through both half-bridges in parallel. Furthermore, a diode was added to the load inductance to block this path for the measurement current.

The heating and cooling of the split hot plate are controlled manually. Ultimately, the entire procedure is completed twice, once with the load inductance parallel to the low-side

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[2] The maximum heating power is 150 W.

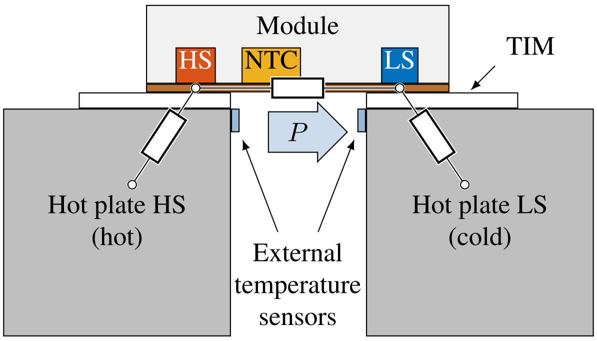


Figure 15.2: Illustration of the thermal model; in this example, the high-side hot plate is hotter than the low-side hot plate; a thermal power flow across the module's baseplate causes the junction temperatures to differ from the hot plate temperatures

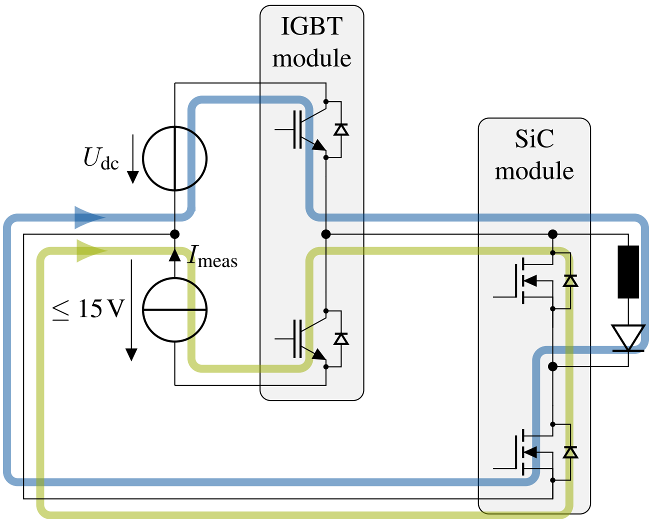


Figure 15.3: Schematic of the test setup; double-pulse current path in blue; measurement current path in green; for the high side (HS) calibration, the inductance must be relocated; the IGBT module driver has short-circuit protection

switch and once with it parallel to the high-side switch.

The recorded temperatures of the high-side and low-side switches during the measurements are shown in Figure 15.4. The expected range of the junction temperatures during continuous PWM operation is marked by a blue square for an intact module. This range is based on the temperature predicted by the thermal model used in Figure 12.18. The range is also extended to illustrate the expected temperature range for an increase in thermal resistance of up to 20 %. The measurements cover the range of interest well.

Data analysis TSEP calibration data is obtained in double-pulse experiments for a variety of load currents, high-side temperatures and low-side temperatures. The aim of the investigation is to distinguish the changes in the current rise time t_{ri} that can be attributed to changes in the MOSFET temperature ϑ_{MOS} or changes in the temperature of the body diode in the partner switch ϑ_{D}.

From the calibration data set, the data points where the MOSFET temperature ϑ_{MOS} is constant and the switched current is within set limits are selected. Thus, changes in the se-

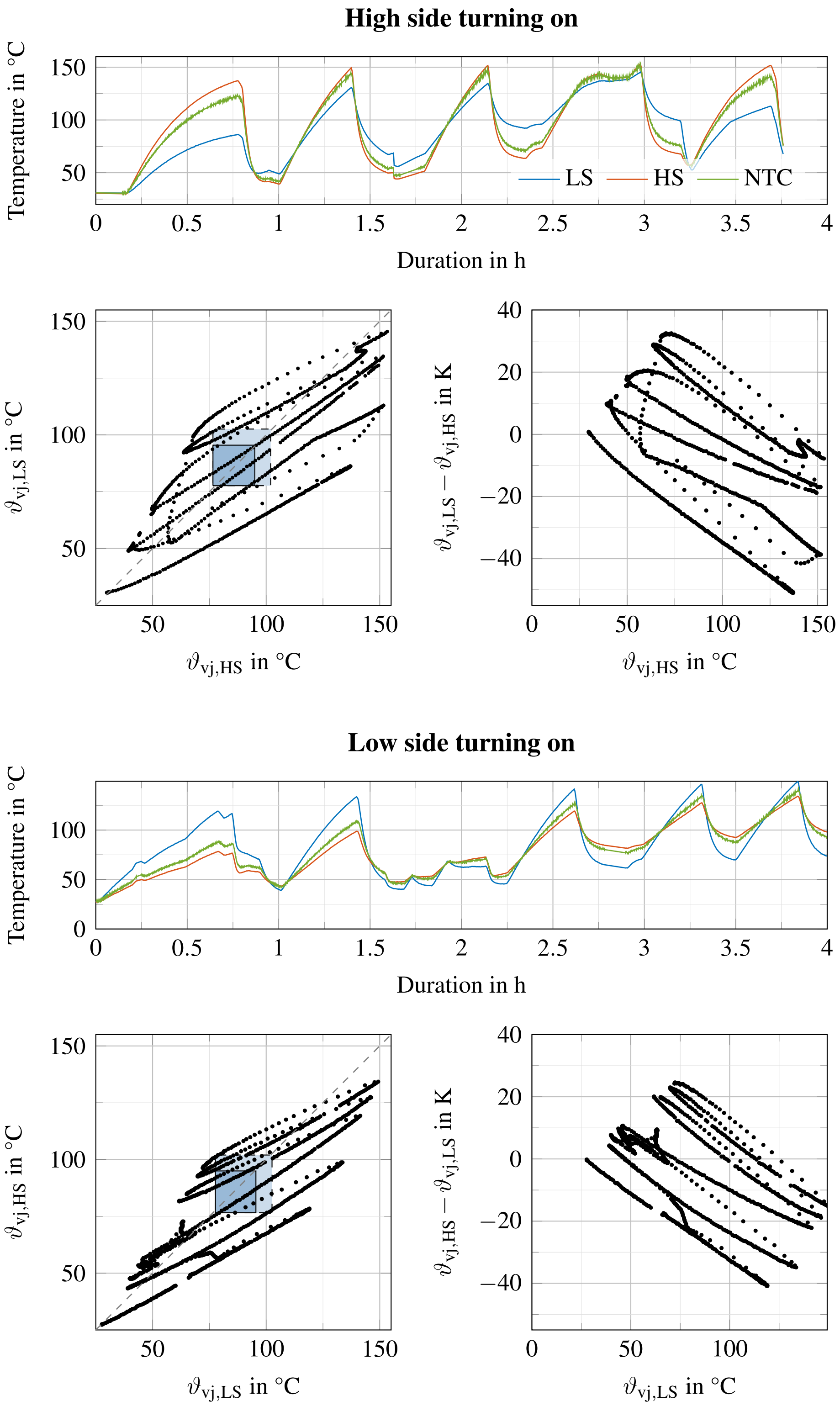
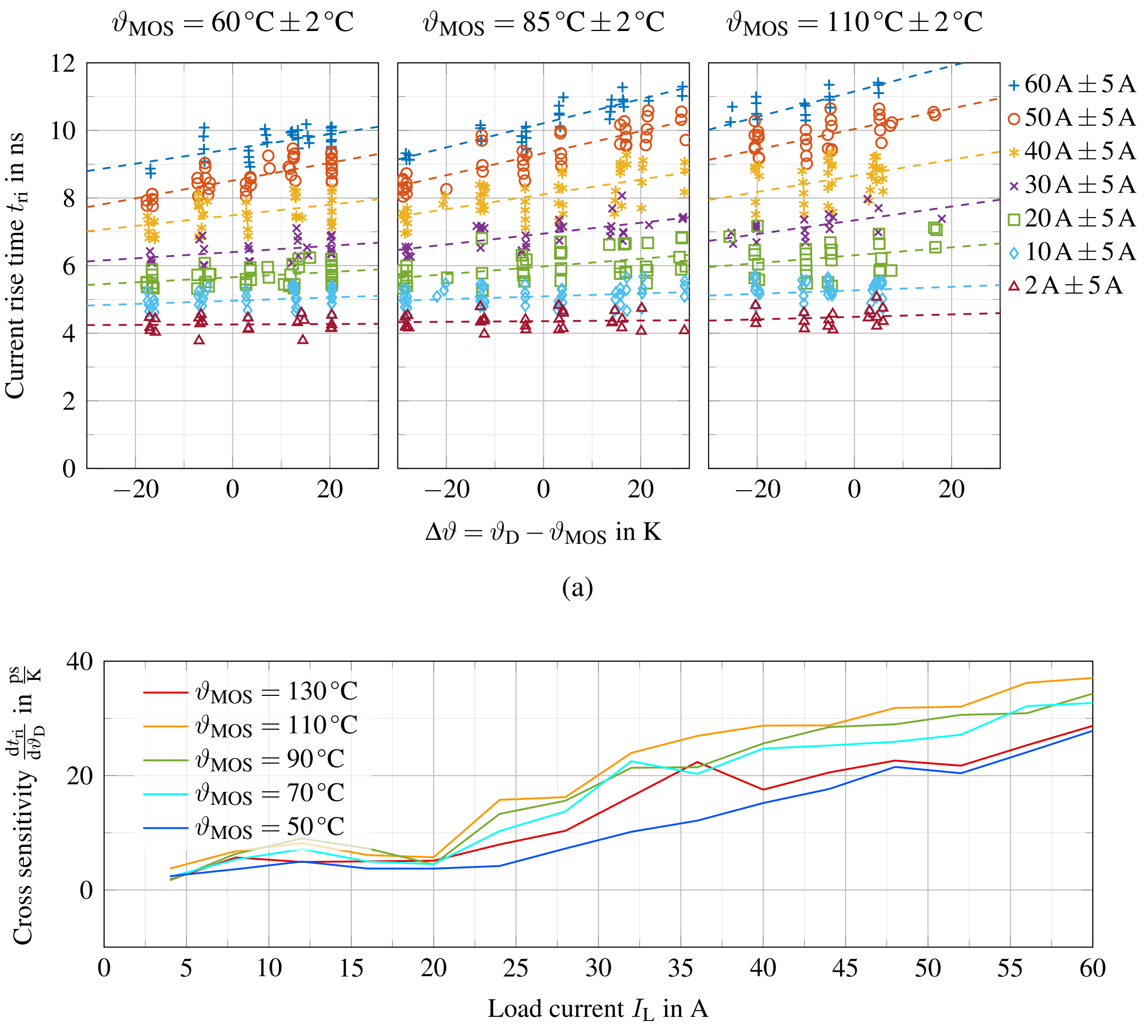


Figure 15.4: Recorded temperatures of the high-side and low-side switches; the three top graphs show double-pulse measurements of the high-side switch being calibrated; the three bottom graphs show the low-side switch being calibrated; expected temperature ranges during continuous PWM operation are shown as blue squares; high-side measurement interrupted at 1.6 h overnight; a temperature measurement was recorded approximately every 10 s; in between, double-pulse experiments were conducted every 0.5 s

lected current rise time measurements should only be caused by changes in the body diode temperature ϑ_{D}. Figure 15.5a shows the measured current rise time t_{ri} with varying body diode temperature. The current ranges are designed to include all samples, i.e., the currents are selected in 10 A steps with a ±5 A inclusion range, which makes the plotted data seemingly noisy. It is assumed that the current rise time sensitivity can be approximated linearly within the inclusion range. Consequently, variations in the current rise time due to differences in the switched load current I_{L} should balance each other out in the first-degree polynomial fit if the number of samples is sufficiently high. The estimated sensitivity of the current rise time towards changes in the body diode $\frac{\mathrm{d}t_{\mathrm{ri}}}{\mathrm{d}\vartheta_{\mathrm{D}}}$ is shown in Figure 15.5b with a finer current resolution. A positive sensitivity towards the body temperature can be observed, especially at high currents. This is expected, as the bipolar carrier density in the body diode increases with current and temperature. The plateau at lower currents is likely caused by the



(a)

(b)

Figure 15.5: (a) changes in the current rise time t_{ri} depending on the temperature difference between the turning-on MOSFET ϑ_{MOS} and the body diode in the partner switch ϑ_{D}; (b) sensitivity of the current rise time t_{ri} to the body diode temperature; the MOSFET temperature ϑ_{MOS} is constant, while the temperature of the body diode ϑ_{D} varies; first-degree polynomial fit shown by dashed lines

capacitive charge in C_{oss} being dominant for the current rise time at low currents.

The same analysis is repeated with the temperature ϑ_{D} of the body diode, which is held constant while the temperature ϑ_{MOS} of the MOSFET is varied. The results are plotted in Figure 15.6. The current rise time shows less sensitivity towards the temperature of the MOSFET that is turned on than to the temperature of the partner switch's body diode. The temperature sensitivity towards the MOSFET being turned on is basically neglectable compared to the dependency on the body diode.

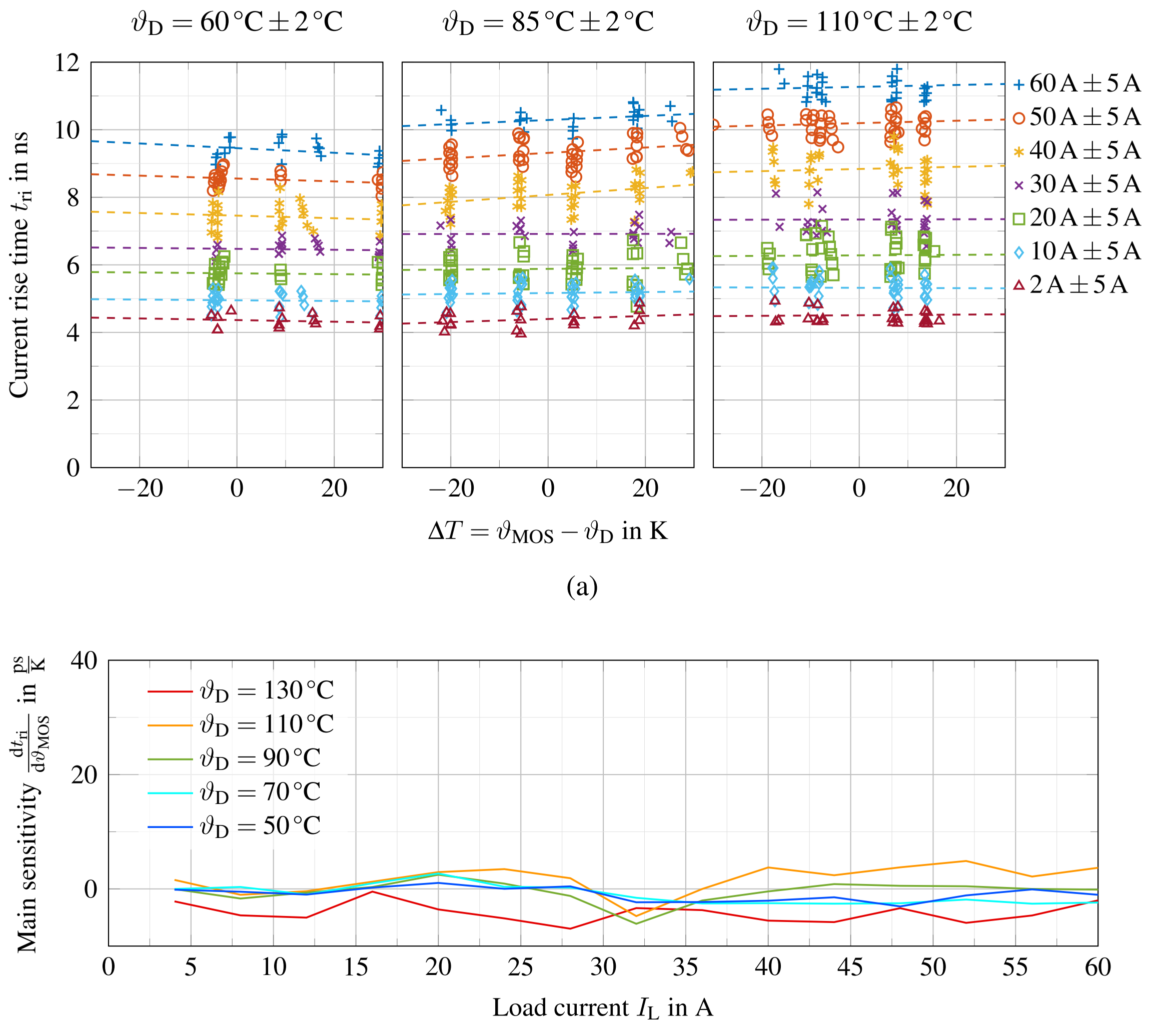


Figure 15.6: (a) changes in the current rise time t_{ri} depending on the temperature difference between the turning-on MOSFET ϑ_{MOS} and the body diode in the partner switch ϑ_{D}; (b) sensitivity of the current rise time t_{ri} to MOSFET temperature; the body diode temperature ϑ_{D} is constant, while the MOSFET temperature ϑ_{MOS} of varies; first-degree polynomial fit shown by dashed lines

As described in Chapter 9, the current rise time depends on several parameters. One reason for this low sensitivity could be the superposition of opposing temperature sensitivities. Table 15.1 provides a list of parameters, their assumed general temperature behavior and their expected impact on the current rise time. The temperature dependency of the transconductance K is determined from the transfer characteristic of the SiC chips, see Appendix F.

Table 15.1: Expected temperature sensitivity impacts

Parameter		Assumption	Expectation
Threshold voltage	U_th	$\frac{\mathrm{d}U_\mathrm{th}}{\mathrm{d}\vartheta_\mathrm{MOS}} < 0$	$\frac{\mathrm{d}t_\mathrm{ri}}{\mathrm{d}U_\mathrm{th}}\frac{\mathrm{d}U_\mathrm{th}}{\mathrm{d}\vartheta_\mathrm{MOS}} < 0$
Transconductance	K	$\frac{\mathrm{d}K}{\mathrm{d}\vartheta_\mathrm{MOS}} < 0$	$\frac{\mathrm{d}t_\mathrm{ri}}{\mathrm{d}K}\frac{\mathrm{d}K}{\mathrm{d}\vartheta_\mathrm{MOS}} > 0$
Internal gate resistance	$R_\mathrm{g,int}$	$\frac{\mathrm{d}R_\mathrm{g,int}}{\mathrm{d}\vartheta_\mathrm{MOS}} > 0$	$\frac{\mathrm{d}t_\mathrm{ri}}{\mathrm{d}R_\mathrm{g,int}}\frac{\mathrm{d}R_\mathrm{g,int}}{\mathrm{d}\vartheta_\mathrm{MOS}} > 0$
Reverse recovery charge	Q_rr	$\frac{\mathrm{d}Q_\mathrm{rr}}{\mathrm{d}\vartheta_\mathrm{D}} > 0$	$\frac{\mathrm{d}t_\mathrm{ri}}{\mathrm{d}Q_\mathrm{rr}}\frac{\mathrm{d}Q_\mathrm{rr}}{\mathrm{d}\vartheta_\mathrm{D}} > 0$
		$\frac{\mathrm{d}Q_\mathrm{rr}}{\mathrm{d}I_\mathrm{L}} > 0$	$\frac{\mathrm{d}t_\mathrm{ri}}{\mathrm{d}Q_\mathrm{rr}}\frac{\mathrm{d}Q_\mathrm{rr}}{\mathrm{d}I_\mathrm{L}} > 0$

In order to validate the results, signal waveforms of matching double-pulse experiments are shown in Figure 15.7 and Figure 15.8. Figure 15.7 shows the turn-on behavior at a fixed temperature of the MOSFET ϑ_MOS and varying temperatures of the body diode ϑ_D. All graphs are shifted such that the beginning of the current rise time t_ri matches $t = 0\,\mathrm{s}$. The turn-on process before reaching the negative peak in u_sk shows almost no change, as expected. After this, the changing reverse recovery behavior of the body diode affects the measured current rise time t_ri until the zero crossing in u_sk occurs.

Figure 15.8 depicts the results with a fixed body diode temperature and changes in the MOSFET temperature. All graphs are shifted such that the end of the current rise time t_ri matches $t = 0\,\mathrm{s}$. The turn-on behavior displays very little change with the MOSFET temperature before reaching the negative peak[3] in u_sk. Even during the turn-on delay, before the threshold voltage is reached, the gate voltage u_g exhibits very little change. A change due to the temperature-dependent variation of the internal gate resistance and the decreasing threshold voltage U_th was expected.

The small change in the gate voltage profile during the turn-on delay time suggests that the internal gate resistance experiences almost no change with temperature. A comprehensive investigation has to be omitted in the context of this work. An in-depth analysis is presented in [167, 168], showing that a temperature independent region of the internal gate resistor can occur in SiC at certain frequencies.

Conclusion The ideal current rise time measurement would end when the drain current of the MOSFET crosses the value of the switched load current during turn-on. The implemented measurement of the current rise time also includes the time until the overcurrent peak in the drain current is reached. Therefore, the measured current rise time t_ri is affected by the reverse recovery behavior of the body diode in the partner switch. Double-pulse experiments with unequal temperatures of the high-side and low-side switches were conducted to distinguish the changes in current rise time caused by the temperature of the MOSFET from those caused by the body diode in the partner switch. It was expected that both temperatures would impact the current rise time and that the current rise time could be modeled as depending on a weighted average of both temperatures.

Instead, the data has shown that the temperature dependency of the measured current

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[3] The peak should approximately correspond to the point where the MOSFET is conducting the entire load current

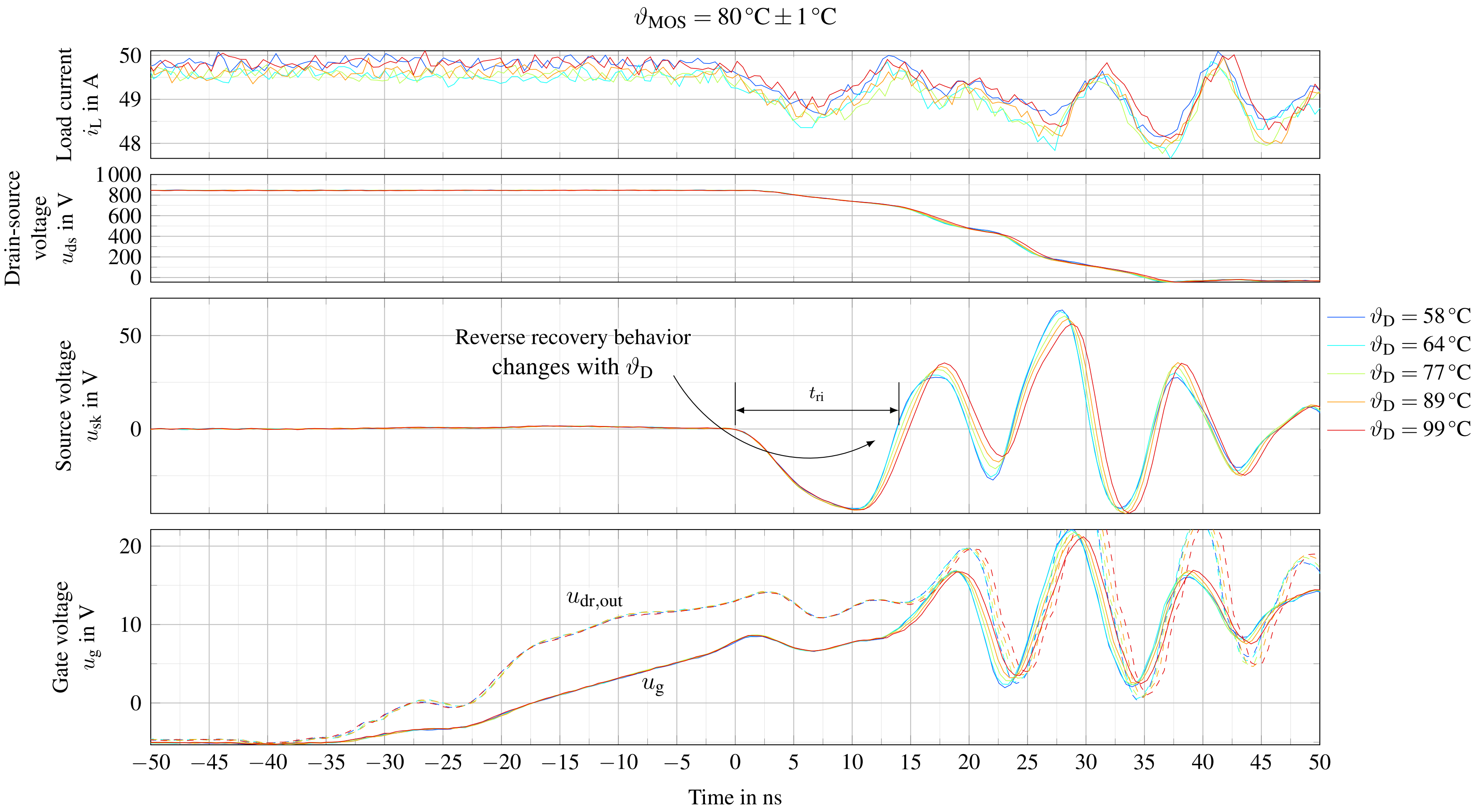

Figure 15.7: Changes in the voltage spike induced between the Kelvin source and source contact of the module u_{sk} at varying body diode temperature ϑ_D only; load current i_L is shown only to compare the switched currents; gate driver output voltage $u_{dr,out}$ according to Figure 10.7

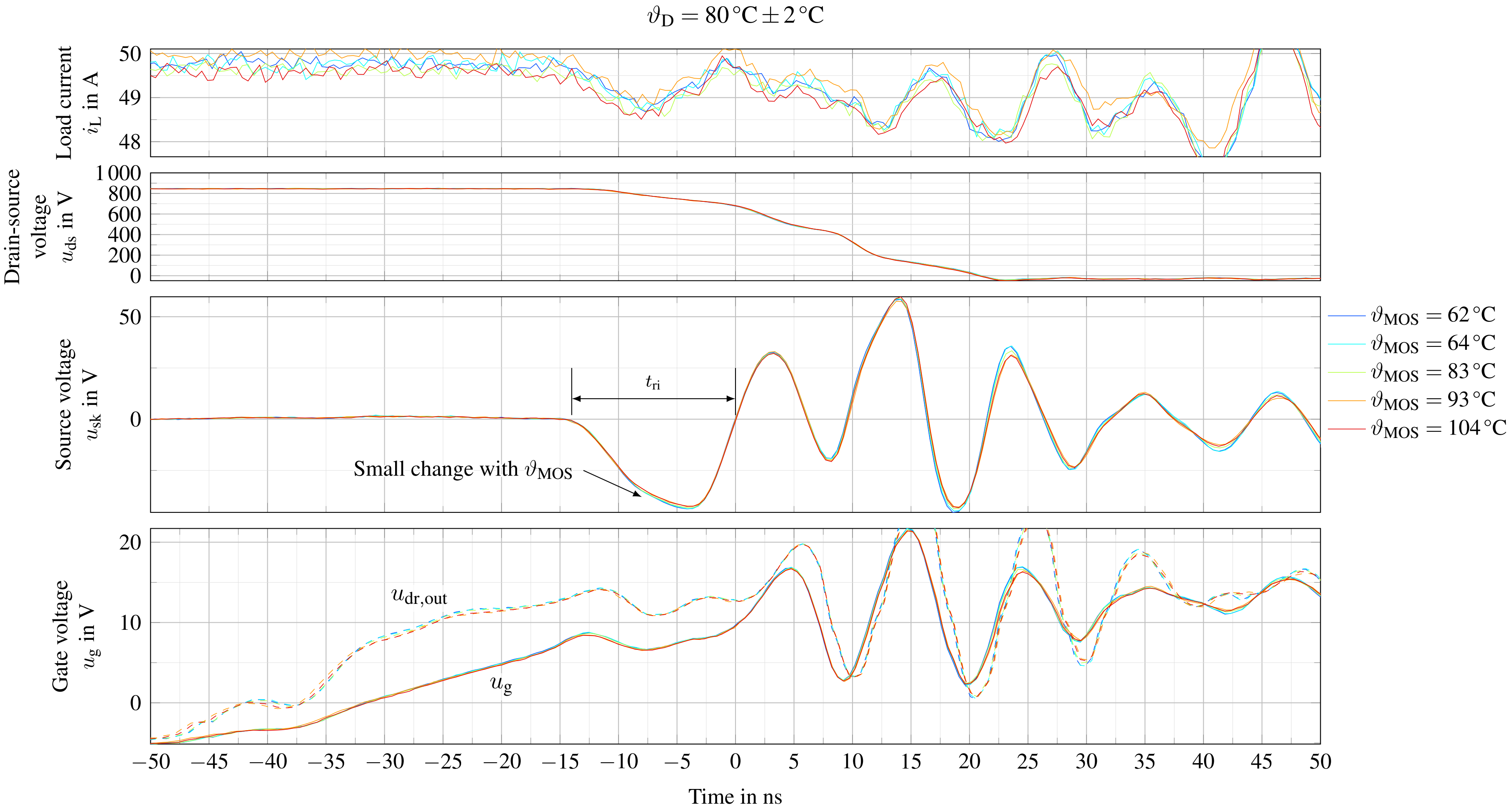

Figure 15.8: Changes in the voltage spike induced between the Kelvin source and source contact of the module u_{sk} at varying MOSFET temperature ϑ_{MOS} only; load current i_{L} is shown only to compare the switched currents; gate driver output voltage $u_{\mathrm{dr,out}}$ according to Figure 10.7

rise time t_{ri} is almost entirely caused by the changes in the body diode's reverse recovery behavior. The MOSFET temperature has a neglectable effect and no weighting is necessary. As a consequence, the measured current rise time can be used directly for a TSEP-based temperature of the partner switch instead of the MOSFET turning on.

16 Outlook

In this thesis, the application of TSEPs to fast-switching wide-bandgap MOSFET devices was investigated, giving special consideration to parasitic impacts. Although many aspects of a successful application of TSEPs to the estimation of the virtual junction temperature or degradation detection have been discussed, numerous improvements and further extensions are possible.

Tracking filters TSEPs in the context of a condition-monitoring system were shown in Figure 1.1. Excluded in this thesis was the design of a tracking filter, e.g., an extended Kalman filter. The addition of an extended Kalman filter would allow the measured TSEPs to be merged with a thermal model.

The predictor-corrector model of the Kalman filter is not limited to correction using a single measurement. Rather, it offers an elegant way to merge all measured TSEPs.

The covariance matrix used in the predictor-corrector steps of the Kalman filter allows the consideration of accuracy differences between different TSEPs, and changing accuracy at different load current levels.

Furthermore, the identified sensitivities of the TSEPs towards discontinuous parasitic effects, e.g., duty-cycle-dependent variations in the gate driver voltages, may be used to determine covariances between the TSEPs. As an example, the dependency of all TSEPs on the positive gate driver voltage $\frac{\partial t_{\mathrm{d}}}{\partial U_{\mathrm{dr,on}}}$, $\frac{\partial t_{\mathrm{rrm}}}{\partial U_{\mathrm{dr,on}}}$, $\frac{\partial U_{\mathrm{ds,virt,turnon}}}{\partial U_{\mathrm{dr,on}}}$ and $\frac{\partial U_{\mathrm{ds,virt,turnoff}}}{\partial U_{\mathrm{dr,on}}}$ could be determined and multiplied by the expected variation in the gate driver voltage $\Delta U_{\mathrm{dr,on}}$ in order to fill the covariance matrix. This approach may allow the elimination of several fast-changing parasitic impacts during the predictor-corrector step that would otherwise be difficult to determine with a disturbance estimation.

Current model improvement The extended current model presented in Chapter 11 only incorporates a well-known load voltage. The current model could be further extended by using a sinusoidal load voltage, and the impact of the estimation errors of the phase and the amplitude of the load voltage on the TSEP-based temperature estimation could be investigated. This effect is of special interest for machine loads due to the saturation dependency of the induced voltage or additional harmonics.

Using the measured switching times for switching-loss estimation The measured on-state voltage is used as an on-line measurement to determine the conduction losses directly. The measured switching times may be used to improve the estimation of the switching losses in the loss model.

Transition to a three-phase load The extended current model already consists of a variety of compensation cases, depending on the duty cycle of each half-bridge and the direction of the load current. Similarly, the compensated slope of the on-state voltage after turn-on depends on the switching state of the other half-bridge, see Section 10.5.

Moving to a three-phase load, the current model and on-state voltage slope compensation must be extended to use more cases.

Hardware reduction Switching-time measurements use the voltage spike induced across the power module's parasitic inductances due to the high current slopes $\frac{\mathrm{d}i_\mathrm{d}}{\mathrm{d}t}$ occurring during switching. The corresponding commutation current loop passes through the high-side switch, the low-side switch and closes through the dc-link capacitor. High-voltage spikes occur across any parasitic inductance within the commutation loop. Thus, switching time measurements can also be acquired at the dc-link capacitor, as shown in Figure 16.1. The commutation loops of all connected switches pass through the dc-link capacitor. Therefore, a single switching time measurement located there could be used to acquire switching time measurements for all switches connected to the same dc-link.

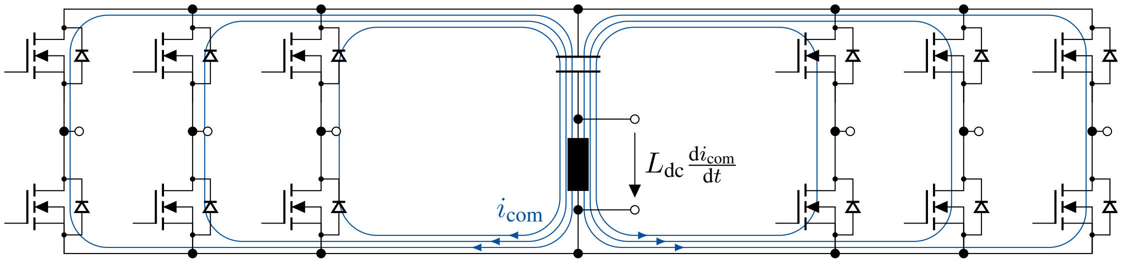

Figure 16.1: Commutation loops of all switches passing through the dc-link capacitor and its parasitic inductance

A measurement of the turn-on delay time t_d or the time t_rrm until the peak of the reverse recovery current occurs could only be performed at this location if a start signal, i.e., the corresponding switching signal, is provided to the central switching time measurement. Alternatively, the current rise time t_ri can be acquired without any other signal needing to be routed to the central measurement location, as the beginning and end of the current rise time are marked by a positive and negative voltage spike across the parasitic inductance. If the parasitic inductances available near the dc-link capacitor are too small, a Rogowski coil can be used for signal acquisition.

The current rise time of a switch can only be measured if no other device is switching simultaneously. Therefore, the measurement of all switches in each period may not always be possible. Considering the very small duration of a switching event compared to the duration of the PWM period, a very high probability that a measurement is possible can be expected, even if numerous switches are connected to a single dc-link.

If no external signals are provided to the central measurement location, the current rise time measurement of the switches may show large variations due to fluctuations in the supply voltages of each gate driver. Nevertheless, this setup would lead to greatly reduced hardware complexity and could be coupled with statistical evaluation approaches, as explained in Section 3.3, or the measurements could be used as a feedback signal for a temperature observer model including the available NTC sensors.

Hysteresis impact The investigation into the impact of the threshold voltage hysteresis on the measured switching times was inconclusive with regard to the specific gate voltage levels, current levels and gate resistor sizes used in this thesis. The impact of the threshold voltage hysteresis was found to be relevant in [142] for small positive gate driver voltages, but irrelevant for large positive gate driver voltages, compared to the gate driver voltage used here. Most investigations of the threshold voltage hysteresis focus on currents relevant for subthreshold conduction, not for typical currents during operation. As the relaxation time of the threshold voltage hysteresis is inversely proportional to the current [120], the effects may not be as relevant in nominal inverter operation. Further investigations are needed using nominal gate driver voltages, nominal external gate resistors and nominal current levels.

Using more precise TDCs The results shown in this thesis revealed that the noise level of the switching times was too high to allow an accurate temperature estimation using the switching times. The time-to-digital converter (TDC) used has a relatively coarse time resolution and accuracy compared to more expensive TDCs from LIDAR applications. Using more accurate TDCs may improve the suitability of switching times as TSEPs.

TDC front-end integration The front end developed for the TDC uses a bipolar junction transistor (BJT) to generate the input trigger signal. The base-emitter path of the BJT allows a current to flow through the analog front end if a voltage spike occurs across the parasitic inductance of the power module. Using a front end that has a current-controlled input, rather than using a (voltage-controlled) MOSFET as the input, allows the insertion of a simple base resistor across which the entire voltage spike of the power module can drop, thereby protecting the subsequent circuitry with a simple measure.

Unfortunately, current-controlled inputs are rare, especially in TDCs. Integrating the analog front end into the input stage of a TDC may increase the stability and EMI tolerance of the time measurements.

Expansion of the data set The TSEP results acquired during the power-cycling tests showed that the high noise level of the TSEPs makes statistical methods a preferred tool for the assessment TSEP data. With today’s technologies, an uplink from the inverter to a centralized computing and storage system is imaginable. In applications where a large number of similar inverters are deployed, i.e., in electric mobility, renewable energy or standardized machines for industrial applications, large sets of data could be gathered centrally. Moving to a centralized TSEP evaluation system with the data from numerous inverters may improve the distinction between irrelevant trends in the TSEPs and failure-predicting trends.

Upstreaming TSEP measurements at the switching frequency is not feasible. Thus, reducing the amount of data that is sent to the central computing unit could be essential, e.g., by determining frequency components of the TSEPs.

Model assessment using second-level inference In this thesis, numerous model variants for fitting TSEP calibration data were generated, as explained in Part III, and their suitability to describe TSEPs was assessed by fitting the models to measured data sets. Additionally, Bayesian regularization was employed to find the most appropriate fit during the training of ANNs, see Section 4.2.1.1. Using Bayesian regularization during training corresponds to *first-level inference* [93], i.e., determining the most likely fit for a given fit function. *Second-level inference*, in contrast, is the determination of the most likely model to describe a data set [93]. This concept could be used to further assess and quantify which model components are needed to model TSEP behavior without overfitting.

Synergies

Multi-use sensors The hardware used in the voltage limiter of the ADC front end matches the hardware needed to detect humidity-based degradation of power modules [169]. Only minuscule extensions are required to use the same hardware to detect thermomechanical and humidity-based degradation mechanisms, creating a multi-use sensor.

Oversampled current models The extended current model demonstrates the large effort needed to estimate the instantaneous current during turn-on from a single current sensor sample. Coupling TSEP-based thermal monitoring or degradation detection systems with other systems that have a current signal with a high time resolution would greatly reduce the complexity of the system, while simultaneously improving the accuracy. An example of such a synergy is sensorless motor controls based on current oversampling [154].

17 Conclusion

This thesis investigated the applicability of TSEPs to fast-switching SiC MOSFET devices. The key focus was on the design of TSEP measurement hardware and the identification of parasitic impacts on the TSEP measurement. This included disturbances caused by the gate driver, the power module packaging itself and the current ripple in continuous PWM operation. A TSEP measurement system was designed to detect the progress of thermomechanical degradation mechanisms.

The sizes of the parasitic impacts were quantified using commercial modules and gate drivers. It was shown that the positive gate driver voltage has a large impact on most of the TSEP measurements considered and that gate driver voltage stabilization is required to employ TSEP-based temperature estimations. The power modules investigated use press-fit technology. Therefore, the temperature of the gate driver circuitry has a good thermal coupling to the power module baseplate or DCB. Heat soaking to the gate driver IC through the pins and the PCB increases the driver's temperature. It was demonstrated that this can lead to a temperature-dependent variation in the internal gate driver resistance, having a relevant impact on the switching times.

A combination concept using multiple TSEPs acquired in close succession was introduced. The chosen TSEPs were the turn-on delay time, the time until the peak of the reverse recovery current was reached, the on-state voltage of one switch shortly after turn-on and the on-state voltage of the partner switch shortly before its turn-off. The combination of these TSEPs allows the elimination or reduction of parasitic impacts. Simple methods for preprocessing to reduce the effects of parasitic impacts were demonstrated, e.g., using the ratio of multiple switching times during one turn-on process instead of the switching times themselves significantly reduces the impact of the gate driver voltage variations on the TSEP measurements. All methods developed in this thesis can be applied before the TSEP measurements are used in subsequent tracking filters. They do not substitute for tracking filters, but rather offer an additional input processing to reduce the impact of fast-changing disturbances.

Artificial neural networks (ANNs) were used to determine the virtual junction temperature of the devices, combining the four measured TSEPs with data from the inverter's current and voltage sensors. ANNs provided a more accurate temperature estimation than physics-based approaches, although it was shown that approximately 360 to 600 calibration points are required to train an appropriate ANN. One of the key benefits of ANNs in the context of this thesis was the tools already available in ANN training frameworks to cope with the nonlinear behavior of the TSEPs and the associated local minima during training.

A variety of detailed models of the on-state voltage and switching times during turn-on were investigated, including SiC-specific effects. The accuracy of the model was evaluated with fit data from 18 SiC MOSFET switches of the same type. It was determined which level of model complexity is needed to reproduce the temperature-dependent and current-dependent behavior of the on-state voltage and the switching times during turn-on.

For modeling the on-state voltage, a MOS channel contribution, a JFET channel contribution, and the contribution of an epitaxial drift region are necessary to accurately reproduce the temperature and current behavior. It could be demonstrated that the nonlinearities of the inversion layer charge in the MOS channel need to be considered in order to separate the small temperature-dependent changes in the on-state voltage from the current-dependent effects.

The measured switching times did not have an accuracy good enough to justify the use of any model of a higher complexity than linear. The analytical models of the switching times displayed a possible impact of the threshold voltage hysteresis on the switching times. Furthermore, it was demonstrated that the drain-current-induced magnetic feedback to the gate loop has a more significant impact on the switching times than changes in the device's junction temperature. Consequently, the transfer of TSEP calibration data, even between different power module models of the same type, is impossible due to the changing magnetic coupling.

Beside the theoretical investigations, TSEP measurement hardware was designed for SiC MOSFETs. Analog front ends for measuring the on-state voltage and the fast-switching times of SiC MOSFETs were developed. Design aspects specific to the application to fast-switching wide-bandgap semiconductors were discussed. Concepts to handle the large oscillations of the commutation loop after turn-on, and to compensate the slope of the on-state voltage due to the switching state of the other half-bridge or the load voltage, were presented.

One of the TSEPs, the turn-on time until the peak of the reverse recovery current is reached, depends on the temperature of both switches, due to the reverse recovery current of the partner switch's body diode. In double-pulse experiments with a controlled temperature difference between the high-side and low-side switches, the temperature dependency of this TSEP was separated into the temperature dependency of the MOSFET turning on and the temperature of the partner switch's body diode. The investigation showed that this TSEP almost entirely depends on the temperature of the body diode involved and very little on the temperature of the turning-on MOSFET. Therefore, this TSEP can easily be used as a temperature reference for the partner switch instead of the turning-on MOSFET.

During PWM inverter operation, only a single scalar current sample is available per PWM period. An extended current model was developed, allowing the estimation of the instantaneous current at the turn-on of the SiC MOSFETs. This adaptation is required, as the chosen TSEPs show a strong cross-dependency on the load current, resulting in a large temperature estimation error otherwise. The test setup given exhibited a carrier shift between the half-bridges of 0.35 % of the PWM period. It was shown that even this small carrier shift would lead to a temperature estimation error of several kelvin.

A thermal impedance model of the power module and test setup was created. It included the cross coupling between the topological switches. The thermal impedance model is coupled with a loss model to provide a temperature reference for the virtual junction temperature, which can be used to compare the TSEP-based estimations against.

Degradation of the chip solder was emulated by increasing the thickness of the thermal interface material between the module and the cooler. This leads to an increase in the module's thermal resistance to ambient by 14 %, reproducing a severely degraded solder layer, even though this is not yet considered defective. It was validated that the TSEP measurement system was capable of clearly detecting the resulting increase in the virtual junction temperature of 4 K in continuous PWM operation. Therefore, the TSEP measurement system is also able to detect solder degradation during regular inverter operation before the device reaches a critical state of degradation.

In addition to the investigations using emulated degradation, power-cycling tests were conducted with seven power modules to generate more realistic thermomechanical degradation effects. The power-cycling tests were halted periodically and the modules analyzed using the TSEP measurement system in double-pulse experiments and in continuous PWM operation. Changes in the switching times were not clearly identifiable due to the high noise level. The expected increase in the on-state voltage could be identified in both modes of operation.

Overall, this thesis gave an insight into external impact factors on TSEP measurements, the required level of model detail to separate temperature-dependent behavior of a TSEP from its current-dependent behavior, and the resulting high complexity of a TSEP-based virtual junction temperature estimation for SiC MOSFETs in continuous PWM operation.

A Regression function performance for IGBTs

n_{par}	Fit function	RMSD training data	RMSD validation data
4	$a_1 + a_2 \cdot \vartheta_{\mathrm{vj}} + \left(a_3 + a_4 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}}$	30.26	29.06
4	$a_1 + \left(a_2 + a_3 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + a_4 \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	13.24	21.07
4	$a_1 + a_2 \cdot \vartheta_{\mathrm{vj}} + a_3 \cdot I_{\mathrm{c}} + a_4 \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	43.96	57.46
5	$a_1 + a_2 \cdot \vartheta_{\mathrm{vj}} + a_3 \cdot I_{\mathrm{c}} + \left(a_4 + a_5 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	14.86	18.08
5	$a_1 + a_2 \cdot \vartheta_{\mathrm{vj}} + \left(a_3 + a_4 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + a_5 \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	6.67	10.39
5	$a_1 + \left(a_2 + a_3 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + \left(a_4 + a_5 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	7.15	12.26
6	$a_1 + a_2 \cdot \vartheta_{\mathrm{vj}} + \left(a_3 + a_4 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + \left(a_5 + a_6 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	6.34	8.03
7	$a_1 + a_2 \cdot \vartheta_{\mathrm{vj}} + a_3 \cdot \vartheta_{\mathrm{vj}}^2 + \left(a_4 + a_5 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + \left(a_6 + a_7 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	5.56	**6.45**
7	$a_1 + a_2 \cdot \vartheta_{\mathrm{vj}} + \left(a_3 + a_4 \cdot \vartheta_{\mathrm{vj}} + a_5 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot I_{\mathrm{c}} + \left(a_6 + a_7 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	5.15	7.01
7	$a_1 + a_2 \cdot \vartheta_{\mathrm{vj}} + \left(a_3 + a_4 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + \left(a_5 + a_6 \cdot \vartheta_{\mathrm{vj}} + a_7 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	5.43	6.58
8	$a_1 + a_2 \cdot \vartheta_{\mathrm{vj}} + a_3 \cdot \vartheta_{\mathrm{vj}}^2 + \left(a_4 + a_5 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + \left(a_6 + a_7 \cdot \vartheta_{\mathrm{vj}} + a_8 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	4.98	9.12
8	$a_1 + a_2 \cdot \vartheta_{\mathrm{vj}} + \left(a_3 + a_4 \cdot \vartheta_{\mathrm{vj}} + a_5 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot I_{\mathrm{c}} + \left(a_6 + a_7 \cdot \vartheta_{\mathrm{vj}} + a_8 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	5.12	7.33
8	$a_1 + a_2 \cdot \vartheta_{\mathrm{vj}} + a_3 \cdot \vartheta_{\mathrm{vj}}^2 + \left(a_4 + a_5 \cdot \vartheta_{\mathrm{vj}} + a_6 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot I_{\mathrm{c}} + \left(a_7 + a_8 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	5.11	7.52
9	$a_1 + a_2 \cdot \vartheta_{\mathrm{vj}} + a_3 \cdot \vartheta_{\mathrm{vj}}^2 + \left(a_4 + a_5 \cdot \vartheta_{\mathrm{vj}} + a_6 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot I_{\mathrm{c}} + \left(a_7 + a_8 \cdot \vartheta_{\mathrm{vj}} + a_9 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	4.97	9.72

Table A.1: Regression results of different regression functions for $U_{\mathrm{ce}} = f\left(I_{\mathrm{c}}, \vartheta_{\mathrm{vj}}\right)$; number of parameters n_{par}; selected fit function in bold font; extract from [89]

n_{par}	Fit function	RMSD training data	RMSD validation data
4	$b_1 + b_2 \cdot \vartheta_{\mathrm{vj}} + \left(b_3 + b_4 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}}$	27.51	45.22
4	$b_1 + \left(b_2 + b_3 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + b_4 \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	21.37	29.93
4	$b_1 + \left(b_2 + b_3 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + b_4 \cdot \sqrt{\left(I_{\mathrm{c}}/\mathrm{A}\right)}$	21.24	27.71
4	$b_1 + b_2 \cdot \vartheta_{\mathrm{vj}} + b_3 \cdot I_{\mathrm{c}} + b_4 \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	17.37	24.05
4	$b_1 + b_2 \cdot \vartheta_{\mathrm{vj}} + b_3 \cdot I_{\mathrm{c}} + b_4 \cdot \sqrt{\left(I_{\mathrm{c}}/\mathrm{A}\right)}$	16.75	22.57
5	$b_1 + b_2 \cdot \vartheta_{\mathrm{vj}} + \left(b_3 + b_4 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + b_5 \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	5.12	7.68
5	$b_1 + b_2 \cdot \vartheta_{\mathrm{vj}} + \left(b_3 + b_4 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + b_5 \cdot \sqrt{\left(I_{\mathrm{c}}/\mathrm{A}\right)}$	3.81	5.25
5	$b_1 + b_2 \cdot \vartheta_{\mathrm{vj}} + b_3 \cdot I_{\mathrm{c}} + \left(b_4 + b_5 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	4.35	12.83
5	$b_1 + b_2 \cdot \vartheta_{\mathrm{vj}} + b_3 \cdot I_{\mathrm{c}} + \left(b_4 + b_5 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \sqrt{\left(I_{\mathrm{c}}/\mathrm{A}\right)}$	3.34	3.94
5	$b_1 + \left(b_2 + b_3 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + \left(b_4 + b_5 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	6.23	10.53
5	$b_1 + \left(b_2 + b_3 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + \left(b_4 + b_5 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \sqrt{\left(I_{\mathrm{c}}/\mathrm{A}\right)}$	8.71	12.60
6	$b_1 + b_2 \cdot \vartheta_{\mathrm{vj}} + \left(b_3 + b_4 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + \left(b_5 + b_6 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \ln\left(I_{\mathrm{c}}/\mathrm{A}\right)$	5.14	5.71
6	$b_1 + b_2 \cdot \vartheta_{\mathrm{vj}} + \left(b_3 + b_4 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + \left(b_5 + b_6 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \sqrt{\left(I_{\mathrm{c}}/\mathrm{A}\right)}$	3.34	3.92
7	$b_1 + b_2 \cdot \vartheta_{\mathrm{vj}} + b_3 \cdot \vartheta_{\mathrm{vj}}^2 + \left(b_4 + b_5 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + \left(b_6 + b_7 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \sqrt{\left(I_{\mathrm{c}}/\mathrm{A}\right)}$	3.23	**3.42**
7	$b_1 + b_2 \cdot \vartheta_{\mathrm{vj}} + \left(b_3 + b_4 \cdot \vartheta_{\mathrm{vj}} + b_5 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot I_{\mathrm{c}} + \left(b_6 + b_7 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \sqrt{\left(I_{\mathrm{c}}/\mathrm{A}\right)}$	3.33	3.69
7	$b_1 + b_2 \cdot \vartheta_{\mathrm{vj}} + \left(b_3 + b_4 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + \left(b_5 + b_6 \cdot \vartheta_{\mathrm{vj}} + b_7 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot \sqrt{\left(I_{\mathrm{c}}/\mathrm{A}\right)}$	3.28	3.59
8	$b_1 + b_2 \cdot \vartheta_{\mathrm{vj}} + b_3 \cdot \vartheta_{\mathrm{vj}}^2 + \left(b_4 + b_5 \cdot \vartheta_{\mathrm{vj}} + b_6 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot I_{\mathrm{c}} + \left(b_7 + b_8 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \sqrt{\left(I_{\mathrm{c}}/\mathrm{A}\right)}$	3.25	3.44
8	$b_1 + b_2 \cdot \vartheta_{\mathrm{vj}} + b_3 \cdot \vartheta_{\mathrm{vj}}^2 + \left(b_4 + b_5 \cdot \vartheta_{\mathrm{vj}}\right) \cdot I_{\mathrm{c}} + \left(b_6 + b_7 \cdot \vartheta_{\mathrm{vj}} + b_8 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot \sqrt{\left(I_{\mathrm{c}}/\mathrm{A}\right)}$	3.26	3.46
8	$b_1 + b_2 \cdot \vartheta_{\mathrm{vj}} + \left(b_3 + b_4 \cdot \vartheta_{\mathrm{vj}} + b_5 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot I_{\mathrm{c}} + \left(b_6 + b_7 \cdot \vartheta_{\mathrm{vj}} + b_8 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot \sqrt{\left(I_{\mathrm{c}}/\mathrm{A}\right)}$	3.23	3.46
9	$b_1 + b_2 \cdot \vartheta_{\mathrm{vj}} + b_3 \cdot \vartheta_{\mathrm{vj}}^2 + \left(b_4 + b_5 \cdot \vartheta_{\mathrm{vj}} + b_6 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot I_{\mathrm{c}} + \left(b_7 + b_8 \cdot \vartheta_{\mathrm{vj}} + b_9 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot \sqrt{\left(I_{\mathrm{c}}/\mathrm{A}\right)}$	3.18	3.71

Table A.2: Regression results of different regression functions for $U_{\mathrm{f}} = f\left(I_{\mathrm{c}}, \vartheta_{\mathrm{vj}}\right)$; number of parameters n_{par}; selected fit function in bold font; extract from [89]

n_{par}	Fit function	RMSD training data	RMSD validation data
3	Polynomial ($n_{U_{\mathrm{dc}}} = 1$, $n_{\vartheta} = 1$)	0.87	1.04
5	Polynomial ($n_{U_{\mathrm{dc}}} = 2$, $n_{\vartheta} = 1$)	0.78	**0.91**
5	Polynomial ($n_{U_{\mathrm{dc}}} = 1$, $n_{\vartheta} = 2$)	0.83	1.02
6	Polynomial ($n_{U_{\mathrm{dc}}} = 2$, $n_{\vartheta} = 2$)	0.78	0.91
7	Polynomial ($n_{U_{\mathrm{dc}}} = 1$, $n_{\vartheta} = 3$)	0.58	1.00
7	Polynomial ($n_{U_{\mathrm{dc}}} = 3$, $n_{\vartheta} = 1$)	0.77	0.99
9	Polynomial ($n_{U_{\mathrm{dc}}} = 2$, $n_{\vartheta} = 3$)	0.39	1.00
9	Polynomial ($n_{U_{\mathrm{dc}}} = 3$, $n_{\vartheta} = 2$)	0.77	0.98
10	Polynomial ($n_{U_{\mathrm{dc}}} = 3$, $n_{\vartheta} = 3$)	0.38	1.02
4	$(d_1 + d_2 \cdot U_{\mathrm{dc}}) \cdot \ln\left(1 - \frac{d_4 + d_5 \cdot \vartheta_{\mathrm{vj}} + 10\,\mathrm{V}}{25\,\mathrm{V}}\right)$	0.79	1.03
5	$\left(d_1 + d_2 \cdot U_{\mathrm{dc}} + d_3 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \ln\left(1 - \frac{d_4 + d_5 \cdot \vartheta_{\mathrm{vj}} + 10\,\mathrm{V}}{25\,\mathrm{V}}\right)$	0.80	1.01
6	$\left(d_1 + d_2 \cdot U_{\mathrm{dc}} + d_3 \cdot \vartheta_{\mathrm{vj}} + d_4 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot \ln\left(1 - \frac{d_5 + d_6 \cdot \vartheta_{\mathrm{vj}} + 10\,\mathrm{V}}{25\,\mathrm{V}}\right)$	0.78	1.03
6	$\left(d_1 + d_2 \cdot U_{\mathrm{dc}} + d_3 \cdot \vartheta_{\mathrm{vj}} + d_4 \cdot U_{\mathrm{dc}}^2\right) \cdot \ln\left(1 - \frac{d_5 + d_6 \cdot \vartheta_{\mathrm{vj}} + 10\,\mathrm{V}}{25\,\mathrm{V}}\right)$	0.74	0.90
6	$\left(d_1 + d_2 \cdot U_{\mathrm{dc}} + d_3 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \ln\left(1 - \frac{d_4 + d_5 \cdot \vartheta_{\mathrm{vj}} + d_6 \cdot \vartheta_{\mathrm{vj}}^2 10\,\mathrm{V}}{25\,\mathrm{V}}\right)$	0.62	0.90
7	$\left(d_1 + d_2 \cdot U_{\mathrm{dc}} + d_3 \cdot \vartheta_{\mathrm{vj}} + d_4 \cdot \vartheta_{\mathrm{vj}}^2 + d_5 \cdot U_{\mathrm{dc}}^2\right) \cdot \ln\left(1 - \frac{d_6 + d_7 \cdot \vartheta_{\mathrm{vj}} + 10\,\mathrm{V}}{25\,\mathrm{V}}\right)$	0.73	0.91
7	$\left(d_1 + d_2 \cdot U_{\mathrm{dc}} + d_3 \cdot \vartheta_{\mathrm{vj}} + d_4 \cdot U_{\mathrm{dc}}^2\right) \cdot \ln\left(1 - \frac{d_5 + d_6 \cdot \vartheta_{\mathrm{vj}} + d_7 \cdot \vartheta_{\mathrm{vj}}^2 + 10\,\mathrm{V}}{25\,\mathrm{V}}\right)$	0.73	0.91
7	$\left(d_1 + d_2 \cdot U_{\mathrm{dc}} + d_3 \cdot \vartheta_{\mathrm{vj}} + d_4 \cdot \vartheta_{\mathrm{vj}}^2\right) \cdot \ln\left(1 - \frac{d_5 + d_6 \cdot \vartheta_{\mathrm{vj}} + d_7 \cdot \vartheta_{\mathrm{vj}}^2 + 10\,\mathrm{V}}{25\,\mathrm{V}}\right)$	0.71	0.95

Table A.3: Regression results of different regression functions for $t_{\mathrm{d}} = f\left(U_{\mathrm{dc}}, \vartheta_{\mathrm{vj}}\right)$; number of parameters n_{par}; selected fit function in bold font; extract from [89]; polynomial fit chosen due to its simplicity and neglectable difference to the best fit

n_{par}	Fit function	RMSE training data	RMSE validation data
6	$e_1 + e_2 \cdot i_{\mathrm{c}} + e_4 \cdot \vartheta_{\mathrm{vj}} + (e_6 + e_7 \cdot i_{\mathrm{c}}) \cdot U_{\mathrm{dc}} + e_8 \cdot \sqrt{i_{\mathrm{c}}}$	3.38	3.75
7	$e_1 + e_2 \cdot i_{\mathrm{c}} + (e_4 + e_5 \cdot i_{\mathrm{c}}) \cdot \vartheta_{\mathrm{vj}} + e_6 \cdot U_{\mathrm{dc}} + \left(e_8 + e_9 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \sqrt{i_{\mathrm{c}}}$	6.54	6.90
7	$e_1 + e_2 \cdot i_{\mathrm{c}} + e_4 \cdot \vartheta_{\mathrm{vj}} + (e_6 + e_7 \cdot i_{\mathrm{c}}) \cdot U_{\mathrm{dc}} + \left(e_8 + e_9 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \sqrt{i_{\mathrm{c}}}$	2.99	3.04
7	$e_1 + e_2 \cdot i_{\mathrm{c}} + (e_4 + e_5 \cdot i_{\mathrm{c}}) \cdot \vartheta_{\mathrm{vj}} + (e_6 + e_7 \cdot i_{\mathrm{c}}) \cdot U_{\mathrm{dc}} + e_8 \cdot \sqrt{i_{\mathrm{c}}}$	2.95	3.03
8	$e_1 + e_2 \cdot i_{\mathrm{c}} + (e_4 + e_5 \cdot i_{\mathrm{c}}) \cdot \vartheta_{\mathrm{vj}} + (e_6 + e_7 \cdot i_{\mathrm{c}}) \cdot U_{\mathrm{dc}} + \left(e_8 + e_9 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \sqrt{i_{\mathrm{c}}}$	2.94	2.94
9	$e_1 + e_2 \cdot i_{\mathrm{c}} + e_3 \cdot i_{\mathrm{c}}^2 + (e_4 + e_5 \cdot i_{\mathrm{c}}) \cdot \vartheta_{\mathrm{vj}} + (e_6 + e_7 \cdot i_{\mathrm{c}}) \cdot U_{\mathrm{dc}} + \left(e_8 + e_9 \cdot \vartheta_{\mathrm{vj}}\right) \cdot \sqrt{i_{\mathrm{c}}}$	2.00	**2.16**

Table A.4: Regression results of different regression functions for $t_{\mathrm{ri}} = f\left(U_{\mathrm{dc}}, I_{\mathrm{c}}, \vartheta_{\mathrm{vj}}\right)$; number of parameters n_{par}; selected fit function in bold font; extract from [89]

B IGBT module gate loop impedance measurement

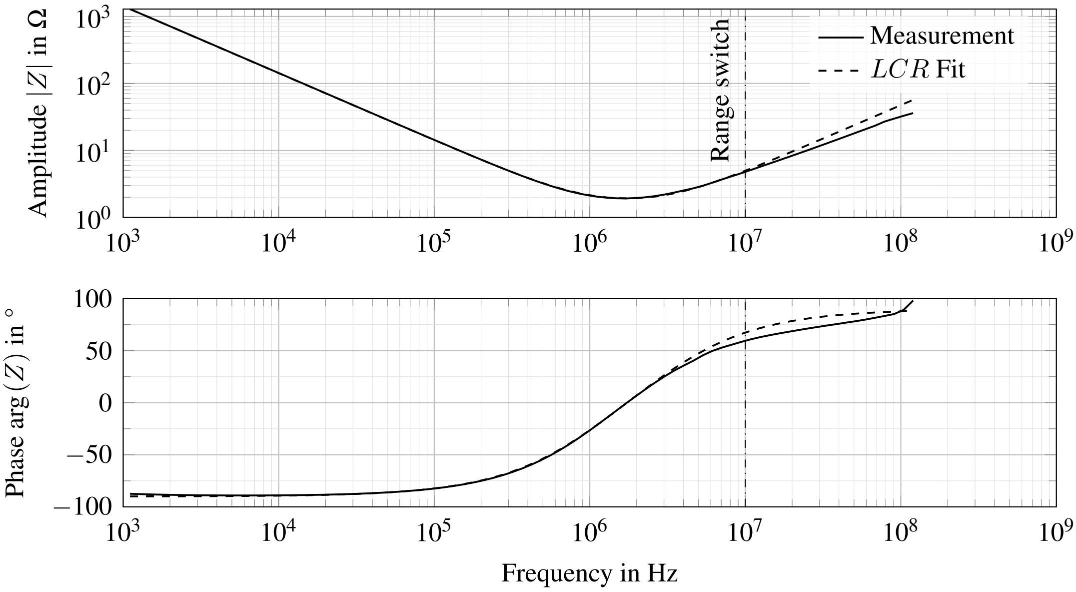

Figure B.1: Measured impedance Z of the IGBT's gate loop with an impedance analyzer; the impedance analyzer *Wayne Kerr 6500B* switches measurement ranges at 10 MHz, causing discontinuities in the measurement method

Table B.1: Estimated values; gate resistance extracted at resonant frequency

Model	$\underline{Z} = R + j\omega L + \frac{1}{j\omega C}$, L and C constant
Resonant frequency	1.7 MHz
Gate capacitance	111.7 nF
Applied dc voltage level	$U_\mathrm{g} = 0\,\mathrm{V}$
Gate loop inductance	75.4 nH (50 nH, 100 nH)
Overall gate resistance	$R_\mathrm{g} = \min(\underline{Z}) = 1.923\,\Omega$

C On-state voltage model combinations

Table C.1: Investigated model combinations for the fitting of the on-state voltage

ID	Bulk mobility	Channel mobility	MOS channel	Accumulation region	Drift region	Interconnects
1	1	1	1	1	1	1
2	2	1	1	1	1	1
3	1	1	1	2	1	1
4	2	1	1	2	1	1
5	1	2	1	1	1	1
6	2	2	1	1	1	1
7	1	2	1	2	1	1
8	2	2	1	2	1	1
9	1	3	1	1	1	1
10	2	3	1	1	1	1
11	1	3	1	2	1	1
12	2	3	1	2	1	1
13	1	1	2	1	1	1
14	2	1	2	1	1	1
15	1	1	2	2	1	1
16	2	1	2	2	1	1
17	1	2	2	1	1	1
18	2	2	2	1	1	1
19	1	2	2	2	1	1
20	2	2	2	2	1	1
21	1	3	2	1	1	1
22	2	3	2	1	1	1
23	1	3	2	2	1	1
24	2	3	2	2	1	1
25	1	1	1	1	1	2
26	2	1	1	1	1	2

Table C.1: Investigated model combinations for the fitting of the on-state voltage

ID	Bulk mobility	Channel mobility	MOS channel	Accumulation region	Drift region	Interconnects
27	1	1	1	2	1	2
28	2	1	1	2	1	2
29	1	2	1	1	1	2
30	2	2	1	1	1	2
31	1	2	1	2	1	2
32	2	2	1	2	1	2
33	1	3	1	1	1	2
34	2	3	1	1	1	2
35	1	3	1	2	1	2
36	2	3	1	2	1	2
37	1	1	2	1	1	2
37	1	1	2	1	1	2
38	2	1	2	1	1	2
39	1	1	2	2	1	2
40	2	1	2	2	1	2
41	1	2	2	1	1	2
42	2	2	2	1	1	2
43	1	2	2	2	1	2
44	2	2	2	2	1	2
45	1	3	2	1	1	2
46	2	3	2	1	1	2
47	1	3	2	2	1	2
48	2	3	2	2	1	2

D Regression parameters $U_{\text{ds,on}}$

Figure D.1 shows box plots of the regression parameters of the selected on-state voltage model Variant 13. The underlying data is the fit result of each regression parameter for each of the 18 switches. Each model was fitted over 100 times, while the initial values were varied by ±50 %. Only the fit with the lowest RMSD on the training data was kept for each of the 18 switches.

Table D.1 shows the regression parameter results for all switches as well as the median of each regression parameter value across the 18 results. The table also includes the used initial values of each parameter.

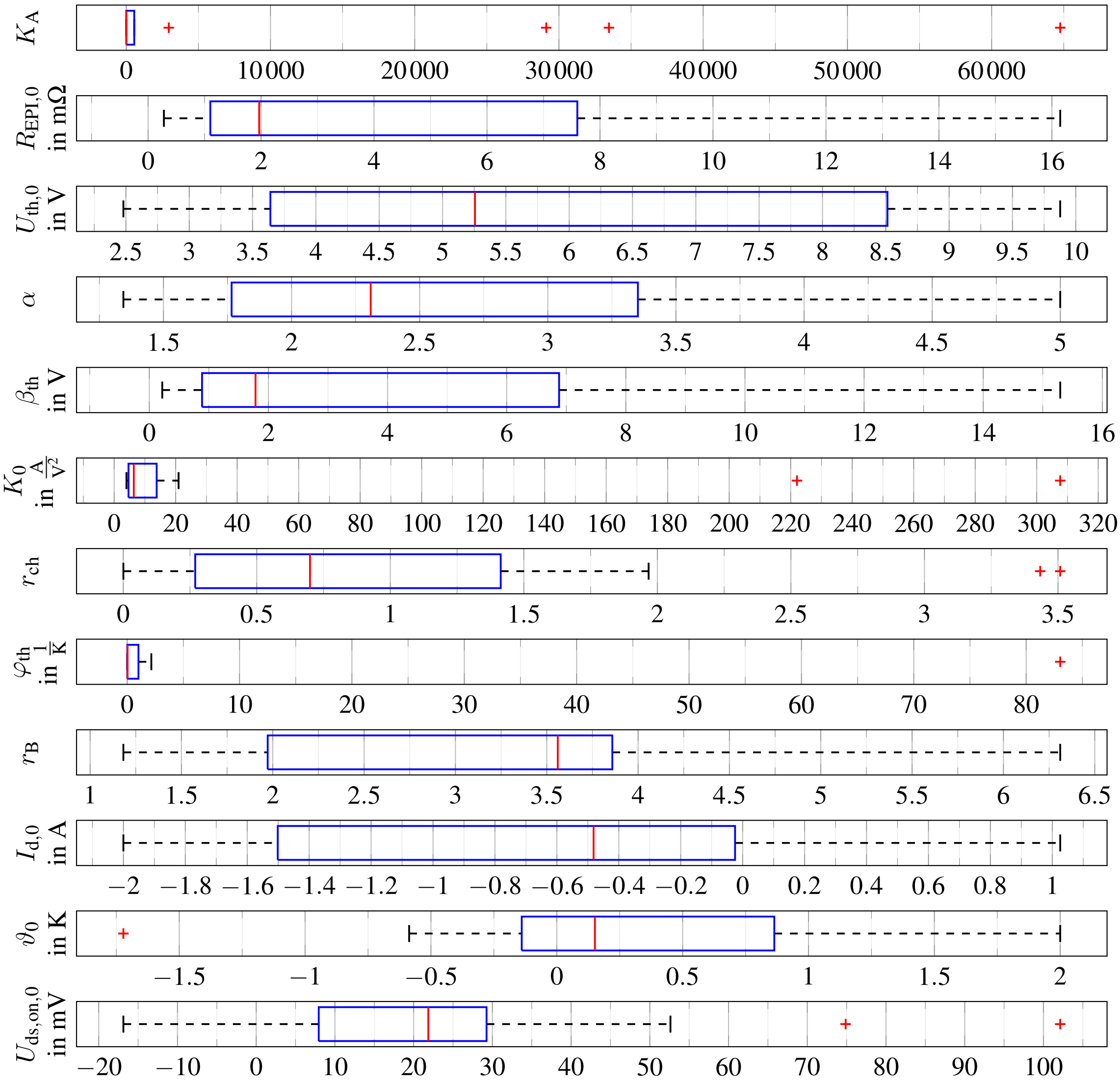

Figure D.1: Box plots of the regression parameters of the selected on-state voltage model Variant 13; data set of 18 values per parameter

Table D.1: Regression parameters of the selected on-state voltage model Variant 13 for each of the 18 switches; median of each regression parameter and the used initial value at the beginning of the fitting process; the RMSD corresponds to the training data (two pages)

Module	Switch	K_A	$R_\mathrm{EPI,0}$ in mΩ	$U_\mathrm{th,0}$ in V	α	β_th in V	K_0 in $\frac{\mathrm{A}}{\mathrm{V}^2}$	r_ch	φ_th in $\frac{1}{\mathrm{K}}$	r_B	$I_\mathrm{d,0}$ in A	ϑ_0 in V	$U_\mathrm{ds,on,0}$ in mV	RMSD in mV
M_0	HS	4.24	0.44	4.83	2.61	0.43	4.00	0.08	0.81	3.84	0.52	0.53	5.19	8.85
M_0	LS	64 754	3.65	3.36	2.83	0.58	4.67	0.63	0.01	3.76	−2.00	−0.36	36.74	18.45
M_1	HS	2948	3.35	3.64	2.07	15.00	4.80	0.27	0.00	4.33	0.02	−0.09	11.30	70.84
M_1	LS	29 122	1.10	4.06	1.47	5.40	4.10	0.36	0.02	6.31	−0.20	−0.59	7.94	47.38
M_2	HS	3.30	0.43	2.48	2.70	0.27	4.32	0.05	1.07	3.80	−0.62	0.49	20.52	60.29
M_2	LS	0.60	0.28	7.01	1.69	0.95	14.76	1.05	0.01	3.06	−0.02	1.37	23.93	33.13
M_3	HS	8.25	1.46	9.88	2.20	1.62	4.33	0.25	1.01	4.31	−0.17	0.86	8.07	46.03
M_3	LS	33 468	8.96	5.82	5.00	0.89	8.26	1.97	0.05	1.55	−2.00	0.34	25.76	61.78
M_4	HS	3.17	1.85	3.68	2.01	0.92	6.42	0.92	0.02	3.22	−0.67	−0.14	23.21	4.22
M_4	LS	4.23	13.04	9.22	3.35	15.29	222	0.63	83.03	1.65	1.03	2.00	29.26	40.67
M_5	HS	1.24	7.60	9.23	4.21	1.95	20.95	3.43	0.01	1.93	0.39	−1.72	1.51	6.29
M_5	LS	2.23	16.15	7.49	3.85	15.27	308	3.51	2.15	1.18	−1.91	1.20	102	44.56
M_6	HS	3.05	1.04	4.80	1.77	0.92	6.35	0.77	0.01	3.65	−0.34	−0.09	23.48	4.61
M_6	LS	554	6.30	8.51	2.42	4.60	8.72	1.82	0.05	1.97	−1.01	−0.32	−3.59	33.53

Table D.1: Regression parameters of the selected on-state voltage model Variant 13 for each of the 18 switches; median of each regression parameter and the used initial value at the beginning of the fitting process; the RMSD corresponds to the training data (two pages)

Module	Switch	K_{A}	$R_{\mathrm{EPI,0}}$ in mΩ	$U_{\mathrm{th,0}}$ in V	α	β_{th} in V	K_0 in $\frac{\mathrm{A}}{\mathrm{V}^2}$	r_{ch}	φ_{th} in $\frac{1}{\mathrm{K}}$	r_{B}	$I_{\mathrm{d,0}}$ in A	ϑ_0 in V	$U_{\mathrm{ds,on,0}}$ in mV	RMSD in mV
M_7	HS	12.86	1.96	5.68	1.63	5.15	5.61	0.83	0.02	4.27	-0.19	0.49	17.52	4.93
M_7	LS	112	8.76	9.17	3.45	8.02	13.83	1.41	0.04	2.27	-0.97	1.89	-16.87	22.99
M_8	HS	5.99	1.97	2.98	1.34	6.88	7.31	$5.34 \cdot 10^{-4}$	1.46	3.86	-1.50	-0.04	52.62	8.13
M_8	LS	3.40	1.17	3.64	2.02	0.22	5.17	0.42	0.01	3.47	-2.00	-0.03	74.87	27.90
Median		4.24	1.96	4.83	2.20	1.62	6.35	0.63	0.02	3.47	-0.34	0	20.52	27.90
Initial values ±50 %		0.50	50.00	4.50	1.50	0.85	2.40[1]	0.86	0.01	5.02	0	0	0	-

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[1] The transconductance K_0 was incorrectly initialized with 2.4 $\frac{\mathrm{A}}{\mathrm{V}^2}$. A more appropriate value is 4.8 $\frac{\mathrm{A}}{\mathrm{V}^2}$, as determined in Section F.

E Fit results terminal-to-chip resistance

Figure E.1 shows the fit results of the terminal-to-chip resistance R_t at reference temperature $\vartheta_\mathrm{ref} = 300\,\mathrm{K}$, as well as the fitted linear temperature coefficient. The fit parameters are limited to the range of $0\,\mathrm{m}\Omega$ to $5\,\mathrm{m}\Omega$, and $0\,\frac{1}{\mathrm{K}}$ to $5 \cdot 10^{-3}\,\frac{1}{\mathrm{K}}$ respectively. The terminal connections are mostly copper and aluminum and should experience less or equal of the temperature change of the baseplate or junction during the double-pulse experiments. Therefore, the fitted temperature coefficient α_t of R_t is expected to be smaller than that of copper or aluminum.

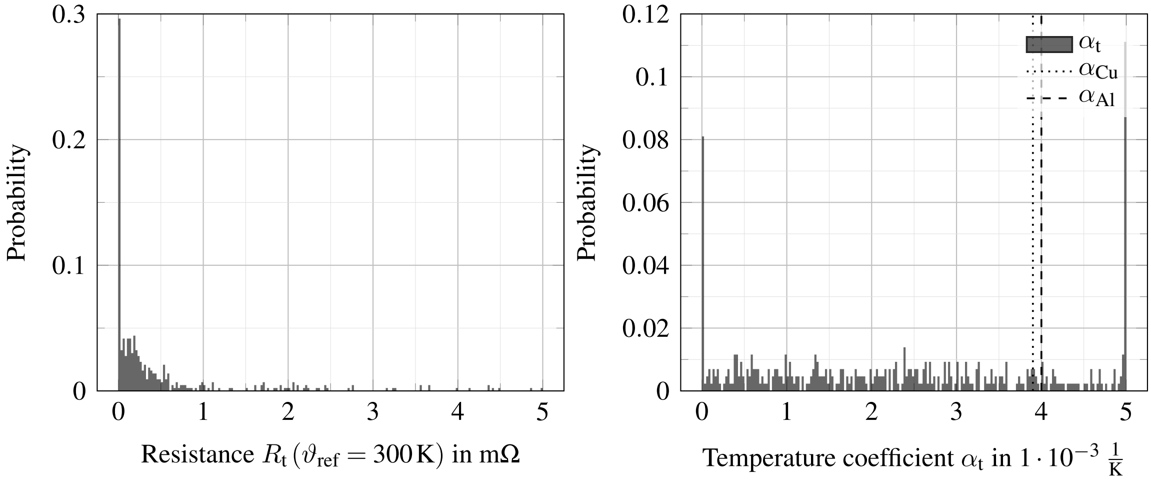


Figure E.1: Fit results of the terminal-to-chip resistance R_t according to Table 8.4; typical temperature coefficients for aluminum and copper marked as vertical lines

The homogenous and widespread results of the temperature coefficient show that the available calibration data and model functions of the rest of the MOSFET do not support distinguishing between linear temperature dependencies of the module interconnects and the slightly nonlinear behavior of the semiconductor within the calibration range.

F Transfer characteristic of the MOSFET under test

The transfer characteristic shown in Figure F.1 was extracted from the datasheet of a different module IMZ120R045M1 [124]. The datasheet of the DUT FF23MR12W1M1_B11 [147] only includes data for room temperature. The module IMZ120R045M1 appears to use a single SiC chip of the same type, while the DUT uses two chips in parallel. Therefore, the estimated transconductance $K^{(\mathrm{IMZ120})}$ is scaled to the DUT transconductance $K^{(\mathrm{FF23})}$. The following fit function was used

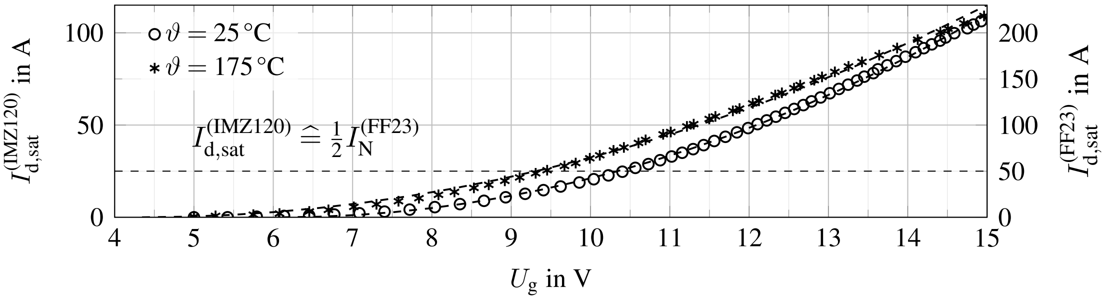


Figure F.1: Transfer characteristic of the matching device IMZ120R045M1 with half the number of equal SiC chips [124] and fit results in dashed

$$I_{\mathrm{d,sat}}^{*} = \frac{K^{(\mathrm{IMZ120})}}{2}\left(U_{\mathrm{g}} - U_{\mathrm{th}}\right)^2, \quad K^{(\mathrm{FF23})} = 2K^{(\mathrm{IMZ120})}. \tag{F.1}$$

The results are listed in Table F.1. They show a negative temperature coefficient for the transconductance K and the threshold voltage U_{th}.

Table F.1: Fit results

ϑ	$K^{(\mathrm{IMZ120})}$	$K^{(\mathrm{FF23})}$	U_{th}
25 °C	$2.8\,\frac{\mathrm{A}}{\mathrm{V}^2}$	$5.6\,\frac{\mathrm{A}}{\mathrm{V}^2}$	6.1 V
175 °C	$2.0\,\frac{\mathrm{A}}{\mathrm{V}^2}$	$4.1\,\frac{\mathrm{A}}{\mathrm{V}^2}$	4.3 V

Furthermore, the fits show a drop in the Miller plateau voltage needed to conduct the nominal current of the DUT

$$\frac{\mathrm{d}U_{\mathrm{M}}\left(I_{\mathrm{N}}\right)}{\mathrm{d}\vartheta} \approx \frac{\Delta U_{\mathrm{g}}}{\Delta \vartheta} = \frac{9.3\,\mathrm{V} - 10.35\,\mathrm{V}}{175\,°\mathrm{C} - 25\,°\mathrm{C}} = -7\,\frac{\mathrm{mV}}{\mathrm{K}}. \tag{F.2}$$

G TDC front-end measurement

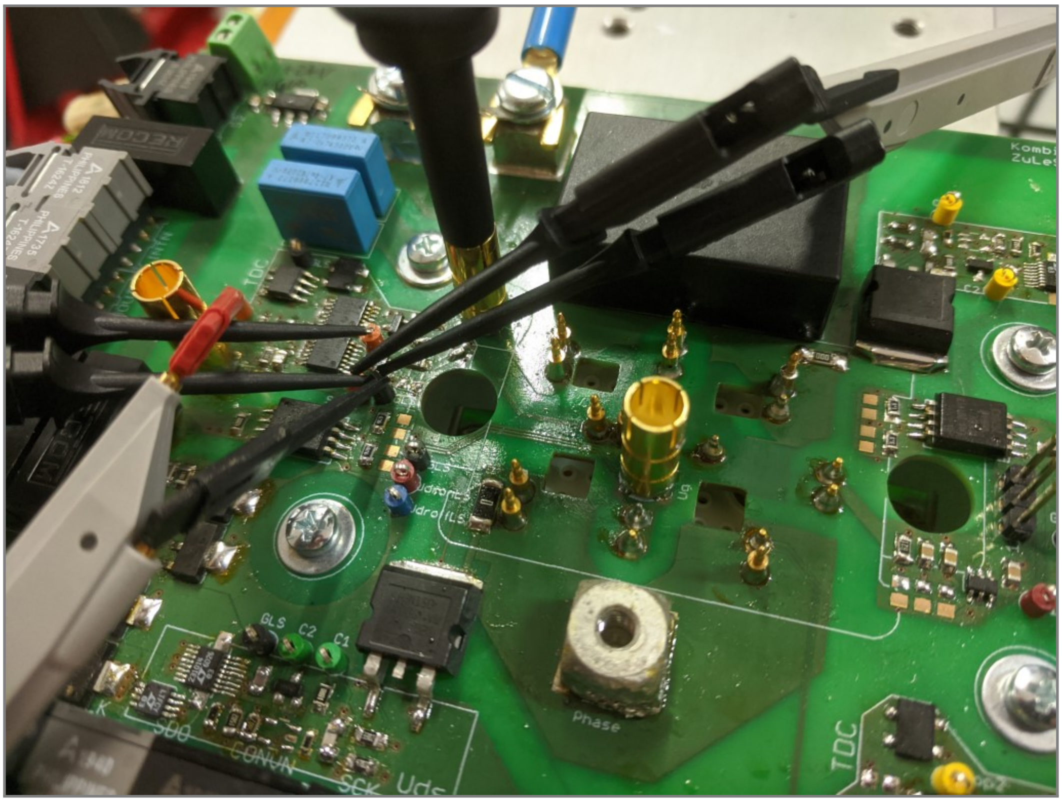


Figure G.1: Photo of the measurement setup of the TDC front-end trigger signals with high EMI

H Current step examples during PWM

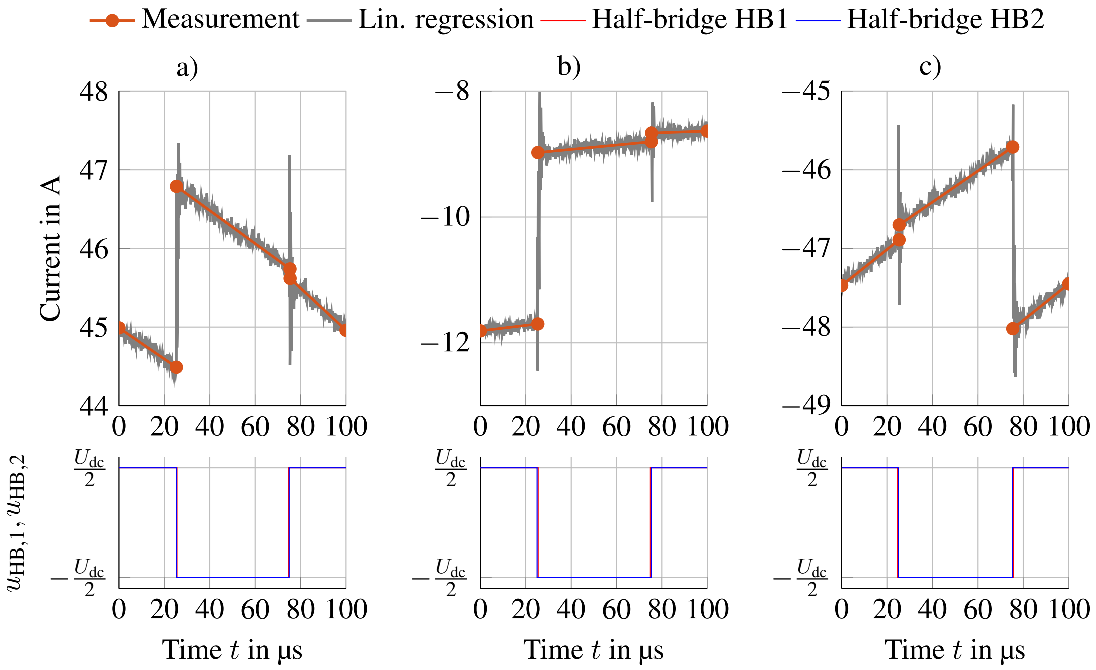


Figure H.1: Measured current waveforms of different PWM periods for different current levels and the expected output voltages of the half-bridges; propagation delay T_{p} not yet included in the shown output voltage

Table H.1: Size of the measured current steps

	a)		b)		c)	
	Expected	Measured	Expected	Measured	Expected	Measured
ΔI_1	0.96 A	2.27 A	1.64 A	2.73 A	−1.00 A	0.17 A
ΔI_2	0.96 A	−0.12 A	1.64 A	0.14 A	−1.00 A	−2.33 A
Σ	1.92 A	2.16 A	3.27 A	2.87 A	−1.99 A	−2.16 A

I Estimation of the node capacitance

Estimating the node capacitance from datasheet values The required charge ΔQ_{node} to change the voltage of the node capacitance C_{node} between 0 V and U_{dc} can be estimated from the nonlinear output capacitance C_{oss} stated in the corresponding datasheets. The datasheet of the module under test [147] does not contain detailed information on C_{oss}, but the module uses two SiC MOSFET chips in parallel which are assumed to be used in other devices as well. The output capacitance listed in the datasheet of IMZ120R045M1 [124], a discrete SiC MOSFET device with matching characteristics and a single chip, is used and scaled by two. The top graph in Figure I.1 shows the C_{oss} extracted from the datasheet, which can be used to find the voltage dependent charge Q_{oss} of one switch in the used SiC module

$$\mathrm{d}Q = C\left(U\right)\mathrm{d}U, \tag{I.1}$$

$$Q_{\text{oss}}\left(U\right) = \int_0^{U_{\text{dc}}} \underbrace{2C_{\text{oss}}\left(U'\right)}_{\text{single-chip datasheet information scaled to the used SiC module}} \mathrm{d}U'. \tag{I.2}$$

This describes the charge for a single topological switch Q_{oss}. The half-bridge consists of two topological switches, the high-side switch and the low-side switch. Both need to be charged, therefore the entire charge required to switch the output voltage of the half-bridge is

$$\Delta Q_{\text{node}} = 2 \cdot Q_{\text{oss}}\left(U_{\text{dc}}\right) \approx 587\,\text{nC}, \tag{I.3}$$

$$C_{\text{node}} = \frac{\Delta Q_{\text{node}}}{U_{\text{dc}}} \approx 736\,\text{pF}. \tag{I.4}$$

Capacitances towards PE are not considered. The bottom graph in Figure I.1 shows the charge of the low-side and high-side switch of a half-bridge depending on the low-side switch's voltage U_{ds}, as well as the total charge of the phase terminal Q_{node} obtained from the superposition of the charge states of both switches

$$Q_{\text{node}}\left(U_{\text{ds}}\right) = Q_{\text{oss}}\left(U_{\text{ds}}\right) - \left(Q_{\text{oss}}\left(U_{\text{dc}} - U_{\text{ds}}\right) - Q_{\text{oss}}\left(U_{\text{dc}}\right)\right). \tag{I.5}$$

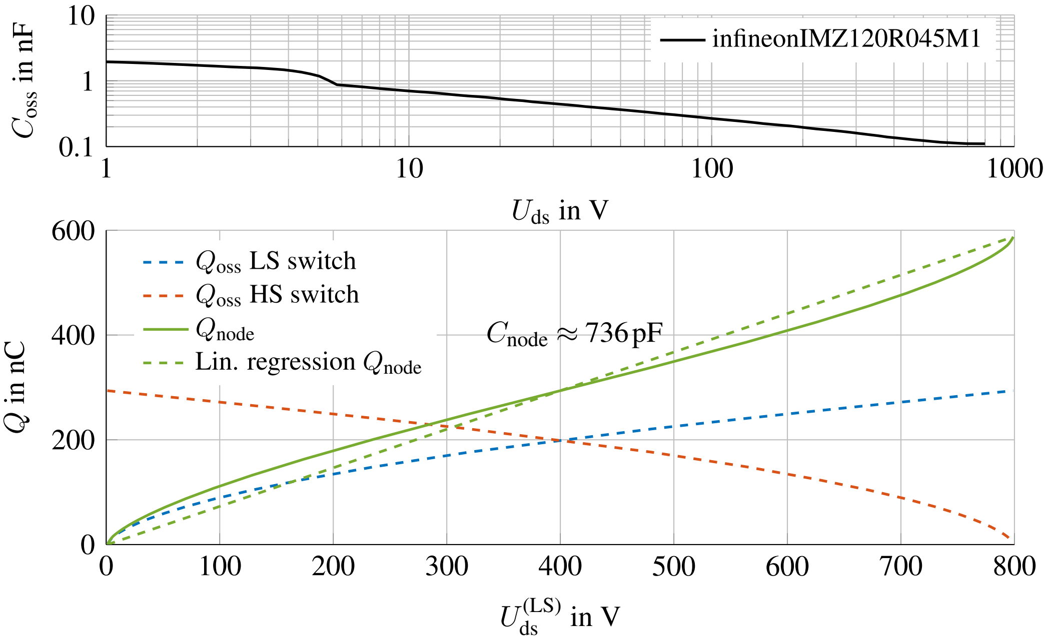


Figure I.1: Output capacitance extracted from another datasheet [124] and the resulting node charge caused by the output capacitances of the MOSFETs only

J Thermal impedance parameters

Table J.1: Z_{th} fit parameters for a single TIM layer, see Figure 12.6

	$R_{\text{th},i}$ in mΩ	τ_i in s	τ_{d} in ms	R_{th} in Ω	R^2	
$z_{\text{th,HS,HS}}$	47.0	$497 \cdot 10^{-6}$	-	1.02	0.9999	Foster models with 5 elements
	241.1	$35 \cdot 10^{-3}$				
	317.6	$242 \cdot 10^{-3}$				
	308.3	1.3				
	106.6	10.2				
$z_{\text{th,LS,LS}}$	47.0	$497 \cdot 10^{-6}$	-	1.05	0.9999	
	227.0	$34 \cdot 10^{-3}$				
	310.2	$224 \cdot 10^{-3}$				
	352.7	1.2				
	117.5	10.2				
$z_{\text{th,HS,LS}}$	84.3	$898 \cdot 10^{-3}$	898	0.19	0.9978	Foster models with 3 elements and a low-pass filter
	80.0	6.1				
	25.5	47.2				
$z_{\text{th,LS,HS}}$	79.2	$886 \cdot 10^{-3}$	886	0.18	0.9974	
	73.5	6.1				
	28.3	41.5				
$z_{\text{th,HS,NTC}}$	122.4	$637 \cdot 10^{-3}$	637	0.24	0.9997	
	92.0	5.0				
	27.8	31.2				
$z_{\text{th,LS,NTC}}$	78.6	$900 \cdot 10^{-3}$	901	0.17	0.9995	
	67.3	6.5				
	19.6	36.4				

Table J.2: Z_{th} fit parameters for a double TIM layer, see Figure 12.6

	$R_{\text{th},i}$ in mΩ	τ_i in s	τ_{d} in ms	R_{th} in Ω	R^2	
$z_{\text{th,HS,HS}}$	47.0	$497{\cdot}10^{-6}$	-	1.17	0.9999	Foster models with 5 elements
	259.4	$40{\cdot}10^{-3}$				
	302.9	$300{\cdot}10^{-3}$				
	428.9	1.7				
	131.7	13.9				
$z_{\text{th,LS,LS}}$	47.0	$497{\cdot}10^{-6}$	-	1.18	0.9999	
	241.9	$32{\cdot}10^{-3}$				
	315.4	$233{\cdot}10^{-3}$				
	440.7	1.5				
	135.9	12.6				
$z_{\text{th,HS,LS}}$	159.6	2.4	403	0.26	0.9985	Foster models with 3 elements and a low-pass filter
	71.3	10.6				
	27.9	62.8				
$z_{\text{th,LS,HS}}$	163.1	2.5	468	0.25	0.9989	
	70.8	13.2				
	19.6	121.1				
$z_{\text{th,HS,NTC}}$	139.1	$734{\cdot}10^{-3}$	734	0.33	0.9998	
	136.9	4.1				
	54.8	25.6				
$z_{\text{th,LS,NTC}}$	104.8	1.2	1000	0.22	0.9997	
	83.3	5.9				
	33.6	31.2				

$$z_{\text{th,Foster5}}(t) = \sum_{i=1}^{5} R_{\text{th},i}\left(1-\mathrm{e}^{-\frac{t}{\tau_i}}\right), \tag{J.1}$$

$$z_{\text{th,Foster3,LP}}(t) = \sum_{i=1}^{3} \frac{R_{\text{th},i}}{\tau_{\text{d}}-\tau_i}\left(\tau_{\text{d}}\left(1-\mathrm{e}^{-\frac{t}{\tau_{\text{d}}}}\right)-\tau_i\left(1-\mathrm{e}^{-\frac{t}{\tau_i}}\right)\right), \tag{J.2}$$

$$R_{\text{th}} = \sum_{i=1} R_{\text{th},i} \tag{J.3}$$

K Switching loss model

The loss model was developed in [162], the results of which are used within this work. Further details are also published in [163]. The loss model functions are

$$E\left(R_{\mathrm{g,on,ext}}, U_{\mathrm{dc}}, I_{\mathrm{L}}, \vartheta\right) = E_{\mathrm{ref}} \cdot f_{\mathrm{R}}\left(R_{\mathrm{g,on,ext}}\right) \cdot f_{\mathrm{U}}\left(U_{\mathrm{dc}}\right) \cdot f_{\mathrm{I},\vartheta}\left(I_{\mathrm{L}}, \vartheta\right), \tag{K.1}$$

$$f_{\mathrm{R}}\left(R_{\mathrm{g,on,ext}}\right) = c_{2,\mathrm{R}} \cdot R_{\mathrm{g,on,ext}}^2 + c_{1,\mathrm{R}} \cdot R_{\mathrm{g,on,ext}} + c_{0,\mathrm{R}}, \tag{K.2}$$

$$f_{\mathrm{U}}\left(U_{\mathrm{dc}}\right) = c_{2,\mathrm{U}} \cdot U_{\mathrm{dc}}^2 + c_{1,\mathrm{U}} \cdot U_{\mathrm{dc}} + c_{0,\mathrm{U}}, \tag{K.3}$$

$$\begin{aligned} f_{\mathrm{I},\vartheta}\left(I_{\mathrm{L}}, \vartheta\right) =& c_{20,\mathrm{I},\vartheta} \cdot I_{\mathrm{L}}^2 + c_{11,\mathrm{I},\vartheta} \cdot I_{\mathrm{L}}\vartheta + c_{02,\mathrm{I},\vartheta} \cdot \vartheta^2 + \\ & c_{10,\mathrm{I},\vartheta} \cdot I_{\mathrm{L}} + c_{01,\mathrm{I},\vartheta} \cdot \vartheta + c_{00,\mathrm{I},\vartheta} \end{aligned} . \tag{K.4}$$

Table K.1: Loss model fit parameters used for the model based temperature prediction [162]

		Turn-on losses $E_{\mathrm{sw,on}}$	Turn-off losses $E_{\mathrm{sw,off}}$	Reverse recovery losses $E_{\mathrm{sw,rec}}$
	E_{ref} in J	$3.62 \cdot 10^{-4}$	$116.7695 \cdot 10^{-6}$	$9.5467 \cdot 10^{-6}$
f_{R}	$c_{2,\mathrm{R}}$ in $\frac{1}{\Omega^2}$	$7.6265 \cdot 10^{-3}$	$4.0675 \cdot 10^{-3}$	–
	$c_{1,\mathrm{R}}$ in $\frac{1}{\Omega}$	$171.1195 \cdot 10^{-3}$	$131.4545 \cdot 10^{-3}$	–
	$c_{0,\mathrm{R}}$	$806.4535 \cdot 10^{-3}$	$853.1685 \cdot 10^{-3}$	–
f_{U}	$c_{2,\mathrm{U}}$ in $\frac{1}{\mathrm{V}^2}$	$1.8805 \cdot 10^{-6}$	$785.0677 \cdot 10^{-9}$	$-1.0572 \cdot 10^{-6}$
	$c_{1,\mathrm{U}}$ in $\frac{1}{\mathrm{V}}$	$622.6339 \cdot 10^{-6}$	$794.3046 \cdot 10^{-6}$	$1.9616 \cdot 10^{-3}$
	$c_{0,\mathrm{U}}$	$-38.7542 \cdot 10^{-3}$	$246.3702 \cdot 10^{-3}$	$212.0079 \cdot 10^{-3}$
$f_{\mathrm{I},\vartheta}$	$c_{20,\mathrm{I},\vartheta}$ in $\frac{1}{\mathrm{A}^2}$	$3.3371 \cdot 10^{-6}$	$158.6369 \cdot 10^{-6}$	$50.3316 \cdot 10^{-6}$
	$c_{11,\mathrm{I},\vartheta}$ in $\frac{1}{\mathrm{A} \cdot \mathrm{K}}$	$55.7749 \cdot 10^{-6}$	$-6.7671 \cdot 10^{-6}$	$218.6022 \cdot 10^{-6}$
	$c_{02,\mathrm{I},\vartheta}$ in $\frac{1}{\mathrm{K}^2}$	$14.0604 \cdot 10^{-6}$	$7.4356 \cdot 10^{-6}$	$53.5762 \cdot 10^{-6}$
	$c_{10,\mathrm{I},\vartheta}$ in $\frac{1}{\mathrm{A}}$	$11.1268 \cdot 10^{-3}$	$2.3922 \cdot 10^{-3}$	$-3.2090 \cdot 10^{-3}$
	$c_{01,\mathrm{I},\vartheta}$ in $\frac{1}{\mathrm{K}}$	$-2.4371 \cdot 10^{-3}$	$-1.3647 \cdot 10^{-3}$	$-8.0557 \cdot 10^{-3}$
	$c_{00,\mathrm{I},\vartheta}$	$405.5779 \cdot 10^{-3}$	$519.7111 \cdot 10^{-3}$	$885.5352 \cdot 10^{-3}$

L Power-cycling tests - TSEP measurements (double-pulse experiments)

Table L.1: Overview of the used modules

Context	Module	Description
Default module	M_0	Used for system development, testing, fundamental investigations
Accelerated aging tests	M_1	Aged PCT module; micro sectioning after 100 % EOL
	M_2	Aged PCT module; micro sectioning after 50 % EOL
	M_3	Aged PCT module
	M_4	Aged PCT module
	M_5	Reference PCT module; mounted during PCT, but no load applied
	M_6	Aged PCT module
	M_7	Aged PCT module

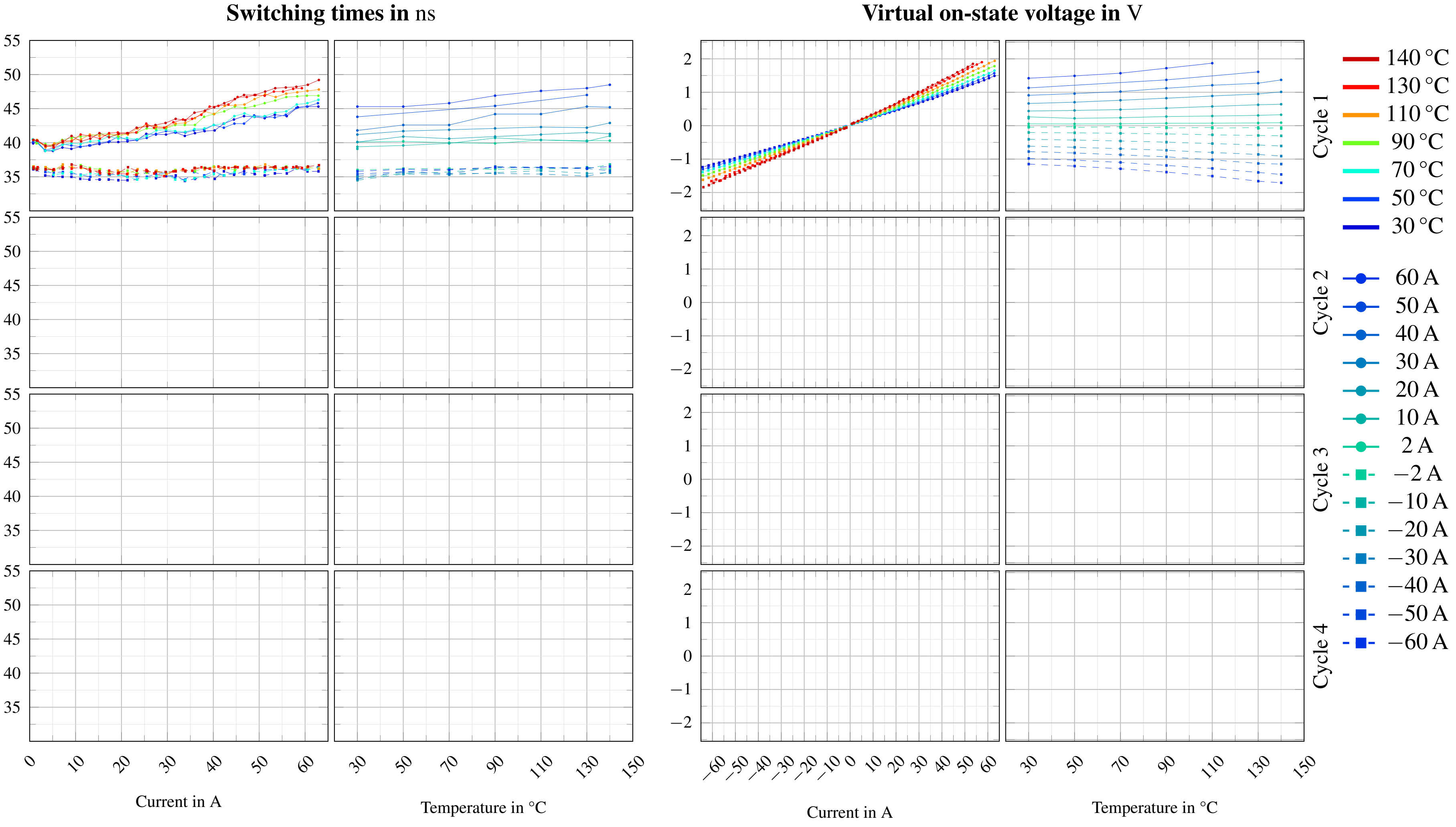


Figure L.1: TSEP measurements for module M_0, high side

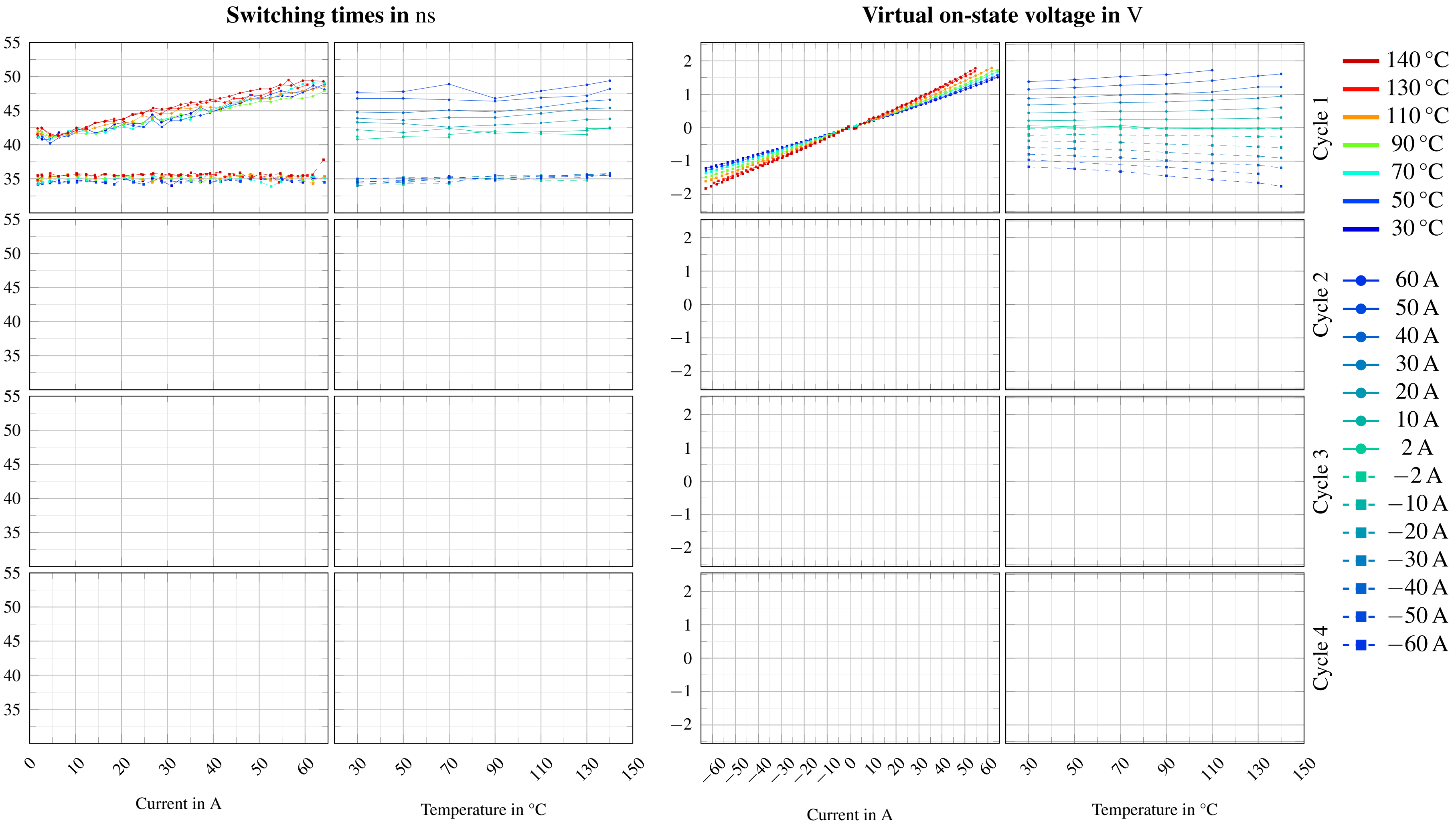


Figure L.2: TSEP measurements for module M_0, low side

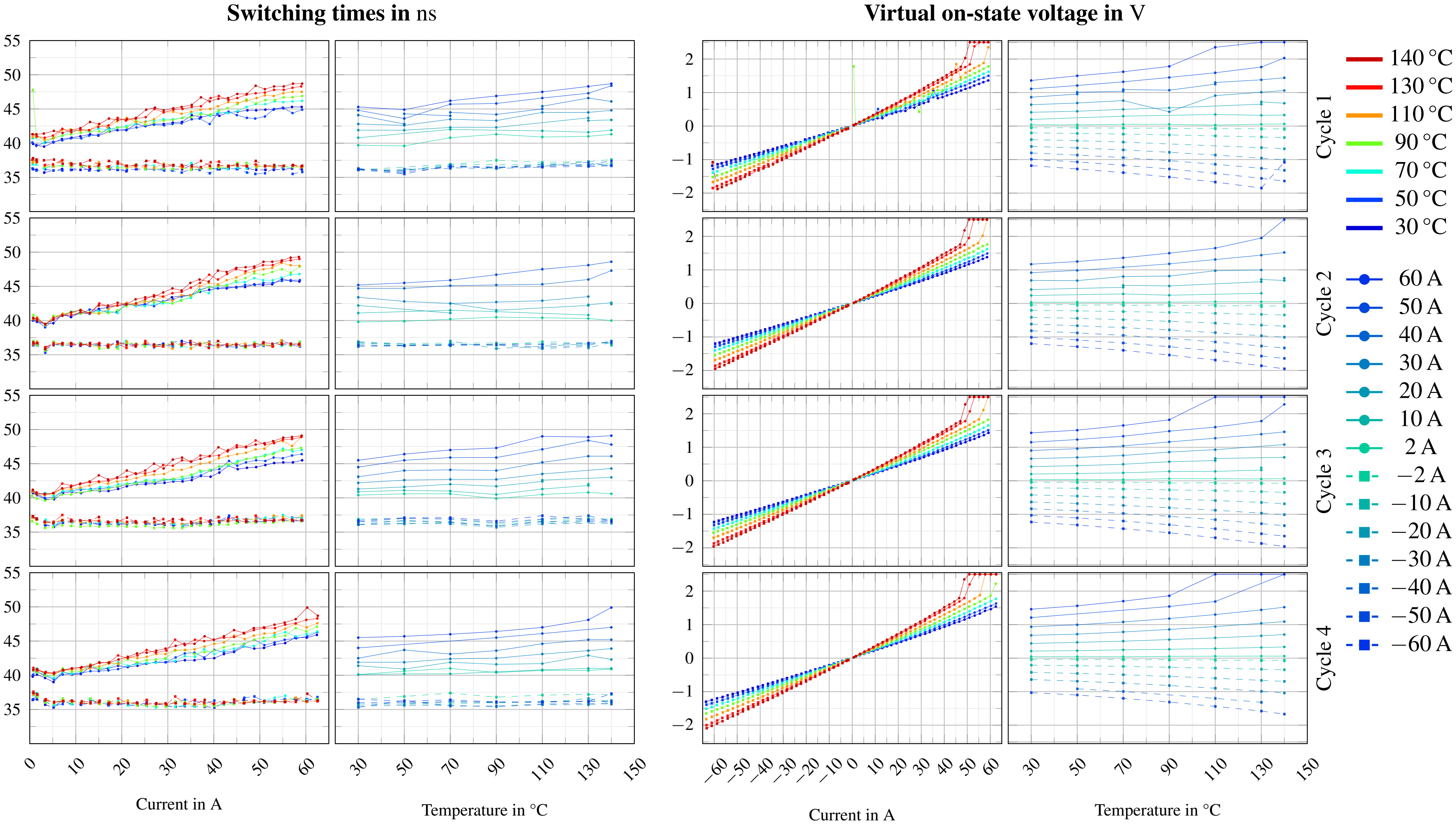


Figure L.3: TSEP measurements for module M_1, high side

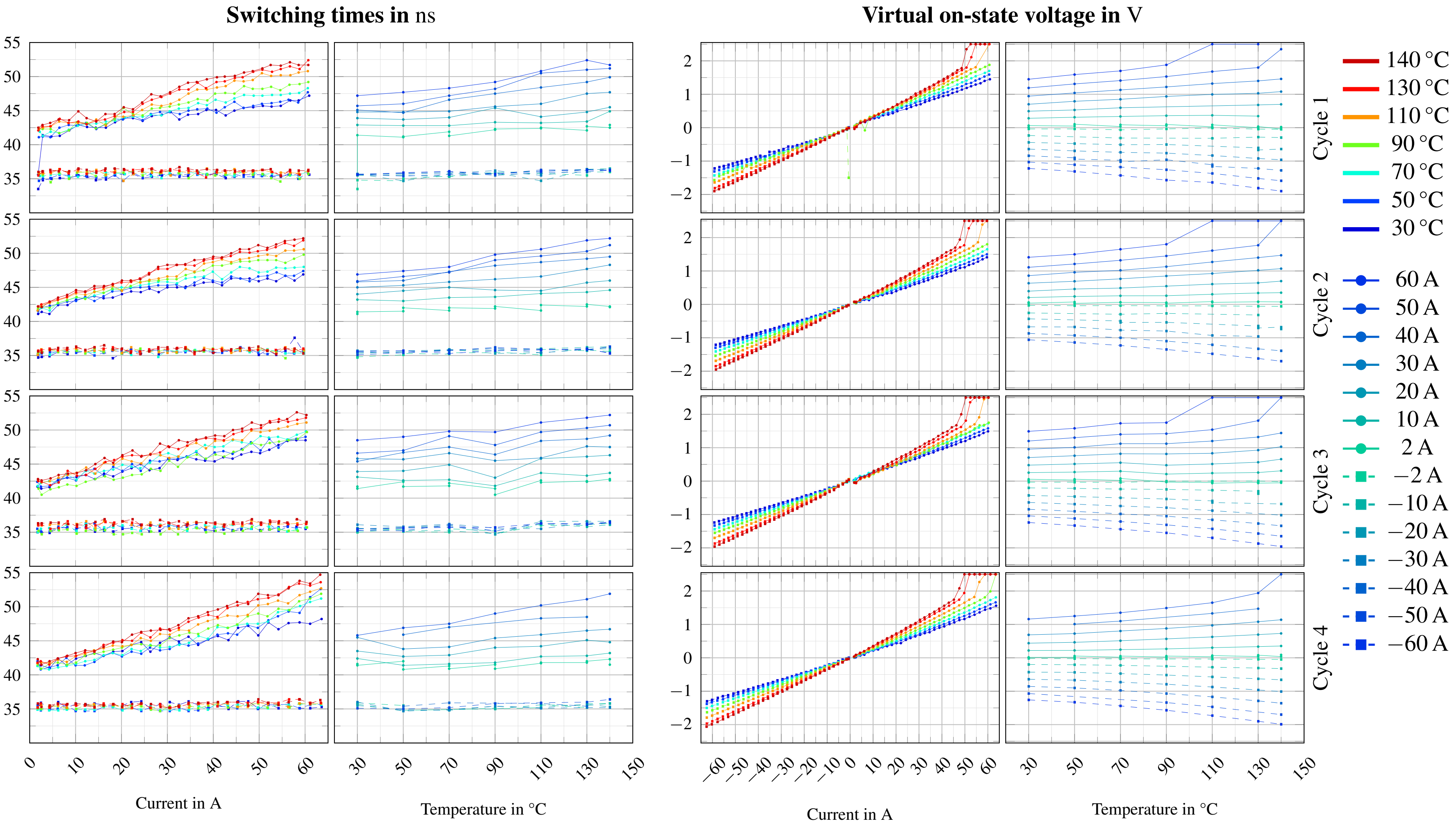


Figure L.4: TSEP measurements for module M_1, low side

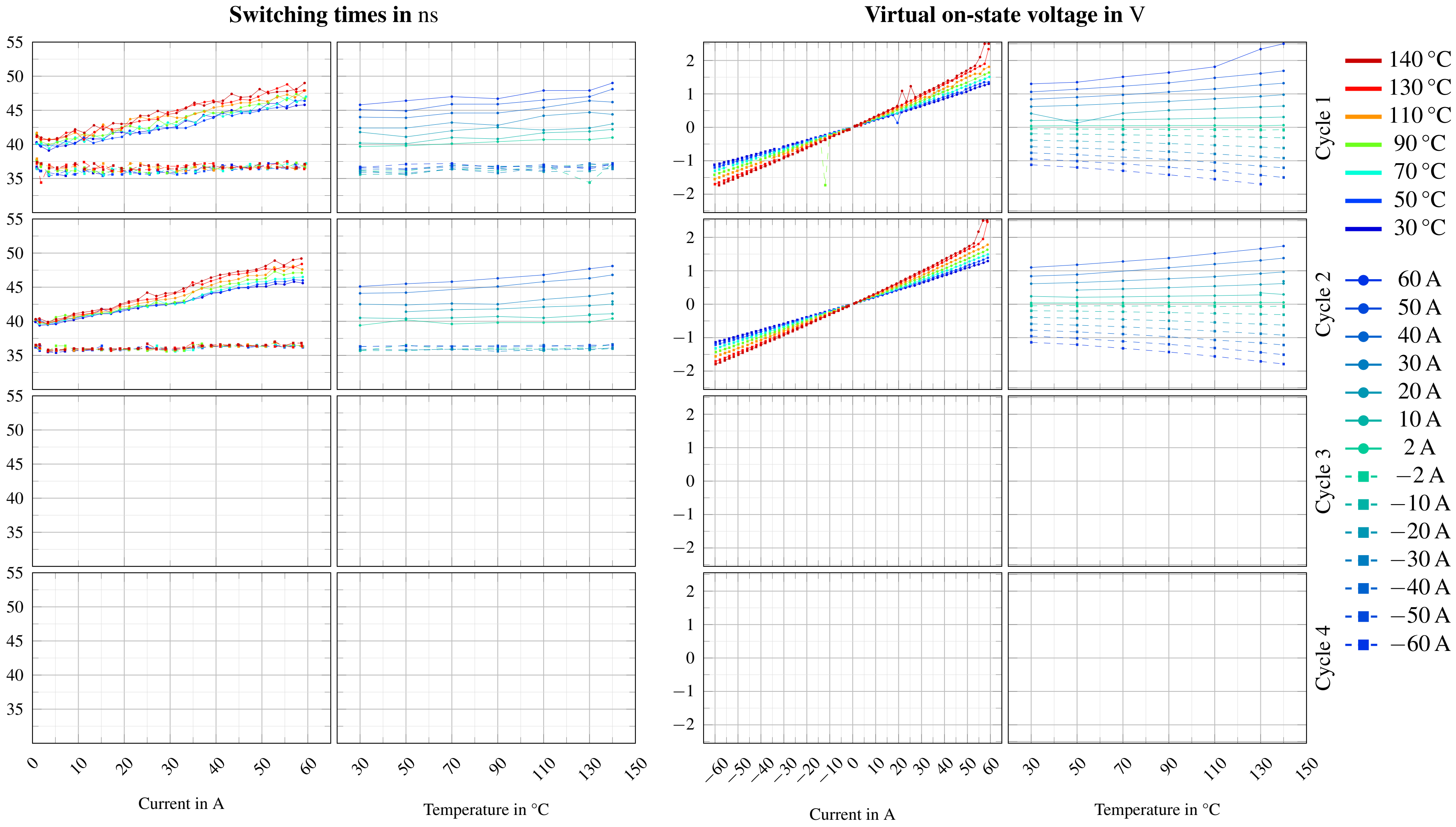


Figure L.5: TSEP measurements for module M_2, high side

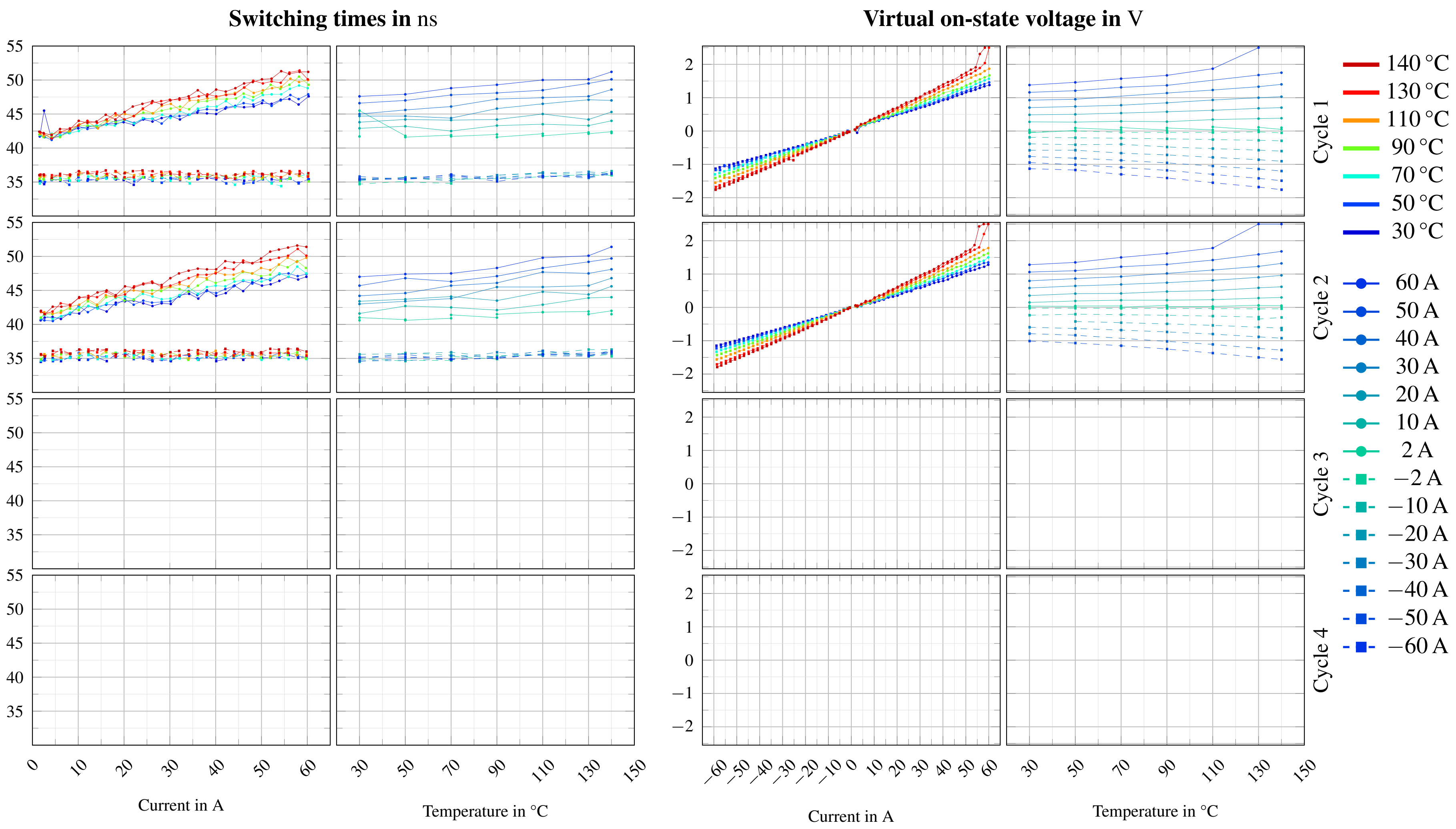


Figure L.6: TSEP measurements for module M_2, low side

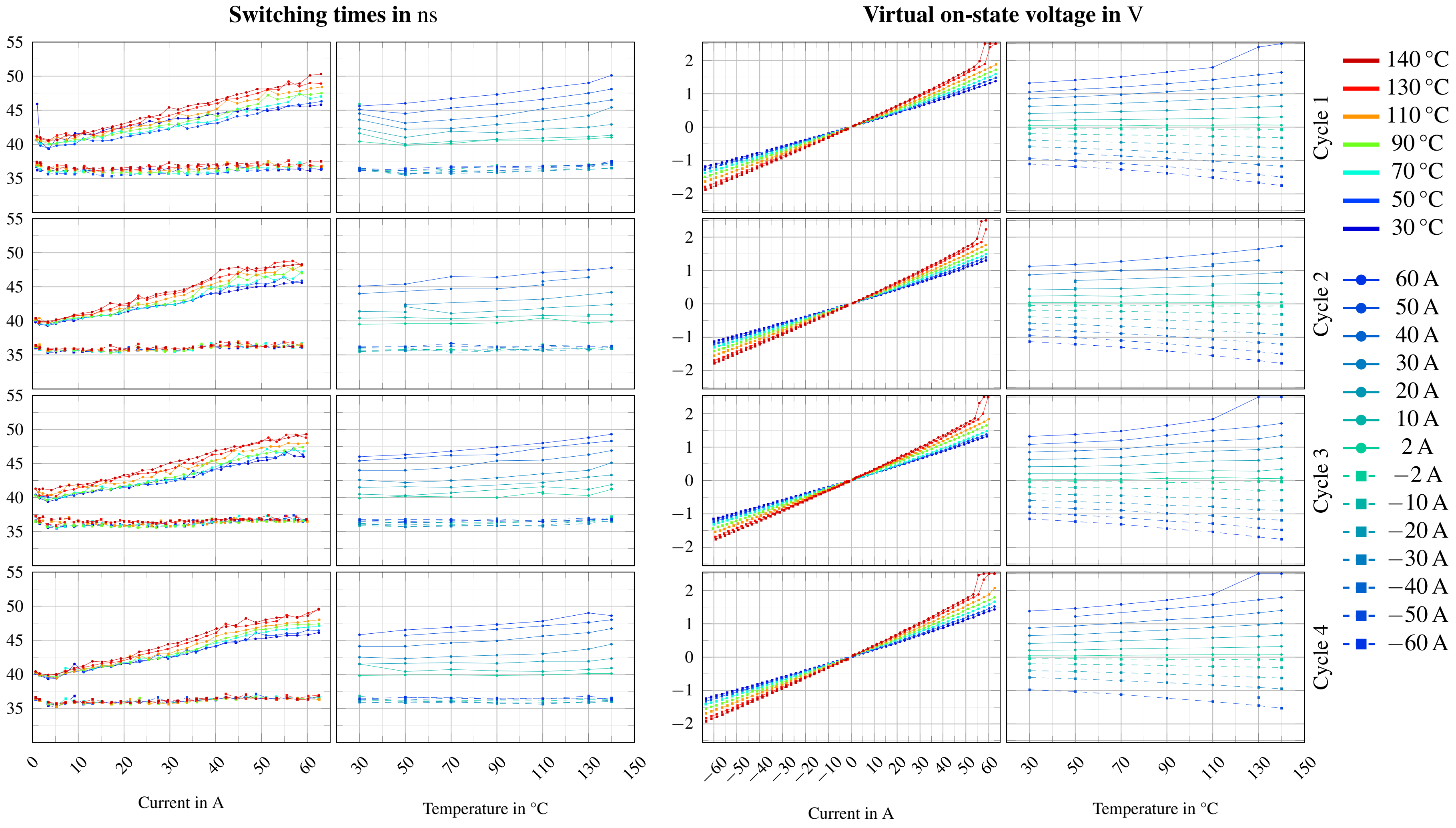


Figure L.7: TSEP measurements for module M_3, high side

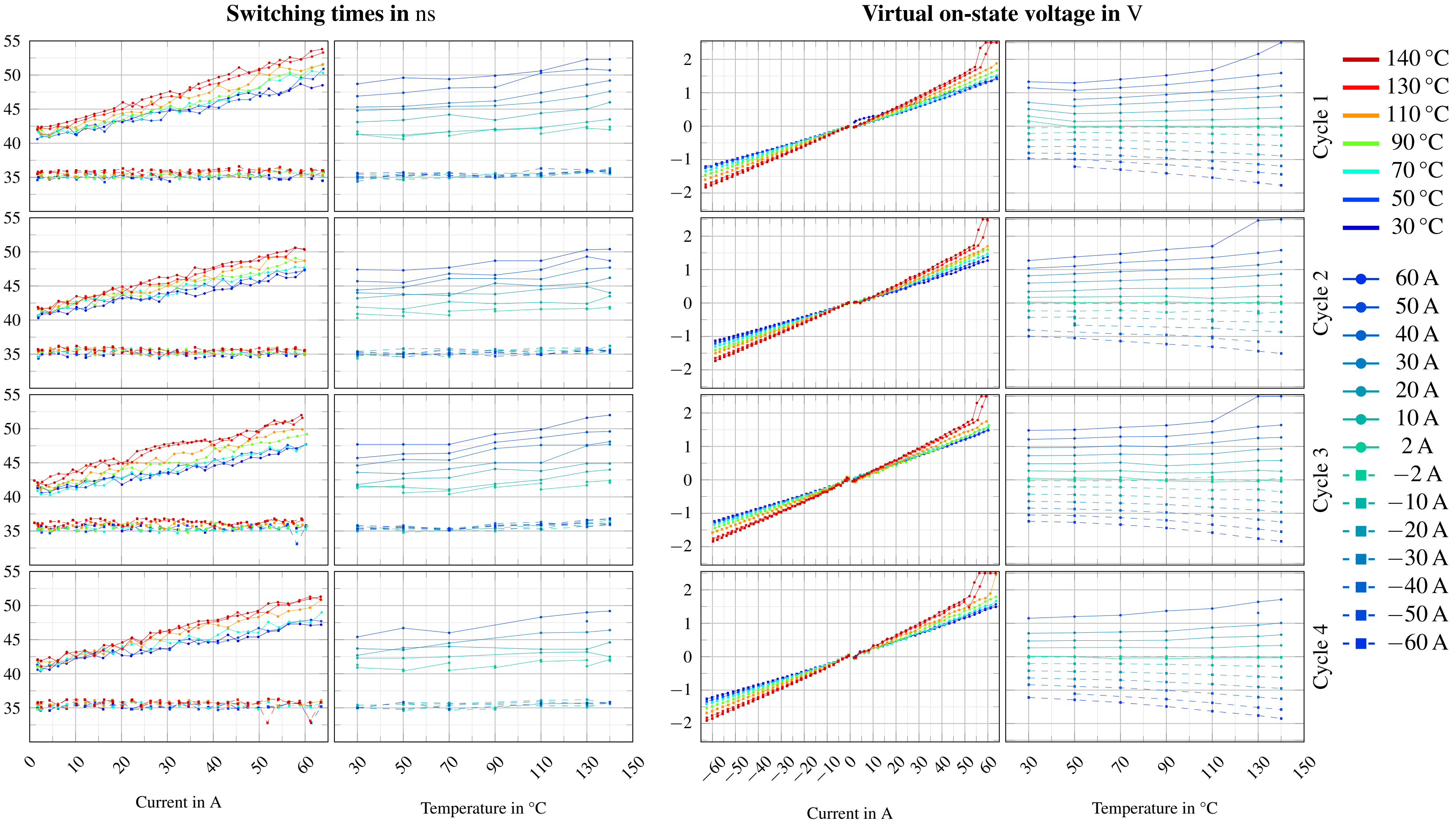


Figure L.8: TSEP measurements for module M_3, low side

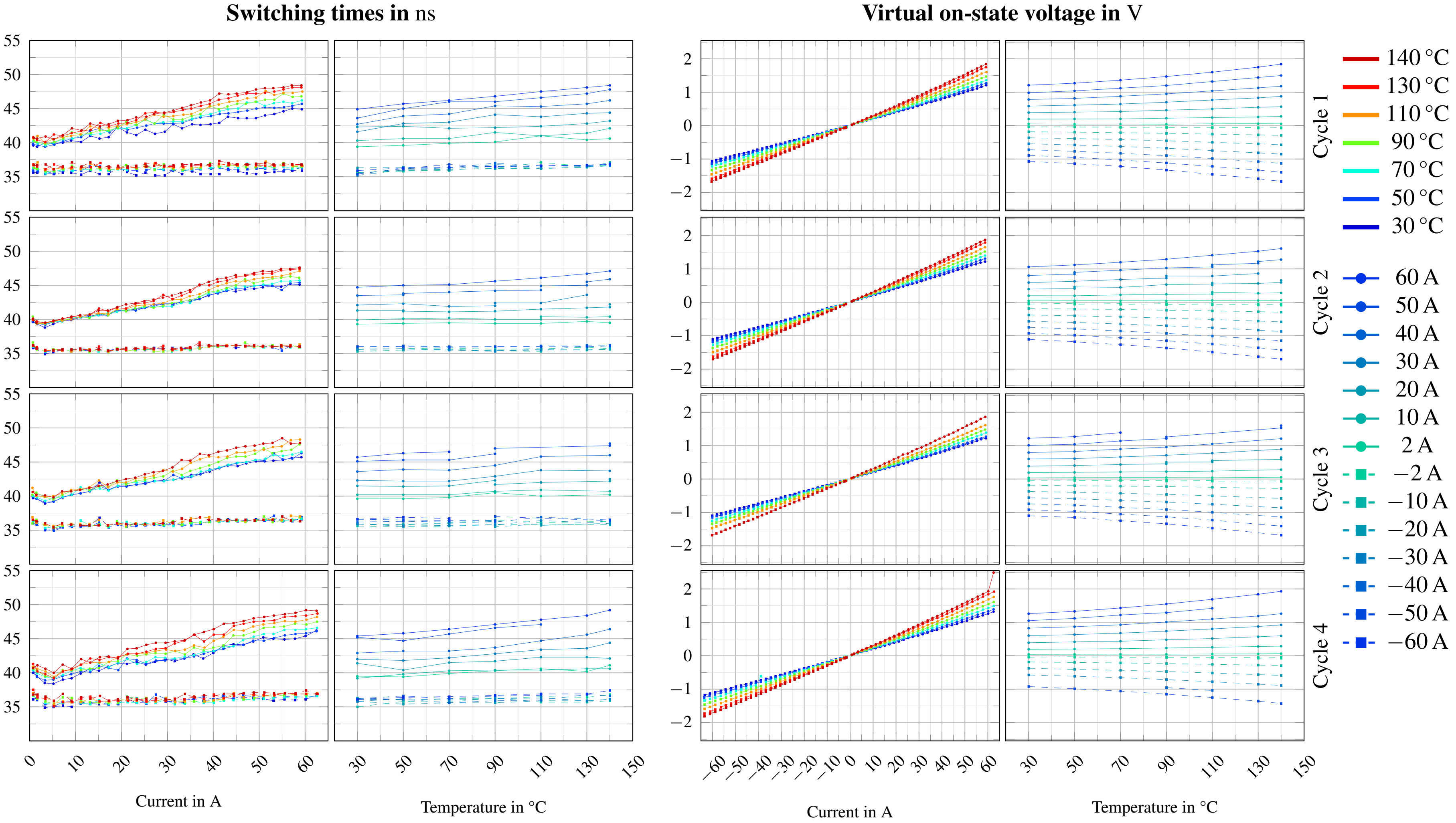


Figure L.9: TSEP measurements for module M_4, high side

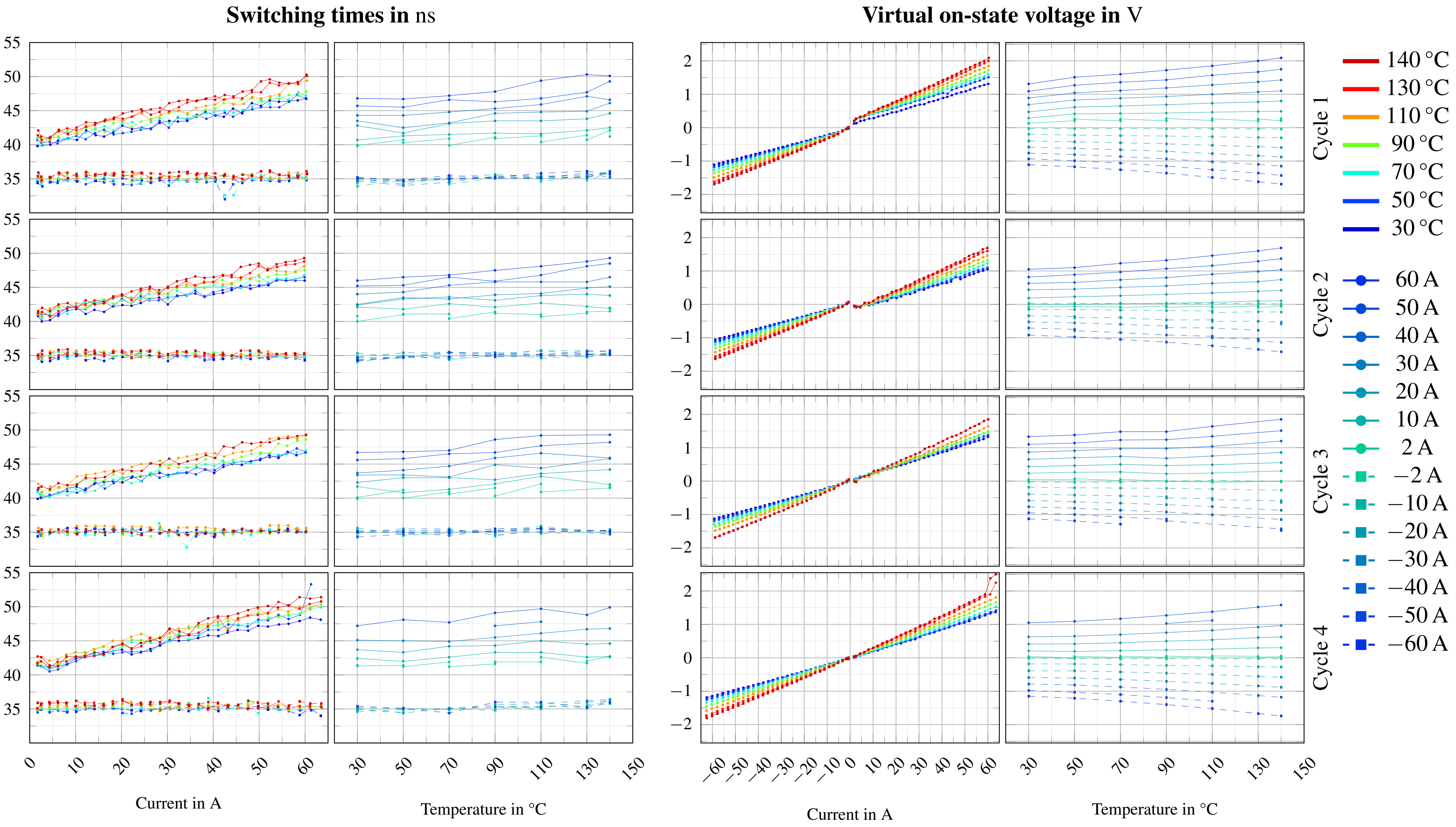


Figure L.10: TSEP measurements for module M_4, low side

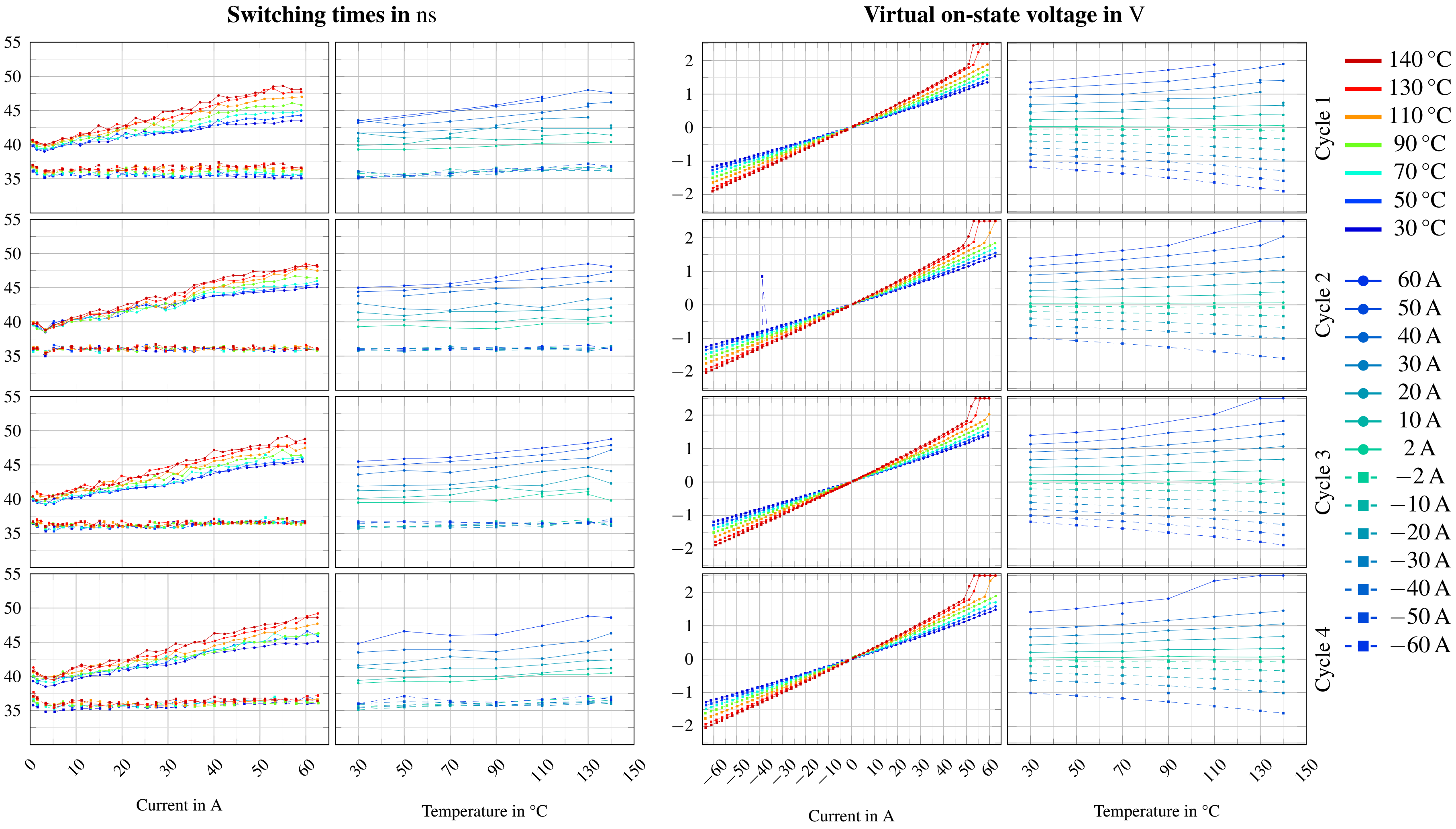


Figure L.11: TSEP measurements for module M_5, high side

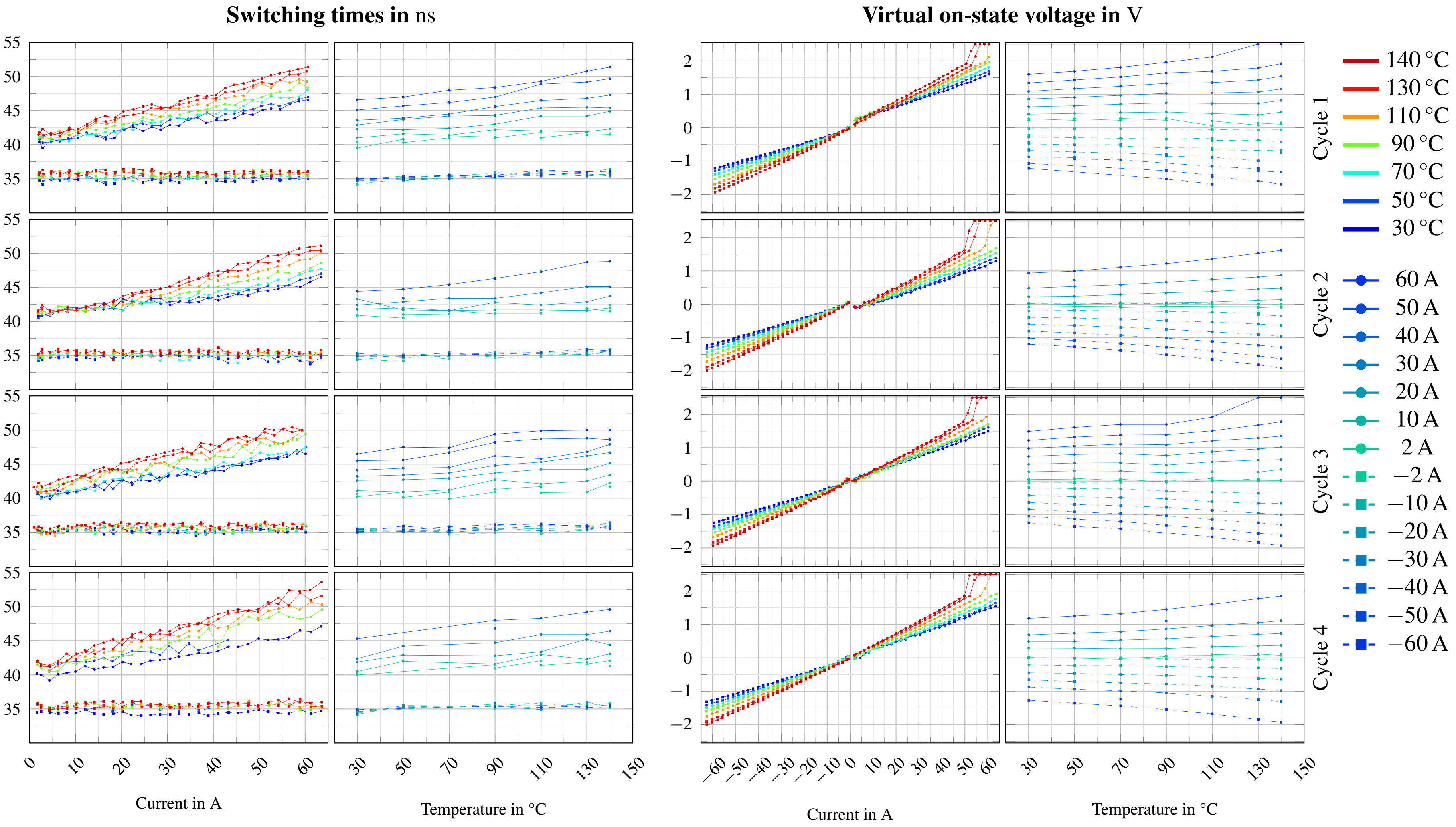


Figure L.12: TSEP measurements for module M_5, low side

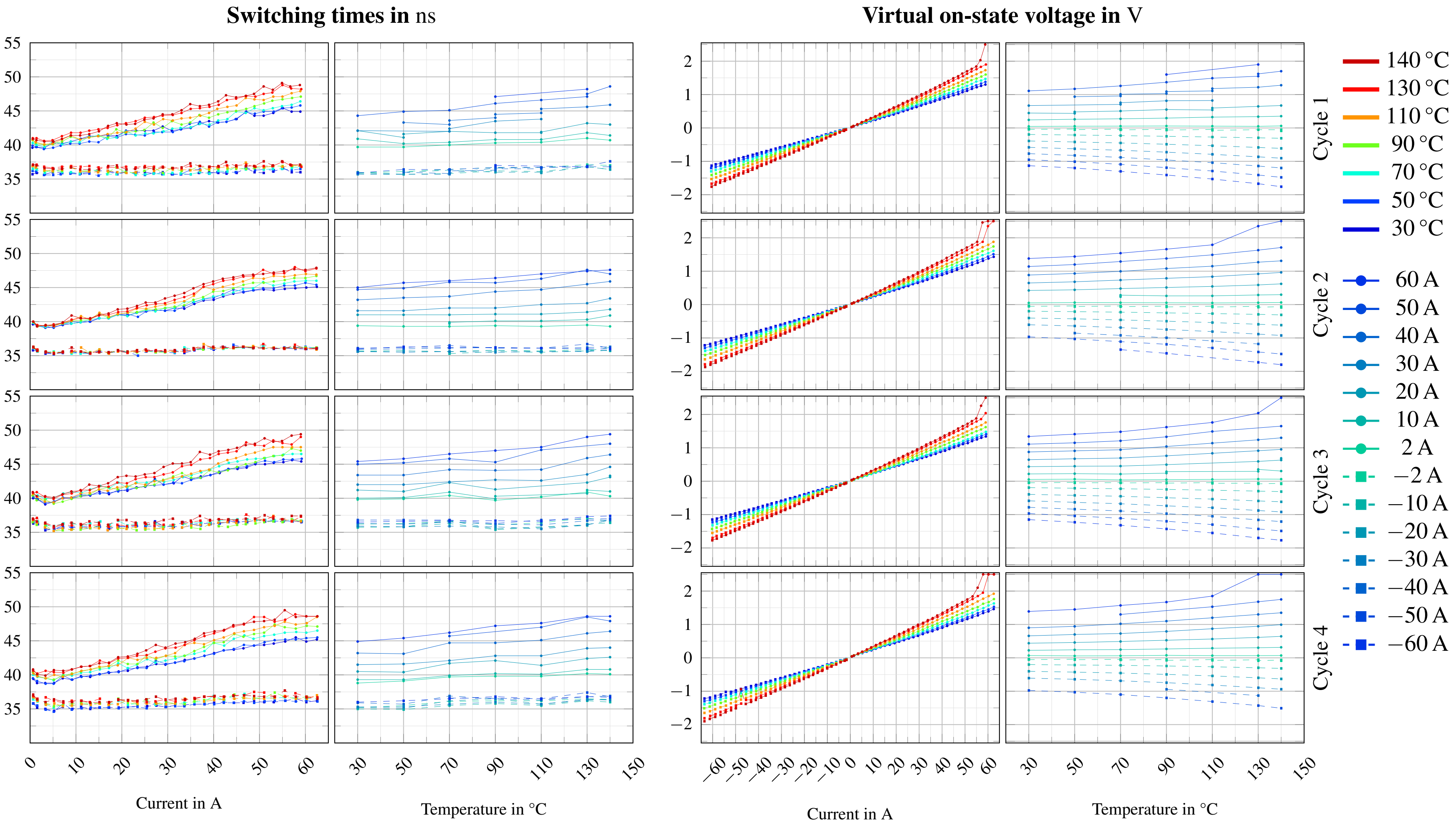


Figure L.13: TSEP measurements for module M_6, high side

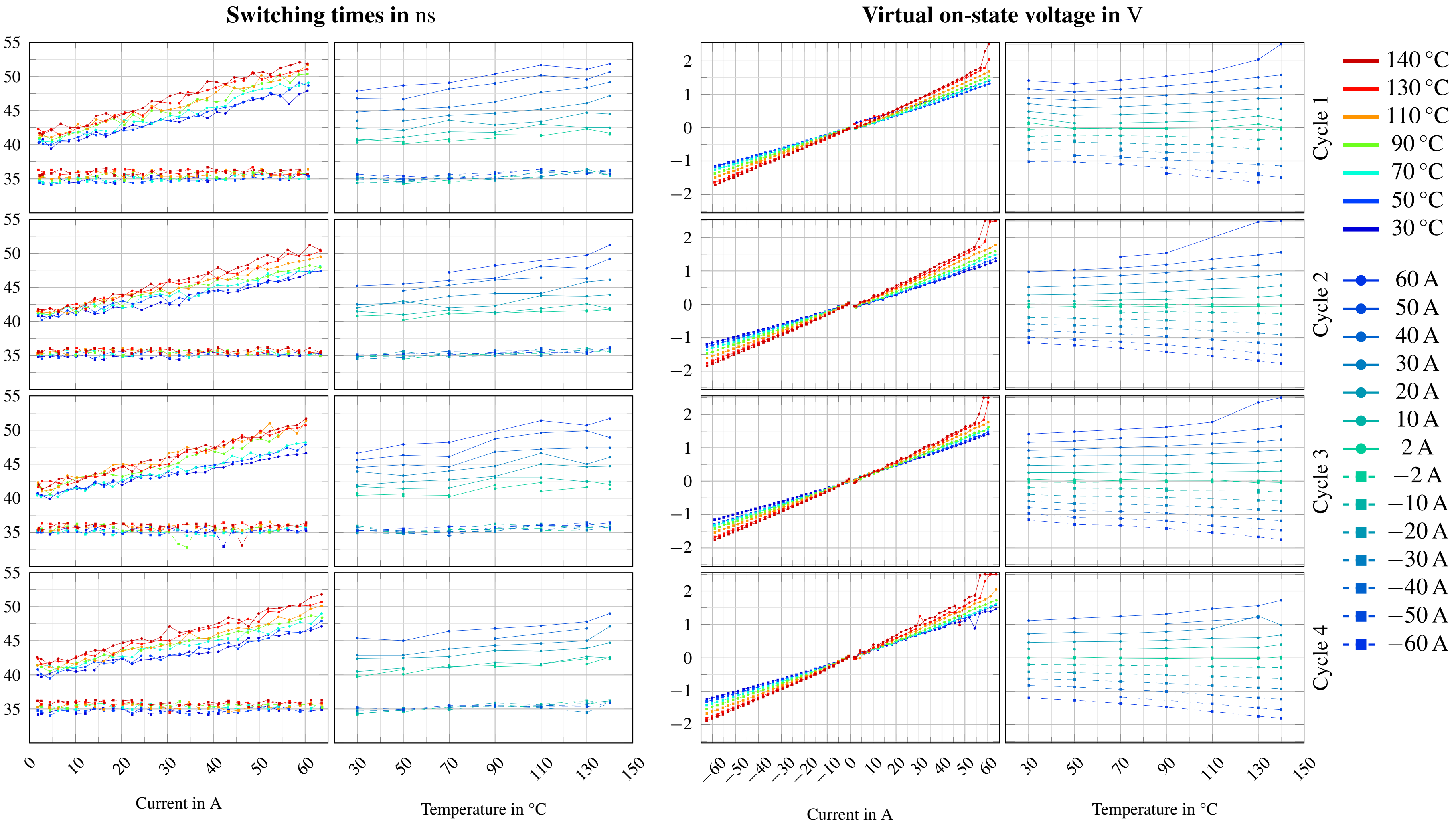


Figure L.14: TSEP measurements for module M_6, low side

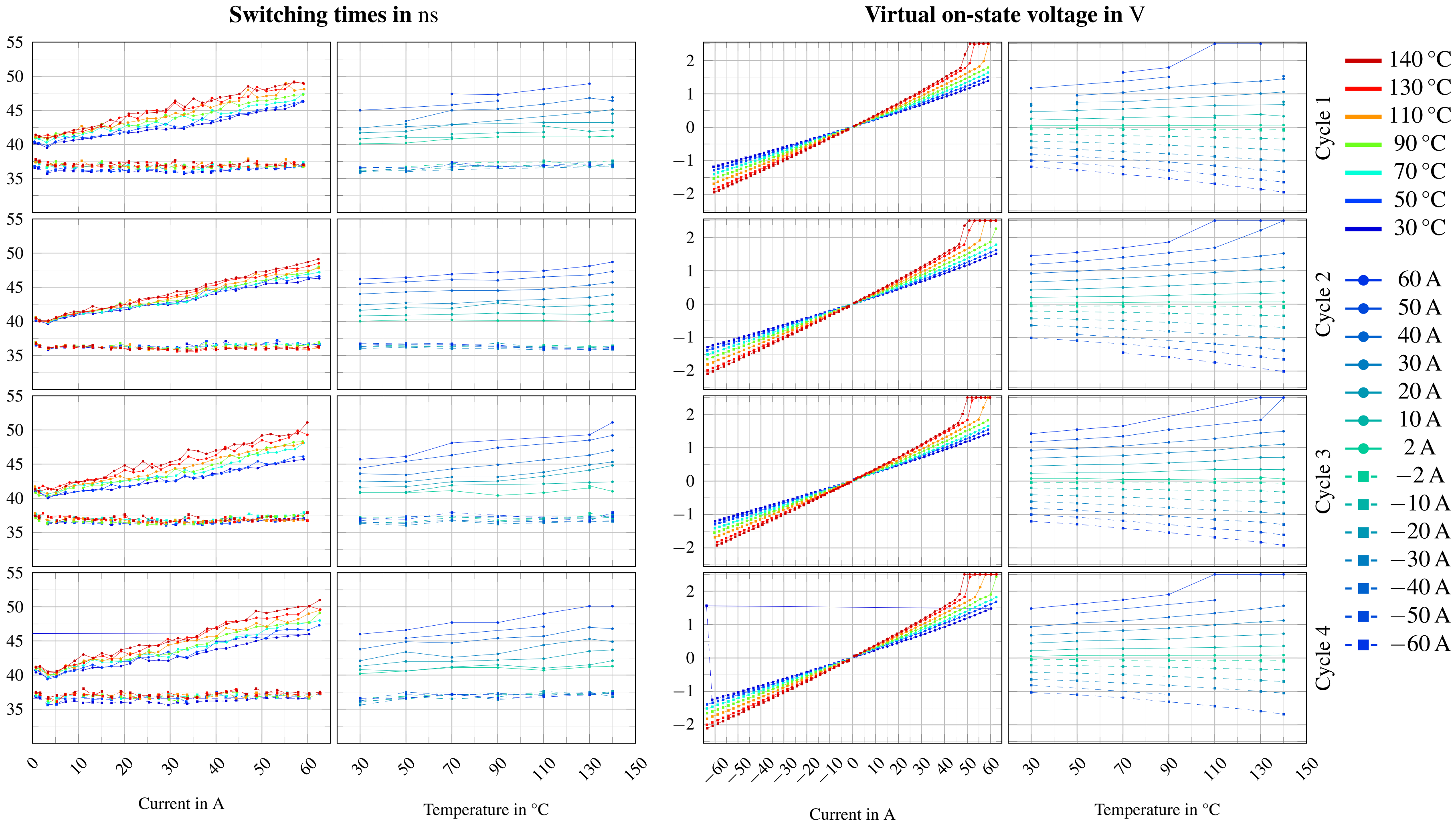


Figure L.15: TSEP measurements for module M_7, high side

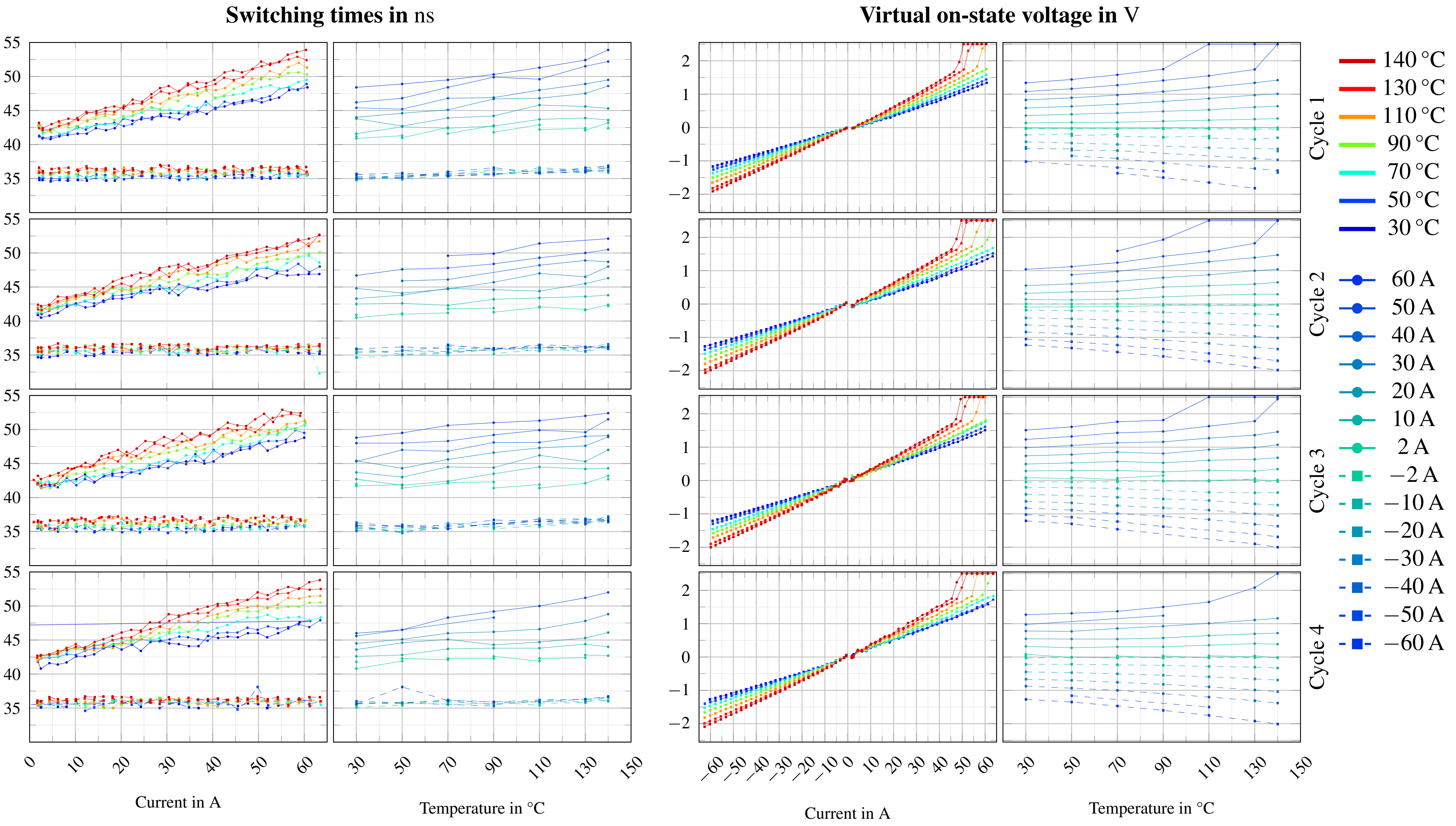


Figure L.16: TSEP measurements for module M_7, low side

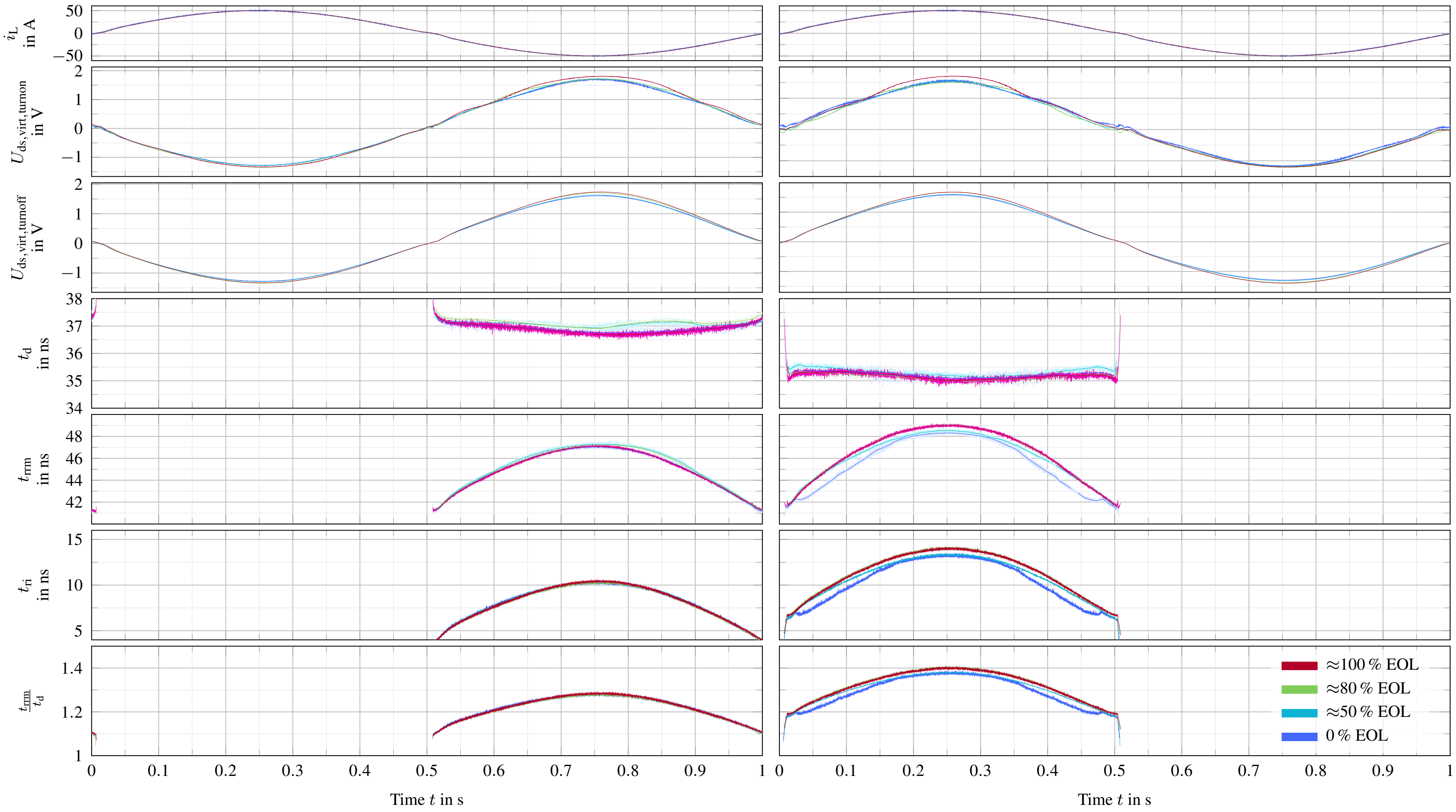
M Power-cycling tests - TSEP measurements (PWM)

Table M.1: Overview of the used modules

Context	Module	Description
Default module	M_0	Used for system development, testing, fundamental investigations
Accelerated aging tests	M_1	Aged PCT module; micro sectioning after 100 % EOL
	M_2	Aged PCT module; micro sectioning after 50 % EOL
	M_3	Aged PCT module
	M_4	Aged PCT module
	M_5	Reference PCT module; mounted during PCT, but no load applied
	M_6	Aged PCT module
	M_7	Aged PCT module

Table M.2: Timing of the TSEP analysis

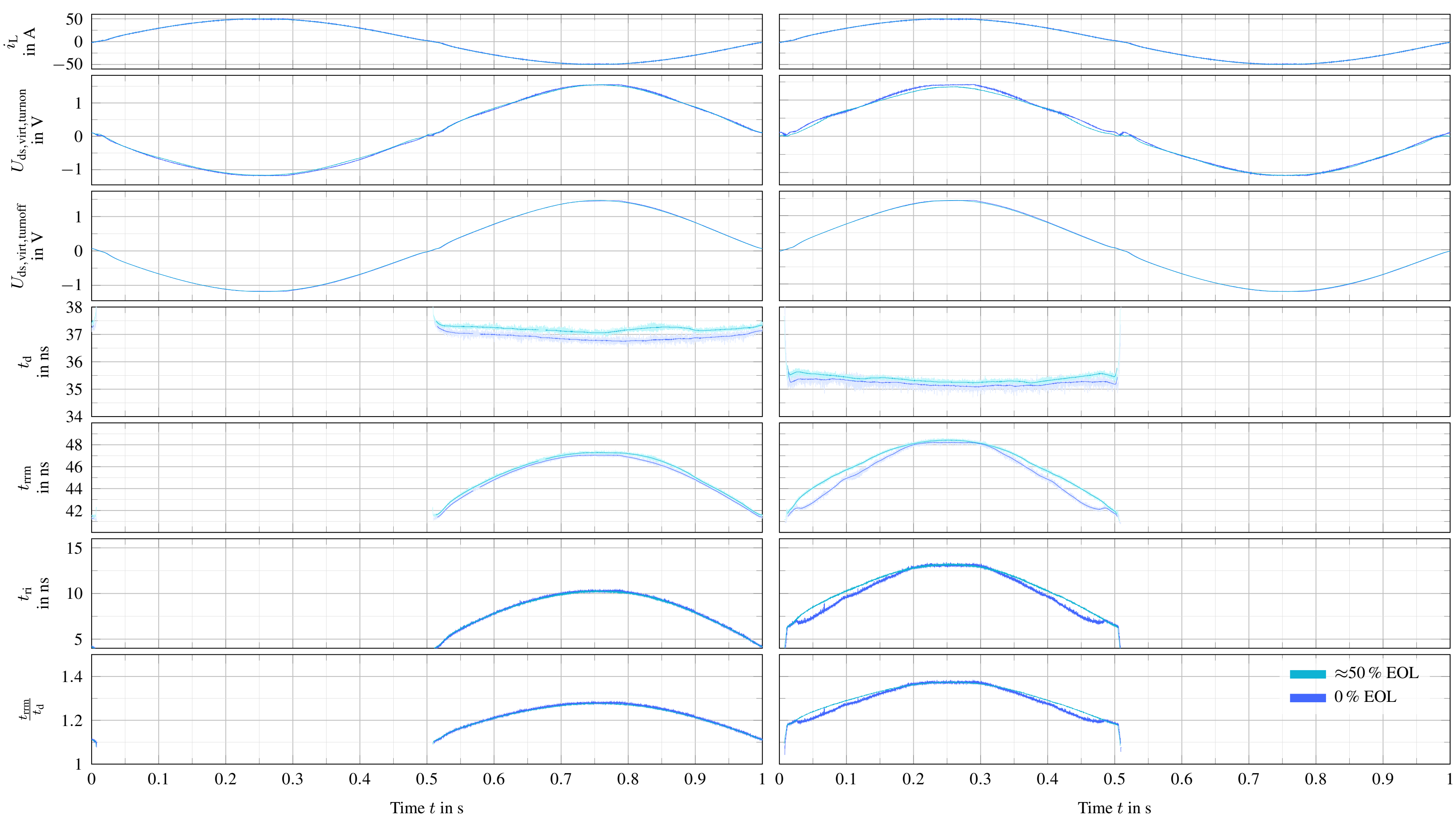
Approximately reached EOL	Cycles n_{cycle}	Comment
0 %	0	Initial measurement of the new modules
50 %	12 500	M_2 removed afterwards for use in another project
80 %	20 000	
100 %	24 077 to 30 718	Power-cycling continued until one EOL criterion was reached for every switch



(a) High-side switch

(b) Low-side switch

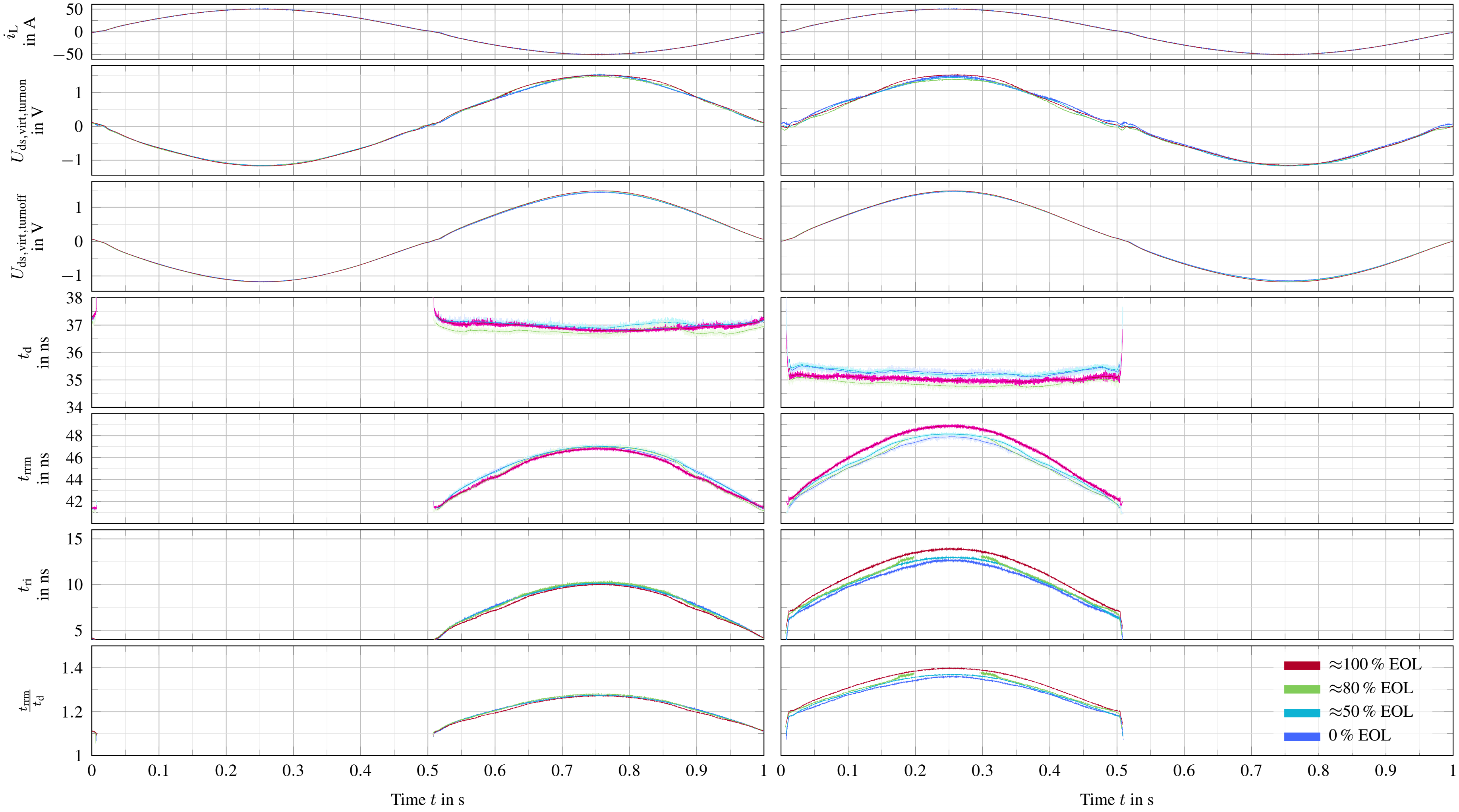
Figure M.1: TSEP measurements for module M_1



(a) High-side switch

(b) Low-side switch

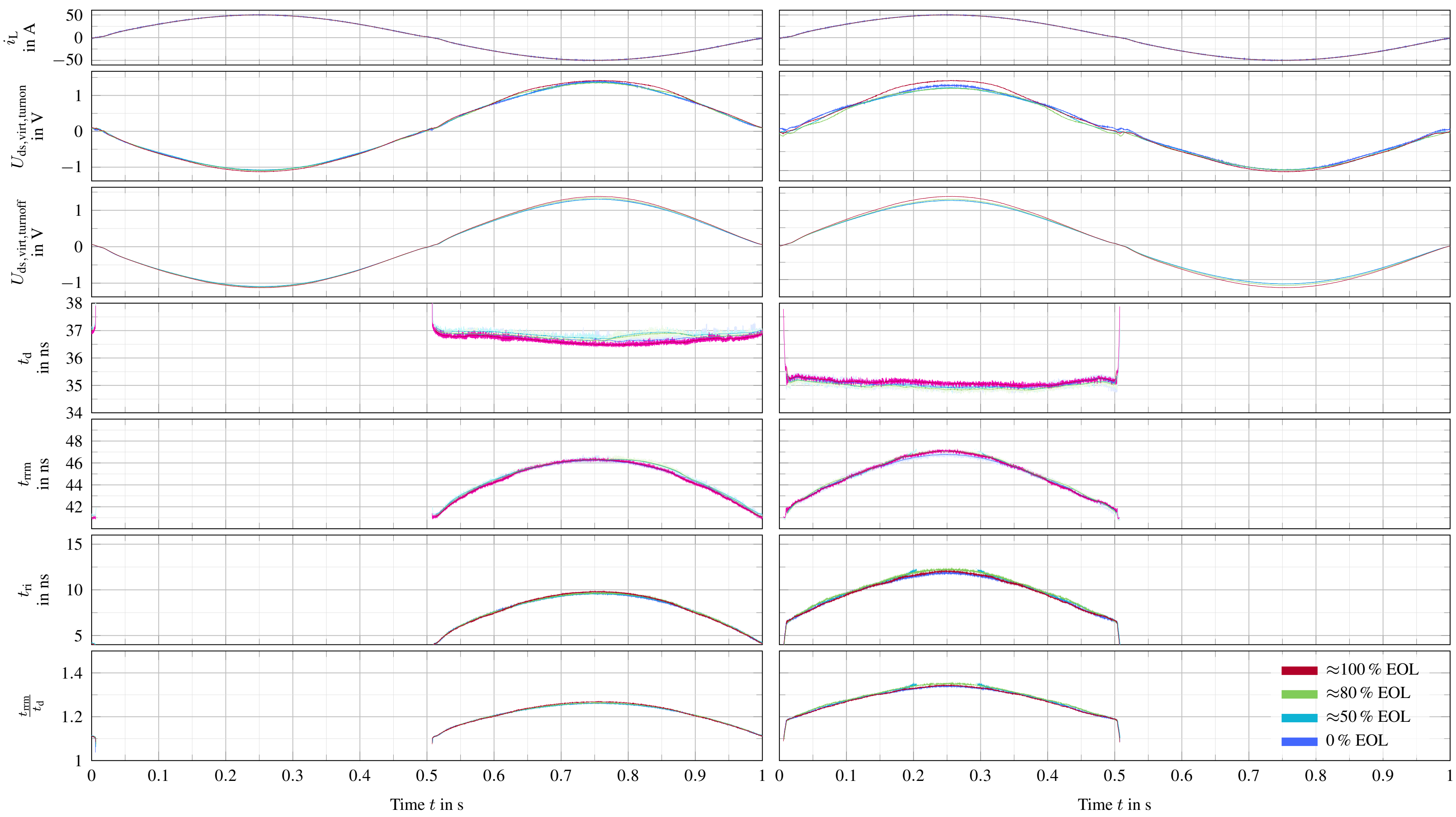
Figure M.2: TSEP measurements for module M_2



(a) High-side switch

(b) Low-side switch

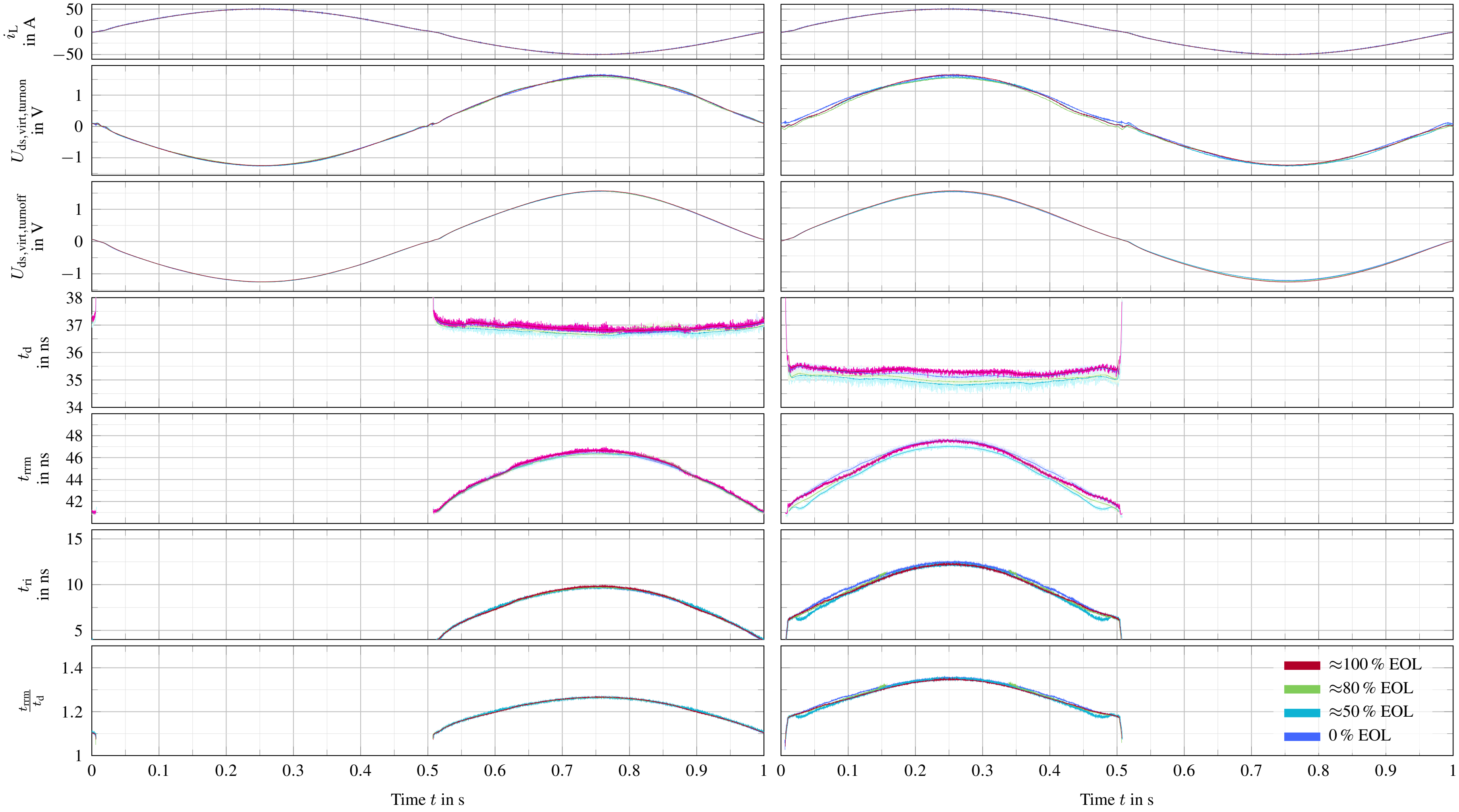
Figure M.3: TSEP measurements for module M_3



(a) High-side switch

(b) Low-side switch

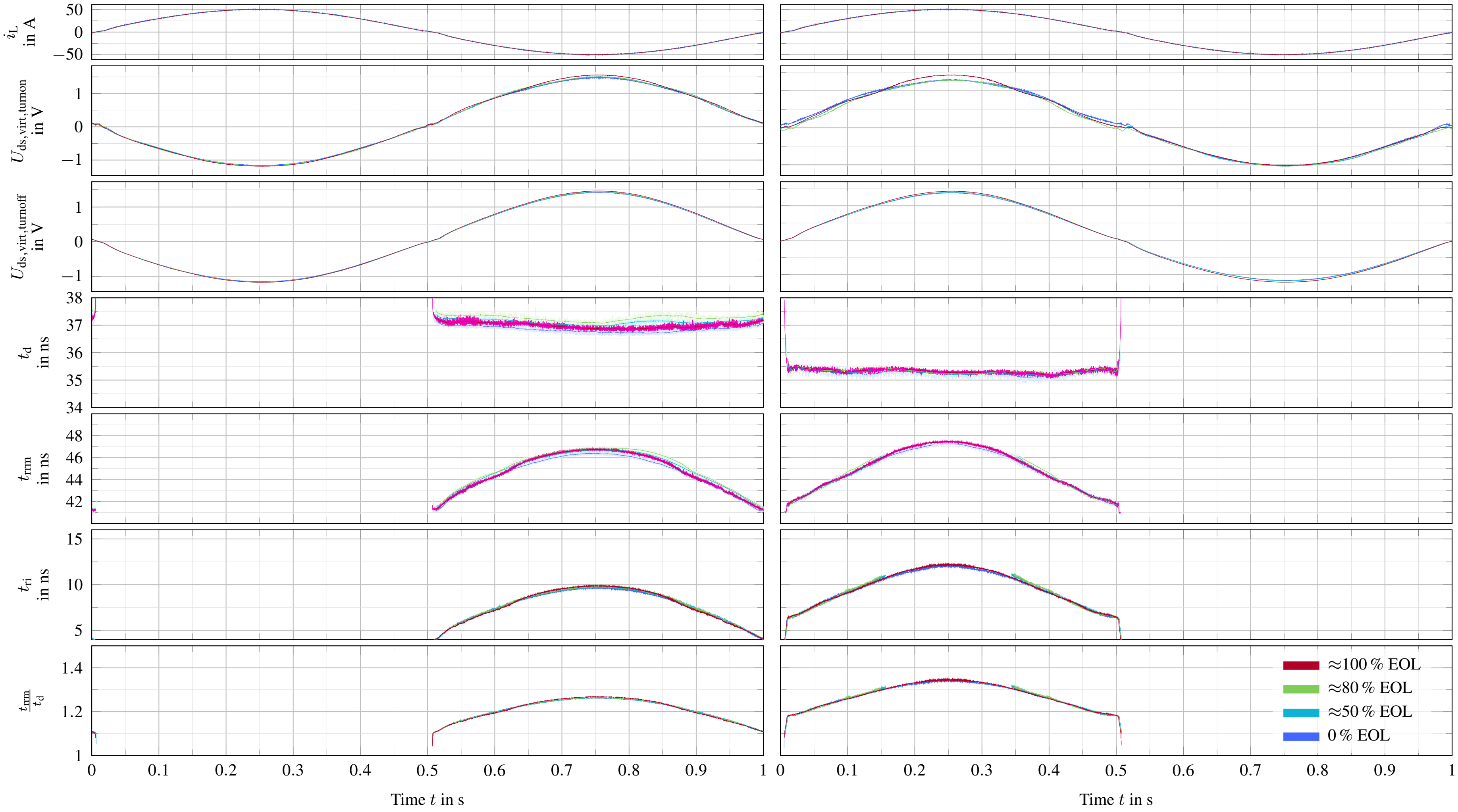
Figure M.4: TSEP measurements for module M_4



(a) High-side switch

(b) Low-side switch

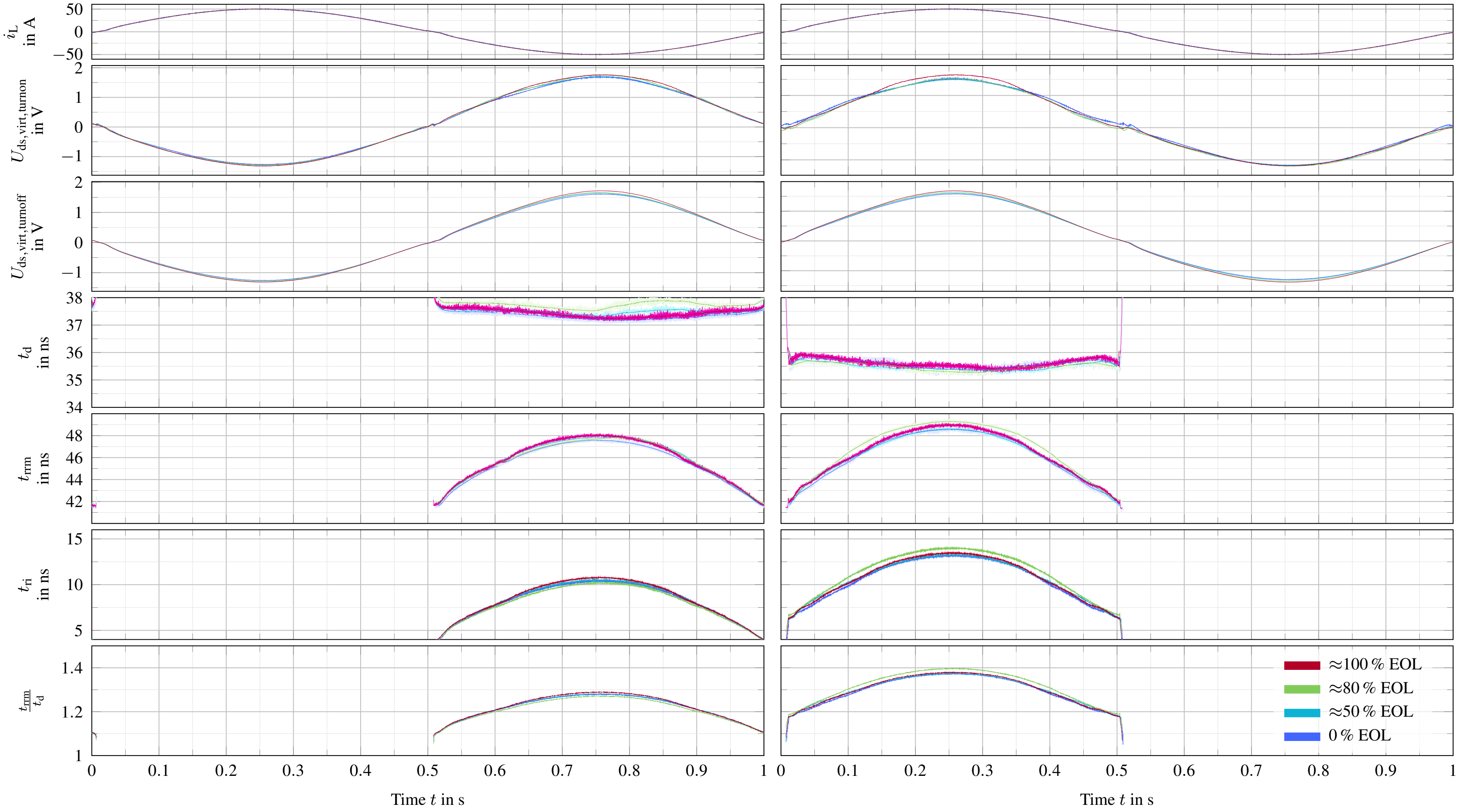
Figure M.5: TSEP measurements for module M_5



(a) High-side switch

(b) Low-side switch

Figure M.6: TSEP measurements for module M_6



(a) High-side switch

(b) Low-side switch

Figure M.7: TSEP measurements for module M_7

N Power-cycling tests - reference module

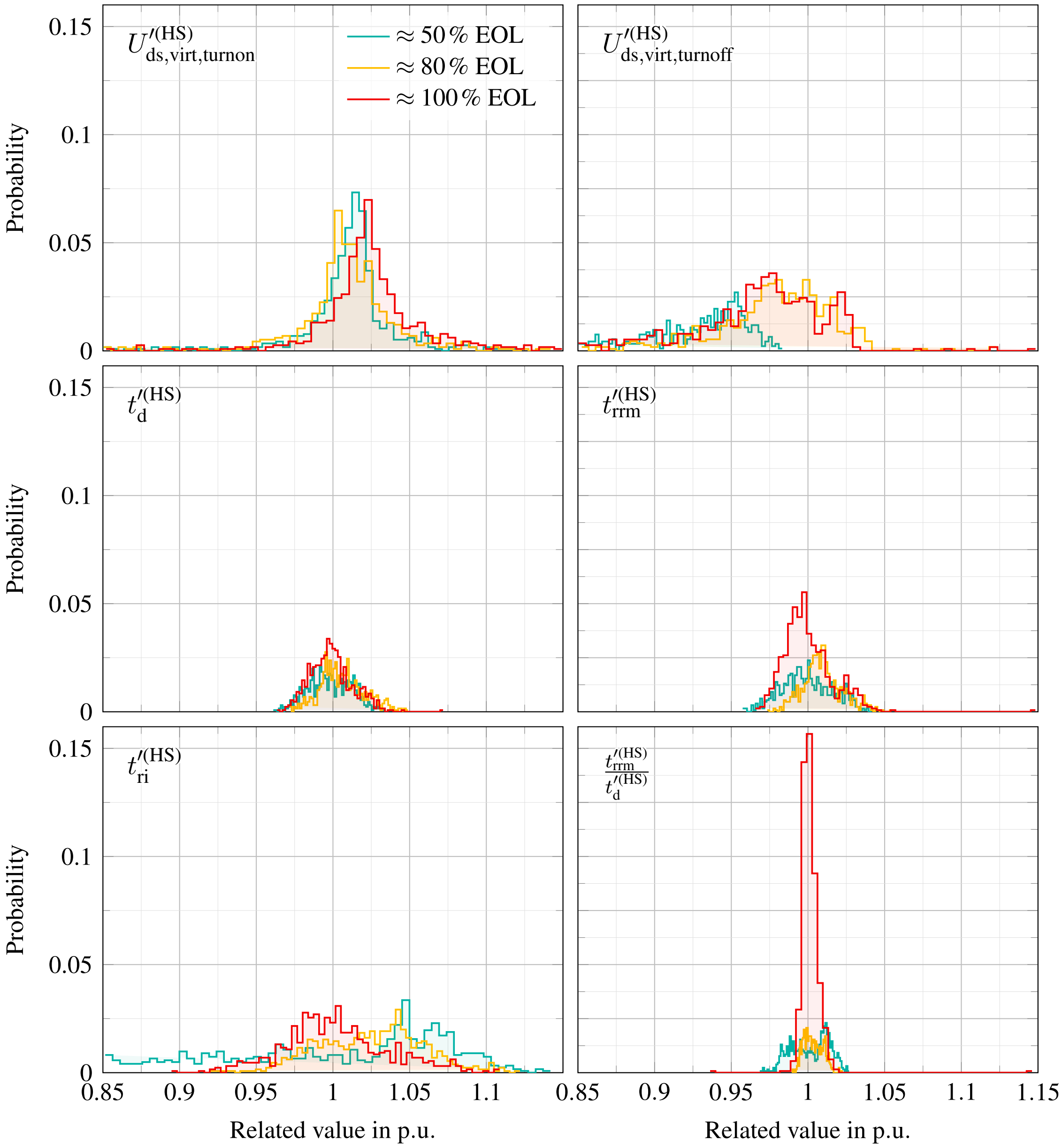


Figure N.1: Histograms of the normalized TSEPs of the reference module's high-side switches depending on the approximately reached EOL of the other (aged) modules

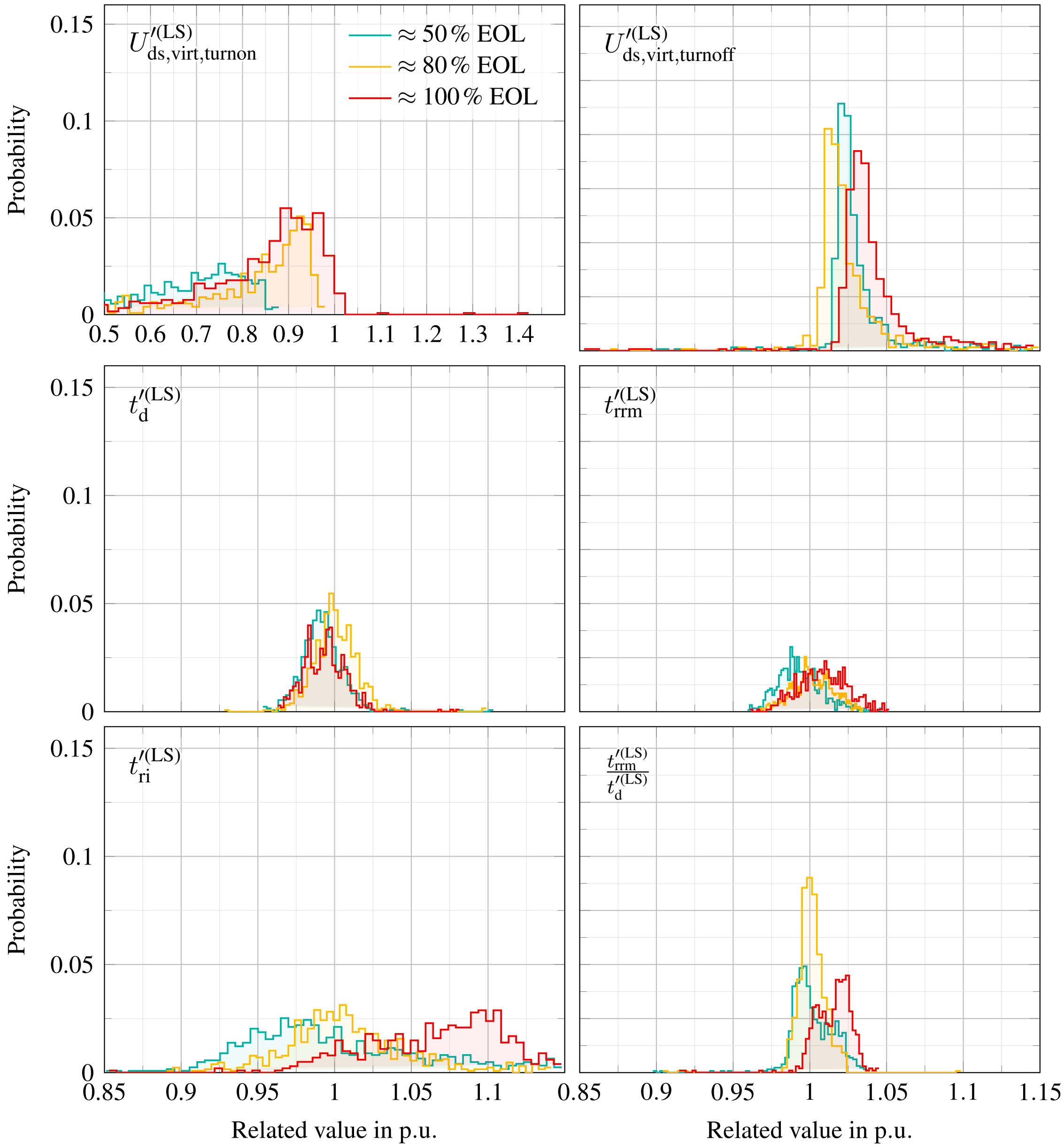


Figure N.2: Histograms of the normalized TSEPs of the reference module's low-side switches depending on the approximately reached EOL of the other (aged) modules; range of $U'_{ds,virt,turnon}$ extended to include its deviations

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Publications

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