## **RESEARCH ARTICLE**

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# Contacting a single nanometer-sized pinhole in the interfacial oxide of a poly-silicon on oxide (POLO) solar cell junction

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## Abstract

The electrical current through poly-Si on oxide (POLO) solar cells is mediated by tunneling and by nanometer-sized pinholes in the interfacial oxide. To distinguish the two processes, a POLO junction with a measured pinhole density of  $1 \times 10^7$  cm<sup>-2</sup> is contacted by different contact areas ranging from  $1 \ \mu m^2$  to  $2.5 \times 10^5 \ \mu m^2$ , and the temperature-dependent current-voltage curves are measured for the different devices. Model regressions to the measured curves, their temperature dependence, and the quantized value of contact resistances indicate average numbers of pinholes per device corresponding to the expected pinhole density. For the small contacts, the different transport processes can be studied separately, which facilitates further improvements in respect to the present-day POLO junctions. Single-pinhole transport is found for one of the contacts with an area of  $1 \ \mu m^2$ . Random telegraph noise observed for this device in the current-voltage characteristics shows a high sensitivity to single charges.

## KEYWORDS

pinhole transport, POLO junction, record energy conversion efficiency, silicon solar cell

## 1 | INTRODUCTION

One focus of recent research on solar cell optimization is the formation of carrier selective and passivating contacts. The principle of any carrier-selective contact is to maximize the blocking effect for minority carriers whilst minimizing the barrier of majority carriers.<sup>1,2</sup> One type of carrier selective junction is realized by a layer of highly doped poly-Si that is deposited on a thin interfacial oxide<sup>3-5</sup> called poly-Si on oxide (POLO) junction. This type of junction is utilized in a *p*-type Si solar cell with a record energy conversion efficiency of 26.1%.<sup>6</sup>

Transport through such POLO junctions is considered to happen via quantum mechanical tunneling and drift-diffusion transport through local disruptions in the oxide, called *pinholes*. Such local disruptions result from local variations of the oxide thickness with regions of vanishing or extremely thin oxide. While the existence of pinholes has been shown in structural investigations<sup>7</sup> and by analyzing transport measurements<sup>8,9</sup> of macroscopic devices, measurements of small devices containing only small number of pinholes are still missing. Measurements on small devices with few pinholes or no pin holes at all allow to study the different transport processes separately. In this way, the microscopic parameters governing transport can be studied directly, and the microscopic variations of these can be studied. Such knowledge is important in respect to improvements of present-day solar cells.

Here, we show measurements on sections of a POLO sample that are small enough to include a countable number of pinholes. We

This is an open access article under the terms of the Creative Commons Attribution-NonCommercial-NoDerivs License, which permits use and distribution in any medium, provided the original work is properly cited, the use is non-commercial and no modifications or adaptations are made. © 2021 The Authors. Progress in Photovoltaics: Research and Applications published by John Wiley & Sons Ltd. analyze current-voltage measurements on these contacted sample sections with a transport model for POLO junctions with the aim of discriminating between the above-mentioned current transport mechanisms and identifying the main factors of influence on the local transport.

#### 2 **EXPERIMENTAL**

To prepare the sample, a 300- $\mu$ m-thick, 200- $\Omega$ cm resistive *p*-type FZ sample is oxidized to a nominal oxide thickness of 2.2 nm (as measured by spectral ellipsometry), and a 225-nm-thick intrinsic poly-Si layer is deposited on both sides of the sample by low pressure chemical vapor deposition. Ex situ doping is performed by B ion implantation with a dose of  $3 \times 10^{15}$  cm<sup>-3</sup>. The POLO junctions are formed upon high temperature annealing for 80 min at 1035°C in oxygen ambient. During this step, B is distributed and activated within the Si layer that crystallizes with grain sizes of  $\sim 20$  nm size (as determined by X-ray diffraction).<sup>10</sup> Furthermore, the interfacial oxide is structurally altered, for example, locally thinned, and pinholes in the interfacial oxide are formed. Also, a certain in-diffusion of B from the poly-Si into the c-Si occurs-as verified by electrochemical capacitance voltage (ECV) and secondary ion mass spectroscopy (SIMS) measurements. The sample preparation to that point is similar to that of the record cell reported by Haase et al.<sup>6</sup> where process details are listed. The passivation quality of this POLO junction enables effective lifetimes of 3500 µs at an injection level of 10<sup>15</sup> cm<sup>-3</sup>. Selective etching of a co-processed sample using the etching method reported in Tetzlaff et al.<sup>7</sup> reveals an areal density of pinholes of approximately  $1 \times 10^7$  cm<sup>-2</sup>.

For the electrical transport measurements, contacts have to be formed on the front and backside of the sample. An ohmic back contact is ensured by the thermally evaporated and afterwards laser-fired Al coating on the full area of the backside. Figure 1A shows a schematic image of the sample highlighting the different layer materials of the front junction. The expected pinholes are shown as areas with modified oxide thickness. To study transport through a small number of pinholes, the processing of contacts with small areas is needed. To form such small contacts and to be able to connect bonding wires to these contacts, a special technology is applied following similar steps as in previous studies.<sup>11-13</sup> A schematic picture of a finalized device is shown in Figure 1B. As a first step, square contacts with different areas (1 µm<sup>2</sup>, 4 µm<sup>2</sup>, 25 µm<sup>2</sup>, 100 µm<sup>2</sup>, 10,000 µm<sup>2</sup>, and 250,000 µm<sup>2</sup>) are defined using electron-beam lithography (EBL). Before evaporation of the contact metals (30-nm Ti and 40-nm Au, or 7-nm Cr and 60-nm Au), an HF dip is performed to remove the native oxide at the surface of the sample. A standard lift-off process is employed to get rid of all metal with the exception of the contacts areas. These areas serve as etch masks in the following  $SF_6$  reactive ion etching step which etches a depth of 600 nm leaving free standing pillars underneath the metal contacts. In Figure 1C,D, two such pillars are shown. One sees that the etching process is not fully anisotropic, leaving the faces of the pillars with an angle. From SEM images as shown in Figure 1, one sees that the pillars have the shape of a cut-off pyramid. The measured junction section is thus approximately 400 nm smaller on each side than the nominal value. To be able to contact these pillars separately, an insulating layer has to be formed. Therefore, the space between the pillars is filled with a negative photo resist of low viscosity that results in an insoluble dielectric film after heating at 180°C. To uncover the photo-resist-coated metal contacts, an oxygen



**FIGURE 1** (A) Sketch of a sample cross section showing the different layer materials of the front junction and the pinholes in the interfacial oxide. (B) Sketch of a sample cross section for one pillar after complete processing of a front contact. (C, D) SEM images of two front contacts with areas  $(2 \times 2) \mu m^2$  and  $(5 \times 5) \,\mu\text{m}^2$  and the accordingly etched pillars

plasma etching step is used. In a final EBL step, pads (10-nm Cr and 190-nm Au) with dimensions  $100 \times 100 \ \mu\text{m}^2$  are defined on top of all pillars in order to have large enough contact areas for wire bonding.

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The finished samples are measured in a two-terminal setup with one contact to the fully metallized base and one contact to the metallized pad area on the front side. DC measurements are performed with a Keithley 2400 source meter and an Ithaco Model 1211 current preamplifier. The applied voltage is swept in the range from -0.1 V to 0.1 V at temperatures varying from  $-20^{\circ}$ C to  $50^{\circ}$ C.

## 3 | RESULTS AND DISCUSSION

A selection of the measured current-voltage curves is given in Figure 2A in a logarithmic scale versus applied voltage for the different pillar dimensions. One observes the expected scaling of absolute current with pillar area. For the smaller areas, the observed noise increases. In order to discuss the measured current-voltage (IV) characteristics in more detail, Figure 2B-G shows IV curves for five different pillar areas and six different pillars at different





temperatures. The two pillars with areas of 1  $\mu$ m<sup>2</sup> show very noisy IV curves (Figure 2F,G), but also very different temperature dependences already hinting towards different transport mechanisms being dominant in the two samples. The sample with an area of 4  $\mu\text{m}^2$  shows a clear increase of junction current with increasing temperature as expected for samples with dominating tunneling transport at Schottky contacts.<sup>8,9</sup> The main temperature dependence stems then from the influence of the energy difference between the valence band edge at the oxide/c-Si interface and the Fermi level. The IV curves for the different temperatures are all nonlinear. The sample with 25  $\mu$ m<sup>2</sup> shows a similar but less pronounced nonlinearity and a weaker temperature dependence in which the conductance decreases with increasing temperature. In contrast, samples with larger pillar areas show pretty linear IV characteristics, and their conductance decreases strongly with increasing temperature. This different electrical behavior hints towards less importance of quantum-mechanical tunneling and dominance of pinhole transport where the temperature dependence is mainly governed by the influence of lattice scattering, that is, phonon scattering, in drift-diffusion transport.

From the pinhole-density of  $1 \times 10^7$  cm<sup>-2</sup>, determined by counting etch-pits, only a small number of two to three pinholes is expected in the 25-µm<sup>2</sup> pillars on average and therefore no clear dominance of tunneling or pinhole transport should be seen. In the 100-µm<sup>2</sup> pillars, around 10 pinholes per pillar are expected and thus a dominance of pinholes in the transport measurements on these samples. This expectation is met with the observation, that for these samples, the temperature dependence of junction currents shows an opposite trend in comparison with the smaller samples.

Table 1 lists the different small contact areas studied and the number of pinholes per pad expected from the pinhole-density of  $1 \times 10^7$  cm<sup>-2</sup>. It also lists the number of devices per contact area studied. For the smallest pillars, 18 pads were investigated to be able to observe any pinhole transport since on average; for example, only 0.1 pinholes are expected for contacts with areas of 1  $\mu$ m<sup>2</sup>. In contrast, for the 100- $\mu$ m<sup>2</sup> contacts, the expected average of 10 pinholes per pillar guarantees pinhole transport, and therefore, only five pads were tested. The pads with areas of 10,000  $\mu$ m<sup>2</sup> and 250,000  $\mu$ m<sup>2</sup> are not listed in the table since for them transport is governed by a large number of pinholes and pinhole statistics does not play any role.

In order to see whether the measurements of the small areas meet the expectations of transport through none or a small number of pinholes and to be able to identify transport through single pinholes, PHOTOVOLTAICS -WILEY-

we applied different approaches. In a first, simplistic approach, we assume that every pinhole has the same resistivity  $R_{pin}$  and that the measured contact resistance  $R_c$  is dominated by pinhole transport due to the fact that tunneling is suppressed exponentially with barrier height and width. The measured contact resistance is given by  $n_{pin}$  single pinhole contact resistances connected in parallel:

$$R_{C} = \left(\sum_{i=1}^{n_{pin}} \frac{1}{R_{pin}}\right)^{-1}.$$
 (1)

This approach allows us to deduce 1/R<sub>pin</sub> as the smallest denominator in all measured contact resistances of 25-um<sup>2</sup> and 100-um<sup>2</sup> pad size where we still expect the presence and domination of pinhole transport.  $R_{pin}$  and  $n_{pin}$  are used here as free fit parameters. We find  $R_{pin} \approx 2.4 \pm 0.3$  M $\Omega$  and estimate the number of pinholes in each of these samples on this basis, using Equation 1. For the  $100 - \mu m^2$  pillars, we find 12 to 16 pinholes per pad. With an average of 14 pinholes per pad, this number is slightly larger than the expected value of 10 pinholes per pad. For the  $25 - \mu m^2$  pads, we find between two and four pinholes per pad again a number being slightly larger than the expected 2.5 pinholes per pad. This small difference between expected pinholes per pad and average number of pinholes deduced from the contact resistances might hint towards a small underestimation of pinhole-density from counting etch-pits. The results for the average number of pinholes deduced from contact resistances are given in the last column of Table 1 with the addition (cont.). This approach is not working for the smallest pads due to the average number of pinholes being below 1.

Therefore, we employ a second approach to identify pinhole transport. We compare the IV-measurements with calculations of the tunneling current density  $J_{tun}$ . The model calculates  $J_{tun}$  on the full area of a polySi/SiO2/c-Si junction, respecting macroscopic charge densities at the oxide faces, that is, charged interface states  $D_{it,k}$  where the index *k* refers to the oxide interface with the c-Si domain (k = cSi) or the poly-Si domain (k = polySi), respectively (MarcoPOLO model).<sup>14</sup> Briefly summarized, the tunneling current is calculated from the energies of the band edges at the SiO<sub>2</sub>/poly-Si and the SiO<sub>2</sub>/c-Si interfaces. These energies are deduced from the solution of the Poisson-equation under the assumption of charge-neutrality including the abovementioned interface charges, comparable with the procedure for a metal-oxide-semiconductor, as reported in, for example,

TABLE 1 Statistical results of all IV measurements for the four smallest pad sizes

Pad dimension [μm²]	Expected pinholes per pad (from etch-pit density)	Examined pads	Interpretable regression	Pads with pinhole (from regression)	Found pinholes per pad
1×1	0.1	18	1	1	0.06 (regr.)
2×2	0.4	21	7	5	0.24 (regr.)
5×5	2.5	17	13	12	3 ± 1 (cont.)
10×10	10	5	5	5	14 ± 2 (cont.)

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Girisch et al.<sup>15</sup> Based on these input parameters,  $J_{tun}(V)$  curves show a distinct variety of shapes that allow an explicit regression to measured curves.

We assume that the measured current is always dominated by the current that flows through the best conducting fraction *f* of the contacted junction area. If this area is very small, we identify it with a pinhole that has the radius  $r_{pin} = \sqrt{fA_0/\pi}$ , where  $A_0$  is the area of the contacted pillar. The calculated junction current then reads

$$J_{junc} = f \cdot J_{tun} (V, D_{it,cSi}, D_{it,poly}, d_{ox}).$$
<sup>(2)</sup>

This can be understood within the picture that a "pinhole" is not necessarily free of any interfacial oxide, but rather corresponds to a region where the interfacial oxide is significantly thinned as compared with its initial thickness prior to high-temperature annealing. Especially at measurements that are best described with a small *f*-value, we find that an extra series resistance  $\rho_{series}$  needs to be added to the evaluation in order to describe the curve shape adequately. One interpretation of the origin of this series resistance are current crowding effects in the vicinity of the local conduction path. It could be also connected to the fact that very small contacts typically have larger contact resistances. Therefore, we add  $\rho_{series}$  in the regression to all measurements with the relation

$$V = V_{bias} - \rho_{series} \cdot J_{junc}, \tag{3}$$

where  $V_{bias}$  is the measurement voltage and V is the voltage that drops across the tunneling oxide. We calculate IV curves from Equations 2 and 3 and fit the calculated  $J_{junc}$  to the measurement data by a least squares regression with respect to  $f_{,\rho_{series}}, d_{ox}, D_{it,cSi}$ , and  $D_{it}$ , poly. All calculations use Boron concentrations of  $3 \times 10^{19}$  cm<sup>-3</sup> and  $5 \times 10^{18}$  cm<sup>-3</sup> in the poly-Si and the c-Si region, respectively, as deduced from ECV profiling on a co-processed sample. Furthermore, we use the valence band difference of c-Si and SiO<sub>x</sub> of 4.8 eV as tunneling barrier height and assume a hole tunneling mass of 0.3 times the electron rest mass. Figure 3 shows the main results from this analysis.

We classify the regression to an IV curve as related to a pinhole, if the deduced oxide thickness  $d_{ox}$  is thinner than 0.5 nm (marked in Figure 3A with a dashed line). The dominance of  $D_{it}$  over the other regression parameters is visible in Figure 3B, where the obtained  $\rho_{series}$  is shown as open and  $D_{itcSi}$  with filled symbols. Most of the samples with areas of 25  $\mu m^2$  and also two samples with 4  $\mu$ m<sup>2</sup> show very low values of  $D_{itcSi}$ . In contrast, samples with small area fractions of 1  $\mu$ m<sup>2</sup> and also most of the samples with 4  $\mu$ m<sup>2</sup> are dominated by large defect densities (>10<sup>12</sup> cm<sup>-2</sup> eV<sup>-1</sup>), which makes the regression analysis insensitive to  $\rho_{series}$ . If measurements are governed by large D<sub>it</sub> values both under forward and backward biases (i.e., both  $D_{it,cSi}$  and  $D_{it,poly}$  are larger than  $10^{12}$  cm<sup>-2</sup> eV<sup>-1</sup>), the regression is even insensitive to  $d_{ox}$ , and we consequently spare the interpretation of these measurements. The number of samples meeting this condition increases with decreasing pillar area, indicating that charges at the defect-rich pillar faces influence the measurement and showing the limits of such a macroscopic model with respect to mesoscopic samples. Lastly, some measurements show a strong asymmetry with ohmic behavior under forward and nonohmic behavior under reverse bias and have been ignored too, for the reason that we attribute it to a bad contact. In Table 1, the remaining IV curves that we were able to classify with the regression are listed as Interpretable regression. The fraction of samples that can be identified as dominated by pinholes roughly agrees with what we would expect from the etch-pit density (compare in Table 1 Expected pinholes per pad with Pads with pinholes (from regression)). For the two smallest pad dimensions, the resulting fraction of pads with pinholes is calculated and shown in the last column of Table 1 with the addition (regr.).



**FIGURE 3** Results from MarcoPOLO regressions. The devices with  $1 \mu m^2$  are shown by squares, the  $4 - \mu m^2$  structures by diamonds and the  $25 - \mu m^2$  samples by circles. (A) Deduced oxide thickness versus pinhole radius. The dashed line at an oxide thickness of 0.5 nm separates devices with assumed pinhole transport (oxide thickness is less than 0.5 nm) from devices without pinhole transport (pure tunneling). (B) Series resistance (left axis, open symbols) and defect density (right axis, filled symbols) versus pinhole radius

As seen in Table 1, one sample of the smallest pads with  $(1 \times 1) \mu m^2$  was identified to have a pinhole. The measurements of this sample are shown in Figure 2G, whereas in Figure 2F, measurements are presented for a typical sample where no pinhole could be identified. Already in Figure 2G, some of the curves are very noisy. More detailed measurements revealed clear switching events as seen in Figure 4 shows one IV curve measured on this  $(1 \times 1) \mu m^2$  sample.  $J_{iunc}(V)$  curves that were determined for this sample with the regression approach in comparison with the measured IV curve at room temperature are shown in addition in Figure 4 as red and blue lines. Apart from the continuous curve, several outliers appear, of which some show a significant enhancement of currents, and some (fewer) show a slight reduction compared to the base curve. This switching effect happens for a few hundred milliseconds at the maximum, which is resolved here on the voltage axis (data acquisition at a specific voltage takes 60 ms). The measured current most likely passed through a pinhole with a thin remaining oxide: regression of the MarcoPOLO model to the base curve (red dashed line) vields a remaining oxide thickness of  $d_{ox} = 0.4$  nm on an area fraction f that corresponds to a pinhole with radius  $r_{pin}$  = 1.5 nm. Given the small dimensions of this conduction path, we believe that the change in the measured current is due to a change of state of a point charge that is located near the pinhole. The measured current in these switched states maintain the same curve shape as in the non-switched case, as depicted by the red line (enhanced current) and the blue dashed line (reduced current). The difference between these curves could easily be attributed to a



**FIGURE 4** Current density as measured at 300 K on a  $1 \times 1 \mu m^2$  pad (black line) and best fit using the MarcoPOLO model (red dashed line). Variation of the tunneling area fraction  $f = \pi r_{pin}^2 / 1 \mu m^2$  gives a good fit to switching features that occurred during the measurement (red line and blue dashed line), indicating a narrowing of the effective tunneling area fraction attributed to single-electron charging of a defect near the single pinhole

change of the interface state density  $D_{it,cSi}$ . However, we dare not to overwork the limits of the macroscopic MarcoPOLO model on these small dimensions and explain the observed reduction of currents by an effective narrowing of the pinhole radius  $r_{pin}$  from 2 to 1.5 nm. We deem that this narrowing is due to a local potential caused by the change of state of a point charge, located in the vicinity of the pinhole.

Similar discrete switching effects are well known for the drain currents of submicron MOSFETs.<sup>16</sup> The discrete random switching between two current levels is called random telegraph noise, and it was also observed in Si-FinFETs.<sup>17</sup> It was shown that in submicron MOSFET structures, the discrete switching effects are caused by the alternate capture and emission of single charges on a single slow interface defect.<sup>18-20</sup> Defects inside oxide were also made responsible for trap-assisted tunneling currents as analyzed, for example, in Yoo et al.<sup>21</sup> In our model, we did not take the possibility of such trapassisted tunneling into account. In our structure, we assume that the single-electron charging of a slow interface defect in the oxide of our small POLO junction is responsible for the observed narrowing of the pinhole radius. Then, the strong discrete switching effect is further evidence that transport through a single pinhole is governing the electrical current through our small device.

Apart measurements of a single pinhole, our micro-scale contacting also allows the measurement of a  $25 - \mu m^2$  sample area without a pinhole, which is highlighted in Figure 3B as pure tunneling. The deduced density of interface states  $D_{it,cSi} = 2.9 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ could not be measured on a larger area of this highly selective junction, as currents through pinholes dominate the measurement if present. This remarkably high  $D_{it}$  value agrees with the value obtained on another, by far not as selective, p-type POLO junction.<sup>15</sup> In contrast to that reported sample, here, we investigate a highly selective sample. The low  $\rho_{\rm C}$  values are due to the high pinhole density; the low surface recombination seems only to be due to the electrostatic passivation that arises from the in-diffusion of dopants and not from a healing-out of interface states. The direct determination of such a high D<sub>it.cSi</sub> value shows a possible path to the further optimization of our record cell, as a reduction of this value by hydrogen treatment can be expected to have a strong positive impact D<sub>it.cSi</sub> and thus on the surface recombination.

## 4 | CONCLUSION

In summary, we showed IV measurements on micrometer-sized areas of a POLO junction being small enough to contain a countable number of pinholes. We analyze the temperature dependence of IV curves, the absolute value of contact resistances and the shape of IV curves and find agreement of pinhole densities obtained by these methods with the pinhole density measured by a selective etching method. The discrete switching observed in the IV curve of one of the smallest contacts is attributed to single-electron charging of a defect in the vicinity of the single pinhole that dominates transport in this sample. From an analysis of a sample without a pinhole we are able to directly obtain the density of defect states undisturbed by pinhole transport. The measured very high value of  $D_{it,cSi} = 2.9 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$  opens a route to further increase the efficiency of solar cells with POLO junctions.

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