IMS
Institut für Mikroelektronische Systeme
Leibniz Universität Hannover

Leibniz Universität Hannover

A Heated Testbench for High Temperature ICs

Fritz Webering, Guillermo Payá Vayá, Evan Aditya, Jan Dürre and Holger Blume
{webering, guipava, aditya, duerre, blume}@ims.uni-hannover.de

Introduction

Some applications require very high temperature electronics [1]
- Automotive (on-engine) -40°C to 150°C
- Geothermal drilling ≥ 200°C
- Aviation (engine control)

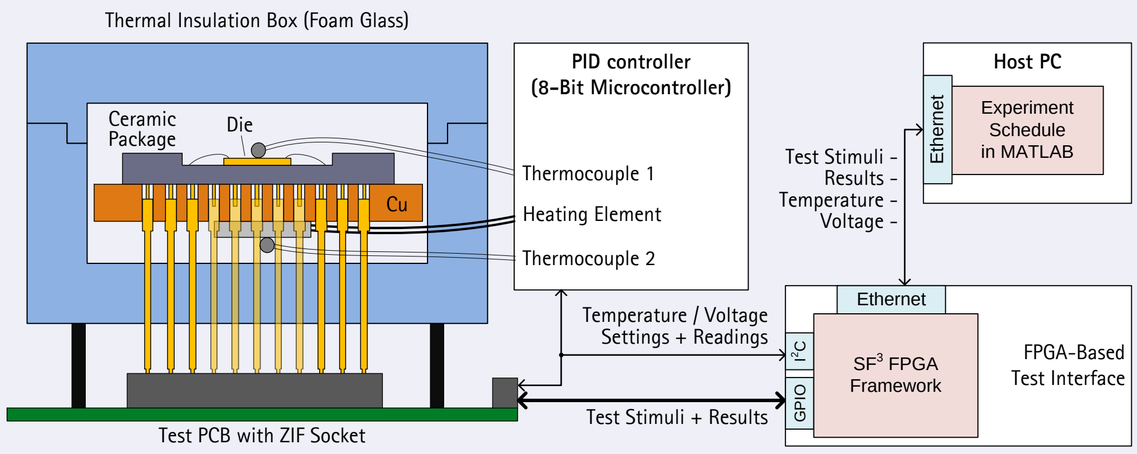
How to test high temperature ICs at temperatures over 200°C?

Simulation: Timing simulation of netlist
- Only few temperatures (corner cases from library)
- Often very pessimistic, no real-world data

Characterization: Build a system to heat the IC during tests
- Meaningful data from real silicon
- Challenging to implement **uniform** heating

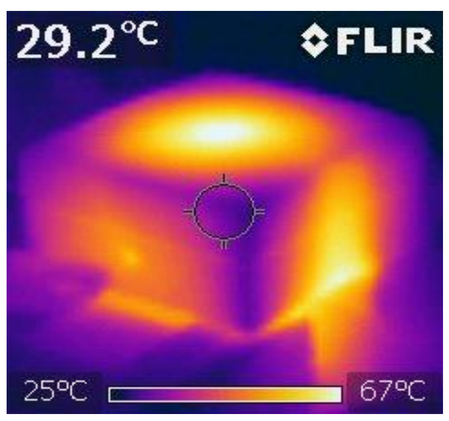
Framework

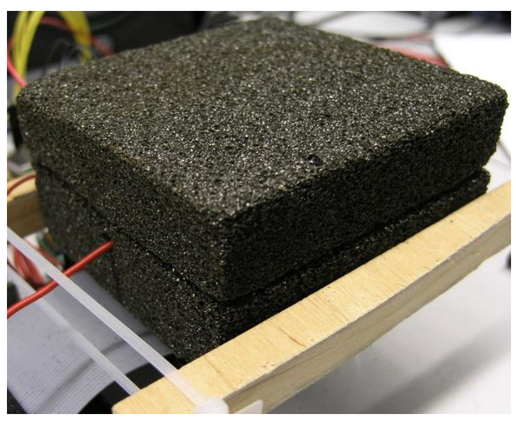
By integrating the heating system into an IC testing framework developed at the IMS, the whole experiment schedule—including variable temperature, supply voltage, and test stimuli—can be written in a single MATLAB script on the host PC.



*The whole setup of the integrated heating system consists of a **thermal insulation box** made of foam glass, which contains the IC under test in a high-temperature **ceramic PGA package**. Long **extension pins** perforate the isolation box in order to establish electrical contact to the test PCB. In order to spread the heat from the **ceramic heating element** uniformly to the whole IC package, a **copper heatspreader** is used. Two **type-K thermocouples** serve as a feedback path to the PID controller which is designed to keep the temperature on the **die** constant. The **FPGA framework** developed at the IMS ensures accurate test timing.*

The insulation box reduces heat loss and temperature fluctuations through convection. Low thermal conductivity reduces heat flow and temperature differences between different parts of the IC. The major weak point are the pins, which have a much higher thermal conductivity than the foam glass.

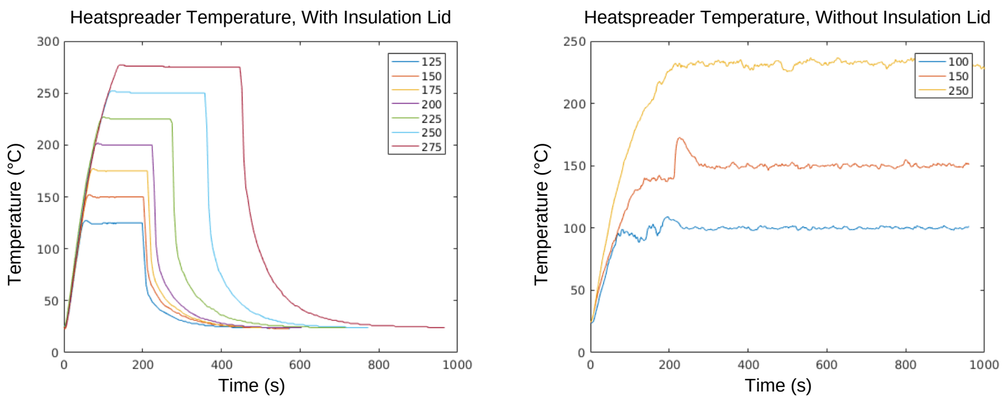




Thermal image and photograph of the insulation box while the heatspreader inside is heated to 250°C. The power dissipation through heat lost to the environment is around 50 Watts in this scenario.

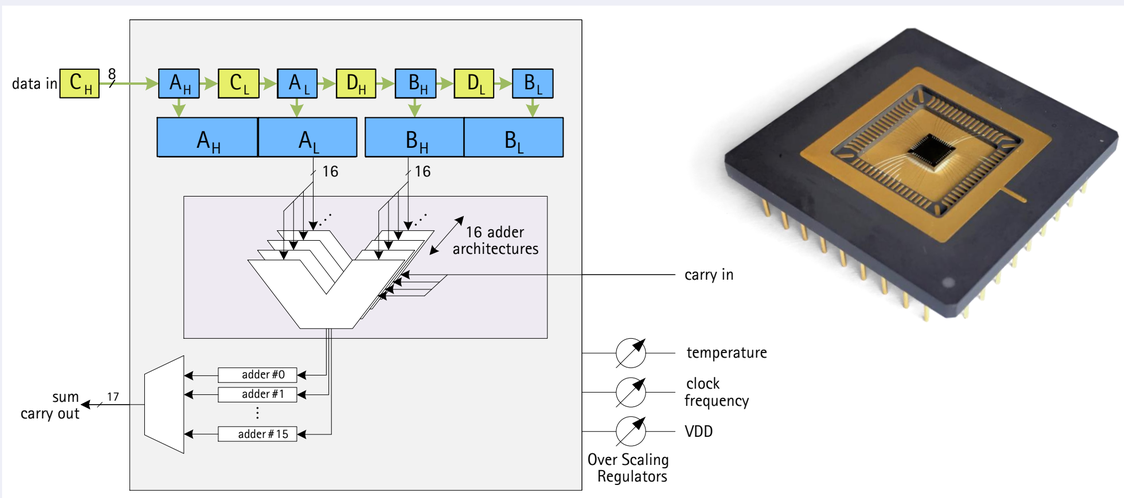
Temperature Controller

In order to achieve reproducible results from high-temperature tests, it is important that the IC temperature is stable. In this heating test, the controller waits until the temperature is stable for a while and then cools down the system.



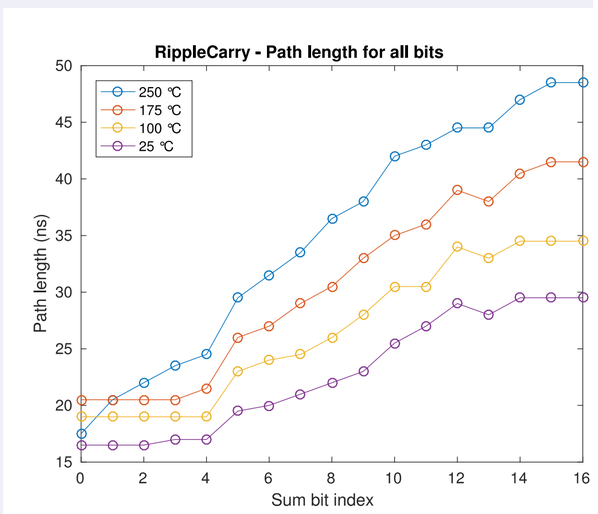
Heating and cooldown curves for two scenarios with and without the insulation lid on the box. Note that without the lid, the temperature fluctuations through convection are so strong, that the controller does not deem the temperature stable and thus does not initiate the cooldown cycle. Also, 250°C are not reached without the lid, because the PID controller limits the heating element temperature to a safe value of 300°C.

Case Study: Timing of Ripple Carry Adder



*Left: Block diagram of the Stochastic ASIC [2], showing the internal structure of the data path, which contains the 16 different adder architectures. Since gate delay depends on the previous state, two additions **A+B** and **C+D** are needed. One to enforce a known state, and the other to be evaluated.*
Right: The Stochastic ASIC, manufactured in the Fraunhofer H10 high-temperature SOI process.

By adding carefully crafted operands at increasing clock rates and then inspecting the individual result bits, one can determine the length of individual paths inside an adder. Using the integrated heating system, these paths can now be measured at different temperatures, as shown to the right.



Conclusion

The presented integrated heating system allows flexible testing of high-temperature ICs by varying factors like supply voltage, operating frequency, and environmental temperature.

Institut für Mikroelektronische Systeme
Fachgebiet Architekturen und Systeme
Prof. Dr.-Ing. Holger Blume
www.ims.uni-hannover.de

References
[1] Watson, Jeff, and Gustavo Castro. "A review of high-temperature electronics technology and applications." *Journal of Materials Science: Materials in Electronics 26.12* (2015): 9226-9235.
[2] Nowosielski, R., et al. "Exploring Different Approximate Adder Architecture Implementations in a 250◦ C SOI Technology." *1st Workshop on Approcimate Computing WAPCO* (2015)