CIRP Annals - Manufacturing Technology 70 (2021) 163–166

Contents lists available at ScienceDirect

CIRP Annals - Manufacturing Technology

journal homepage: https://www.editorialmanager.com/CIRP/default.aspx

Additive manufacturing of copper vertical interconnect accesses by laser processing

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ARTICLE INFO

Article history:
Available online 20 April 2021

Keywords:
Coating
Sintering
Multilayer

This paper introduces a new manufacturing process for vertical interconnect accesses (VIA). In contrast to industrially established VIA metallization technologies, the presented approach takes place without any chemical plating by combining copper ink and epoxy insulator coating with CO_2 laser processing for VIA drilling and copper ink sintering. The minimum VIA resistances are less than 50 mΩ, fitting the theoretically calculated value. A laboratory application scenario testing a 10×10 contact pad array with a pitch of 800 µm successfully demonstrates routing across five printed metallization layers, including 128 blind and 112 buried VIA.

1. Introduction

The production of vertical interconnect accesses (VIA) is a well-established technology in the semiconductor and printed circuit board (PCB) industry. However, its relevance in additive manufacturing [1] and 3D printed electronics [2] is just beginning to be explored. This research presents a novel additive manufacturing technology for printing multilayer conductive traces with blind and buried VIA by laser processing. Printed electronics technologies enable cost-efficient conductive circuit production while simultaneously opening new fields of application for electronics. However, until now, most printed electronics have focused on applications with a single metallization layer. Therefore, the level of integration is limited compared to that of PCB technologies with multilayers, including blind, buried, or through-hole VIA. The increasing demand for higher integration of electronic systems requires printed VIA connecting printed double and multilayers. Most established VIA manufacturing processes for PCB depend on chemical plating for metallization. Due to the high costs, complexity, and adverse environmental impact, chemical plating is not suitable for printed electronics.

Recently, research groups have begun the development of printed VIA processes with silver ink. The first processing step for printed through hole VIA is either punching [3] or laser drilling [4]. Through-hole VIA in printed electronics are also found in roll to roll [5], droplet [6], inside porous paper [7], or silicon [8] processes. Processing blind VIA requires a careful production of cavities without destroying the underlying conductive layer. A sophisticated method is laser drilling to create cavities on 100 µm thick silver metallization [9]. Another way for blind VIA cavity generation is by dispensing a solvent drop to selectively dissolve a polymer insulator [10]. Employing conventional direct writing [11] or multi-material laser direct writing [12] for blind VIA generation by an aerosol jet enables the generation and metallization of VIA cavities directly during the printing of the insulator [13]. The VIA filling proceeds by either screen printing [3], ink-jetting [4], dispensing [9,10] or aerosol-jetting [13] of silver ink cured by heat convection. This research presents the CO_2 laser drilling of cavities and full-surface copper ink coating with subsequent CO_2 laser curing of VIA.

Table 1 lists a comparison of costs between the existing silver ink-jetting approach and the novel process from this research. In contrast to the commonly used silver ink, the presented copper process incurs lower material costs. However, the tendency of copper to oxidize may cause an increase in electrical resistance. Thus, this study uses a rapid sintering technique (pulsed laser) to minimize the oxidation of copper, which goes along with higher system investment but lower maintenance and operation costs and further technical advantages. The resolution is limited only by the laser spot size. Additionally, the digital sintering enables to apply the copper ink with a full-surface coating to achieve high throughput. In contrary to ink-jetting, the presented process is transferable to print on 3D components.

Table 1
Comparison of costs (+ high; – low).

	Ink-jetting silver	Laser sintering copper
Material	+	–
System	–	+
Maintenance and Operation	+	–

An application scenario demonstrates the manufacturing of a multilayer contact pad array for the assembly of ball grid array (BGA) packages to enable fine-pitch contacting in micro BGA [14] and miniaturized electrical 3D components [15]. Fig. 1 shows a printed 10×10 contact pad array with a pitch of 800 µm to demonstrate the routing of 100 contact pads across five printed layers. The 64 inner contact pads require VIA for the routing.

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https://doi.org/10.1016/j.cirp.2021.03.006

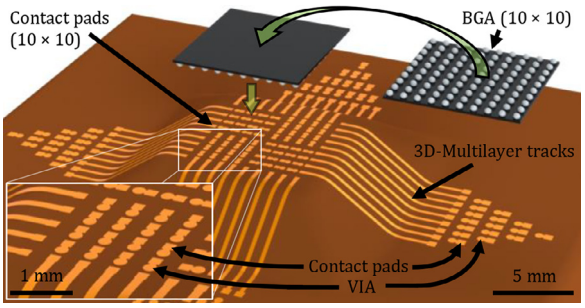


Fig. 1. Printed multilayer 10 × 10 contact pad array render.

2. Approach

Fig. 2 shows the schematic process flow of copper VIA printing. Multiple full-surface coating of the substrate (a) creates alternating insulator (b/e/i) and copper ink (c/g) layers. For VIA, the laser drilling of cavities (f) follows the insulator coating (e). Owing to the Gaussian intensity distribution of a laser beam and the selected processing parameters, the laser drilling of the insulator material creates a tapered VIA. The parabolic VIA radius enables continuous copper ink coating. The coated copper ink is cured by laser sintering used for the conductive traces (d/h) and VIA (h) generation. In the last step, another insulator coating levels the cavity (i) to enable the processing of another layer.

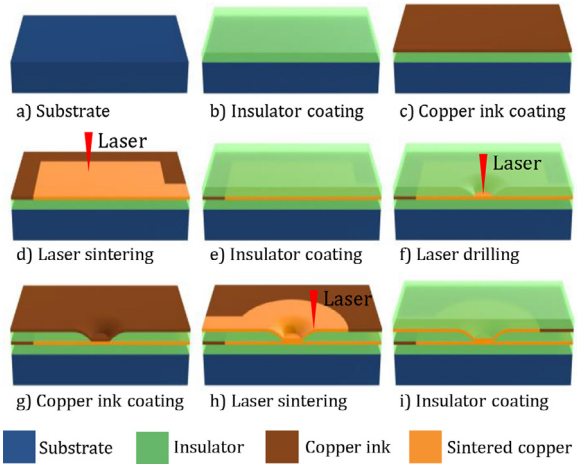


Fig. 2. 3D schematics of copper VIA printing process flow.

3. VIA resistance model

By slicing a 3D VIA with a variable cross-sectional area in small pieces, electric modeling of the resistance is possible [16]. The following is a theoretical calculation of the resistance for a VIA connecting two layers through an insulator with a certain thickness (h), as schematically shown in Fig. 3. The VIA resistance consists of the contact resistances at the connecting layers (R_I and R_{III}) and the inner VIA resistance (R_{II}). The VIA has only sidewall metallization; hence the cross-sectional area of R_{II} is smaller than that of R_I and R_{III}. Therefore, the inner VIA resistance R_{II} represents the bottleneck of the electric current between zero ($x = 0$) and the upper limit ($x = U$). Consequently, it dominates the total VIA resistance ($R = R_I + R_{II} + R_{III}$). The points (U,A), (0,B), (U,C), and (0,D) determine the parabolic formulas for inner (1a) and outer radii (1b) of the inner VIA metallization for $0 \le x \le U$. The resistance is calculated using the resistivity (ρ) across the variable annulus cross-sectional area of the inner VIA metallization.

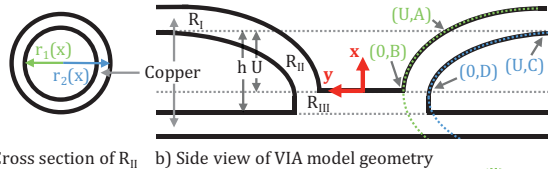


Fig. 3. Geometry for the VIA resistance model.

$$r_1(x) = \frac{A-B}{U^2}x^2 + B \tag{1a}$$

$$r_2(x) = \frac{C-D}{U^2}x^2 + D \tag{1b}$$

$$R_{II} = \rho \frac{x}{Area(x)} = \rho \frac{x}{\pi\left((r_2(x))^2 - (r_1(x))^2\right)} \tag{2}$$

R_{II} is calculated by the integration across the VIA height. Therefore, the formulae (1a) and (1b) are inserted into (2) and dx replaces x. As there is no primitive function, a computer-aided calculation assists the evaluation.

$$R_{II} = \frac{\rho}{\pi}\int_0^U \frac{dx}{\left(\frac{C-D}{U^2}x^2 + D\right)^2 - \left(\frac{A-B}{U^2}x^2 + B\right)^2} \tag{3}$$

The model verifies the experimental data in the following Section 5 by inserting the geometric points from the cross-sectional view and measured resistivity.

4. Experimental procedure

This study uses an additive manufactured photopolymer (VeroBlue) substrate material printed with a multi-jet modeling 3D printer (Enden260VS, Stratasys). For the insulator coating (DM-INI-7003, Dycotec Materials Ltd), the sample surface is fully covered by a manual pipette application of the insulator. Subsequently, the sample stays in a vertical position for 30 s to dispose of the excess insulator. The insulator is cured using a broadband UV-light (BlueWave 50 UV) for 20–30 s. The copper ink (DM-CUI-5002, Dycotec Materials Ltd) wets by fully dipping the sample in a vertical position into a reservoir filled with ink twice. Therefore, the sample was immersed and extracted at a speed of 0.6 cm/s and had a dwell time of 5 s. After the dipping process, the sample was dried at 60 °C. This study uses a CO_2 (10.6 µm wavelength) laser system (Laser Cutter – Epilog Fusion 32 M2 Dual, 51 mm lens) for laser drilling as well as for sintering. The following parameters are constant: 42 µm hatch distance, 45° hatch angle, laser beam in focus, 76.2 µm focus diameter, 875 mm/s speed for sintering and 700 mm/s for VIA drilling, 1200 dpi resolution, and 400 mW laser sintering power. A confocal microscope (Nanofocus, µsurf custom) determines the resulting insulator layer thickness. First experiments evaluate the influence of laser power (0.3 W – 0.7 W) on the insulator ablation depth with different cavities (150, 250, or 350 µm computer-aided design (CAD) diameter). It follows an analysis of confocal and microscope pictures during the VIA processing. For laboratory tests, a 5 × 5 contact pad array (zoomed area in Fig. 1) representing a quarter of the 10 × 10 array demonstrates the process in an application scenario. The 5 × 5 array enables a statistical evaluation with a simple setup, including a smaller layout and routing. Fig. 4a shows the schematic routing of the inner contact pads inside the array. The schematic side view in Fig. 4b visualizes the alternating VIA positioning method to circumvent the VIA stacking on top of each other.

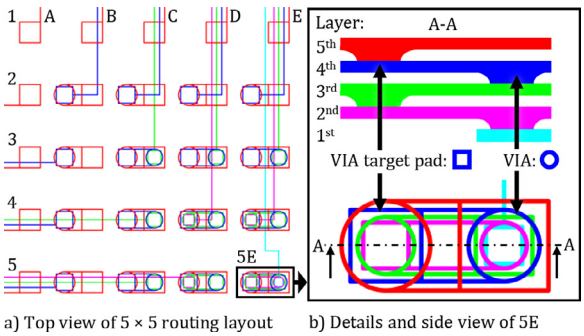
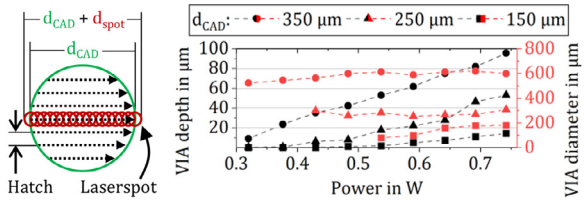


Fig. 4. Multilayer routing design for 5 × 5 quarter array of 10 × 10 array.

5. Results and discussion

5.1. Insulator coating and laser drilling

For a reliable VIA drilling process, the most crucial parameter is the repeatability of the insulator coating. Confocal microscope measurements resulted in a mean coating thickness of 30.8 µm with a standard deviation of 3.43 µm. It is possible to add a thinner to reach a smaller insulator coating thickness for higher miniaturization and integration. Fig. 5a shows the CAD diameter and the relevance of the laser spot size. Fig. 5b plots the laser drilling parametrization results with an insulator coating of thickness >100 µm. The data for the maximum cavity depth (black) indicates that the ablation ratio is approximately linear to the increase in power. However, the slope decreases for a 150 µm cavity and ablation only starts from a threshold at a power of 0.5 W. In contrast to the smaller VIA, the 350 µm cavity is significantly larger than the CAD diameter (350 µm), inclusive of the additional focus diameter of 76.2 µm. The increasing thermal agglomeration on the top surface due to the high direct absorbance of the CO_2 laser wavelength, explains the larger diameter [17]. The combination of larger and smaller diameter in multiple processing can create different cavity shapes.

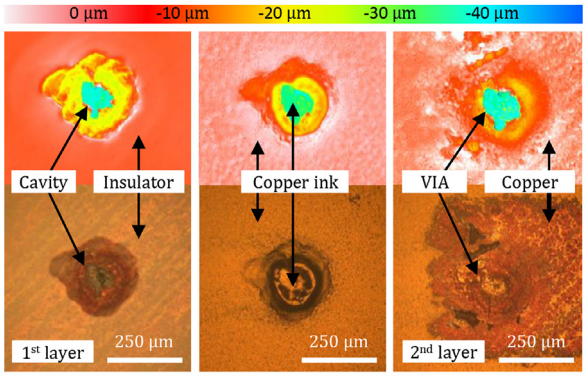


a) VIA diameter b) Laser drilling power parametrization

Fig. 5. Laser drilling with different VIA diameters.

5.2. Copper ink coating and laser sintering

A multiple 0.537 W laser drilling, twice with a diameter of 250 µm and once with a diameter of 150 µm, provides more than 34 µm of maximum drilling depth (as per data in Fig. 5). The sintered copper in the first layer reflects the laser radiation and contributes additional protection from drilling too deep. Further processing is shown in Fig. 6, run as in the process schematics in Fig. 2. After the VIA drilling (Figs. 2f and 6a), the copper ink coating covers the entire surface (Figs. 2g and 6b), and the laser sinters copper traces and VIA metallization (Figs. 2h and 6c).



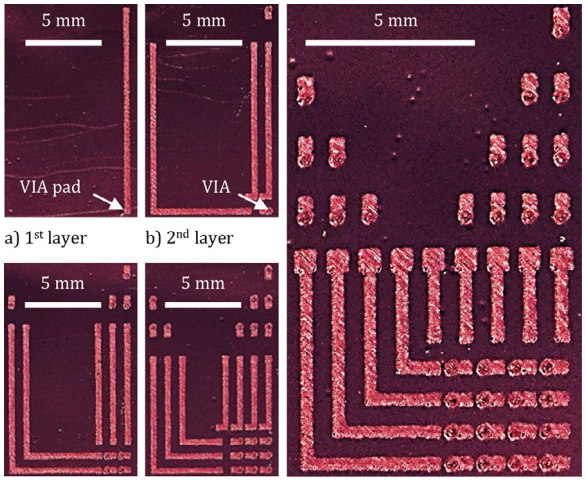
a) Drilled cavity b) Cu ink coating c) Sintered copper

Fig. 6. Confocal and microscopic VIA processing images.

The top diameter of the insulator cavity is larger than the bottom diameter, indicating the desired parabolic shape. The confocal analysis in Fig. 6a shows the top insulator surface (red), the cavity sidewalls (yellow), and the exposed (and partially ablated) sintered copper area of the first layer (cyan). The remaining areas of the VIA target pad ensure a possible contact and are entirely coated with copper ink in the next step. In Fig. 6b, it is clear that the ink coating has a higher roughness (Rz > 2 µm; Ra > 500 nm) than the insulator (Rz < 1 µm; Ra < 100 nm). After laser sintering, the roughness increased even more (Rz > 8 µm; Ra > 1 µm) as small copper agglomerates formed an uneven surface. Black areas in the microscopic image (Fig. 6c) indicate cracks at the edges and sidewalls of the VIA. Kim et al. also observed this defect with printed silver VIA due to the shrinkage of the ink during sintering [4].

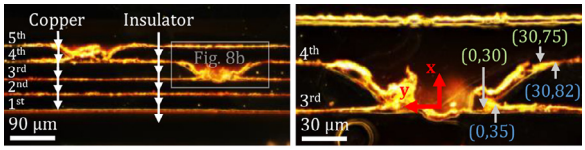
5.3. Printing of multilayer contact pad array (5 × 5)

Testing the application scenario by producing four 5 × 5 arrays resulted in 98 out of 100 working contact pads. Several contact pads require more than one VIA, and every routing to the outside pads needs two VIA (one for the 5 × 5 array and one for the outside contact pad). Thus, the ratio of working VIA was higher than 99%. Fig. 7 includes a picture of every sintered layer along with the metalized VIA. A polished cross-section of the contact pad 5C (two VIA connecting three layers) is shown in Fig. 8a. The high magnification cross-sectional view of a VIA in Fig. 8b shows a sintered connection between the third and fourth layers. The cavity profile fits the set model with parabolic sidewalls (Section 3, Fig. 3). Inserting the planar traces resistivity determined in preliminary tests (ρ = 69 µΩ cm) and the four coordinate points (Fig. 8b) into Eq. (3) results in a theoretical inner resistance of 20.2 mΩ.



a) 1st layer b) 2nd layer c) 3rd layer d) 4th layer e) 5th layer

Fig. 7. Top view image series of 5 × 5 contact pad array production.



a) Cross section of contact pad 5C b) VIA connecting 3rd and 4th layer

Fig. 8. VIA cross-section after sintering (coordinate points in µm).

By measuring the 2-points resistance for every contact pad during the production process, it is possible to determine the additional resistance from each layer and the VIA. Fig. 9a plots all contact pad resistance values in Ω/cm (Fig. 4 shows labeling code), recalculated with the exact conductive trace length for every layer, including the extra distance (600 µm) from the two VIA contact pads representing the contact resistances (R_I and R_{III}).

The data in Fig. 9b includes all 115 measured VIA resistances (R_{II}), calculated by extracting the resistance difference of two layers and dividing by two. The division by two is necessary because two VIA contribute to the resistance of every additional layer plotted in Fig. 9a. The box (orange) includes 50% of the data between the upper and lower quartiles. The mean value (1 Ω) is much higher than the

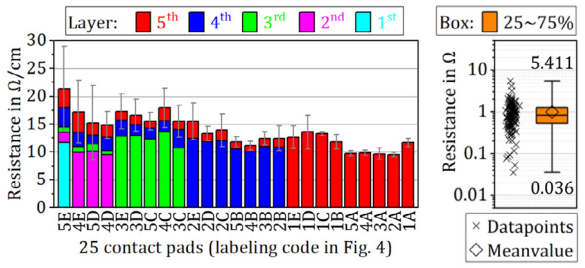


Fig. 9. Resistance evaluation.

theoretically calculated value (20.2 mΩ). Only a few VIA resistances reach close to the theoretical value. The lowest measured resistance was 36 mΩ.

Assuming the mean value (1 Ω) is the actual internal VIA resistance, the VIA resistivity is approximately fifty times of the resistivity of the planar conductive traces. The mean resistivity of the VIA is significantly higher than that of the conductive traces for several reasons. The ink layer inside the VIA is thicker and requires more energy to sinter completely, but the conductive traces and VIA are on the same focal plane with the same sintering parameters. The elliptical projection of the laser beam on the sidewalls leads to a more significant reduction in the actual energy reaching the VIA sidewalls [18]. Moreover, the cracks observed in Fig. 7c could also explain the relatively high resistivity of the VIA as they dramatically reduce the cross-sectional area. Another possible explanation lies in additional contact resistances from the interface region between R_{II} and R_I or R_{III}. Precise measurement with 4-point sensing and more data could potentially determine the exact contact resistance in the future.

6. Conclusion

This paper introduces a new printing and sintering process for VIA using copper ink. Compared to ink-jet printed silver VIA literature, the obtained copper VIA resistances are in the same range. While Khorramdel et al. reached 4 Ω per silver VIA [8], Kim et al. showed an average silver VIA resistance of 0.2 Ω [4]. However, since the VIA geometries are different, a direct comparison is not possible.

Using a near-infrared laser (1.064 µm, Nd:YAG) for sintering could result in a lower VIA resistivity, as already reported for single-layer conductive traces on 3D surfaces in [19]. However, this would lead to losing the advantage of having the sintering and drilling process in the same laser machine because the direct VIA drilling with 1.064 µm is impossible due to the high transmissivity of the insulator at this wavelength.

A significant advantage of the approach is the low number of processing steps without any chemical metallization baths. Compared to other printing technologies this research provides an economical working processing approach due to the low copper material and laser maintenance and operation costs concerning a large throughput. Moreover, contacting (ultra) fine-pitch BGA packages with printed multilayers and VIA becomes possible as only the laser spot size determines the resolution. Another considerable advantage over standard VIA technologies and previous research in this field is that the presented process is fully transferable to 3D components, enabling printed multilayers on 3D surfaces in the future.

Declaration of Competing Interest

None.

Acknowledgments

The authors would like to thank the German Federal Ministry of Economics and Energy (BMWi) for funding the project “3D-Copper-Print” (20133N) and the German Research Foundation (DFG) for funding the Cluster of Excellence PhoenixD (EXC 2122) based on a resolution of the German Bundestag.

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