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Silicon heterojunction solar cells combining an $a$-Si:H($n$) electron-collector with a PEDOT:PSS hole-collector

Ralf Gogolina, Dimitri Zielkea, Wilfried Lövenichb, Rüdiger Sauerb, Jan Schmidtac

aInstitute for Solar Energy Research Hamelin (ISFH), Am Ohrberg 1, 31860 Emmerthal, Germany
bHeraeus, Electronic Materials Division, Chempark Leverkusen, 51368 Leverkusen, Germany
cInstitute for Solid State Physics, Leibniz University Hanover, Appelstrasse 2, 30167 Hanover, Germany

Abstract

We combine PEDOT:PSS as hole-selective layer on c-Si with a well-passivating electron-selective $a$-Si:H($n$) layer in an alternative type of silicon heterojunction solar cell. As the interface between the PEDOT:PSS and the c-Si substrate plays a crucial role in the cell performance, we examine the impact of an interfacial SiOₓ tunneling layer between the c-Si substrate and PEDOT:PSS in detail. We find that a natural SiOₓ layer grown within a couple of minutes leads to low $J_{0}$ values ranging between (80 - 130) fA/cm², allowing for $V_{oc}$ values of ~690 mV. Implementation of this PEDOT:PSS/SiOₓ/c-Si junctions into solar cells with phosphorus-diffused $n$+ front results in low series resistance values of only 0.6 $\Omega$cm² and good fill factors >80%, leading to efficiencies >20%. We then implement the PEDOT:PSS/SiOₓ/c-Si junction to the back of heterojunction cells with an $a$-Si:H($n$)/ITO front, in order to demonstrate the feasibility of this novel cell concept, which has a higher $V_{oc}$ potential compared to cells with a conventionally processed front side. The cell efficiencies of the first batch reach 15.2%. This relatively moderate efficiency of the first cell batch is due to technological issues with the screen-printed front metallization grid, leading to poor fill factors of only 71%, whereas the $V_{oc}$ values of this first batch were already above 650 mV.

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Keywords: PEDOT:PSS; heterojunction; organic-silicon junction; interface preparation

1. Introduction

Heterojunction solar cells combining c-Si technology with the hole-conducting polymer poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) [PEDOT:PSS] have been introduced only recently into photovoltaics [1,2,3,4,5,6,7]. As we have demonstrated [5-7], the PEDOT:PSS/c-Si interface shows excellent passivation properties, if the interface between PEDOT:PSS and c-Si is properly prepared. The optimal interface
preparation led us recently to solar cell efficiencies of up to 20.6%. However, so far we have not revealed the details of our optimized interface preparation. These details will be revealed in this contribution. In addition, we present a novel type of heterojunction solar cell combining PEDOT:PSS with the a-Si:H/c-Si technology. Due to the low $J_0$ values of both implemented junctions, this cell type should have a strongly increased $V_{oc}$ potential compared to previous cells with PEDOT:PSS/c-Si junction. We present here results of our first cell batch.

2. Optimization of PEDOT:PSS/c-Si interface

For the passivation optimization we use transient photoconductance decay (PCD) measurements on lifetime samples, as schematically shown in the inset of Fig. 1, and extract the saturation current densities ($J_0$) according to Ref. 8. We use 300 µm thick $p$-type float-zone (FZ) silicon wafers with a resistivity of ~150 Ωcm to assure $J_0$ determination under high injection level conditions. After an RCA cleaning, we deposit a 100 nm thick well-passivating SiN$_x$ layer by means of plasma-enhanced chemical vapor deposition (PECVD) onto one side of the wafer.

After the SiN$_x$ deposition, we apply different treatments to the other side of the wafer prior to the subsequent deposition of the PEDOT:PSS dispersion (Heraeus, Germany) using spin-coating and annealing at 130°C in ambient air. The spin-coating is performed with 500 revolutions per minute (rpm) for 10 seconds and subsequently 1000 rpm for 30 seconds, leading to a film thickness of approximately 100 nm. A first set of samples is (i) coated with PEDOT:PSS directly after the SiN$_x$ deposition without any further pre-treatment. For the next three sets of samples the wafers were HF-dipped (1%, 1 minute) and stored in ambient air for (ii) 10 minutes, (iii) 20 hours, and (iv) 30 days prior to the PEDOT:PSS deposition, respectively. Furthermore, we examine the following additional tunneling layers: (v) a chemically grown SiO$_x$ by omitting the final HF dip in the RCA cleaning sequence, (vi) an O$_2$-plasma treatment of the silicon wafer surface, and (vii) a thermally grown (500°C, 15 min) SiO$_x$.

![Fig. 1. Saturation current densities $J_0$ for different silicon surface treatments prior to the PEDOT:PSS deposition. The different bars in one group belong to different samples with the same treatment. The inset schematically shows the structure of the lifetime test samples.](image-url)
The $J_0$ results of these samples are shown in Fig. 1. We measure $J_0$ values of $\sim 200 \text{ fA/cm}^2$ for the samples coated with PEDOT:PSS directly after the SiN$_x$ deposition. However, waiting for 10 minutes after an additional HF dip prior to the PEDOT:PSS deposition leads to significantly lower $J_0$ values of (80 - 130) fA/cm$^2$. Note that 10 minutes in air is the minimal time between HF dip and PEDOT:PSS deposition limited by the manual handling. The lowest $J_0$ values of below 50 fA/cm$^2$ are measured for the 30-days stored samples. The other three SiO$_x$ tunneling layers (v)-(vii) show much higher $J_0$ values in the range of (400 - 1200) fA/cm$^2$ and are hence not suitable for the application to high-efficiency solar cells. Note that the measured $J_0$ values also include the non-negligible recombination losses of the SiN$_x$-passivated surface of the samples. The reported $J_0$ values are hence upper limits to the true $J_0$ of the PEDOT:PSS/SiO$_x/c$-Si junctions.

In order to determine the contact resistance $R_c$ of the PEDOT:PSS/SiO$_x/c$-Si interface we apply the method according to Ref. 9, using 4-point-probe (4PP) test samples as schematically shown in the inset of Fig. 2. We use 300 μm thick $p$-type FZ silicon wafers with a resistivity of 1.5 Ωcm. After an RCA cleaning and HF dip (1%, 1 minute) we deposit PEDOT:PSS onto one side of the wafers after (i) 10 minutes, (ii) 24 hours, and (iii) 4 days storage in ambient air. We then measure the sheet resistance $R_{\text{sheet}}$ with a 4PP setup (RT-70/RG-7A, Napson Corporation) on the uncoated side of the wafer. The measured $R_{\text{sheet}}$ values are shown as green symbols in Fig. 2. The error bars represent the standard deviation of four measurements on the same sample.

Additionally, the 4PP sheet resistance is simulated in dependence over a broad range of interface contact resistances using Sentaurus device [10]. The simulation results are shown as red lines in Fig. 2 for typical sheet resistances of our PEDOT:PSS layers, which are in the range of (100-110) Ω/$\sqrt{\text{cm}^2}$.

Comparing the measured with the simulated $R_{\text{sheet}}$ values, we determine contact resistances $R_c$ of (0.49 ± 0.21) Ω$\text{cm}^2$, (0.82 ± 0.27) Ω$\text{cm}^2$ and (3.3 ± 0.4) Ω$\text{cm}^2$ for the 10 minutes, 24 hours and 4 days stored samples, respectively. It becomes obvious that the contact resistance between the silicon wafer and the PEDOT:PSS layer increases with an extended native SiO$_x$ formation time in air. Consequently, for achieving a low series resistance the formation time of a native SiO$_x$ has to be chosen as short as possible.

![Fig. 2. Measured (green symbols) and simulated (red lines) 4-point-probe sheet resistances as a function of the contact resistance for three storage times after HF-dip prior to the PEDOT:PSS deposition.](image-url)
3. Solar cell results

On the basis of our $J_0$ and $R_c$ results we first fabricate solar cells with phosphorus-diffused front surface and evaporated contacts featuring two different pre-treatments of the silicon surface prior to the PEDOT:PSS coating (see inset of Fig. 3). Details of the solar cell process can be found in Ref. 11. After finishing the conventionally processed front side of the solar cells, all samples were dipped in a 1% HF solution for 1 minute. After this HF dip, some samples were processed within 10 minutes (‘thin’ native SiO$_x$) while other samples were kept in air for 48 hours (‘thick’ native SiO$_x$). Subsequently, the PEDOT:PSS layer was deposited by spin-coating on the entire rear at 500 revolutions per minute (rpm) for 10 seconds and subsequently 1000 rpm for 30 seconds. The samples were then annealed on a hotplate in air at 130°C for 15 minutes for drying and to remove residual solvents. Finally, the entire rear surface is metalized with silver by means of evaporation.

Table 1 and Fig. 3 show the solar cell performances of the two best cells with a ‘thin’ native SiO$_x$ (red triangles) and a ‘thick’ native SiO$_x$ (blue squares) tunneling layer, respectively. The $J_{sc}$ and $V_{oc}$ values of the two solar cells in Fig. 3 are almost identical. However, we observe a large deviation in the fill factors $FF$. The $FF$ of the solar cell with ‘thick’ SiO$_x$ shows a drastically increased series resistance $R_s$ of 2.15 Ωcm$^2$, leading to a low $FF$ of only 73.1% compared to 80.6% and an $R_c$ of 0.5 Ωcm$^2$ for the cell featuring the ‘thin’ SiO$_x$ tunneling layer. The $R_s$ values are determined using the double-light method according to Ref. 12. This result correlates well with the $R_c$ values measured on our test structures. We hence conclude that a too thick SiO$_x$ interface layer hampers the transport of holes from the c-Si wafer into the hole-conducting PEDOT:PSS layer and in order to achieve high efficiencies a sufficiently thin SiO$_x$ interface layer has to be chosen to obtain low contact resistances between PEDOT:PSS and c-Si.

Table 1. Solar cell performances of two solar cells with different times between HF dip and PEDOT:PSS deposition. The cell area is (2 x 2) cm$^2$.

<table>
<thead>
<tr>
<th></th>
<th>$J_{sc}$ [mA/cm$^2$]</th>
<th>$V_{oc}$ [mV]</th>
<th>$FF$ [%]</th>
<th>$\eta$ [%]</th>
<th>$R_s$ [Ωcm$^2$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>‘thin’ native SiO$_x$ (10 min)</td>
<td>38.9</td>
<td>657</td>
<td>80.6</td>
<td>20.6</td>
<td>0.5</td>
</tr>
<tr>
<td>‘thick’ native SiO$_x$ (48 h)</td>
<td>38.7</td>
<td>657</td>
<td>73.1</td>
<td>18.6</td>
<td>2.15</td>
</tr>
</tbody>
</table>

Fig. 3. Current-voltage characteristics of two solar cells with PEDOT:PSS hole-selective layer at the cell rear featuring two different SiO$_x$ tunneling layer thicknesses. The inset shows a schematic cross section of the fabricated solar cells.
However, since the $V_{oc}$ of these solar cells is limited by the conventionally processed front side, we propose here a novel cell design: An attractive alternative is the combination of the PEDOT:PSS hole-selective layer with the $a$-Si:H($i/n$) electron-selective layer, which is well known for its outstanding $V_{oc}$ potential [13]. A schematic cross section of such a solar cell is shown in the inset of Fig. 4. Here, the electron collector is realized at the cell front by $n$-type $a$-Si:H with an interfacial intrinsic $a$-Si:H layer to achieve excellent interface passivation ($V_{oc}$ potential $> 730$ mV [14]). The front side is then coated with a sputtered ITO layer and contacted by a screen-printed low-temperature silver paste. Note that it is also possible to achieve quite high $V_{oc}$ values with an $a$-Si:H($n$) layer without interfacial $a$-Si:H($i$) layer, which is not the case for $a$-Si:H($p$). Hence, it is a further simplified option to combine a single-layer $a$-Si:H($n$) electron-selective contact with PEDOT:PSS as hole-selective contact, which would only require one single PECVD process step. The performance of a representative solar cell of our first batch of PEDOT:PSS/c-Si/a-Si:H($n$)/ITO cells is shown in Fig. 4. Although the cell performance is far below optimal, this is a clear proof of principle. However, the full potential of this cell type could not be exploited in our first batch due to a non-optimal front side preparation (too thick $a$-Si:H and ITO layers limit $J_{SC}$, front screen-printed contact limits $R_s$, poor a-Si passivation limits $V_{oc}$).

![Fig. 4. Current-voltage characteristics of our first proof-of-principle PEDOT:PSS/c-Si/a-Si:H($i/n$)/ITO solar cell. The inset shows a schematic cross section of the cell structure.](image)

4. Summary

We have presented a detailed study of the c-Si surface preparation prior to the PEDOT:PSS deposition. We have shown that native oxides grown in ambient air after an HF dip provide low saturation current density values. We achieved the lowest $J_0$ value of only $\sim 50$ fA/cm² for an oxide grown within 30 days. However, the lowest contact resistivity $R_c$ of $(0.49 \pm 0.21) \ \Omega \cm$ was found for an oxide grown in only 10 minutes, still providing $J_0$ values of $(80 - 130) \ \text{fA/cm}^2$, allowing for a $V_{oc} > 690$ mV. We have suggested an attractive novel heterojunction cell structure comprising a hole-selective PEDOT:PSS layer and an electron-selective $a$-Si:H($n$) layer on a c-Si substrate to exploit the full $V_{oc}$ potential of the PEDOT:PSS/c-Si heterojunction. Our first cell batch demonstrated the feasibility of this cell type, however, the achieved maximum cell efficiency was limited by technological restrictions of the front junction.
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References