

Integrated High-Voltage Switched-Capacitor DC-DC Converters

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Abstract

The focus of this work is on the integrated circuit (IC) level integration of high-voltage switched-capacitor (SC) converters with the goal of fully integrated power management solutions for system-on-chip (SoC) and system-in-package (SiP) applications. The full integration of SC converters provides a low cost and compact power supply solution for modern electronics. Currently, there are almost no fully integrated SC converters with input voltages above 5 V. The purpose of this work is to provide solutions for higher input voltages. The increasing challenges of a compact and efficient power supply on the chip are addressed. High-voltage rated components and the increased losses caused by parasitics not only reduce power density but also efficiency. Loss mechanisms in high-voltage SC converters are investigated resulting in an optimized model for high-voltage SC converters. The model developed allows an appropriate comparison of different semiconductor technologies and converter topologies. Methods and design proposals for loss reduction are presented. Control of power switches with their supporting circuits is a further challenge for high-voltage SC converters. The aim of this work is to develop fully integrated SC converters with a wide input voltage range. Different topologies and concepts are investigated. The implemented fully integrated SC converter has an input voltage range of 2 V to 13 V. This is twice the range of existing converters. This is achieved by an implemented buck and boost mode as well as 17 conversion ratios. Experimental results show a peak efficiency of 81.5%. This is the highest published peak efficiency for fully integrated SC converters with an input voltage > 5 V. With the help of the model developed in this work, a three-phase SC converter topology for input voltages up to 60 V is derived and then investigated and discussed. Another focus of this work is on the power supply of sensor nodes and smart home applications with low-power consumption. Highly integrated micro power supplies that operate directly from mains voltage are particularly suitable for these applications. The micro power supply proposed in this work utilizes the high-voltage SC converter developed. The output power is 14 times higher and the power density eleven times higher than prior work. Since plenty of power switches are built into modern multi-ratio SC converters, the switch control circuits must be optimized with regard to low-power consumption and area requirements. In this work, different level shifter concepts are investigated and a low-power high-voltage level shifter for 50 V applications based on a capacitive level shifter is introduced. The level shifter developed exceeds the state of the art by a factor of more than eleven with a power consumption of 2.1 pJ per transition. A propagation delay of 1.45 ns is achieved. The presented high-voltage level shifter is the first level shifter for 50 V appli-

cations with a propagation delay below 2 ns and power consumption below 20 pJ per transition. Compared to the state of the art, the figure of merit is significantly improved by a factor of two. Furthermore, various charge pump concepts are investigated and evaluated within the context of this work. The charge pump, optimized in this work, improves the state of the art by a factor of 1.6 in terms of efficiency. Bidirectional switches must be implemented at certain locations within the power stage to prevent reverse conduction. The topology of a bidirectional switch developed in this work reduces the dynamic switching losses by 70% and the area consumption including the required charge pumps by up to 65% compared to the state of the art. These improvements make it possible to control the power switches in a fast and efficient way.

Index terms — integrated power management, high input voltage, multi-ratio SC converter, level shifter, bidirectional switch, micro power supply

Zusammenfassung

Der Schwerpunkt dieser Arbeit liegt auf der Erforschung von Switched-Capacitor (SC) Spannungswandler für höhere Eingangsspannungen. Ziel der Arbeit ist es, Lösungen für ein voll auf dem Halbleiterchip integriertes Power Management anzubieten, um System on Chip (SoC) und System in Package (SiP) zu ermöglichen. Die vollständige Integration von SC Spannungswandlern bietet eine kostengünstige und kompakte Spannungsversorgungslösung für moderne Elektronik. Der kontinuierliche Trend hin zu immer kompakterer Elektronik und hin zu höheren Versorgungsspannungen wird in dieser Arbeit adressiert. Aktuell gibt es sehr wenige voll integrierte SC Spannungswandler mit einer Eingangsspannung größer 5 V. Die mit steigender Spannung zunehmenden Herausforderungen an eine kompakte und effiziente Spannungsversorgung auf dem Chip werden in dieser Arbeit untersucht. Die höhere Spannungsfestigkeit der verwendeten Komponenten korreliert mit erhöhten Verlusten und erhöhtem Flächenverbrauch, welche sich negativ auf den Wirkungsgrad und die Leistungsdichte von SC Spannungswandlern auswirken. Bestandteil dieser Arbeit ist die Untersuchung dieser Verlustmechanismen und die Entwicklung eines Modells, welches speziell für höhere Spannungen optimiert wurde. Das vorgestellte Modell ermöglicht zum einen die optimale Dimensionierung der Spannungswandler und zum anderen faire Vergleichsmöglichkeiten zwischen verschiedenen SC Spannungswandler Architekturen und Halbleitertechnologien. Demnach haben sowohl die gewählte Architektur und Halbleitertechnologie als auch die Kombination aus gewählter Architektur und Technologie erheblichen Einfluss auf die Leistungsfähigkeit der Spannungswandler. Ziel dieser Arbeit ist, die Vollintegration eines SC Spannungswandlers mit einem weiten und hohen Eingangsspannungsbereich zu entwickeln. Dazu wurden verschiedene Schaltungsarchitekturen und Konzepte untersucht. Der vorgestellte vollintegrierte SC Spannungswandler weist einen Eingangsspannungsbereich von 2 V bis 13 V auf. Dies ist eine Verdopplung im Vergleich zum Stand der Technik. Dies wird durch einen implementierten Auf- und Abwärtswandler-Betriebsmodus sowie 17 Übersetzungsverhältnisse erreicht. Experimentelle Ergebnisse zeigen einen Spitzenwirkungsgrad von 81.5%. Dies ist der höchste veröffentlichte Spitzenwirkungsgrad für vollintegrierte SC Spannungswandler mit einer Eingangsspannung größer 5 V. Mit Hilfe des in dieser Arbeit entwickelten Modells wird eine dreiphasige SC Spannungswandler Architektur für Eingangsspannungen bis zu 60 V entwickelt und anschließend analysiert und diskutiert.

Ein weiterer Schwerpunkt dieser Arbeit adressiert die kompakte Spannungsversorgung von Sensorknoten mit geringem Stromverbrauch für Anwendungen wie Smart Home und Internet der Dinge (IoT). Für diese Anwendungen eignen sich besonders gut hochintegrierte Mikro-Netzteile, welche direkt mit dem $230V_{\text{RMS}}$ -Hausnetz (bzw. $110V_{\text{RMS}}$) betrieben werden können. Das in dieser Arbeit vorgestellte Mikro-Netzteil nutzt einen in dieser Arbeit entwickelten SC Spannungswandler für hohe Eingangsspannungen. Die damit erzielte Ausgangsleistung ist 14-mal größer im Vergleich zum Stand der Technik.

In SC Spannungswandlern für hohe Spannungen werden viele Leistungsschalter benötigt, deshalb muss bei der Schalteransteuerung besonders auf einen geringen Leistungsverbrauch und Flächenbedarf der benötigten Schaltungsblöcke geachtet werden. Gegenstand dieser Arbeit ist sowohl die Analyse verschiedener Konzepte für Pegelumsetzer, als auch die Entwicklung eines stromsparenden Pegelumsetzers für 50 V-Anwendungen. Mit einer Leistungsaufnahme von 2.1 pJ pro Signalübergang reduziert der entwickelte Pegelumsetzer mit kapazitiver Kopplung um mehr als elfmal die Leistungsaufnahme im Vergleich zum Stand der Technik. Die erreichte Laufzeitverzögerung beträgt 1.45 ns. Damit erzielt der vorgestellte Hochspannungs-Pegelumsetzer als erster Pegelumsetzer für 50 V-Anwendungen eine Laufzeitverzögerung unter 2 ns und eine Leistungsaufnahme unter 20 pJ pro Signalwechsel. Im Vergleich zum Stand der Technik wird die Leistungskennzahl um den Faktor zwei deutlich verbessert. Darüber hinaus werden im Rahmen dieser Arbeiten verschiedene Ladungspumpenkonzepte untersucht und bewertet. Die in dieser Arbeit optimierte Ladungspumpe verbessert den Stand der Technik um den Faktor 1.6 in Bezug auf den Wirkungsgrad. Die in dieser Arbeit entwickelte Schaltungsarchitektur eines bidirektionalen Schalters reduziert die dynamischen Schaltverluste um 70% und den benötigten Flächenbedarf inklusive der benötigten Ladungspumpe um bis zu 65% gegenüber dem Stand der Technik. Diese Verbesserungen ermöglichen es, die Leistungsschalter schnell und effizient anzusteuern.

Schlagworte — Integriertes Powermanagement, hohe Eingangsspannung, Multi-Ratio SC Spannungswandler, Pegelumsetzer, bidirektionaler Schalter, Mikro-Netzteil

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1 Introduction

In recent years, many new applications have emerged in areas such as the Internet of Things IoT, smart homes, mobile devices, autonomous cars and e-mobility. The power supply for these applications is a key challenge and a strong driver for integrated power management. Modern power supplies are required to have the same or higher output power at lower area consumption and lower cost without losing any functionality [1–3].

In the field of power management a trend towards higher integration with the goal of full IC-level integration has been observed in recent years. Figure 1.1 shows this trend beginning with multiple bulky external passives leading to smaller and higher integrated components. Generally, output power decreases with higher integration level due to the lower values of the integrated passives. However, this still corresponds to an ever increasing number of applications, as the power consumption of many applications continues to decrease. Higher integration enables higher switching frequencies which reduces the size of the passives to a level where on-chip integration is possible. Furthermore, a higher integration level facilitates new topologies and concepts that increase power density and efficiency. In addition to efficiency, lifetime also

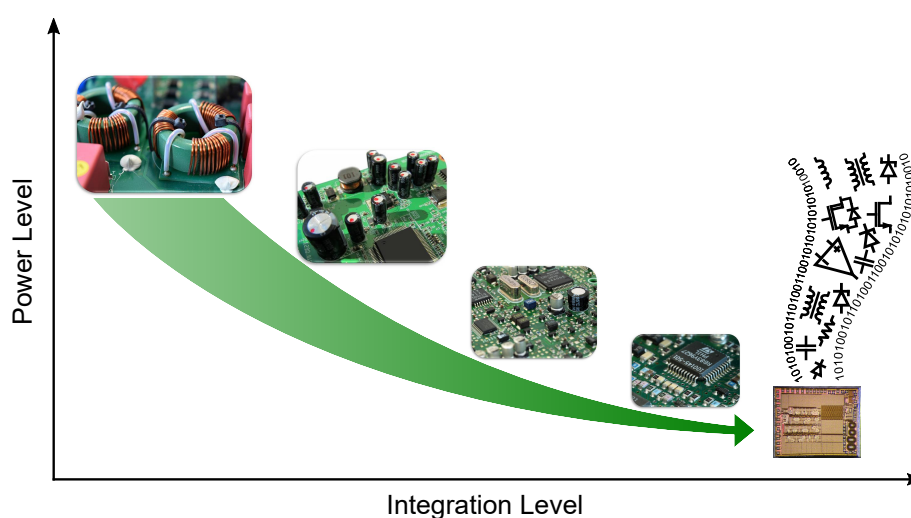


Fig. 1.1: Integration trend of power electronics.

increases, and weight and costs decrease [3]. This gives new freedom for system design and enables compact power electronics applications. Many applications require different voltage levels, that in many cases need to be dynamically adjustable depending on the required load [4–9]. This leads to decentralized energy management and division into individual small power supplies. Several smaller power supplies have a number of advantages compared to a single power supply, as they can be optimized for specific usage and are easier to integrate due to the lower power level. These power supplies can be realized by different DC-DC converter types. In addition to classic inductive converters, there are SC converters, which use capacitance recharging. They offer compact design and good on-chip integration capability.

The requirements for the power supply are defined by the application. Electrical parameters, such as efficiency, output power and input voltage range, are important. Many areas of application increasingly demand small sizes, low form factors and low weight. These parameters especially for portable applications which are mostly battery powered, have a strong influence on system performance. Application examples include e-bikes, e-scooters, lawnmowers, robotic vacuum cleaners and drones. In addition to the drive unit these applications typically include a power supply (DC-DC converter) for the control electronics which comprise sensors, actuators and micro controllers. The input voltages required for the DC-DC converter depend on the application specific nominal battery voltage level, which are, for example, between 7.2 V and 18 V for vacuum robots, between 18 V and 36 V for lawnmowers, between 24 V and 36 V for e-bikes and up to 72 V for Segways. This results in a demand for high input voltages and large input voltage ranges needing to be covered. In order to supply the control unit the input voltage must be converted with an appropriate efficiency to a voltage of typically 5 V or less. The power consumption of the control unit for such devices are approximately 1 mW to 10 W [10, 11].

One particular challenge is the compact and efficient power supply for internet of things (IoT) applications [12]. By 2020, the number of connected devices is expected to exceed 50 billion [13]. For years, progress has been made in the field of energy harvesting. However, indoor energy sources are limited and usually not reliably available [14]. Batteries would be an alternative source, but have the disadvantage of being high maintenance. Mains voltage, however, is a reliable and practically unlimited energy source for indoor applications. Micro power supplies which are connected directly to the mains could be suitable for the supply of sensor nodes, which are required for room monitoring, building control, indoor navigation and more. These applications consume particularly little power in the low mW range. The compact micro power supplies recently presented in [15–18] could be a possible solution. However, they only deliver low power in the sub-mW range.

The trend towards higher input voltages and higher integration level of power supplies can be observed in many applications. Currently, there is a gap between the demands for fully integrated power supplies and existing converters and concepts. In recent years, the main focus in research has been on SC converters with

lower input voltages of less than 5 V [4, 5, 7, 9, 19–40]. There is a large number of different concepts and converters that achieve fully integrated output powers of up to 1.65 W [5, 30]. However, the range above 5 V input voltage is rarely covered [41–44].

There are only a few fully integrated high-voltage SC converters due to the challenges of high-voltage SC converter design. The focus of this work is on high-voltage SC converters. Since the term "high-voltage" is technically not clearly defined and can be used for voltages starting from a few volts and range up to several kVs, it is defined in this work as follows. The term "low voltage" describes voltages that are equal to or lower than the oxide breakdown voltage of the digital core voltage of the CMOS technology used. The typical low-voltage level is lower than 5 V for the CMOS technologies considered in this work [45–47]. All voltages over this level are considered "high-voltage". Additional challenges arise in the design of SC converters over this voltage level. With increasing voltages the voltage maximum ratings of the components, e.g. capacitors and transistors, also need to be higher. High-voltage transistors require a larger die area and cause higher gate charge losses compared to low-voltage transistors. Likewise, for capacitors, the capacitance density decreases. Each parasitic capacitance which is charged or discharged causes losses that increase with the square of the voltage. This limits both the output power and the efficiency. Unlike low-voltage designs, many power switches in a high-voltage domain require supporting circuits, such as a level shifter and a charge pump. Since the power stage usually consists of many power switches, the supporting circuits must be optimized for implementation in high-voltage SC converters with regard to power consumption, area consumption, and component voltage ratings. The output power achievable and the availability of suitable high-voltage low-power supporting circuits are the main limitations for the full integration of high-voltage SC converters.

1.1 Scope of this Work

Figure 1.2 summarizes and illustrates the scope of this work. The goal is to fully integrate high-voltage SC converters and achieve fully integrated power management solutions for modern electronics. The trend towards higher integration levels and more powerful voltage supplies operating at higher input voltages poses new challenges. Increased maximum voltage ratings of the components result not only from the increase in input voltage in particular, but also from voltage range. The focus of this work is on fully integrated SC converters in the range below 100 mW with input voltages of up to 60 V and output voltages below 5 V. Losses caused by parasitic effects and other aspects, such as component requirements, increase with increasing voltage. These reduce output power and efficiency. New supporting circuit concepts and converter topologies are essential. These challenges are addressed in this work by the following:

1. Elaborating design aspects and guidelines for the design of integrated high-voltage SC converters.
2. Investigations into the impact of high-voltage effects on losses and elaboration of concepts to reduce these losses.
3. Investigation and optimization of high-voltage supporting circuits that address the requirements for fully integrated high-voltage SC converters.
4. Investigation and evaluation of fully integrated high-voltage converter topologies and development of a suitable high input-voltage SC converter topology.
5. Investigation and analysis of micro power supplies, derivation and implementation of a micro power supply concept for mains operation so as to increase output power and power density. This micro power supply, developed as part of this work, utilizes high-voltage SC converters.

1.2 Outline of this Work

After this introductory chapter, Chapter 2 highlights the motivation for and the demands of designing and building highly integrated SC converters. Section 2.2 explains the basics and the operating principles of SC converters. Loss mechanisms as well as the modeling of a SC converter are explained in Section 2.3. In addition to power switches, capacitors are one of the most important components within an integrated SC converter. The different capacitors available in CMOS technologies are described in Section 2.4. Section 2.5 provides an overview of the various standard SC converter topologies. Possible control concepts are explained in Section 2.6.

Chapter 3 describes the design and the challenges it has with regards to integrated high-voltage SC converters. Section 3.1 compares low and high-voltage SC converters and the associated requirements and challenges. The resulting design aspects and a design guideline lead to a model optimized for high-voltage SC converters, described in Section 3.2. Based on the model presented different CMOS technologies are investigated and evaluated with regard to their high-voltage capabilities in Section 3.3. In Section 3.4, different SC converter concepts and topologies are described and compared beginning with the state of the art. In Section 3.4.1 a topology for a fully integrated SC converter with a wide input voltage range is presented and discussed. The evaluation of the implemented topology will be discussed later in Chapter 5. Section 3.4.2 presents a three-phase SC converter topology which was developed within the context of this work.

Chapter 4 examines supporting circuits, which are an essential part of high-voltage SC converters, required for the control of the power switches, including level shifters and charge pumps. Section 4.1 first describes and evaluates conventional level shifters. In Section 4.1.2, the capacitive high-speed and power-efficient

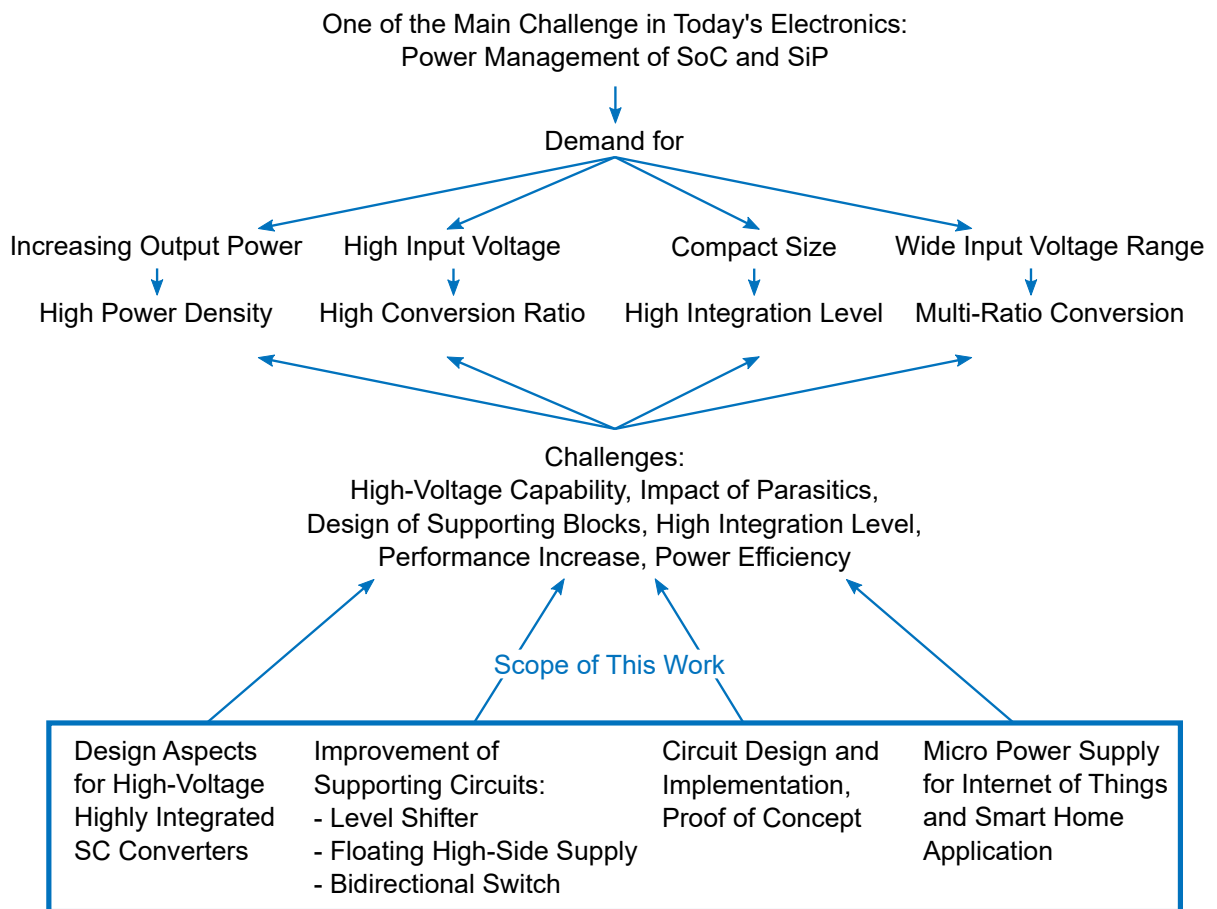


Fig. 1.2: Scope of this work.

high-voltage level shifter developed in this work is presented, and the design implementation is described. In Section 4.1.3, the level shifter presented is investigated, verified and compared with the state of the art. In Section 4.2, different charge pump concepts are analyzed and evaluated. In order to make optimal use of the various floating high-side supplies, the concepts are prioritized according to the application. In Section 4.3, a novel bidirectional switch topology is presented which shows significantly lower dynamic switching losses compared to conventional topology. Finally, Section 4.4 presents a method for reducing parasitic bottom-plate losses.

Chapter 5 explains the sizing and implementation of the fully integrated high-voltage SC converter proposed in Section 3.4.1. The topology was implemented in a $0.35\ \mu\text{m}^2$ CMOS technology and verified by measurements. Section 5.1 describes the system architecture and in Section 5.2 the implementation of the transistor level of the power stage is discussed. Section 5.3 introduces the implementation circuit for buck and boost operations. The control of the SC converter is shown in Section 5.4. In Section 5.5 design aspects and optimal sizing are described. The parasitic pnp-bipolar effect that can occur in low-cost CMOS technologies is investigated in Section 5.6. Section 5.7 contains the experimental results of the high-voltage SC converter implemented, which are then compared to the state of the art in Section 5.8.

The power supply is a key challenge for smart home and industry 4.0 applications. Possible energy sources are analyzed in Section 6.1, different concepts and their limits discussed in Section 6.2. The architecture of the proposed micro power supply is derived in Section 6.3, which consists of a mains-coupled AC-DC converter and a subsequent high-voltage DC-DC converter, both fully integrated on the chip. The design and implementation of the AC-DC and the DC-DC converter is described in Sections 6.4 and 6.6, respectively. The sizing of the DC link capacitor is described in Section 6.5. Followed by the measurement results of the manufactured micro power supply presented in Section 6.7.

1.3 Contributions of this Work

The following list summarizes the main outcome and the contributions of this work.

1. A major difference of SC converters for high input voltages in comparison to low voltages is that components with several different voltage classes have to be used. The SC converter model proposed in this work incorporates these requirements. It enables technology and voltage-dependent weighting and optimized sizing. It is not only optimized for the lowest output resistance, but also for a loss minimum. The model presented enables a proper comparison of SC converter concepts under equal conditions. Since the technology has a significant influence on converter performance, the model also provides the opportunity to evaluate and properly compare different semiconductor technologies. By

means of the model presented a promising three-phase SC converter topology which operates for input voltages up to 60 V is developed and discussed.

2. In low-power applications an efficient and compact floating high-side supply is crucial, especially in systems with multiple switches. For the source-supplied charge pump in this work, a circuit published earlier for discrete electronics is utilized and optimized for on-chip integration. As a result, full integration of the charge pump is achieved, and the efficiency was improved by a factor of about 1.6 compared to the self-boost charge pump proposed in prior art. The source-supplied charge pump proposed was published in IEEE Journal of Emerging and Selected Topics in Power Electronics in 2018 [44].
3. One of the major challenges in today's high-voltage electronics is the control of the power switches. The level shifter must cope with high-voltages and high switching frequencies. The high-speed and high-voltage level shifter proposed in this work is based on a capacitive level shifter that transmits the signals via two capacitors to the high-side voltage domain. The switching node falling edge detection introduced enables a robust and reliable signal detection for voltage slopes up to 6 V/ns, and is verified by measurement. Simulations have shown that the circuit works reliably at slopes up to 100 V/ns. A maximum switching frequency of 120 MHz is achieved. The power consumption is only 2.1 pJ per transition improving the state of the art by a factor of more than eleven. Thus, the level shifter presented is the first level shifter for 50 V applications which consumes less than 20 pJ per transition, and the first published level shifter for 50 V with a propagation delay less than 2 ns. Furthermore, this work points out the importance of minimizing the losses caused by parasitic isolation well capacitance. This is achieved by a compact design. A figure of merit (FOM) specifically derived for level shifters, which takes into account power consumption, propagation delay, technology size and maximum voltage capability, is used for comparison with the state of the art. The level shifter presented in this work improves the state-of-the-art FOM by a factor of two. The proposed level shifter was published at ESSCIRC 2018 [48].
4. Due to the reconfiguration of multi-ratio SC converters some switches in the power stage have to be bidirectional switches, which is usually realized by back-to-back transistor configuration. The proposed back-to-back switch topology in this work reduces the dynamic gate charge losses by more than 70% compared to conventional back-to-back switch topology. The area consumption of the power switches is increased by a factor of about two compared to the standard solution, depending on the design trade-off. If the area consumption of the required charge pumps is taken into account, the total area consumption is reduced by up to 65% compared to the state of the art. The loss and area optimized back-to-back switch topology proposed in this work was filed for patent under the numbers

DE102015011396A1 and WO2017036592A1. The back-to-back switch topology was published at ISSCC 2016 [41].

5. The trend towards fully integrated power supplies with a wide and high input voltage range has continued strongly in recent years. The proposed fully integrated SC converter contributes to fulfilling this demand. It covers a wide and a high input voltage range by utilizing buck and boost mode. A fine granular coverage of the entire input voltage range is achieved with a total of 17 ratios. The absolute input voltage range was doubled compared to the state of the art and ranges from 2 V to 13 V. The peak efficiency of 81.5% is the highest published efficiency for fully integrated SC converters with an input voltage greater than 5 V and represents a significant improvement compared to the state of the art. The target output voltage is set at 5 V and can be scaled down to 3.3 V. An output power of 10 mW on an active area of 6.8 mm² is achieved. The proposed fully integrated buck-boost SC converter was published at ISSCC 2016 [41].

6. The micro power supply presented in this work, is designed to power small IoT sensor nodes, which are increasingly required for smart home and industry 4.0 applications. The proposed micro power supply is fabricated in a 700 V ultra-high voltage CMOS technology. It can be connected directly to the mains (either 110 V or 230 V). The two-stage approach comprises a fully integrated SC converter with a high input voltage of up to 17 V. The proposed micro power supply achieves an output power of 3 mW, which is an improvement by a factor of 14 compared to prior art. The chip area of 7.7 mm², results in a power density of 390 μW/mm². This is eleven times better than previous designs. The proposed micro power supply was published at ESSCIRC 2016 [49] and in the IEEE Journal of Emerging and Selected Topics in Power Electronics in 2018 [44] and even received the journal's 2019 First Prize Paper Award.

2 Switched-Capacitor DC-DC Converter Fundamentals

2.1 Motivation

The trend towards more compact and smaller power supplies is increasing, as shown in Fig. 1.1. The goal of this work is the full integration of voltage converter and application on the same chip. The main drivers in modern electronic are cost, size, weight, efficiency and reliability. For the voltage conversion in such applications there are three common principles, the linear voltage regulator, the inductive voltage converter and the capacitive voltage converter. These three types of converters are shown in Fig. 2.1 and are described below and evaluated with regard to their suitability for integration on-chip.

Linear Voltage Regulator

A linear voltage regulator consists of an adjustable resistor R connected in series between the input voltage and the output voltage as shown in Fig. 2.1(a). The adjustable resistor is usually replaced by a NMOS or PMOS transistor for on-chip implementation. The linear voltage regulator can be realized on-chip. By means of the reference voltage, the output voltage can be set variable or fixed. However, the output voltage is always lower than the input voltage. Boost operation is not possible. The losses occur almost exclusively

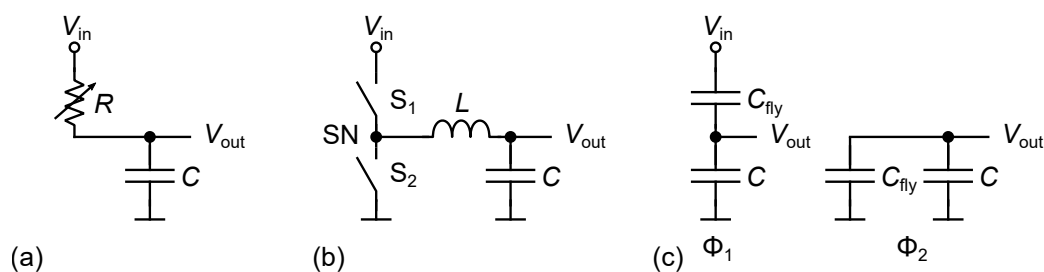


Fig. 2.1: DC-DC voltage conversion concepts (a) linear voltage regulator (b) inductive voltage conversion and (c) capacitive voltage conversion.

in the adjustable resistor and are calculated from the voltage difference between input voltage and output voltage $P_{\text{loss}} = (V_{\text{in}} - V_{\text{out}}) \cdot I_{\text{out}}$. The efficiency of the linear voltage converter can be calculated as follows:

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} = \frac{V_{\text{out}} \cdot I_{\text{out}}}{(V_{\text{out}} + V_{\text{in}} - V_{\text{out}}) \cdot I_{\text{out}}} = \frac{V_{\text{out}}}{V_{\text{in}}}. \quad (2.1)$$

As (2.1) indicates that the efficiency depends on the voltage conversion ratio (VCR) of $V_{\text{out}}/V_{\text{in}}$ and decreases with increasing voltage difference between V_{in} and V_{out} , which is indicated by a smaller value of VCR. Hence, linear voltage regulator is mostly used in applications with small voltage differences between input and output voltage or in applications that require a precisely regulated output voltage with low-voltage ripple.

Inductive Voltage Converter

An inductive switch-mode power supply (SMPS) is an efficient possibility to convert the voltage. Figure 2.1(b) shows an inductive step-down converter. The switches S_1 and S_2 are turned on and off in reverse phase creating a pulsating voltage with an amplitude of V_{in} at the switching node SN. This voltage is converted into a constant output voltage V_{out} by means of the LC filter consisting of L and C . The duty cycle of the switch S_1 and S_2 controls the output voltage. Thus, the VCR between input and output can be freely adjusted over a wide range. In addition, inductive converters can be designed as step-up and step-down converters. The efficiency outperforms by far the efficiency of the linear voltage regulator, especially in case of larger voltage differences between V_{in} and V_{out} . Inductive switch-mode power supplies are used in many applications. However, full integration suffers from poor inductance integration. Expensive post-processing can improve the quality and the inductance value, but still only small inductance values can be realized on-chip. Currently, there are great efforts to realize inductors on-chip with high quality and larger inductance values, but these are not yet available. Due to cost, this option may only be suitable for some applications. Therefore, currently external inductors are used, this contradicts the goal of full integration.

Switched-Capacitor Converter

Another possibility is to convert the voltage capacitively. Figure 2.1(c) shows a switched-capacitor (SC) converter. SC converters essentially consist of switches and capacitors that transport the charge from the input to the output. Both power switches and capacitors in different types and voltage classes are available in all low cost CMOS technologies. This enables full integration of the voltage converter. SC converters usually operate in two equally long phases, in this case the capacitors are charged in series during the first phase ϕ_1 . In phase ϕ_2 , the flying capacitor C_{fly} is now connected in parallel to the other capacitor

and the output and charge flows to the output. SC converters consists of fixed and flying capacitors. The fixed capacitors are usually used to buffer the charge, while the flying capacitors are responsible for charge transportation. For SC converters, the circuit topology defines the VCR and not like the inductive based converters by the duty cycle. The topology in Fig. 2.1(c) realizes an ideal voltage conversion ratio (iVCR) of 2:1. A high efficiency, theoretical without any losses of 100%, can be achieved when operating at iVCR, but if the operating point shifts, the efficiency is reduced and becomes comparable to a linear voltage regulator. The ideal theoretical efficiency for a SC converter can be described by the LDO efficiency equation (2.1) and the ideal iVCR. Since the input voltage V_{in} of a SC converter is divided by the ratio, iVCR must be multiplied by the input voltage V_{in} . This results in the theoretically maximum possible efficiency:

$$\eta = \frac{V_{out}}{V_{in} \cdot iVCR} \cdot 100\% \quad (2.2)$$

For increasing the efficiency over a wide input voltage range, multiple VCRs can be used. Multi-ratio converters realize different VCRs depending on the operating point. The finer the gradation of the VCRs, the higher the theoretical average efficiency. Figure 2.2 shows the possible ratios depending on the number of flying capacitors for a two phase SC converter [50]. Ratios 1 and 1/2 can be realized with one flying capacitor. By using three flying capacitors, the theoretical average efficiency can be increased from 71% to 90% for the given input voltage range in Fig. 2.2. For comparison, the efficiency curve of an ideal linear voltage regulator (as described in Section 2.1) is shown. The efficiency of multi-ratio SC converters increases significantly compared to the linear voltage regulator as the conversion ratio rises, as shown in Fig. 2.2.

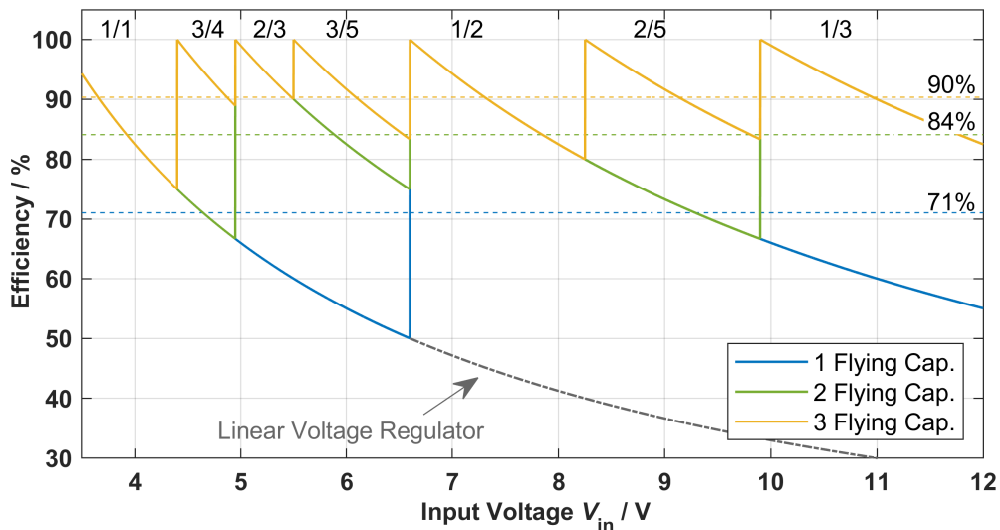


Fig. 2.2: Theoretical maximum possible efficiency of a SC converter with an output voltage $V_{out} = 3.3$ V for one, two and three flying capacitors.

The ideal efficiency is reduced by charge balancing, I_{out} and by control losses. However, especially for lower output power in the mW to W range, high efficiencies of 85% and higher can be achieved [4,9,20,23,32,51,52]. Capacitive voltage conversion is a promising approach for full integration of voltage converters with a wide input voltage range as well as with high input voltages. Above all, the IC level integration of both switches and capacitors enables on-chip power management. The focus of this work is therefore exclusively on SC converters. In the following the functionality and the fundamentals of the SC converters are described. First the SC converter equivalent model is introduced, that models the different losses in a SC converter. Afterwards, the occurring losses are categorized and analyzed.

2.2 Switched-Capacitor Converter Operation Principle

A capacitive direct current to direct current (DC-DC) converter consists of flying and buffer capacitors. Flying capacitors are responsible for the charge transport, while the buffer capacitors stabilize and buffer the voltage. The voltage conversion ratio of a SC converter is determined by the circuit topology. Various topologies can be utilized to build SC converters. Section 2.5 gives an overview of different SC converter topologies. Figure 2.3 shows the operating principle of a SC converter for the 2:1 series-parallel SC converter of Fig. 2.1(c). The clock period of an SC converter consists usually of two phases, phase ϕ_1 and phase ϕ_2 . The duty cycle of the two phases is 50%. A short dead time between the clock phases ϕ_1 and ϕ_2 is required to avoid cross-currents. The switches are turned on either in phase ϕ_1 or ϕ_2 as indicated in Fig. 2.3.

The energy transfer between input and output takes place through the flying capacitance C_1 . In phase ϕ_1 , C_1 and the output V_{out} are in series charged from the input voltage V_{in} . In phase ϕ_2 , C_1 is connected in parallel to the output V_{out} . In both phases charge is transferred to the output. In the steady state, the capacitor C_1 has the same voltage value as V_{out} due to charge balancing. The output voltage V_{out} corresponds ideally and

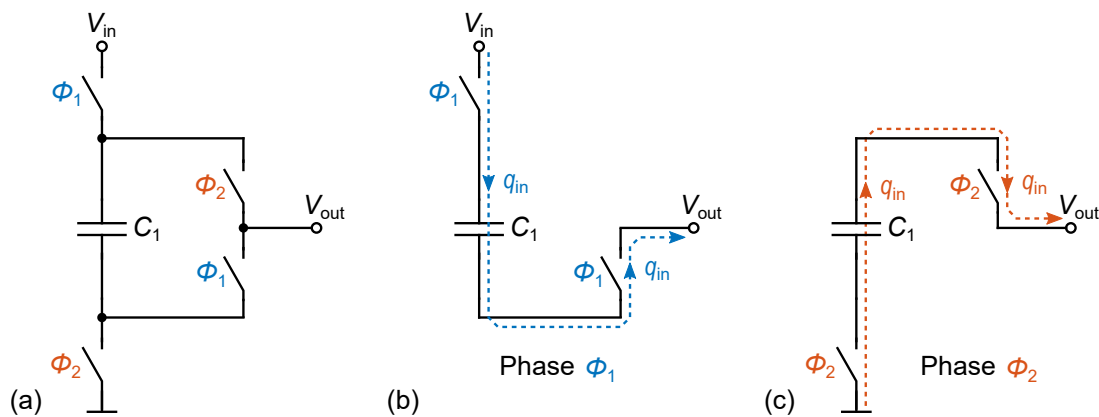


Fig. 2.3: Functional principle of a series-parallel 2:1 SC converter in two-phase configuration.

without load exactly to half of the input voltage V_{in} . This results in a VCR of 2:1, which is independent of the sizing of the capacitor and is only defined by the topology. In case of a load current, the charge must be transferred between input and output. The capacitors of the converter are discharged and must be recharged. This leads to charging and discharging losses as well as to a voltage drop and ripple of the output voltage. This voltage drop depends on the output current I_{out} , the switching frequency f_{sw} , the topology and the sizing of the SC converter.

2.3 Modeling and Loss Mechanisms of Switched-Capacitor Converters

SC converters can be described by the model shown in Fig. 2.4. It consists of an ideal transformer which represents the ideal voltage conversion ratio $iVCR$. The different losses are represented by the output resistance R_{out} and the parallel resistance R_p . In R_{out} all intrinsic losses caused by the energy transport from the input to the output are modeled. In R_p the extrinsic losses are described, which are caused by the control of the power switches and by parasitic effects. The output voltage results from the ideal output voltage $V_{out,ideal}$ minus the voltage drop over R_{out} caused by the output current I_{out} .

In the following, the losses occurring in a SC converter are described, that reduce the efficiency and the output voltage of the SC converter.

These losses are modeled by R_{out} (Section 2.3.1):

- $P_{R_{out}}$: Including all intrinsic losses, such as charge losses of capacitors and resistive losses in power switches

The following losses are modeled by R_p (Section 2.3.2):

- P_{gate} : Gate charging losses of the power switches
- P_{ctrl} : Losses caused by controlling the power switches. These include the losses caused by level shifters, charge pumps and gate drivers

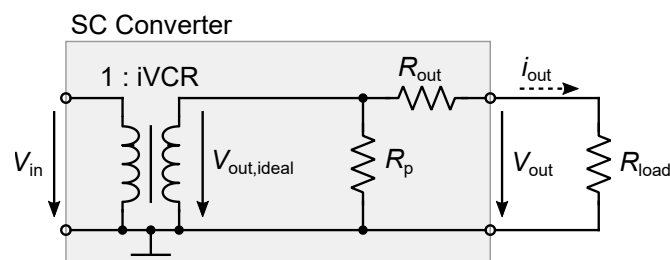


Fig. 2.4: SC converter equivalent circuit diagram.

- P_{Cbp} : Losses caused by recharging the parasitic bottom-plate capacitance of the flying capacitors C_{fly}
- P_{well} : Losses caused by recharging the isolation wells

2.3.1 Modeling of the Output Resistance R_{out}

In this section the modeling of R_{out} from Fig. 2.4 and its impact on the losses and the operation point of a SC converter is described. The calculation is based on the charge flow analysis [53,54], which optimizes the intrinsic losses of a SC converter. The output resistance comprises the recharging losses of the capacitors as well as the resistive losses in the power switches. Both components depend on the charge flowing through the capacitors and power switches. Figure 2.3 shows the charge flow vectors in the 2:1 SC converter cell. This analysis is the basis for the calculation of R_{out} and can be applied to any complex SC converter topology. For each phase j a charge flow vector is created for both the capacitors $a_c^{(j)}$ and the power switches $a_r^{(j)}$. The definition $q_{out} = \sum q_{in}^{(j)}$ yields the vector

$$\begin{aligned} a_c^{(j)} &= \begin{bmatrix} q_{out}^{(j)} & q_{C,1}^{(j)} & \dots & q_{C,i}^{(j)} & q_{in}^{(j)} \end{bmatrix} / q_{out} \\ &= \begin{bmatrix} a_{out}^{(j)} & a_{C,1}^{(j)} & \dots & a_{C,i}^{(j)} & a_{in}^{(j)} \end{bmatrix} \end{aligned} \quad (2.3)$$

for the capacitors and the equivalent vector

$$\begin{aligned} a_r^{(j)} &= \begin{bmatrix} q_{out}^{(j)} & q_{R,1}^{(j)} & \dots & q_{R,i}^{(j)} & q_{in}^{(j)} \end{bmatrix} / q_{out} \\ &= \begin{bmatrix} a_{out}^{(j)} & a_{R,1}^{(j)} & \dots & a_{R,i}^{(j)} & a_{in}^{(j)} \end{bmatrix} \end{aligned} \quad (2.4)$$

for the power switches. The symbol i represents one element from the number of capacitors or one element from the number of power switches. With the charge flow analysis, the ideal conversion ratio iVCR for any topology can be calculated as follows:

$$iVCR = \frac{\sum q_{in}^{(j)}}{\sum q_{out}} \quad (2.5)$$

Depending on the switching frequency f_{sw} of the converter, two operating modes, the slow switching limit (SSL) and the fast switching limit (FSL) mode, are defined [53]. At low frequencies, the output resistance is determined by the resistance R_{SSL} caused by the recharging of the capacitors C_i :

$$R_{SSL} = \sum_i^{caps} \sum_j^n \frac{(a_{C,i}^j)^2}{2 \cdot C_i \cdot f_{sw}} \quad (2.6)$$

For high switching frequency f_{sw} , R_{SSL} decreases because f_{sw} is in the denominator. For higher switching frequencies R_{FSL} takes over and dominates the output resistance. The resistance R_{FSL} comprises the on-resistance R_i of the power switches. However, R_{FSL} is a constant value, which is not a function of the switching frequency. R_{FSL} can be derived for n phases by

$$R_{FSL} = n \cdot \sum_i^{switches} \sum_j^n R_i \cdot (a_{R,i}^j)^2. \quad (2.7)$$

With (2.6) and (2.7) the output resistance R_{out} can be approximated sufficiently accurately from the two partial resistances R_{SSL} and R_{FSL} as follows [53]:

$$R_{out} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2}. \quad (2.8)$$

The intrinsic losses can be determined with R_{out} from (2.8) and the output current I_{out} ,

$$P_{Rout} = R_{out} \cdot I_{out}^2. \quad (2.9)$$

Figure 2.5 shows R_{out} over the switching frequency and is composed of R_{SSL} and R_{FSL} as given in (2.8). Thereby R_{SSL} is not only a function of the switching frequency, but also depends on the capacitance values C_i (refer to (2.6)). With increasing capacitance values the curve is shifted downwards and the crossing point

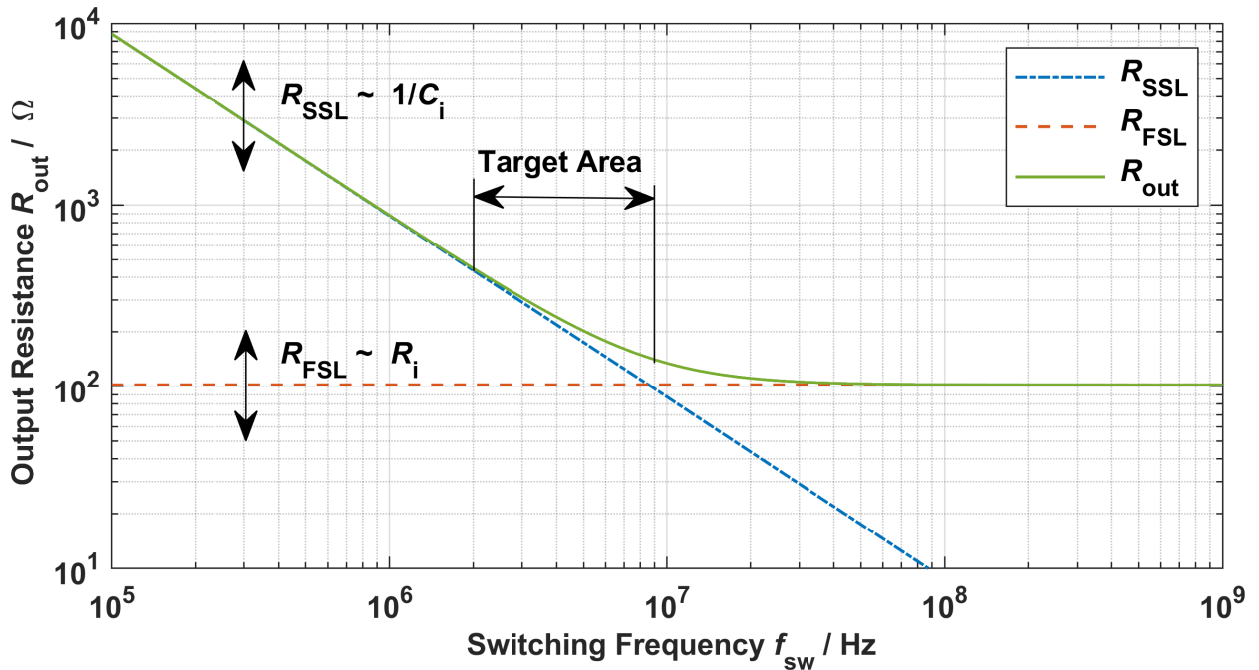


Fig. 2.5: Output resistance of a SC converter.

between R_{SSL} and R_{FSL} moves to lower frequencies. The value of R_{FSL} depends on the turn-on resistance of the power switches (refer to (2.7)). The lower the turn-on resistances, the lower the value of R_{FSL} . As a result, the intersection of R_{SSL} and R_{FSL} moves to higher frequencies. The optimum operating range is marked in Fig. 2.5. The sizing goal is to ensure that the peak efficiency of the SC converter is within this range. If the peak efficiency is at a lower frequency, this indicates that the turn-on resistances have been designed too small and the efficiency could be further improved by adjusting the transistor size. If the peak efficiency is at a higher switching frequency than indicated by the target area, the capacitance values or the turn-on resistance have been chosen too high and the efficiency could be further improved. To fully exploit the potential of the SC converter, the switching frequency at which the maximum performance is achieved should be within the limits shown in Fig. 2.5. The input voltage level has an indirect impact on the output resistance R_{out} . As the input voltage increases, the used devices must have a higher dielectric strength, which has a negative effect on the capacitance size and the turn-on resistance of the switches and results in an increase of R_{out} and higher losses.

2.3.2 Modeling of the Parallel Resistance R_p

This section describes the modeling of the extrinsic losses, associated with the parallel resistance R_p in Fig. 2.4.

Gate Charge Losses

To turn MOS transistors on or off, the gate capacitance must be recharged. The required energy adds to the extrinsic losses. The gate losses P_{gate} can be calculated from the gate capacitance C_{gate} , the voltage V_{GS} and the switching frequency f_{sw} :

$$P_{gate} = C_{gate} \cdot V_{GS}^2 \cdot f_{sw} \quad (2.10)$$

Integrated transistors are sized by the length L and the width W of the gate. With the oxide capacitance density C_{oxide} , C_{gate} can be approximated:

$$C_{gate} = W \cdot L \cdot C_{oxide} \quad (2.11)$$

The gate losses for n transistors depending on the sizing are derived by inserting (2.11) into (2.10):

$$P_{gate} = \sum_i^{i=n} W_i \cdot L_i \cdot C_{oxide} \cdot V_{GS}^2 \cdot f_{sw} \quad (2.12)$$

As the dielectric strength increases, the minimum length L of the high-voltage transistors increases, as well as the related width W , resulting in an increase in the gate area. Consequently, the gate capacitance may increase significantly and simultaneously the losses P_{gate} .

Modeling of the Switch Control Losses

In Fig. 2.6(a) a gate driver is used to control a ground-related MOS transistor. Each power transistor requires a gate driver. The gate driver losses P_{GD} , result from the sum of the used gate drivers n :

$$P_{\text{GD}} = \sum_i^{i=n} P_{\text{GD},i} \quad (2.13)$$

For the floating high-side transistor shown in Fig. 2.6(b), additional circuit blocks like level shifter and charge pump are required. The level shifter converts the control signal to the high-side voltage domain. The power consumption P_{LS} is determined at a certain frequency f_1 . Since the losses scale linearly with the switching frequency, the power consumption can be approximated by:

$$P_{\text{LS}} = \frac{P_{\text{LS},f1}}{f_1} \cdot f_{\text{sw}} \quad (2.14)$$

The charge pump in Fig. 2.6(b) provides the power for the level shifter and the gate driver. For a given high-side power P_{HS} and a charge pump efficiency η_{CP} , the power consumption required by the charge pump can be calculated:

$$P_{\text{CP}} = \frac{P_{\text{HS}}}{\eta_{\text{CP}}} \quad (2.15)$$

The transistor control losses can be calculated by equations (2.13), (2.14) and (2.15) for n switches i :

$$P_{\text{ctrl}} = \sum_i^{i=n} P_{\text{GD},i} + P_{\text{LS},i} + P_{\text{CP},i} \quad (2.16)$$

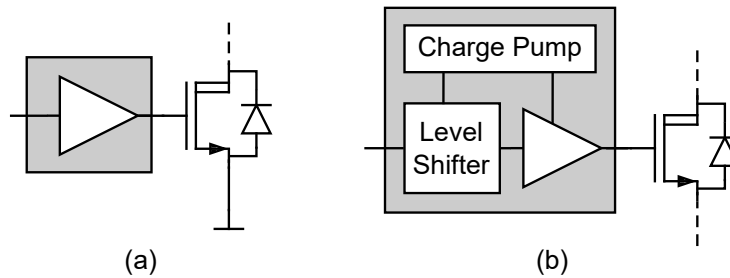


Fig. 2.6: Switch control concepts for (a) ground-related transistors and for (b) floating high-side transistors.

The total losses caused by the power switches and their control can be summarized as follows:

$$P_{sw,ctrl} = \sum_i^{i=n} P_{GD,i} + P_{LS,i} + P_{CP,i} + P_{gate,i} \quad (2.17)$$

Bottom-Plate Losses

For integrated capacitors in particular, parasitic substrate capacitance between the capacitor plates and the substrate are unavoidable. When the voltage at these parasitic capacitors changes, recharging losses occur, which are a significant part of the total losses in fully integrated SC converters. Figure 2.7(a) shows the parasitic capacitance C_{tp} between the top plate and the substrate and C_{bp} between the bottom plate and the substrate in a 2:1 series-parallel converter cell. Due to the structure (see Fig. 2.7(b)), the C_{tp} is much smaller than the C_{bp} and contributes additionally to the charge flow. Therefore, the losses caused by C_{tp} can be neglected in first order. The value of C_{bp} can be calculated by

$$C_{bp} = \alpha \cdot C_{fly} , \quad (2.18)$$

in which α is a technology-dependent factor. It depends on the type of capacitor and the technology and indicates the ratio between the parasitic and the main capacitance. Section 2.4 provides an overview of the different capacitor types available in standard CMOS technologies, typical values are $\alpha = 1\%$ to 5% depending on the capacitor type. The losses caused by charging and discharging C_{bp} within a switching period are calculated:

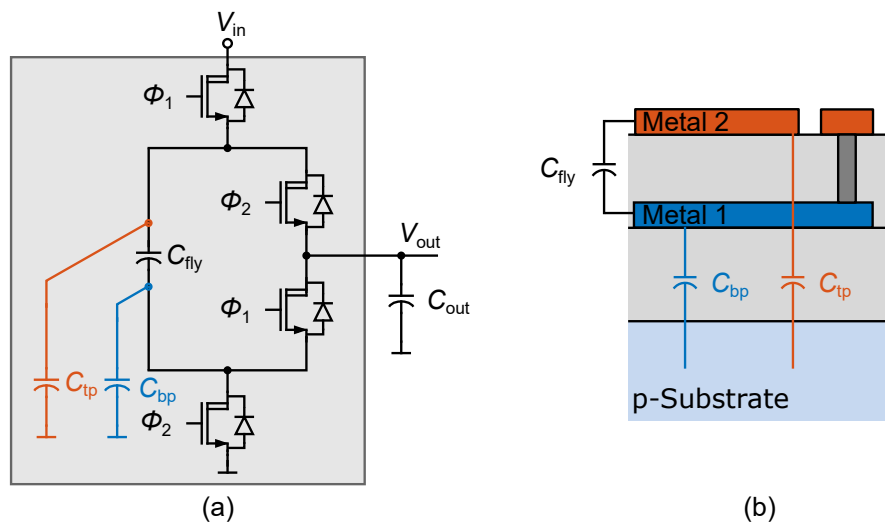


Fig. 2.7: The parasitic capacitance of an integrated MOM capacitance is depicted.

$$P_{\text{Cbp}} = \sum_i^{i=n} \alpha_i \cdot C_{\text{fly},i} \cdot \Delta V_{\text{bp},i}^2 \cdot f_{\text{sw}} \cdot \quad (2.19)$$

P_{Cbp} depends on the switching frequency f_{sw} , α , C_{fly} and on the voltage swing at the capacitor plates ΔV_{bp} . Thereby the voltage swing scales quadratic and thus the losses increase significantly with increasing voltage. For this reason, the lowest possible value for α is essential, especially for integrated SC converters with high voltages.

Parasitic Well Losses

The well losses P_{well} result from recharging the parasitic junction capacitance of the power transistors (see Fig. 2.8). All n-type MOS transistors, where the back gate may not be directly connected to the substrate potential require isolation by means of an n-well. Figure 2.8 shows a cross-section of an isolated double diffused metal oxide semiconductor (DMOS), which can be used as a switch for higher input voltages. The n-well forms an insulation to the substrate. A pn junction is formed, which is required to stay inverse biased. Depending on the junction voltage, a junction capacitance C_j is formed. Its value depends on the geometry of the well and the semiconductor technology. The capacitance value of C_j depends further on voltage and doping concentration. The parameters can be taken from the technology data.

Due to the operating mode of SC converters, the node voltages at the drain and thus at the n-well change. This causes periodic recharging of the junction capacitance C_j , which leads to charging losses:

$$P_{\text{well}} = \sum_i^{i=n} f_{\text{sw}} \cdot C_{j,i} \cdot \Delta V_i^2 \quad (2.20)$$

In this case n represents the number of isolated switches and ΔV_i the respective voltage swing, which periodically recharges $C_{j,i}$.

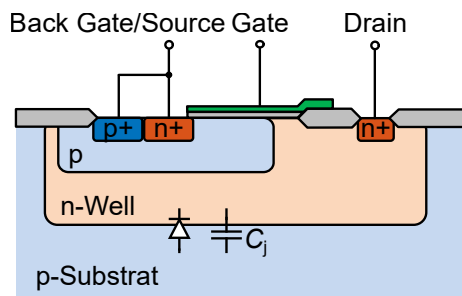


Fig. 2.8: Cross-section of a DMOS.

The extrinsic losses P_{Rp} , which are modeled by the parallel resistance R_p (see Fig. 2.4), can be summarized by:

$$P_{Rp} = P_{sw,ctrl} + P_{Cbp} + P_{well} \quad (2.21)$$

2.4 Capacitor Types for Integrated Switched-Capacitor Converters

The quality as well as the achievable values of the capacitors are decisive for the converter performance. Different capacitor types can be realized on-chip. These differ in the parameters like capacitance density, dielectric strength and parasitic coupling to the substrate. The different types are discussed below.

Metal-Oxide-Semiconductor (MOS) Capacitor

Figure 2.9(a) shows the cross-section of a MOS capacitor. Depending on the design and technology, this can be realized by both a NMOS and a PMOS transistor. The capacitance is formed between the gate and the shorted terminals source, drain and back gate. These MOS capacitors are available in any CMOS baseline technology and typically have a capacitance density of $4 \text{ fF}/\mu\text{m}^2$ and higher [45–47,55]. Due to the design, however, the parasitic substrate capacitance values are high and can be around $\alpha = 5\text{-}10\%$ [55,56]. The dielectric strength is limited to a few volts, identical to the maximum gate oxide voltage rating of the used transistor, and the capacitance value is non-linear. MOS capacitors are not so well suited for flying capacitors due to the large value of α . Due to their high capacitance density, however, they are suitable as buffer and output capacitors.

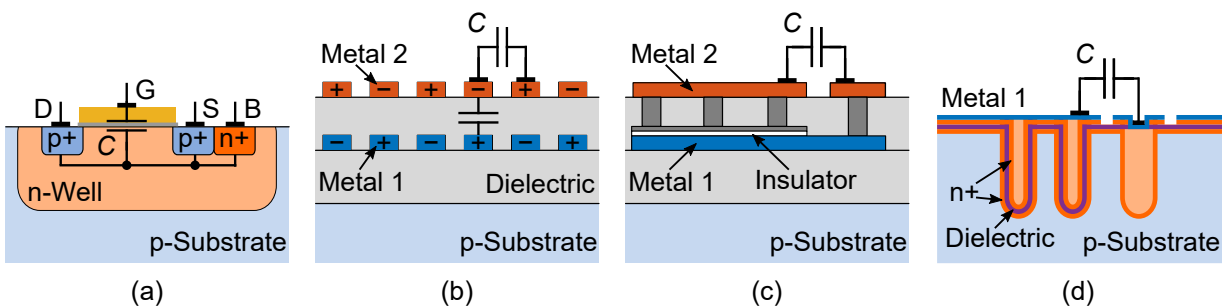


Fig. 2.9: Cross section of different on-chip capacitors, (a) MOS capacitor, (b) MOM capacitor, (c) MIM capacitor and (d) trench capacitor.

Metal-Oxide-Metal (MOM) Capacitor

The cross-section in Fig. 2.9(b) shows the typical structure of a metal-oxide-metal (MOM) capacitor. They are easy to integrate on-chip, all available metal layers of the used technology can be utilized to increase the capacitance density. However, the achievable capacitance densities are usually low $< 0.5 \text{ fF}/\mu\text{m}^2$. Depending on the technology and on the particular construction, they may have a low parasitic capacitance. MOM capacitors are usually only used in high-voltage SC converters or in combination with MOS capacitors in a stack to increase the total capacitance value.

Metal-Insulator-Metal (MIM) Capacitor

Figure 2.9(c) shows the structure of a metal-insulator-metal (MIM) capacitor. MIM capacitors are available in most CMOS technologies. The difference to the MOM capacitor comes from the thin insulation layer instead of the thick oxide layer. Due to the small plate spacing and the insulator used, MIM capacitors achieve a high capacitance density of several $\text{fF}/\mu\text{m}^2$ with a dielectric strength of several tens of volt. The low parasitic capacitance value around $\alpha = 1\%$ and the high capacitance density are the reasons why MIM capacitors are often used for the flying capacitors in SC converters.

Trench Capacitor

Trench capacitors, Fig. 2.9(d), are not available in baseline CMOS technologies and require expensive silicon-on-insulator (SOI) technologies. They achieve extremely high capacitance densities of up to several hundreds of $\text{fF}/\mu\text{m}^2$ along with low parasitic capacitance values. Due to the low dielectric strength of a few volts, these can be used in high-voltage SC converters to a limited extent only. However, they are well suited for use in low-voltage SC converters [5, 51, 57, 58].

Ferroelectric Capacitor

There are also exotic capacitor types like ferroelectric capacitors. These are rarely used in SC converters. This is mainly due to poor availability in common CMOS and SOI technologies and additional costs. [9] demonstrates a high SC converters efficiency with ferroelectric capacitors.

2.5 Standard Switched-Capacitor Topologies

As described in Section 2.1, only a small input-voltage range can be covered efficiently via the output resistance (R_{out}) for a single conversion ratio. Therefore, for small voltage ranges, only a few conversion ratios are often sufficient. However, in order to cover a larger voltage range, several conversion ratios are required. Converters with a regular topology, are especially suitable as they usually enable a large number of conversion ratios. They comprise a regular structure, which can be easily extended and thus covers a larger voltage range. In addition to easier configurability, there are design and layout advantages as well. Figure 2.10 shows three regular SC converter topologies, where (a) depicts the series-parallel SC converter topology. This topology can easily be extended by an additional ratio due to three switches and a flying capacitor. Figure 2.10(b) shows the ladder topology, where the basic cell consists of two switches and two capacitors. The third topology is the Dickson configuration, which is shown in Fig. 2.10(c). This topology can be extended by three switches and one flying capacitor per ratio.

The three presented regular topologies offer good scalability. However, they differ in the voltage requirements for the switches and capacitors. Depending on the application and the used CMOS technology the achievable performance differs. The ladder topology, for example, has the lowest maximum voltage requirements for switches and capacitors. However, this topology requires a larger number of capacitors compared to the others. On the other hand, for the Dickson and the series-parallel topologies, the voltage ratings of the components increase. The used technology can have a significant impact on the performance of the different topologies, which will be further discussed in Section 3.3. More SC converter topologies are presented and discussed in [53, 54, 59, 60].

2.6 Control Concepts for Switched-Capacitor Converters

There are various control options and methods that fit differently well to a particular application. The control adjusts the output voltage to the desired value independent of the input voltage and the load at the output. In the following, the most common concepts are briefly presented and the advantages and disadvantages are described. The various control concepts have already been verified in SC converters and reflect the state of the art. With focus on overall conversion concepts, the development of new control concepts has not been a focus of this work.

In contrast to the inductive converters, a multi-ratio SC converter control consists of two control loops. Within a ratio, the output voltage can be adjusted in a limited range via R_{out} (see Fig. 2.4) depending on the load current and the input voltage. This represents the fine control loop, which adjusts the output voltage V_{out} with precision. However, if, for example, the input voltage changes to such an extent that the fine

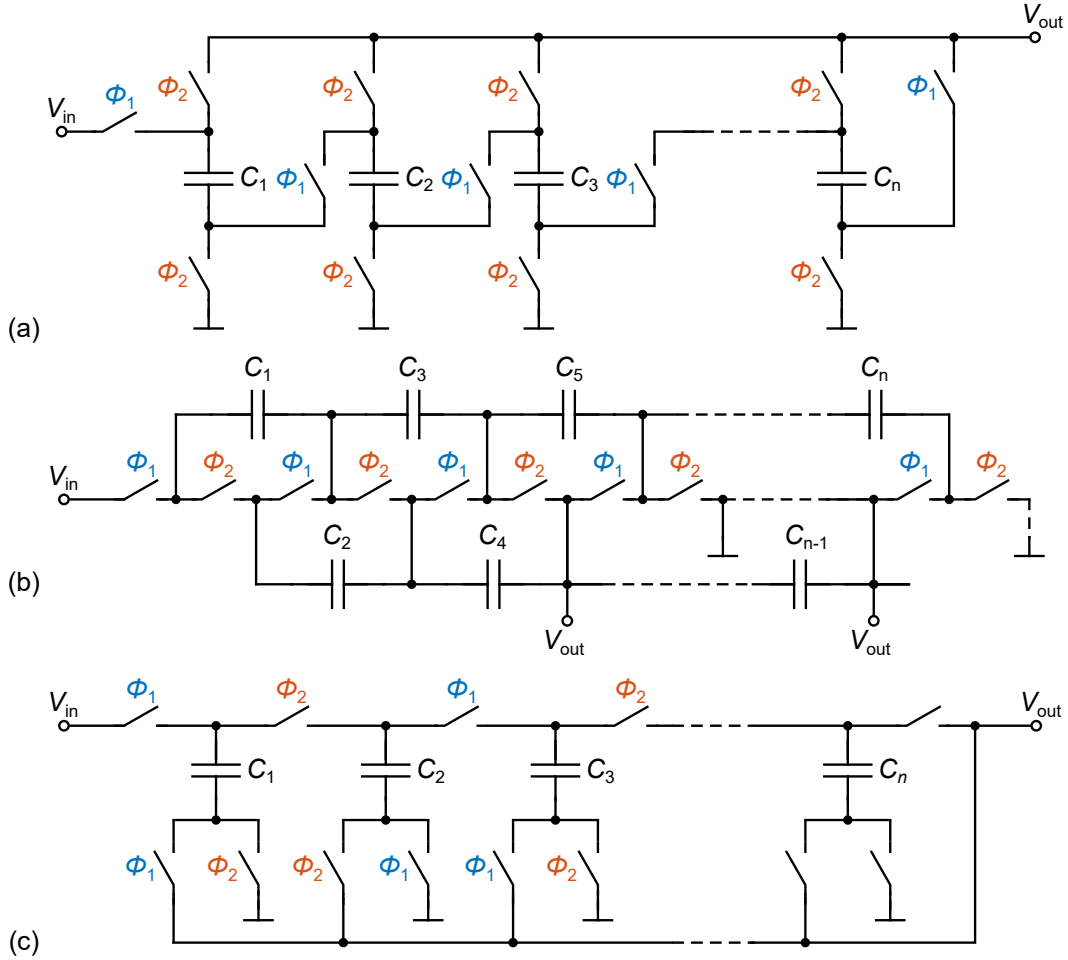


Fig. 2.10: Regular SC converter topologies as (a) series-parallel SC converter topology, (b) ladder topology, and (c) Dickson topology.

control alone can no longer compensate for this change, the outer control loop becomes active and adapts the iVCR (see Fig. 2.4) to the new conditions. For SC converters with a fixed ratio the fine control loop is sufficient.

2.6.1 R_{out} Control Methods

The output voltage of the fine control loop is set by the output resistance R_{out} . Since the output resistance is always positive, this leads for example in a step-down converter to an increased value for the real conversion ratio due to losses and the output resistance compared to the iVCR. The output resistance R_{out} consists of the components R_{SSL} and R_{FSL} according to (2.8). The fine control concepts modulate either R_{SSL} or R_{FSL} to adjust the output resistance.

Frequency Modulation Control

Frequency modulation is a control method that changes the output resistance component R_{SSL} by adjusting the switching frequency f_{sw} . The reciprocal dependence on the switching frequency is shown in (2.6). The frequency variation has the advantage that the switching losses decrease with decreasing switching frequency. This has a particularly positive impact for low load conditions [61]. However, the noise spectrum also varies, which can be undesirable in some applications. Frequency modulation can be implemented either as continuous control by means of an error amplifier and a voltage controlled oscillator (VCO) [39, 54, 62], or with discontinuous hysteretic control [7, 9, 23, 42, 54, 63–65]. Both types are well suited for fully integrated SC converters and are mostly used due to their good adjustability and efficiency.

Capacitance Modulation Control

The capacitance modulation control concept fragments and modulates the flying capacitors used for charge transfer. According to (2.6), the capacitance value affects the output resistance via R_{SSL} . The weighting and fragmentation of the capacitors results in a limited control accuracy. At low output loads the losses decrease, similar to frequency modulation. The fixed switching frequency has a beneficial effect on the interference spectrum, making it constant and predictable. In some application this behavior is required. The fragmentation results in a higher circuit complexity and a higher circuit effort. The overhead and additional power dissipation increase significantly for high-voltage SC converters. Depending on the resolution, a large number of level shifters is required. In addition, capacitors are temporarily not used for charge transport. This has a negative effect on charge transfer and therefore on efficiency. For this reason, this method is not optimally suitable for fully integrated SC converters, since the goal is always to utilize the total available on-chip capacitance value. This control concept was used in [66].

Conductance Modulation Control

By modulating the conductivity of the power switches conductance modulation control affects the R_{FSL} instead of the R_{SSL} , as can be derived from (2.7). Conductance modulation can be achieved by fragmenting the power switches or by changing the gate-source voltage of the power switches. The segmentation of the power switches results in a limited control accuracy [37, 67]. Conductivity modulation by the gate-source voltage, on the other hand, does not result in limitation [68–70]. The segmentation of the switches can only be realized with considerable effort for high-voltage SC converters, as is the case for capacitance modulation. The implementation of the gate-source voltage variation, however, is difficult for floating high-side power switches. The constant switching frequency is an advantage, because the interference spectrum

is predictable. This may be required in some applications. However, the switching frequency has to be set high in order to dominate the output resistance by R_{FSL} (see Fig. 2.5). This has a negative effect on the efficiency in the light-load case.

Voltage Control with Subsequent Linear Regulator

Instead of varying the switch conductance, capacitance conductance or the switching frequency a linear regulator could be connected in series to the SC converter as in [71]. This linear regulator adjusts the output voltage to the desired voltage level. An advantage would be the significantly reduced output voltage ripple. The disadvantage of this approach is that no loss scaling occurs at low load and the total losses are increased by the losses of the linear regulator.

2.6.2 Ratio Control Methods

The ratio control of multi-ratio SC converters takes action as soon as the fine control of the output resistance R_{out} is no longer sufficient. This adapts the conversion ratio to the given conditions. The conversion ratio can be adjusted depending on V_{in} or V_{out} . For a small number of ratios, the V_{in} related control is particularly suitable, since the additional circuit effort is limited [8, 9, 19, 24, 28, 65, 70, 72]. With increasing number of ratios, the number of comparators and hence the power consumption [24] also increases. The control dependent on the output voltage limits the number of comparators and thus the circuit effort for a large number of conversion ratios. Especially for low-power applications the power consumption can be reduced. However, for start-up it must be ensured that the correct ratio is set as quickly as possible [23, 27, 70, 73].

Further details on inner and ratio control concepts and methods can be found in [54, 69, 74].

3 High-Voltage Switched-Capacitor Converter Concepts

As SC converters are well suitable for IC level integration they enable full integration of the power management and new topologies overcome the fixed input/output voltage limitation. In recent years, SC converters have established themselves especially for voltages below 5V. They achieve high efficiency at high-power densities. SC converters are not only attractive for mobile hand-held devices with low input and output voltages, but also for power conversion in IoT, smart home, industrial and automotive applications. The goal of this work is to develop and implement fully integrated SC converters for these high input voltages applications.

In Section 3.1 the differences between low-voltage and high-voltage SC converters are discussed. Further the requirements for high-voltage SC converters are derived. By means of the model introduced in Section 3.2, which is optimized for high-voltage SC converters, different technologies are investigated in Section 3.3. With the help of the model, different SC converter topologies are examined and evaluated for their suitability for high input voltages in Section 3.4. A SC converter topology is selected, which is particularly suitable for high input voltages on the one hand and for a wide input voltage range on the other hand. In addition, a high-voltage three-phase SC converter topology is presented that is particularly well suited for full or partial integration.

3.1 Low-Voltage Versus High-Voltage Switched-Capacitor Converters

This section highlights the main difference between designing a low-voltage or high-voltage SC converter. As defined in Chapter 1 the high-voltage domain begins if the input voltage V_{in} exceeds the transistor oxide breakdown voltage of the digital core domain voltage. As the voltage increases, also the dielectric strength of the devices has to increase. The devices can be classified into low-voltage, medium-voltage and high-voltage devices. Typical transistor voltage classes in various semiconductor technologies are 5 V (low voltage), 10 V to 20 V (medium voltage) and 40 V to 50 V (high voltage) [45–47]. Due to the higher

dielectric strength, the on-state resistance and area consumption for high-voltage transistors increase considerable. By doubling the dielectric strength, the on-state resistance and hence the area rises by a factor of four typically [45–47]. The same applies to capacitors. Most high-voltage CMOS technologies offer MIM capacitors in addition to the MOS and MOM capacitors, as described in Section 2.4. With rising dielectric strength the capacitance density decreases, from typically $4 \text{ fF}/\mu\text{m}^2$ for MOS capacitors with 5 V ratings, to $1 \text{ fF}/\mu\text{m}^2$ for MIM capacitors at a breakdown voltage at 10 V and to less than $0.6 \text{ fF}/\mu\text{m}^2$ for MOM capacitors at 10 V and higher. This lead also to an area increase of approximately four times, when moving from MOS to MIM capacitors and another factor of four from MIM to MOM capacitors, for the same capacitor value [45–47].

With increasing voltage, the transistor and capacitor parameters degrade, such as low turn-on resistance or high capacitance density. This mainly affects the area consumption and the parasitic charging losses of isolation wells and parasitic bottom-plate losses (see Section 2.3). As a result, the power density of the converter decreases. If the area stays constant, lower capacitor values and higher turn-on resistances result for high voltages. These effects can be partially compensated by a higher switching frequency, as shown in Section 2.3, to provide the same output power. By increasing the switching frequency, higher losses such as gate charge losses, switch control losses, bottom-plate losses, etc. result (see Section 2.3). As the voltage increases, the voltage-dependent losses like bottom-plate losses also scale. These losses reduce the efficiency with increasing voltage. To illustrate this influence and to highlight the differences between low-voltage SC converters and high-voltage SC converters, the peak efficiency of a three-phase high-voltage SC converter (which is described in detail in Section 3.4.2) over the input voltage V_{in} is shown in Fig. 3.1. For the simulated SC converter the topology, ratio, chip area and I_{out} are kept constant. The efficiency drops with increasing input voltage significantly, due to the described effects. If V_{in} exceeds the device breakdown voltage, the next higher device voltage class of transistors and capacitors must be used. This leads to a significant drop in efficiency, as can be noticed for the used technologies in this plot, when the input voltage exceeds 10 V and 30 V. At these transitions low-voltage devices change to medium-voltage devices and medium-voltage devices to high-voltage ones, respectively. The peak efficiency curve shown in Fig. 3.1 varies for different topologies and technologies but the qualitative trend generally applies.

As the input voltage increases, also the ratio rises in order to keep the output voltage at the same level. The higher the ratio becomes, the more flying capacitors are needed [75–77]. Since the area is limited, the available area is divided into the higher number of capacitors. By increasing the ratio, the number of switches also increases compared to smaller ratios. In order to transport the same amount of charge to the output and to achieve the same R_{out} (refer to Section 2.3), the switching frequency must be increased. With increasing frequency also the frequency-dependent losses increase, like the gate charge losses. This means that here a trade-off between increasing the switching frequency and increasing the frequency-dependent

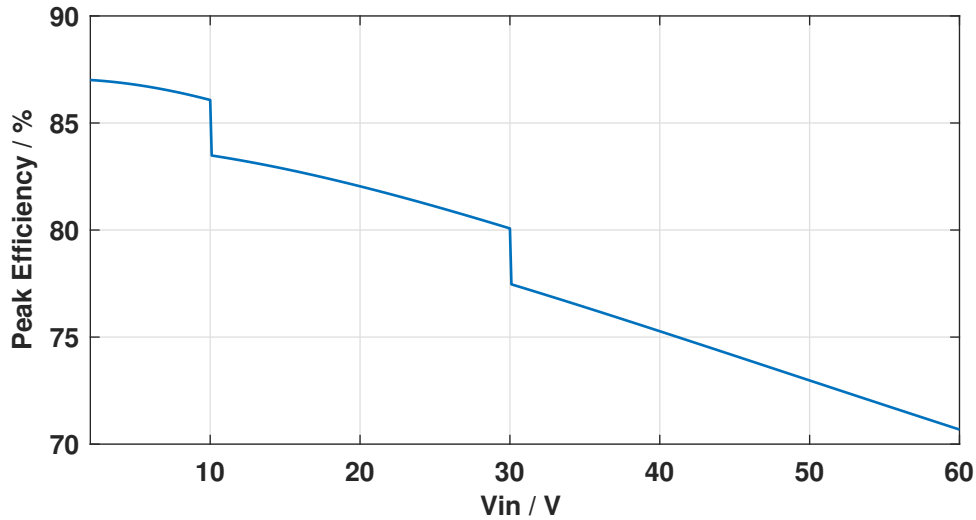


Fig. 3.1: Influence of increasing input voltage (V_{in}) on the peak efficiency of SC converters for fixed VCR.

losses must be made in order to achieve high efficiency. In Fig. 3.2 this behavior is shown representatively for a ladder topology as introduced in Section 2.5, Fig. 2.10(b). The behavior is more or less the same for all SC converter topologies. With rising VCR the efficiency decreases.

Another major influence on power density and efficiency is caused by the high-voltage supporting blocks. These blocks are required with increasing voltage, as the power switches can no longer be controlled directly. A floating high-side supply, which is typically realized by a charge pump and a level shifter are required, which consume some power and degrade efficiency. Figure 3.3 shows the chip photograph of a low-voltage SC converter and a high-voltage SC converter, respectively. Both converters are based on the same 4-bit recursive topology [23]. The area of the power switches and control circuits is marked on the

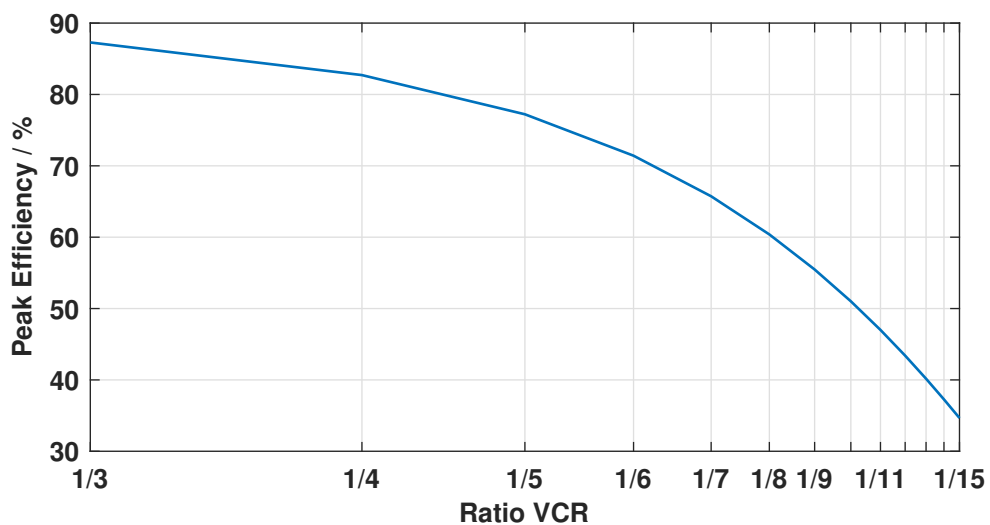


Fig. 3.2: Conversion ratio influence on SC converter efficiency for fixed V_{in} .

chip photograph, which are shown to scale. While only around 5% of the area of the low-voltage converter is occupied by control circuits and power switches, the area requirement increases by a factor greater than seven to around 38% for the high-voltage converter. This significantly reduces the power density and the additional losses caused by charge pump and level shifter further reduce the efficiency. Many methods which are used for low-voltage SC converters to increase performance, such as multiple stages with time interleaving, charge recycling or complex bottom-plate loss reduction are not applicable to high-voltage SC converters [28, 32, 38, 78, 79]. These methods require many additional transistors, which in turn require additional blocks such as a level shifter and a charge pump for driving these transistors. In addition to the extensive required area, the power consumption of these blocks has a major negative impact on the efficiency and overall performance of high-voltage SC converters. Therefore, methods to increase the performance for low-voltage SC converters are often not beneficial for high-voltage SC converters.

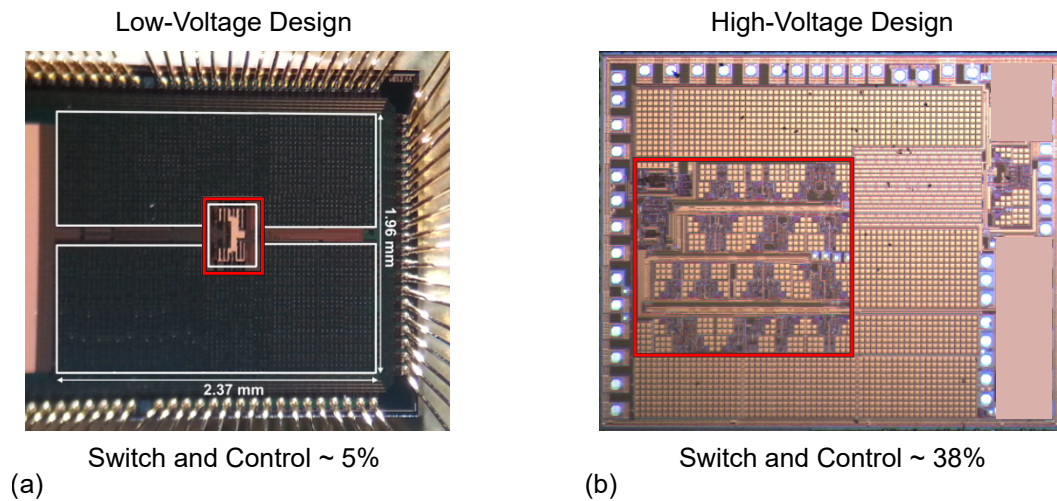


Fig. 3.3: Comparison of low-voltage vs. high-voltage SC converter designs. The chip photograph in (a) shows a design of $V_{in} = 2.5$ V (courtesy of the authors of [23]) and (b) shows a design for V_{in} up to 13 V [41], drawn to scale.

3.2 High-Voltage Switched-Capacitor Converter Model

In order to achieve maximum efficiency even for high-voltage SC converters, this section introduces a SC converter model for sizing high-voltage SC converters. This model allows to optimally dimension and compare different converter topologies. In order to create the same framework conditions, each converter is based on the same chip area and the same technology. High-voltage SC converters make use of components of different voltage classes. This results in different process-specific parameters. In order to be able to compare different topologies fairly, the available chip area must be optimally distributed among the various components of the power stage with the different voltage classes. In the model presented, the area assigned

to a component is weighted depending on topology and process specific parameters. This enables not only the comparison of different topologies, but also the comparison of different semiconductor technologies.

In a first step, the area related to the control loop is subtracted from the total active chip area A_{chip} . The resulting chip area $A_{\text{chip,SC}}$, which is dedicated to the capacitors and switches, is divided into two parts as shown in Fig. 3.4, one part for the power switches A_{sw} and one part for the capacitors A_{cap} . The latter occupy usually the largest part of the chip area. The partial areas are calculated as follows:

$$A_{\text{cap}} = A_{\text{chip,SC}} \cdot xc \quad (3.1)$$

$$A_{\text{sw}} = A_{\text{chip,SC}} \cdot xr \quad (3.2)$$

$$xc = 1 - xr . \quad (3.3)$$

The parameters xr and xc vary between 0 and 1, where xr is used to set the area ratio of the switches to capacitors between 0 and 100%. By sweeping xr , the optimum area ratio of switches to capacitors can be determined, which, for example, achieves the highest efficiency or power density.

If the chip area is divided, the partial areas must again be divided among the individual components. This allocation is made on the basis of an individual weighting for each power switch and each capacitor, based on the following parameters of the technology:

- cx : Capacitance density of the used capacitors in $\frac{\text{fF}}{\mu\text{m}^2}$
- α : Denotes the parasitic capacitance of the used capacitors as described in Section 2.3.2
- rx : Specific on-resistance of the switches in $\Omega\mu\text{m}^2$
- $OL_{\text{cap}}, OL_{\text{sw}}$: Overlay factor expressing the ratio between active and total component area for capacitors and switches, respectively

While the capacitance density cx and α can be taken from the data sheet, the values for the specific on-resistance rx is only provided for some high-voltage devices. Hence, rx as well as the overlay factors OL_{cap}

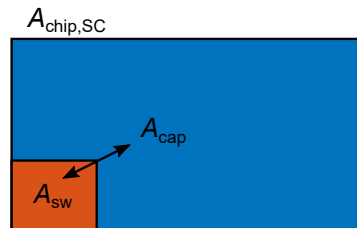


Fig. 3.4: Division of chip area into area for switches and area for capacitors.

for capacitors and OL_{sw} for switches must be determined. For a switch with known resistance R_{on} , its gate area is determined by W and L , resulting in $rx = W \cdot L \cdot R_{on}$.

The overlay factors OL_{cap} and OL_{sw} must be extracted for all components used. Each device consists of an active and a passive area which add up to the total area required by the device. For the MOSFET shown in Fig. 3.5(a), the active area is determined by the above mentioned gate area. The passive area $A_{passive}$ around the active area includes drain and source area, isolation wells, spacing for placement and density rules etc. The overlay factor describes the ratio between active and total required area. This factor should be scalable. For a constant number of transistor fingers and for neglecting the small end areas, the ratio between total area and active area of the switches is approximately constant and scales linearly with the component size. If the number of fingers for a transistor changes, an approximation error occurs. However, since the switches occupy only a small part of the chip area and the worst case is modeled, the deviation is negligible.

The same applies to the capacitance value. Distances and density rules must be observed, which reduces the available active area and thus the capacitance value. In the model, the ratio for both transistors and capacitors is expressed by

$$OL = \frac{A_{active}}{A_{active} + A_{passive}}, \tag{3.4}$$

and must be calculated for each transistor and capacitor type separately.

In addition to the technology parameters, topology parameters must also be specified for the weighting of the partial area distribution:

- voltage class of the individual components to assign the corresponding technology parameters
- charge flow vectors of the topology (see Section 2.3.1)

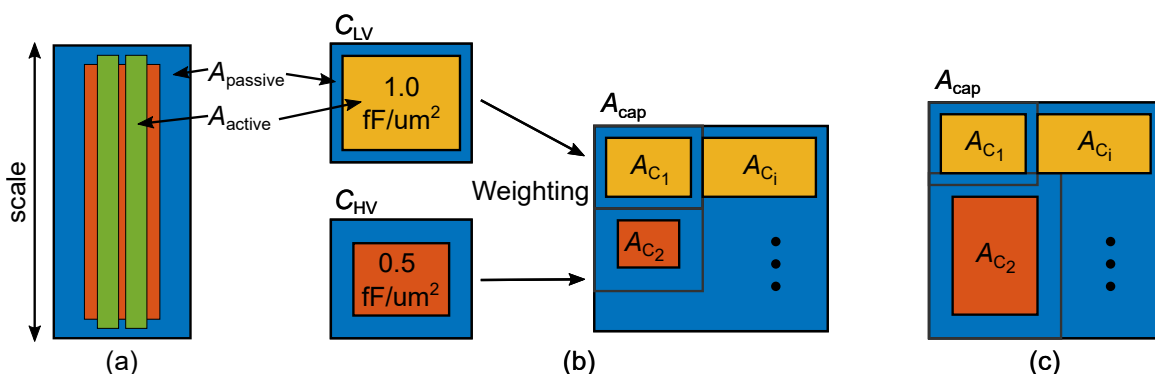


Fig. 3.5: (a) shows the passive and active area of a MOSFET, which add up to the total device area, (b) shows the charge flow based common weighting approach for different capacitor types and (c) shows the proposed loss optimized sizing approach for high-voltage SC converter.

- voltage swing at the relevant nodes (to be determined by topology analyses)

With the technology and topology parameters, a vector is introduced for the switches and the capacitors, which contains the weighting for each element and forms the basis for the area distribution.

In the charge flow analysis introduced in [59] the sizing only depends on the charge flow through the devices, expressed by the charge flow vector according (2.3) and (2.4). From this, the area distribution for the capacitors is calculated according to

$$A_{C,i} = \frac{a_{C,i}}{\sum_i^n a_{C,i}} \cdot A_{\text{cap}} , \quad (3.5)$$

where $A_{C,i}$ is the single device area and $a_{C,i}$ the charge flow vector from (2.3). Same applies for the transistors:

$$A_{R,i} = \frac{a_{R,i}}{\sum_i^n a_{R,i}} \cdot A_{\text{sw}} . \quad (3.6)$$

Especially for converters with high input voltages and components in different voltage classes, not only the output resistance R_{out} (intrinsic losses) shown in Fig. 2.4 should be optimized, but also the sum of both loss sources R_{out} and R_{p} . Parts of the modeled R_{p} depend on the same quantities and parameters as R_{out} . The component size for instance has an influence on both modeled loss sources R_{p} and R_{out} via the bottom-plate losses, the recharging losses of the isolation wells and the control losses. By enhancing the charge flow based sizing with an optimized sizing proposal which additionally takes extrinsic losses such as gate charge, bottom plate or well charge losses into account, efficiency can be further increased. If, for example, large bottom-plate losses occur at a capacitor due to a large voltage swing, these must be taken into account during sizing. By reducing the component size compared to the sizing with the charge flow analysis, the intrinsic charge flow losses (represented through R_{out}) increase, but the bottom-plate losses (represented by R_{p}) are reduced and the total losses are minimized. A more detailed analysis of the parasitic losses reveals that they scale with the voltage. The voltage swing V_{swing} which the corresponding components experience is decisive. Investigation of this work have shown that scaling with the reciprocal of the voltage swing V_{swing} results in a close approximation to the optimum.

In order to ideally size the capacitors, the proposed sizing approach enhances the common charge flow sizing approach by the parameter capacitance density cx , the overlay factor OL_{cap} and the voltage swing V_{swing} . This additional parameters are important for SC converter which utilizes different capacitor types. This is

the main difference and challenge compared to sizing a low-voltage SC converter. Since low-voltage SC converters usually use only one capacitor and one transistor type. Figure 3.5(b) shows the sizing challenge using the common charge flow based sizing approach for a high-voltage SC converter. Two capacitors, a low-voltage capacitor C_1 and a high-voltage capacitor C_2 have to be sized. Both have the same charge flow vector $a_{C,1} = a_{C,2}$, however, both capacitors should have the same capacitance value with respect to R_{out} . If the area is distributed like in (3.5) the actual value of C_1 would be less than half of the value of C_2 due to low capacitance density and spacing requirements, as shown in Fig. 3.5(b). Therefore the vector G_{cap} is introduced, which takes the high-voltage related parameters cx , OL_{cap} and V_{swing} into account:

$$G_{cap,i} = \frac{a_{C,i}}{cx_i \cdot OL_{cap,i} \cdot V_{swing,i}} \cdot \quad (3.7)$$

As a result, different capacitors have the same weighting in relation to their capacitance value. To allocate the area weighted by G_{cap} , each element is normalized to the sum of the vector and multiplied by the total area that is assigned for the capacitors. By normalizing to $\sum G_{cap}$ the area A_{cap} is completely divided into the subareas $A_{C,i}$:

$$A_{C,i} = \frac{G_{cap,i}}{\sum G_{cap}} \cdot A_{cap} \quad (3.8)$$

This results in a value for each capacitor:

$$C_i = A_{C,i} \cdot OL_{cap,i} \cdot cx_i \cdot \quad (3.9)$$

The proposed sizing approach, shown in Fig. 3.5(c) divides the provided area between the low-voltage capacitor C_1 and high-voltage capacitor C_2 such that the two capacitors have the same capacitance value assuming both capacitors have the same voltage swing. The voltage swing parameter V_{swing} weights the corresponding capacitors in order to realize the described loss optimization between bottom-plate losses and losses due to charge flow.

The same sizing approach is applied to the power switches:

$$G_{sw,i} = \frac{a_{R,i} \cdot rx_i}{OL_{sw,i} \cdot V_{swing,i}} \cdot \quad (3.10)$$

Similar to the different capacitor types, the parameters rx and OL_{sw} also differ significantly between the different transistor types. The difference between low-voltage MOS transistors and high-voltage DMOS transistors is particularly large and must be considered. With high-voltage DMOS transistors, the area

required and the associated losses are significantly greater. By the factor V_{swing} a loss optimum between R_p and R_{out} is also achieved. The area allocated to each switch is calculated:

$$A_{\text{sw},i} = \frac{G_{\text{sw},i}}{\sum G_{\text{sw}}} \cdot A_{\text{sw}} \quad (3.11)$$

This results in the switch-on resistance

$$R_i = \frac{rx_i}{A_{\text{sw},i} \cdot OL_{\text{sw},i}} \quad (3.12)$$

With the calculated values for the switches and the capacitor values the resulting losses can be determined according to Section 2.3.

Figure 3.6(a) shows the influence of different optimization approaches on the efficiency of a SC converter with high input voltages. If no optimization is considered and all switches and capacitors are executed with uniform values, 50% efficiency is achieved. If an optimization is implemented based on the charge flow vectors, almost 70% efficiency is possible under the same conditions. As shown in Fig. 3.6(a), a significant additional efficiency gain of up to 10% over a wide range and 3% peak efficiency improvement can be achieved at high input voltages with components of different voltage classes through the proposed sizing approach. However, if a topology only uses components of the same voltage class, as is often the case for low-voltage SC converters, the proposed optimization does not lead to an advantage, nor to a disadvantage.

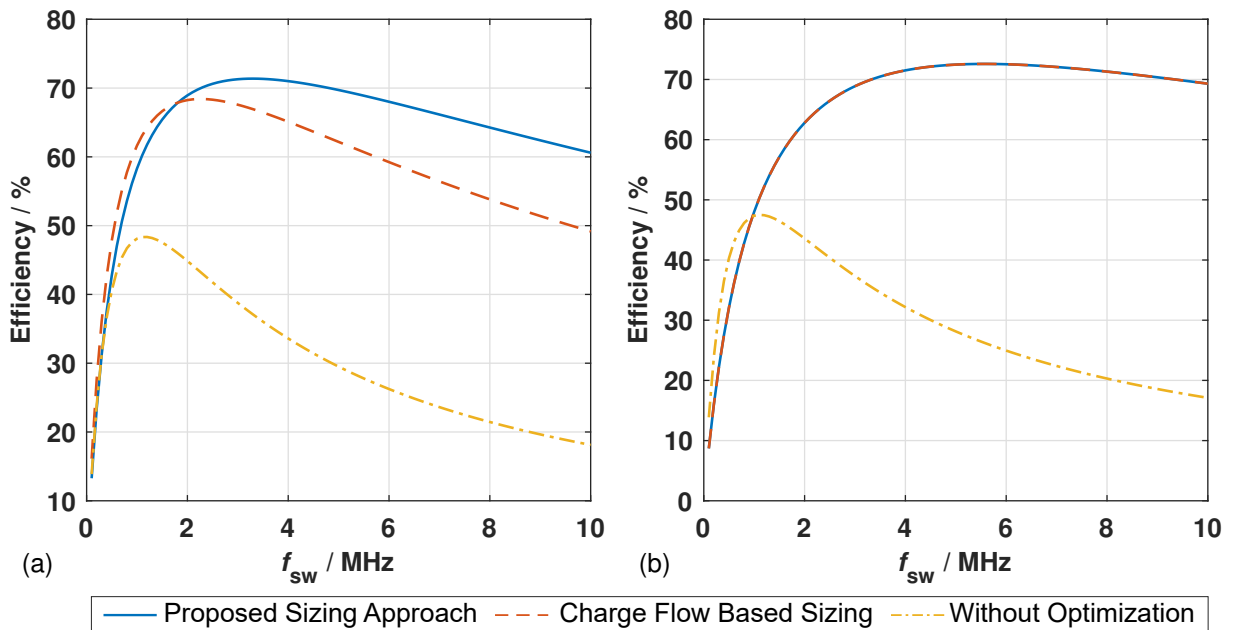


Fig. 3.6: Comparison of the different sizing approaches on: (a) high-voltage SC converter $V_{\text{in}} = 60\text{ V}$, $V_{\text{out}} = 3.3\text{ V}$, $I_{\text{out}} = 12\text{ mA}$ and (b) SC converter with only one low-voltage transistor and capacitor type.

This case is simulated and illustrated in Fig. 3.6(b). The curves of the proposed and the charge flow based approach lie on top of each other.

Figure 3.7 shows the flow diagram of the proposed model for optimized sizing of power switches and capacitors depending on the available chip area, topology and technology used. This allows a comparison of different topologies and technologies for the same framework conditions. In addition to common two-phase converters, it is also possible to compare multi-phase topologies, which will be introduced in Section 3.4.2.

The model presented in this work to determine the optimal sizing for high-voltage SC converters operates as follows. First, all process related data and parameters are recorded in the process parameter file. In addition, the topology dependent data are defined in the topology parameter file, like voltage ratings and voltage classes of the components and a starting value for the capacitor-switch ratio (rx) and the chip area are defined. These data are required in the following step to perform the sizing of the capacitors and power switches. Once the individual devices are sized, the output resistance R_{out} can be calculated then the losses can be determined. In the next step, the target parameters of the analysis such as efficiency, power density etc. can be calculated. If the model is now run through cyclically and rx is increased step by step from the start value to 1, the optimum sizing for the desired target parameters can be determined. After the routine, the results can be evaluated.

3.3 Technology Investigation

The choice of technology plays a key role for integrated high-voltage SC converters, as it has a strong influence on the efficiency, etc. The technologies differ significantly in the following aspects:

- Capacitance density values of the available capacitors
- Parasitic capacitance values of the capacitors (see Section 2.3.2)
- Specific turn-on resistance of transistors
- Availability and voltage steps of the dielectric strength of the high-voltage components

By means of the model presented in Section 3.2, different technologies can be compared fairly. To show the influence of the technology on the achievable efficiency, two topologies for four different $0.18\ \mu\text{m}$ high-voltage technologies were investigated. The Dickson converter topology and the three-phase SC converter topology introduced in Section 3.4.2 are exemplarily chosen.

The influence of the technology on the peak efficiency can be clearly seen in Fig. 3.8. The peak efficiency

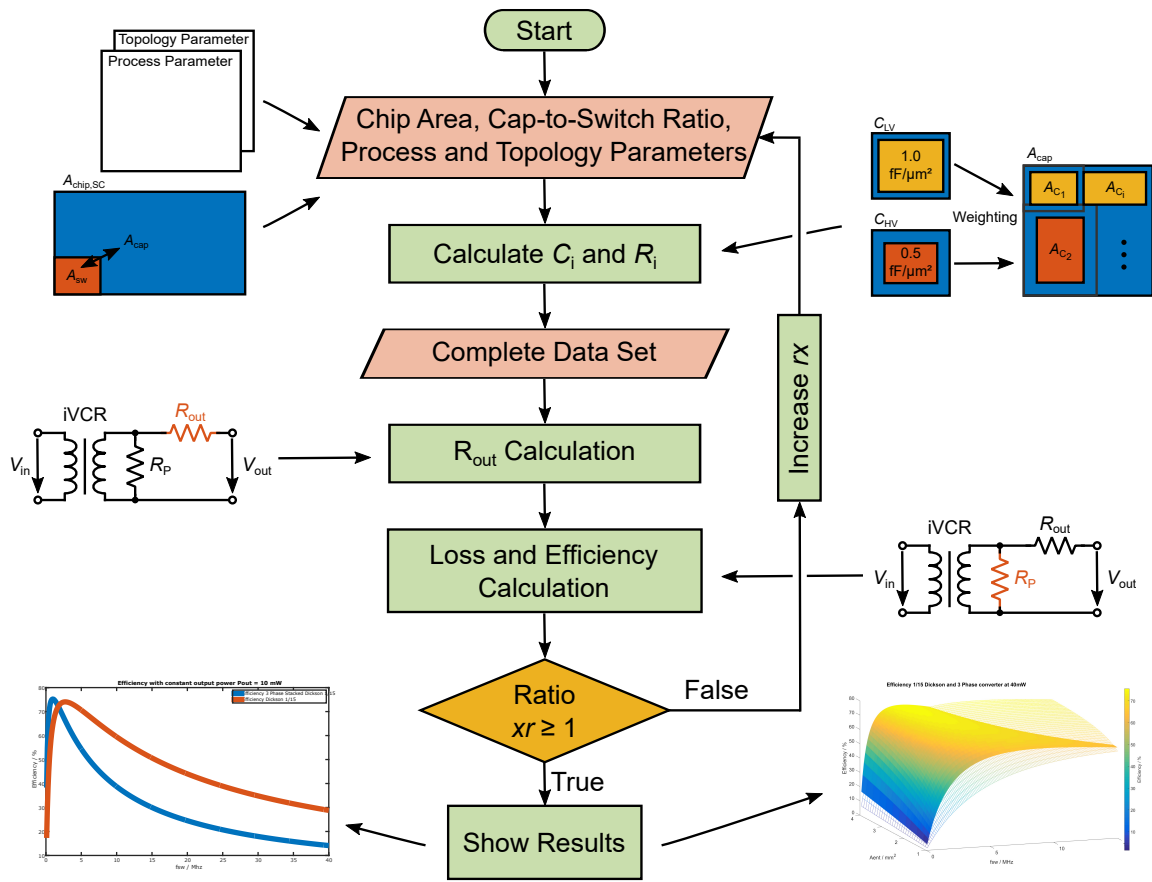


Fig. 3.7: Flow diagram of the proposed model.

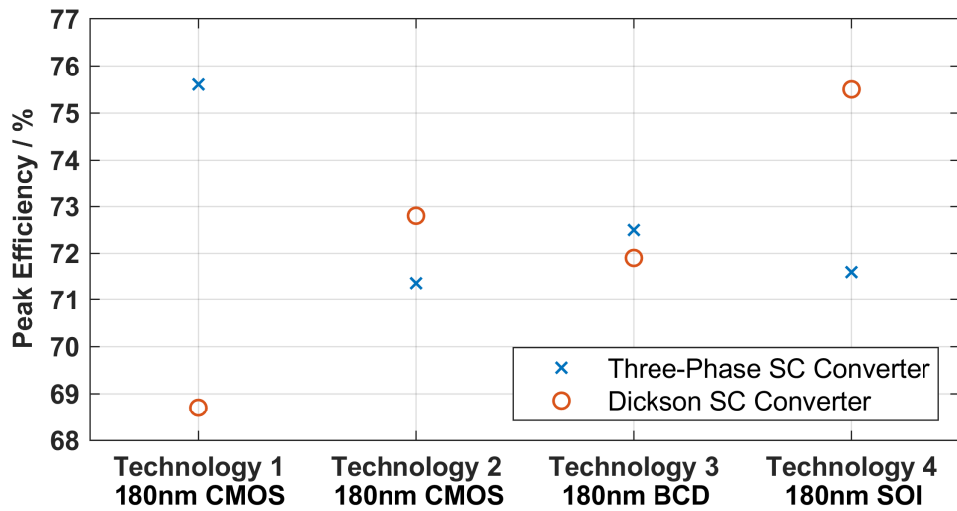


Fig. 3.8: Technology influence on high-voltage SC converter topologies.

varies by up to 7%, depending on the technology. On the other hand, the technology parameters have different impact depending on the converter topology. While the three-phase SC converter for Technology 1 achieves the highest peak efficiency, the Dickson converter achieves the highest peak efficiency for Technology 4. This can be explained by the fact that Technology 4 has good high-voltage capacitors, from which the Dickson converter particularly benefits. In contrast, the three-phase SC converter does not use these high-voltage capacitors and therefore has no advantage. Technology 1 has good low-voltage capacitors and good high-voltage switches, which obviously benefits the three-phase SC converter. This confirms that the technology should be matched to the topology and vice versa. The presented model enables an efficient way to compare different topologies or different approaches of a topology under the same conditions, e.g. chip area or technology. For example, different types of transistors or transistor stacks can be compared appropriately. This facilitates a model-based decision for the selected topology choice.

When choosing a technology, it is also important to ensure that devices such as Zener diodes or Schottky diodes are available if required. In addition, some parasitic effects, such as parasitic bipolar transistor structures (see Section 5.6), are not modeled in all technologies. However, these effects can have a significant impact and influence the choice of technology. Besides technical aspects, factors such as costs and availability influence the choice of technology as well. This comparison of the technologies offers the designer the possibility to make the best choice depending on the boundary conditions. For the realization of a Dickson converter Technology 4 is clearly to be favored and for the three-phase SC converter Technology 1. Instead of comparing the peak efficiency as in Fig. 3.8, other parameters such as average efficiency, power density or area can be used for the technology decision.

3.4 Switched-Capacitor Converter Topologies

By choosing the right topology and technology, as shown in Fig. 3.8, parameters like efficiency, power density etc. can be significantly improved. In this section, the choice of topology will be discussed. The technology used defines, for example, the voltage swing at the individual circuit nodes and devices and determines the voltage-dependent losses, such as the parasitic bottom-plate losses, etc. The number of high-voltage devices required is also decisive. Regular structures as the Dickson or Ladder topology (Section 2.5) benefit mostly from the fact that only few high-voltage devices are used. Most devices can be realized as low-voltage devices, but with the drawback that the total number of devices increases.

As discussed in the fundamentals (Section 2.1), a SC converter works efficiently only in the ideal ratio. Several ratios are required to cover a wide voltage range. In many applications, high and varying input voltages are present, which must be converted to an output voltage of 5 V or lower. Possible applications are battery powered high-voltage applications such as robotic vacuum, e-bike and robotic lawnmowers.

Energy harvesters also have high varying source voltages, which must be converted [80–82]. Another possible application is in micro power supplies [44,75], as presented in Chapter 6.

Multi-Ratio Switched-Capacitor Converters

In recent years there has been a strong trend towards multi-ratio SC converters. Especially in the low-voltage field there are many concepts and topologies. In principle, multi-ratio SC converters can be divided into two groups, regarding to the number of ratios. On the one hand the converters with regular structure, which are characterized by numerous ratios [4, 20, 23, 29, 42, 64, 69, 70, 83–85] and, on the other hand, topologies, which have two to four ratios and use specific optimized ratios [5, 21, 30, 35, 75, 86–88]. This is also reflected in the state of the art of multi-ratio SC converters shown in Fig. 3.9. For most of these SC converters, the input voltage varies, but there are also converters where the output voltage or both the input and output voltages change. Therefore, for comparison, the number of ratios over the input or output voltage range is plotted for the references [4, 7, 9, 19–29, 38, 39, 41, 42, 64]. There are a lot of converters in the range of less than 10 ratios and less than 5 V. For a higher number of ratios there are significantly fewer concepts and there are only a few converters for input voltages higher than 5 V. The goal of this work is to increase both the voltage range and consequently the number of ratios, highlighted in Fig. 3.9. To cover a wide voltage range with high efficiency, a high number of ratios is required (refer to Section 2.1). However, this lead to significantly lower power density as shown in [89] and other publications. Depending on the input range, more than 20-30 ratios make little sense, since both the control and the device effort increase too much. This is the reason, why [4] uses only 15 of 45 and [25] uses 24 out of 79 possible ratios.

Due to the large number of ratios and the relatively manageable control effort, the recursive binary weighted approach as demonstrated in [23] offers a good basis for covering a wide voltage range. This is discussed further in Section 3.4.1.

Resonant Switched-Capacitor Converters

Recently, a remarkable research effort can be noticed in the field of integrated resonant and soft-charging SC converters. These SC converters can achieve high efficiency and high-power density [67, 90–93]. However, resonant switching requires relatively large values for the inductive and capacitive components. For this purpose [91] considers the current ripple ΔI_L and voltage ripple ΔV_C in state-of-the-art buck converters:

$$\Delta I_L \propto \frac{V_{in}}{f_{sw} \cdot L} \quad (3.13)$$

$$\Delta V_C \propto \frac{\Delta I_L}{f_{sw} \cdot C} \quad (3.14)$$

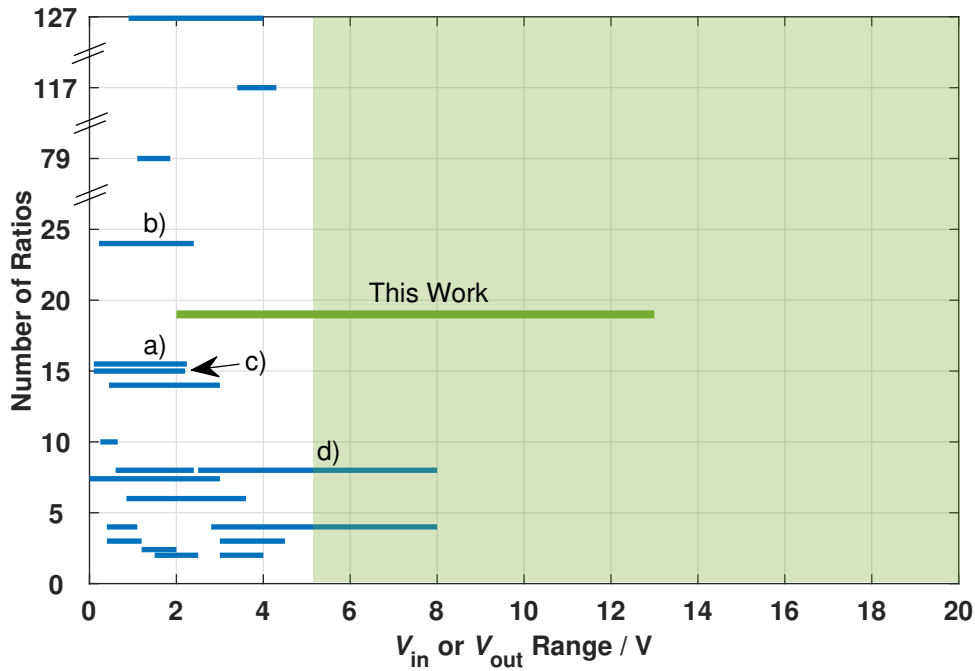


Fig. 3.9: State-of-the-art comparison of SC converters with a wide input or output voltage range. The SC converters indicated are the following: a) [4], b) [25], c) [23] and d) [42].

For a constant ripple, the values L , C of the passive components can be reduced by increasing the switching frequency f_{sw} . Due to proper resonant operation usually external inductors are used, which makes a full integration approach unsuitable [90–94]. Some concepts stack the external components directly on top of the chip in order to save space and enable a compact design [67, 93–95]. There is a trend towards full integration of all components [67]. However, to increase the input voltage, (3.13) and (3.14) show that either the switching frequency or L and C must be increased to compensate for the higher input voltage. As the passive components are already at the integration limit, this leads to a further increase in the switching frequency, which is already high at around ≥ 50 MHz [67, 96–98]. Such high switching frequencies lead to high gate charge losses and excessive losses in the supporting circuits, as outlined in Section 2.3. This is further aggravated by high-voltage transistors, as discussed in Section 3.1. In order to achieve a proper resonant operation, low turn-on resistance values must be achieved, which make the high-voltage transistors large and, hence, gate charge losses rise further. Additionally, most of the concepts are only suitable for a limited input voltage range or limited to less than three ratios [67, 90, 95, 96]. This makes it hard to realize a fully integrated high-voltage SC converter with a wide input voltage range, therefore this work will focus on conventional non-resonant SC converter topologies.

3.4.1 Recursive Buck-Boost Switched-Capacitor Converter

Regular topologies such as the recursive binary weighted SC converter in [23] and the Dickson SC converter in [42,43] are well suited for high input voltages. A closer comparison of the two topologies shows that [23] can better handle a wide input voltage range from 2 V to 20 V, which is a design goal of this work. Building small ratios up to 15/16 is a further advantage of the recursive binary weighted SC converter [23], whereby the Dickson converter [43] can only achieve a minimum ratio of 1/2 and by using a subconverter [42] a minimum ratio of 2/3 due to the topology structure.

The recursive SC converter (RSC converter) is composed of uniform 2:1 cells (Fig.2.3), identical to the series-parallel converter stage discussed in Section 2.2. These regular structures offer advantages in design and layout.

Recursive Switched-Capacitor Converter Topology

The 2:1 cells can be connected in different ways to achieve a high number of conversion ratios. Only n 2:1 cells (n flying capacitors) lead to $2^n - 1$ conversion ratios. Four such 2:1 cells are required for a gap-less coverage of the desired voltage range of 2 V - 20 V. These four cells can be connected in many ways to create 15 different configurations. This work proposes to utilize the 15 different configuration to either convert the input voltage up or down, resulting in 30 possible ratios ranging from $V_{out} = 1/16 V_{in}$ to $V_{out} = 16 V_{in}$. Figure 3.10 shows one of the 2:1 cells along with three possible configurations of the power stage.

In Fig. 3.10(b) the cells are cascaded and stacked to build up the step-down ratio 9/16, by changing the input and output connection of the cell, the ratio 16/9 can be realized. To increase the efficiency of the power stage, the goal is to maximize the number of V_{in} and ground connections. This reduces the charge

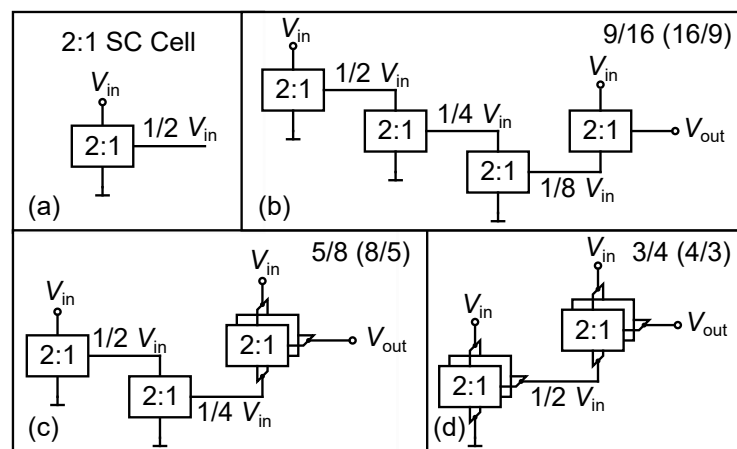


Fig. 3.10: System-architecture block diagram of the recursive buck-boost SC converter.

transmission of the flying capacitors and the cascading losses. Therefore, each cell is connected either to V_{in} or to ground or both. This optimizes the charge flow and reduces charging losses. In Fig. 3.10(c) the ratio 5/8 (boost mode: 8/5) is shown, this ratio can be built up with only three of the four cells. As an advantage of the recursive SC converter proposed in [23], the 2:1 cells, which are not required to build up the ratio, can be utilized to optimize the output resistance and thus the efficiency. In this case, the fourth cell is connected in parallel to the third cell, which supplies the output voltage V_{out} . The same applies to the 3/4 ratio shown in Fig. 3.10(d). For the ratio 1/2 (boost mode: 2/1) all four cells are connected in parallel. In Section 5.5 the optimal sizing and allocation of the capacitance values with respect to the efficiency is discussed.

Figure 3.11 shows the schematic structure of the recursively binary weighted SC converter topology with four 2:1 cells. Each cell has at least one and up to three inputs and one output depending on the cell's position. The topology switches (T) outside the 2:1 cells are required to configure the different conversion ratios. Only one of the two switches marked with "or" is active in Fig. 3.11, depending on the selected conversion ratio. Due to the topology of the converter, the voltages at the lower switch connections (the source contacts if realized by an NMOS transistor) are referred to different voltage levels and not to ground. Supporting circuits are necessary for the most of the switches. A level shifter is required to ensure that the switches are turned on correctly. In addition, a charge pump must be used to generate the required voltage overdrive. The overdrive cannot be generated for most switches simply from the intermediate node voltages nor via a bootstrap circuit. Low-power design of the additional circuits is crucial to keep the efficiency reduction as small as possible. Chapter 4 presents the required supporting circuits and offers more circuit concepts for high-voltage SC converters.

The presented recursive SC converter obtains the excellent conditions for a fully integrated SC converter with a wide and high input voltage range. Therefore, this topology is favored and kept as the focus of this work. Chapter 5 describes the design of this fully integrated recursive SC converter topology and presents measurement results.

3.4.2 High-Vin Switched-Capacitor Converter Concepts for 60V and above

In this section concepts for SC converters with a high conversion ratio for input voltages up to 60 V will be investigated. The goal is to convert a high input voltage down to an output voltage of ≤ 5 V. The recursive SC converter presented in Section 3.4.1 is not optimally suited for this application, as only one single high conversion ratio is required. Therefore, the recursive SC converter cannot benefit from its multiple ratios. Possible approaches are topologies with regular structure like the Dickson, Ladder or series-parallel converter topology [53], as well as optimized topologies [77] with two or more phases. Investigations using the proposed model (Section 3.2) confirm that, among the regular structured two-phase converters,

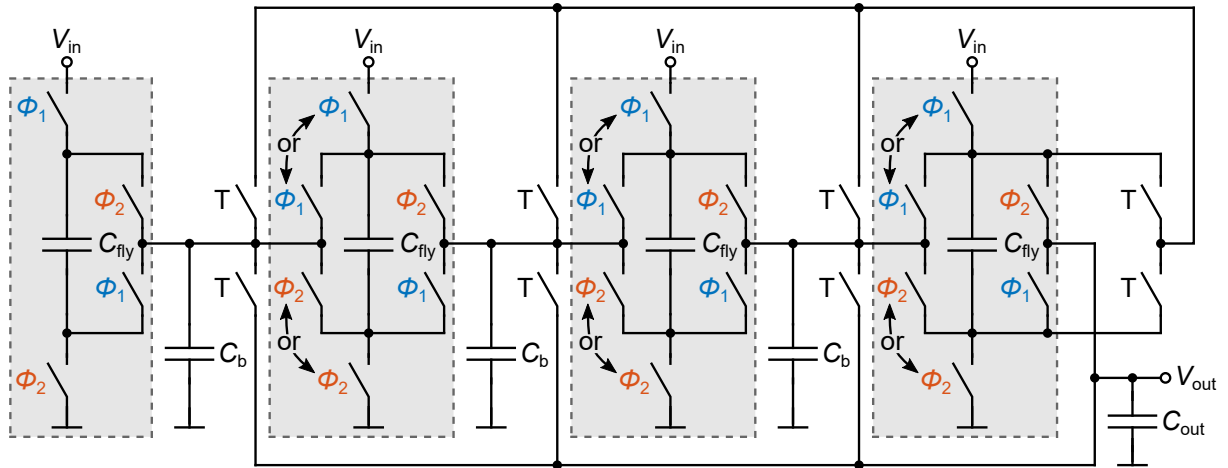


Fig. 3.11: Power stage of the four stage recursive buck-boost SC converter.

the Dickson topology is well suited for high input voltages as explored in [77, 99]. Most SC converters operate in two phases, but dividing the switching period into three or more phases enables new possibilities. This means that, within one switching period, there are three or more capacitor configurations. In contrast to two-phases SC converters, this technique provides additional ratios or, important for the goal of this work, higher conversion ratios, without the need for additional capacitors [21, 36, 100]. This reduces the area needed for SC converters with high conversion ratios. Table 3.1 confirms that, the maximum possible conversion ratio begins to increase significantly compared to the two phase approach for four and more flying capacitors [100]. This make a multi-phase approach attractive for the goals of this work. However, so far this technique is applied in low-voltage SC converters, for example in [21, 36]. More than three phases could also be beneficial and useful for high-voltage SC converters. This is not further investigated in this work.

Tab. 3.1: Maximum achievable conversion ratio based on [100].

| Number of Flying Capacitors | 1 | 2 | 3 | 4 | 5 | 6 |
|--|-----|-----|-----|------|------|------|
| $iVCR_{\max}$ - Two-Phase Conversion | 1/2 | 1/3 | 1/5 | 1/8 | 1/13 | 1/21 |
| $iVCR_{\max}$ - Three-Phase Conversion | 1/2 | 1/4 | 1/7 | 1/13 | 1/24 | 1/44 |

Three-Phase Switched-Capacitor Converter Topology

In order to reduce the number of capacitors and power switches and to improve the maximum converter efficiency, a three-phase topology is introduced in this section, which utilizes five flying capacitors. To convert an input voltage of 50 V - 60 V to ≤ 3.3 V output voltage, a ratio of 1/15 is required. Due to the additional phase, more charge is exchanged between the capacitors and transferred to the output, from which the required high conversion ratio is achieved. The proposed 1/15 topology in Fig. 3.12 is optimized with regard to the voltage swing at the capacitor bottom-plate switching nodes and the number of high-voltage components. Further detailed information about the 1/15 SC converter topology can be found in Appendix B. In Appendix C a further optimized high-voltage three-phase 1/16 SC converter topology is described in detail, which is as well a promising approach for future work.

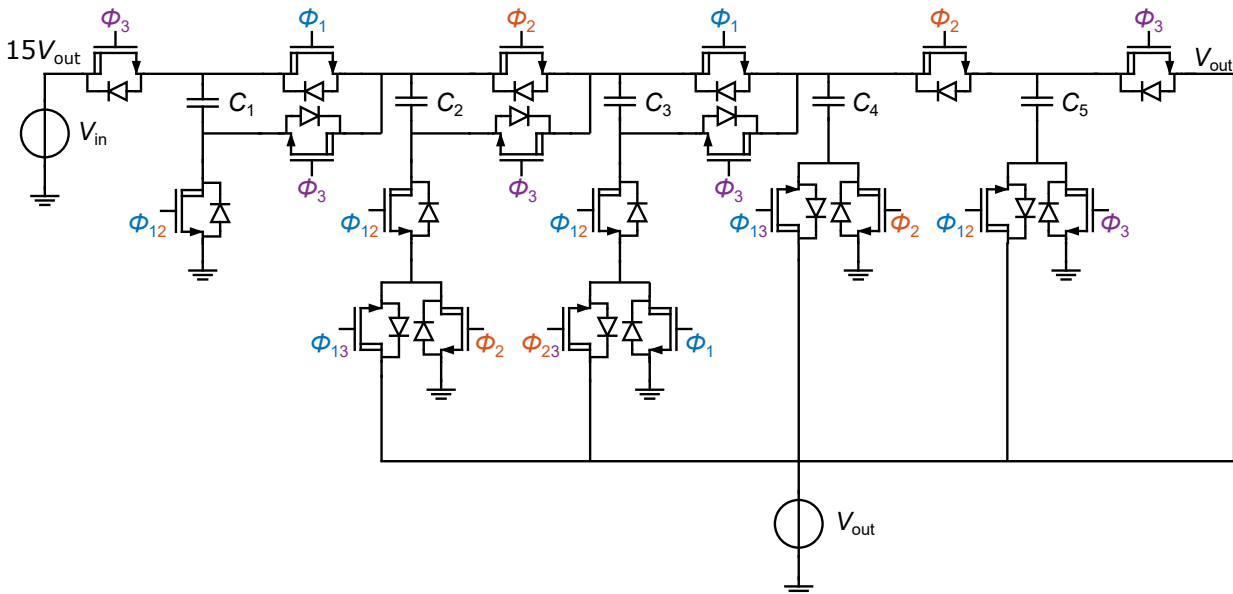


Fig. 3.12: Three-phase SC converter topology.

If the Dickson converter (introduced in Section 2.5) and the proposed three-phase SC converter are compared with respect to the required components in Table 3.2, the three-phase topology offers a more promising approach for high input voltages due to a significantly lower number of capacitors. In addition, some capacitors can be implemented with lower dielectric voltage strength and consequently higher capacitance density. The number of switches required is 18 instead of 44. However, due to the asymmetry of the third phase, some of these switches have to be designed with higher voltage ratings. For all switches that cannot be switched to ground, a level shifter and a charge pump are additionally required. With three-phase converters, significantly fewer of these components are needed, but the requirements for level shifter and floating high-side supply increase due to larger voltage swings and charge amounts. This is an advantage for the Dickson topology, since the voltage swings are low (only $V_{\text{swing}} = V_{\text{out}}$), therefore, switch control

and supply are easier to realize. However, the level shifter presented in Section 4.1.2 was developed and optimized especially for the three-phase converter requirements.

Tab. 3.2: Comparison of Dickson and three-phase SC converter topology for VCR=1/15.

| Dickson Converter | Three-Phase SC Converter |
|--|--|
| 14 Capacitors ($1 - 14 \cdot V_{out}$) | 5 Capacitors ($1 - 5 \cdot V_{out}$) |
| 43 Switches ($1 - 2 \cdot V_{out}$) | 20 Switches ($1 - 10 \cdot V_{out}$) |
| 29 Level Shifter + 29 Charge Pump | 15 Level Shifter + 15 Charge Pump |

Fully Integrated Approach

In this section the full integration of the Dickson topology and the three-phase SC converter topology is investigated. The input voltage should be converted from maximum $V_{in} = 60\text{ V}$ to an output voltage of $V_{out} = 3.3\text{ V}$ with an output power of 40 mW . Initially, the loss mechanisms and differences of the two topologies are investigated with the presented model (see Section 3.2). Figure 3.13 shows the relative loss distribution for the above parameters. The intrinsic losses in the output resistance represent the dominant part in both topologies. There are conceptual differences regarding the extrinsic losses. While within the Dickson converter the control losses P_{ctrl} make up the largest part with 34%, for the three-phase SC converter it is the bottom-plate losses P_{Cbp} and the losses of the isolation wells P_{well} , which together reach 26%.

This behavior can be explained by looking at the phase configurations of the converters. The nodes of the Dickson converter experience maximum voltage swings of V_{out} . Due to this structure, the isolation

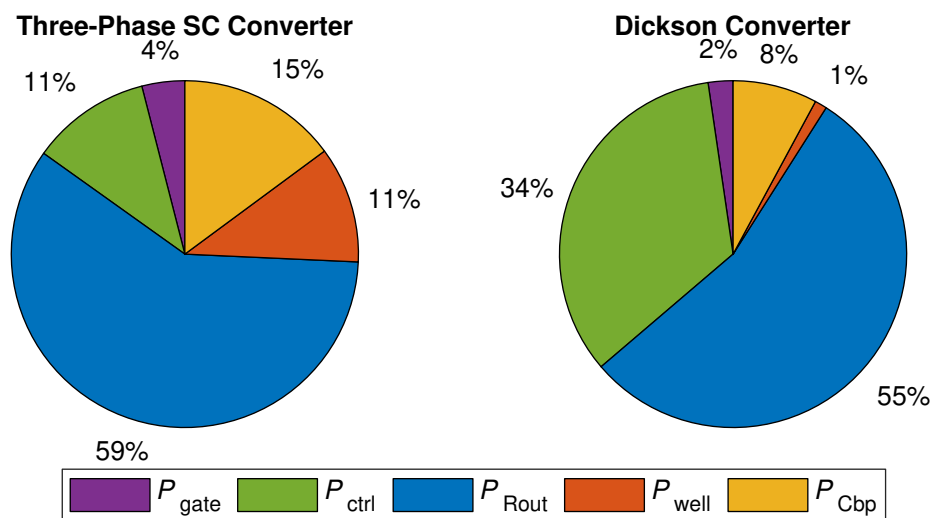


Fig. 3.13: Loss breakdown of the three-phase SC converter and the Dickson Converter.

wells and bottom-plate losses are small. The large driving losses result from the large number of switches and supporting circuits. In addition, the driving losses are increased by the significantly higher switching frequency compared to the three-phase SC converter. This can be seen in Fig. 3.14, where the efficiency curves for the two SC converter are shown for the switching frequency. While the peak efficiency for the tree-phase SC converter is achieved at around $f_{sw} = 3$ MHz, the Dickson converter has an approximate three times larger switching frequency with $f_{sw} = 10$ MHz. However, the three-phase SC converter has significantly larger voltage swings and thus significantly larger bottom-plate and well losses occur. This disadvantage is compensated by the lower switching frequency as well as the lower number of switches and supporting circuits.

Both topologies achieve comparable peak efficiencies, Fig. 3.14. Comparing the two efficiency curves it is noticeable that the efficiency curve of the three-phase converter for higher switching frequencies decreases strongly. This can be explained by the high bottom-plate and well charging losses, which scale with frequency and have a strong impact on efficiency. In general, bottom-plate losses represent a large proportion of total losses in fully integrated high-voltage SC converter topologies.

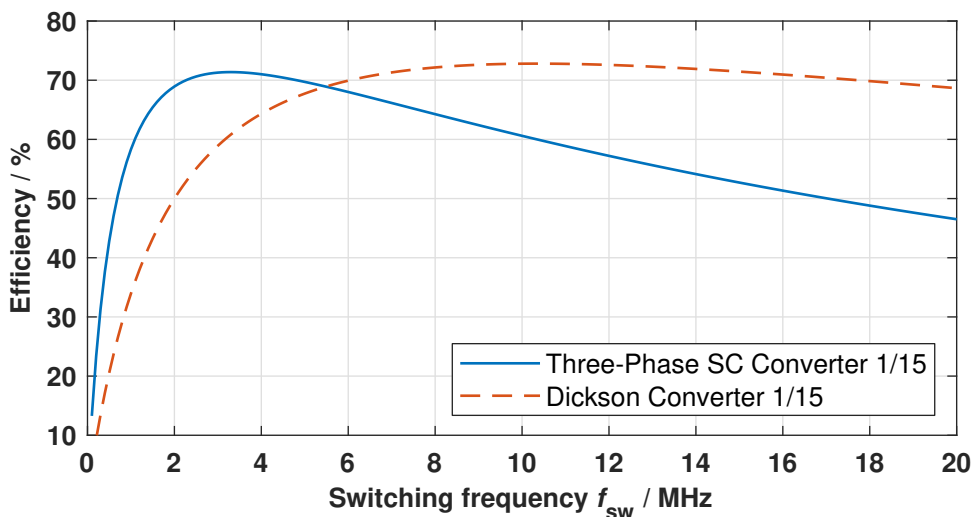


Fig. 3.14: Efficiency of the proposed three-phase SC converter and the Dickson converter at $V_{in} = 60$ V, $V_{out} = 3.3$ V and $P_{out} = 40$ mW.

Partially Integrated Approach

The maximum efficiency and output power in a fully integrated SC converter is limited mainly by losses in the output resistance and by recharging the parasitic bottom-plate capacitors. The low achievable capacitance values and the parasitic bottom-plate capacitance of the integrated capacitors are responsible for this limitation. External capacitors can be used to improve efficiency and increase output power. Thus, the

parasitic bottom-plate capacitance and the resulting losses are almost eliminated. In addition, the output resistance decreases significantly and the switching frequency can be considerably reduced, which has a positive effect on the extrinsic losses. In [101] a compact two-phase 11-to-1 SC converter with external capacitors is presented. With an input voltage of 37 V to 3.3 V, this converter achieves a high peak efficiency of up to 95.5%. The three-phase approach could reduce the number of external capacitors from 5 to 4, thus enabling an even more compact design. For this reason, the three-phase SC converter presented in this work is particularly suitable for implementation with external capacitors. Due to the small number of external capacitors, a compact design can be realized. Partial integration of the Dickson converter does not make sense due to the large number of capacitors.

Various partially integrated solutions of the three-phase SC converter are also possible, whereby, for example, only the flying capacitors are external. Figure 3.15 shows the efficiency of the different integration levels in comparison to the fully integrated approach. By replacing the two capacitors with the highest voltage swing and thus with the highest bottom-plate losses, the efficiency can be significantly increased compared to the fully integrated version. This is because these two capacitors cause about 70% of the bottom-plate losses in the fully integrated version. If all five capacitors are realized externally, the peak efficiency can be increased from 70% to over 90%. This shows the great potential of the three-phase SC converter for partially integrated solutions. By using external capacitors, the performance and efficiency can be significantly increased. Investigations by means of the proposed SC converter model (see Section 3.2) have shown that with small discrete capacitors (100 nF) an output power of 500 mW with a peak efficiency of greater than 90% can be achieved with a required chip area of only 2.5 mm².

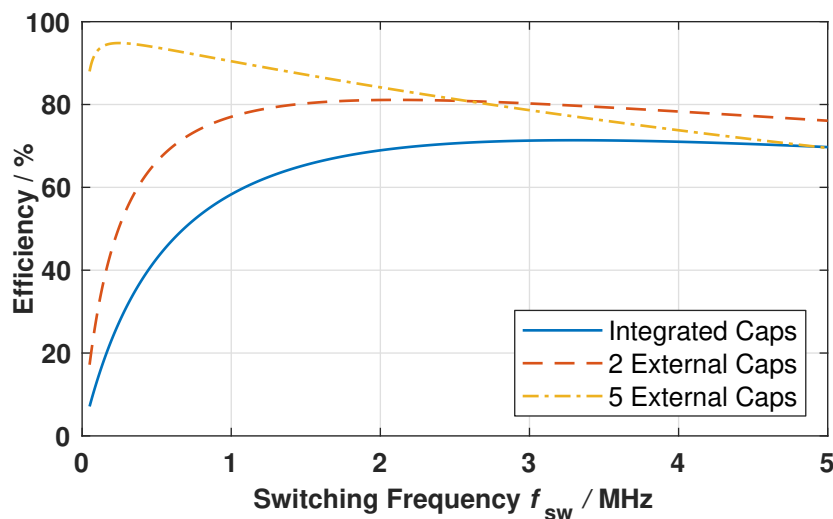


Fig. 3.15: Efficiency comparison of the proposed 15-to-1 three-phase SC converter for partially and fully integrated approach at $V_{in} = 60$ V, $P_{out} = 40$ mW and the external capacitors are realized by 100 nF each. The chip area for the integrated and two external capacitor approach is 4 mm² and for the five external capacitor approach is 0.5 mm².

The three-phase SC converter is a promising approach to achieve high conversion ratios for high input voltages. Through the full and partial integration, this concept is particularly suitable for the micro power supply presented in Chapter 6. In Chapter 4 the level shifter and other required supporting circuits will be introduced and discussed. However, in the framework of this research, priority was given the converter of Section 5 and various supporting circuits like level shifter, charge pump and back-to-back switch. As a future work, the three-phase SC converter is worth to be implemented and experimentally verified.

4 Building Blocks for High-Vin Switched-Capacitor Converters

One of the key challenges in high-voltage SC converters is the control of the power switches. Power switches may see different reference potentials depending on the respective conversion ratio, which can also change from one to the other phase. The supporting circuits required for reliable control are presented and discussed in this chapter.

In Section 4.1 conventional level shifters and their limitations are discussed in comparison to the high-voltage low-power optimized level shifter proposed in this work. An overview of common floating high-side supplies and the charge pump optimized for full integration in this work is given in Section 4.2, where also various concepts and their limitations are discussed. In Section 4.3 the loss and area optimized back-to-back switch configuration developed in this work is presented and explained. Section 4.4 addresses the loss optimization of the parasitic bottom-plate losses of the flying capacitors in the power stage.

4.1 Level Shifter

This Section highlights the challenges of the high-voltage capability and low-power consumption of common level shifter concepts and presents a capacitive high-speed and power-efficient level shifter. This section is based on the proposed level shifter, which was first published as part of this work in [48]. It is optimized for a sensitive and robust signal detection even at steep slopes of the reference voltage node V_{SSH} , suitable for highly integrated applications of up to 50 V. In Section 4.1.2 the design and implementation of the level shifter is shown and verified by the measurements in Section 4.1.3.

4.1.1 Conventional Level Shifter Concepts

In highly integrated systems, which can contain several power switches, the level shifter becomes an important building block, especially in high-voltage applications. A level shifter in such conditions should

comprise the following characteristics: (1) high-voltage capability, (2) low-power consumption, (3) low-propagation delay and (4) small area consumption. For low-voltage applications or applications where the signals need to be shifted to a constant voltage level, these characteristics can be achieved with good results [102–104]. The high-voltage capability of level shifters is often achieved at the cost of high-power consumption and increased propagation delay [102, 105–115]. Figure 4.1 shows the basic structure of a capacitive level shifter. In general, a level shifter consists of a low-side and a high-side part. These two parts are either connected by transistors or, as in the capacitive case shown, by coupling capacitors (C_{on} and C_{off}). Further the driver and the power switch of the power stage are shown. The high-side ground voltage V_{SSH} refers to the source of the power switch.

First, the loss mechanisms of high-voltage level shifters based on the capacitive level shifter are discussed in order to subsequently compare different level shifter concepts more precisely. With increasing voltage the high-side part of the level shifter must be isolated. In CMOS technologies this is done by a negatively doped well (n-well). This well forms a parasitic capacitance to the substrate C_{n-well} , which is charged and discharged by each voltage swing between a low- and a high-voltage value of V_{SSH} . Also the coupling capacitors C_{on} and C_{off} are charged and discharged. For transistor coupled concepts the parasitic drain-source capacitance must be recharged. Assuming that V_{SSH} switches between $V_{SSH} = V_{in}$ and $V_{SSH} = 0V$, the losses for one cycle (on/off) are derived by $P_{cap} = 2 \cdot 0.5 \cdot C \cdot V^2$. These losses scale quadratically with the voltage and causes a huge part of the power losses within a high-voltage level shifter. Since these losses occur in the power stage, they will not affect the power consumption of the level shifter. For this reason they are often not considered. However, these losses can have a significant impact on the system efficiency. Therefore, it is important to minimize the values of C_{on} , C_{off} , the size of the isolation n-well and other capacitance values from active devices between the high-side and the low-side of the level shifter.

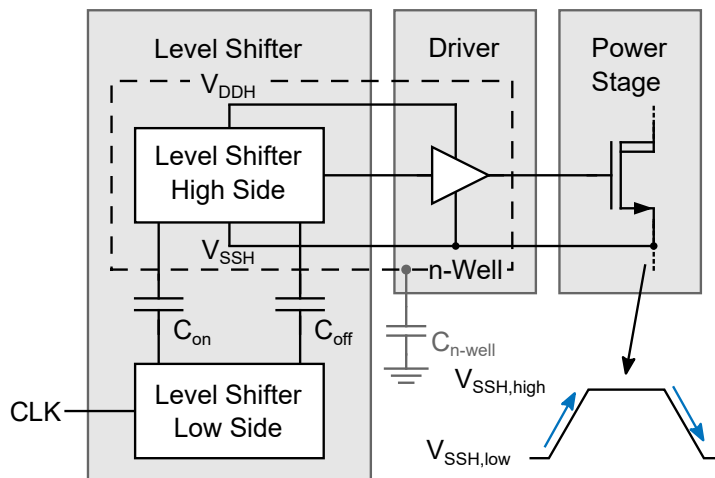


Fig. 4.1: Capacitive level shifter with driver stage and power switch.

Further with rising voltage slopes and voltage swings of V_{SSH} , also the Common Mode Displacement Currents (CMDC) or coupling currents in the signal path of C_{on} and C_{off} rises. For voltage slopes of several V/ns, the coupling currents are a few times higher than the signal currents are. This requires a reliable and robust signal detection on the level shifter high-side.

In Fig. 4.2 the commonly used level shifter topologies are shown. In Fig. 4.2(a) a common cross-coupled high-voltage level shifter is shown. It uses high-voltage transistors which require a large die area. Furthermore, the high-voltage transistors add large parasitic capacitance values that cause large coupling losses and increase the propagation delay of the level shifter significantly [106, 112, 116]. A shorter propagation delay can be obtained with larger devices but with the drawback of even larger area and higher losses, as discussed in [109, 116, 117]. [116] improves the cross-coupled level shifter in terms of propagation delay and power consumption but suffers from the cross-current drawn from V_{DDH} , these losses scale with the voltage level of V_{SSH} . The pulsed resistive level shifter depicted in Fig. 4.2(b) shows a good performance even at increasing voltage level of V_{SSH} [41, 44]. However, this concept also suffers from the parasitic capacitance values caused by the high-voltage transistors and the cross-currents from the high-side supply to the low-side part while this effect increases with the level of V_{DDH} . These cross-currents can be reduced to a minimum, by reducing the pulse length of the control signal. However, robust switching requires a minimum pulse width still causing losses. In Section 6.6.3 the sizing and design aspects are discussed in more detail. Figure 4.2(c) shows a simplified circuit of a current mirror based level shifter. This concept is utilized in [104, 109, 111] giving good results in terms of power consumption, speed and area, but also suffers from high peak currents drawn from V_{DDH} at every rising edge of the switching node V_{SSH} . This large amount of charge need to be buffered leading to a large buffer capacitor of the high-side supply. The latched capacitive level shifter shown in Figure 4.2(d) is often used for signal shifting to small high-side voltage levels or to a static reference voltage V_{SSH} like in [43, 67, 103, 104]. For a static V_{SSH} , such a level shifter achieves a low-power consumption even for high-voltage values of V_{SSH} as it does not scale up with

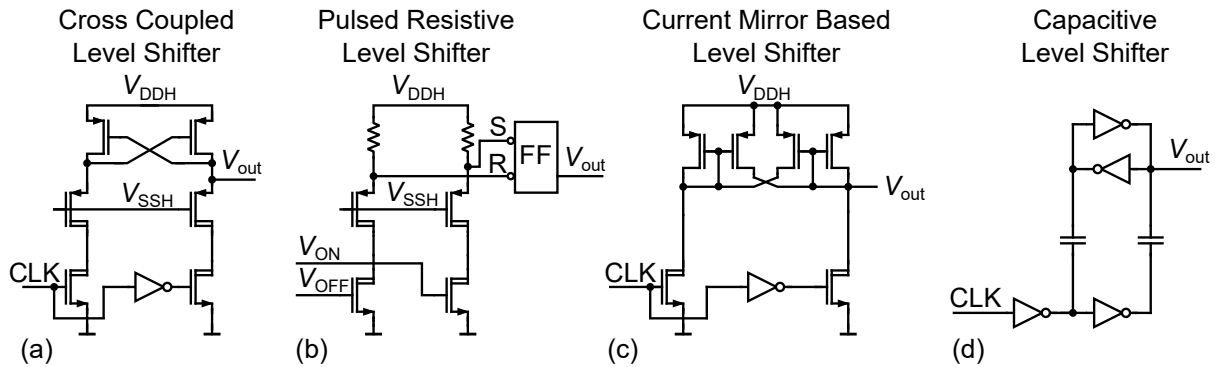


Fig. 4.2: Common level shifter topologies: (a) cross coupled level shifter, (b) pulsed resistive level shifter, (c) current mirror based level shifter and (d) capacitive level shifter.

the voltage level at V_{SSH} . Also, the propagation delay is independent of V_{SSH} .

Various clamping options are used to protect the low-voltage components referred to the floating high-side. The cross-coupled and pulsed resistive level shifters in Fig. 4.2(a) and (b) use PMOS cascodes for protection of the sensitive nodes. In the current mirror-based level shifter (Fig. 4.2(c)), the diode-connected PMOS transistors clamp the voltage at the sensitive nodes, additionally cascode transistors can be inserted. For the capacitive level shifter in Fig. 4.2(d), the intrinsic body diodes of the two inverter gates are responsible for clamping and protection.

The coupling between the low-side and the high-side voltage domain of a level shifter can be divided into two basic concepts. The coupling path is either realized by a high-voltage transistor like for the concepts in Fig. 4.2(a)-(c) or by a high-voltage capacitor like the capacitive level shifter in Fig. 4.2(d).

The robustness is an advantage of the transistor coupled concepts, which can be improved at the costs of power consumption. This counteracts to the design goal of lower power consumption. To improve the robustness of the capacitive level shifter a signal detection is introduced for the proposed level shifter in the following section. The level shifter of this work includes a switching node falling edge detection which allows both, small coupling capacitors C_{on} and C_{off} together with a sensitive and safe signal detection. This enables a robust operation during steep dv/dt transitions and a low-power consumption.

4.1.2 Capacitive High-Speed and Power-Efficient Level Shifter

The capacitive high-voltage level shifter is depicted in Fig. 4.3 with the corresponding signals in Fig. 4.4. This level shifter consists of the low-side part, the coupling capacitors C_{on} and C_{off} and the high-side part, which includes a sense blocks, a high-side logic block and a flip-flop.

The low-side inverters of the level shifter generate a negative and a positive transition at the bottom plate of C_{on} and C_{off} , respectively. This transition is shifted complementary by C_{on} and C_{off} (both 60fF) to the 1.8V high-side domain and is processed by the sense block. Every positive pulse at the nodes $V_{pulse,on}$ and $V_{pulse,off}$ is detected by the inverter consisting of MP_2/MN_3 or MP_4/MN_6 , respectively, passing a 'low' signal to the logic block. The transistors MN_1/MN_4 are used instead of pull-down resistors, and act as a weak pull-down resistor to bias $V_{pulse,on}$ and $V_{pulse,off}$ to V_{SSH} after a turn-on/-off event or a transition at V_{SSH} . The used NMOS transistors need significantly lower die area compared to resistors, which reduces the size of the n-well and hence the charging losses. Further the parasitic input capacitance at the sense block inputs $V_{pulse,on}$ and $V_{pulse,off}$ is reduced, which leads to a larger voltage signal after the charge balancing process between C_{on}/C_{off} and the parasitic input capacitance. This facilitates a further reduction of the coupling capacitors size and hence less charging losses occur. Negative pulses are clamped by the body diodes of the NMOS transistors MN_1/MN_2 or MN_4/MN_5 , respectively. The goal is, that a positive pulse at the node

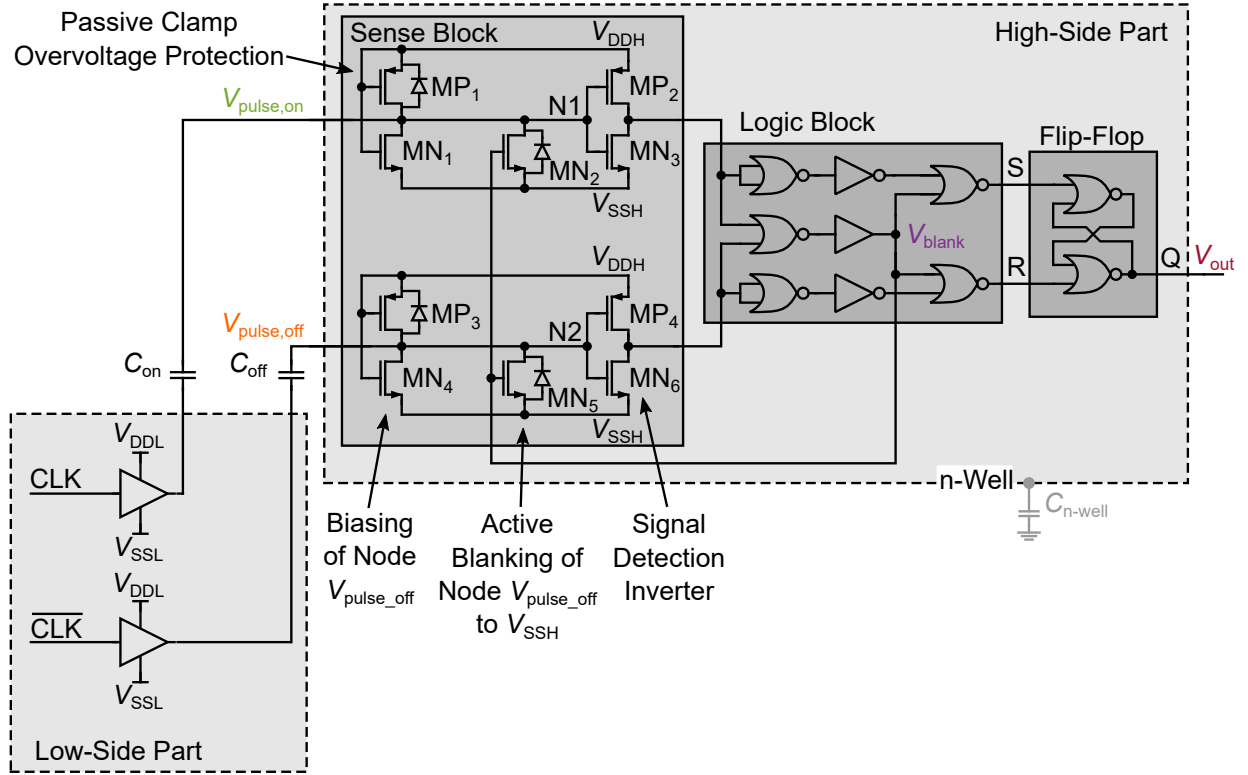


Fig. 4.3: Proposed capacitive level shifter implementation.

$V_{pulse,on}$ causes a set pulse at the flip-flop input S. Equally a positive pulse at the $V_{pulse,off}$ node yields a reset pulse to set the level shifter output V_{out} correctly.

In case of a rising transition at the node V_{SSH} , a negative pulse at both nodes $V_{pulse,off}$ and $V_{pulse,on}$ occurs, which does not trigger the input inverters and thus the inverter states are not affected. A falling transition at V_{SSH} results in a positive pulse at the input nodes, which triggers the inverters and lead to a logic ‘low’ at both sense block outputs. If these signals were connected directly via inverters to the flip-flop inputs, they would lead to a malfunction. Since the flip-flop is reset dominant, a falling transition of V_{SSH} would lead to a logic ‘low’ at V_{out} , even if a logic ‘high’ was transmitted from the low side. For this reason, a switching node falling edge detection circuit is realized in the logic block. This circuit detects a falling transition at V_{SSH} . In this case both signals $V_{pulse,off}$ and $V_{pulse,on}$ are ‘high’ and generate the blank signal V_{blank} . By design, it must be ensured that signal generation of V_{blank} is faster than the signal propagation to the flip-flop inputs. If the signal V_{blank} is ‘high’, a ‘low’ occurs at both flip-flop inputs, which leads to an unchanged output Q and thus keeps V_{out} at a constant level during interferences from V_{SSH} . While V_{blank} is ‘high’, the level shifter cannot receive input changes. In applications like in SC converters the timing of the V_{SSH} transitions is known and it can be designed such that an input change does not occur during these events. Since the interfering signals pump a much larger amount of charge into the input nodes than the signal does, the pull-down transistors would need a long time to pull down the nodes to the high-side

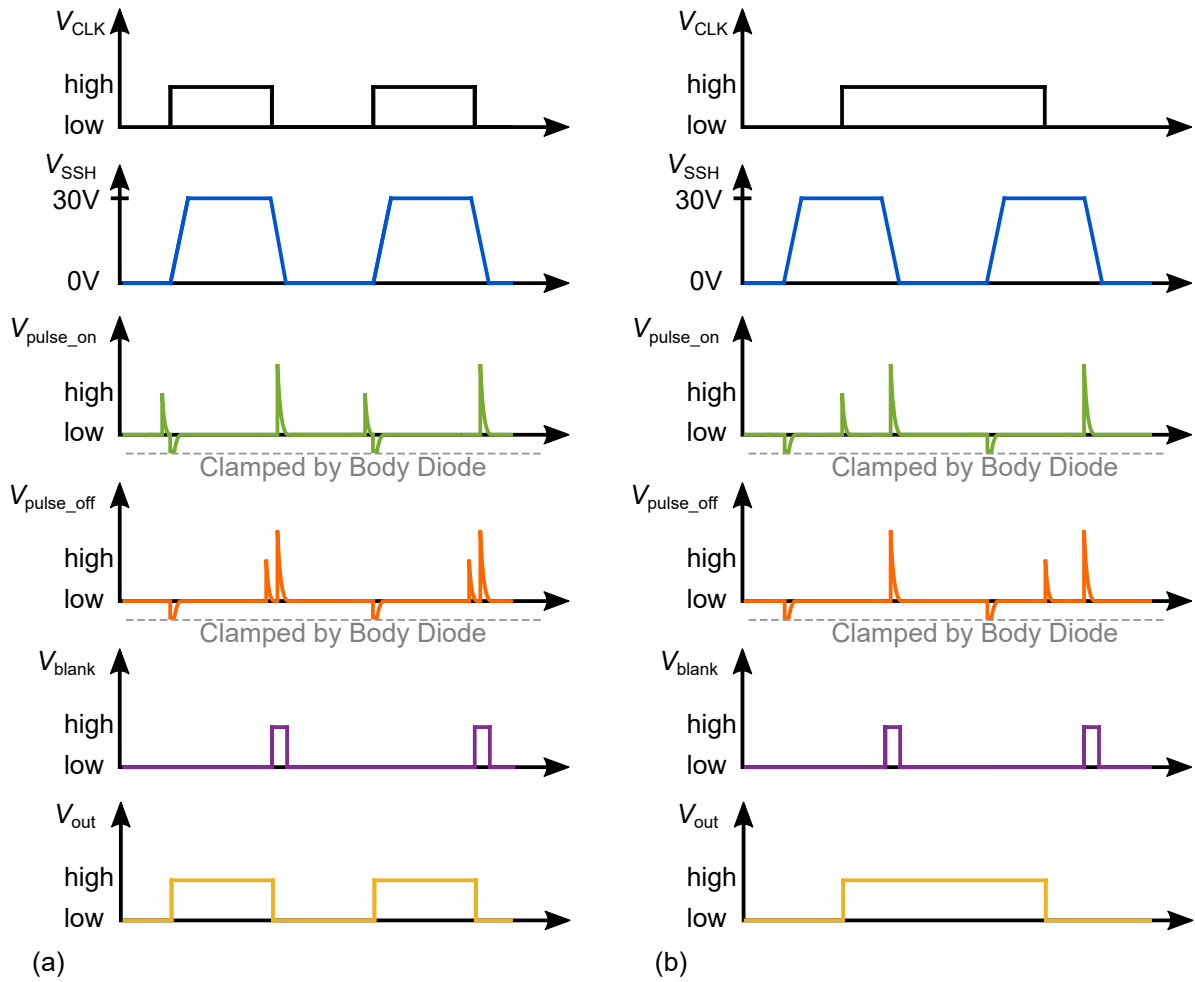


Fig. 4.4: Signal diagram of the proposed level shifter in (a) a half bridge, the high-side switch is triggered by the CLK signal and V_{SSH} follows. In (b), the signals CLK and V_{SSH} , are independent of each other.

ground. Therefore, the blank transistors MN_2 and MN_5 are inserted, which connect the input nodes during a disturbance with high-side ground. As a result, the sense block returns faster to the initial state. This active clamping enables high impedance bias transistors (MN_1 and MN_4), which reduce the size of the transistors and makes the input nodes more sensitive. This allows a further reduction of the size of C_{on} and C_{off} . This is possible because most of the charge will be shorted to high-side ground by the blank transistors MN_2 and MN_5 and the voltage will remain in the range of the maximum ratings of the sense block devices. MN_2 and MN_5 are controlled directly from the logic block. As an advantage, the capacitors C_{on}/C_{off} discharge to V_{SSH} and not to V_{DDH} with every falling transition of V_{SSH} . This is in contrast to cross-coupled level shifters, where at least one coupling element is clamped to V_{DDH} . Such level shifter concepts require a larger high-side buffer capacitance, since the recharge current flows through the buffer capacitor charging and discharging it. Nevertheless, the amplitude of these interfering signals at $V_{pulse,on}/V_{pulse,off}$ can be a few times larger than the amplitude of the wanted signals and may still exceed the device maximum ratings. To protect the circuit against these over voltages, the body diodes of the transistors MP_1/MP_3 clamp the nodes to V_{DDH} . Furthermore, the sense block transistors have a maximum rating of 5 V. All other transistors are 1.8 V thin gate oxide transistors.

The introduced capacitive level shifter design achieves a low-power consumption and a robust and reliable signal detection as verified by the measurement results in the following Section.

4.1.3 Experimental Results

The level shifter has been manufactured in a 0.18 μm high-voltage CMOS technology, the chip photograph is depicted in Fig. 4.5. The circuit area including the isolation wells measures $7350\mu\text{m}^2$ ($3370\mu\text{m}^2$ without isolation wells). The measurements in Fig. 4.6 confirm a robust switching of the level shifter at V_{SSH} transitions up to 50 V with slew rates of up to 6 V/ns. Both, the V_{out} high- and low-state are kept stable during a rising and falling transition of V_{SSH} , respectively. While the slew rates in the measurement setup

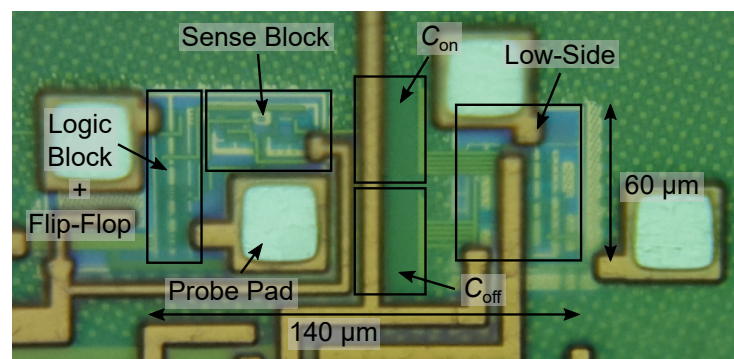


Fig. 4.5: Photograph of the capacitive level shifter.

are limited to several V/ns, postlayout simulations show a robust level shifter operation for V_{SSH} transitions of up to 100V/ns.

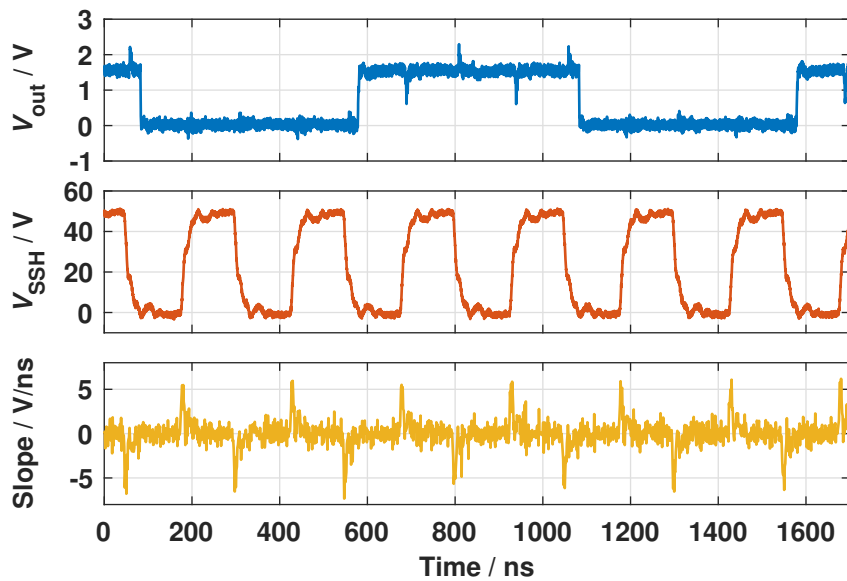


Fig. 4.6: Measurement verification of the robustness and functionality of the proposed level shifter at 50 V V_{SSH} transients.

Figure 4.7 confirms the correct operation at a switching frequency of 120MHz and a voltage level of $V_{SSH} = 50$ V. While the voltage is limited by the technology, used in this design, the proposed level shifter concept can be applied for even higher voltages.

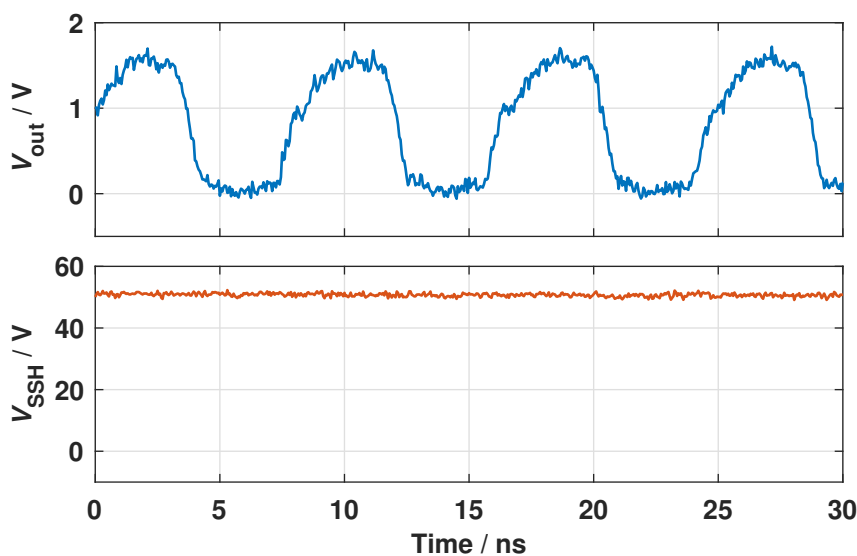


Fig. 4.7: Level shifter switching at maximum frequency of 120 MHz at $V_{SSH} = 50$ V.

Figure 4.8 shows the measured level shifter propagation delays of the rising and falling edge of V_{out} over the floating ground potential V_{SSH} . The measurements confirm a nearly constant propagation over a wide voltage range of the floating ground potential V_{SSH} . A rising and falling propagation delay of less than 1.45 ns and 1.3 ns, respectively, is achieved. The difference between the rising and the falling edge propagation delay is caused by the reset dominant flip-flop. For the rising edge, there is one gate more in the signal path, which results in the shown difference.

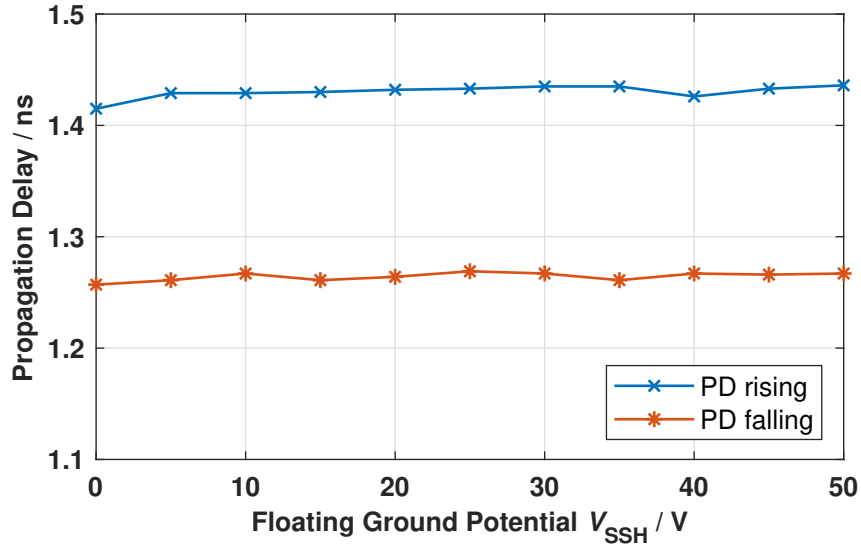


Fig. 4.8: Propagation delay measurements of the proposed level shifter.

In Fig. 4.9 the measured energy consumption per transition is depicted over increasing voltage values of V_{SSH} . At a static V_{SSH} voltage, the level shifter requires in total only 2.1 pJ energy per transition, the high-side and the low-side part of the level shifter consume both around 1 pJ. The low-power consumption at the high-side part, of the proposed design, leads to relaxed requirements for the high-side power supply. The power consumption remains constant over the entire voltage range. This is due to the capacitive coupling, where no charge flows from the high-side part to the low-side part. The energy consumption is almost the same for 50 MHz and 100 MHz operation, as expected. Figure 4.9 indicates the state of the art for 50 V design [109] and for 20 V designs [108, 117]. For these concepts the power consumption scales up with the voltage level of V_{SSH} . This is due to the concept related cross-currents from the high-side voltage domain to ground (V_{SSL}). The power consumption of the proposed concept is reduced by at least 65% at 17.5 V.

Table 4.1 gives a comparison to the state of the art. The listed level shifters are all integrated level shifters. The voltage capability of the proposed level shifter is up to 50 V. Even at this high voltage, the level shifter energy consumption, is as low as 2.1 pJ per transition. This is the lowest reported power consumption for a level shifter, which copes 50 V. Compared [108, 109, 111, 117] to this work, the power consumption of

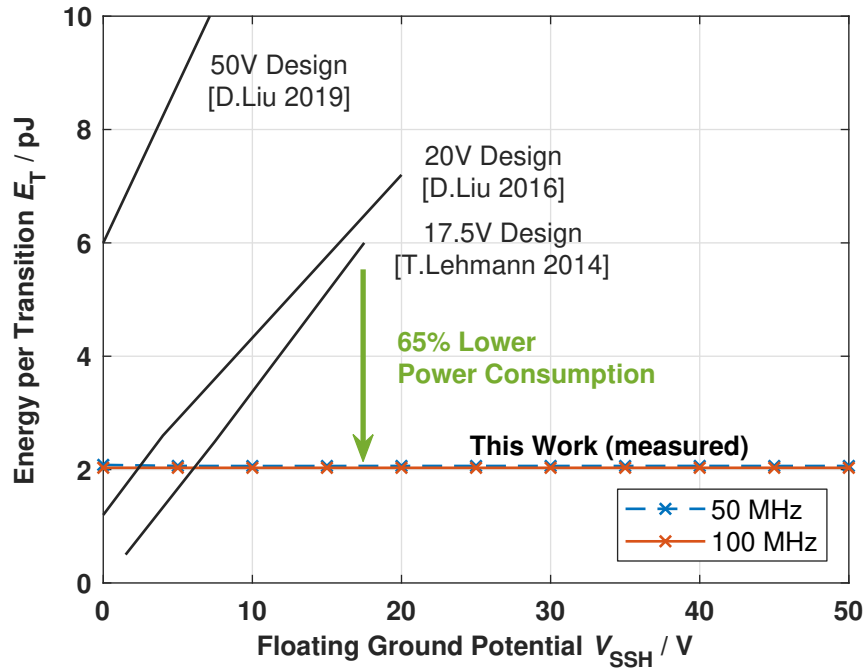


Fig. 4.9: Energy consumption measurements of the proposed level shifter with a comparison to the state of the art.

this work is significant lower even compared to designs for lower voltages. The power consumption of the proposed high-voltage level shifter is more than eleven times lower compared to the state of the art. The achieved propagation delay is less than 1.45 ns. Only [117] and [109] is faster, but [117] operates only up to 20 V and [109] requires a higher power consumption. For a fair comparison, a figure of merit was introduced by [117]. This figure of merit takes the process node, the maximum voltage, the energy consumption and the delay into account. A lower value is better. This work achieves the lowest reported value of 10.5, however, this corresponds to a reduction of 50% compared to the state of the art.

Tab. 4.1: Comparison with previous work

| | [116] | [108] | [117] | [102] | [106] | [111] | [109] | This Work |
|------------------|--------------------|--------------------|--------------------|-------------------|--------------------|--------------------|--------------------|--------------------|
| Technology | 0.35 μm | 0.35 μm | 0.18 μm | 0.5 μm | 0.18 μm | 0.35 μm | 0.18 μm | 0.18 μm |
| Voltage (V) | 10 | 20 | 20 | 40 | 50 | 50 | 50 | 50 |
| E_t (pJ) | 24 ² | 6 ¹ | 7.2 ¹ | 246 ² | N/A | 23.75 ² | 30.3 | 2.1 |
| Delay (ns) | 2.4 | 3 ¹ | 0.37 | 2 ¹ | 5 | 2.03 | 0.53 | 1.45 |
| FOM ³ | 134.3 | 21 | 23 | 98.4 | N/A | 22.5 | 54 | 10.5 |

¹Simulated. ²Extracted from results in the publication. ³From [117]: $(E_t \cdot \text{Delay}) / (\text{Process node}^3 \cdot \text{Voltage})$
Unit: $(\text{pJ} \cdot \text{ns}) / (\mu\text{m}^3 \cdot \text{V})$, lower is better.

4.2 Charge Pump

The challenge of building a floating high-side supply, is the floating voltage reference level V_{SSH} , which is usually the switch node. V_{SSH} may change over time, which makes it impossible to use a power supply fixed to a constant voltage level like ground (V_{SSL}). This section describes various floating high-side supplies concepts and discusses their suitability in integrated SC converters. As part of this work, a charge pump concept is optimized for use in fully integrated SC converters and is based on and first published in [44].

The floating high-side power supply required to drive the power switches in high-voltage SC converters can be solved by different approaches. It can be realized by a transformer [118, 119]. This offers the advantage of galvanic isolation, but the integration of a transformer still suffers from the worse performance and the area consumption for on-chip integration. The usage of a transformer based floating high-side supply in a SC converter is not applicable, because of the several power switches within the power stage, where each switch needs its own floating high-side supply. Therefore the transformer-based approach will not be further investigated. A voltage supply solution can be realized by a low-dropout regulator (LDO) or series regulator [120, 121]. This solution can be used in certain cases, but may be inefficient depending on the conditions. Depending on the voltage level and the operating mode of the SC converter, e.g. buck or boost operation, the series regulator approach may not be suitable.

A bootstrap circuit can be used for the floating high-side power supply. This concept can be integrated on-chip and is often used in half bridges, but there are two main limitations. First, the high-side supply must be recharged frequently. This requires a regular switching transition from V_{SSH} to ground and prevents a permanent turn on. Secondly, there may be a large voltage drop across the on-resistance of the low-side switch, this could lead to an insufficient power supply to adequately turn on the power switches [122, 123]. In Fig. 4.10(a) a bootstrap circuit is depicted. This circuit is simple and efficient and should be used if possible [44, 124, 125].

In many cases where the switching node, which is connected to V_{SSH} , does not return to ground frequently, a charge pump is needed instead of the bootstrap circuit. The first fully integrated Dickson charge pump was introduced in 1976 [126]. Since then, many different charge pump topologies have been introduced [107, 122, 123, 127]. Some of them, have been especially optimized for applications and requirements, such as for permanent turn on. These special circuits are usually complex and not suitable for the use in SC converters where several charge pumps are needed [107, 127]. The requirements of floating high-side supplies for SC converters with high input voltages, are high dielectric strength and efficiency. In addition, they should be easy to integrate into CMOS and take up little space as they are required for each switch of the power stage. The system clock of SC converters is suitable for regular recharging due to a duty cycle of

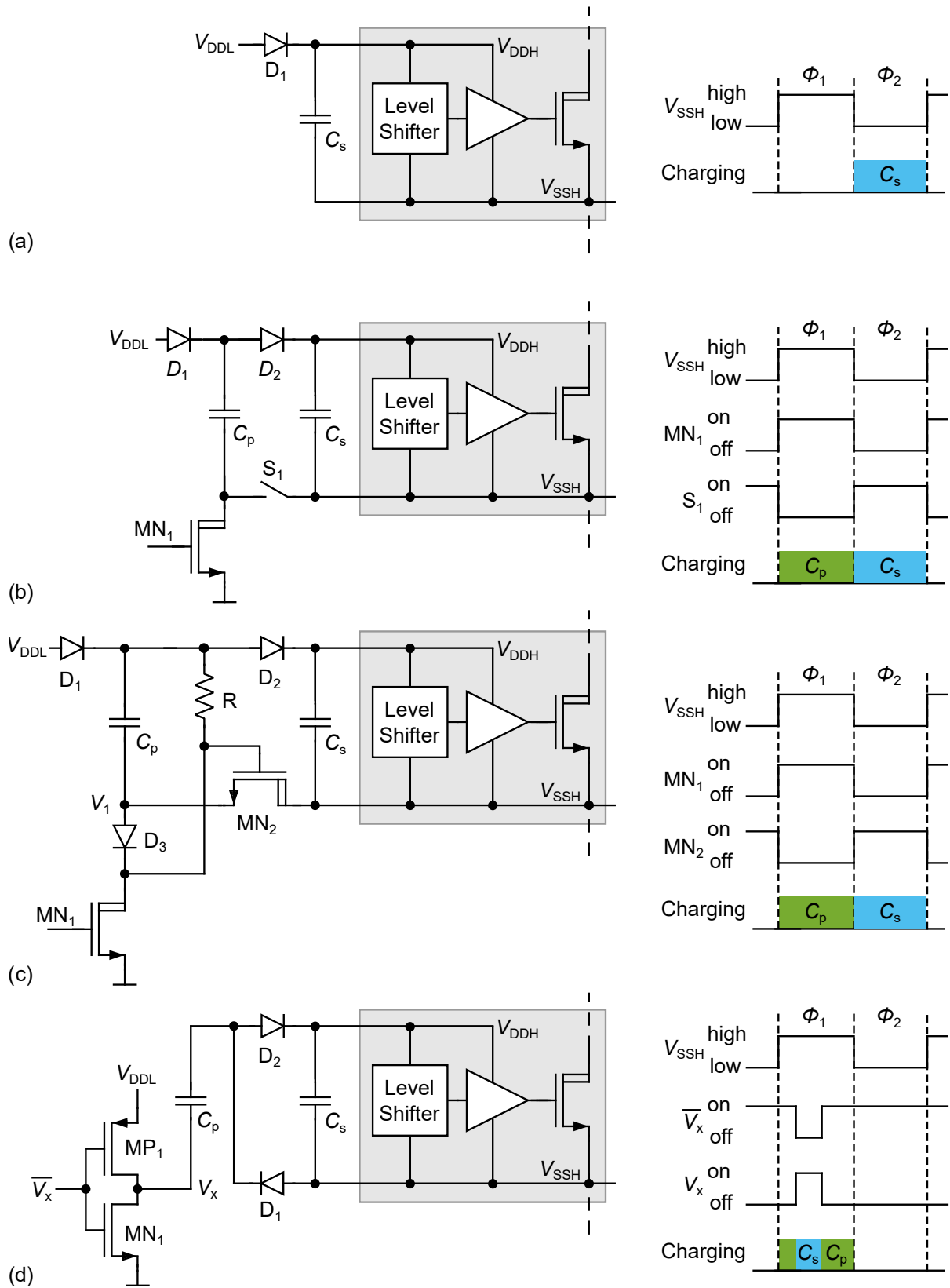


Fig. 4.10: Overview of the different charge pump topologies, (a) bootstrap circuit, (b) ideal floating charge pump (c) self-boost charge pump and (d) source-supplied charge pump.

50%. In Fig. 4.10(b) an ideal charge pump is depicted. The pump capacitor C_p will be charged via diode D_1 when the switch S_1 is open and the transistor MN_1 is turned on (phase ϕ_1). The stored charge in C_p will be shifted up by turning off transistor MN_1 and closing S_1 . C_p charges the buffer capacitor C_s via D_2 (phase ϕ_2). The difficulty of the floating charge pump is the implementation of switch S_1 . If S_1 is a PMOS transistor, a voltage level of $V_{SSH} - V_{DDL}$ has to be generated in order to drive the PMOS properly. If S_1 is replaced by a NMOS transistor, then the drain is connected to V_{SSH} and the source to the drain of MN_1 . For this configuration an additional level shifter needs to control the NMOS transistor. The challenges associated with S_1 are solved for the self-boost charge pump depicted in Fig. 4.10(c) [123]. In this topology the switch S_1 and the level shifter is formed by the high-voltage transistor MN_2 , the resistor R and the diode D_3 . If MN_1 is turned on, C_p will be charged from V_{DDL} via D_1 , D_3 and MN_1 (in phase ϕ_1). MN_2 remains turned off as long as MN_1 is turned on. After MN_1 is switched off, the pull up resistor R turns MN_2 on and the stored charge on C_p will be transferred to C_s (in phase ϕ_2). The self-boost charge pump is an universal charge pump, which works independent of the voltage levels on the voltage reference node V_{SSH} . This comes at the cost of the losses in R , while transistor MN_1 is turned on. A reduction of these losses can be achieved by a pulsed control signal for MN_1 . A major disadvantage of this concept is the use of three diodes, which increases the losses and significantly reduces the turn-on voltage ($V_{DDH} - V_{SSH} = V_{DDL} - 3V_F$). The use of Schottky diodes allows to keep the voltage drop at an acceptable level. Also the parasitic bottom-plate capacitance of the pumping capacitor represents an additional loss mechanism. The voltage swing of node V_1 in Fig. 4.10(c) ranges from 0 V to V_{SSH} . Since V_{SSH} can take high-voltage levels, the losses due to parasitic bottom-plate capacitance are significant. To reduce these losses, the proposed technique, described in Section 4.4 can reduce these losses.

In order to eliminate the additional diode voltage drop and to increase the efficiency, the source-supplied charge pump of Fig. 4.10(d) is utilized. This charge pump topology was introduced in [122]. However, the proposed sizing and operation mode are not suitable for integrated low-power SC converters. [122] proposes a sizing of $C_s \gg C_p$, which leads to high charge pump switching frequency $f_{cp} \gg f_{sw} = 1$ MHz, which would reduce the charge pump efficiency. In [128], further types of charge pumps with slightly different concept and operation were compared, but these concepts suffer from worse efficiency and are not suitable for multi-ratio SC converters. For integrated low-power applications, the source-supplied charge pump shows a good trade-off between efficiency, area consumption and voltage ripple on C_s with a sizing approach of $C_s \sim 2 \times C_p$ and $f_{cp} = f_{sw}$ in this work.

C_p will be charged from the reference voltage node V_{SSH} via D_1 , while MN_1 is turned on and V_x is connected to ground (section of phase ϕ_1). By switching node V_x to V_{DDL} , the bottom-plate of C_p receives a voltage step of V_{DDL} , and the stored charge will be transferred to C_s (section of phase ϕ_1). Figure 4.10 also shows the timing of the signals for the charge pump. For a correct function of the charge pump, the pulse of signal

V_x needs to happen while V_{SSH} is at high level. The pulse length is determined by the RC time constant of the charge balancing process between C_p and C_s . The source-supplied charge pump reduces the parasitic bottom-plate losses due to the reduced voltage swing especially at high input voltages. The voltage drop is reduced from three to two diodes. This charge pump works, if the floating voltage reference level (V_{SSH}) is fix at a certain voltage or if the voltage swing at node V_{SSH} is in the range of V_{DDL} or smaller.

In Fig. 4.11, the efficiency simulation results of the self-boost charge pump and the introduced source-supplied charge pump are shown for different use cases. In Fig. 4.11(a), the general setup and signal definition are depicted. The signal V_{SSH} represents the source potential of a power stage transistor, i.e. it is one of the switching nodes of a SC converter. This node jumps during the two phases between a low and a high-voltage level. The value of this difference is represented by the variable ΔV_S . The second variable $V_{SSH,low}$ indicates the voltage difference between ground and the lowest value of V_{SSH} . The efficiency of both concepts is shown in Fig. 4.11(b) for a constant source potential $V_{SSH} = 0\text{ V}$ while ΔV_S sweeps from 0 V to 5 V. The graph shows a small efficiency enhancement of the source-supplied charge pump compared with respect to the self-boost charge pump because of only two diodes instead of three diodes in the charging path. For this setting, a bootstrap circuit could be used with slightly higher efficiency of up to 78%. For the following settings Fig. 4.11(c) and (d) the bootstrap circuit is not applicable because V_{SSH} does not return to ground. In Fig. 4.11(c) the efficiency is shown for the same conditions as in (b) except for $V_{SSH,low} = 10\text{ V}$. In this plot the impact of the bottom-plate losses become obvious. For the source-supplied charge pump, the bottom plate will be charged and discharged with $V_{DDL} = 5\text{ V}$ compared to the self-boost charge pump where the bottom plate of C_p will be charged and discharged with $V_{SSH,low} = 10\text{ V}$. Hence, the efficiency enhancement of the source-supplied charge pump is more than 30%. The efficiency increase of the source-supplied charge pump starting at around $\Delta V_S = 4.5\text{ V}$ is due to additional charge, which is transferred from C_p to C_s during ϕ_2 . The impact of the bottom-plate losses to the efficiency can also be noticed in Fig. 4.11(d). For this plot the voltage $V_{SSH,low}$ rises from 1 V to 20 V and $\Delta V_S = 0\text{ V}$. However, the efficiency of the source-supplied charge pump stays constant as expected, since the bottom plate of C_p is charged and discharged with the fixed voltage of V_{DDL} . For the self-boost charge pump, the bottom plate of C_p is charged and discharged with the rising voltage of $V_{SSH,low}$. This leads to a reduced efficiency due to rising bottom-plate losses. The simulation results show the significant efficiency improvement of the utilized source-supplied charge pump in this work compared to the self-boost charge pump. The efficiency enhancement is significant at 20 V.

Both the self-boost and the source-supplied charge pump have been implemented in a 0.35 μm high-voltage CMOS technology, Fig. 4.12. The self-boost charge pump occupies slightly more area than the source-supplied charge pump due to the extra high-voltage components. The marked biasing resistance R_{bias} is used in both charge pumps for the bottom-plate loss reduction of C_p and C_s , which is introduced in Section 4.4.

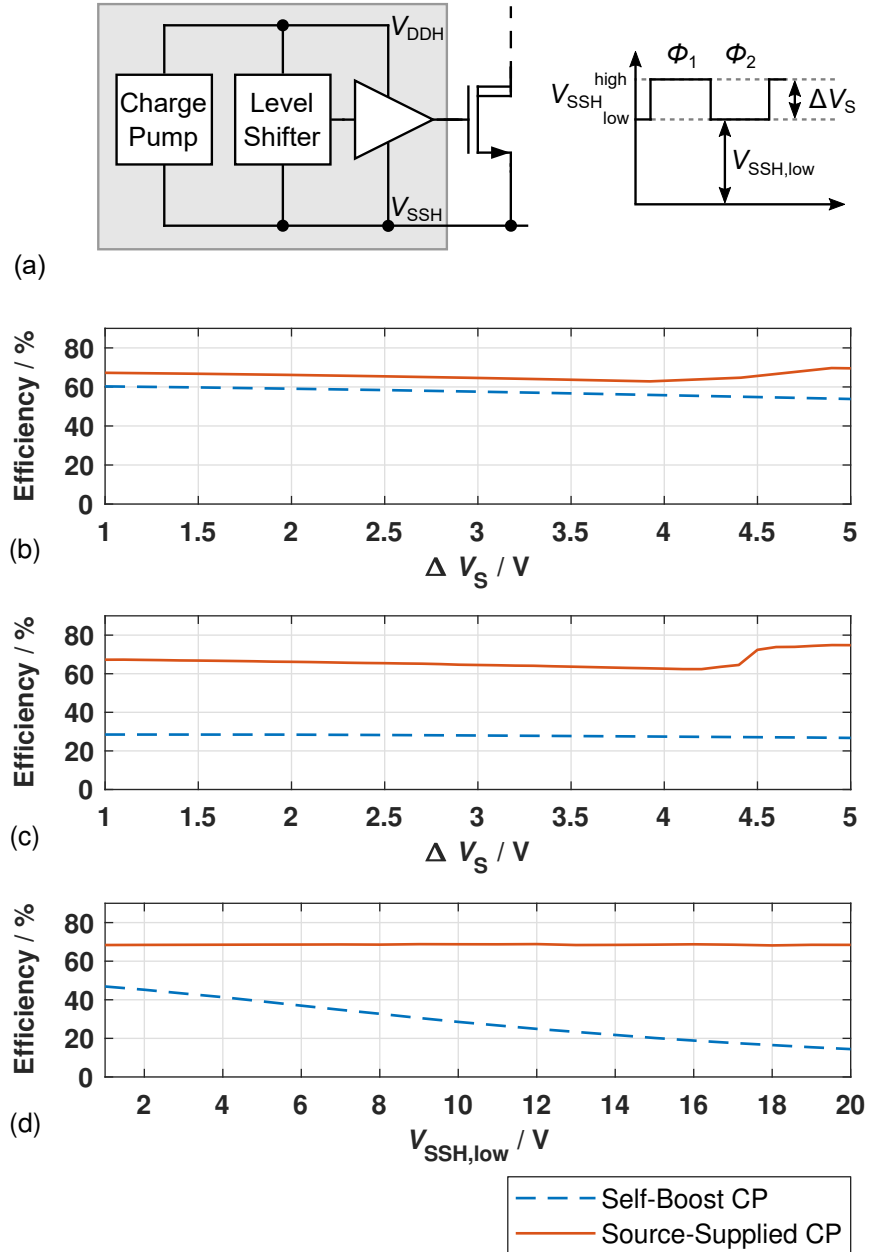


Fig. 4.11: Efficiency comparison of the self-boost charge pump and the source-supplied charge pump for different conditions. (a) Setup and signal definition. Simulation results for (b) $V_{SSH,low} = 0V$, $\Delta V_S = 1...5V$, (c) $V_{SSH,low} = 10V$, $\Delta V_S = 1...5V$ and (d) $V_{SSH,low} = 1...20V$, $\Delta V_S = 0V$.

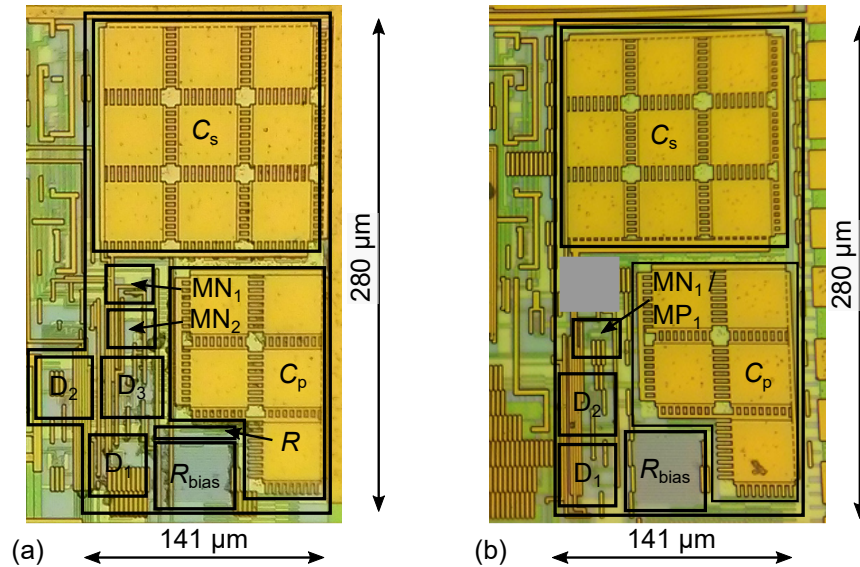


Fig. 4.12: Photograph of the implemented (a) self-boost charge pump and (b) source-supplied charge pump.

In this design, MIM capacitors were used for C_p and C_s instead of MOS capacitors, as these cause lower bottom-plate losses and thus improve overall efficiency.

Table 4.2 shows a comparison of the floating high-side supply concepts of Fig. 4.10 and a LDO. The bootstrap circuit, LDO, self-boost charge pump and the source-supplied charge pump are evaluated with respect to the number of high-voltage devices, voltage drop caused by diodes, integration on-chip, usability in SC converters and the efficiency. The count of high-voltage devices somehow correlates to the size and the efficiency of the floating high-side supplies. For the bootstrap circuit (Fig. 4.10(a)) only D_1 is a high-voltage device. The self-boost charge pump (Fig. 4.10(c)) needs four high-voltage devices, two high-voltage transistors MN_1 and MN_2 and two diodes D_1 and D_2 . For the source-supplied charge pump (Fig. 4.10(d)) only one high-voltage capacitor (C_p) is required. The number of diodes also impacts the efficiency. Considering the efficiency, the table indicates that the bootstrap circuit and the source-supplied charge pump have a good overall performance and are the first choice if the usage is possible. The self-boost charge pump can be used where bootstrap and source-supplied charge pump are not applicable. Section 6.6 shows the usage of the different floating high-side supplies in a 4:1 SC converter.

4.3 Bidirectional Switch

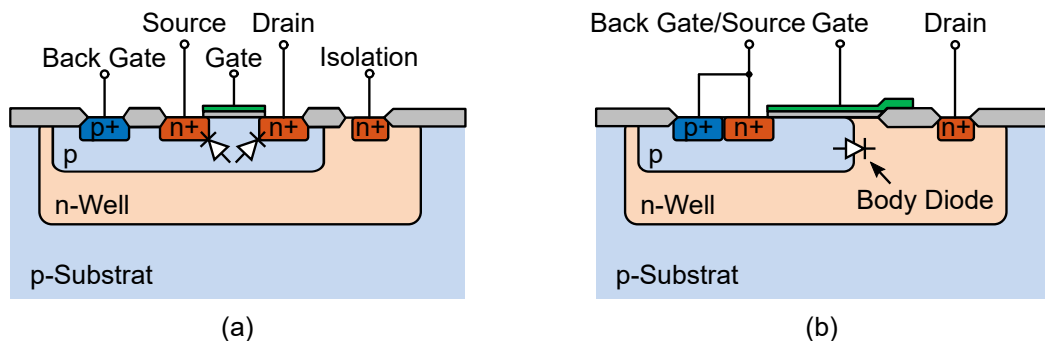
The reconfigurability of multi-ratio SC converters and other high-voltage applications can result in different voltage polarity across the power switches. Depending on the configuration, charge flow through the body diode need to be prevented. This can also occur in other applications and demands for a bidirectional

Tab. 4.2: Floating high-side supply comparison

| | Bootstrap | LDO | Self-Boost | Source-Supplied |
|----------------------------|-----------|-----|------------|-----------------|
| HV Devices | 1 | 1 | 4 | 1 |
| Drops by Diodes | V_F | - | $3 V_F$ | $2 V_F$ |
| Suitable for Integration | + | + | + | + |
| Suitable for SC Converters | + | o | ++ | + |
| Efficiency | ++ | - | - | ++ |

switch, also known as a back-to-back switch. The conventional back-to-back switch concept requires large switches to keep its total on-resistance at the same level. This, however, increases the gate charge losses P_{gate} (Section 2.3.2) of the power switches by a factor of four reducing the system efficiency. The back-to-back switch concept presented in this section [41] significantly reduces the dynamic switching losses and the total area consumption.

For different conversion ratios of multi-ratio SC converters the voltage across the drain-source voltage of a power transistor can vary. It can even be negative, which would result in a current through the intrinsic body diode that causes cross-currents and a malfunction of the circuit. In Fig. 4.13 a cross section of a symmetrical NMOS and an asymmetrical DMOS is shown, respectively. The intrinsic body diodes are situated between the p-region and the n-regions for the symmetrical NMOS, one diode to the source and one to the drain. In DMOS transistors, source and back gate are directly connected by metal, so the body diode forms between source (back gate) and drain. For both transistor types the intrinsic body diode is always there. Figure 4.14(a) illustrates the body diode scenario at a high-voltage power transistor. For example, this could be a switch in the recursive buck-boost SC converter of Section 3.4.1. The voltage levels of the source and drain contact indicate a positive V_{SD} voltage for the shown transistor. In this case, even if the

**Fig. 4.13:** Cross section of (a) a symmetric low-voltage NMOS and (b) an asymmetric high-voltage DMOS.

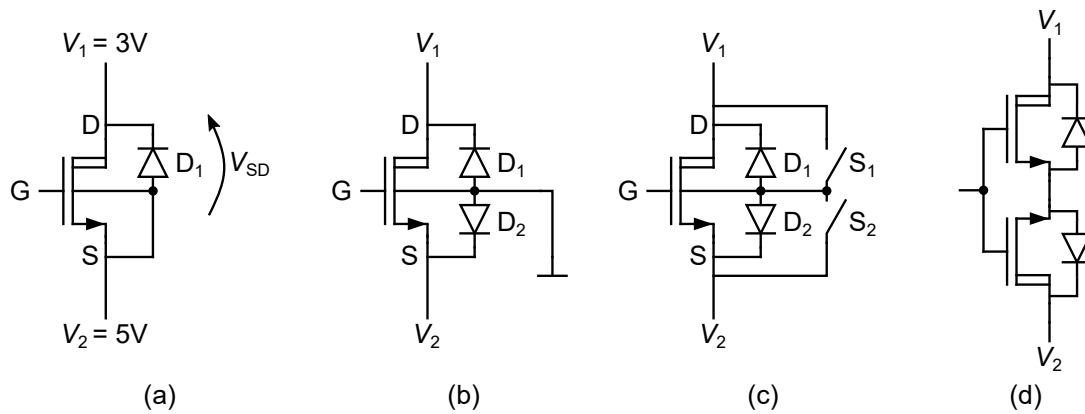


Fig. 4.14: Different circuit solutions to avoid body diode conduction.

transistor is turned off, a current flows through the body diode and leads to a malfunction.

There are three options to prevent this malfunction. A first option is depicted in Fig. 4.14(b), for this case the back gate is connected to ground or to the lowest occurring voltage-level at this transistor, as a consequence D_1 and D_2 will block the current. This usually works only for low-voltage applications where the maximum voltages across the device is equal or less than the maximum voltage ratings of the device. The limiting factor here is the oxide breakdown voltage of the transistors. However, this solution is not suitable for high-voltage application. The second option, Fig. 4.14(c), avoids the diode conduction by connecting the back gate dynamically to the lower voltage level of either source- or drain-potential by closing S_2 or S_1 , respectively. This concept needs some overhead circuit to control the switches S_1 and S_2 and is limited to the lowest voltage rating of the device, which is usually V_{GS} or V_{BS} . For symmetric devices as shown in Fig. 4.13(a), the transistor parameters V_{GS} , V_{DG} , V_{BS} and V_{DB} have usually the same maximum voltage ratings, and can be therefore used for this concept. But for asymmetric high-voltage devices like the DMOS depicted in Fig. 4.13(b), the maximum voltage-rating of V_{GS} is usually a few times lower compared to V_{DG} . For a typical 20 V high-voltage DMOS transistor with $V_{DG} = 20$ V V_{GS} is restricted to 5 V. These asymmetric voltage ratings make using this option particular difficult. A standard solution is the anti-serial switch structure called "back-to-back" configuration or "bidirectional switch", which is shown in Fig. 4.14(d). This structure can be build by connecting either the source or the drain terminals of two transistors. By connecting the source terminals, the same gate drive (consisting of charge pump, level shifter and gate driver) for both transistors can be used. For the block mode of the structure (both transistors are turned off) one of the body diodes is in reverse and blocks the current. This concept works for low-voltage and high-voltage applications. The serial connection of two transistors has a negative effect on the total R_{On} resistance value of the circuit. In order to eliminate the undesired increase in resistance, the transistor size must be doubled. This increases the gate charge losses and the area required by a factor of four compared to a single transistor. Both effects have a negative impact on efficiency and system performance. For

applications where the back-to-back switch is rarely turned on or off, the standard topology in Fig. 4.14(d) is the best choice and the increased gate charge losses are negligible. However, if the switching frequency increases, the losses get too large and require alternative solutions.

In many applications the voltage polarity of $V_1 - V_2$ is known, e.g. by the system state or in case of a SC converter the current ratio defines the polarity. Often, the voltage polarity of $V_1 - V_2$ in such applications changes only from time to time, e.g. if the SC converter changes its ratio. These preconditions enable the gate charge loss minimization through the back-to-back topology proposed in this work. Figure 4.15(a) shows the modification of the standard back-to-back topology of Fig. 4.14(d), where transistors A and B can be separately controlled. Assuming $V_1 < V_2$ (Fig. 4.15(a)) allows transistor A to be turned on statically, since the body diode of transistor A conducts for this voltage levels anyway. This yields half the gate charge losses, since compared to the standard topology only transistor B is driven dynamically with the CLK signal. Furthermore the charge pump can be half the size compared to the standard solution because only half the gate charge has to be provided. The dynamic gate charge losses of transistor B can be further reduced by reducing the transistor size of the dynamic switching transistor B and increasing the size of static turned on transistor A, as shown in Fig. 4.15(b). The sum of the total resistance remains constant. This allows to reduce the transistor size of B almost to the original size of the single switching transistor, which is replaced by the back-to-back switch. This corresponds approximately to a further reduction of the transistor size by half and consequently of the losses and charge pump size. In the event that the voltage V_1 is greater than V_2 , the switch configuration must be reversed as shown in Fig. 4.15(c). In this case, transistor D is permanently turned on and transistor C is clocked. The combination of (b) and (c) results in the loss-optimized back-to-back switch topology shown in Fig. 4.15(d). The control signals still refer to the case that V_1 is greater than V_2 . This results in the equivalent circuit diagram shown in Fig. 4.15(e). In order to save layout area, transistor B is permanently switched on in parallel to transistor D. Taking this into account, the sizing of

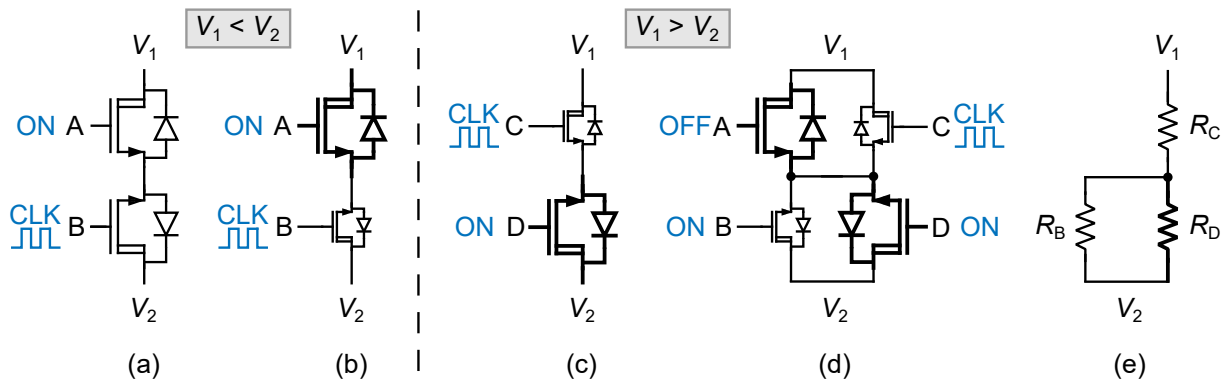


Fig. 4.15: Proposed loss optimized back-to-back circuit structure and equivalent circuit.

all four transistors needs to be in a way that the overall resistance $R_{on,total}$ fulfills the target resistance. With $R_A = R_D = R_{static}$ and $R_B = R_C = R_{dynamic}$, $R_{on,total}$ can be calculated by

$$R_{on,total} = R_{dynamic} + \frac{R_{dynamic} \cdot R_{static}}{R_{dynamic} + R_{static}} \tag{4.1}$$

The sizing goal is to minimize the gate charge losses P_{gate} for a given $R_{on,total}$. This means that the transistors B and C are sized as small as possible, ideally like the size of the single transistor, which is replaced by the back-to-back switch.

Figure 4.16 shows the normalized gate charge losses and the normalized required area of the power transistors as a function of the ratio $x = R_{static}/R_{dynamic}$. Losses and area are normalized to the common back-to-back switch concept as depicted in Fig. 4.14(d). While the area scales up for $x > 1$, the loss reduction is significant for small ratios and saturates at 25%, which is equal to the losses of a single transistor. A ratio greater

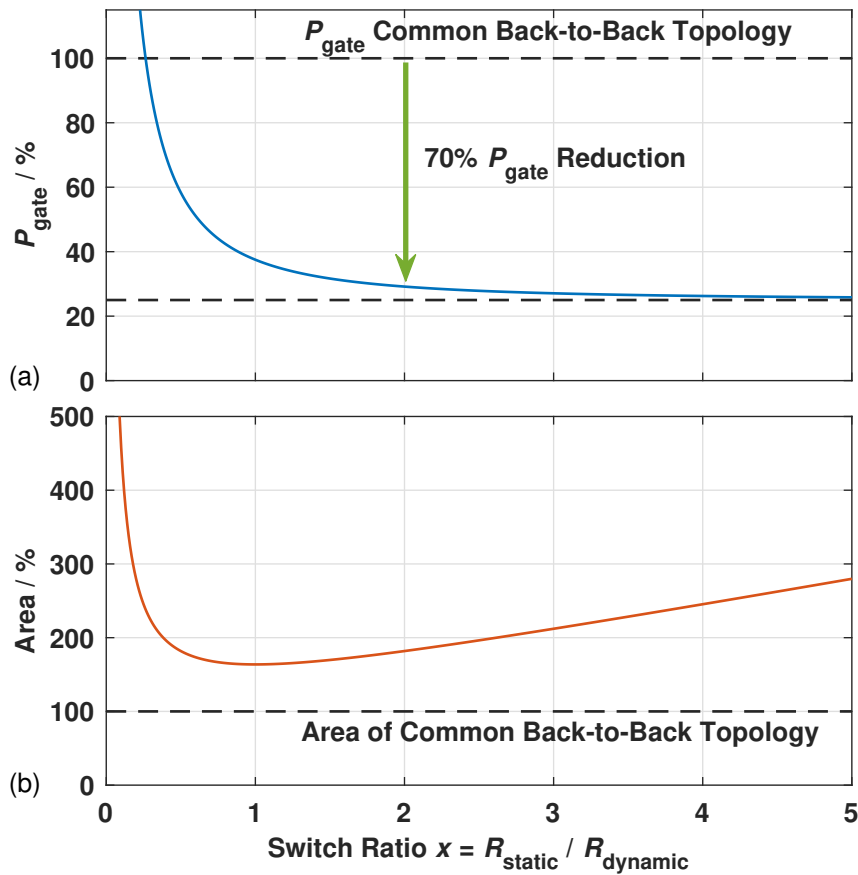


Fig. 4.16: Optimization trade-off between power loss and required area normalized to the standard back-to-back switch topology.

than $x = 3$ is not reasonable, since the P_{gate} is already at 27% and does not improve much afterwards. By increasing the static switch size, the required charge to turn on the switch increases and therefore also the charge pump output requirements. A good trade-off is a ratio around $x = 2$, where the area consumption increase of the transistors is around 80%. Since the area, which is occupied by all power switches of a SC converter, is less than 1% for a typical fully integrated SC converter [41], a ratio of $x = 2$ has a small impact on the total area consumption.

The proposed back-to-back switch topology and its control is depicted in Fig. 4.17. The voltage polarity (topology) and the switch control (CLK) signals are shifted by two level shifter to the logic block, which selects the corresponding switches. The respective switch states are shown in the table of Fig. 4.17.

The presented back-to-back switch topology has been implemented in a 0.35 μm high-voltage CMOS technology, Fig. 4.18. For the implementation a transistor ratio of $x = 2$ was chosen. In Fig. 4.18 the different circuit blocks are marked. The charge pump occupies the largest part of the area. The two level shifters have approximately the same area as the four back-to-back power transistors.

The total area consumption of the proposed topology without power transistors is approximately 67 000 μm^2 . Due to a careful layout (all four back-to-back switch within one isolation well), the theoretically 80% increase in area (see Fig. 4.16) could be reduced down to around 40% for the implemented four back-to-back switches in this work. Although the standard back-to-back switch topology (Fig. 4.14(d)) does not require any additional circuit blocks an increased area requirement of the standard solution is caused by the charge pump. This is due to the fourfold gate charge requirement compared to the proposed topology. Since the area of the charge pump is mainly determined by the size of the capacitors C_p and C_s (see Section 4.2), the area requirement increases by a factor of about four. This has a significant impact on the total area consumption. Thus the area consumption of the proposed topology with the additional circuits is reduced by up to 65% compared to the standard topology.

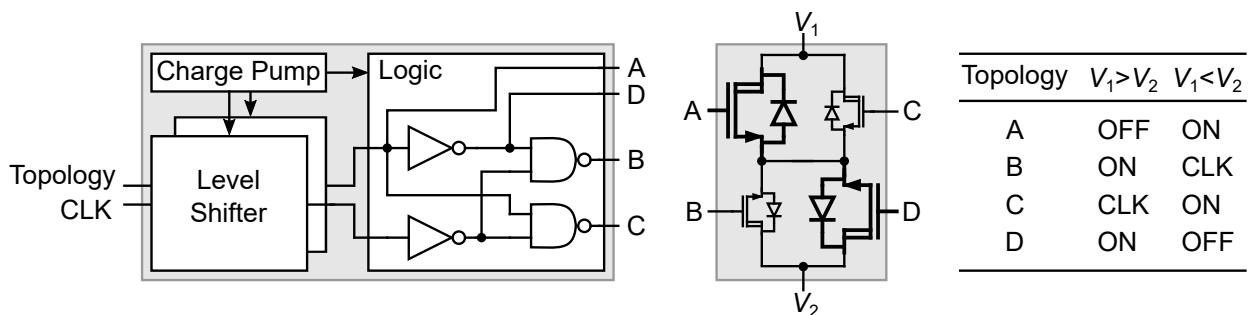


Fig. 4.17: Circuit block diagram of the proposed back-to-back switch topology, including the switch state table.

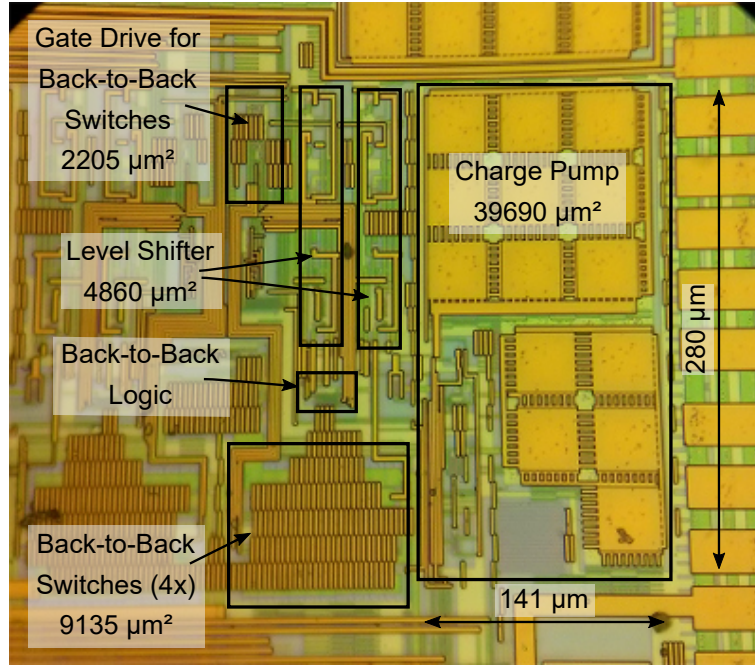


Fig. 4.18: Photograph of the proposed loss optimized back-to-back switch topology.

4.4 Bottom-Plate Loss Optimization

As outlined in Section 2.3.2, integrated capacitors build a parasitic capacitance (C_{bp} and C_{tp}) between the plates of the capacitor and the substrate. The resulting charge losses $P_{C_{bp}}$ can be derived as given in (2.19). The parasitic bottom-plate capacitance and the voltage swing of this capacitance are the most important factors, whereas the latter scale quadratically. The factor α depends on the used capacitor type and the technology. Figure 4.19 shows the peak efficiency of the 2:1 SC converter shown in Fig. 2.3 with an input voltage $V_{in} = 10\text{ V}–12\text{ V}$, $V_{out} = 5\text{ V}$, $P_{out} = 10\text{ mW}$, $C_{fly} = C_1 = 1.6\text{ nF}$ and $\Delta V_{bp} = 5\text{ V}$. The theoretically possible maximum peak efficiency considering the losses $P_{C_{bp}}$ is depicted. If MOS capacitors with $\alpha = 5\%$ are used for this SC converter, where α is the technology dependent factor between the parasitic bottom-plate capacitance and the main capacitance, the resulting losses would significantly reduce the efficiency of the converter by almost 10%. If the same converter operates with a higher input voltage, such that the voltage swing corresponds to $\Delta V_{bp} = 7.5\text{ V}$ or even 10 V , the losses would already reduce the efficiency by around 18% and around 28%, respectively. Therefore, a lot of effort and different concepts are introduced to reduce the parasitic bottom-plate losses [21, 33, 35, 39, 88, 129–131]. Especially for converters with high input voltages, C_{bp} and consequently α must be as low as possible in order to reduce this significant losses.

A common method to reduce the C_{bp} of MOS capacitors, which are typically used in low-voltage SC converters, is shown in Fig. 4.20(a). For PMOS capacitors, the isolation n-well is connected such that a series connection of the channel capacitance C_{cn} and C_{n-well} result for C_{bp} as shown in the equivalent circuit dia-

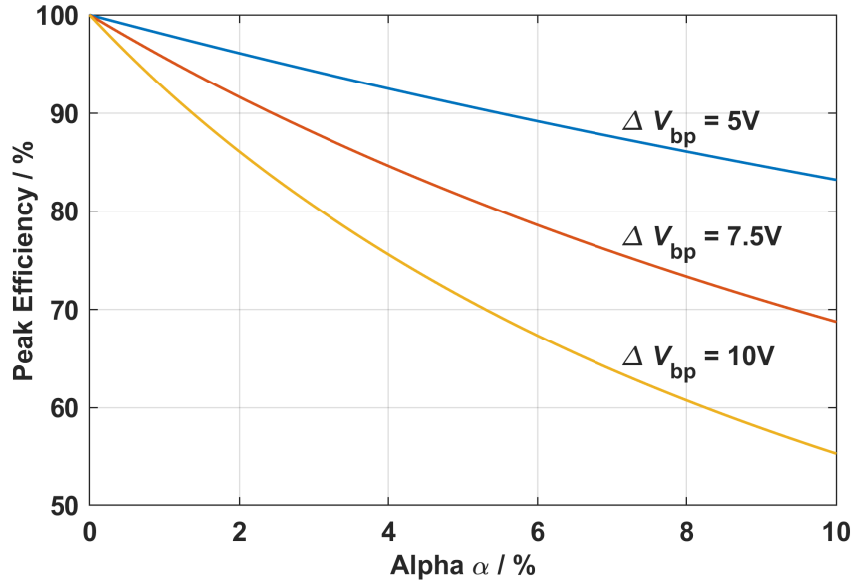


Fig. 4.19: Efficiency comparison for rising α and different voltage swings at the bottom-plate capacitance ΔV_{bp} of a 2:1 SC converter with $V_{in} = 10\text{ V} - 12\text{ V}$, $V_{out} = 5\text{ V}$ and $P_{out} = 10\text{ mW}$.

gram. The capacitance value of $C_{n\text{-well}}$ can be influenced by biasing the n-well with V_{bias} . The capacitance value of $C_{n\text{-well}}$ and C_{cn} decreases with rising V_{bias} . There are two ways to bias this n-well. The n-well can be directly biased as indicated by configuration (1). By biasing the n-well with a high voltage V_{bias} the capacitance value of C_{cn} is reduced [21]. By connecting the n-well directly to V_{bias} the series connection with $C_{n\text{-well}}$ becomes useless and therefore α does not further reduce. But this configuration avoids coupling currents into the substrate. A further concept introduced in [130] makes use of C_{cn} and connects (1) directly to the top plate (G) in a way that C_{gate} and C_{cn} are parallel. This solution is technology dependent and is only beneficial if the value of C_{cn} is a few times greater compared to $C_{n\text{-well}}$. In option (2) the n-well is biased by a high-impedance resistor with V_{bias} . The higher V_{bias} the smaller the voltage dependent capacitance value of $C_{n\text{-well}}$ and consequently C_{bp} gets smaller [39, 131]. The high-impedance resistor can also be realized in low-voltage SC converters with small voltage swings by a PMOS pseudo resistance [79]. It benefits from the compact high-impedance solution but V_{bias} is reduced by a diode voltage drop. However, for the sizing of the biasing resistance R_{bias} it is important that the RC time constant resulting from R_{bias} and $C_{n\text{-well}}$ is much longer than the half of the switching period of the SC converter. This prevents recharging losses of $C_{n\text{-well}}$. The trade-off is between area consumption and high-impedance biasing.

In this work, the n-well biasing technique option (2) is applied to MIM and MOM capacitors. Due to their higher dielectric strength, these capacitors are usually used in high-voltage SC converters. Despite the fact that α for MIM and MOM capacitors are approximately $\alpha = 1\%$ or less, the losses P_{Cbp} are significant with increasing voltage. For an input voltage of $V_{in} = 20\text{ V}$, which corresponds to a voltage swing of $\Delta V_{bp} = 10\text{ V}$, the converter efficiency is significantly reduced by about 7.5% (see Fig. 4.19). By inserting an n-well under

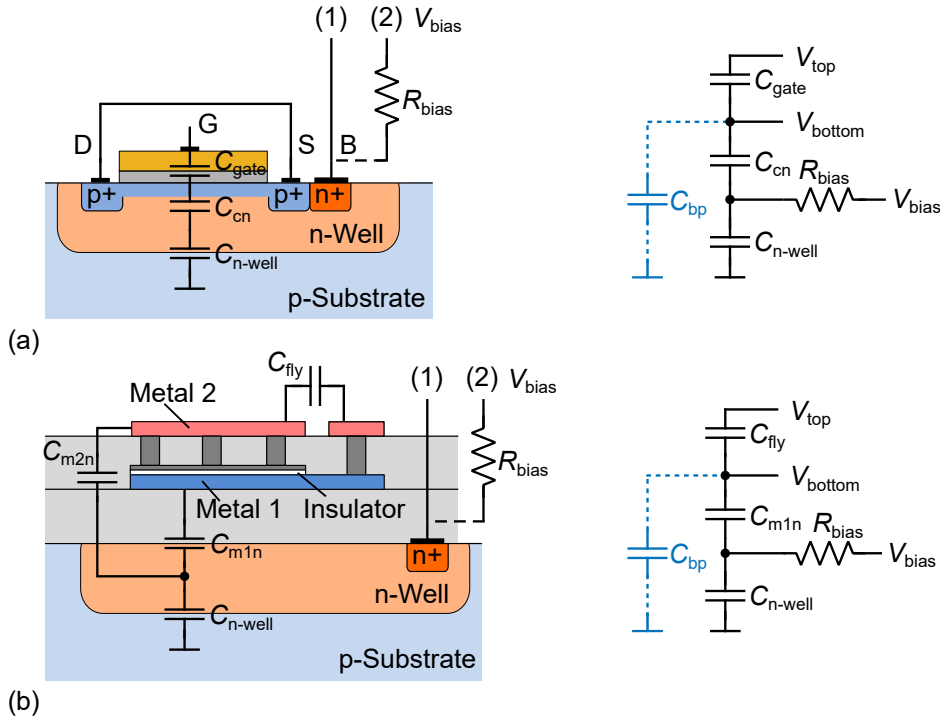


Fig. 4.20: Cross-section and equivalent circuit for bottom-plate loss optimization approaches for (a) MOS capacitors and (b) MIM capacitors.

a MOM capacitance or as shown in Fig. 4.20(b) under a MIM capacitor, the illustrated equivalent circuit diagram is obtained. By connecting C_{m1n} and C_{n-well} in series, the effective substrate capacitance C_{bp} can be reduced. The voltage dependence of C_{n-well} on the biasing voltage V_{bias} is shown in Fig. 4.21(a). For the 2:1 SC converter assumed from Fig. 4.19, a reduction of C_{n-well} by a factor of approximately 4.5 for a bias voltage $V_{bias} = 10$ V results. Figure 4.21(b) shows α for C_{bp} as introduced in Fig. 4.20(b) (MIM cap with $\alpha = 1\%$). Due to the series connection and a biasing voltage of $V_{bias} = 10$ V, α is reduced down to $\alpha = 0.5\%$, which is a reduction by a factor of two. This results in a significant improvement of the peak efficiency from 92.5% to over 96% for the SC converter in Fig. 4.19 for $V_{in} = 20$ and $\Delta V_{bp} = 10$ V. For high-voltage SC converters only option (2) with a high impedance resistor R_{bias} is reasonable to avoid high bottom-plate losses, since the PMOS pseudo resistance only works properly for small voltage swings ΔV_{bp} . In the chip photograph of the implemented charge pump in Fig. 4.12, which uses MIM capacitors, the marked resistor $R_{bias} = 10$ M Ω biases the n-well underneath the capacitors C_s and C_p with a value of around $C_{n-well} = 0.2$ pF. At a switching frequency $f_{sw} = 1$ MHz this leads to an approximately 25 times longer RC time constant, which sufficiently minimizes the charging losses in C_{n-well} .

C_{tp} is typically much smaller than C_{bp} (Section 2.3.2) and it also contributes to the charge flow towards the output. Intrinsic charge recycling discussed in [132] can further increase efficiency by flipping the connections of the capacitor. The physical bottom plate will be connected to the SC converters top plate

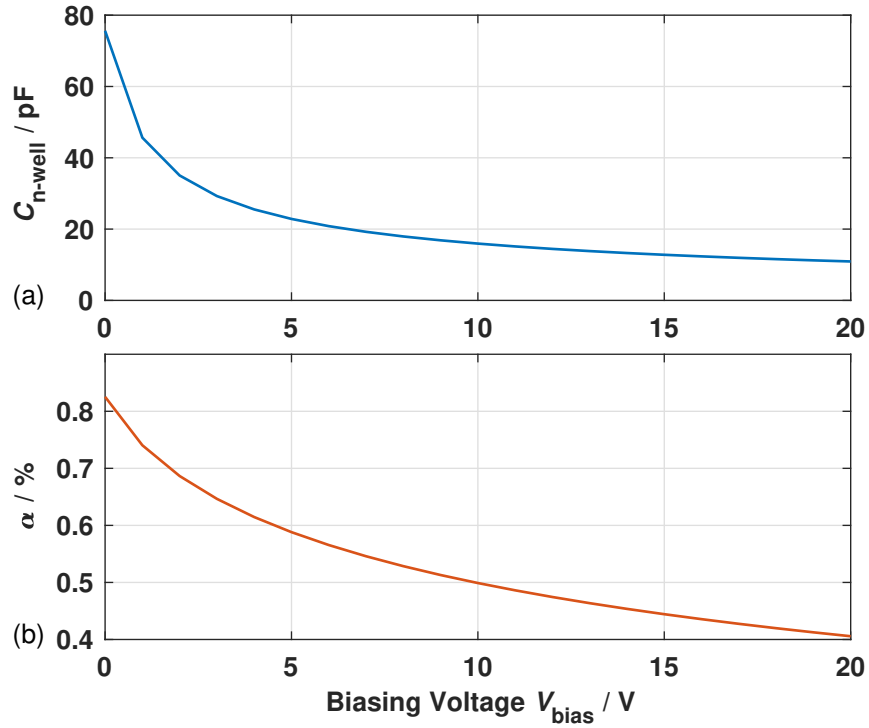


Fig. 4.21: (a) Voltage-dependent capacitance curve of $C_{\text{n-well}}$ and (b) voltage-dependent curve of α for the 2:1 SC converter of Fig. 4.19.

connection and vice versa, as indicated in Fig. 5.2 for the flying capacitors $C_{\text{fly}1}$ to $C_{\text{fly}4}$. The intrinsic charge recycling method and the n-well biasing concept are applied in the SC converters in this work in Chapters 5 and 6.

5 A Fully Integrated High-Vin Switched-Capacitor Converter

This chapter describes the sizing, implementation and measurement results of the recursive buck-boost SC converter for a high and wide input voltage range. Sections 5.1 and 5.2 explain the system architecture and the power stage transistor implementation for the integrated SC converter introduced in Section 3.4.1. The buck-boost selector required for buck and boost mode is explained in Section 5.3. The integrated control of the high-voltage SC converter is described in Section 5.4. In Section 5.5 the design aspects and the choice of the optimal operating point follow. The effect of parasitic bipolar structures is described in Section 5.6. Section 5.7 presents the measurement results. Section 5.8 compares the converter to the state of the art.

5.1 System Architecture

The system architecture of the presented recursive buck-boost SC converter is shown in Fig. 5.1. It consists of two main blocks, the control block and the block with the high-voltage circuits. The power stage within the high-voltage circuit block comprises four series-parallel 2:1 SC converter cells, as introduced in Section 2.2. The power switches of these 2:1 cells are controlled by the high-voltage supporting circuits. These include the circuits described in Chapter 4, i.e. level shifter, charge pump and driver. The buck-boost selector allows to configure the power stage to form either a buck or a boost converter.

The control block comprises two main parts. The V_{out} -Regulator generates and regulates the clock signal CLK depending on the output voltage V_{out} and forms the frequency control loop (refer to frequency modulation control Section 2.6). The conversion ratio is set by the Ratio Controller. For evaluation purposes a test interface was implemented in this design, which allows for setting the conversion ratio externally. The control signals for the high-voltage circuits are generated by the pulse generation and switch controller.

A shunt regulator ensures a smooth start-up from V_{in} and supplies all blocks until V_{out} is available. After the start-up, the blocks are powered by V_{out} to increase efficiency. A low-power optimized design of all imple-

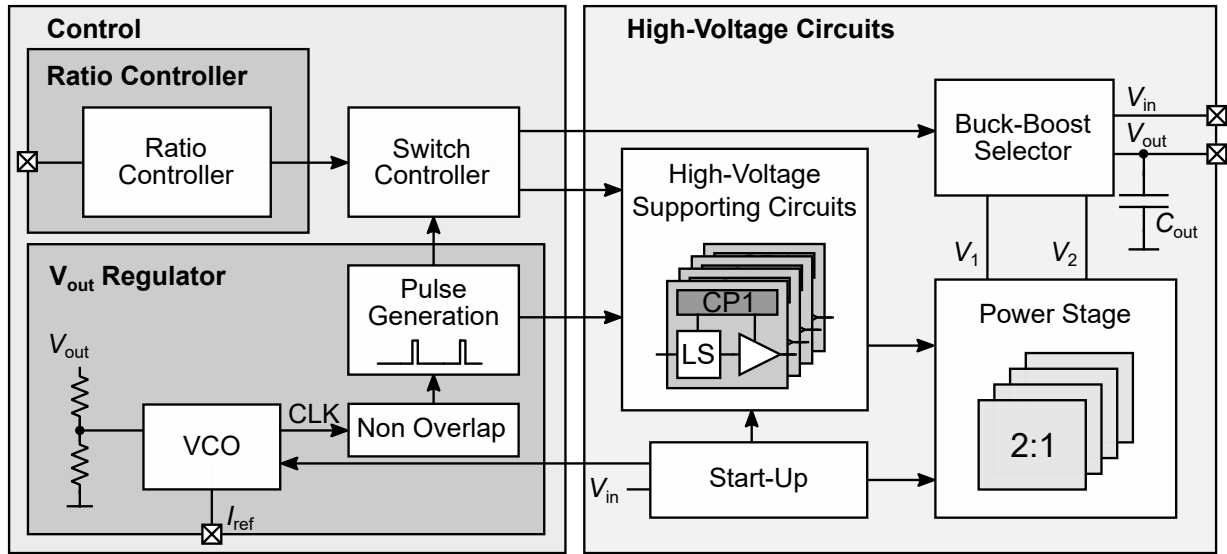


Fig. 5.1: System-architecture block diagram of the recursive buck-boost SC converter.

mented blocks is crucial to achieve a high overall system efficiency. In the following, the implementation of the individual blocks and circuits is described.

5.2 Power Stage and Supporting Circuits

Figure 5.2 depicts the transistor implementation of the power stage. This figure shows the implementation of the four 2:1 cells, cell 1 to cell 4. There are two input/output pins, V_1 and V_2 . For the buck mode the pin V_1 serves as input and pin V_2 as output. For the boost mode, vice versa, V_2 serves as input and V_1 as output. The following description always refers to the buck mode, but it can be applied to the boost mode as well. There are three different cell types. The basic series-parallel 2:1 cell, with four power switches is used in cell 1. This cell has one input terminal V_1 and one output terminal V_{mid1} . The cell type of cell 2 and cell 3 is extended by two power switches, which build an additional input terminal for these cells. This additional input allows to choose either V_{in} or the output of the prior cell as an input. The third cell type (cell 4) is further extended by an additional input, which allows to choose V_{in} or any output of the other cells as input. The switches outside of the cells are topology switches, which control the cell configuration for the different ratios. Due to the high input voltage all used power transistors are realized as 20 V DMOS devices with a 5 V gate oxide. The topology switches are turned on or off depending on the ratio and do not switch with the clock frequency (CLK). Due to the reconfigurability, several switches have to be bidirectional switches. The bidirectional topology switches, are realized by a standard back-to-back switch configuration, since these switches are turned on or off only if the ratio change. The bidirectional switches within the cells, which turn on/off with ϕ_1/ϕ_2 , are replaced by the proposed loss and area optimized back-to-back switch

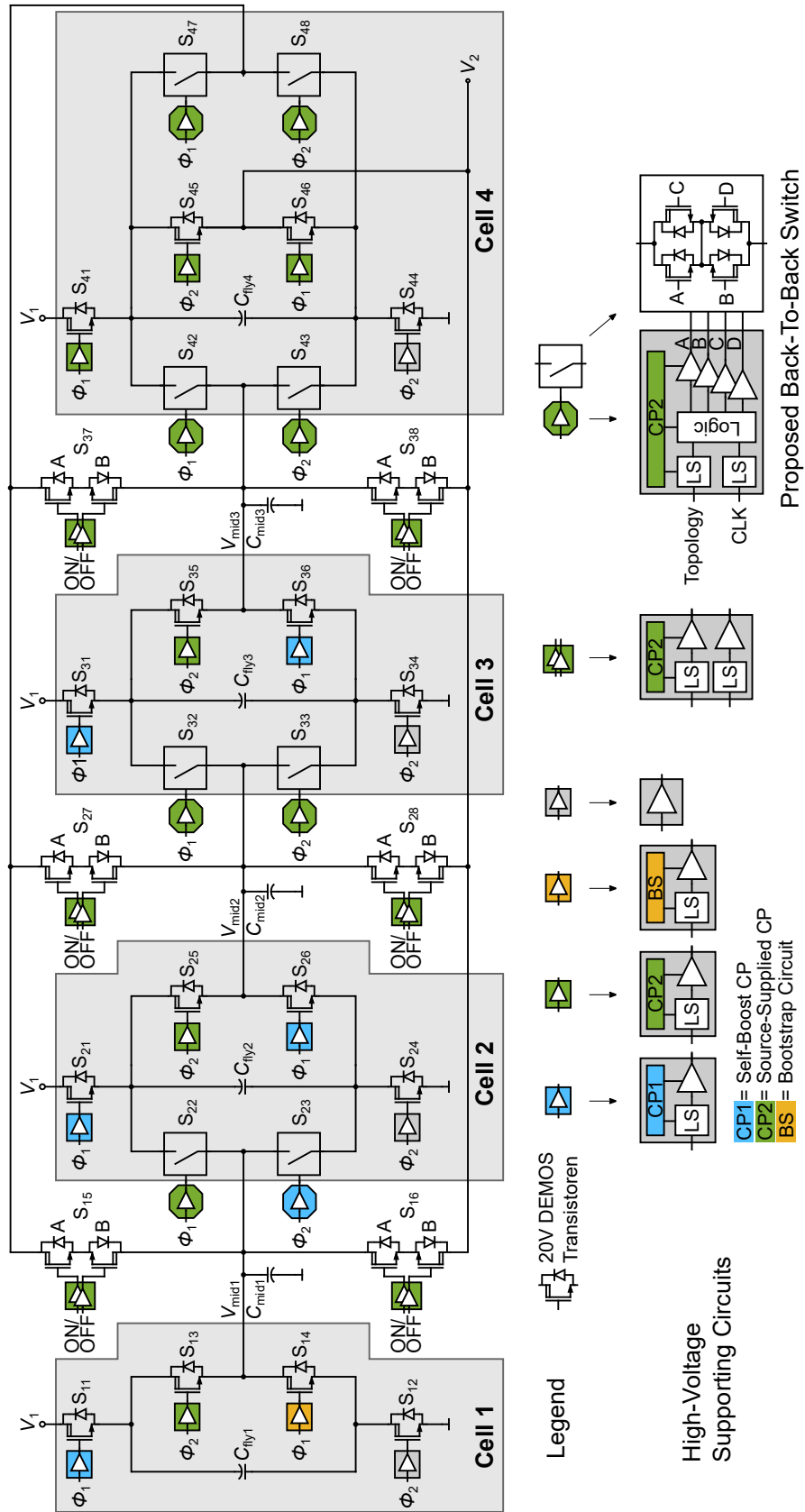


Fig. 5.2: Power stage implementation of the recursive buck-boost SC converter.

topology, introduced in Section 4.3. Each power switch needs a high-voltage supporting circuit including a level shifter, a driver and a floating high-side supply, except for switches S_{12} , S_{24} , S_{34} and S_{44} . These switches are low-side switches, which can be controlled directly with a driver. The different high-voltage circuits are depicted in the lower part of Fig. 5.2. They differ by the floating high-side supply, which can be realized as a bootstrap circuit, a self-boost charge pump or a source-supplied charge pump depending on the source voltage condition of the power transistor, as described in Section 4.2. The pulsed resistive level shifter from Section 4.1 was used in all supporting circuits. The high-voltage supporting circuits for the standard back-to-back switch consist of two level shifters and two drivers. The proposed back-to-back switch, is also depicted in Fig. 5.2. As described in Section 4.3, two level shifters, a logic block, four drivers and one of the three floating high-side supplies, are required. A detailed description of the power transistor control signals for the different ratios is presented in Appendix A. The cell configurations and the resulting switch conditions for the ratios 1/4 to 15/16 and 16/15 to 4/1 respectively are visualized in Fig. A.1 to Fig. A.12.

5.2.1 Capacitor Implementation

There are two main types of capacitors within the power stage of Fig. 5.2, the flying capacitors C_{fly1} to C_{fly4} and the buffer capacitors C_{mid1} to C_{mid3} . The flying capacitors are responsible for the charge transfer from V_{in} to V_{out} , while the buffer capacitors store the charge during conversion. These buffer capacitors are required, since the implemented 2:1 cells deliver charge to the output in both phases, but source charge only in one phase from the input. Depending on the configuration of the four cells, in some ratios cell 1 to cell 3 work as source for another cell and hence the outputs of these cells are buffered by C_{mid1} to C_{mid3} . However, cell 4 is always connected to V_{out} , therefore this cell is buffered by C_{out} .

For the four flying capacitors C_{fly1} to C_{fly4} a low value of α is important due to the high-voltage swings on their bottom plate. In addition, for area minimization, the capacitance density should be as high as possible. In the used 0.35 μm high-voltage CMOS technology only MOS, MOM and MIM capacitors are available (see Section 2.4). Since the maximum voltage of the flying capacitors exceeds 5 V, only the MIM capacitor is suitable with a breakdown voltage of 10 V. It achieves a low parasitic bottom-plate capacitance of $\alpha = 1\%$. The density of the MIM capacitor is 0.7 fF/ μm^2 . The buffer capacitors C_{mid1} to C_{mid3} and also C_{out} refer to ground. Therefore, the parasitic bottom-plate capacitance causes no losses and only the breakdown voltage and the density of the capacitor type is important. The MOS capacitor achieves the highest capacitor density in the used technology of 1.2 fF/ μm^2 . With a breakdown voltage of 5 V it is used for C_{out} . C_{mid1} , C_{mid2} and C_{mid3} need voltage ratings of >5 V. Therefore, MIM capacitors are implemented in this design.

In order to minimize the parasitic bottom-plate capacitance at the flying capacitors $C_{\text{fly}1}$ to $C_{\text{fly}4}$, the proposed bottom-plate loss optimization method of Section 4.4 for reducing the parasitic bottom-plate capacitance is utilized. Also the discussed intrinsic charge recycling by flipping the top-plate and bottom-plate contacts, were applied.

5.3 Buck-Boost Selector

The buck-boost selector, shown in Fig. 5.3, connects the terminals V_{in} , V_{out} and V_1 , V_2 depending on the active mode of the SC converter, either buck or boost mode. V_1 and V_2 correspond to the terminals of the power stage as shown in Fig. 5.2. The buck mode is active for Mode = 'high', in this case the terminals V_{in} and V_1 and V_{out} and V_2 are connected. For the Mode = 'low', the boost mode is active and the terminals V_{in} and V_2 and V_{out} and V_1 are connected. The power switches are controlled by the same high-voltage supporting circuits as used within the power stage. For all four switches the source-supplied charge pump with the level shifter and a driver is used. The power switch orientation is important to ensure a proper function of the buck-boost selector and to avoid cross-currents through the intrinsic body diodes. The implemented buck-boost selector also supports the start-up in buck mode due to the intrinsic body diodes. When the voltage at V_1 rises and becomes higher than the output voltage V_{out} , a current flows through the body diode to the output and charges the output capacitor.

5.4 Control

The control for multi-ratio SC converters is divided into two parts as explained in Section 2.6. In the block diagram of the recursive buck-boost SC converter (Fig. 5.1), the two parts of the control are shown. On one hand, the output voltage must be controlled as a function of the load. On the other hand, the conversion ratio must be set as a function of the input voltage V_{in} . The control of the output voltage V_{out} is realized by pulse-frequency modulation (PFM). It consists of a feedback voltage divider and a VCO, which generates

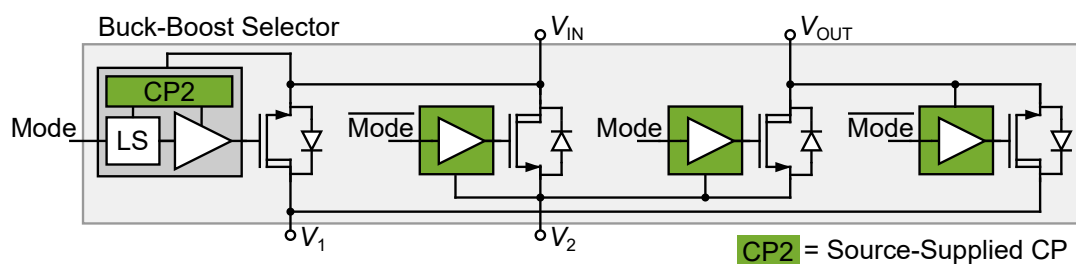


Fig. 5.3: Buck-Boost Selector.

the switching frequency as a function of the output voltage. The clock signal CLK is converted into a non-overlapping two phase clock and subsequently into control pulses for the switch controller and the high-voltage supporting circuits. When selecting the oscillator, the power consumption is crucial. A three-stage ring oscillator optimized for low power, as discussed in [133], is used.

As shown in Fig. 5.1, for measurement flexibility, an external ratio control interface has been implemented. This test interface is used to directly control the ratio controller, which drives the switch controller to activate the corresponding power switches depending on the selected ratio. One of the control techniques described in Section 5.4 could be used to control the conversion ratio.

The measurement results in Fig. 5.4 show a load step from 0.9 mA to 0.4 mA and back to 0.9 mA. The VCO changes the switching frequency from 1 MHz to 430 kHz and back to 1 MHz to adjust the output resistance R_{out} . This keeps the output voltage V_{out} constant at 3.3 V.

5.5 Design Aspects and Optimum Operating Point

5.5.1 Capacitor Sizing

The optimal distribution of the total capacitance value to the individual capacitors is a main challenge during the development of a multi-ratio SC converter. Due to the different ratios, the load currents at the individual capacitors change. As a result, an optimal allocation of the total capacitance value looks different for each ratio. For low-voltage converters as in [7], the capacitance distribution can be optimally adjusted for each ratio separately (dynamic sizing), since the additional cost of the required extra switches is low. For the high-voltage SC converter, however, effort, area requirements and losses increase due to high-voltage switches, level shifters and floating high-side supplies. A fixed distribution of the total capacitance to the capacitors C_{fly1} to C_{fly4} optimized to the overall conversion ratios is the goal. For the selected recursive 4-bit SC converter approach, the optimal distribution of the total capacitance to C_{fly1} to C_{fly4} corresponds to the charge flow analysis (described in Section 2.3.1) for the conversion ratio $x/16$. The total value of the flying capacitance $C_{fly,total}$ is divided between C_{fly1} to C_{fly4} as follows:

$$C_{fly1} = \frac{1}{15} \cdot C_{fly,total} \quad (5.1)$$

$$C_{fly2} = \frac{2}{15} \cdot C_{fly,total} \quad (5.2)$$

$$C_{fly3} = \frac{4}{15} \cdot C_{fly,total} \quad (5.3)$$

$$C_{fly4} = \frac{8}{15} \cdot C_{fly,total} \quad (5.4)$$

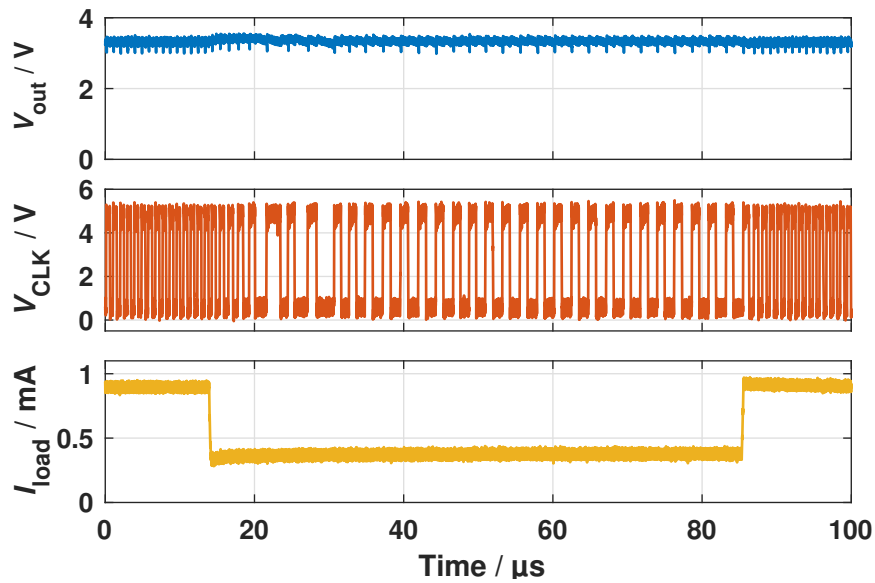


Fig. 5.4: Transient measurements of the signals V_{out} , CLK and I_{load} for a load step of 0.5 mA.

To realize the ratios $x/8$ the capacitors C_{fly3} and C_{fly4} are connected in parallel (recursive approach). The same applies for the ratios $x/4$, where C_{fly1} and C_{fly2} , and C_{fly3} and C_{fly4} are connected in parallel. For the ratio $1/2$ C_{fly1} to C_{fly4} are connected in parallel. The selected fixed sizing achieves only minor deviations in efficiency over the entire working range compared to the optimized dynamic sizing for each conversion ratio as shown in Fig. 5.5. Due to the fixed sizing, an improvement of the efficiency is partly achieved, this is due to the reduced capacitance value of cell 1 and cell 2, which at the same time have the highest voltage swing. This reduces the bottom-plate losses as described in 3.2 and, hence, a higher efficiency is achieved. When sizing the buffer capacitors C_{mid1} to C_{mid3} , it turned out that sizing according to the charge

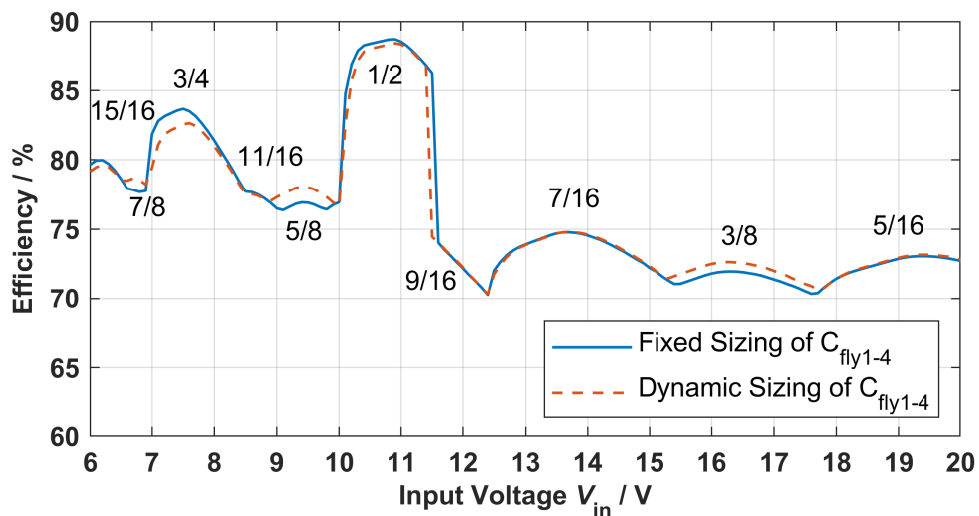


Fig. 5.5: Scaling approaches of the flying capacitor C_{fly1} to C_{fly4} .

flow analysis is not suitable, since C_{mid1} and C_{mid2} must buffer different currents. Investigations revealed that the following sizing of C_{mid1} , C_{mid2} and C_{mid3} show the best performance:

$$C_{\text{mid1}} = C_{\text{mid2}} = C_{\text{mid3}} = \frac{3}{15} \cdot C_{\text{fly,total}}. \quad (5.5)$$

5.5.2 Power Switch Sizing

The power switches are sized as described in section 3.2. Depending on the parameters resulting from the charge flow analysis of Section 2.3 and the corresponding weighting resulting from the equations (3.10) and (3.11), the power switch on-resistance R_i can be determined using (3.12). As the charge, that flows from cell 1 to cell 4 increases, the power switches also increase in area and decrease in on-resistance. This results in a similar scaling of the on-resistance of the power switches compared to the sizing of the flying capacitors. The on-resistance of the power switches for the first cell (cell 1) is 480 Ω . The on-resistance of the power transistors for cell 2, cell 3 and cell 4 is 240 Ω , 120 Ω and 60 Ω , respectively.

5.5.3 Optimum Operating Point

The selection of the switching frequency has a great influence on all loss mechanisms in a SC converter as shown in the fundamentals (Section 2.3). In Fig. 5.6(a) the frequency dependent losses are shown over the switching frequency exemplarily for the ratio 5/16, which is one of the most lossy conversion ratios. The losses can be divided into intrinsic losses P_{Rout} and extrinsic losses P_{Rp} like introduced in Section 2.3. The losses P_{Rout} decrease with the switching frequency. The extrinsic losses like bottom-plate losses P_{Cbp} , P_{well} and $P_{\text{sw,ctrl}}$, which includes the gate losses P_{gate} , the level shifter losses P_{LS} , charge pump losses P_{LS} and the gate driver losses P_{GD} , scale up with increasing switching frequency. The losses P_{well} are small and can therefore be neglected. For the selected sizing a minimum of the total losses results at an optimal switching frequency of 2 MHz. When selecting the switching frequency f_{sw} , it is essential that f_{sw} is located in the target area as indicated in Fig. 2.5. This allows to control the output resistance R_{out} and consequently the output voltage V_{out} by varying the switching frequency. Figure 5.6(b) shows the total losses and their breakdown for the ratios 5/16 to 15/16 for $f_{\text{sw}} = 2$ MHz. These conversion ratios cover the entire input voltage range from 6 V to 20 V. Considering the losses at the output resistance P_{Rout} , it can be observed that the losses for the ratios $x/8$ and $x/16$ are equal. This results from the charge flow analysis of the R_{out} . In contrast, the extrinsic losses P_{Cbp} , $P_{\text{sw,ctrl}}$ and P_{well} are voltage-dependent, so these losses decrease with decreasing ratio from 5/16 to 15/16, since the input voltage decreases. This is due to the reduced voltage swings at the parasitic bottom-plate capacitors and voltage-dependent losses, which occur for instance in the level shifter.

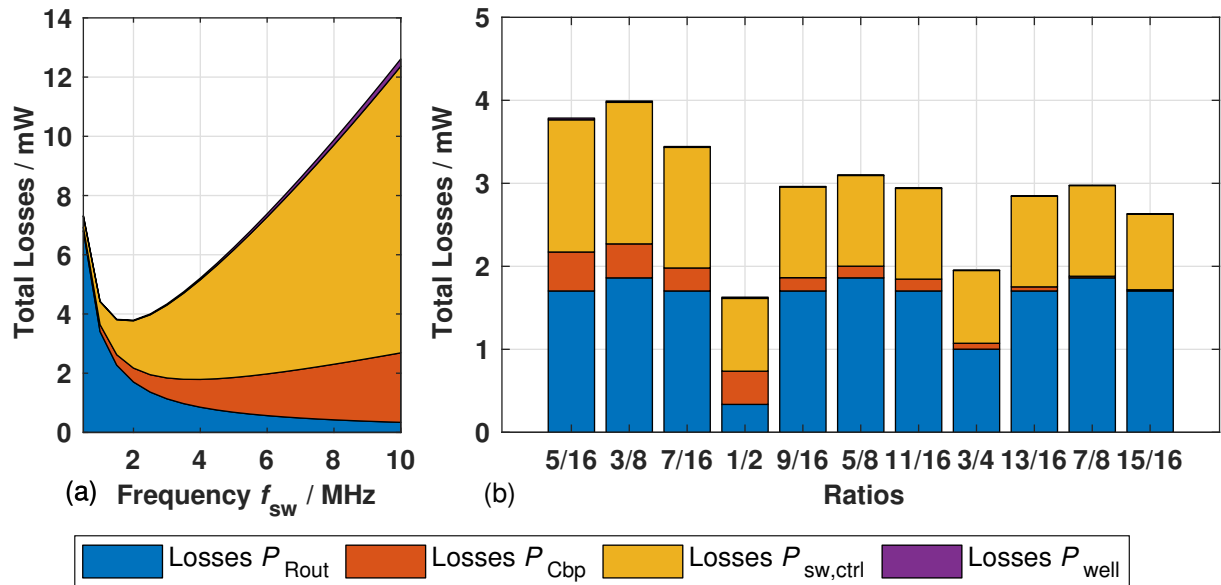


Fig. 5.6: Loss-break down (a) for the ratio 5/16 over the switching frequency and (b) for the ratios 5/16 to 15/16 for a switching frequency of 2 MHz.

The loss breakdown in Fig. 5.6 shows that for converters with high V_{in} the $P_{sw,ctrl}$ losses together with the P_{Rout} make up the largest part. This confirms that for high-voltage SC converters methods like time interleaving or charge recycling as proposed in [28, 38, 79, 134] cannot be realized efficiently due to the large number of high-voltage switches with high $P_{sw,ctrl}$ losses and control overhead.

In Fig. 5.7 the efficiency of the different ratios over input voltage and output power is plotted. For small output power $P_{out} < 5$ mW the efficiency η is very low. This is due to the losses $P_{sw,ctrl}$ and P_{Cbp} , which have a significant influence. The black area at about $V_{in} = 5$ V is not considered in this figure, by implementing the conversion ratio 1:1 this area can be covered. At a very high output power P_{out} and, consequently, high output current I_{out} , the voltage drop and power dissipation P_{Rout} at the output resistance R_{out} increases. This results in a larger drop of the output voltage V_{out} , whereby the individual voltage conversion ratios VCR cannot be used optimally. This is visible in Fig. 5.7 for high output power, especially in the range $V_{in} = 14 - 20$ V. The highest efficiency for the input voltage range is achieved at the selected optimum operating point at around $P_{out} = 10$ mW. By further increasing the output power P_{out} and thus the output current I_{out} , the ripple ΔV_{out} of the output voltage V_{out} also increases and exceeds the specified value. For the optimal operating point the values for $C_{fly1} = 100$ pF to $C_{fly4} = 800$ pF and for the buffer capacitors according to $C_{mid1} = C_{mid2} = C_{mid3} = 300$ pF are derived.

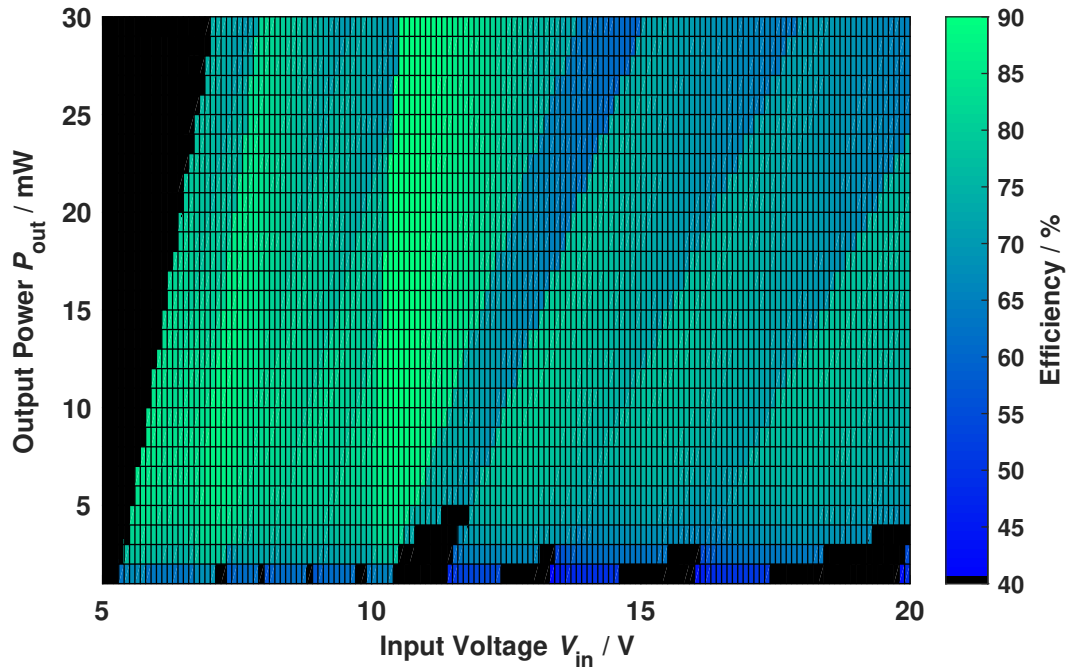


Fig. 5.7: SC converter efficiency in buck mode as a function of input voltage and output power.

5.6 Parasitic Bipolar PNP-Structure

In this section, a parasitic effect is investigated that may strongly affect efficiency. It occurs in high-voltage CMOS technologies that do not use a n-buried layer. This effect is not modeled in many technologies.

In Fig. 5.8(a) the first 2:1 SC converter cell of the presented recursive buck-boost SC converter from Fig. 5.2 is shown. This cell consists of four high-voltage DMOS transistors. In Fig. 5.8(a) the charge flow of the first phase ϕ_1 is depicted. The charge of transistor S_{14} flows in the direction of the body diode. The orientation of S_{14} is derived from the voltage levels at V_{mid1} and V_{Cbp} , so that S_{14} blocks during the phase ϕ_2 . The charge flow in ϕ_1 , respectively the series connection of the capacitors C_{fly1} and C_{mid1} , results in a voltage drop over the source-drain path $V_{S_{14},SD}$ of the transistor S_{14} , as shown in Fig. 5.8(b). The peak value of $V_{S_{14},SD}$ depends on the voltage ripple at the capacitors. The size of the transistors only determines the charging duration. If this voltage drop exceeds the intrinsic body diode forward voltage (source-drain path), it becomes conductive. Consequently, the charge not only flows through the transistor channel, but a part of it also flows through the body diode. In combination with the p-doped substrate, this forms a parasitic bipolar pnp transistor structure [135]. This is shown in the cross-section in Fig. 5.8(c). The pn-junction between source and drain (body diode) forms the emitter-base path and the substrate drain diode the collector-base path. A base current (current through the body diode) results in a collector current of the parasitic pnp transistor into the substrate. The collector current depends on the current gain of the pnp transistor ($\beta = I_{collector}/I_{basis}$). This parasitic pnp transistor structure is not modeled in some technologies, including the

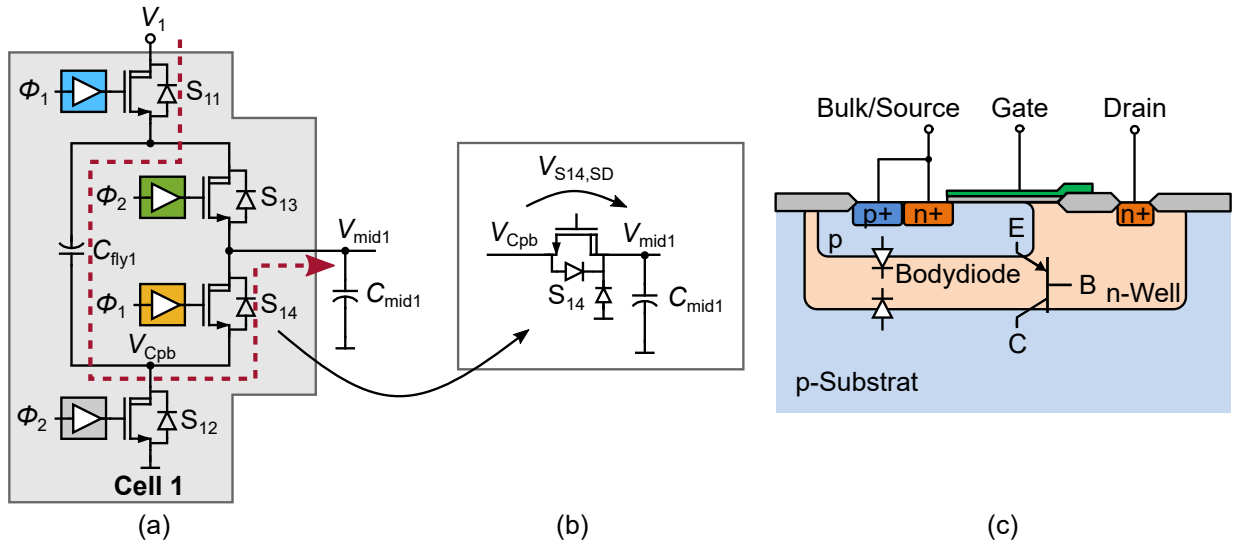


Fig. 5.8: Problem of the parasitic bipolar pnp transistor by means of (a) SC converter 2:1 cell, (b) switch S_{14} , and (c) cross-section of a DMOS.

technology used. The substrate currents causes losses that reduce the efficiency of a SC converters and can even lead to malfunction. This effect needs to be considered especially for fully integrated SC converters.

Figure 5.9 shows the measured voltage curves of V_{mid1} and V_{Cpb} . The source-drain voltage of the switch S_{14} $V_{S14,SD}$ reaches a peak value of approximately 0.4 V for this measurement and then decreases according to the discharge curve of a capacitance. The peak value of the measured substrate current is about 3-4 mA. This can be significantly higher depending on the conversion ratio. Since the voltage difference between

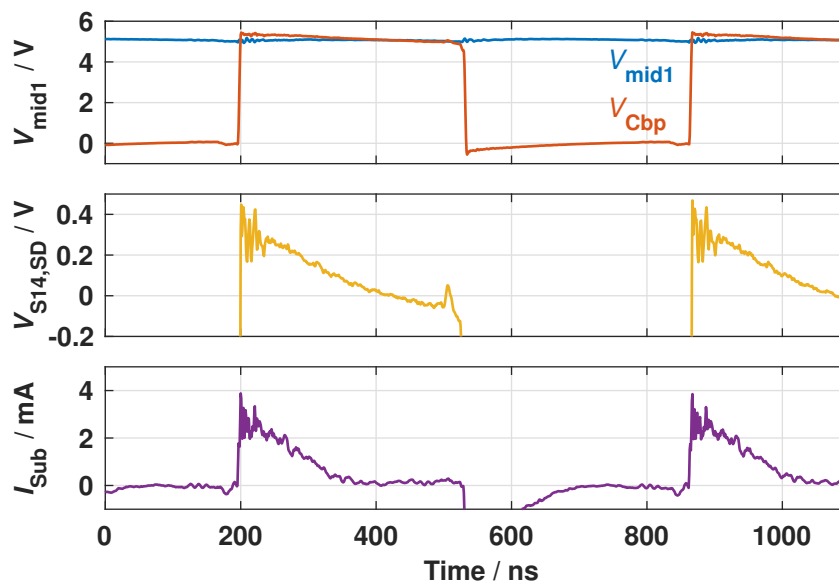


Fig. 5.9: Transient measurements of the voltage waveform V_{mid1} , V_{Cpb} and $V_{S14,SD}$ and the corresponding substrate current caused by the parasitic bipolar pnp transistor structure.

V_{Cbp} and V_{mid1} is load-dependent, the substrate current is also load-dependent. The losses are proportional to the drain voltage of S_{14} . The parasitic pnp transistor occurring in a CMOS technology can be made almost completely ineffective by an n-buried layer below the n-well. This layer is usually not available in low-cost CMOS technologies such as in the used technology. Alternatively, an SOI technology can be used, which prevents the parasitic bipolar effect by isolating the power switch, but comes at higher cost. From a circuit design perspective, switch-stacking with isolated low-voltage MOS transistors could also be a solution, depending on the application.

5.7 Experimental Results

The recursive buck-boost SC converter of Fig. 5.2 was manufactured in a $0.35\ \mu\text{m}$ high-voltage CMOS technology. Figure 5.10 shows the chip photograph of this converter with an active chip area of $6.8\ \text{mm}^2$. The picture indicates the area distribution of the flying capacitors C_{fly1} to C_{fly4} , buffer capacitors C_{mid1} to C_{mid3} , C_{out} , buck-boost selector, control and high-voltage supporting circuits. The enlarged section shows one power switch and the required supporting circuits consisting of level shifter, charge pump and gate driver. These circuits have been implemented 26 times, and the gate driver has been adapted to the size of the power switch. The high-voltage supporting circuits, power switches and control occupy about 38% of the active area compared to about 5% for a low-voltage design as described in Section 3.1.

Figure 5.11 shows the measured efficiency of the recursive buck-boost SC converter including all circuits except for the voltage controlled oscillator over the input voltage. For measurement reasons the clock signal was generated externally. The output power in buck mode is $6.5\ \text{mW}$ and in boost mode $1\ \text{mW}$ at an output voltage of $V_{out} = 5\ \text{V}$. For an input voltage of $V_{in} \leq 6\ \text{V}$ the SC converter works in boost mode (ratios 4/1 to 8/7) and for $V_{in} > 6\ \text{V}$ in buck mode (ratios 15/16 to 9/16). The parasitic effect described in Section 5.6

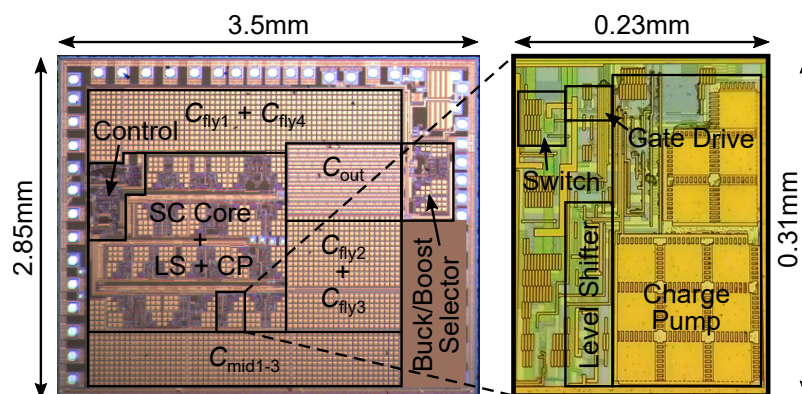


Fig. 5.10: Photograph of the recursive buck-boost SC converter and a detail section of one of the 26 power switches with the required high-voltage supporting circuits.

partially reduces efficiency by up to around 15%. As the input voltage increases, so do the emitter-collector voltage of the parasitic bipolar pnp transistor and the resulting losses (see Section 5.6). This results in decreasing efficiency with increasing voltages and depending on the given conversion ratio. The parasitic effect also limits the input voltage range from 2 V to 20 V to a still large input range from 2 V to 13 V. This wide input voltage range represents a factor of two improvement over the state of the art. The peak efficiency reaches 81.5% (ratio 1/2). The minimum efficiency in buck mode is 54.1%, while the maximum output power is 10 mW. In boost mode, the efficiency is lower compared to buck mode. This is mainly due to the high-voltage components, which are over-designed for boost mode and cause high losses. The maximum efficiency in boost mode is 70.9% and it decreases to 22.7% for a minimum input voltage of 2 V. The fine granular adjustment of the ratio is well visible. It can be noticed that some of the boost ratios differ from those in buck mode, which confirms the need for a large number of conversion ratios.

The Fig. 5.12(a) shows the measured efficiency over the output current in buck mode with a maximum output current of up to 4 mA at an output voltage of $V_{\text{out}} = 5$ V, corresponding to an output power of 20 mW. In boost mode, Fig. 5.12(b), a maximum I_{out} of 1.4 mA is reached at an input voltage of $V_{\text{in}} = 2.9$ V. Both diagrams confirm a high efficiency over a wide load range.

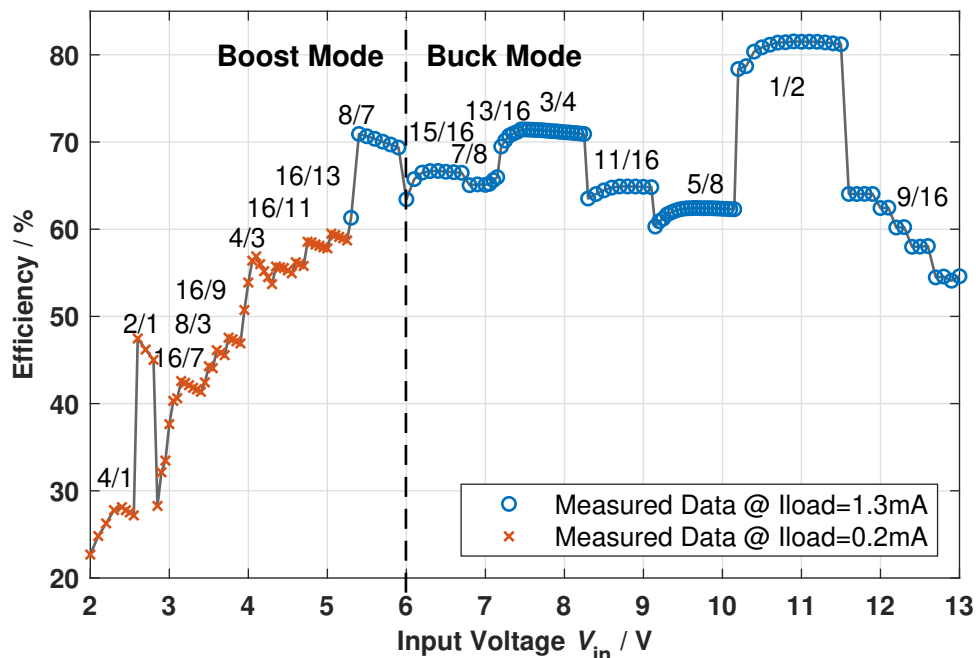


Fig. 5.11: Measured efficiency versus input voltage (V_{in}) and conversion ratio at $V_{\text{out}} = 5$ V, for $I_{\text{out}} = 1.3$ mA in buck mode and $I_{\text{out}} = 0.2$ mA in boost mode.

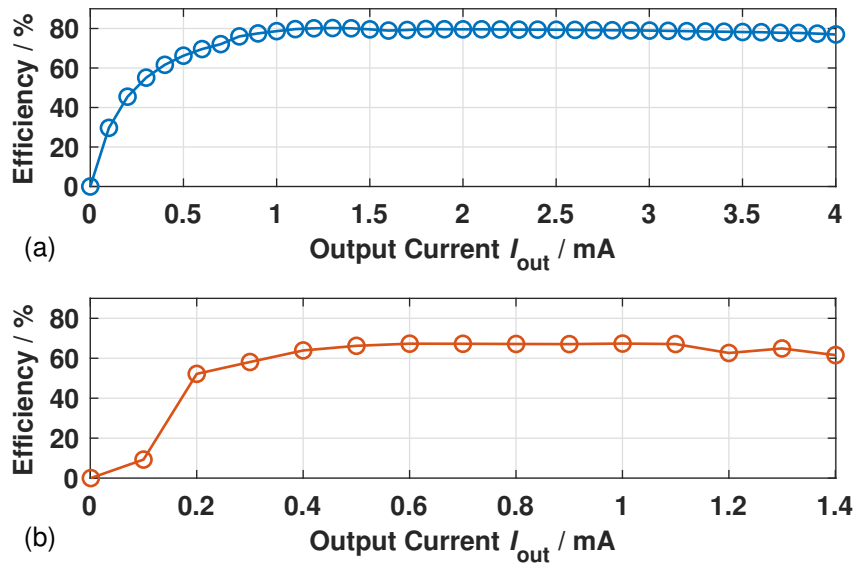


Fig. 5.12: Measured efficiency versus output current (I_{out}) (a) for buck mode operation in ratio 1/2 at $V_{in} = 10.7$ V and (b) for boost mode operation in ratio 2/1 at $V_{in} = 2.9$ V.

5.8 State-of-the-Art Comparison

Table 5.8 shows the state-of-the-art comparison for fully integrated SC converters. The SC converter in this work has the largest technology structure size, which is due to the high dielectric strength. This has a negative effect on the active area. The total capacitance of the SC converter of 3.64 nF is comparably low. [25] has the highest total capacitance of 15 nF. This has a positive effect on the output power and efficiency and is favored by the low input voltage of < 2.5 V and the small technology size of 65 nm. The presented recursive multi-ratio SC converter achieves the highest reported input voltage of 13 V. In addition, the 4-bit architecture in combination with the implemented buck and boost mode allows a wide-input voltage range starting from 2 V to 13 V. The fine granularity is realized by 8 buck and 9 boost ratios. The achieved peak efficiency of 81.5% is comparable or higher compared to the state of the art. Only [25] and [23] provide a higher peak efficiency, but their maximum input voltage is ≤ 2.5 V. The presented SC converter achieves an output power of 10 mW in buck mode with an active area of 6.8 mm².

In summary it can be stated that the presented recursive buck-boost SC converter exceeds the state of the art for fully integrated multi-ratio SC converters in the following areas. The maximum input voltage is increased from 8 V to 13 V. The converter also has the widest reported absolute input voltage range starting from 2 V to 13 V, which improves the state of the art by a factor of two. The peak efficiency of 81.5% is significantly higher than the state of the art for fully integrated SC converters with an input voltage of 5 V or higher.

Tab. 5.1: Performance comparison of fully integrated SC converter

| | Salem [23] ISSCC' 14 | Saraf. [42] ASSCC' 15 | Le [39] ISSCC' 13 | Jiang [25] ISSCC' 18 | Saadat [27] ASSCC' 15 | Hua [34] CICC' 15 | This work [41] ISSCC' 16 |
|------------------|--------------------------------|---------------------------------|-----------------------------|--------------------------------|---------------------------------|-----------------------------|------------------------------------|
| Technology | 250 nm | 90 nm | 65 nm | 65 nm | 250 nm | 65 nm | 350 nm |
| Buck-Boost | no | no | no | yes | yes | yes | yes |
| Number of ratio | 15 | 8 | 2 | 24 | 8 | 6 | 17 |
| Total cap amount | 3 nF | 6 nF* | 3.88 nF | 15 nF | 5.8 nF* | N/A | 3.64 nF |
| Input voltage | 2.5 V | 2.5-8 V | 3-4 V | 0.22-2.4 V | 0.6-2.4 V | 0.5-3.3 V | 2-13 V |
| Output voltage | 0.1-2.18 V | 1.2 V | 1 V | 0.85-1.2 V | 1.2-1.5 V | 1 V | 5 V |
| Efficiency(peak) | 85% | 75% | 74.3% | 84.1% | 76% | 70.4% | 81.5% |
| Output power | 4.4 mW* | 20 mW | 122 mW* | 96 mW* | 0.15 mW* | 0.003 mW* | 10 mW |
| Active area | 4.65 mm ² | 1.5 mm ² * | 0.64 mm ² | 2.4 mm ² | 1.95 mm ² | 0.48 mm ² | 6.8 mm ² |

* calculated from publication

6 Micro Power Supply

In recent years, there has been a trend towards increasingly connected devices and applications, especially in the smart home and industry 4.0 area. Up to 50 billion such connected devices are expected by 2020 [13]. One of the greatest challenge is the compact and efficient power supply, especially for applications such as sensor nodes, which have a low-power consumption and small size [12, 136–139]. This chapter is based on the micro power supply proposed as part of this work and first published in [44, 49]. Section 6.2 investigates existing concepts of a so called micro power supply. The limits of common concepts are discussed and a new concept is derived in Section 6.3. The micro power supply proposed in this work consists of a fully integrated AC-DC converter described in Section 6.4 and a fully integrated DC-DC converter introduced in Section 6.6. The two converters are linked by an external low-voltage SMD buffer capacitor. Its sizing is derived in Section 6.5. The measurement results of the fabricated micro power supply are presented in Section 6.7. The power supply achieves an output power of 3 mW, resulting in a power density of $390 \mu\text{W}/\text{mm}^2$. This exceeds prior art by a factor of eleven.

6.1 Introduction

For applications in the smart home and industry 4.0 area, various sensor nodes are used. The nodes measure environmental parameters such as air pressure, humidity, temperature, brightness and air quality. More complex tasks such as motion detection, gesture recognition and voice control can be performed by these sensor nodes [136–140]. The recorded parameters and data can then be sent either to a server or directly to a mobile device like mobile phone or smart watch via a wireless connection, e.g. WiFi, ZigBee or Bluetooth, as shown in Fig. 6.1. Depending on the application, the data can be further processed and evaluated. The collected data enables applications such as intelligent lighting and air conditioning, indoor localization and navigation as well as building security.

With increasing complexity, the power consumption of these applications increases and becomes a limiting factor. Despite the fact that in recent years great progress has been made in the area of energy harvesting for indoor applications, this energy source is still not sufficient in many cases. Moreover, power sources as

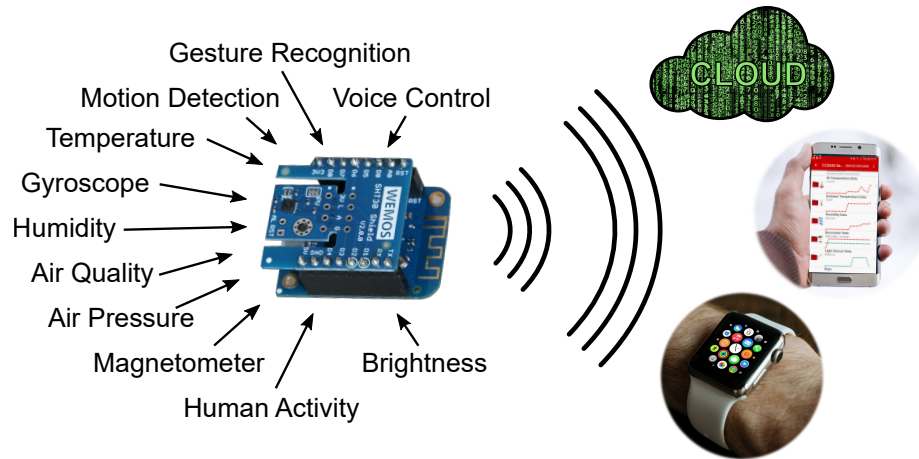


Fig. 6.1: Sensor node for smart home applications.

light, vibration, RF are not reliable, rather depending on their environment and suffering from the limited available energy [14]. Batteries are an alternative energy source, which brings also disadvantages like regular maintenance, limited lifetime and size. For example, to power an application with a power consumption of 1 mW from an AAA battery with 1200mAh at 1.5 V, the application will only run for 75 days. To power this application for at least one year, five AAA batteries are needed. The lifetime can be extended by introducing deep sleep cycles were the application power consumption is as low as possible typically only a few tens of μW . This increases the lifetime but with the cost of availability and still the lifetime is limited. This leads either to a high maintenance effort or to a large package size and weight, which is also not desirable. Another solution could be a low-voltage DC supply grid, which would avoid maintenance issues, but at the expense of additional infrastructure, since it is not available yet. However, the mains voltage is readily accessible at many points indoor e.g. on ceilings (close to lamps or smoke detectors), windows (electric shutters or ventilators) or walls (close to sockets or lighting). Further, the mains voltage is suitable for many indoor applications, it is a reliable and practically unlimited energy source. Therefore, the focus in this work is on the mains voltage as the supply source.

6.2 Micro Power Supply Concepts

In general, there are three possibilities to convert the mains voltage down to an integrated circuit supply voltage of 3.3 V or less, as shown in Fig. 6.2. The voltage can be converted by (a) a transformer, (b) a capacitive divider or (c) by a resistive divider and rectified with a subsequent full bridge rectifier. The goal is to build a highly integrated mains interface to overcome bulky discrete power supplies, which also require a lot of PCB space and high component count [15, 16, 49, 141]. The on-chip integration of a transformer still suffers from a low quality factor and large parasitics. The capacitive divider is an efficient way to convert

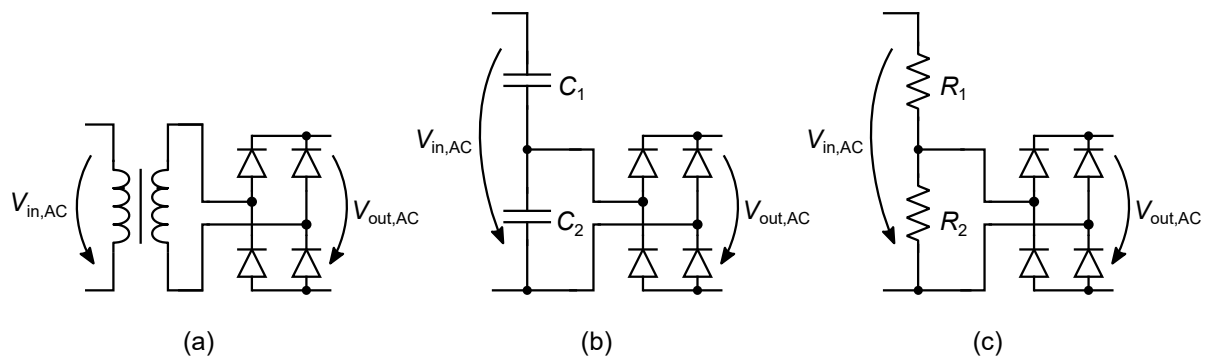


Fig. 6.2: Three ways to convert high voltage down to a lower level: (a) with a transformer, (b) with a capacitive divider and (c) with a resistive divider.

the mains voltage down to a low-voltage level as shown in [15, 16, 142]. These highly integrated power supplies are implemented in standard CMOS technologies. These concepts suffer from the low frequency of the mains and the low density of the high-voltage capacitor. This leads to a low capacitor value (C_1 in Fig. 6.2(b)), which limits the output power of this concept. In [16] a high-voltage capacitor of 50 pF is implemented at a density of 12.5 pF/mm², which covers a silicon area of 4 mm², whereas providing a maximum output power of 287 μ W. The resistive divider depicted in Fig. 6.2(c) shows a poor efficiency, but can deliver significantly higher output power on chip level, providing a solution for applications like mentioned above. The mains interface in [141] is built in an expensive silicon on sapphire SOS technology, which is not always suitable for products. A challenge of down-converting the mains voltage is its zero crossing phase of the mains voltage. For this time period, energy has to be buffered by a capacitor C_B to maintain the converter output power. This work shows the potential of buffering this energy at a high-voltage level to increase efficiency. A series regulator is used in the AC-DC interface of the proposed integrated micro power supply, implementing the concept of Fig. 6.2(c). It is designed in a low cost high-voltage CMOS technology, which allows a direct connection to the mains voltage. This implementation overcomes the power limitation of Fig. 6.2(b) and realizes high-power density with a small form factor of the micro power supply. For the subsequent DC-DC converter a fully integrated high-input voltage SC converter with a fixed conversion ratio of 4:1 is used in a first step. A multi-ratio SC converter can be utilized to further improve the output power or to reduce C_B .

6.3 System Architecture

The process technology has major influence on the possible system architecture. The use of a standard CMOS technology reduces the maximum manageable voltage on-chip to less than 100 V. A mains interface requires either a capacitive or a resistive passive step down conversion with the limitations described above. The high-voltage CMOS technology, used in this work, allows to handle voltages up to 700 V. In Fig. 6.3 the system architecture of the proposed micro power supply is depicted. It comprises an AC-DC and a DC-DC converter. The AC-DC converter is connected to the mains and linked to the DC-DC converter by the buffer capacitor C_B . The AC-DC converter rectifies the mains voltage and reduces it to an unregulated manageable DC voltage, which is defined by a stack of diodes. This unregulated DC voltage $V_{out,AC}$ is converted into the regulated output voltage V_{out} by the subsequent DC-DC converter. Due to the low frequency of the mains, the buffer capacitor C_B is needed to bridge the voltage gap at AC zero crossing. C_B is an external low-voltage SMD capacitor. The goal of this architecture is to keep C_B as small as possible and eventually to integrate C_B in a further step. The full integration is also supported by the DC-DC converter. A fully integrated SC converter is implemented, which utilizes C_B more efficiently compared to a linear regulation due to its higher efficiency. This DC-DC converter includes a SC power stage, which is controlled by a VCO, the pulse generator, the switch controller, the supply generation and the supporting circuits, consisting of level shifters, charge pumps and drivers. Overall, the system architecture of Fig. 6.3 enables high output power of the micro power supply. This is limited by the energy throughput of the DC-DC converter, not by the AC-DC mains interface like in the capacitive based approaches.

A safe start-up is achieved through the AC-DC converter implementation. The supply generation of the DC-DC converter starts the circuits with the rising input voltage $V_{out,AC}$.

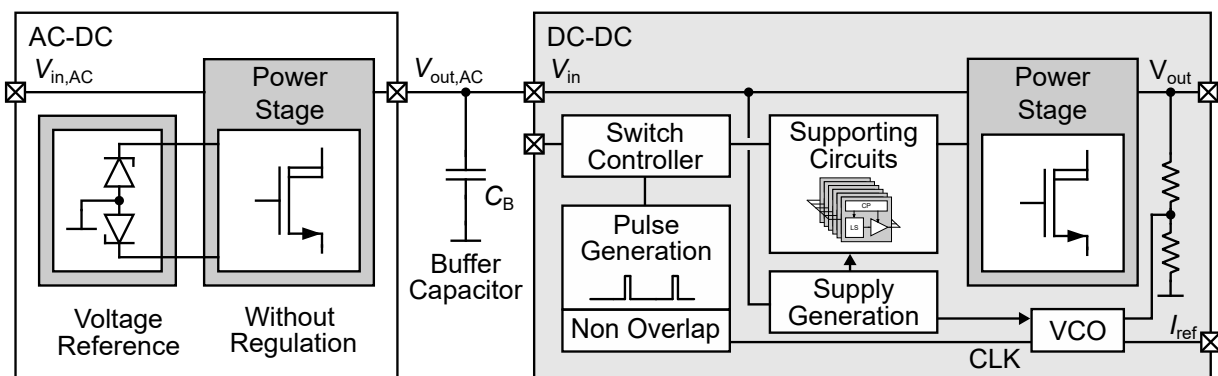


Fig. 6.3: Top-level block diagram of the proposed micro power supply.

6.4 AC-DC Converter Implementation

6.4.1 AC-DC Converter Design

The schematic of the proposed AC-DC converter, depicted in Fig. 6.4, comprises a full bridge rectifier (MN₁, MN₃, D₂ and D₄), combined with two series regulators (SR) (SR1: R₁, D₁, MN₂ and SR2: R₂, D₃, MN₄), one for each half-wave of the AC input voltage. The mains voltage, is rectified and down converted to a defined output voltage. The current of the positive half-wave flows from the input V_{AC+} through MN₂ and D₂ to the output $V_{out,AC}$ and through MN₃ back to V_{AC-} . For the negative half-wave a similar path is formed by the devices MN₄, D₄ and MN₁. Only MN₁, MN₂, MN₃, MN₄, R₁ and R₂ have to withstand the high input voltage of the mains. The high-ohmic resistors R₁ and R₂ ensure a soft turn on of MN₂ or MN₄ respectively and a smooth charging of C_B. SR1, SR2 provide the output voltage $V_{out,AC}$. The output voltage $V_{out,AC}$ is determined by the diodes D₁ and D₃, which are implemented as stacked devices to get the desired biasing voltage for MN₂ and MN₄, respectively. The output power can be increased by scaling up MN₁ to MN₄. This full bridge rectifier provides three major advantages over a conventional full bridge rectifier, especially with respect to IC level integration:

- 1) It rectifies the large AC input voltage and converts it down in a single step.
- 2) It reduces the high-voltage device count. D₂ and D₄ can be realized with low-voltage devices in this design, which reduces area consumption.

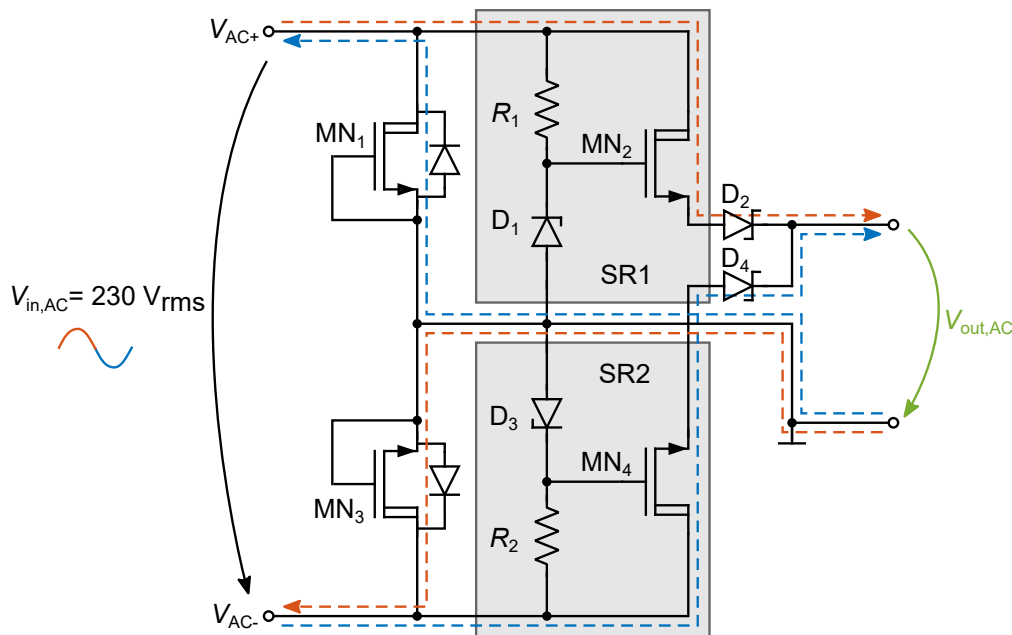


Fig. 6.4: AC-DC converter implementation.

- 3) This topology can be implemented without high-side devices. For high-voltage CMOS technologies the source-substrate voltage of high-voltage NMOS devices and the drain-source voltage of high-voltage PMOS devices is often limited. The introduced rectifier topology can use such devices, since the output voltage of the AC-DC converter complies to these limits (source-bulk voltage of MN₂ and MN₄).

Figure 6.5(a) shows the different waveform of the AC-DC converter. The positive half-wave V_{AC+} and the negative half-wave V_{AC-} are rectified. The dashed line $V_{out,AC}$ shows the rectified and reduced output voltage, without buffer capacitor C_B . The output voltage $V_{out,AC}$ follows the input voltage V_{in} and is clamped to a certain voltage V_{clamp} . In Fig. 6.5(b), the enlarged section of the zero crossing including the buffer capacitor C_B is depicted. It shows the voltage drop ΔV starting at V_{clamp} during the zero crossing (t_{gap}).

The high-voltage devices MN₁ to MN₄ and R₁, R₂ are connected to the mains. In case of 230 V_{RMS}, 50 Hz the peak voltage is as high as $\sqrt{2} \cdot 230 \text{ V} = 325 \text{ V}$. The size of these high-voltage devices scales with the voltage, hence the number of these devices has to be minimized. However, the high-voltage transistors MN₁ to MN₄ occupy more than 1/2 of the total AC-DC converter area (see Fig. 6.12). D₁ and D₃ are stacked zener diodes with a nominal zener voltage of 5.8 V each. The low-voltage diodes D₂ and D₄ are realized with Schottky diodes.

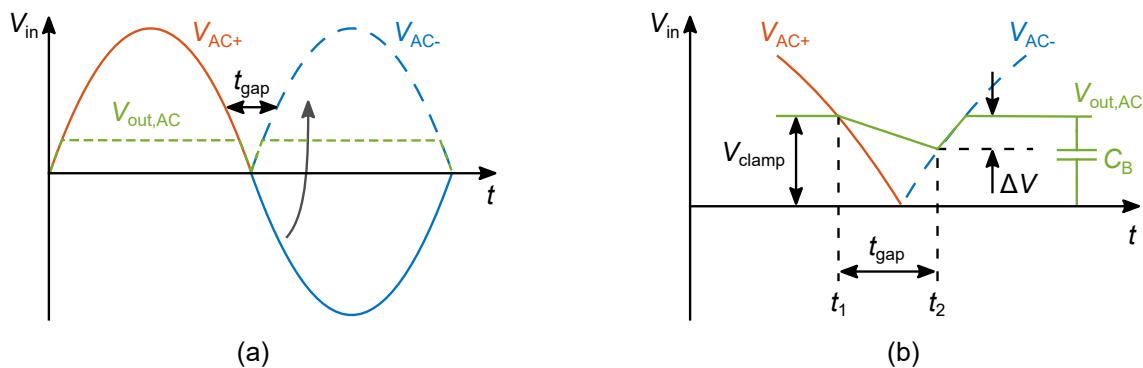


Fig. 6.5: Waveforms of the AC-DC converter. (a) full period without buffer capacitor C_B at $V_{out,AC}$, (b) enlarged section at zero crossing with $C_B \neq 0$.

6.4.2 AC-DC Converter Efficiency

The most lossy parts of the AC-DC converter are the series regulators SR1 and SR2. The losses are caused by the fact, that the high input voltage drops across MN₂ and MN₄. To analyse the losses and to keep them as low as possible, a simplified model is used. The efficiency of the series regulator can be approximated by

$$\eta = \frac{V_{\text{out,AC}}}{V_{\text{in,RMS}}} \cdot 100\% \quad (6.1)$$

$V_{\text{in,RMS}}$ is the RMS value of the AC-DC input voltage $V_{\text{in,AC}}$, whereas $V_{\text{out,AC}}$ is the DC output voltage of the AC-DC converter. The gate biasing losses of the series regulators and the losses of the rectifier are negligible. The ideal efficiency decreases with increasing $V_{\text{in,RMS}}$ and increases with higher output voltage $V_{\text{out,AC}}$, while it is independent from load current. Since the mains voltage is fixed, only $V_{\text{out,AC}}$ can be changed to increase the efficiency and should be as high as possible [16]. For choosing $V_{\text{out,AC}}$ also the efficiency of the AC-DC and DC-DC converter has to be considered. The DC-DC converter performance depends on the topology and the technology parameters, e.g. voltage ratings of the devices and their parasitics, as discussed in Chapter 3. The voltage $V_{\text{out,AC}}$ in this work is about 17 V and is limited to the maximum input voltage of the subsequent DC-DC converter used in this work.

6.5 Buffer Capacitor Sizing

During the time when the mains voltage is lower than the clamp voltage V_{clamp} (see Fig. 6.5(b)), capacitor C_{B} has to buffer the input voltage of the DC-DC converter. In order to determine the size of C_{B} , the time gap t_{gap} , which is depicted in Fig. 6.5(b), has to be calculated. With

$$V_{\text{in}}(t) = \sqrt{2} \cdot V_{\text{in,RMS}} \cdot \sin(2\pi ft) \quad (6.2)$$

the time to voltage correspondence

$$t(V_{\text{in}}) = \arcsin\left(\frac{V_{\text{in}}}{\sqrt{2} \cdot V_{\text{in,RMS}}}\right) \cdot \frac{1}{2\pi f} \quad (6.3)$$

can be derived. From $V_{\text{in}}(t_1) = V_{\text{clamp}}$ and $V_{\text{in}}(t_2) = V_{\text{clamp}} - \Delta V$, the value for t_{gap} can be calculated $t_{\text{gap}} = t_2 - t_1$. The charge Q , which have to be stored at C_{B} , is

$$Q = I_{\text{C}} \cdot t_{\text{gap}} \quad (6.4)$$

The input current I_{in} of any DC-DC converter can be calculated from the output current I_{load} , the output voltage V_{out} , the input voltage V_{in} and the efficiency $\eta_{\text{DC-DC}}$ of the DC-DC converter.

$$I_{\text{in}} = \frac{I_{\text{load}} \cdot V_{\text{out}}}{\eta_{\text{DC-DC}} \cdot V_{\text{in}}} \quad (6.5)$$

Since the voltage at C_B varies, which is the input voltage of the DC-DC converter, the input current I_{in} also varies with an average value of

$$I_{in,avg} = \frac{I_{load} \cdot V_{out}}{\eta_{DC-DC} \cdot (V_{clamp} - (\frac{\Delta V}{2}))}. \quad (6.6)$$

The size of the buffer capacitor C_B can be calculated with:

$$C_B = \frac{I_{in,avg} \cdot t_{gap}}{\Delta V}. \quad (6.7)$$

Inserting (6.6) in (6.7) and replacing t_{gap} by $t_2 - t_1$ yields to

$$C_B = \frac{I_{load} \cdot V_{out}}{\eta_{DC-DC} \cdot (V_{clamp} - (\frac{\Delta V}{2}))} \cdot \frac{(t_2 - t_1)}{\Delta V}. \quad (6.8)$$

Figure 6.6 shows the dependencies of (6.8). The size of the buffer capacitor C_B is shown over the voltage drop ΔV at C_B for three different DC-DC converter efficiencies. The simulation results were performed for the conditions $V_{clamp} = 17 \text{ V}$, $V_{out} = 3.3 \text{ V}$ and $P_{out} = 10 \text{ mW}$. In order to achieve a compact implementation, the buffer capacitor should be as small as possible. C_B can be reduced by increasing the voltage drop ΔV at C_B and by increasing the efficiency. An increase of V_{clamp} does not achieve the desired reduction of C_B , since the buffer time $t_{gap} = t_2 - t_1$ increases with rising V_{clamp} . If the efficiency of the DC-DC converter increases towards 100%, the size of C_B can be more than halved compared to a converter efficiency of 45%, e.g. with a voltage drop $\Delta V = 1 \text{ V}$, C_B can be reduced from $> 4 \mu\text{F}$ down to $2 \mu\text{F}$. Using a linear regulator instead of the DC-DC converter allows a wide voltage range from V_{clamp} down to nearly V_{out} , thus reducing

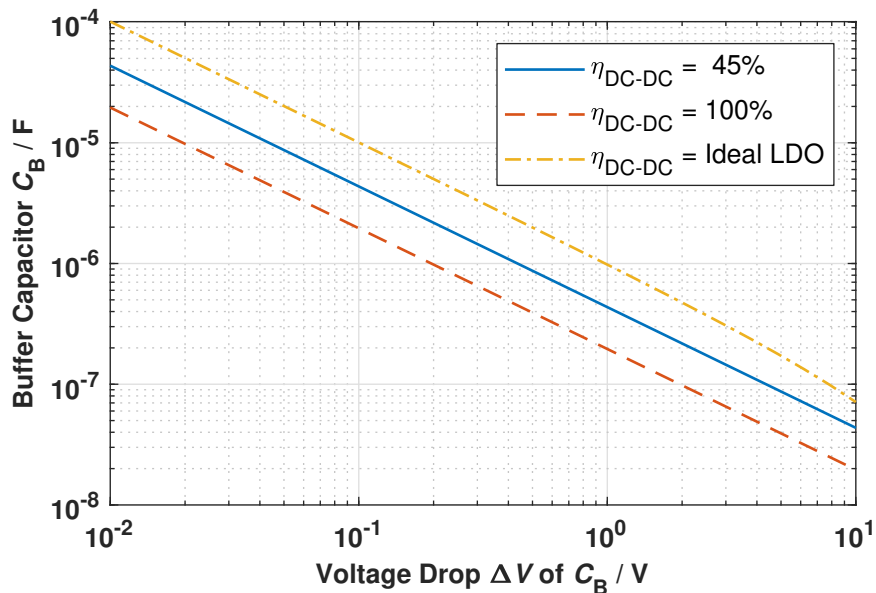


Fig. 6.6: Sizing of the buffer capacitor C_B as a function of the voltage drop ΔV and DC-DC converter efficiency, simulated for the parameters $V_{clamp} = 17 \text{ V}$, $V_{out} = 3.3 \text{ V}$ and $P_{out} = 10 \text{ mW}$.

the size of C_B . However, due to the poor linear regulator efficiency C_B is not used properly. By selecting a multi-ratio SC converter, as described in Chapter 5, the voltage range could be extended, while C_B could be used more efficiently. This contributes to the goal of further reducing the capacitor size. The following section introduces the high-voltage DC-DC converter developed for this application.

6.6 DC-DC Converter

In order to achieve a high overall efficiency, the input voltage of the DC-DC converter $V_{in} = V_{out,AC}$ should be as high as possible (see (6.1)). Furthermore, the DC-DC converter should be fully integrated on-chip to allow a compact design. For these requirements SC converters are particularly suitable, as described in Chapter 2. Figure 6.7 shows a state-of-the-art comparison of fully integrated SC converters with a high-input voltage. There are only a few high-voltage SC converters with an input voltage greater than 5 V. This is related to the challenges which come up with building a high-voltage SC converter in terms of efficiency, power density, topology, technology, parasitic losses and the high-voltage building blocks as discussed in Chapter 3 and 4. The topology investigations in Section 3.3 show that the cascaded 4:1 SC converter based on two 2:1 SC converter cells, as also used in Chapter 5 in the recursive buck-boost SC converter, is particularly suitable for this purpose. It is therefore used in the proposed high-voltage SC converter.

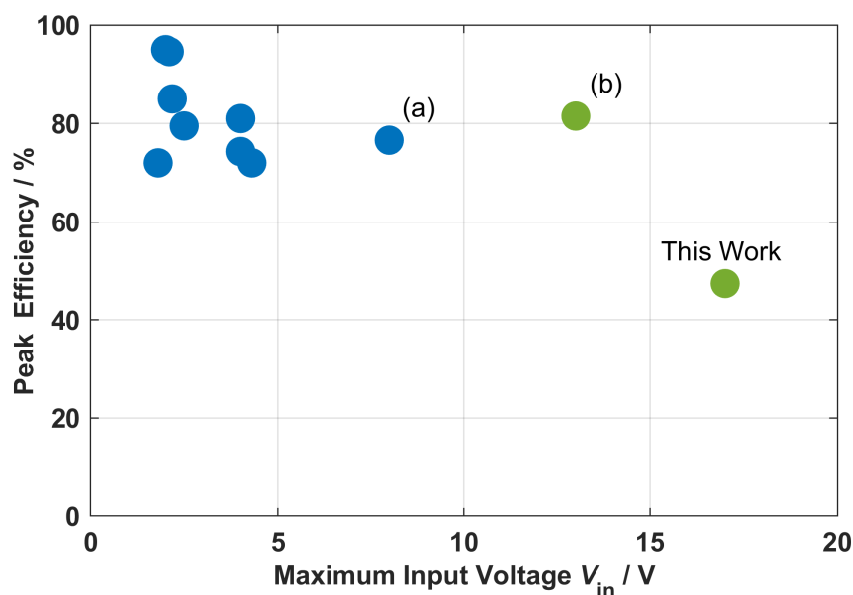


Fig. 6.7: State-of-the-art comparison for fully integrated DC-DC SC converters with (a) = [42, 43] and (b) = [41].

6.6.1 High-Voltage Switched-Capacitor Converter Architecture

Figure 6.8 shows the cascaded 4:1 high-voltage SC converter topology. The converter comprises two 2:1 SC converter cells including two flying capacitors ($C_{\text{fly}1}$ and $C_{\text{fly}2}$) and a buffer capacitor $C_{\text{mid}1}$. The cascaded 4:1 topology offers three main advantages compared to a 4:1 series-parallel topology. First, the maximum voltage ratings of the switches decrease from $3/4 V_{\text{in}}$ to $1/2 V_{\text{in}}$, with all the advantages described in Section 3.1. Latest research confirms that cascaded SC converter topologies enhance conventional SC converter in terms of components voltage rating and consequently achieve higher efficiencies [143]. Secondly, two instead of three flying capacitors are required and the voltage swing of the parasitic bottom-plate capacitance is reduced, which reduce bottom-plate losses as described in Section 2.3.2. Finally, the cascaded topology can be expanded in a further step to a multi-ratio SC converter to enlarge the input voltage range to reduce the buffer capacitor C_{B} as described in Section 6.5.

For the desired output voltage $V_{\text{out}} = 3.3 \text{ V}$ an input voltage range from 16 V to 17 V results for the conversion ratio of 4:1. The converter works with two phases ϕ_1 and ϕ_2 at a duty cycle of 50%. The component voltages of cell 2 is half of cell 1, but the current scales inversely. As a consequence, the turn-on resistance of switch S_5 to S_8 has to be half compared to S_1 to S_4 according to the charge flow analysis [59]. Each power switch is driven by a high-voltage circuit, except of the low-side switches S_4 and S_8 . Each high-voltage circuit includes a charge pump, a level shifter and a driver as introduced in Chapter 4, all designed for low-power consumption. In this design the pulsed resistive level shifter (see Fig. 4.2(c)) is used for the signal shifting. As illustrated in Fig. 6.8, the different charge pump types from Section 4.2 are used according to their properties, this will be discuss in Section 6.6.2. In phase ϕ_1 , the flying capacitors $C_{\text{fly}1}$ and $C_{\text{fly}2}$ are in series with C_{mid} and the output capacitor C_{out} , respectively. For the second phase ϕ_2 , the flying capacitors $C_{\text{fly}1}$ and $C_{\text{fly}2}$ are connected in parallel to C_{mid} and C_{out} , respectively.

6.6.2 High-Voltage SC Converter Implementation

The high-voltage SC converter is implemented in the same 700 V technology as the AC-DC converter. This technology provides lateral DMOS devices, suitable for high-voltage power switches and for the supporting high-voltage circuits like gate drivers, level shifters and charge pumps.

Signal Generation

The clock signal CLK, depicted in Fig. 6.3, is generated by a three-stage ring oscillator and is regulated by V_{out} in the VCO block. The blocks non-overlap, pulse generation and switch controller, as depicted

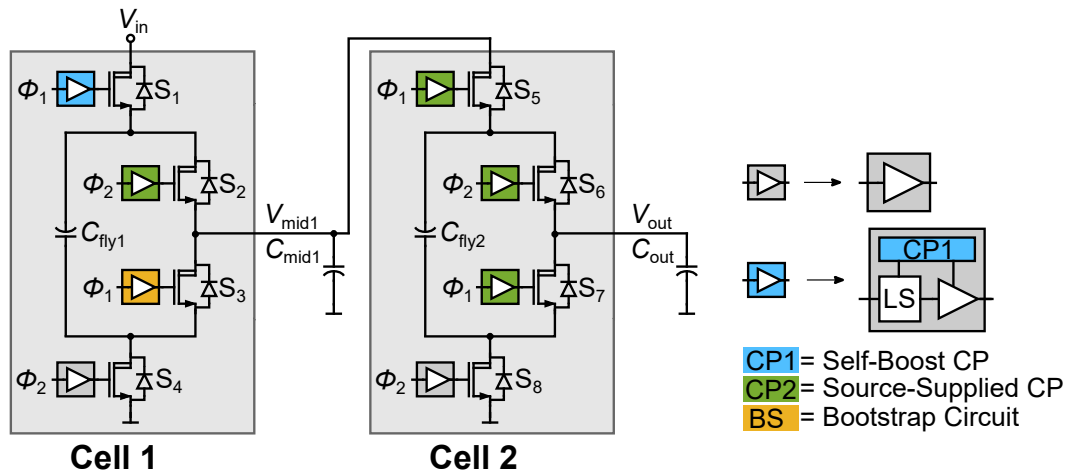


Fig. 6.8: Cascaded 4:1 SC converter power stage.

in Fig. 6.3, generate the pulses required to control the charge pumps and the level shifters for the power switches in the power stage. The implementation of these blocks are shown in Fig. 6.9. The block non overlap generates non-overlapping two-phase clock signals (ϕ_1 and ϕ_2). The signals ϕ_1 and ϕ_2 are used to generate the on and off pulses, which are shifted by the level shifters to control the power switches, as well the signal V_x for the charge pumps. These signals are connected to the switch controller, which distributes the signals to each level shifter, charge pump and driver.

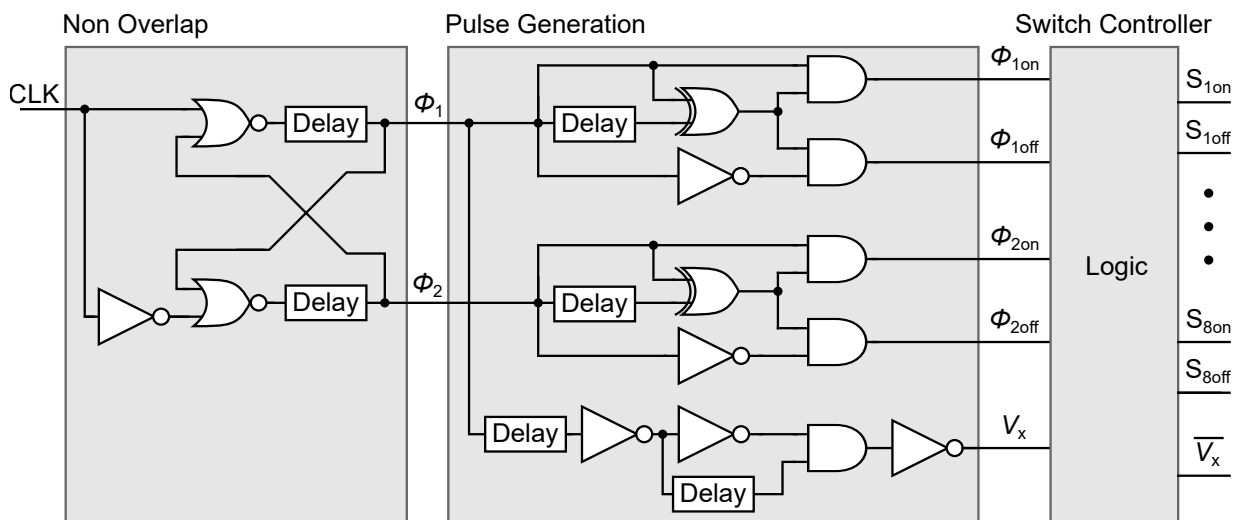


Fig. 6.9: Pulse generation of the control signals for level shifters, charge pumps and power switch drivers.

Charge Pump Implementation

The SC converter consists of eight power switches, which are connected to different voltage levels (see Fig. 6.8). The switches S_4 and S_8 can be direct controlled without level shifter and charge pump. The switches S_3 and S_7 can be supplied by a bootstrap circuit since the source potential is connected to the ground during ϕ_2 . At switch S_5 , the voltage of the source changes between ϕ_1 (e.g. 8.5 V) and ϕ_2 (e.g. 4.2 V), hence the use of a bootstrap circuit is not possible. Therefore, the source-supplied charge pump of Fig. 4.10(d) is used. In Fig. 6.10 the implemented high-voltage circuits for switch S_5 which comprise the implemented pulsed resistive level shifter, the source-supplied charge pump and the driver are shown. The source-supplied charge pump can also be used for S_2 and S_6 , since their source is connected to a fixed voltage level (see Section 4.2). In this design, the charge pump capacitors are implemented as MIM capacitors. The sizing of C_p and C_s is set as to drive the transistors of the second 2:1 cell (see Fig. 6.8), where each transistor requires a gate charge of 2.3 pC per transition. Additionally, the charge pump also has to provide 1 pC/MHz to supply the level shifter. The target charge pump output voltage for the switch drivers and the level shifters is 4 V. However, two Schottky diodes are in the current path, with a forward voltage of around 250 mV each, the voltage drop caused by the equivalent output resistance of the charge pump should be 0.5 V. With the charge flow analysis [59], $C_p = 6.6$ pF follows from $C_p = Q_{\text{total}}/\Delta V$. A capacitance value of $C_s = Q_{\text{total}}/\Delta V = 12$ pF for the output capacitor can be derived for a maximum output voltage ripple of $\Delta V = 275$ mV. With an added safety margin, in this design a value of 6.9 pF for C_p and 12.4 pF for C_s was chosen. The signal V_x is generated by the pulse generation block, depicted in Fig. 6.9. A pulse length of 60 ns is sufficient for the charge balancing process between C_p and C_s . Figure 6.11 shows the simulated voltage signals of the source-supplied charge pump for S_5 (see Fig. 6.8) at a clock frequency of 1 MHz. The voltage across C_s (Fig. 6.11(c)) has a maximum voltage drop of 230 mV. V_x receives pulses of 60 ns, in which C_s gets charged from C_p , see Fig. 6.11(d). In Fig. 6.11(e), the gate-source voltage of transistor S_5 is depicted.

For switch S_1 the source-supplied charge pump cannot be used, since the source voltage swing of switch S_1 is greater than $V_{\text{DDH}} - V_{\text{SSH}}$. Therefore, the self-boost charge pump has to be used in this case. The sizing is carried out under the same procedure and conditions as for the source-supplied charge pump.

6.6.3 Level Shifter Implementation

The implemented pulsed resistive level shifter (see Section 4.1) was optimized for low-power consumption and propagation delay, which correlates to some extent. Figure 6.10 shows the implemented pulsed resistive level shifter. The resistors R_1 and R_2 define the peak currents I_{peak} from V_{DDH} down to V_{SSL} and have main

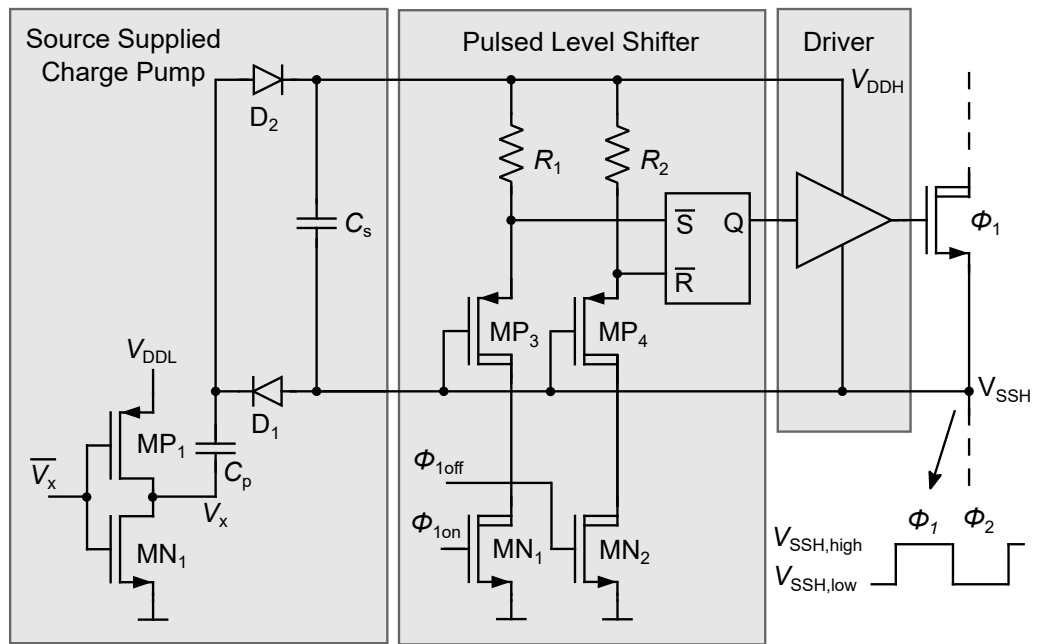


Fig. 6.10: Implementation of high-voltage circuits which comprise a source-supplied charge pump, a pulsed resistive level shifter and a driver.

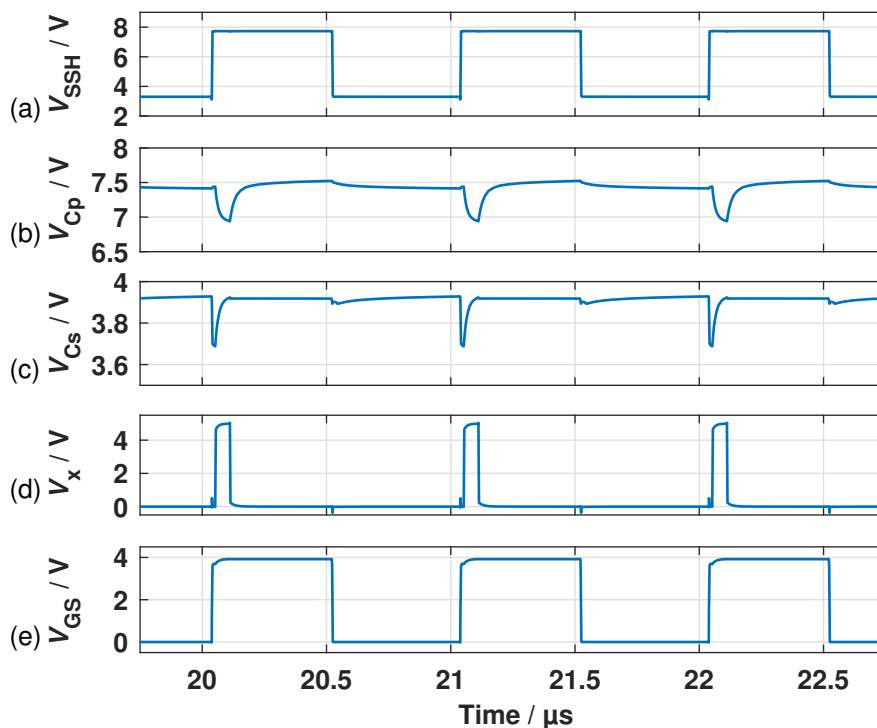


Fig. 6.11: Simulation results of the source-supplied charge pump used for switch S_5 (see Fig. 6.8) at a clock frequency of 1 MHz.

influence on power consumption and speed. To keep the losses small, the pulse length of 5 ns was kept to be as short as possible. The implemented values for R_1 and R_2 can be derived by the input capacitance of the flip-flop, the pulse length and a safety margin which includes temperature and process variation. A good trade-off between speed, losses and safety margin is a value of 300 k Ω for R_1 and R_2 in the proposed design. To increase the speed of the level shifter, the \bar{S} and \bar{R} inputs of the SR flip-flop were designed with a threshold close to V_{DDH} for faster detection of the set or reset pulses. The high-voltage transistors MP_3 and MP_4 protect the floating high-side circuits. All four high-voltage transistors MN_1 , MN_2 , MP_3 and MP_4 are sized with minimum gate length and width to minimize the gate charge losses. A total power consumption of 15 μ W at a switching frequency $f_{sw} = 2$ MHz was achieved. This is five times less compared to a standard cross-coupled level shifter under same test conditions and more than six times less compared to an ultra-fast cross-coupled level shifter proposed in [116].

6.6.4 Power Stage Implementation

The power switches are sized such that the converter operates with in the slow switching limit (SSL), see Section 2.3. The flying capacitors (C_{fly1} and C_{fly2} (total 1500 pF)) and C_{mid} (600 pF) were implemented as MIM capacitors with a dielectric strength of 10 V and a low parasitic bottom-plate capacitance density as described in Section 2.4. C_{out} (1400 pF) was implemented by a MOS capacitor with a high capacitance value and a dielectric strength of 5 V. In order to reduce the parasitic bottom-plate losses of C_{fly1} and C_{fly2} , the introduced bottom-plate loss optimization approach and the discussed intrinsic charge recycling technique described in Section 4.4 were applied. Hence, the bottom-plate losses were reduced by around 50% from 24% down to 14% of the total SC converter losses.

6.7 Experimental Results

Figure 6.12 shows the chip photograph of the implemented micro power supply. The section of the AC-DC converter stage is enlarged to indicate the area, which is mainly occupied by the high-voltage transistors MN_1 to MN_4 . Both converters are implemented on the same chip in a low cost 0.35 μ m 700 V CMOS technology. The AC-DC converter occupies a chip area of 0.9 mm² and the DC-DC converter an active area of 6.77 mm², which adds up to a total active area of 7.7 mm².

The micro power supply was tested for several input voltages up to $V_{in} = 230 V_{RMS}$ at $f_{mains} = 50$ Hz and 60 Hz. An output power of up to $P_{out} = 3$ mW was achieved. In Fig. 6.13 the waveforms of the micro power supply are depicted for $V_{in} = 230 V_{RMS}$, $f_{mains} = 50$ Hz (325 V peak) and $P_{out} = 2$ mW. C_B is 10 μ F (SMD 0603) for this measurements. $V_{out,AC}$ reaches a value of around 16 V, set by the implemented diode stack

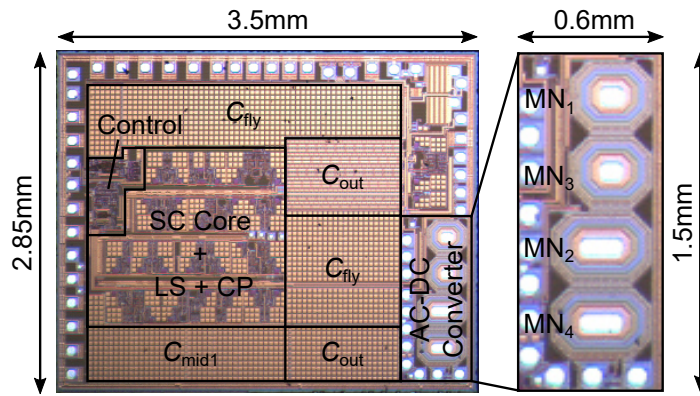


Fig. 6.12: Photograph of the micro power supply.

D_1 , D_3 (see Fig. 6.3 and Fig. 6.5). The ripple of $V_{out,AC}$ has an acceptable level in the order of 100 mV. V_{out} is smooth and stable at around 4 V for this measurement without external output capacitor. V_{out} has a ripple of less than 200 mV, which is 6% of V_{out} . The measured efficiency of only the AC-DC converter is 5% for $V_{in} = 110 V_{RMS}$ and 2.5% for $230 V_{RMS}$, which is low, as expected from Section 6.4.2.

Figure 6.14(a) shows the measured efficiency vs. load current. For a wide load range, starting from 0.15 mA to the maximum load current of 1.9 mA, the SC converter shows a high efficiency of more than 40%, with a maximum efficiency of 47.4% at 1.2 mA load current. The efficiency versus the input voltage is shown in Fig. 6.14(b) for $V_{out} = 3.3 V$ and a load current of 1 mA. An efficiency of more than 40% is achieved over an input voltage of 15.5 V to 17 V. The efficiency in this design suffers from the internal supply

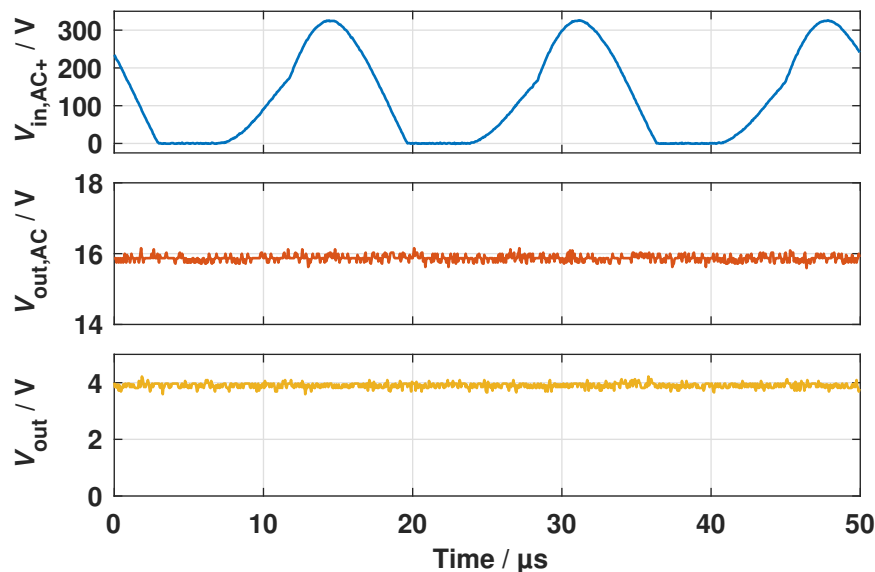


Fig. 6.13: Measured waveforms of the micro power supply for $C_B = 10 \mu F$, $V_{in,AC} = 230 V_{RMS}$, $f_{mains} = 50 Hz$ and $P_{out} = 2 mW$.

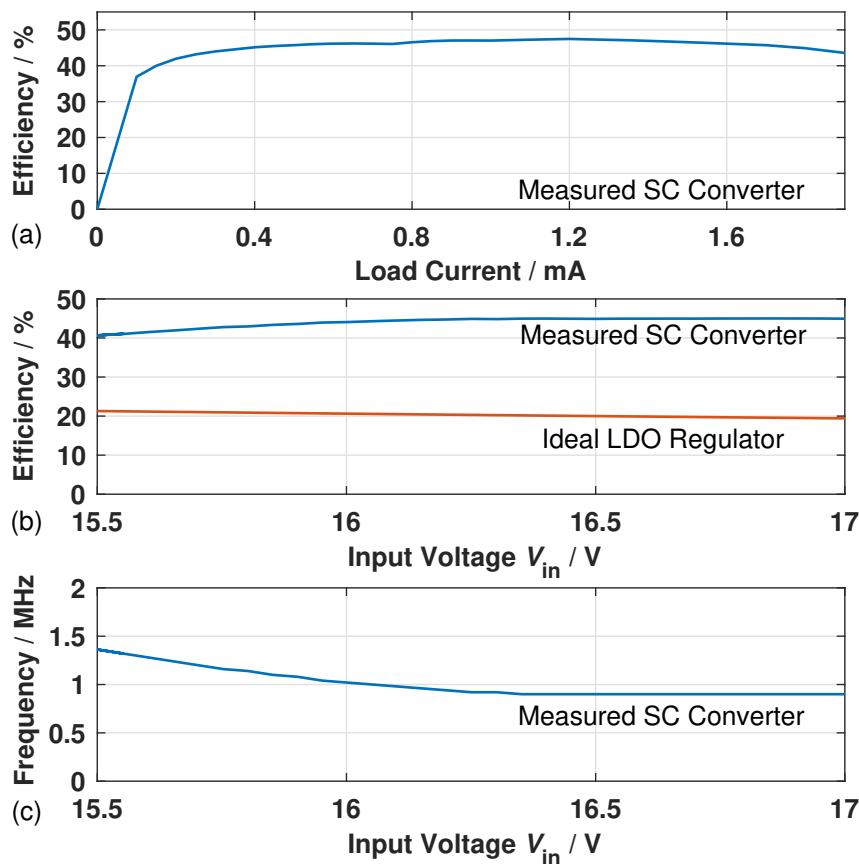


Fig. 6.14: (a) Measured efficiency vs. load current. (b) Measured 4:1 SC converter efficiency for 1 mA load compared to the ideal LDO efficiency curve. (c) Switching frequency vs. SC converter input voltage.

generation by a series regulator (see Fig. 6.3). The converter efficiency could be improved with a more efficient supply generation. The ideal efficiency of an LDO (also shown in Fig. 6.14(b)) is still about half of the 4:1 SC converter efficiency. Figure 6.14(c) depicts the variation of the switching frequency of the DC-DC converter in the range of 1 MHz. The transient response of a load step from 1.0 mA to 0.5 mA and up again to 1.0 mA is shown in Fig. 6.15. At 1.0 mA the clock frequency is 900 kHz. At the negative load step, the V_{out} regulator detects the rising voltage of V_{out} and reduces the clock frequency, which settles at 400 kHz. The V_{out} regulator stabilizes V_{out} at the target voltage. Similarly, at the positive load step, the clock frequency immediately increases and V_{out} stabilizes.

Table 6.1 shows a state-of-the-art comparison of highly integrated micro power supplies for input voltages up to 230 V_{RMS} . The proposed micro power supply achieves more than 14 times higher P_{out} and more than eleven times higher power density compared to prior art. The efficiency of the AC-DC converter is low, due to the concept, but the efficiency of the DC-DC converter with its input voltage up to 17 V, is twice as

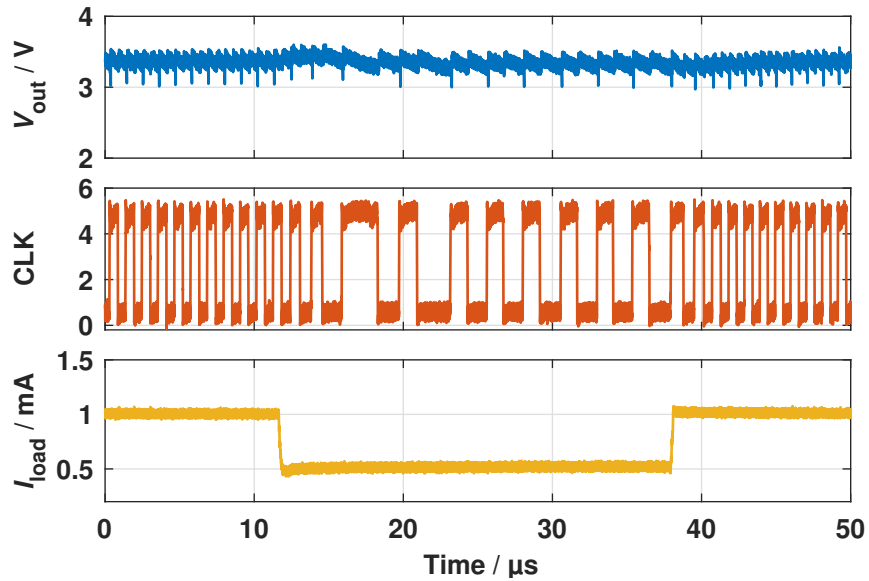


Fig. 6.15: Measured 4:1 SC converter transient response for 0.5 mA load step at the converter output.

Tab. 6.1: Comparison to state-of-the-art

| | [15] | [16] | [17] | [142] | This work |
|-----------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|-------------------------------|
| Technology | 0.13 μm | 0.35 μm | 0.35 μm | 0.35 μm | 0.35 μm |
| V_{in} | 120 V _{RMS} | 120/230 V _{RMS} | 120 V _{RMS} | 120 V _{RMS} | 110/230 V _{RMS} |
| V_{out} | 4 V | 3.3 V | 9.5 V | 9.5 V | 3.3 V |
| Ext. Components | - | 1x SMD cap | - | 2x SMD cap | 1x SMD cap |
| Chip Size | 3.5 mm ² | 6 mm ² | 9.8 mm ² | 9.8 mm ² | 7.7 mm ² |
| $P_{\text{out,max}}$ | 1.5 μW | 208 μW | 15.16 μW | 14.27 μW | 3 mW |
| Power Density | 0.43 $\mu\text{W}/\text{mm}^2$ | 34.6 $\mu\text{W}/\text{mm}^2$ | 1.55 $\mu\text{W}/\text{mm}^2$ | 1.46 $\mu\text{W}/\text{mm}^2$ | 390 $\mu\text{W}/\text{mm}^2$ |
| $\eta_{\text{AC-DC}}$ (120/230 V) | 59% | 68*/57*% | 80.7% | 84% | 5**/2.5% |
| $\eta_{\text{DC-DC}}$ | not reported | not reported | not reported | not reported | 47.4% |

*simulated **measured at 110 V

high compared to a linear regulator, with a peak efficiency of 47.4%. The proposed micro power supply has a high degree of integration with increased power density and output power. The future steps will be to improve the overall efficiency and to further reduce the size of the buffer capacitor. This can be achieved by improving the efficiency of the AC-DC converter, e.g. by further increasing the output voltage of the AC-DC converter $V_{out,AC}$. The three-phase SC converter proposed (section 3.4.2) is a promising approach to increase the input voltage of the DC-DC converter, which is linked to $V_{out,AC}$. By using the recursive buck-boost SC converter proposed (Chapter 5), the input voltage range of the DC-DC converter can be significantly improved and thereby C_B further reduced, resulting in a more compact design. A photograph of the prototype is shown in Fig. 6.16. It occupies a fraction of a 1 Euro-Cent coin.

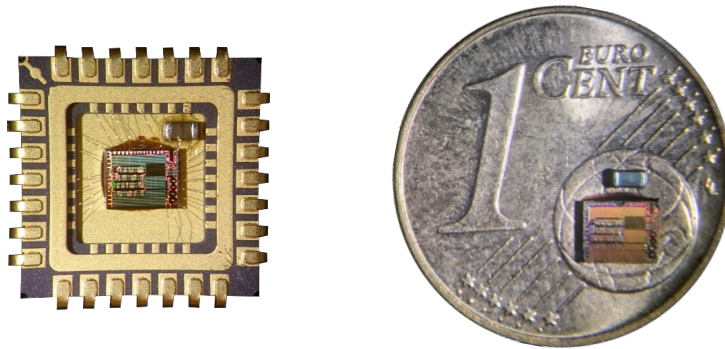


Fig. 6.16: Prototype of the micro power supply.

7 Conclusion and Outlook

This chapter concludes the research presented in this work. Also, an outlook is given, which describes possibilities how high-voltage SC converters can be further improved by future work.

7.1 Conclusion

One of the key challenges in modern power electronics is the compact and efficient design of the power supply. A variety of new applications in future fields such as the Internet of Things IoT, smart home, autonomous driving and e-mobility poses a challenge not only in terms of maximum efficiency, but also in terms of size and weight. In recent years, there has been a strong trend towards an even higher degree of integration up to full integration of power supplies on chips. This highly integrated power management enables optimal adaptation of the power supply to the application. This leads to an increased demand in highly integrated high-voltage power supplies with high input voltages and greater input voltage ranges.

This work focuses on integrated high-voltage switched-capacitor (SC) converters with a wide input voltage range of up to 60 V input voltage and an output power of up to 40 mW. Currently, there are few approaches of fully integrated converters with an input voltage greater than 5 V. As the input voltage increases, supporting circuits such as level shifters and charge pumps, which are needed to control the power switches, become more challenging. Since SC converters usually consist of a large number of power switches, the low-power consumption and the area are crucial. This work investigated these supporting circuits and presents a power and area optimized level shifter, a charge pump and a bidirectional switch. In addition, this work focuses on highly integrated mains micro power supplies for low-power applications such as sensor nodes that are directly connected to the mains. State-of-the-art concepts currently only provide an output power in the sub-mW range, which is not sufficient for most applications. This work achieves a high output power in the mW range and a compact form factor.

Within the scope of this work, several level shifter concepts are evaluated. A pulsed resistive level shifter in a 0.35 μm high-voltage CMOS technology is proposed, which can handle up to 20 V. The pulse length is chosen to be as short as possible in order to keep the losses due to cross-currents as low as possible.

The pulse length in this work is only 5 ns. A low-power consumption of 15 μW is achieved at a switching frequency of $f_{\text{sw}} = 2 \text{ MHz}$. In comparison to a conventional cross-coupled level shifter under the same conditions, this corresponds to only one-fifth of the power consumption. Within the scope of this work, a capacitive coupled low-power level shifter for high-voltage applications is proposed. This high-speed capacitive and power efficient level shifter is the first 50 V floating high-side level shifter published that has a power consumption of less than 20 pJ per transition. With only 2.1 pJ per transition, the presented capacitive level shifter consumes more than eleven times less power compared to the state of the art. The level shifter is manufactured in a 0.18 μm high-voltage CMOS technology and verified by measurements at V_{SSH} transitions of up to 50 V with voltage slopes up to 6 V/ns. Post-layout simulations even show a robust operation for V_{SSH} transitions up to 100 V/ns. With a rising and falling propagation delay of less than 1.45 ns, the level shifter was the first 50 V level shifter with a propagation delay of less than 2 ns at the time of publication. The figure of merit for high-voltage level shifters, which takes technology node, maximum voltage, power consumption and propagation delay into account, is improved by a factor of two.

Especially in applications with low power and many power switches, such as SC converters, a compact and efficient charge pump circuit, as presented in this work, is crucial. Existing concepts are investigated and analyzed. A previously published circuit for discrete electronics has been adapted and optimized for an on-chip integrated source-supplied charge pump in a 0.35 μm high-voltage CMOS technology. As a major advantage of the developed source-supplied charge pump the losses do not increase with increasing high-voltage level and remain constant compared to the self-boost charge pump (state of the art). The efficiency could be improved by a factor of 1.6 for typical use, compared to the self-boost charge pump. The concept proposed shows constant efficiency since the losses do not scale with the voltage level. The efficiency is improved compared to the self-boost charge pump by a factor of four and higher for high-side voltages of up to 20 V. Since the source-supplied charge pump in this work only needs one high-voltage capacitor, it offers a more compact layout. This charge pump is used in the SC converters presented in this work.

Multi-ratio converters require bidirectional switches at certain positions within the power stage, usually realized by a back-to-back transistor configuration. The switch topology proposed in this work is optimized for low dynamic gate charge losses, small size and high-voltage applications. The presented back-to-back switch topology reduces the dynamic gate charge losses by up to 70% compared to the standard topology. The area requirements are reduced by up to 65% compared to the conventional solution. The circuit is implemented and tested in a 0.35 μm high-voltage CMOS technology.

Within the scope of this research, multi-ratio SC converter topologies are investigated for a wide and high input voltage range. The proposed and implemented recursive multi-ratio SC converter reaches the highest and widest reported input voltage range from 2 V to 13 V. Fine granular coverage of the entire input voltage range is achieved with a 4-bit buck-boost architecture and a total of 17 ratios. The SC converter presented

achieves an output power of 10 mW in buck mode with an active area of 6.8 mm² and is manufactured in a 0.35 μm high-voltage CMOS technology. The recursive buck-boost SC converter presented exceeds the state of the art for fully integrated multi-ratio SC converters in particular with regards to three key parameters. The maximum input voltage is increased from 8 V to 13 V. The SC converter improves the state of the art of the absolute input voltage range by a factor of two. The peak efficiency of 81.5% is significantly higher than the state of the art for fully integrated SC converters with an input voltage of 5 V or higher. It is the first published fully integrated SC converter in this category achieving a peak efficiency of greater than 80%.

The micro power supply published as part of this work is designed in such a way that it can supply small sensor nodes, which are for example, used more and more in smart home and industrial 4.0 applications. One of the main challenges is to develop an adequate, reliable and compact power supply for such low-power applications. Several energy sources and topologies are investigated and evaluated. Whereas energy harvesting is still insufficient and unreliable for most indoor applications, the mains is accessible, reliable and practically unlimited. It is a perfect energy source for such applications and used in this work. To improve the state of the art, the focus is on increasing the output power towards the mW range and a high degree of integration leading to a small form factor. The micro power supply developed is realized in a high-voltage CMOS technology, which allows for direct coupling to the mains (230/110 V_{RMS}). The micro power supply chip requires a total active area of 7.7 mm². The presented two-stage approach includes a fully integrated SC converter with an input voltage as high as 17 V. The peak efficiency of 47.4% is twice as high as that of a linear regulator. The proposed micro power supply achieves an output power of 3 mW and the power density improves the state of the art by a factor of 14 and eleven, respectively.

7.2 Outlook

The trend towards full integration of high-voltage SC converters, which is considered in this work, offers a high potential for future work. In particular, the three-phase SC converter topology proposed in this work is promising. Further investigations on even more phases and even higher input voltages are worthwhile. The technologies currently available and particularly the accessible passive components limit the performance of high-voltage SC converters. The low capacitance density of the high-voltage capacitors on the chip is the main disadvantage. This limits both efficiency and power density. To overcome these technological limitations, partial integration with external capacitors is an option. The multi-phase approach presented reduces the number of external capacitors, which makes it particularly promising. The use of external capacitors eliminates nearly all bottom-plate losses and reduces the output resistance R_{out} considerably. Due to the higher capacitance values, the output power can be significantly increased, while reducing the switching frequency at the same time. This has a positive effect on the overall efficiency and enables efficiencies of more than 90%.

The high-voltage SC converters developed in this work are limited to exploit their full potential in terms of efficiency and input voltage range because the high-voltage CMOS technology limits the performance to a great extent. The parasitic bipolar structure limits the maximum input voltage from potentially 20 V down to 13 V and also causes large efficiency drops of up to 15%. By using technologies with better isolation capabilities, in particular SOI technologies, these losses could be avoided. Additionally the charging losses due to the parasitic bottom-plate effect could be further reduced. This would result in an efficiency increase of 5 - 15% over the entire voltage range.

The power consumption and the area are decisive, especially in supporting blocks for high-voltage applications. The source-supplied charge pump improves the state of the art. However, its usage is limited by the voltage swing. Since this circuit offers a great potential for improvement in high-voltage applications, it is recommended that this concept is extended to overcome the restriction due to the limited voltage swing and to enable universal operation.

The micro power supply for low-power applications is optimized in terms of output power and size, but it still needs to be improved in terms of efficiency. The AC-DC conversion stage should be replaced by a more efficient solution. Low-loss charging of the buffer capacitor with the sinusoidal mains voltage would be an option. To reduce the buffer capacitance value, the possible voltage drop at the buffer capacitor should be increased. The multi-ratio SC converter introduced in this work is therefore well suited to replace the fixed-ratio SC converter used in the micro power supply presented. By utilizing the boost mode implemented the voltage at the buffer capacitor could even fall below the output voltage. This would further reduce the size of the buffer capacitor and thus the overall size of the micro power supply.

Appendix

A Recursive Buck-Boost SC Converter Configuration Details

This section provides supplementary configuration details about the recursive buck-boost SC Converter introduced and implemented in Chapter 3 and 5, respectively. The multi-ratio SC converter provides a total of 15 ratios, eleven of these ratios are used in this work. Table A.1 shows the switch control configuration for the different conversion ratios. The signal names provide information like active switching phase (either ϕ_1 or ϕ_2) of the corresponding switch and T stands for the topology. It is required for the proposed back-to-back switch configuration, which is presented in Section 4.3. The ONOFF label is used for the topology switches, as described in Section 5.2. To define the source potential in the standard and proposed back-to-back switch configuration, the transistor with the conducting body diode (see Section 4.3) is always turned on. This facilitates a constant power supply on the high-side voltage domain by means of the floating high-side supply for the corresponding back-to-back switch. A '1' in the table indicates, this switch is active in the defined ratio and a '0' indicates an inactive switch. Figures A.1 to A.12 show the ratios of the proposed recursive buck-boost SC converter from 15/16 to 4/16 with the corresponding ideal voltage values at the switching nodes. Black switches indicates active switches in the respective ratio and are either permanently turned on or turned on with the corresponding phase. The gray switches are turned off for the corresponding ratio.

Tab. A.1: Switch control signal table of the recursive buck-boost SC converter

| Switch | $\frac{15}{16}$ | $\frac{7}{8}$ | $\frac{13}{16}$ | $\frac{3}{4}$ | $\frac{11}{16}$ | $\frac{5}{8}$ | $\frac{9}{16}$ | $\frac{1}{2}$ | $\frac{7}{16}$ | $\frac{3}{8}$ | $\frac{5}{16}$ | $\frac{1}{4}$ | $\frac{3}{16}$ | $\frac{1}{8}$ | $\frac{1}{16}$ |
|-------------|-----------------|---------------|-----------------|---------------|-----------------|---------------|----------------|---------------|----------------|---------------|----------------|---------------|----------------|---------------|----------------|
| S11_phi1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S12_phi2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S13_phi2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S14_phi1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S15_ONOFF_A | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| S15_ONOFF_B | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| S16_ONOFF_A | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S16_ONOFF_B | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S21_phi1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| S22_T | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| S22_phi1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| S23_T | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| S23_phi2 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| S24_phi2 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| S25_phi2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S26_phi1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S27_ONOFF_A | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| S27_ONOFF_B | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| S28_ONOFF_A | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| S28_ONOFF_B | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| S31_phi1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| S32_T | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| S32_phi1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| S33_T | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| S33_phi2 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| S34_phi2 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| S35_phi2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S36_phi1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S37_ONOFF_A | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| S37_ONOFF_B | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S38_ONOFF_A | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| S38_ONOFF_B | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S41_phi1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S42_T | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| S42_phi1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| S43_T | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S43_phi2 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S44_phi2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S45_phi2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S46_phi1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S47_T | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| S47_phi1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| S48_T | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S48_phi2 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

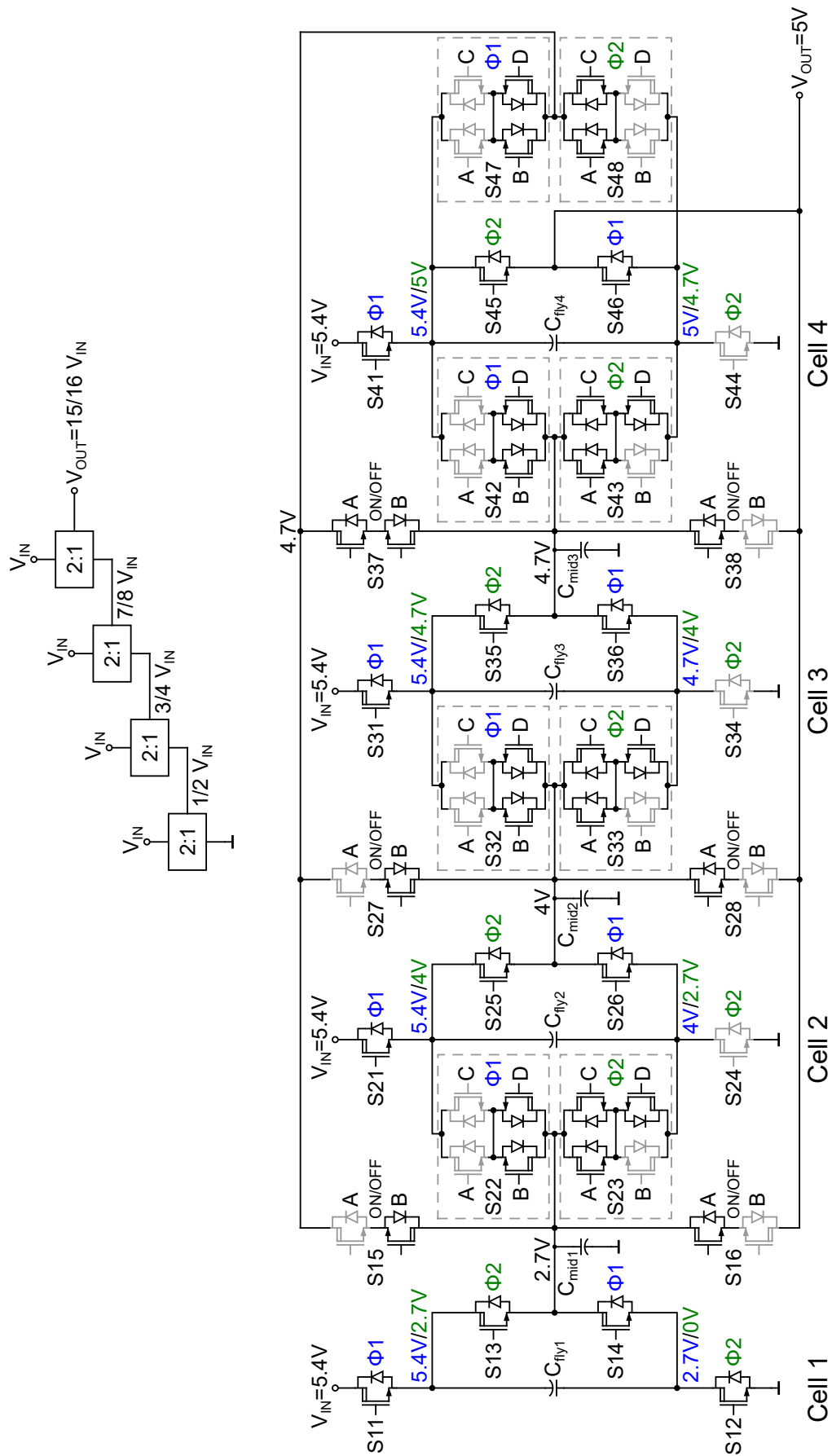


Fig. A.1: Power stage implementation of the recursive buck-boost SC converter in 15/16 ratio configuration.

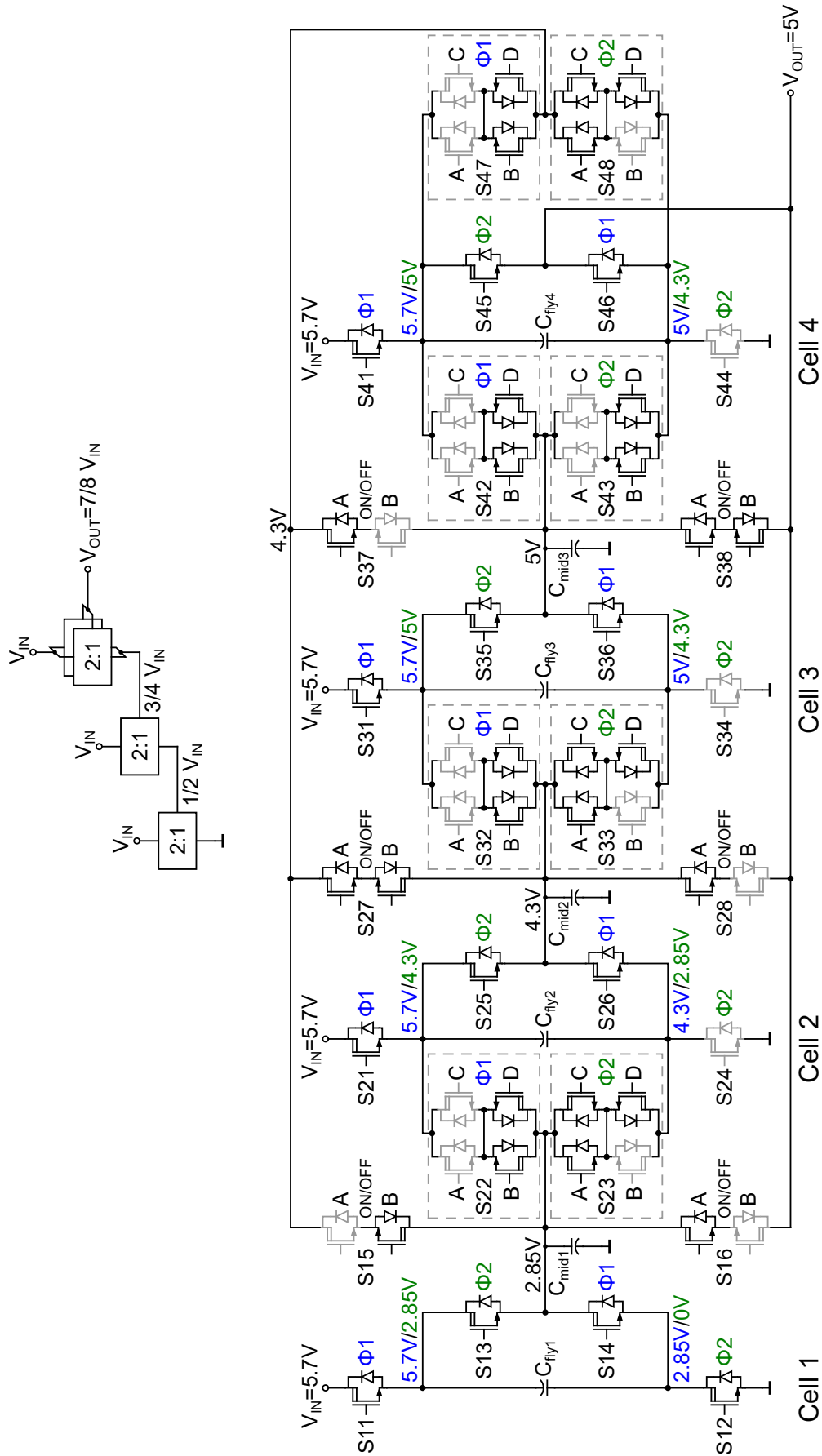


Fig. A.2: Power stage implementation of the recursive buck-boost SC converter in 14/16 ratio configuration.

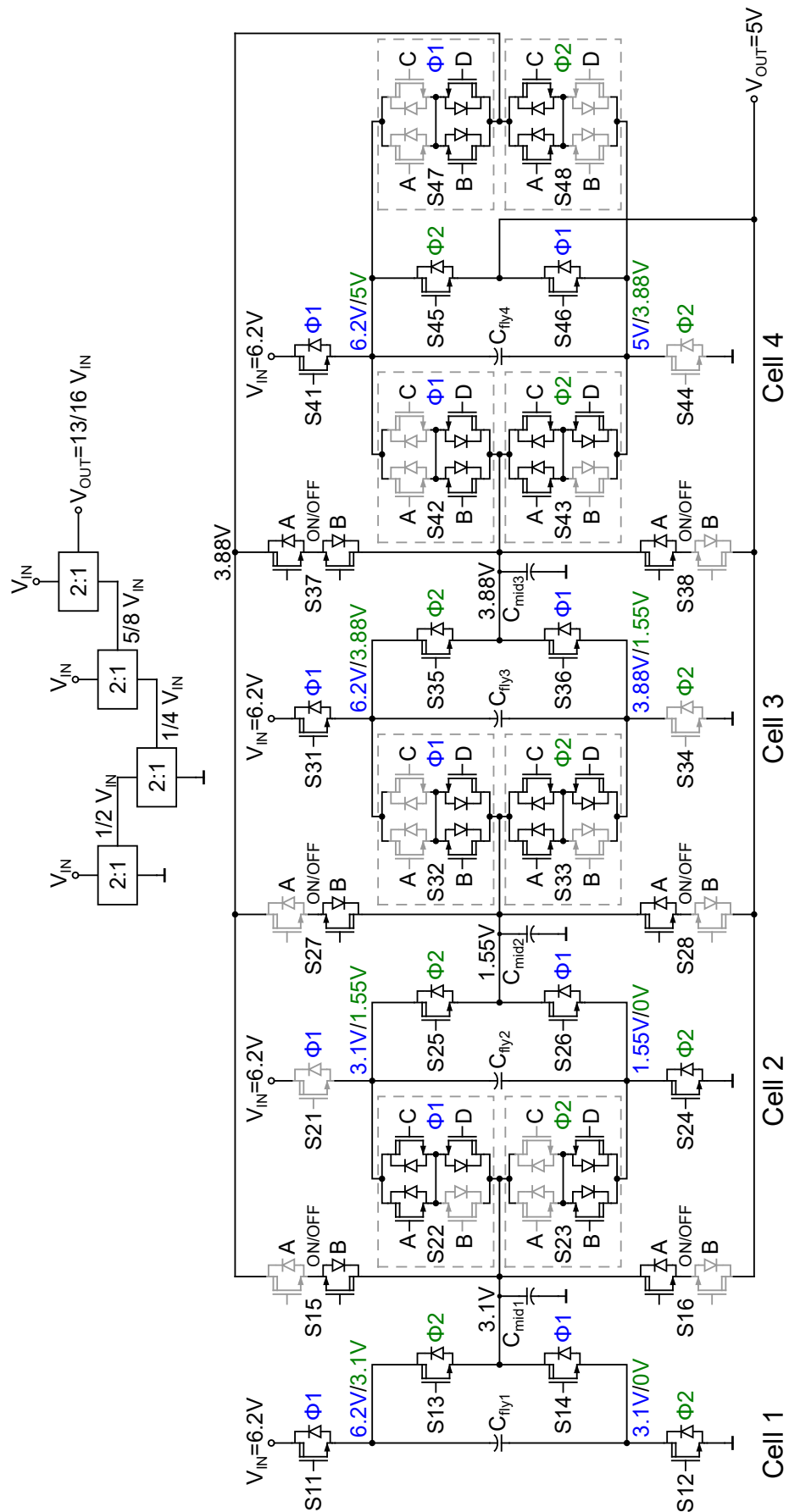


Fig. A.3: Power stage implementation of the recursive buck-boost SC converter in 13/16 ratio configuration.

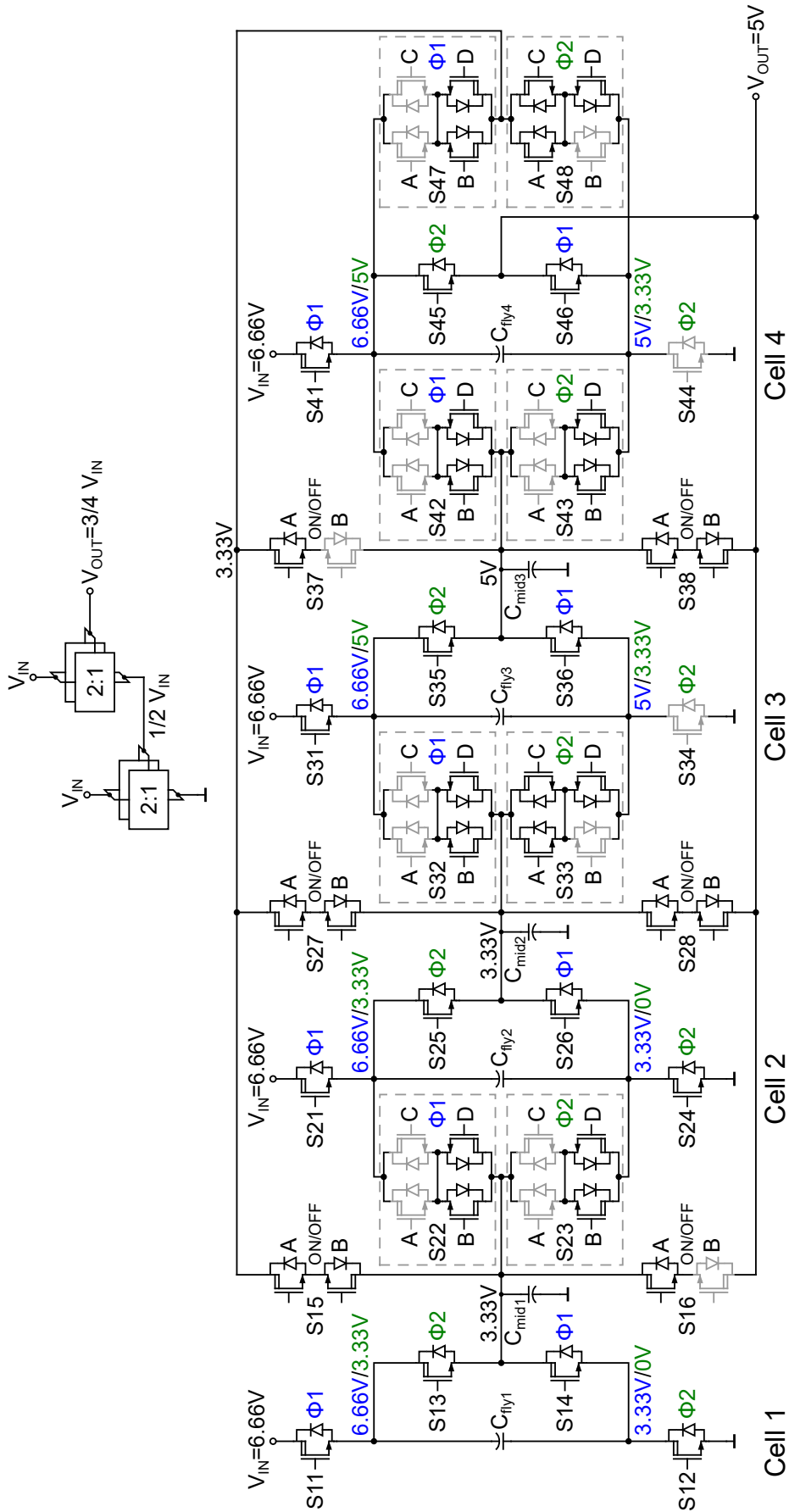


Fig. A.4: Power stage implementation of the recursive buck-boost SC converter in 12/16 ratio configuration.

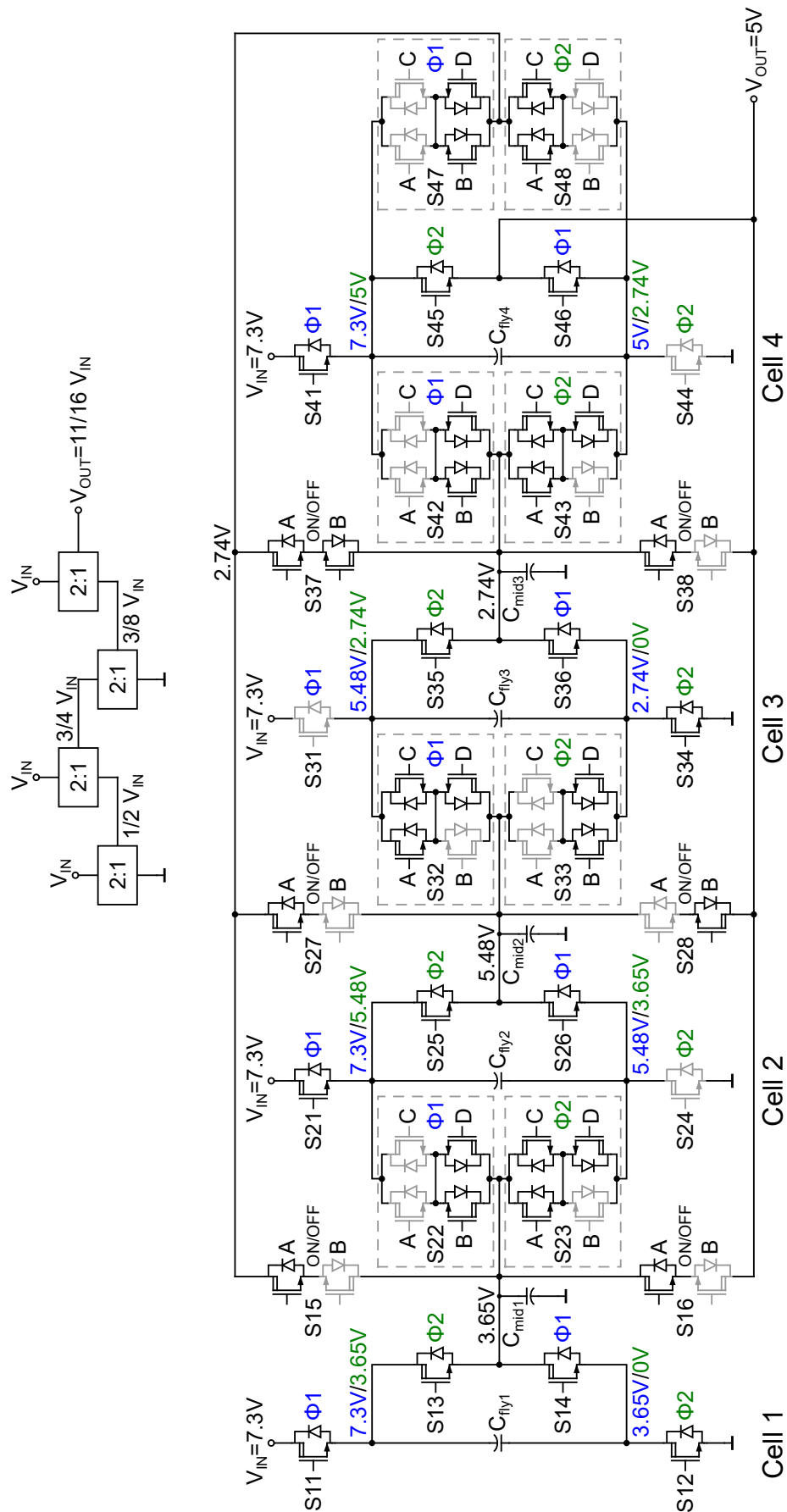


Fig. A.5: Power stage implementation of the recursive buck-boost SC converter in 11/16 ratio configuration.

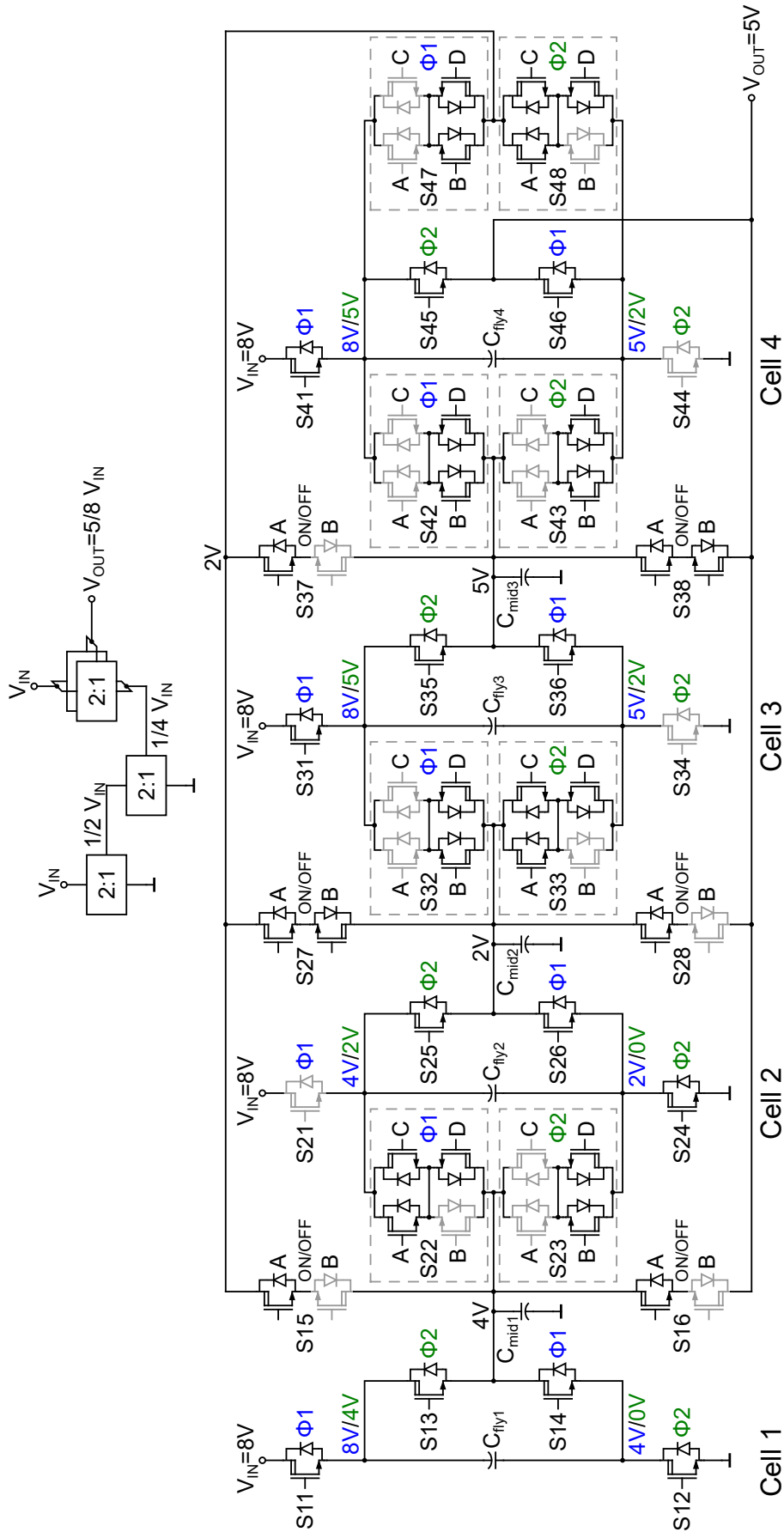


Fig. A.6: Power stage implementation of the recursive buck-boost SC converter in 10/16 ratio configuration.

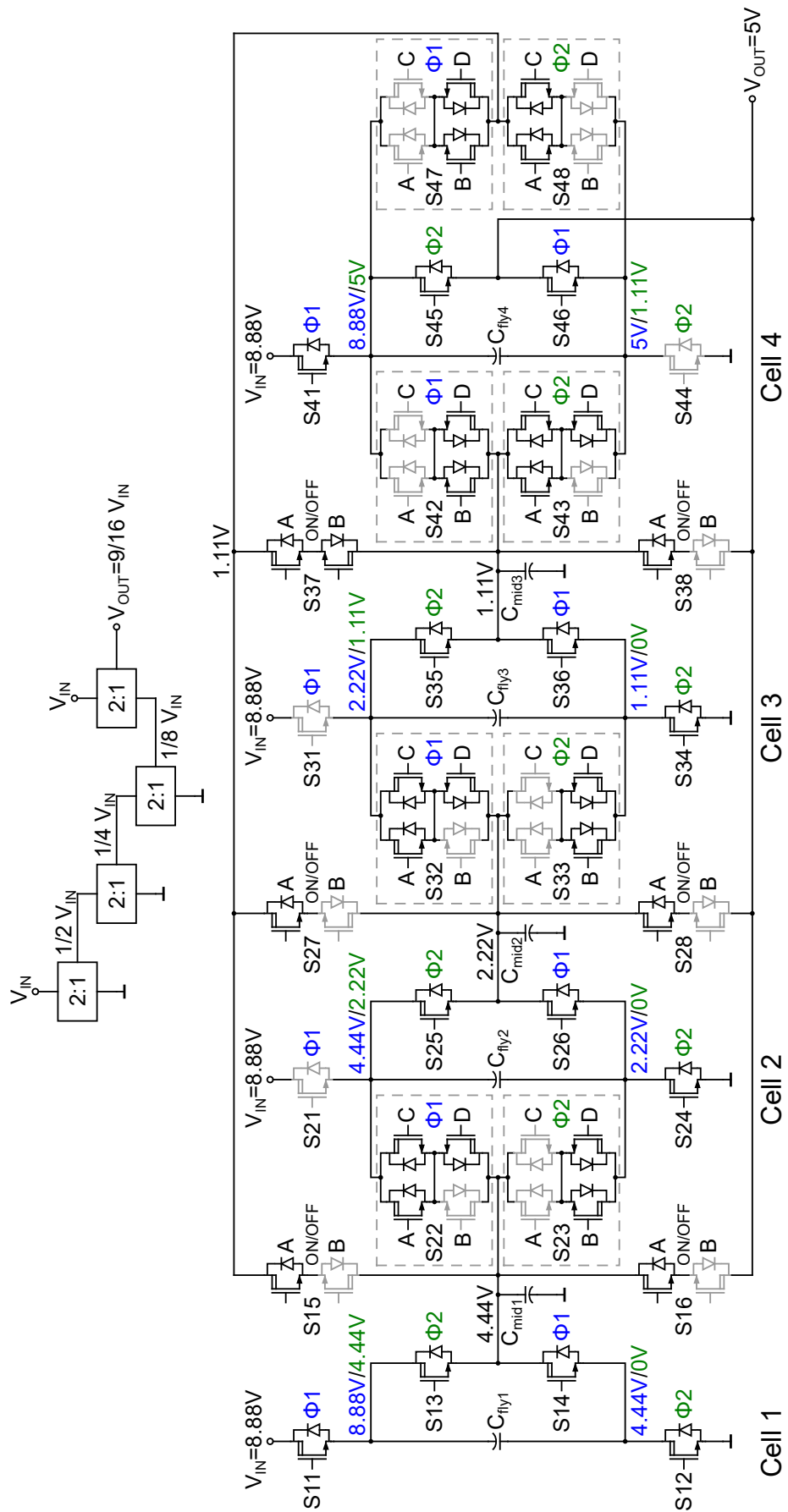


Fig. A.7: Power stage implementation of the recursive buck-boost SC converter in 9/16 ratio configuration.

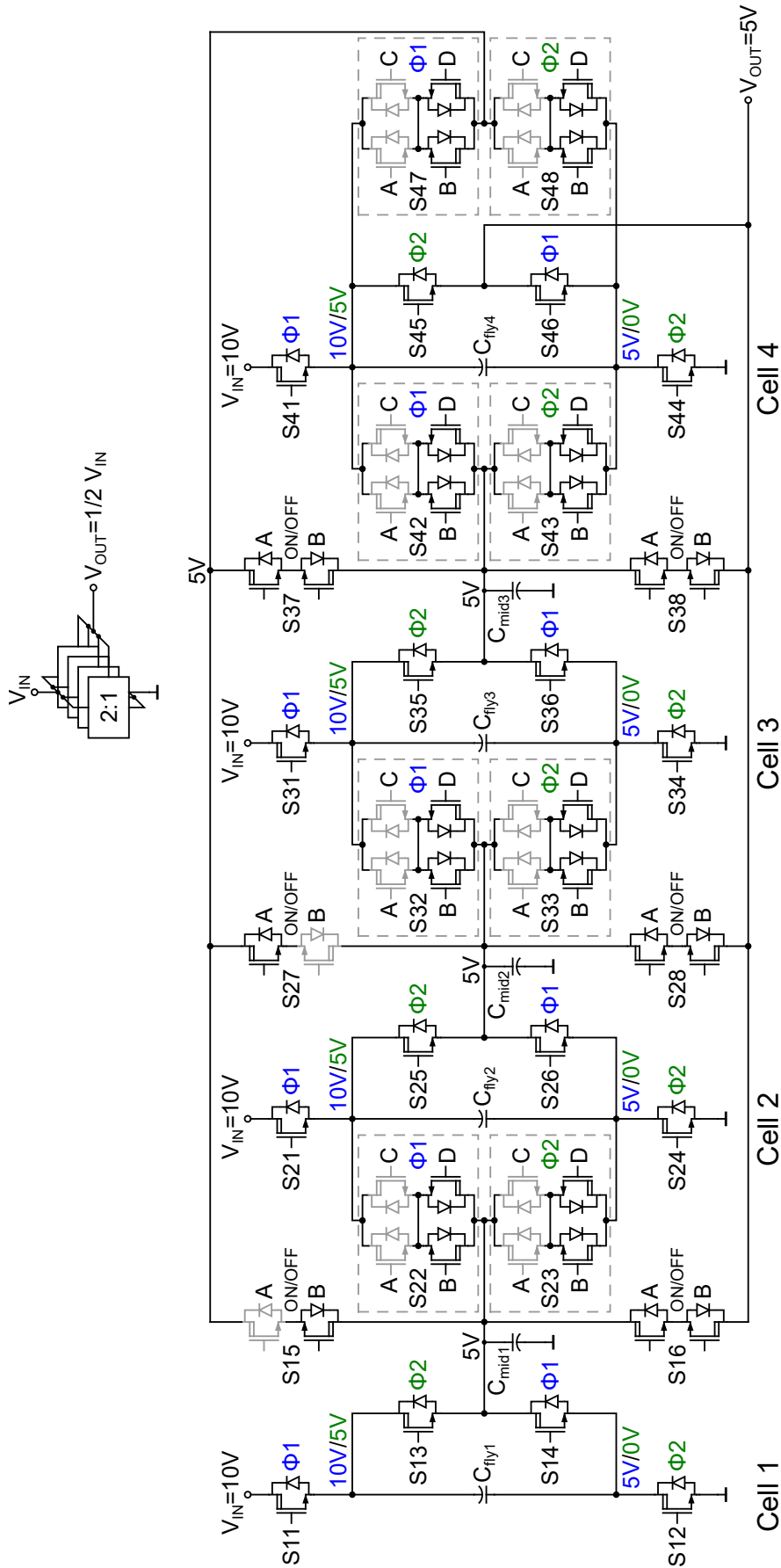


Fig. A.8: Power stage implementation of the recursive buck-boost SC converter in 8/16 ratio configuration.

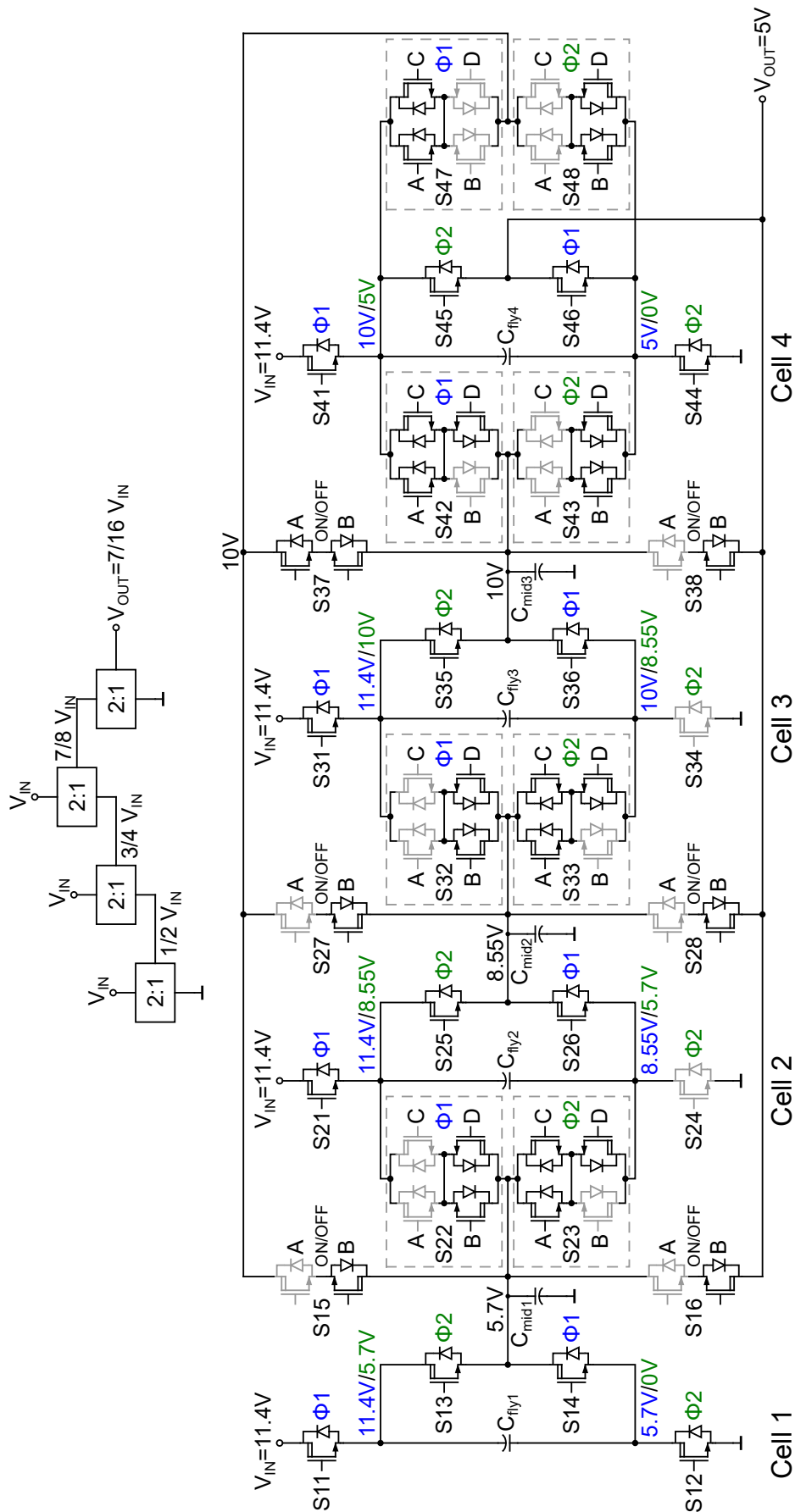


Fig. A.9: Power stage implementation of the recursive buck-boost SC converter in 7/16 ratio configuration.

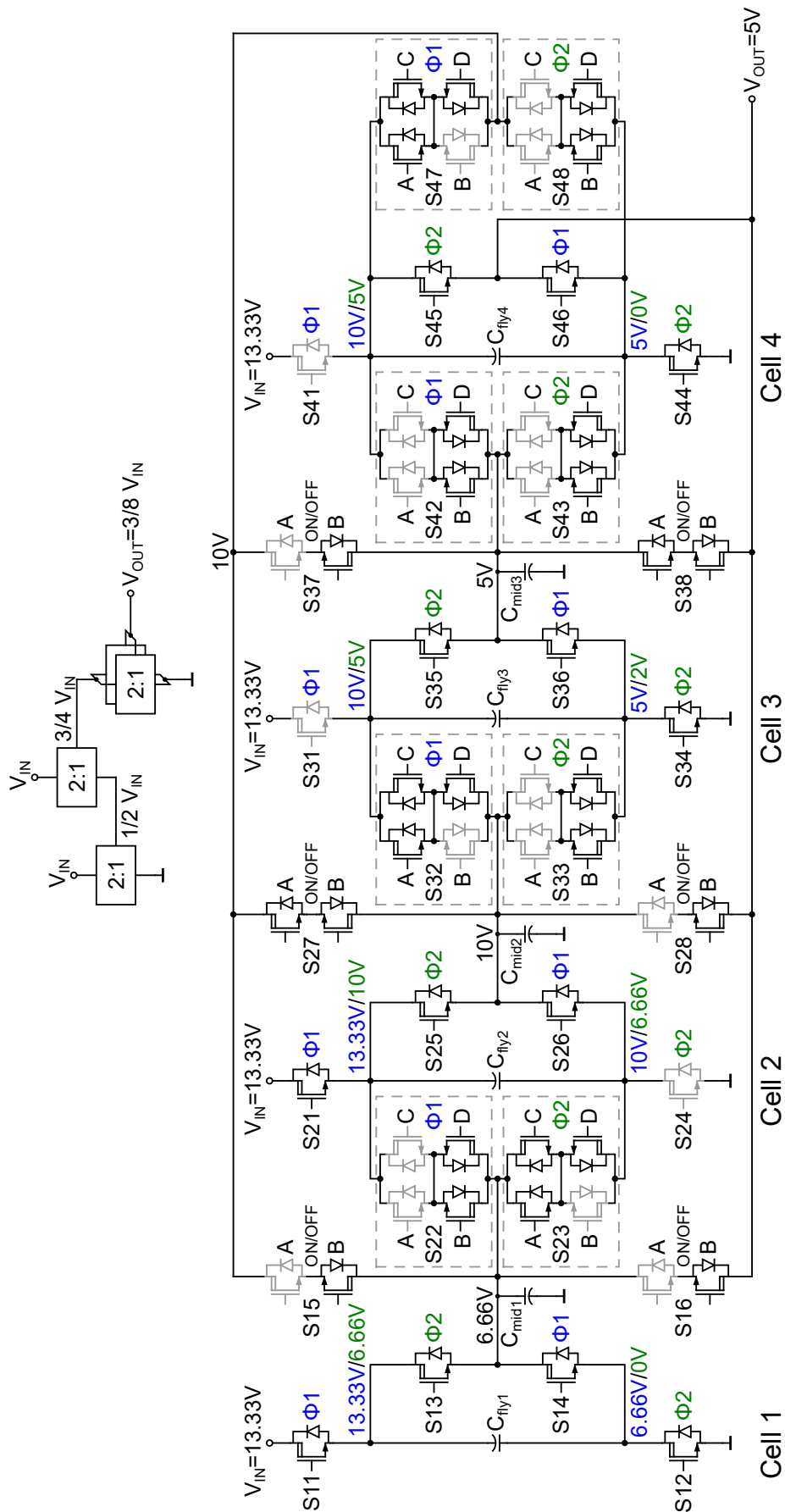


Fig. A.10: Power stage implementation of the recursive buck-boost SC converter in 6/16 ratio configuration.

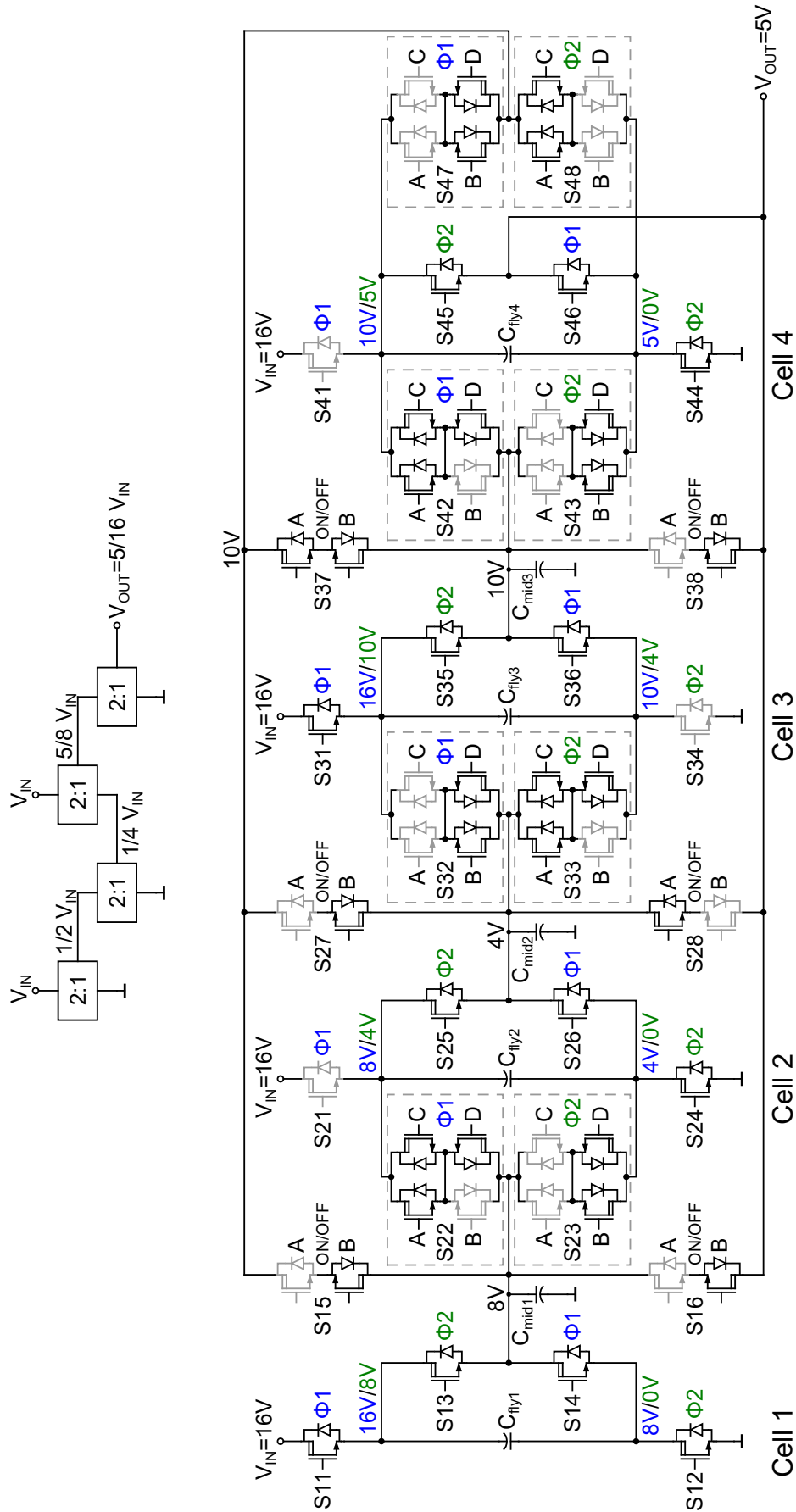


Fig. A.11: Power stage implementation of the recursive buck-boost SC converter in 5/16 ratio configuration.

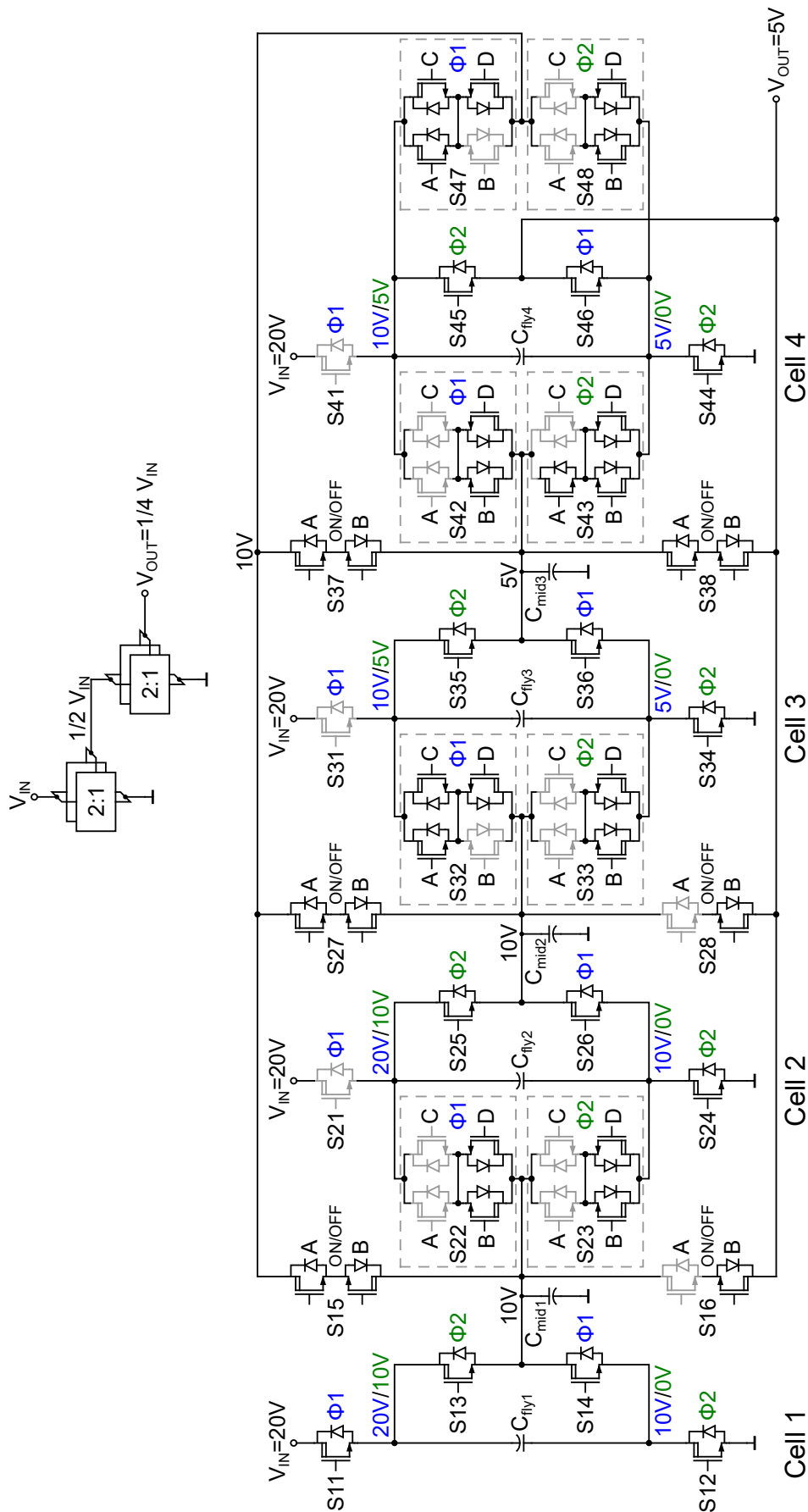


Fig. A.12: Power stage implementation of the recursive buck-boost SC converter in 4/16 ratio configuration.

B High-Voltage Three-Phase 1/15 SC Converter Topology

Figure B.13 shows the optimized three-phase SC converter (see Fig. 3.12) phase configuration of the three phases. The parameters resulting from the charge flow analysis (see Section 2.3) are shown in Table B.2. The table shows also the voltage ratings of the capacitors C_1 to C_5 and the voltage swing of these capacitor bottom plate contacts normalized to the output voltage V_{out} . The charge flow vectors a_c^1 to a_c^3 (see (2.3)), which are nominated to q_{in} , are given for the three phases. The Table B.3 shows the drain-source voltages of the switches, which are normalized to V_{out} . The charge flow vectors a_r^1 to a_r^3 (see (2.4)) of the switches are normalized to q_{in} are shown as well.

Phase Configuration:

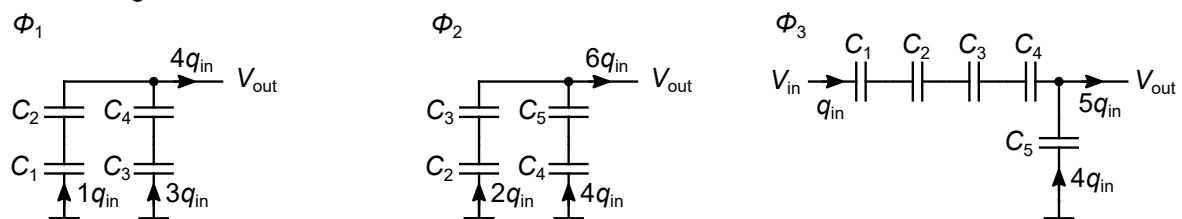


Fig. B.13: Phase configuration of the proposed three-phase SC converter of Fig. 3.12.

Tab. B.2: Voltage ratings of the flying capacitors

| | Normalized to: | C_1 | C_2 | C_3 | C_4 | C_5 |
|---------------|----------------|-------|-------|-------|-------|-------|
| V_C | V_{out} | 5 | 4 | 3 | 2 | 1 |
| $V_{BPswing}$ | V_{out} | 10 | 6 | 3 | 1 | 1 |
| a_c^1 | q_{in} | -1 | 1 | -3 | 3 | 0 |
| a_c^2 | q_{in} | 0 | -2 | 2 | -4 | 4 |
| a_c^3 | q_{in} | 1 | 1 | 1 | 1 | -4 |

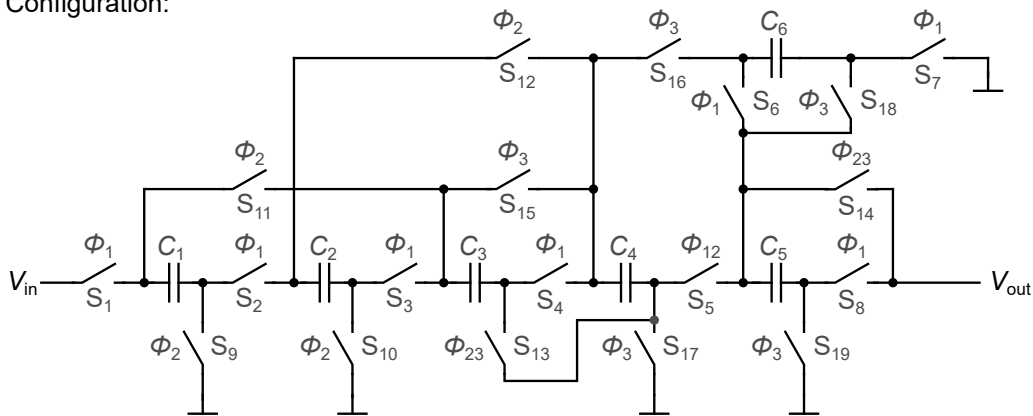
Tab. B.3: Voltage ratings of the switches

| | Normalized to: | S_1 | S_2 | S_3 | S_4 | S_5 | S_6 | S_7 | S_8 | S_9 | S_{10} | S_{11} | S_{12} | S_{13} | S_{14} | S_{15} | S_{16} | S_{17} | S_{18} | S_{19} | S_{20} |
|----------|----------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| V_{ds} | V_{out} | 10 | 5 | 1 | 1 | 3 | 1 | 1 | 4 | 1 | 1 | 2 | 1 | 10 | 5 | 4 | 3 | 1 | 1 | 5 | 2 |
| a_r^1 | q_{in} | 1 | 1 | 1 | 3 | 3 | 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 3 |
| a_r^2 | q_{in} | 0 | 0 | 0 | 0 | 0 | 0 | 2 | 2 | 2 | 4 | 4 | 4 | 0 | 0 | 0 | 0 | 0 | 0 | 2 | 2 |
| a_r^3 | q_{in} | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 4 | 4 | 0 | 0 |

C High-Voltage Three-Phase 1/16 SC Converter Topology

Due to the reduced number of capacitors, multi-phase SC converters are well suited for partial integration. Figure C.14 shows a three-phase SC converter topology with a ratio of 1/16. The topology is optimized in terms of voltage swing at the capacitor bottom plate switching nodes and the number of high-voltage components. Figure C.14 depicts the converter topology and the phase configuration. In Table C.4 and Table C.5 the parameters of the charge flow analysis described in Section 2.3 are shown. These parameters are normalized to V_{out} and q_{in} as described in Section B.

Switch Configuration:



Phase Configuration:

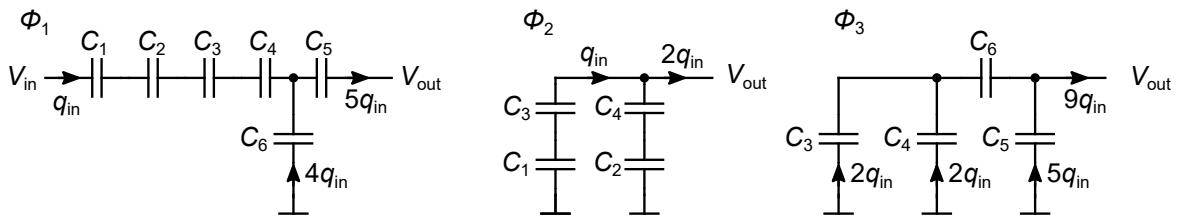


Fig. C.14: Switch and phase configuration of a high-voltage three-phase 1/16 SC converter topology.

Tab. C.4: Voltage ratings of the flying capacitors

| | Normalized to: | C ₁ | C ₂ | C ₃ | C ₄ | C ₅ | C ₆ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| V_C | V_{out} | 4 | 4 | 3 | 3 | 1 | 2 |
| $V_{BPswing}$ | V_{out} | 12 | 8 | 5 | 2 | 1 | 1 |
| a_c^1 | q_{in} | 1 | 1 | 1 | 1 | 5 | -4 |
| a_c^2 | q_{in} | -1 | -1 | 1 | 1 | 0 | 0 |
| a_c^3 | q_{in} | 0 | 0 | -2 | -2 | -5 | 4 |

Tab. C.5: Voltage ratings of the switches

| | Normalized to: | S ₁ | S ₂ | S ₃ | S ₄ | S ₅ | S ₆ | S ₇ | S ₈ | S ₉ | S ₁₀ | S ₁₁ | S ₁₂ | S ₁₃ | S ₁₄ | S ₁₅ | S ₁₆ | S ₁₇ | S ₁₈ | S ₁₉ |
|----------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| V_{ds} | V_{out} | 12 | 4 | 4 | 3 | 1 | 2 | 1 | 1 | 12 | 8 | 8 | 7 | 3 | 1 | 3 | 3 | 2 | 2 | 1 |
| a_r^1 | q_{in} | 1 | 1 | 1 | 1 | 1 | 4 | 4 | 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| a_r^2 | q_{in} | 0 | 0 | 0 | 0 | 2 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 2 | 0 | 0 | 0 | 0 | 0 |
| a_r^3 | q_{in} | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 | 9 | 2 | 4 | 4 | 4 | 5 |

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List of Abbreviations

| | |
|---------------|---|
| AC-DC | Alternating Current to Direct Current |
| CMOS | Complementary Metal Oxide Semiconductor |
| CMDC | Common Mode Displacement Current |
| DC | Direct Current |
| DC-DC | Direct Current to Direct Current |
| DMOS | Double Diffused Metal Oxide Semiconductor |
| FOM | Figure of Merit |
| FSL | Fast Switching Limit |
| IC | Integrated Circuit |
| IoT | Internet of Things |
| iVCR | Ideal Voltage Conversion Ratio |
| LDO | Low-Dropout Regulator |
| MIM | Metal-Insulator-Metal |
| MOM | Metal-Oxide-Metal |
| MOS | Metal Oxide Semiconductor |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| NMOS | N-Channel Metal Oxide Semiconductor |
| PCB | Printed Circuit Board |
| PFM | Pulse-Frequency Modulation |
| PMOS | P-Channel Metal Oxide Semiconductor |
| RF | Radio Frequency |
| RMS | Root Mean Square |
| RSC | Recursive Switched-Capacitor |
| SC | Switched-Capacitor |
| SiP | System-In-Package |
| SMD | Surface-Mounted Device |
| SMPS | Switch-Mode Power Supply |
| SoC | System-On-Chip |

| | |
|------------|-------------------------------|
| SOI | Silicon-On-Insulator |
| SOS | Silicon-On-Sapphire |
| SSL | Slow Switching Limit |
| VCO | Voltage Controlled Oscillator |
| VCR | Voltage Conversion Ratio |

List of Symbols

| | | |
|----------------------|--------------|--|
| $a_c^{(j)}$ | | Charge flow vector for the capacitors |
| A_{active} | m^2 | Active area of a device |
| A_{cap} | m^2 | Occupied chip area by capacities |
| A_{chip} | m^2 | Chip area |
| $A_{\text{chip,SC}}$ | m^2 | Chip area dedicated to capacitors and switches |
| A_{passive} | m^2 | Passive area of a device |
| $a_r^{(j)}$ | | Charge flow vector for the power switches |
| A_{sw} | m^2 | Occupied chip area by switches |
| C | F | Capacitor |
| C_B | F | Buffer capacitor |
| C_{bp} | F | Parasitic bottom-plate capacitance of a capacitor C |
| C_{cn} | F | Channel n-well junction capacitance of a PMOS capacitor |
| C_{fly} | F | Flying capacitor of a SC converter |
| C_{fly1} | F | Flying capacitor of a SC converter |
| C_{fly2} | F | Flying capacitor of a SC converter |
| C_{fly3} | F | Flying capacitor of a SC converter |
| C_{fly4} | F | Flying capacitor of a SC converter |
| C_{gate} | F | Gate capacitance of a transistor |
| C_j | F | Junction capacitor |
| CLK | Hz | Clock frequency |
| $C_{\text{n-well}}$ | F | Parasitic substrate capacitance of a negative doped isolation well |
| C_{mid} | F | Buffer capacitor of a SC converter |
| C_{mid1} | F | Buffer capacitor of a SC converter |
| C_{mid2} | F | Buffer capacitor of a SC converter |
| C_{mid3} | F | Buffer capacitor of a SC converter |
| C_{m1n} | F | Parasitic metal 1 to n-well capacitance |
| C_{off} | F | Coupling capacitor of the level shifter |
| C_{on} | F | Coupling capacitor of the level shifter |

List of Symbols

| | | |
|-----------------|--------------------|--|
| C_{out} | F | Output capacitor |
| C_{oxide} | F/m ² | Oxide capacitance density of a MOS transistor |
| C_p | F | Pump capacitor of the charge pump |
| $C_{fly,total}$ | F | Total assigned capacitance value to flying capacitor of a SC converter |
| C_s | F | Storage capacitor of the charge pump |
| C_{tp} | F | Parasitic top-plate capacitance of a capacitor C |
| c_x | fF/um ² | Capacity density of integrated capacitor |
| E_t | J | Energy per transition |
| f_{cp} | Hz | Switching frequency of the charge pump |
| f_{mains} | Hz | Mains frequency |
| f_{sw} | Hz | Switching frequency of the power stage |
| G_{cap} | | Weighting vector for the area distribution of the capacitors |
| G_{sw} | | Weighting vector for the area distribution of the switches |
| I_{basis} | A | Basis current of the bipolar Transistor |
| I_C | A | Capacitor current |
| $I_{collector}$ | A | Collector current of the bipolar Transistor |
| I_{in} | A | DC-DC converter input current |
| $I_{in,avg}$ | A | DC-DC converter average input current |
| I_{load} | A | Input current |
| I_{out} | A | Output current of a switched-capacitor (SC) converter |
| I_{peak} | A | Peak current |
| L | um | Transistor gate length |
| n | | Number of arbitrary elements |
| OL_{cap} | | Ratio of active area to component area for capacitors |
| OL_{sw} | | Ratio of active area to component area for switches |
| P_{cap} | W | Charging and discharging losses of a capacitance |
| P_{Cbp} | W | Charging losses of a parasitic bottom-plate capacitance C_{bp} |
| P_{CP} | W | Losses caused by the charge pump circuit |
| P_{ctrl} | W | Switch control losses including P_{LS} , P_{CP} and P_{GD} |
| P_{gate} | W | Charging and discharging losses of the transistor gate capacitance |
| P_{GD} | W | Losses caused by a gate driver circuit |
| P_{loss} | W | Power losses |
| P_{LS} | W | Losses caused by a level shifter circuit |
| P_{out} | W | Output power |
| $P_{out,max}$ | W | Maximum output power |

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| P_{Rp} | W | Extrinsic losses of the SC converter model |
| P_{Rout} | W | Power dissipation at output resistor R_{out} |
| P_{Rp} | W | Power dissipation at resistor R_p , which models the extrinsic losses |
| $P_{sw,ctrl}$ | W | Switch control losses including P_{gate} , P_{LS} , P_{CP} and P_{GD} |
| P_{well} | W | Charging losses of the isolation n-well |
| q_{in} | C | Charge flowing into the system |
| q_{out} | C | Charge flowing from the system |
| Q_{total} | C | Total amount of charge delivered in one cycle to the charge pump output |
| R_A | Ω | Resistor A of the back-to-back circuit |
| R_B | Ω | Resistor B of the back-to-back circuit |
| R_{bias} | Ω | Resistor for well biasing |
| R_C | Ω | Resistor C of the back-to-back circuit |
| R_D | Ω | Resistor D of the back-to-back circuit |
| $R_{dynamic}$ | Ω | On-resistance of the fast switching back-to-back transistor |
| R_{FSL} | Ω | Fast switching limit impedance of a SC converter |
| R_{on} | Ω | On-resistance of a power-switch in a converter |
| $R_{on,total}$ | Ω | Total on-resistance of the proposed back-to-back circuit |
| R_{out} | Ω | Output resistor, which represents the intrinsic losses in the SC converter model |
| R_p | Ω | Parallel resistor, which represents the extrinsic losses in the SC converter model |
| R_{SSL} | Ω | Slow switching limit impedance of a SC converter |
| R_{static} | Ω | On-resistance of the slow switching back-to-back transistor |
| rx | Ωum^2 | Specific sheet resistance of integrated resistor |
| S_{14} | | Power switch within the first cell of the proposed SC converter |
| t_{gap} | s | Time which is defined by $t_2 - t_1$ |
| t_1 | s | Time when $V_{in} = V_{clamp}$ |
| t_2 | s | Time when $V_{in} = V_{clamp} - \Delta V$ |
| V_{bias} | V | Biasing voltage |
| V_{blank} | V | Active blanking control signal |
| V_{BS} | V | Bulk-source voltage of a transistor |
| V_{clamp} | V | Clamping voltage, which defines the output voltage of the AC-DC power stage |
| V_{Cbp} | V | Bottom plate voltage of C_{fly1} |
| V_{DB} | V | Drain-bulk voltage of a transistor |
| V_{DDL} | V | Low-side supply voltage |
| V_{DDH} | V | High-side supply voltage |

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|------------------|---------------|--|
| V_{DG} | V | Drain-gate voltage of a transistor |
| V_F | V | Voltage drop of a diode |
| V_{GS} | V | Gate-source voltage of a transistor |
| V_{in} | V | Input voltage |
| $V_{in,AC}$ | V | Input voltage |
| $V_{in,RMS}$ | V | Input voltage of the alternating current to direct current (AC-DC) power stage |
| V_{mid1} | V | Voltage over C_{mid1} of the recursive buck-boost SC converter power stage |
| V_{out} | V | Output voltage |
| $V_{out,AC}$ | V | Output voltage of the AC-DC power stage |
| $V_{out,ideal}$ | V | Ideal output voltage of a SC converter |
| $V_{pulse,off}$ | V | Input voltage node of the sense block |
| $V_{pulse,on}$ | V | Input voltage node of the sense block |
| V_{RMS} | V | Root-Mean-Square voltage |
| V_{SSL} | V | Ground potential |
| V_{SSH} | V | High-side ground voltage |
| V_{swing} | V | Voltage swing at a node of the SC converter |
| $V_{S14,SD}$ | V | Source-drain voltage of power switch S_{14} |
| V_x | V | Voltage of the bottom plate of C_p of the source-supplied charge pump. |
| V_1 | V | Input / output voltage of the recursive buck-boost SC converter power stage |
| V_2 | V | Input / output voltage of the recursive buck-boost SC converter power stage |
| W | μm | Transistor gate width |
| xr | | Proportion of switch area to total chip area |
| xc | | Proportion of capacitor area to total chip area |
| α | | Quality factor of on-chip integrated capacitors |
| β | | Current amplification of a bipolar transistor |
| ΔI_L | A | Current ripple of the inductor current |
| ΔV_C | V | Voltage ripple of the capacitor voltage |
| ΔV | V | Voltage difference |
| ΔV_{bp} | V | Voltage swing of a capacitor bottom plate |
| ΔV_{out} | V | Output voltage ripple |
| ΔV_S | V | Voltage difference between phases ϕ_1 and ϕ_2 of the switching node |
| η | | Efficiency |
| η_{DC-DC} | | DC-DC converter efficiency |
| ϕ_1 | | Clock phase one |
| ϕ_2 | | Clock phase two |

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Patents

"Vorrichtung und Verfahren zum elektrischen Verbinden und Trennen zweier elektrischer Potentiale sowie Verwendung der Vorrichtung"("Apparatus and Method for Electrically Connecting and Disconnecting Two Electrical Potentials, and Use of the Apparatus"), publication date: 02. Mar. 2017, patent numbers: DE102015011396, WO/2017/036592.

Awards

IEEE Journal of Emerging and Selected Topics in Power Electronics - 2019 First Place Prize Paper Award

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List of Master Theses Supervised by the Author

- Yasin Karınca: *Integrierter kapazitiver 1mW Low-Power DC-DC Wandler mit variabler Eingangsspannung bis 10V*
- Peter Renz: *Vollintegrierter kapazitiver Low-Power DC-DC Wandler mit 5-20V Eingangsspannungsbereich*
- Florian David: *Regelung für einen vollintegrierten kapazitiven Low-Power DC-DC Wandler*
- Dominik Ruoff: *Vollintegrierte kapazitive Hochvolt-Spannungswandler für 230V Mikronetzeile*

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