Dual-Loop Gate Drivers with Analog and Digital Slope Shaping

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Abstract

Setting the values of the switching transients ($\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$) has become more and more important especially for modern power semiconductor technologies, like insulated gate bipolar transistors (IGBTs) in the newest trench-/fieldstop technologies, Superjunction MOSFETs or silicon carbide (SiC). The extremely fast switching speeds of these devices have led to switching losses of almost close to zero, but has also complicated the control of voltage and current spikes or electromagnetic compatibility (EMC) in switched applications like motor drives, switched-mode power supplies (SMPS) and power factor correction (PFC) stages. The focus of this work is on a new hardware concept for an active gate driver that is capable of flexible switching behavior optimization by using a dual-loop approach. This enables regulated $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ transients to be optimal for specific application requirements. Conventional gate drivers, as used in most commercial products, are commonly designed in passive architectures and are therefore unsuitable for an effective and flexible optimization of the switching behavior, due to their limited capabilities to influence the switching transients ($\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$). Closed-loop gate drivers offer a sophisticated approach to achieve a desired trade-off between switching losses, delay, EMC and safe operating area (SOA) and can be realized in the analog or in the digital domain. The dual-loop design adressed in this work comprises both analog and digital closed-loop control on $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$. Hence, it combines high speed and linearity of a closed-loop analog gate driver, that is able to perform continous-time regulation, with the advantages of adaptive digital control, like flexibility and parameter independency.

As the analog loop is the critical element, setting the dynamics and stability of the system, it is modeled and analyzed in the small-signal domain with focus on non-linearity of parameters and operating point dependencies. The model parameters are extracted from experimental data for an IGBT and a Superjunction MOSFET. Major parameters of influence, such as gate resistor and the capacitance in the summing node, are investigated to achieve stable control. Another important detail is the sensing of $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ to generate input data for the signal processing blocks of the digital loop. This guarantees for accurate interaction between the analog and the digital loop. The sensing blocks are optimized for accuracy and bandwidth. Different circuit concepts for the gate driver are evaluated and the full system is designed in hardware. Experimental results show that the combination of a digital and an analog loop increases the accuracy of the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ control compared to a pure analog loop system by more than 10%, independent of the actual device technology utilized. Precise slew rate control is demonstrated for IGBT,

Superjunction MOSFET and SiC.

Due to the device-independency, the gate driver enables the flexible use of different device technologies in a given application. The more accurate control helps to control voltage and current overshoots. In motor drives, the control of $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ helps to protect the motor from destruction and therefore increases the lifetimes.

Index terms: Slope shaping, gate drivers, multi-loop control

Zusammenfassung

Die Einstellbarkeit der Schalttransienten ($\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ und $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$) gewinnt heutzutage erheblich an Bedeutung, insbesondere bei der Nutzung moderner Leistungshalbleiter-Technologien wie Trench-/Fieldstop-IGBTs, Superjunction MOSFETs oder Siliziumkarbid (SiC). Die extrem schnellen Schaltflanken dieser Bauelemente haben zwar die Schaltverluste auf ein Minimum reduziert, jedoch gleichzeitig die Kontrolle über Strom- und Spannungsspitzen sowie elektromagnetischer Verträglichkeit (EMV) in geschalteten Anwendungen wie Motorantrieben, Schaltnetzteilen (Switched-Mode Power Supplies, SMPS) oder Leistungsfaktorkorrekturstufen (Power Factor Correction, PFC) zum Teil deutlich erschwert. Der Schwerpunkt dieser Arbeit liegt auf einem neuartigen Hardware-Konzept für einen aktiven Gate-Treiber, der in der Lage ist, das Schaltverhalten durch Nutzung eines Dual-Loop-Ansatzes flexibel zu optimieren. Dieser ermöglicht über eine $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ und $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ – Regelung, die Schaltflanken auf anwendungsseitig vorgegebene Spezifikationen einzustellen. Konventionelle Gatetreiber, die in den meisten kommerziellen Produkten genutzt werden, weisen häufig eine passive Architektur auf, die hierfür aufgrund der begrenzten und unflexiblen Beeinflussbarkeit der Schalttransienten ungeeignet ist. Gatetreiber mit geschlossener Regelschleife, die entweder analog oder digital ausgeführt werden kann, bieten hingegen einen geschickten Ansatz, einen Kompromiss zwischen Schaltverlusten, Schaltverzögerungen, EMV sowie sicherem Betriebsbereich (safe operating area, SOA) herzustellen. Das Dual-Loop-Design in dieser Arbeit beinhaltet sowohl eine analoge als auch eine digitale geschlossene Regelschleife für $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ und $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$. Hierdurch wird die hohe Regelgeschwindigkeit und Linearität der analogen Regelung, die zeitkontinuierlich aktiv ist, mit den Vorteilen einer adaptiven digitalen Regelung, wie Flexibilität und Parameterunabhängigkeit, kombiniert. Da die analoge Regelschleife das kritische Element ist, das die Dynamik und Stabilität des Gesamtsystems festlegt, wird diese mit Hilfe eines Kleinsignalansatzes modelliert und analysiert, mit dem besonderen Fokus auf nichtlinearen Parametern sowie Arbeitspunktabhängigkeiten. Die Modellparameter werden dabei am Beispiel eines IGBT und eines Superjunction MOSFETs aus experimentell gewonnenen Datensätzen extrahiert. Die Parameter mit größerem Einfluss auf Stabilität und Systemdynamik werden vorgestellt. Ein weiteres wichtiges Detail ist die Erfassung von $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ und $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ für die anschließende Signalverarbeitung in der digitalen Regelschleife. Diese Erfassung stellt die Genauigkeit im Zusammenspiel zwischen digitaler und analoger Regelschleife sicher. Aus diesem Grund wird die Messhardware in einem experimentellen Ansatz in ihrer Genauigkeit und Bandbreite optimiert. Mehrere Schaltungskonzepte für den Gatetreiber werden

vorgestellt, ausgewertet und in Hardware ausgelegt und hergestellt. Experimentelle Ergebnisse zeigen, dass die Kombination aus analoger und digitaler Regelscheife die Genauigkeit der $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ und $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ – Regelung im Vergleich zu einer rein analogen Regelschleife unabhängig vom eingesetzten Leistungshalbleiter um mindestens 10% erhöht. Die präzise Flankenregelung wird dabei für IGBT, Superjunction MOSFET und SiC nachgewiesen. Aufgrund der Unabhängigkeit vom verwendeten Bauelement ermöglicht der Gatetreiber den sicheren und flexiblen Einsatz verschiedener Technologien in einer vorgegebenen Anwendung. Die genauere Regelung unterstützt dabei, während des Schaltvorgangs auftretende Strom- und Spannungsspitzen im Griff zu halten. In Motorantrieben hilft die $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$-Regelung, den Motor vor Zerstörung zu schützen und damit die Laufzeiten zu erhöhen.

Schlagworte: Schaltflankenregelung, Gate-Treiber, Multi-Loop-Regelung

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Contents

1 Introduction

1.1 Introduction

The development of power semiconductor devices is mainly driven by the increasing need for electrical energy. One of the strongest driver is industrial power control (IPC), along with the upward trend to electric and hybrid electric vehicles (EV/HEV) and the increasing employment of electric motors in industry applications [1]. Hence, the growth of semiconductor devices is expected to continue for the next decades [2].

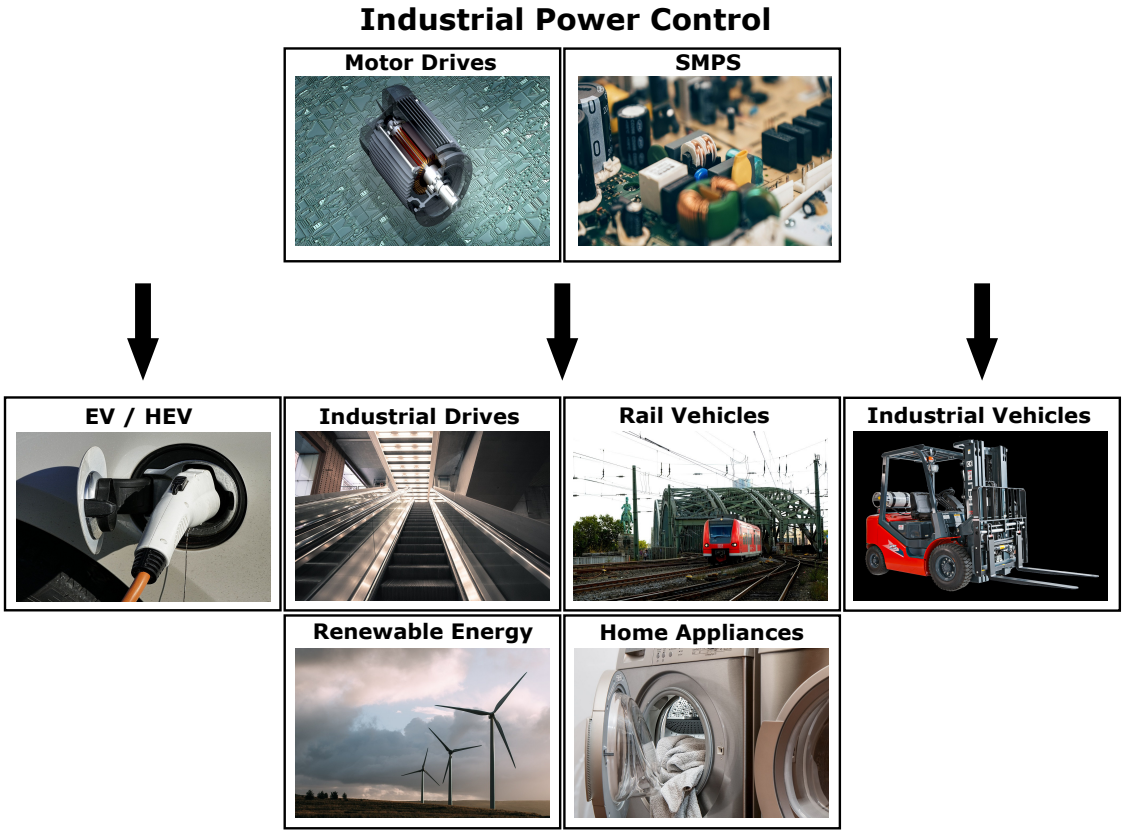


Fig. 1.1: Applications in industrial power control.

Industrial power control covers the conversion of electrical energy in medium and high power industrial applications. This comprises a wide power range, from refrigerators of some hundred watts up to 50 MW

natural gas compressors [3]. Typical applications that fall into this category, depicted in Fig. 1.1, include renewable energies (photovoltaic inverters and wind power stations), home appliances (inductive cooking, dishwashers, air-conditioning, washing machines, etc.), industrial vehicles (forklifts, constructional vehicles, electric buses, etc.), rail vehicles, uninterruptable power supplies (UPS) and industrial drives (e.g. in elevators or traction motors). As an example for the continuous growth, Fig. 1.2 shows an expected market analysis for applications employing IGBTs [4], one of the standard switching components in IPC. Beside the high volume automotive sector, a further big field are motor drive applications, for which a compound annual growth rate (CAGR) of 4.6% is expected until 2022. Significant increase is also expected for further applications, such as welding or home appliances, which are labeled in green labeled as "Others".

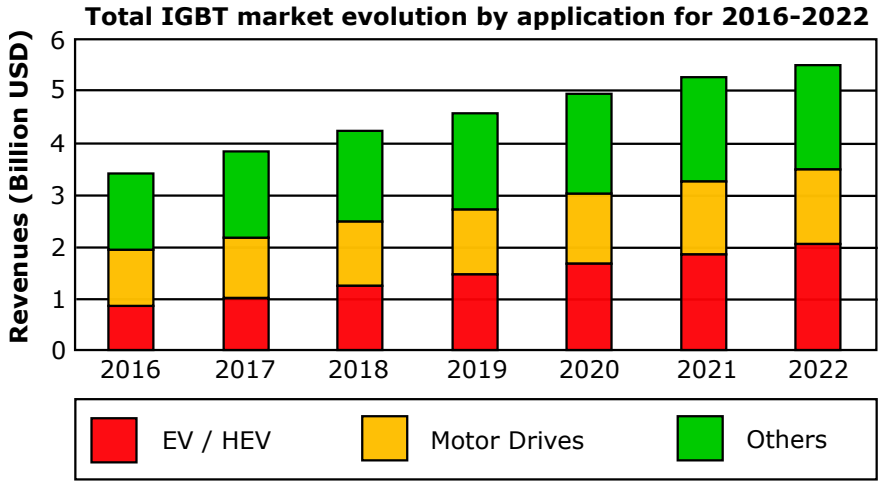


Fig. 1.2: IGBT market evolution by application until 2022 [4].

Induced by the increasing volumes, the demand for higher efficiencies in power conversion is growing to cope with the limited energy ressources. Hence, there is a rapid development in the existing silicon-based power semiconductor technologies, such as for insulated gate bipolar transistors (IGBTs) in newest trench-/fieldstop technologies [5–8], and for metal oxide semiconductor field-effect transistors (MOSFETs) [9] [10] . Furthermore, new device technologies based on wide-bandgap (WBG) semiconductors, in particular SiC, have emerged [11–15]. These trends have lead to devices with steadily increasing switching speeds, along with lower switching losses, and therefore to higher converter efficiencies. The slew rates of modern semiconductor devices (collector-emitter/drain source voltage derivative $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$, and collector/drain current derivative $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$) may reach 100 V/ns and 1 A/ns. However, these fast voltage and current transients have turned out to be critical, as they cause violations in electromagnetic interference (EMI) and lead to extremely high voltage and current spikes, which may cause damage or even destruction of the power device [16]. In some cases, including a high amount of parasitic inductance apparent in the system, these overshoots can exceed the nominal values by more than 100%.

In motor drives, the fast switching typically leads to a fast change in the voltage across the motor terminals (high $\mathrm{d}V/\mathrm{d}t$) . This can lead to destruction of the motor winding isolation due to partial discharge between the windings, and to destruction of the bearings due to displacement currents between rotor and stator [17] [18].
In order to achieve a suitable trade-off between the converter efficiency, switching delay times, EMC and SOA, gate drivers have to fulfill complex requirements [19]. The main task of gate drivers is to provide the appropriate energy to the gate of the semiconductor device in order to perform a full turn-on or turn-off transition. To achieve a desired trade-off, the transfer of charge to or from the gate has to be controlled, resulting in a limitation of the switching transients. However, conventional gate drivers have only limited technical capabilities in the independent control of both slew rates. Hence, there has been a trend to gate drivers with closed-loop slope shaping (closed-loop control of $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and/or $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$) in recent years [20]. Closed-loop slope shaping gate drivers are either implemented as digital or analog gate drivers, which refers to the domain of the individual slew rate control design. They exhibit several advantages over conventional drivers. Closed-loop analog gate drivers offer continous-time control and, therefore, both high linearity and operating point independency, but are prone to statistical variations, leading to inaccurate control, which may not be acceptable for the fast transients of modern devices. Furthermore, their regulation parameters usually need to be tuned to a target power device to achieve control stability, which is difficult due to the inflexible analog design.
In contrast, digital gate drivers are highly flexible and accurate, as they provide programmable control parameters and employ the concept of adaptive learning. However, due to limited processing speed, they typically do not come with continous-time control, especially not for fast-switching devices. Thus, they need to be operated in cycle-by-cycle mode.
The concept pursued in this work combines the advantages of analog control and digital control in a dual-loop approach. This enables precise and device-independent slope shaping, which is required to optimize the switching behavior of state-of-the-art power devices for multiple sets of application requirements.

1.2 Scope of this Work

The scope of this work, based on the presented trends in industrial power control, is summarized and depicted in Fig. 1.3. The rapid evolution towards faster power switches in multiple applications continously increases the requirements on slope shaping gate drivers, due to the faster transients and larger differences in technology between the individual devices.
By combining analog and digital control in a dual-loop gate drive concept, the gate driver is able to cope with the statistical variations in the parameter set. It can establish flexible, linear and precise closed-loop control

on the switching transients, independent of the actual power device. In this regard, the main challenges are the required accuracy and bandwidth in sensing of $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ for appropriate interaction between the analog and the digital loop, the required high precision in the control and to achieve stable closed-loop control independent of the power switch.
These challenges are adressed in this work as follows:

1. A small-signal model is created for the core blocks of the dual-loop gate driver. This is the basis for an analysis of dynamic stability. Requirements for reliable and stable control are derived.

2. A concept for sensing of $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ is developed and optimized in bandwidth and accuracy, both in theory and experimentally in hardware.

3. Circuit concepts for the analog and digital blocks are investigated, with respect to the requirements.

4. A hardware evaluation module is built up, to test and evaluate the proposed dual-loop concept in an arbitrary parameter set for different switches, and to compare it with an existing commercial gate driver.

1.3 Contribution of this Work

The contribution of this work is dedicated to a new hardware concept for an intelligent gate driver, that is capable of precise and device-independent slope shaping by using a dual-loop approach, combining the benefits of a closed-loop analog control with the advantages of a closed-loop digital control (see Fig. 3.1).
In detail, this work advances the state-of-the-art by the following contributions:

1. This work presents the first dual-loop concept in slope shaping, which consists of both analog and digital closed-loop control of $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$. The concept is developed in this work. Simulations and measurements made throughout this work show that the advantages of the two domains add up together in one concept. Due to the continous-time control of the analog loop, the system exhibits high linearity in the switching transients and independency on the operating point. The digital controller adaptively compensates for statistical variations in the switching speed of the driven switch, as well as for statistical variations of the analog loop. This leads to a precise $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ and $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ control, independent of the actual power device in use. The dual-loop approach has been presented at PRIME 2017 [22].

   The dual-loop concept can be further extended by a new anti-windup method proposed in this thesis, that prevents the analog loop during the periods without active $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ and $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback, which is during the switching delay, from reaching the voltage limitation. This is required for a higher linearity

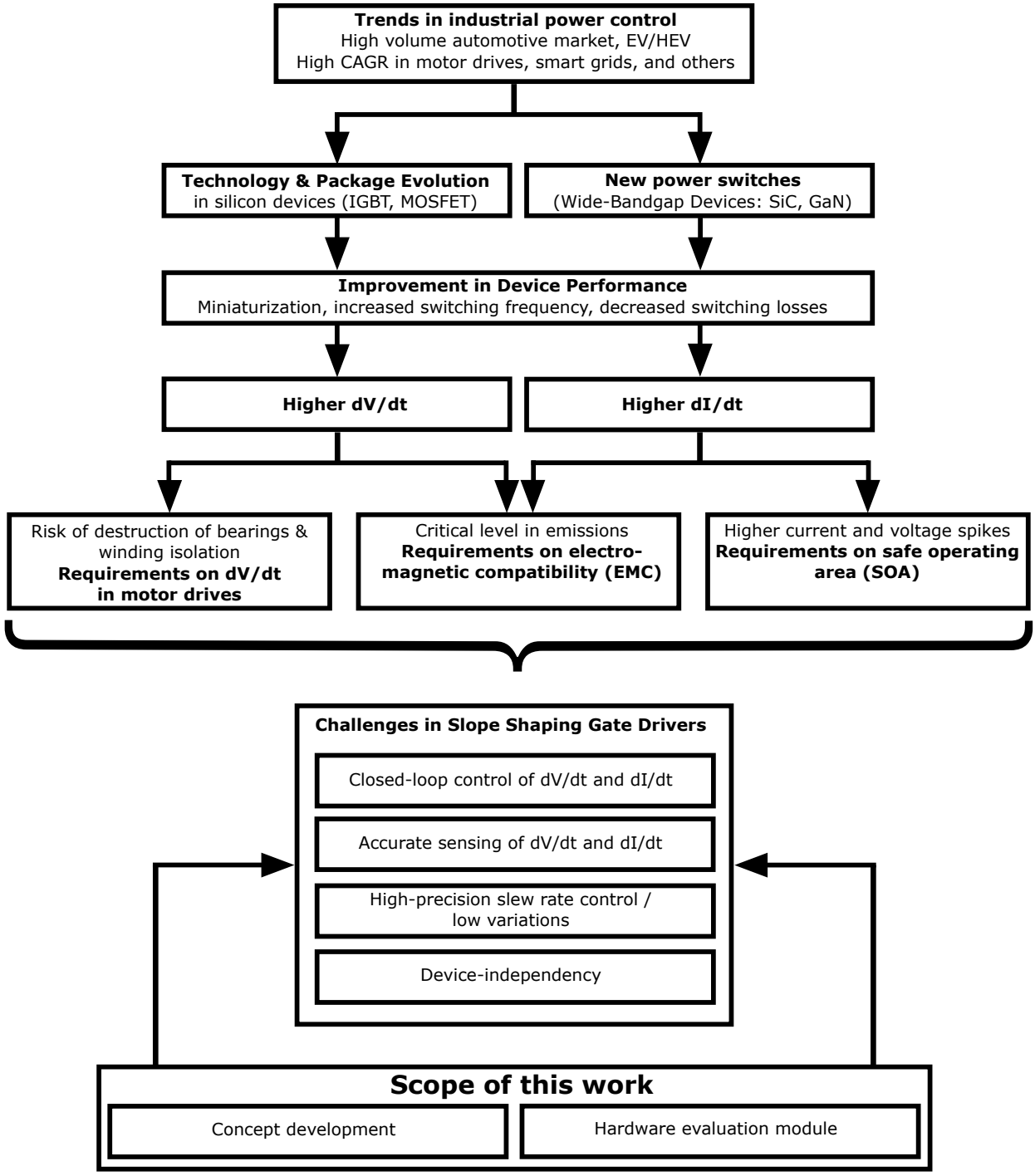


Fig. 1.3: Trends in industrial power control and scope of this work.

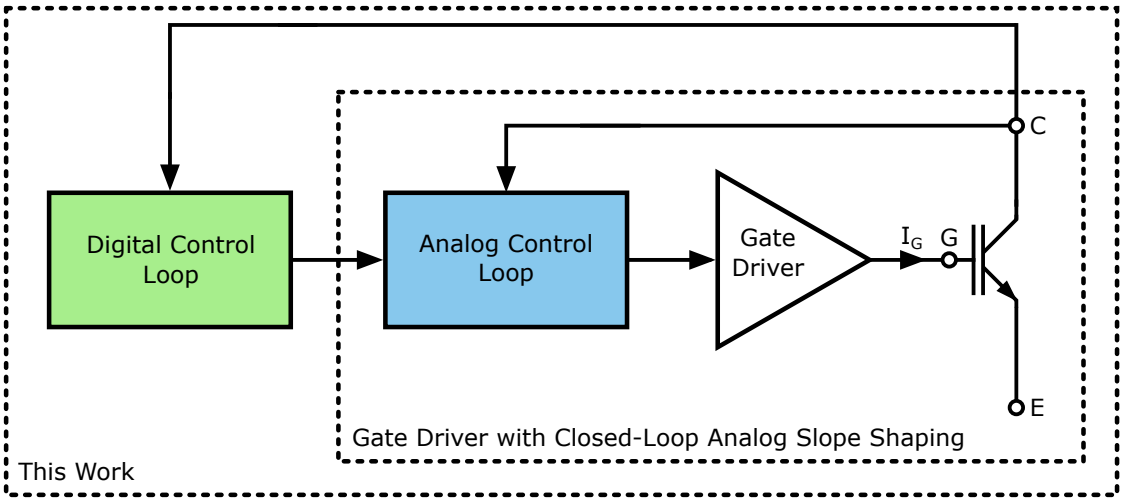


Fig. 1.4: This work: Dual-loop gate driver with combined digital and analog slope shaping.

in the beginning of the first transient, as it compensates for the windup-effect, which causes a non-linearity in parts of the slew rates. In contrast to the prior art anti-windup concepts, which control the gate current during the switching delay phases, the voltage slew rate at the output of the driver ($\mathrm{d}V_{\mathrm{out,drv}}/\mathrm{d}t$) is put in closed-loop control. Hence, the gate current level during the delay period adapts automatically if the power device is exchanged. The circuit can be designed with optional power-down switches to decrease the power consumption. The concept and circuitry referring to the anti-windup method have been filed as a patent application [23].

2. A requirement list for the slope shaping system, fitted to the application of motor drives, is provided. As part of this work, the dynamic stability of the gate driver core, represented by the analog closed-loop control of $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$, is investigated in an analytical stability analysis. For this purpose, the system is paritioned into functional blocks and modeled in the small-signal domain. In advance to prior small-signal approaches in slope shaping, the created model also includes the non-linearity of parameters, which are taken into account via curve-fits on actual switch parameters. It is shown for two different power switch types, an IGBT in trench-/fieldstop technology and a Superjunction MOSFET, that control stability is achieved independent of the actual power device. However, a further outcome of the stability analysis is that the main impact on the dynamics (maximum regulation bandwidth, etc.) is determined by the power device under control. The analysis shows that major parameters of influence, which can be controlled externally, are the gate resistor, the summing node capacitance and an optional voltage gain in the driver. The analysis of dynamic stability has been presented at PRIME 2017 [22].

3. An optimized concept for a $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ sensing circuitry is developed, which is required to guarantee for accurate interaction between the analog loop and the digital loop. In many state-of-

the-art slope shaping works, this is realized by monitoring the absolute values of V_{CE} and I_C [24]. However, better accuracy at lower DC power loss is achieved by sensing techniques for a reliable passive detection, which avoid any DC path from the high voltage network into the sensing network. The optimization of the sensing block is obtained by an experimental study based on equivalent circuit models including all relevant parasitics with effect on bandwidth and accuracy, which have been created in this work. The optimized sensing network supports all devices that exhibit fast $\mathrm{d}V_{CE}/\mathrm{d}t$ and $\mathrm{d}I_C/\mathrm{d}t$ up to 100 V/ns and 1 A/ns and beyond, making the sensing technique attractive for IGBTs, Superjunction MOSFETs and SiC. The sensing concept has been presented at APEC 2017 [25].

4. An experimental hardware evaluation module is implemented to investigate and verify the proposed circuit and system concepts. The full hardware realization of the dual-loop, in all its components, is presented in this work. The measurements demonstrate that the system is capable of the following features, advancing state-of-the-art concepts:

   - Linear slope shaping of the voltage and current transients, independent of the actual operating point (DC link voltage and load current) and temperature, which offers the possibility to optimize the switching behavior for a given application, and during operation. This has been verified in experiment using a new generation trench-/fieldstop IGBT with 600 V and 50 A rating, for a DC link voltage range of $V_{DC} = \{100\text{V} \,..\, 400\text{V}\}$ and a load current range of $I_{Load} = \{5\text{A} \,..\, 75\text{A}\}$.

   - Device-independent $\mathrm{d}V_{CE}/\mathrm{d}t$, $\mathrm{d}I_C/\mathrm{d}t$ control of various modern gate-controlled power semiconductor devices, demonstrated for three state-of-the-art power switches with voltage rating up to 1200 V: Trench-/fieldstop IGBT, Superjunction MOSFET (CoolMOS^{TM}), SiC.

   - Precise and linear slew rate control due to the combination of continous-time analog and adaptive digital closed-loop control. The setpoints of $\mathrm{d}I_C/\mathrm{d}t$ and/or $\mathrm{d}V_{CE}/\mathrm{d}t$ can be variably adjusted during operation up to more than 2 A/ns and 10 V/ns. They are reached by the adaptive controller in less than 10 switching cycles.

1.4 Outline

This section describes the structure of this work in its particular chapters.

Chapter 2 starts with an introduction into the fundamentals. In the beginning, the most important state-of-the-art power semiconductor devices are introduced and described in their key figures and applications. The switching mode of a gate-controlled device for inductive load switching, also referred to as hard switching,

is described. In addition, the essential ideas and operating principles of state-of-the-art gate drive concepts with slope shaping are depicted.

The dual-loop gate driver concept with both closed-loop analog and digital $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ control is investigated in Chapter 3. The first part contains an analytical small-signal stability analysis of the analog loop, which allows to derive requirements on the control parameters for stable operation. The small-signal analysis is confirmed and completed by a large-signal analysis in the transient domain. The next section elaborates the optimized sensing concept for $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$. Furthermore, the digital loop concept is depicted. Based on the system specifications, requirements for the circuit blocks are derived, with the main focus on motor drive applications.

Chapter 4 presents circuit concepts for the analog loop blocks. In the beginning, two concepts for the driver stage, source follower and common-source amplifier, are analyzed. Thereafter, a method for an anti-windup, which controls the slew rate of the driver output voltage ($\mathrm{d}V_{\mathrm{out,drv}}/\mathrm{d}t$), is shown. Furthermore, a $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback circuit for the analog closed-loop gate driver is designed.
As part of the following sections, the conceptual circuit blocks are inserted into the analog closed-loop, in order to further investigate and to verify the full functionality of the analog loop design in system simulations, which include a stability analysis and a verification of the performance parameters. In addition, the reference value of the analog control loop is varied in order to shape the switching slopes. By doing so, the minimum and maximum rates of $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ are identified. In the end of the chapter, the gate driver is compared to passive gate driver concepts.

Based on the concept analysis of the previous chapters, a hardware evaluation module is built up in Chapter 5, which comprises the full dual-loop slope shaping system. A discrete hardware design for the analog loop blocks is created, adressing the circuit concepts of Chapter 4. Afterwards, hardware for the digital loop is presented and connected to the analog loop. Measurement results prove the performance of the dual-loop gate driver, demonstrate the control of different power switches and compare the dual-loop gate driver with a commercial passive gate driver.

This work concludes with a summary and an outlook.

2 Fundamentals

2.1 Devices and Circuits in Power Electronics

2.1.1 Modern Generation Power Semiconductor Devices

Each application in power electronics comes along with individual requirements, which are the basis for a selection of a specific power semiconductor device, to achieve a reliable and robust behavior. Four different types of commercially available products, which exhibit an insulated gate electrode and can therefore be controlled by gate drivers, are listed in Table 2.1. The insulated gate bipolar transistor (IGBT) has become the standard switching component for lower or medium switching frequencies at high power densities [26]. IGBTs are able to cope with much higher power up to 6500 V and 3600 A, if they are used in modules. Due to their bipolar nature, they do not exhibit ohmic behavior when turned-on ($R_{DS,on}$), which leads to comparably lower on-state losses.
If the application demands for a higher switching frequency, Superjunction MOSFETs are employed. However, the silicon-based power MOSFETs are limited in power handling capability [27].

Tab. 2.1: Typical key performance parameters of modern commercial power semiconductor devices.

	IGBT Discretes	IGBT Modules	CoolMOS™	OPTIMOS™
V_{max} / V	600 - 1200	400 - 6500	500 - 950	30 - 250
I_{nom} / A	up to 120	up to 3600	up to 100	up to 300
f_{SW} / kHz	up to 60	up to 20	up to 200	>100
Q_G / nC	9 - 772	up to 10000	20 - 240	5 - 252
$R_{DS,on}$ / mΩ			17 - 6000	0.4 - 400
Applications	Motor Drives, Solar Inverters, Welding	Motor Drives, Solar Inverters, Wind Turbines	PFC stages, Computing, Server	Audio Amps, SMPS, Telecom

In recent years, the CoolMOS™ has become the leading product in the group of Superjunction MOSFETs. These switches withstand high voltages (from 500 to 950 V) when kept at low to medium currents (up to 100

A). At lower voltages, medium-voltage devices can be utilized, for instance the Infineon OPTIMOS^{TM}. In recent years, new wide-bandgap (WBG) devices have emerged to attack the market of the classical silicon-based applications. Table 2.2 compares the two most important technologies, silicon carbide (SiC) and gallium nitride (GaN).

Tab. 2.2: Key performance parameters of WBG power devices.

	SiC	GaN
V_{max}/V	60 - 1700	100 - 650
I_{nom}/A	up to 225	up to 120
f_{SW}	>100 kHz	>100 MHz
Q_G/nC	5.6 - 406	1.5 - 18
$R_{DS,on}/m\Omega$	3.1 - 1150	5 - 150
$Power/W$	35 - 520	55 - 125

The SiC technology is able to carry much higher power densities compared to silicon-based MOSFETs and is expected to advance to the IGBT power range. Hence, SiC switches can be utilized in classical IGBT applications to yield much lower switching losses and the lowest $R_{DS,on}$ in its corresponding voltage class. In contrast, GaN is extending the power density and frequency range of silicon MOSFETs, making them more suitable for use in Superjunction MOSFET applications.

2.1.2 Half-Bridge Circuits in Electrical Converters

The fundamental block in electrical converters is a half-bridge. It consists of two power devices acting as switches, which are referred to as low side and high side. A half-bridge forms the basic element of any converter stage. Multiple bridges can be combined to achieve different power electronic topologies, such as e.g. H-bridges or three-phase inverters. Figure 2.1 shows a half-bridge consisting of (a) IGBTs or (b) MOSFETs. The high side can establish a low-ohmic connection to the supply voltage V_{DC}, which is referred to as the DC link voltage, when it is turned on. The low side connects the output switching node to the ground reference.

Both high side and low side are turned on and off by gate drivers, that are usually controlled by pulse-width modulation (PWM) signals. The gate driver is responsible to deliver the required gate charge (Q_G) of the switch in order to establish the gate-source voltage (gate-emitter voltage for IGBTs) needed to fully turn on the device, and to remove the same amount of charge during the turn-off event. Some drivers also involve a negative supply voltage to enable a faster discharging of the gate during turn-off, which is especially important if the device exhibits a large gate charge Q_G, as for instance in larger IGBT modules. The use

of a negative gate voltage further prevents an undesired parasitic turn-on when the device is fully turned off [28].

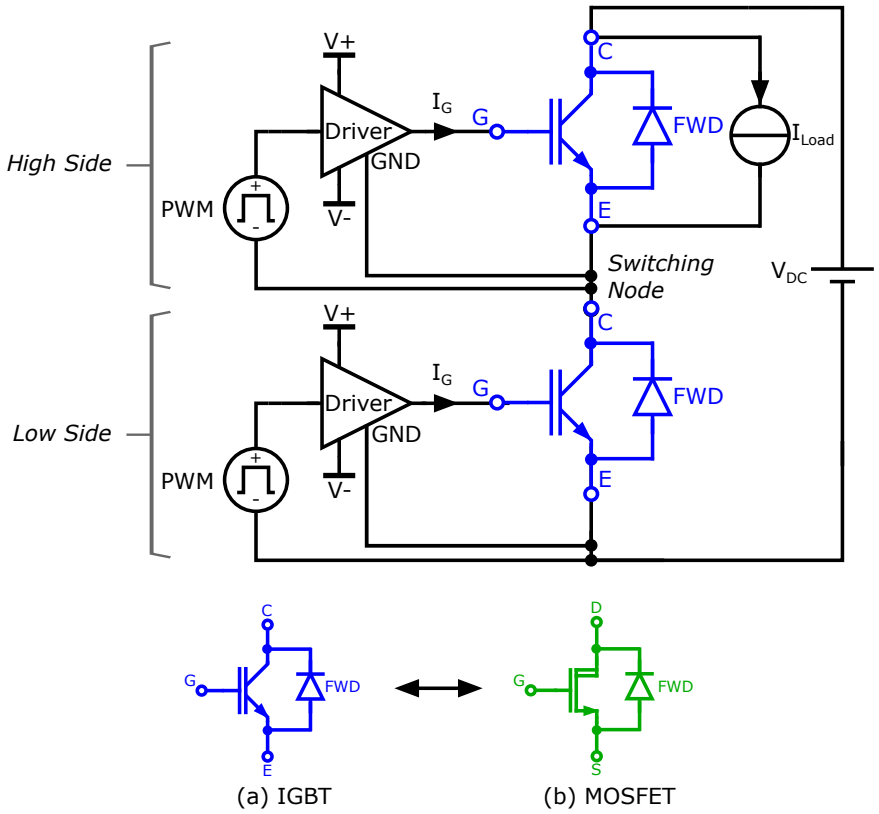


Fig. 2.1: Typical half bridge power stage as used in various kinds of electrical converters, realized with (a) IGBTs and (b) MOSFETs.

2.2 Switching Behavior of Gate-Controlled Devices

2.2.1 Equivalent Circuit for the Switching Dynamics

To understand the dynamics in the switching transition of a power transistor, parasitics in the switch and in the half bridge circuit need to be taken into account. Figure 2.2 shows an equivalent circuit for a test setup, used for analysis of the switching behavior. The model, which is based on [29], adds parasitics to the half-bridge schematic from Fig. 2.1 (C_{GE}, C_{GC}, C_{CE},L_S). Furthermore, the high side stays turned off, such that only the free-wheeling diode (FWD) is apparent, while the low side is turned on and off. This structure serves as a basis for the description of the switching behavior, and also for later investigations on the dual-loop control concept. The circuit employs a resistive push-pull gate driver, which provides either a negative or a positive output voltage. The gate current and, consequently, the rates of $\mathrm{d}I_C/\mathrm{d}t$ and $\mathrm{d}V_{CE}/\mathrm{d}t$ are defined by the size of the gate resistor R_G. The DC link voltage V_{DC} and the load current I_{Load}, which represents

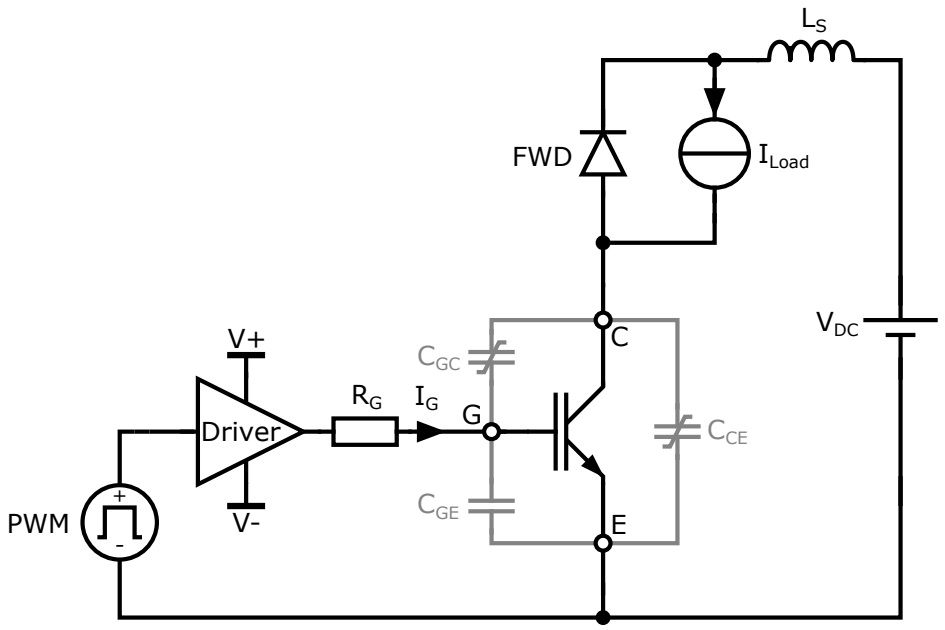


Fig. 2.2: Equivalent circuit for hard switching of the low-side IGBT including parasitics.

the current impressed by the inductive load, are assumed to be constant within the switching period. The stray inductance L_S represents the sum of all the parasitic inductances in the commutation loop (e.g. DC link, busbars, device lead inductances) [30] [31]. The parasitic device capacitances C_{GE}, C_{GC} and C_{CE} are considered as well. C_{GC} and C_{CE} are strongly non-linear and depend mainly on V_{CE}. Figure 2.3 shows the typical voltage dependency of C_{GC} for a 1.2 kV IGBT. The dashed line indicates the approximation of $C_{GC,L}$ for small values of V_{CE} lower than the gate-emitter voltage ($V_{CE} < V_{Ge}$) and $C_{GC,S}$ for higher values of V_{CE} ($> V_{Ge}$) [32].

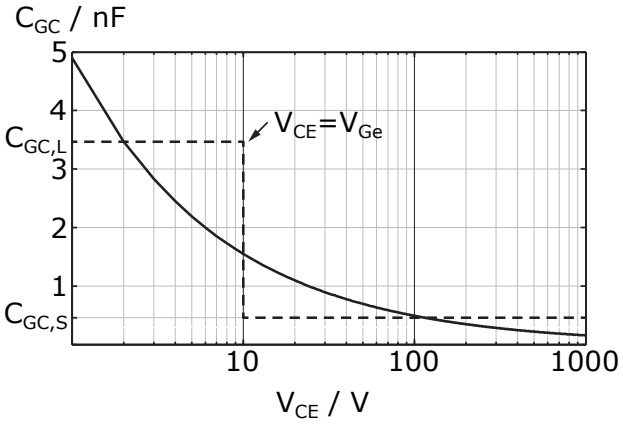


Fig. 2.3: Typical voltage dependency of the Miller capacitance C_{GC} [32].

The capacitances of a power switch are typically defined in datasheets as follows :

$$\text{Input capacitance:} \quad C_{\text{iss}} = C_{\text{GE}} + C_{\text{GC}} \tag{2.1}$$

$$\text{Output capacitance:} \quad C_{\text{oss}} = C_{\text{GC}} + C_{\text{CE}} \tag{2.2}$$

$$\text{Reverse transfer capacitance:} \quad C_{\text{rss}} = C_{\text{GC}} \tag{2.3}$$

Beside the gate resistance, these parasitic capacitances have the main impact on the switching transients. In particular, C_{GE} influences $\mathrm{d}I_{\text{C}}/\mathrm{d}t$ and C_{GC} influences $\mathrm{d}V_{\text{CE}}/\mathrm{d}t$, as will be derived and demonstrated in the following Sect. 2.2.2, cf. Eq. (2.6) and Eq. (2.10). Therefore, these parameters are essential and need to be included into the plant models for an appropriate design of a closed-loop $\mathrm{d}V_{\text{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\text{C}}/\mathrm{d}t$ control, which will be discussed in more detail in Sect. 3.3.

2.2.2 Turn-on Switching Behavior

During turn-on, the load current I_{Load} commutates from the freewheeling diode to the power switch and the blocking voltages transits from the power switch to the diode [33]. The waveforms of V_{CE}, I_{C}, V_{Ge} and I_{G} during turn-on are shown in Fig. 2.4. The turn-on is subdivided into the intervals I-V which are described below.

I: Gate charge delay ($t_0 < t < t_1$)

The turn-on is initiated by the gate driver at $t = t_0$, by applying a voltage step from $V_{\text{out,drv}} = V_{-}$ to $V_{\text{out,drv}} = V_{+}$. Accordingly, the input capacitance of the power switch is charged. As a resistive gate driver is used, this process relates to the charging of a *RC*-lowpass, where R equals the gate resistor R_{G} and C is formed by the input capacitance C_{iss}. The turn-on gate charge delay (time until the threshold voltage $V_{\text{Ge,th}}$ is reached and the collector current starts to rise) for a resistive gate driver can be calculated as

$$t_{\text{d,Gc}} = t_1 - t_0 = R_{\text{G}} \cdot C_{\text{iss}} \cdot \ln\left(\frac{\Delta V_{\text{out,drv}}}{V_{+} - V_{\text{Ge,th}}}\right). \tag{2.4}$$

II: Current rise ($t_1 < t < t_{1A}$)

At $t > t_1$, the gate voltage V_{Ge} is above the threshold voltage $V_{\text{Ge,th}}$. Therefore, the load current starts to commutate from the freewheeling diode to the power switch. As the power switch is operated in the active

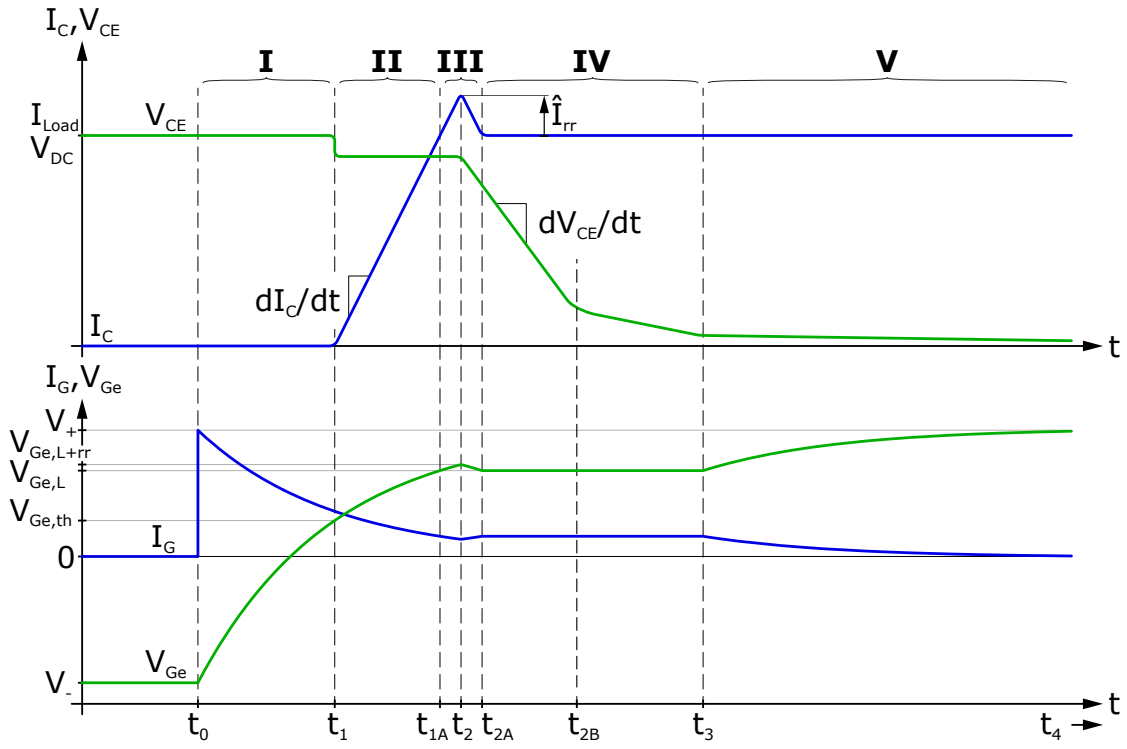


Fig. 2.4: Turn-on transients for inductive load switching.

region, the collector current (drain current in case of a MOSFET) is defined as

$$I_{\mathrm{C}}(t) = g_{\mathrm{m}} \cdot \left(V_{\mathrm{Ge}}(t) - V_{\mathrm{Ge,th}}\right). \tag{2.5}$$

From Eq. (2.5), collector current slew rate can be calculated as a function of the gate current,

$$\frac{\mathrm{d}I_{\mathrm{C}}}{\mathrm{d}t} = g_{\mathrm{m}} \cdot \frac{\mathrm{d}V_{\mathrm{Ge}}}{\mathrm{d}t} = g_{\mathrm{m}} \cdot \frac{I_{\mathrm{G}}}{C_{\mathrm{iss}}} \approx g_{\mathrm{m}} \cdot \frac{I_{\mathrm{G}}}{C_{\mathrm{GE}}}. \tag{2.6}$$

In a typical power switch, the transconductance g_{m} strongly depends on the operating point. Hence, $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ is not constant during the switching phase in a conventional gate driver. Table 2.3 compares values for $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ in different commercial IGBTs, two discretes and two modules, for an injected gate current of $I_{\mathrm{G}} = 50$ mA during the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ transient. The slew rate depends on the device input capacitance. Therefore, $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ decreases for larger devices if the same gate driver strength is used. As the rising collector current flows through the stray inductance L_{S}, a voltage is induced over L_{S} which reduces the voltage drop over the power switch,

$$V_{\mathrm{CE}} = V_{\mathrm{DC}} - L_{\mathrm{S}} \cdot \frac{\mathrm{d}I_{\mathrm{C}}}{\mathrm{d}t}. \tag{2.7}$$

According to Eq. (2.7), this leads to an overlap of the subsequent current and voltage transition, as there is a voltage drop, and therefore non-zero $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$, during the current transition, as indicated in Fig. 2.4.

Tab. 2.3: Typical values for $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ for commercial switches, calculated using Eq. (2.6), assuming I_G = 50 mA during the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ transition. Values are taken out of the corresponding datasheets.

Device	Type	V_{max} / V	I_{nom} / A	g_m / S	C_GE / pF	$\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ / [A/ns]
IKW50N60T	Discrete IGBT	600	50	31	3047	0.67
IKW50N65NH5	Discrete IGBT	650	50	62	2989	1.04
FF225R12ME4	IGBT Module	1200	225	105	13000	0.40
FF900R12IE4	IGBT Module	1200	900	445	54000	0.41

However, the subsequent occurence is the basis for the small-signal approach in Sect. 3.3. Therefore, the stray inductance must be kept small to enable individual control of $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$.

III: Reverse recovery of the diode ($t_{1A} < t < t_{2A}$)

I_C reaches the load current level I_Load at $t = t_{1A}$. The diode current reverses its polarity and the reverse recovery process starts. This means that the stored charge Q_rr in the diode is actively removed. As a consequence, the collector current exhibits an overshoot with the peak reverse recovery current $\hat{I}_\mathrm{rr}$. Assuming a symmetrical triangular-shaped reverse recovery approximation [34], the peak reverse recovery current can be expressed as

$$\hat{I}_\mathrm{rr} = \sqrt{Q_\mathrm{rr} \cdot \frac{\mathrm{d}I_\mathrm{C}}{\mathrm{d}t}}. \tag{2.8}$$

At $t = t_2$, I_C reaches its maximum and the diode gains voltage blocking capability. Therefore, the collector-emitter voltage of the power switch starts to decay.

IV: Voltage decay ($t_{2A} < t < t_3$)

While the power switch remains in the active region, the collector current continues at I_Load. According to Eq. (2.5), the gate voltage stays at $V_\mathrm{Ge,L}$,

$$V_\mathrm{Ge}\big|_{I_\mathrm{C}=I_\mathrm{Load}} = V_\mathrm{Ge,L} = V_\mathrm{Ge,th} + \frac{I_\mathrm{Load}}{g_\mathrm{m}}. \tag{2.9}$$

This constant level of gate voltage during turn-on, which also occurs during turn-off is referred to as *Miller Plateau*. The gate current is almost constant during this interval, as it only discharges the Miller capacitance

C_{GC}. Accordingly, the decay of the collector-emitter voltage can be described as

$$\frac{dV_{CE}}{dt} = -\frac{dV_{GC}}{dt} = -\frac{I_G}{C_{GC,S}}. \tag{2.10}$$

Table 2.4 compares values for dV_{CE}/dt in different commercial IGBTs, two discretes and two modules, for an injected gate current of I_G = 100 mA during the dV_{CE}/dt transient. The Miller capacitance C_{GC} shows

Tab. 2.4: Typical values for dV_{CE}/dt for commercial switches, calculated using Eq. (2.10), assuming I_G = 100 mA during the dV_{CE}/dt transition. Values are taken out of the corresponding datasheets.

Device	Type	V_{max} / V	I_{nom} / A	C_{GC} / pF	$\lvert dV_{CE}/dt \rvert$ / [V/ns]
IKW50N60T	Discrete IGBT	600	50	93	1.07
IKW50N65NH5	Discrete IGBT	650	50	11	9.09
FF225R12ME4	IGBT Module	1200	225	705	0.14
FF900R12IE4	IGBT Module	1200	900	3000	0.03

a non-linear dependency on V_{CE} as shown in Fig. 2.3. At $t = t_{2B}$, V_{CE} reaches a value close to V_{Ge}. This leads to a very small dV_{CE}/dt according to Eq. (2.10), as C_{GC} increases strongly and the gate current stays constant during this period.

V: Gate charge ($t_3 < t < t_4$)

Once the power switch transits from the active region into the saturation region, the gate is no longer clamped and the gate driver continues charging of the input capacitance. After this interval, the device is fully turned-on.

2.2.3 Turn-off Switching Behavior

During turn-off, the load current I_{Load} commutates from the power switch to the freewheeling diode and the DC link voltage drop transits from the diode to the power switch. The waveforms of V_{CE}, I_C, V_{Ge} and I_G during turn-off are shown in Fig. 2.5 in a similar way as for turn-on. In particular, the switching transients are inversed compared to turn-on, except for the reverse recovery behavior. The turn-off is subdivided into the intervals VI-X, which are described below.

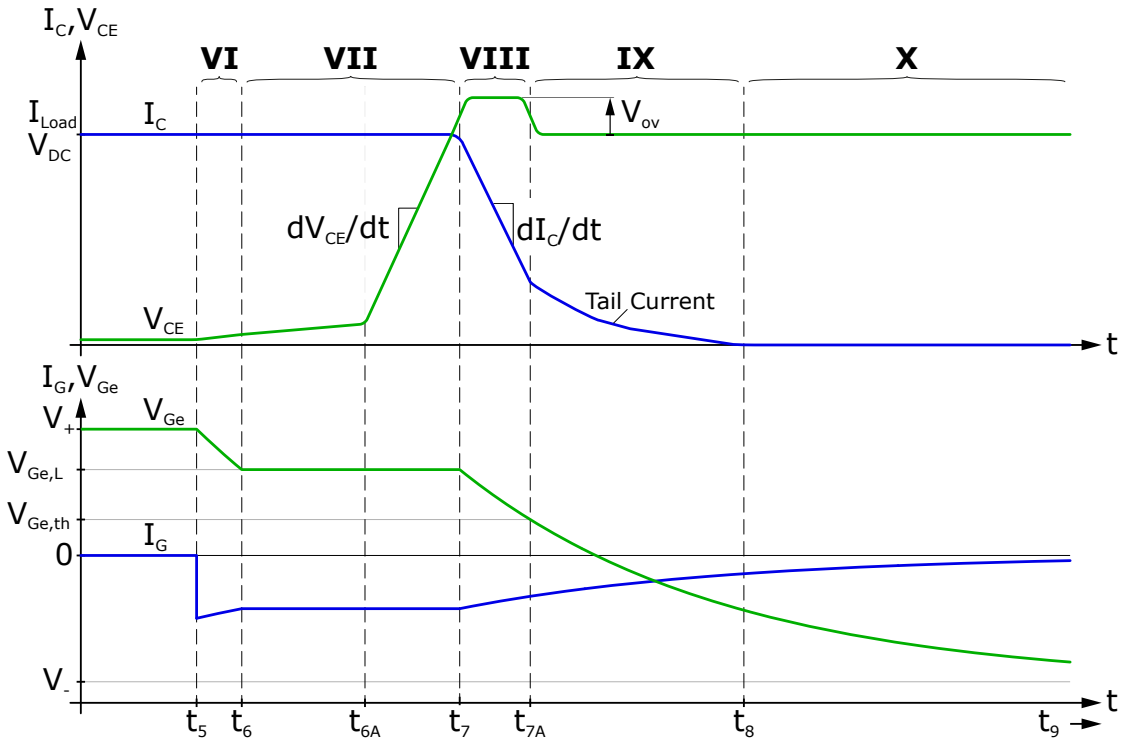


Fig. 2.5: Turn-off transients for inductive load switching.

VI: Gate discharge delay ($t_5 < t < t_6$)

The turn-off is initiated by the gate driver at $t = t_5$, by applying a voltage step from $V_{\text{out,drv}} = V_+$ to $V_{\text{out,drv}} = V_-$. The gate voltage at off-state is often negative to prevent a parasitic turn-on for large values of $\mathrm{d}V_{\text{CE}}/\mathrm{d}t$.

According to the voltage step, the input capacitance of the power switch is discharged with an *RC*-behavior. The gate current performs a step to its minimum value and starts to rise. The gate discharge delay until the power switch enters the active region can be calculated as

$$t_{\text{d,Gd}} = t_6 - t_5 = R_{\text{G}} \cdot C_{\text{iss}} \cdot \ln\left(\frac{\Delta V_{\text{out,drv}}}{V_{\text{Ge,L}} - V_-}\right). \tag{2.11}$$

VII: Voltage rise ($t_6 < t < t_7$)

The power switch enters the active region and V_{Ge} reaches the Miller Plateau $V_{\text{Ge,L}}$ (see Eq. (2.9)). A constant gate current charges the Miller capacitance, which is large due to the low value of V_{CE} (see Fig. 2.3). At t_{6A}, the collector-emitter voltage reaches V_{Ge}, which leads to a strong decrease in C_{GC}. Therefore, V_{CE} starts to rise very fast with $\mathrm{d}V_{\text{CE}}/\mathrm{d}t$ according to interval IV at turn-on (see Eq. (2.10)). The additional

delay prior to t_{6A} caused by the large Miller capacitance can be calculated as

$$t_{\mathrm{d,GC}} = t_{6A} - t_6 = (V_{\mathrm{CE,sat}} - V_{\mathrm{Ge,L}}) \cdot \frac{C_{\mathrm{GC,L}}}{I_{\mathrm{G}}}. \tag{2.12}$$

VIII: Current decay ($t_7 < t < t_{7A}$)

Once V_{CE} reaches the value of the DC link voltage V_{DC}, the freewheeling diode gets forward biased. Therefore, the load current starts to commutate from the power switch to the diode. The gate voltage is no longer clamped and C_{iss} is discharged like in interval VI. The amount of $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ can be calculated in a similar way as for turn-on in interval II (see Eq. (2.6)). Due to the falling collector current, flowing through the stray inductance L_{S}, a negative voltage is induced in L_{S} that leads to an overshoot in the collector-emitter voltage,

$$V_{\mathrm{CE}} = V_{\mathrm{DC}} - L_{\mathrm{S}} \cdot \frac{\mathrm{d}I_{\mathrm{C}}}{\mathrm{d}t} = V_{\mathrm{DC}} + V_{\mathrm{OV}}. \tag{2.13}$$

IX: Tail current ($t_{7A} < t < t_8$)

If the switching device is an IGBT, the collector current reaches the level of the tail current at $t = t_{7A}$. In this period, the gate driver is no longer able to control the device. The characteristic tail is caused by minority carriers that are stored in the IGBT to reduce the voltage drop in on-state. V_{Ge} is below $V_{\mathrm{Ge,th}}$, which means that the channel stops conducting. As the channel current stops, the remaining charges in the IGBT can only be removed by recombination. Therefore, the tail current highly depends on the IGBT's technology (in particular the size of the drift zone), the charge carrier lifetime and varies with the junction temperature T_{j} [35].

X: Gate discharge ($t_8 < t < t_9$)

While the current decays, the gate voltage decreases down to $V_{\mathrm{Ge}} = V_{-}$. The freewheeling diode is now carrying the whole load current, and the power switch is fully in blocking mode.

2.2.4 Trade-offs Resulting from the Slew Rates of the Switching Transients

Setting the rate of the voltage and current slopes ($\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$) in a power semiconductor device enables a trade-off between switching losses, switching delays, SOA operation and electromagnetic interference (EMI). The influence of slow or fast switching transients on these switching behavior parameters is briefly reviewed in the following.

Switching Losses

The switching losses during turn-on or turn-off result from the temporary overlap of the collector-emitter voltage V_{CE} and the collector current I_C. Hence, the energy loss highly depends on the transient switching waveforms. This is illustrated in Fig. 2.6.

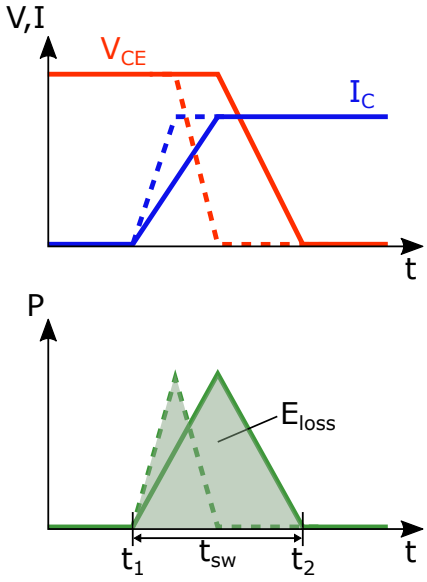


Fig. 2.6: Switching loss caused by the current and voltage transients of an IGBT.

The energy loss during the switching time t_{sw} is given by

$$E_{loss} = \int_{t_1}^{t_2} V_{CE} I_C \, dt, \tag{2.14}$$

which can be simplified to the approximation

$$E_{loss} \approx 0.5 \cdot V_{CE} \cdot I_C \cdot t_{sw}, \tag{2.15}$$

as the multiplication of V_{CE} and I_C results in a triangular shaped waveform over time. (2.15) The switching losses depend strongly on the switching time t_{sw}, which is defined by the amount of V_{CE} and I_C. Hence, fast switching transistions are preferred, if high efficiency is the major design goal.

Switching Delay

The switching delay time indicates the interval from triggering the turn-on or turn-off until the switching transients start to rise. These delays should be kept as small as possible because they act as phase shift

between the actual PWM control signal and the generated output current and voltage waveform. A large delay could lead to a minor bandwidth and a reduced phase margin of the superordinate control of the power electronic system (e.g. field-oriented control of an electric motor). The delay during turn-on is given by the time period for charging the gate to threshold level $V_{\mathrm{Ge,th}}$ (see Eq. (2.4)). The turn-off switching delay is defined by the discharging of the gate to Miller Plateau level (Eq. (2.11)) and by charging the large Miller capacitance to the gate voltage level (Eq. (2.12)). The turn-on and turn-off delay mainly depend on the size of the gate resistor and the gate current. Hence, fast switching (low gate resistor and high gate current) is preferred for short turn-on and turn-off switching delays.

Tab. 2.5: Typical turn-on and turn-off delay values of different IGBTs (datasheets values).

Device	Type	V_{max} / V	I_{nom} / A	$t_{\mathrm{d,Gc}}$ / ns	$t_{\mathrm{d,Gd}}$ / ns
IKW50N60T	Discrete IGBT	600	50	26	299
IKW50N65NH5	Discrete IGBT	650	50	21	180
FF225R12ME4	IGBT Module	1200	225	160	380
FF900R12IE4	IGBT Module	1200	900	200	660

Safe Operating Area (SOA)

Fast switching is beneficial in terms of low switching losses and small switching delay times. However, a fast collector current transient leads to an increased peak reverse recovery current during turn-on (Eq. (2.8)) and to a higher overvoltage during turn-off (Eq. (2.13)). These individual peaks in power loss need to be maintained within certain limits defined by the safe operating area (SOA). The boundaries, which are determined by properties of the semiconductor material, are shown schematically in Fig. 2.7 together with the switching trajectories of different speeds. These SOA diagrams, which depict the specific limits in I_{C} and V_{CE} at a specific gate-emitter voltage V_{Ge}, are typically shown in the device datasheets.

Hence, the switching speed of the device has to be decreased to such a level, that operation in the SOA is guaranteed for the whole range of operating conditions (load current, DC link voltage and temperature). This results in increased switching losses. Furthermore, it is usually required that the devices need to be designed for a higher voltage rating than the utilized DC link voltage V_{DC}, which leads to higher parasitics and therefore to associated disadvantages such as higher delay times and losses.

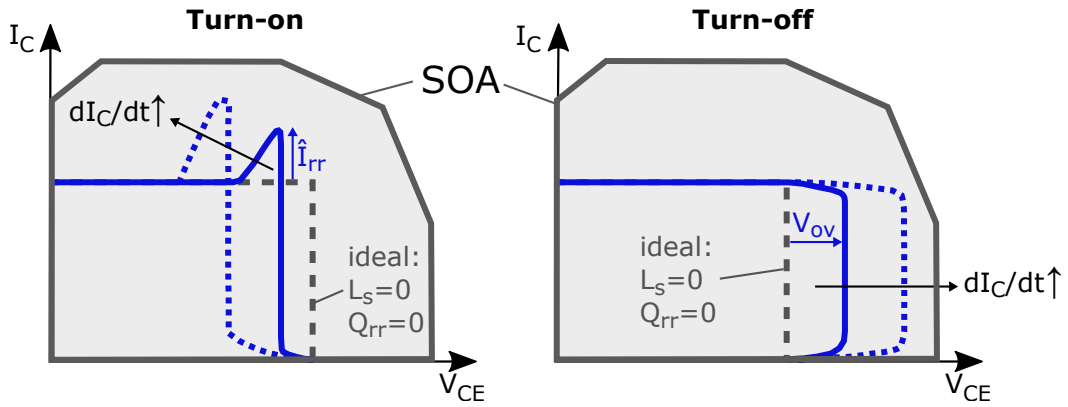


Fig. 2.7: Switching trajectories of a gate-controlled power switch considering reverse recovery during turn-on and overvoltage during turn-off inside the safe operating area. The dashed line in black represents the trajectory for an ideal commutation loop without stray inductance ($L_S = 0$) and no reverse recovery ($Q_{rr} = 0$).

Tab. 2.6: Typical values for the reverse recovery peak current in different IGBT devices (datasheets values at specific dI_C/dt).

Device	Type	V_{max} / V	I_{nom} / A	dI_C/dt / [A/ns]	$\hat{I}_{rr}$ / A
IKW50N60T	Discrete IGBT	600	50	1.28	27.7
IKW50N65NH5	Discrete IGBT	650	50	1.20	16.7
FF225R12ME4	IGBT Module	1200	225	5.75	300
FF900R12IE4	IGBT Module	1200	900	5.70	500

Electromagnetic Interference (EMI)

Another design aspect in power electronic systems is the EMI, which is caused by the switching transitions. EMC analysis differentiates between common mode noise and differential mode noise [36]. Thereby, the fast voltage changes (dV_{CE}/dt) are causing common mode noise, which couples via parasitic capacitances into the supply lines. Differential noise mainly results from the fast changing load current (dI_C/dt) in the commutation loop and from the reverse recovery of the body diode.

The electromagnetic emissions of a PWM controlled driver are typically predicted with the frequency spectrum of a trapezoidal signal [37]. For simplicity, the trapeze exhibits an equal rise time τ_r and fall time τ_f (see Fig. 2.8a). Employing this assumption, the emission of a trapeze signal in the frequency domain is given by

$$E_{dB} = 20\log\left(2A\frac{\tau}{T}\right) + 20\log\left|\frac{\sin(\pi\tau f)}{\pi\tau f}\right| + 20\log\left|\frac{\sin(\pi\tau_r f)}{\pi\tau_r f}\right|. \tag{2.16}$$

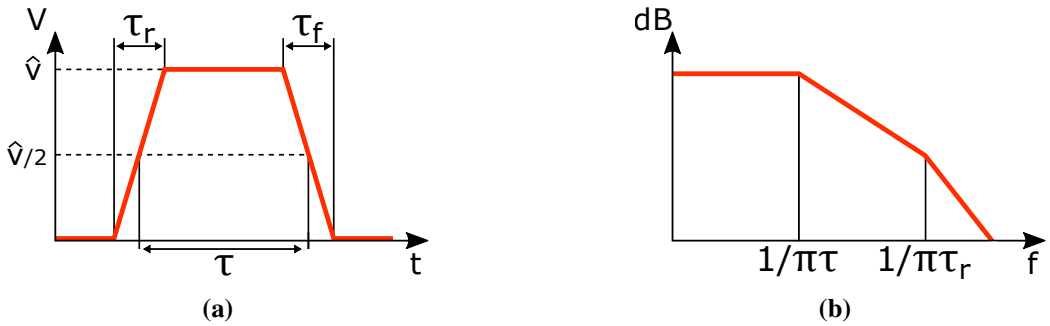


Fig. 2.8: (a) Trapeze in time domain (b) Trapeze in frequency domain [39].

The resulting frequency spectrum is illustrated in Fig. 2.8b. The first term of Eq. (2.16) represents a constant level of emission and is mainly influenced by the amplitude A of the signal and the on-time τ. The second term marks the first breakpoint, at which the emissions decrease with 20 dB/decade. The breakpoint depends on the switching frequency f and τ. As the parameters A, f and τ are given by the application, only the third term remains for reducing the emission by the gate driver. This term represents the second breakpoint, at which the signal emissions fall with 40 dB/decade. Lowering the rise and fall times of the voltage transients shifts the second breakpoint to lower frequencies and hence reduces the emissions in the higher frequency range. The real emission spectrum differs from the illustration in Fig. 2.8b, because the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ causes ringing, which results in additional emissions due to induced voltages in the parasitic inductances. The additional EMI, caused by $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$, generally occurs in the higher frequency spectrum. The EMI in the lower frequency spectrum has to be reduced with filters or further sophisticated techniques such as edge shaping [38], as it can usually not be influenced by the slew rates of the switching slopes [39].

Requirements on $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ in Motor Drives

The IEC 60034-17 standard defines the voltage peak limits in relation to the rise time for general purpose 500 VAC motors when fed by motor drives and IEC 60034-25 specifies the limits for motors rated 500 VAC and 690 VAC [40]. Depending on the rise time, the maximum $\mathrm{d}V/\mathrm{d}t$ can be up to 5 V/ns [41]. However, most manufacturers recommend to reduce the $\mathrm{d}V/\mathrm{d}t$ at the motor terminals to 1 V/ns in order to reduce the voltage stress on the motor insulation and to increase the motor's lifetime [40] [16].
Considering the reflections at the motor terminal, the achievable rates for $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ of the closed-loop gate driver should be in the following ranges:

$$\mathrm{d}I_\mathrm{C}/\mathrm{d}t \approx 0.1\ \mathrm{A/ns}\ \text{ to }\ 1.0\ \mathrm{A/ns} \tag{2.17}$$

$$\mathrm{d}V_\mathrm{CE}/\mathrm{d}t \approx 0.5\ \mathrm{V/ns}\ \text{ to }\ 2.5\ \mathrm{V/ns}. \tag{2.18}$$

Trade-off Definition

In summary, fast switching transitions are beneficial for low switching losses and small switching delay times. However, operation of the device within the SOA under all conditions and the compliance with EMC standards demand for decreasing the slew rates of the voltage and current slope. Table 2.7 shows an exemplary trade-off matrix for a 50 A, 600 V IGBT in a modern trench-/fieldstop technology, where $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ is limited to 1 V/ns due to a given requirement, and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ is used to limit the reverse recovery current peak $\hat{I}_{\mathrm{rr}}$ at turn-on and the voltage overshoot V_{OV} at turn-off. The values are calculated using the approximations in Eq. (2.8), Eq. (2.13) and Eq. (2.15). In case $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ is decreased by factor 10 (from 5 A/ns to 0.5 A/ns), $\hat{I}_{\mathrm{rr}}$ is decreased by 68% (95 A to 30 A) and V_{OV} by a factor of 10 for the given switch under the mentioned conditions. These exemplary calculations show that a trade-off between SOA and switching losses is possible by $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ adjustment. To achieve an appropriate trade-off between these design goals,

Tab. 2.7: Exemplary trade-off matrix for 50 A, 600 V Discrete IGBT IKW50N60T.
V_{DC} = 400 V, I_{Load} = 50 A, $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ = 1 V/ns, L_{S} = 100 nH, Q_{rr} = 1.8 µC

IKW50N60T	E_{loss} / mJ	$\hat{I}_{\mathrm{rr}}$ / A	V_{OV} / V
$\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ = 0.5 A/ns	5	30	50
$\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ = 1.0 A/ns	4.5	42	100
$\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ = 5.0 A/ns	4.1	95	500

depending on the requirements of a specific power electronics application, gate drive concepts with slope shaping are employed, that are able to control the voltage and/or current slew rates.
There are different methods to control $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ of a power semiconductor device. They are described in the following section, including their advantages and disadvantages.

2.3 State-of-the-Art Gate Drive Concepts

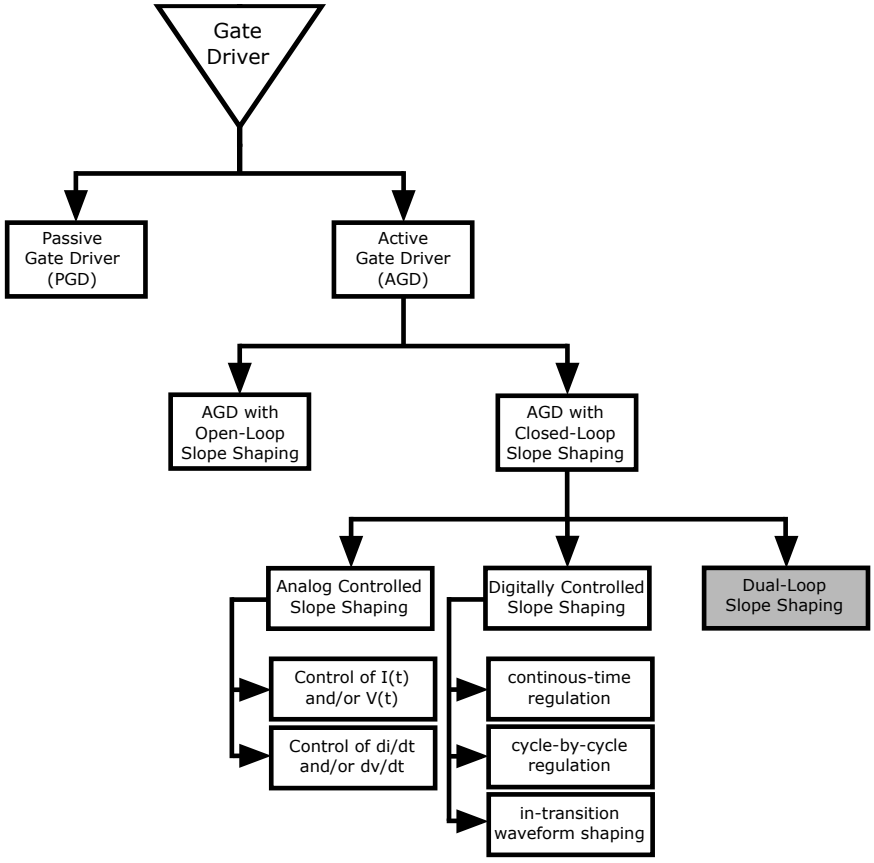


Fig. 2.9: Overview on the state-of-the-art in slope shaping gate drivers.

The gate driver is responsible for the static and dynamic switching performance of the power semiconductor device and is thus also responsible for the associated switching and conduction losses. The switching cycles of the driver are controlled by PWM signals applied by a microcontroller or comparable control units. Thereby, the driver acts as an amplifier, which amplifies the control signal by boosting the voltage and current levels to reach the desired driving capability. The main function of the gate driver is to charge and discharge the input and reverse transfer capacitance of the power switch. The total charge is referred to as gate charge [28] [42]. Figure 2.9 provides an overview of existing gate driving techniques that are able to limit or control the slew rates of current and/or voltage. In general, two basic principles can be distinguished [43]. The first group is formed by *Passive Gate Drivers* (PGDs), the second by *Active Gate Drivers* (AGDs). Active gate drivers consist of two categories, gate drivers with open-loop and gate drivers with closed-loop slope shaping. The different gate drivers are introduced in the following.

2.3.1 Passive Gate Drivers

Gate drivers without any kind of active control on the switching behavior during the transition are referred to as passive gate drivers (PGD). They are frequently used in today's products. In general, passive gate drivers can be subdivided into the following four gate driving schemes:

1. **Voltage source gate driver with resistive** $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$**,** $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ **adjustment (hard switching driver)**

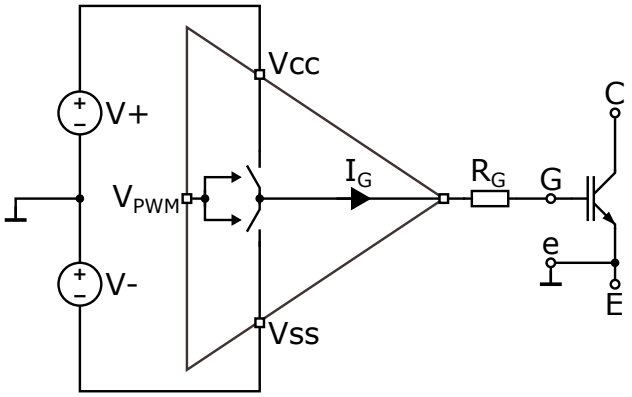


Fig. 2.10: Voltage source gate driver with resistive $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$,$\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ adjustment.

The driver acts like a constant voltage source, which is applied to the gate during a switching event, and the whole switching behavior (delay times, $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$, $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$) is predefined by the external gate resistor R_G mounted to the gate. In general, a larger gate resistor R_G leads to a lower gate current I_G and therefore to lower voltage and current slopes. This approach, which is depicted in Fig. 2.10, is the most common implementation and is widely used in commercial products, as for example in the *Infineon EiceDRIVER*^{TM} product family [44].

2. **Voltage source gate driver with individual** $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ **and** $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ **adjustment**
   In contrast to the resistive driver, the mounting of external passive components to the gate is not limited to a gate resistor, but extended by further passive components, such as capacitors $C_\mathrm{GC,ext}$ and $C_\mathrm{GE,ext}$. Hence, the switching speed can be set by the corresponding *RC* time constant. Therefore, these gate drivers are also known as RC-compensated gate drivers. Tuning of the external capacitors enables individual adjustment of $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$. It is recommended to use a gate resistor in series with $C_\mathrm{GE,ext}$ to damp a possible resonant circuit consisting of the gate path inductances and gate path capacitances. However, the major drawback of this method is that the switching delay times and the gate drive losses are increased due to the larger input capacitance.
   By adding an external Miller capacitance $C_\mathrm{GC,ext}$, $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ is slowed down (see Eq. (2.10)) with only

minor impact on $\mathrm{d}I_C/\mathrm{d}t$. Using this technique, it has to be considered that the external capacitor $C_{GC,ext}$ must provide at least the same blocking voltage capability as the device under control [28].

3. **Voltage source gate driver with separate ON / OFF adjustment**

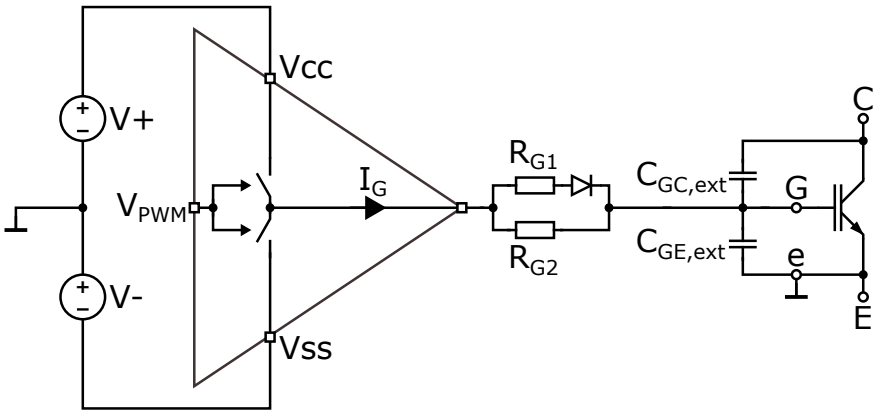


Fig. 2.11: Voltage source gate driver with separate ON/OFF adjustment of the switching transients.

If separate control is required for turn-on and turn-off, two gate resistors can be utilized in combination with diodes according to Fig. 2.11. This allows to individually tune the switching slopes for turn-on and turn-off. In the case of Fig. 2.11, the effective gate resistor during turn-on is $R_{G,on} = R_{G1}||R_{G2}$ and the effective gate resistor during turn-off is $R_{G,off} = R_{G2}$.

4. **Predefined current sources**

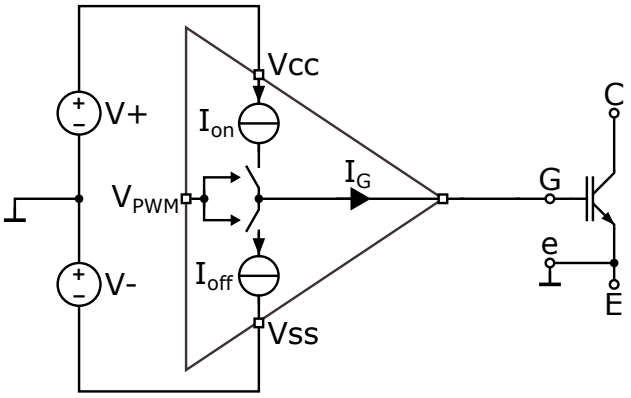


Fig. 2.12: Gate driver with predefined current sources.

The power switch and its switching behavior is directly controlled by a defined current into the gate. The driver consists of one or more current sources for positive and negative current (see Fig. 2.12). The advantage of this method is, that the gate current does not rely on a *RC*-time constant, as it is in case of voltage source drivers. Therefore, the rates of $\mathrm{d}V_{CE}/\mathrm{d}t$ and $\mathrm{d}I_C/\mathrm{d}t$ can be directly controlled

in feed-forward configuration. The disadvantage is mainly that the power losses generated by the driving current are dissipated in the current source within the driver and not in the gate resistor as for voltage source drivers [28].

Although the passive approach includes concepts that allow for individual tuning of the voltage and current transients, and therefore scaling of the switching losses, there are a couple of limitations. Passive gate drive concepts are purely feed-forward, which means that the output of the driver is predefined and not actively changed during the switching operation. The external passive components limit the gate current I_G during the whole switching event. This typically leads to unwanted higher switching delay. Furthermore, if advanced IGBT devices (e.g. IGBTs in trench-field-stop technology) are used, it can occur that $\mathrm{d}I_C/\mathrm{d}t$ during turn-off gets higher although the gate resistor is increased. This effect results from the large amount of stored charge, which is built up in conduction mode, so that $\mathrm{d}I_C/\mathrm{d}t$ at turn-off is sensitive to a *desaturation* of the semiconductor (for a specific range of gate resistor values). The stored charge in the IGBT's drift region is partly extracted at turn-off, which results in a faster $\mathrm{d}I_C/\mathrm{d}t$ and accordingly a higher voltage overshoot on V_{CE} [45].

2.3.2 Active Gate Drivers with Open-Loop Slope Shaping

Active gate drivers are capable of interventions to the gate at specific points during the switching transition, either based on timing or as a reaction on different type of local feedback. Open-loop gate drivers feature an adjustable output stage, that allows for individual control of the gate current. This behavior can generally be achieved with an adjustable gate voltage [46] or gate current source (see Fig. 2.13). The adjustable gate current can be implemented either as programmable current sources [47] [48] or with switchable gate resistors [49] [50].

The main idea is to divide the switching process into different intervals, for instance, pre-charge delay, $\mathrm{d}I_C/\mathrm{d}t$ interval, $\mathrm{d}V_{CE}/\mathrm{d}t$ interval and post-charge delay [51–54]. For each interval a specific gate voltage or gate current is provided, in order to achieve the desired behavior and individual open-loop control.

The reference profile can be either fixed [47] or based on feedback of the switching transients [55] [56, 57]. A very fast detection of the different intervals and also a quick switching of the driver output is needed to achieve an accurate control of the power semiconductor switch.

The main limitation of the passive and the open-loop concepts is the dependency on the operating conditions such as varying junction temperature, load current or DC link voltage. Furthermore, the non-linearities of the switch cannot be compensated by this kind of control. Hence, these concepts have to be designed for the worst case, which means that in nominal case the transients are not as fast as possible, resulting in higher losses and non-ideal behavior during nominal conditions.

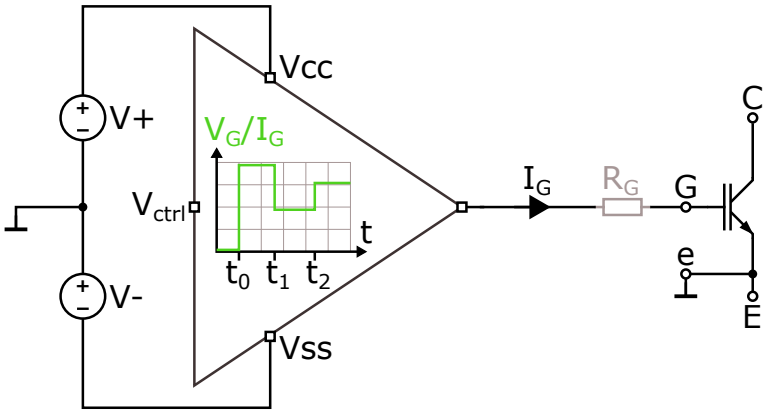


Fig. 2.13: Open-loop gate drive concept with adjustable output (adjustable gate voltage source or gate current source).

2.3.3 Active Gate Drivers with Closed-Loop Slope Shaping

To overcome the aforementioned limitations of passive and open-loop gate drivers, and to achieve a more precise and optimized control of the power switch, closed-loop concepts with negative feedback are employed. These concepts allow for compensation of the non-linearities, as well as for operating point (DC link voltage and load current) and temperature dependencies.

In closed-loop slope shaping, there are two significant trends. On the one hand, there is analog closed-loop control on the switching transients [58–75]. The other method is digital closed-loop slope shaping [24, 76–86]. Both principles are described in the following.

Analog Closed-Loop Gate Drivers

Within analog control, one can differentiate between two concepts: Concepts controlling the absolute values of $V_{CE}(t)$ and $I_C(t)$ (voltage/current control) and topologies which directly control dI_C/dt and dV_{CE}/dt (slope control).

Concepts for analog voltage/current control use a profile of $V_{CE}(t)$ and/or $I_C(t)$ as reference signal. An approach for an analog $V_{CE}(t)$ control is presented in [58], an analog $I_C(t)$ control with a reference profile can be realized in a similar way. However, if a combination of $V_{CE}(t)$ and $I_C(t)$ control is necessary, the reference profiles have to be generated by analog circuits for both $V_{CE}(t)$ and $I_C(t)$. Due to the mutual dependency of the voltage and the current slope and the dependency on the operating point, this is hard to implement.

Analog control loops, which directly control the dI_C/dt and dV_{CE}/dt, are cost-effective and show good control performance. Due to constant reference values, simple control amplifier stages and passive measurements, these controls offer a high analog control bandwidth [67].

A very sophisticated approach, which combines the control of $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$, and where both loops are closed simultaneously via a single proportional-integral (PI) controller is shown in Fig. 2.14.

The combination of $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ control with one controller is feasible, as the collector current slope and the collector-emitter voltage slope at hard switching of inductive loads occur in direct sequence with low overlap at turn-on or turn-off, if the parasitics in the system are kept small. However, there is a short overlap of the I_C and V_CE slope during the reverse recovery of the freewheeling diode (see Fig. 2.4 in Sec. 2.2.2). Therefore a clipping circuit is implemented in [67] to prevent an unwanted $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback during this phase.

The control loop is usually based on voltage signals. The reference signal $V_{\mathrm{ref,d}/\mathrm{d}t}$ is kept constant and set once at the beginning of every switching operation. There are two feedback paths with individual gain k_I and k_V for the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ feedback. The controlled signal of the summing node is amplified and integrated by a PI controller, which consists of an operational amplifier with *RC*-feedback. Thereafter, an output amplifier stage (emitter follower) is used to achieve the necessary driving capability required for the input capacitance of an IGBT module.

In addition, the circuit exhibits a gate current control, that is used to define the gate current during turn-on and turn-off delay intervals (not shown in Fig. 2.14). This additional circuit prevents any overshoots or poor control behavior during the beginning of the actual slope control after the switching delay at turn-on or turn-off [67].

Similar approaches as the control concept in Fig. 2.14 can be found in [72] or [87]. The main difference is, that these closed-loop concepts are based on current signals instead of voltage signals. Furthermore, these concepts do not include features like the clipping circuit, the PI controller or the gate current control.

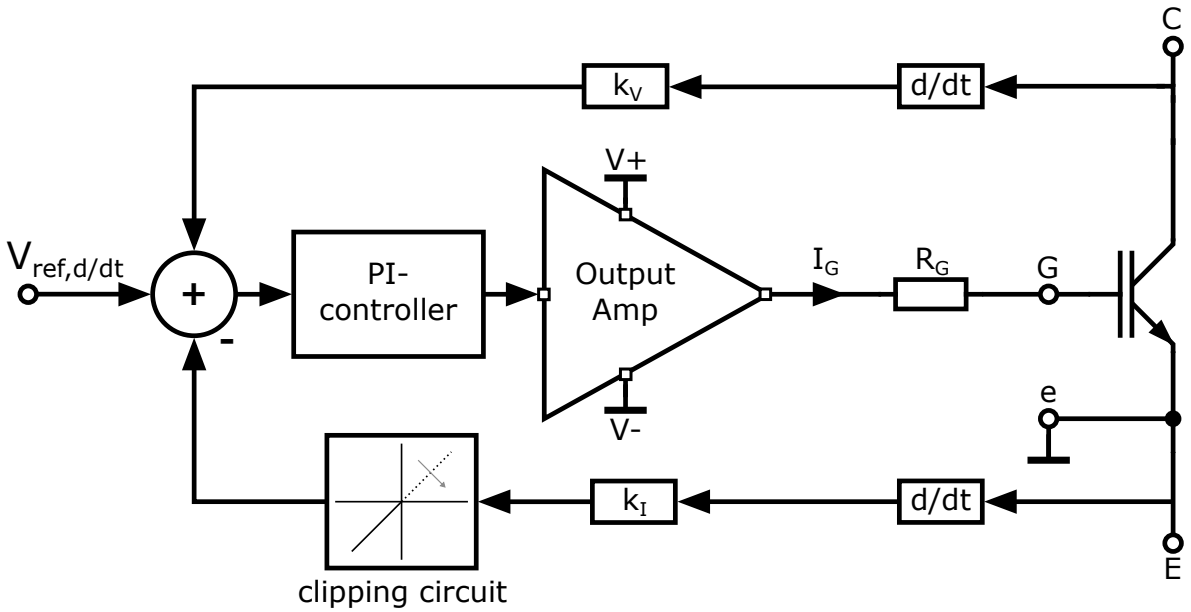


Fig. 2.14: Gate driver with closed-loop $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ and $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ control [67].

Analog feedback compensates for the non-linearities apparent in the power switch. As analog regulation achieves bandwidths in the MHz range, it can perform a continous-time closed-loop control [65]. However, a pure analog solution is relatively inflexible and does typically not support changes inside the control loop design during operation. In addition, some solutions leave remaining control errors [67].

Digital Closed-Loop Gate Drivers

The second trend in closed-loop slope shaping is digital control. A combined control of $V_{CE}(t)$ and $I_C(t)$ becomes feasible if a digital control unit is implemented. A digital gate unit (DGU) realized in [24] for digital closed-loop control of $\mathrm{d}V_{CE}/\mathrm{d}t$ and $\mathrm{d}I_C/\mathrm{d}t$ is shown in Fig. 2.15. Digital-to-analog converters (DACs) are used for generating the reference signal and the according feedback signals have to be digitalized by analog-to-digital converters (ADCs). Digital control of the slew rates has the key advantage of its high flexibility in driving strategies, as the regulation parameters can be programmed. As an example, it is possible to fit an arbitrary waveform to the desired application [82]. However, continous-time regulation is difficult due to the bandwidth-limited interfacing and the time-consuming digital algorithm. Therefore, a continous-time approach is limited to switching transients slower than approximately 2 µs [86]. Furthermore, the performance of this kind of control is limited by the highly dynamic reference and feedback signals, as well as by the limited bandwidth of high-power current sensors [76]. It demands for wide-bandwidth current sensors with galvanic isolation [88], increasing the cost of the control system.
To overcome the speed limitation, digital slope shaping is typically implemented by a predictive cycle-by-cycle regulation [77]. This kind of regulation is prone to errors in case of changing operating conditions between switching cycles, as for example in failure cases, which may lead to malfunction of the control loop.
As a conclusion, Table 2.8 provides a summary on the advantages and disadvantages of digital and analog control in closed-loop slope shaping.

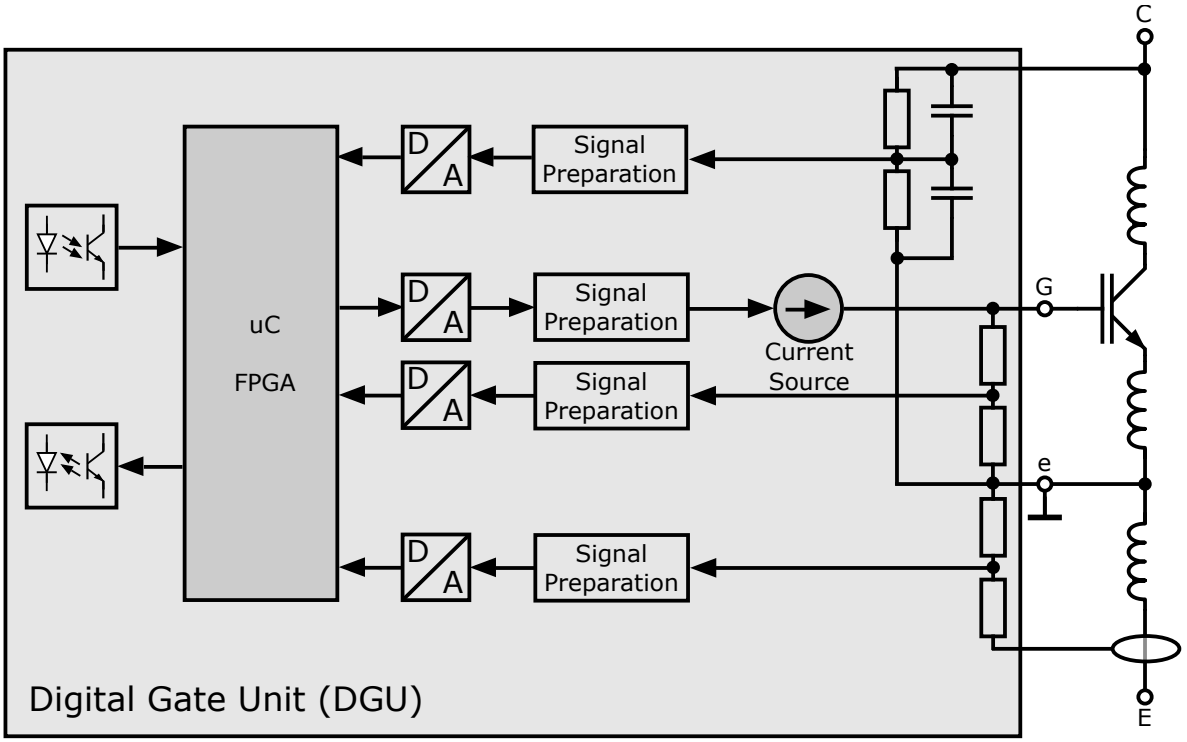


Fig. 2.15: Gate Driver with Digital Gate Unit (DGU) [24].

Tab. 2.8: Comparison of analog and digital closed-loop slope shaping gate drivers.

	Digital	Analog
Advantages	High flexibility in driving strategies	Continous-time regulation
	Compensation of non-linearities and operating point dependencies	Compensation of non-linearities and operating point dependencies
	More powerful filter functions	
	Adaptive learning	
Disadvantages	No continous-time regulation	Inflexible to changes in the control loop
	Limited handling of overload conditons	Higher complexity in analog design
	Costs	

3 The Dual-Loop Gate Driver Concept

3.1 Introduction

Figure 3.1 shows the proposed dual-loop slope shaping gate driver concept, which comprises both analog and digital closed-loop control.
This hybrid approach combines the advantages of the two domains, as listed in Table 2.8.

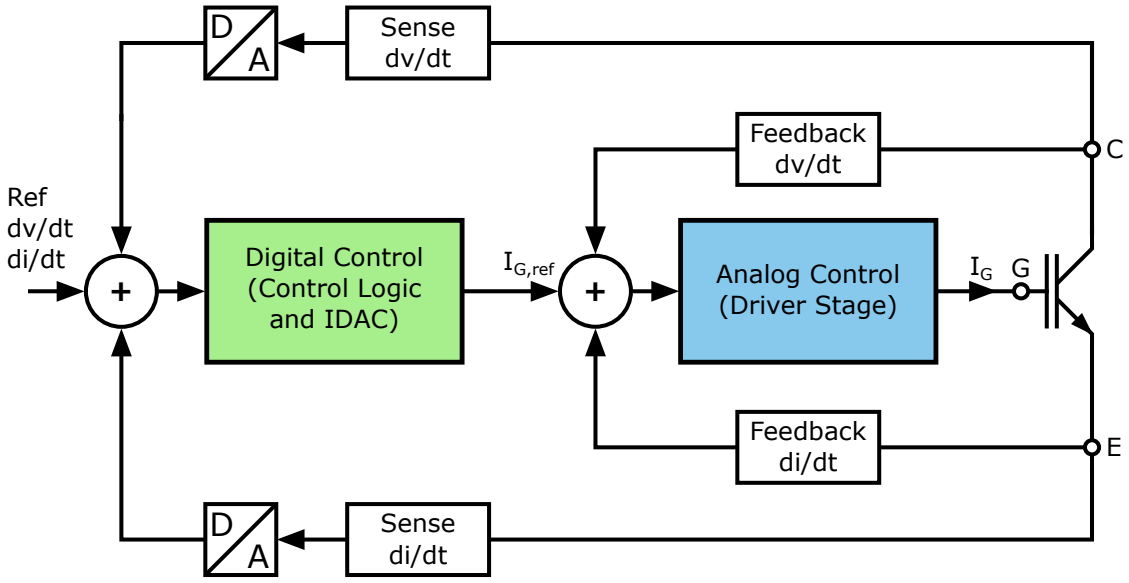


Fig. 3.1: Gate drive concept with combined digital and analog $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$, $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ control.

The continous-time control and high linearity of a closed-loop analog control are put together with the flexibility of a digital control in one system. Therefore, the gate driver is suitable for a variety of applications employing different power semiconductor devices.
The inner analog loop performs a continous-time regulation. As the analog loop is the core of the gate driver, setting the dynamics and stability of the system, it is modeled and analyzed in the small-signal domain with focus on non-linearity of parameters and operating point dependencies. System parameters affecting the dynamic stability, such as the external gate resistor and the summing node capacitance, are pointed out. In the following, a large-signal analysis is done. This demonstrates the limits of the small-signal approach, in

particular the limited control range due to the limited voltage swing in the summing node.
Another detail for the loop functionality is the sensing of $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$, as it guarantees accurate interaction between the analog and the digital loop. Hence, reliable detection of both voltage and current slopes is required. Parasitics in the sensing circuitry, affecting the sensing bandwith and accuracy, are taken into account. To gain an accurate representation of the voltage and current derivative waveforms, system parasitics are investigated and classified in three categories. Design rules for an optimized setup are derived. The digital loop, which operates in cycle-by-cycle mode as adaptive control, is implemented as a PI controller. Hence, it compensates for statistical variations in the switching speed of the driven switch, as well as for statistical variations of the analog loop. This enables a highly precise control for any unipolar or bipolar gate-controlled power semiconductor device.
As a result of the analysis, a list of design requirements is created for the example of a motor drive application.

3.2 The Analog Loop Concept

Figure 3.2 shows the analog loop in detail along with its sub-blocks.

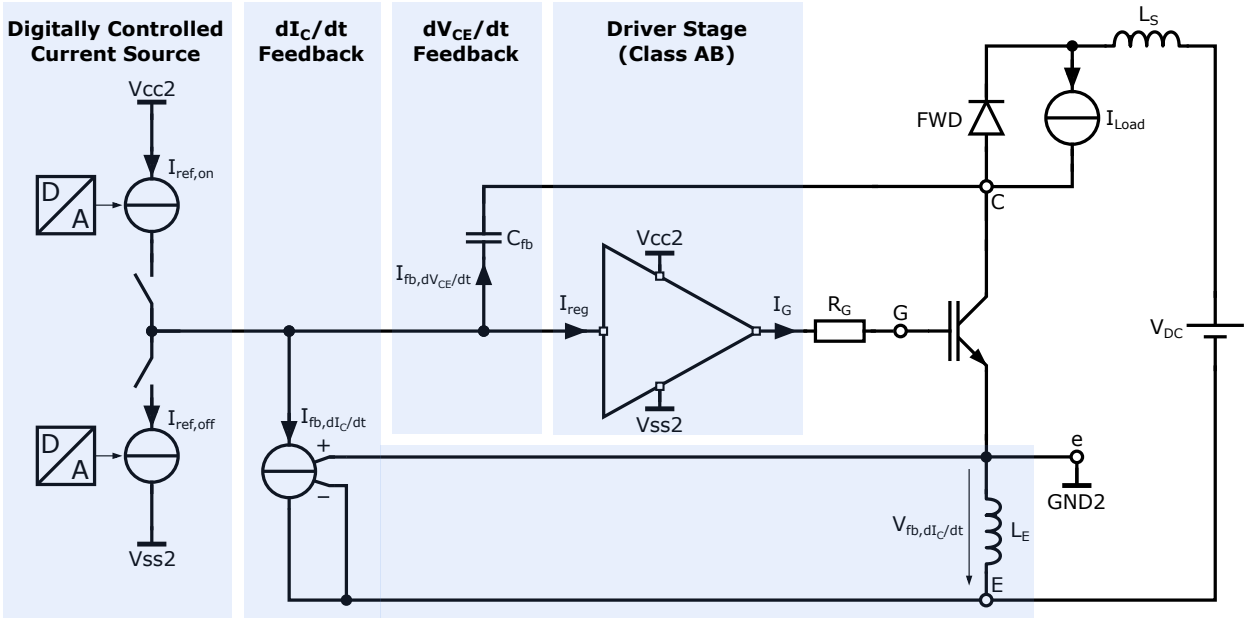


Fig. 3.2: Proposed closed-loop current slope and voltage slope control based on current regulation.

A dynamic reference current ($I_{\mathrm{ref}} = I_{\mathrm{ref,on}}$ at turn-on, $I_{\mathrm{ref}} = I_{\mathrm{ref,off}}$ at turn-off) is injected into a current summing node by a programmable digitally controlled current source. In the simplest case, the reference current is constant during the whole switching process. However, in combination with the outer digital loop shown in Fig. 3.1, this current can also be subdivided into several intervals like pre-charge delay, current rise, volt-

age rise and post-charge delay (as described for open-loop gate drive concepts in Sect. 2.3.2), which allows to independently control the current and voltage slopes. In addition, the switching delays can be reduced with a profile based reference current.

The reference current is reduced during the current and voltage switching transients by the feedback currents for $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$. This negative feedback allows to control the switching slopes effectively. The current $I_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t}$ for the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback is generated by a voltage controlled current source with transconductance G_fb. A linear behavior of the feedback current can be achieved with a constant value for G_fb. This current can be described by

$$I_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t} = G_\mathrm{fb} \cdot V_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t}. \tag{3.1}$$

The voltage $V_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t}$ is induced in the package lead inductance L_E between Kelvin (e) and power emitter (E) when the collector current changes,

$$V_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t} = L_\mathrm{E} \cdot \frac{\mathrm{d}I_\mathrm{C}}{\mathrm{d}t}. \tag{3.2}$$

This voltage drop $V_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t}$ is further utilized to sense $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ during the transient for monitoring and as an input for the digital loop [25].

The $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ feedback current $I_{\mathrm{fb},\mathrm{d}V_\mathrm{CE}/\mathrm{d}t}$ is provided by the displacement current through a high-voltage capacitor C_fb connected to collector or drain of the power device. This current is defined as

$$I_{\mathrm{fb},\mathrm{d}V_\mathrm{CE}/\mathrm{d}t} = C_\mathrm{fb} \cdot \frac{\mathrm{d}V_\mathrm{CE}}{\mathrm{d}t}. \tag{3.3}$$

The behavior of $I_{\mathrm{fb},\mathrm{d}V_\mathrm{CE}/\mathrm{d}t}$ is linear for different voltage gradients.

The regulated current I_reg, which represents the error signal of the analog loop, is given by

$$I_\mathrm{reg} = I_\mathrm{ref} - I_{\mathrm{fb},\mathrm{d}V_\mathrm{CE}/\mathrm{d}t} - I_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t}. \tag{3.4}$$

As the current and voltage transients occur subsequently (see Fig. 2.4 and 2.5), $I_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t} = 0$ during a voltage transient and $I_{\mathrm{fb},\mathrm{d}V_\mathrm{CE}/\mathrm{d}t} = 0$ during a current transient. Therefore, Eq. (3.4) simplifies to

$$I_\mathrm{reg} = \begin{cases} I_\mathrm{ref} - I_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t} & \text{during a } I_\mathrm{C} \text{ transient.} \\ I_\mathrm{ref} - I_{\mathrm{fb},\mathrm{d}V_\mathrm{CE}/\mathrm{d}t} & \text{during a } V_\mathrm{CE} \text{ transient.} \end{cases} \tag{3.5}$$

I_reg charges the parasitic capacitance of the summing node. This capacitance is dominated by the input capacitance of the driver stage. The charging of the capacitance adds an integrating behavior to the control and the regulated current is thus converted into a voltage. This voltage is then transferred to the gate of the power switch by the driver. This driver stage, which acts as an impedance converter, is used to shield the

high impedance current summing node from the transistor gate, which requires a low impedance input. The behavior of the driver can be described by

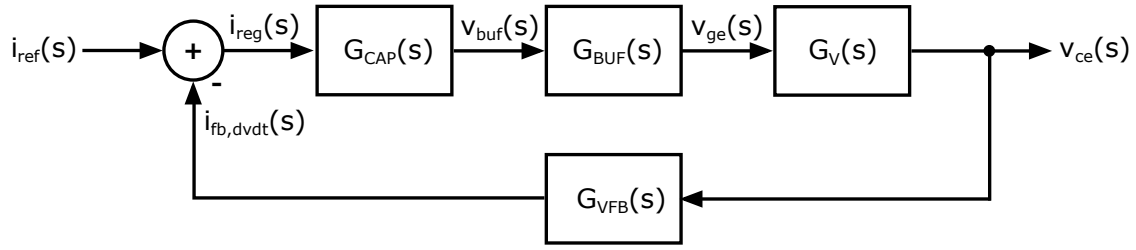
$$V_{\mathrm{out,drv}} = A_{\mathrm{V}}(j\omega) \cdot \underbrace{\left(\frac{1}{C_{\mathrm{buf,in}}} \cdot \int_0^t I_{\mathrm{reg}}(t)\,\mathrm{d}t + V_0 \right)}_{V_{\mathrm{in,buf}}}. \tag{3.6}$$

Depending on the voltage gain $A_{\mathrm{V}}(j\omega)$ of the driver, its behavior correlates either to a PI element (in case of an amplifier: $|A_{\mathrm{V}}(j\omega)|>1$) or a pure I element (in case of a voltage follower buffer stage).

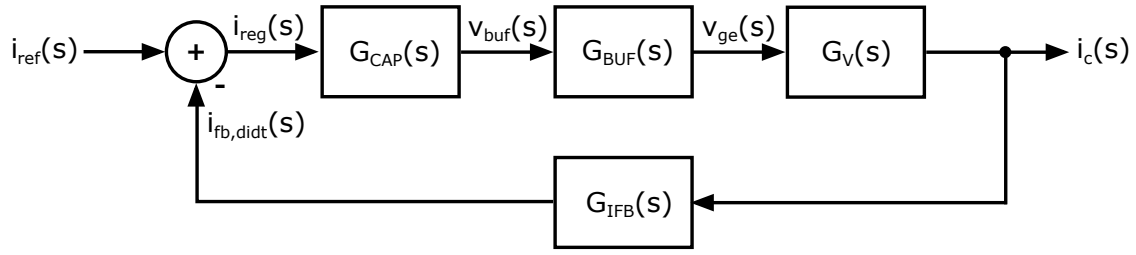
3.3 Modeling and Analysis

3.3.1 Small-Signal Modeling of the Gate Driver

The circuit can be partitioned into the blocks according to Fig. 3.2. In a hard-switched power semiconductor device, the current and voltage transitions occur subsequently, if system parasitics are kept small [32]. This circumstance allows for separate small-signal analysis of the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ loop, as only one of them is active at a time. This is a prerequisite for the operating principle of the loop concept, because a change in the regulating variable leads to a change in only one of the two controlled variables at a time. The $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback loops are depicted in Fig. 3.3 with the small-signal models of the single blocks provided in the following sections.



(a) Closed-loop control of $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$.



(b) Closed-loop control of $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$.

Fig. 3.3: Control theory view on the closed $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ regulation loops.

Power Semiconductor Device - $G_V(s)$, $G_I(s)$

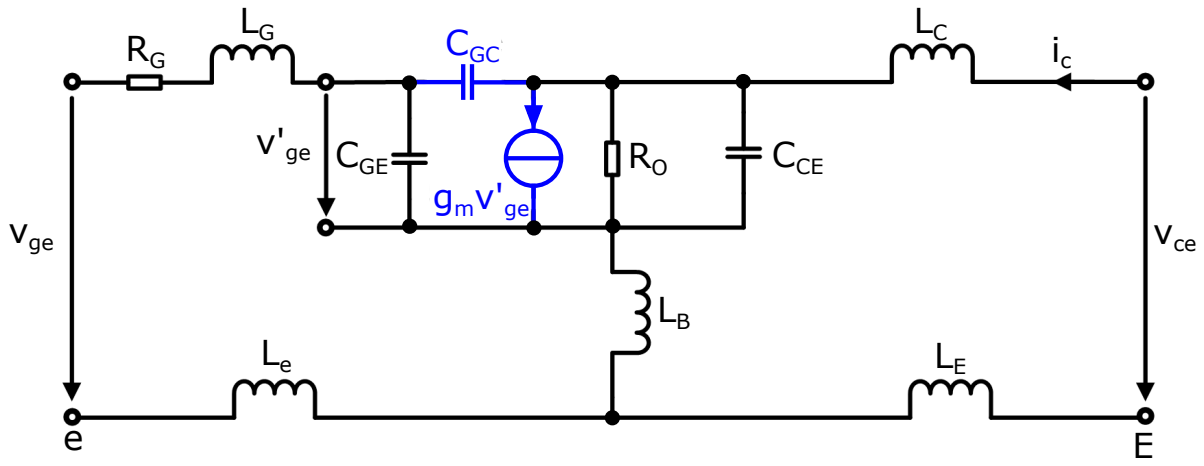


Fig. 3.4: Small-signal model of the controlled switch.

Fig. 3.4 shows a small-signal model of the power semiconductor device. This model includes all main relevant parasitics affecting the AC behavior, such as terminal capacitances and lead inductances. Two separate transfer functions can be derived on the basis of this model from the gate voltage input to a voltage output (G_V) and a current output (G_I) using circuit analysis techniques [59] [65]. Most of the component values can either be read out of the datasheet or extracted from a SPICE model, if available. However, care should be taken upon the operating point dependency of the model. The major non-linearities (C_{GC} and g_m) are highlighted in Fig. 3.4. The non-linear capacitance can be characterized by measurements. This way, the non-linear behavior can be approximated mathematically via curve-fit,

$$C_{GC}(V_{CE}) = C_2 \cdot e^{-\frac{V_{CE}}{V_2}} + C_1 \cdot e^{-\frac{V_{CE}}{V_1}} + C_0. \tag{3.7}$$

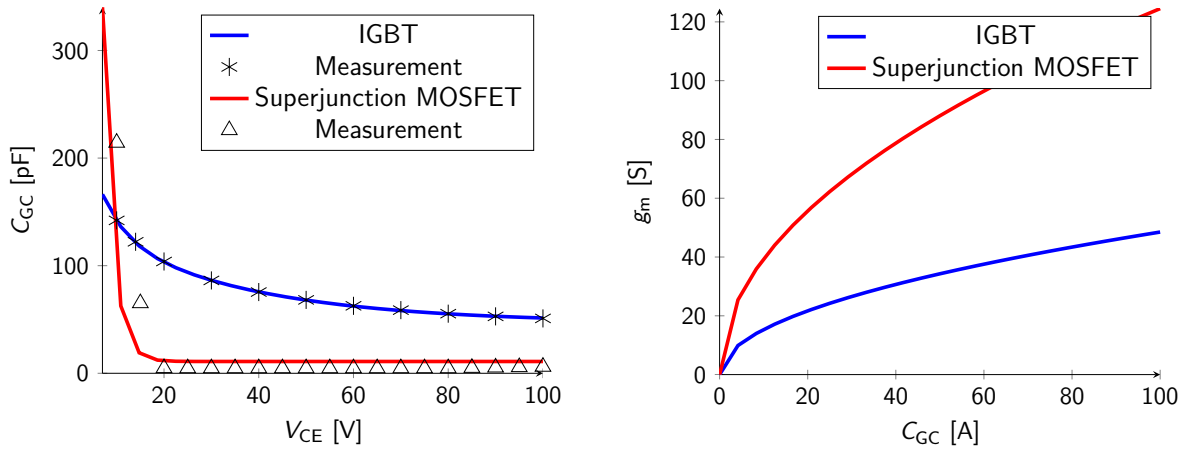
C_0, C_1, C_2, V_1 and V_2 are fitting parameters. For the transconductance, the transfer characteristic has been measured, and the MOSFET equation (which is also valid for IGBTs and further gate-controlled devices) can be fitted to it,

$$I_C(V_{Ge}) = \frac{\beta}{2} \cdot (V_{Ge} - V_{Ge,th})^2. \tag{3.8}$$

In Eq. (3.8), β can be found as a fitting parameter, and g_m can be calculated subsequently by:

$$g_m(I_C) = \frac{\partial I_C(V_{Ge})}{\partial V_{Ge}} = \sqrt{2\beta I_C}. \tag{3.9}$$

The fitted functions of the non-linearities are shown in Fig.3.5 for two examples, a discrete IGBT in trench-/fieldstop technology (IKW50N60T) [89] and a Superjunction MOSFET (IPZ65R019C7) [90].



(a) I_C **(b)** g_m

Fig. 3.5: Modeling of the measured non-linear device parameters.

Buffer Stage - $G_{BUF}(s)$

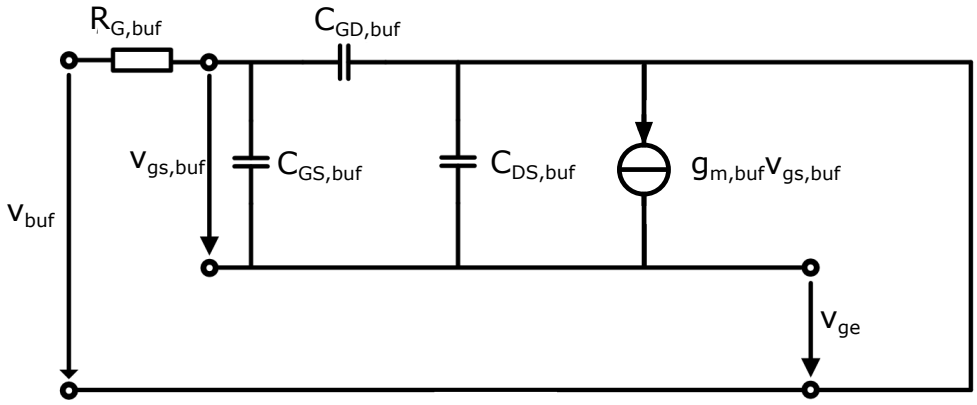


Fig. 3.6: Small-signal model of the buffer stage.

The buffer stage is assumed as a Class-B source follower output stage. Therefore, it is modeled with the small-signal model of a MOS transistor in common-drain configuration, Fig. 3.6. The transconductance $g_{m,buf}$ and the input capacitance $C_{buf,in}$ are defined by the MOS transistors in use. Therefore, their values can be read out of the corresponding datasheets.

dV_{CE}/dt **Feedback** - $G_{VFB}(s)$

The dV_{CE}/dt feedback is provided by the displacement current through a feedback capacitor, as indicated in Fig. 3.2:

$$G_{VFB}(s) = \frac{i_{fb,dV_{CE}/dt}(s)}{v_{ce}(s)} = s \cdot C_{fb}. \tag{3.10}$$

The influence of further parasitics in the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ feedback branch turned out to be negligible even for steep slopes.

$\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ Feedback - $G_{\mathrm{IFB}}(s)$

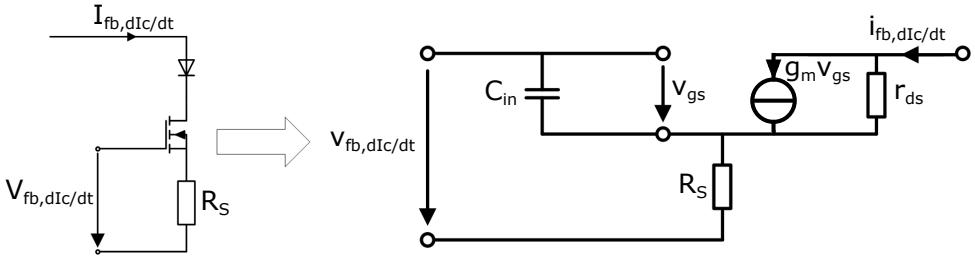


Fig. 3.7: Small-signal model of the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback.

The $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback is generated utilizing the voltage drop across the package stray inductance during the current transition ($V_{\mathrm{fb,d}I_{\mathrm{C}}/\mathrm{d}t} = L_{\mathrm{E}} \cdot \mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$). For the control mode in use, the voltage needs to be converted into a current, cf. Fig. 3.2. In order to achieve a linear conversion, a degeneration resistor R_{s} is used. The small-signal model of this voltage controlled current source is depicted in Fig. 3.7.

High-Impedance Control Summing Node - $G_{\mathrm{CAP}}(s)$

The summing node is kept high-ohmic due to the impedance-converting nature of the source follower. Thus, the incoming regulated current sees only the accumulated parasitic capacitance, which is dominated by the buffer input capacitance:

$$G_{\mathrm{CAP}}(s) = \frac{v_{\mathrm{buf}}(s)}{i_{\mathrm{reg}}(s)} = \frac{1}{s \cdot C_{\mathrm{buf,in}}}. \tag{3.11}$$

3.3.2 Small-Signal Stability Analysis

In this section, the two loops, depicted in Fig. 3.3, are analyzed for standard design parameters targeting slew rates of 1 V/ns and 100 mA/ns, which are typical for motor drive applications, as shown in Table 3.1. Figures 3.8 and 3.9 show the location of the poles and zeros for the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ loop at a typical operating point. No instabilities can be identified for the given parameter set. However, a right halfplane zero (RHPZ) appears at higher frequencies in both loops, which leads to a 90° phase lag, decreasing the system phase margin. Hence, the transit frequency of both control loops must be kept well below this value, as it represents a hard requirement on the maximum regulation bandwidth. Figure 3.10 shows the variation of the poles and zeros crossing all the operating points during a full switching transition, in a root locus plot exemplary for the IGBT under investigation.

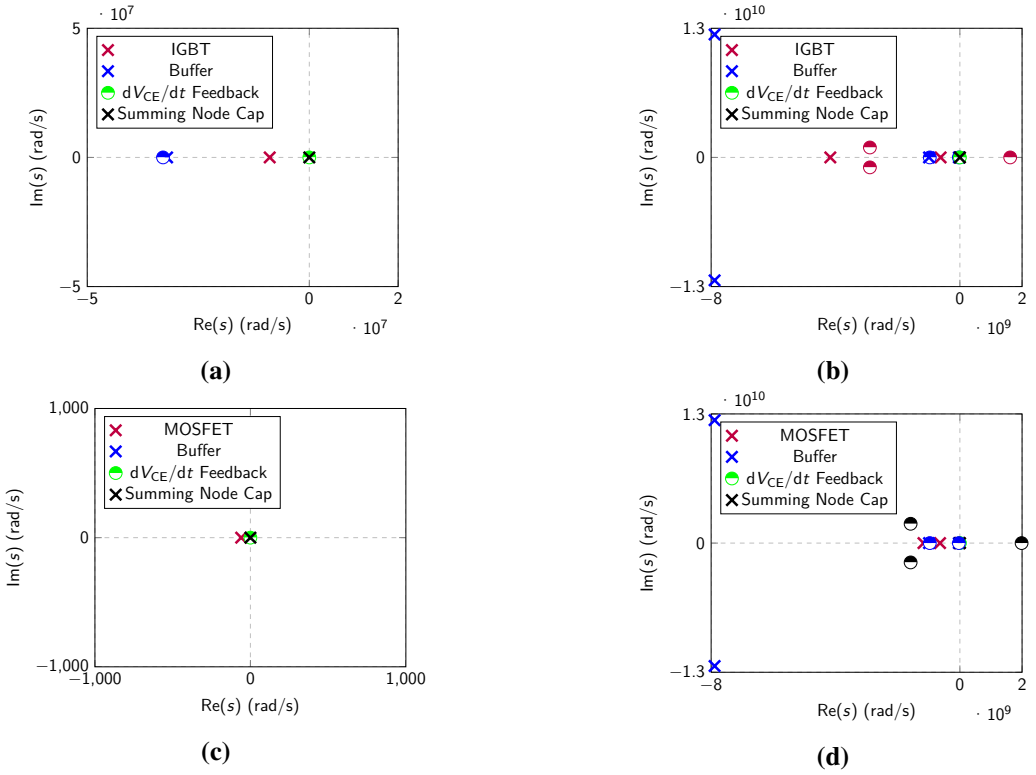


Fig. 3.8: Pole-Zero Analysis of $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ loop, for typical operating point during the switching transition (V_{CE}=360V, I_{C}=50A).

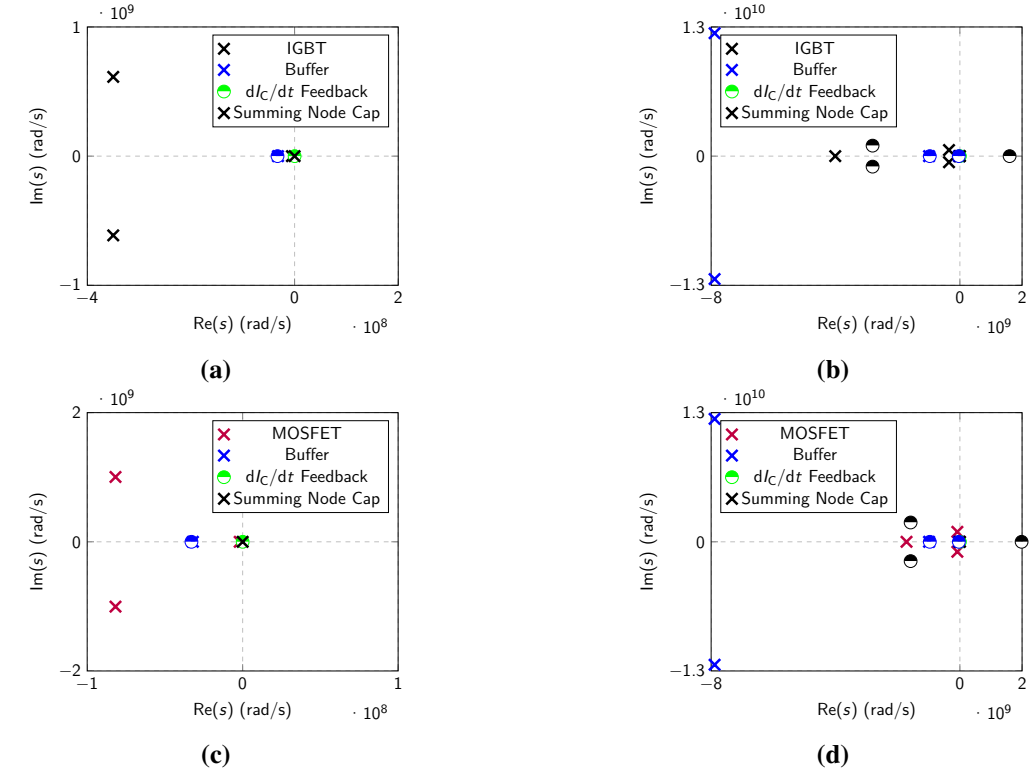


Fig. 3.9: Pole-Zero Analysis of $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ loop, for typical operating point during the switching transition (V_{CE}=400V, I_{C}=45A).

Tab. 3.1: Standard loop design parameters.

C_{fb}	R_{G}	L_{G}
10 pF	10 Ω	10 nH

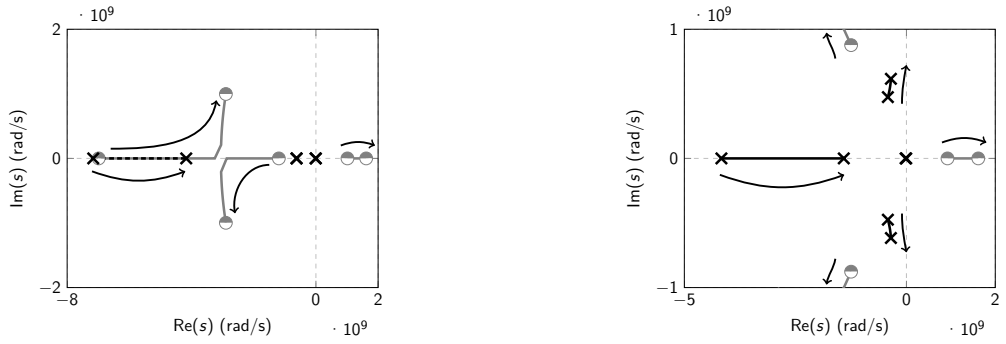
In conclusion, the system is not threatened by critical instabilities for the devices under test during the transition. However, for further different switch types outside of this analysis, the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ loop may become unstable. In such cases, stability can be maintained by reducing the loop gain, which can be achieved by (1) increasing the external gate resistor R_{G}, (2) increasing the capacitance in the summing node, or (3) modifying the feedback gain.

The left graph in Fig. 3.11 shows a root locus plot for variation of the gate resistor. R_{G} not only decreases the loop gain, but also influences instable poles. A good rule to keep the system stable has been postulated in [27]:

$$R_{\mathrm{G,min}} \geq 2 \cdot \sqrt{\frac{L_{\mathrm{G}}}{C_{\mathrm{GE}} + C_{\mathrm{GC}}}}. \tag{3.12}$$

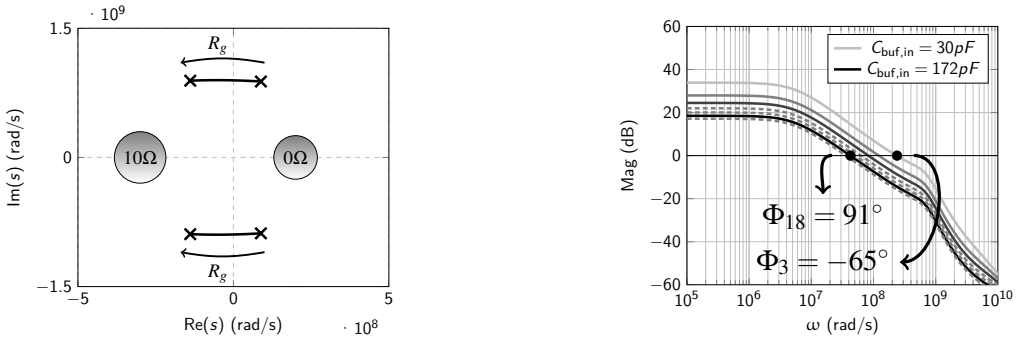
The system can achieve stable operation for any switch following the given rule. However, the amount of parasitic gate inductance determines the location of the dominant poles. Furthermore, a higher gate resistor is required, which limits gain and therefore bandwidth of the regulation loop. Hence, the regulation performance is limited by the device in use. The right graph in Fig. 3.11 shows a bode plot at varied node capacitance. It does not lead to a change of poles and zeros, but an increase reduces gain. The desired phase margin can be effectively selected using this method.

Figure 3.12 and Table 3.2 show the results of the analysis for IGBT, Superjunction MOSFET and two IGBT modules. Figure 3.12 shows the required minimum gate resistor $R_{\mathrm{G,min}}$ as a function of switch input capacitance for different values of gate inductance L_{G}. The corresponding numbers are also shown in Table 3.2. The internal gate resistor $R_{\mathrm{G,int}}$ is given as well, a value which usually can be found in the datasheets. From these results, it becomes evident that, especially for large modules, the value of $R_{\mathrm{G,min}}$ is located below the internal gate resistor, such that they can be operated without further mounting of an external gate resistor. However, for devices comprising smaller input capacitance, the use of an external gate resistor becomes necessary for typical values of the gate inductance. In conclusion, the gate inductance should be kept as low as possible to avoid oscillations in the switching trajectories, and to enable reliable operation of the closed-loop regulation.



(a) **(b)**

Fig. 3.10: Operating point variation in IGBT (*left*: V_{CE} from 10 V to 400 V for $\mathrm{d}V_{CE}/\mathrm{d}t$ loop, *right*: I_C from 1A to 50A for $\mathrm{d}I_C/\mathrm{d}t$ loop).



(a) **(b)**

Fig. 3.11: Variation of gate resistor (left) and summing node capacitance (right) to increase stability and optimize the dynamic behavior (IGBT, $\mathrm{d}I_C/\mathrm{d}t$ control).

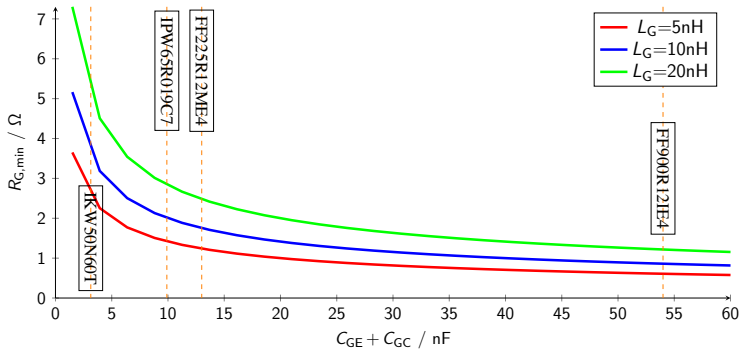


Fig. 3.12: Minimum gate resistor in dependency of the input capacitance.

Tab. 3.2: Minimum gate resistor for different types of power semiconductor devices.

Switch	Type	$C_{GE}+C_{GC}$/nF	$R_{G,int}/\Omega$	$R_{G,min}$ / Ω ($L_G = 5$nH)	$R_{G,min}$ / Ω ($L_G = 10$nH)	$R_{G,min}$ / Ω ($L_G = 20$nH)
IKW50N60T	IGBT Discrete	3.14	N/A	2.5	3.56	5.04
IPW65R019C7	CoolMOS™	9.90	0.45	1.42	2.01	2.8
FF225R12ME4	IGBT Module	13.00	3.30	1.24	1.75	2.48
FF900R12IE4	IGBT Module	54.00	1.20	0.61	0.86	1.21

3.3.3 Large Signal Transient Domain Analysis

Transient simulations of a large-signal model are utilized to analyze the control behavior and to verify the analog loop. The small-signal approach of the previous section is validated and its limits are revealed.

Simulation Setup

The simulation setup is built up according to Fig. 3.2, using the following parameters:

- Device: Discrete IGBT IKW50N60T (SPICE model).
- Load current: $I_{Load} = 20$ A.
- DC link voltage: $V_{DC} = 400$ V (selected as 2/3 of the IGBT voltage rating).
- Freewheeling diode: Turned-off IGBT (IKW50N60T).
- Driver/Buffer Stage: Equivalent circuit of a source follower (common drain stage), with two different input capacitances $C_{buf,in1} = 10$ pF and $C_{buf,in2} = 130$ pF (shown in Fig. 3.13). For simplification, the input capacitance is distributed to the two terminals.

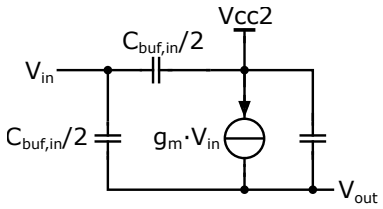


Fig. 3.13: Source-follower model with parasitic input and output capacitance.

- dI_C/dt feedback: Ideal voltage controlled current source, with $G_{fb} = 20$ mA/V.

- $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ feedback: Ideal capacitor with $C_{\mathrm{fb}} = 10$ pF.
- Reference currents: Constant currents, $I_{\mathrm{ref,on}} = I_{\mathrm{ref,off}} = 10$ mA.
- External gate resistor: $R_{\mathrm{G,ext}} = 10\,\Omega$.
- Stray inductance: $L_{\mathrm{S}} = 100$ nH.
- Parasitic inductance in the gate path (not shown in Fig. 3.2): $L_{\mathrm{G}} = 10$ nH.

Nonlinearity in the First Slope

Figue 3.14 shows simulations for turning on and off the IGBT under investigation at a large-signal input step, for two different input capacitances $C_{\mathrm{buf,in}}$ of the buffer (10 pF and 130 pF). $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ show nearly linear behavior due to the closed-loop regulation for low buffer input capacitance.
However, for larger input capacitances, there is a non-linearity in the first slope of the switching operation ($\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ at turn-on and $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ at turn-off). This is mainly caused by the high input capacitance, as the settling of the buffer output takes much longer.
The input capacitance of the buffer stage is mainly defined by the input capacitance of the high-voltage DMOS transistors due to their large geometry. Therefore, the settling behavior can only be improved by reducing the dimension of the driver output stage, which results in a lower driving capability.
From a control theory point of view, the described problem can be identified as a windup effect, which occurs in controllers with integrating behavior and limited control range of the actuating variable (see Fig. 3.15). When the controlling element is in saturation ($|u(t)| \geq u_{\max}$), the control loop is further fed with a constant input variable ($\pm u_{\max}$) independent of the output y. Therefore, the feedback is no longer active, and the control is operated in open-loop. Although u^* cannot be further increased, the integral part u_{i} of the actuating variable is further increased due to the continuous integration of the control error e. As soon as the control error e changes its sign (due to active feedback), the integral part u_{i} of the actuating variable gets smaller and the control loop is operating in closed-loop. During the settling phase of u_{i}, the output y overshoots.
An approach for an improved settling behavior without reducing the driving capability would be the implementation of an anti-windup circuit, which is a later part of this research (see Sect. 4.2).

3.4 Optimized $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$, $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ Sensing

In order to guarantee for safe and correct interaction between the analog and the digital loop, the sensing circuits must be designed for sufficient bandwidth and accuracy. The focus of the following sections is on

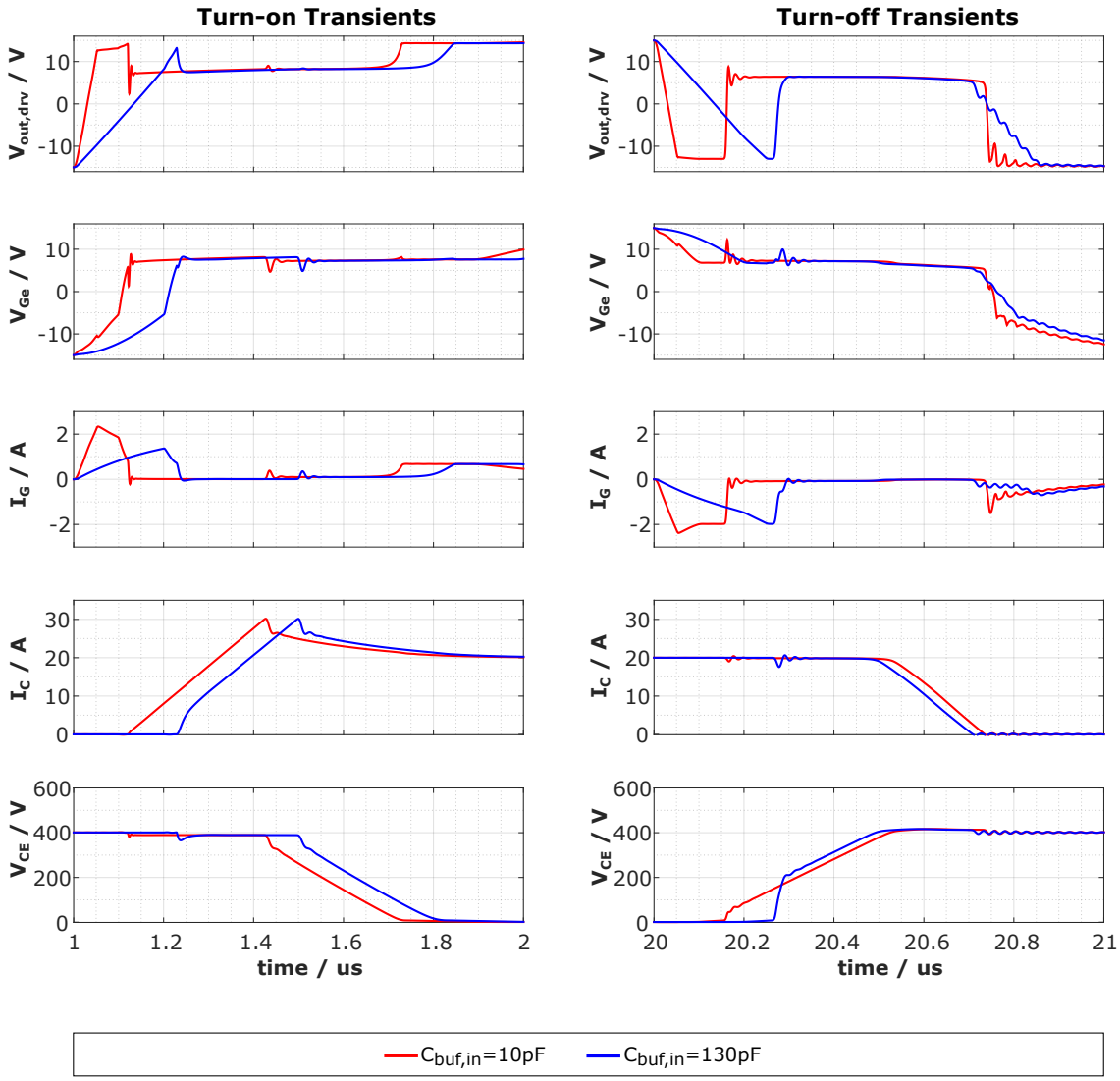


Fig. 3.14: Turn-on and turn-off transient signals (V_{CE}, I_C, V_{Ge}, $V_{out,drv}$, I_G) with an equivalent circuit of a source-follower with different input capacitances ($C_{buf,in} = 10$ pF and $C_{buf,in} = 130$ pF) as driver stage.

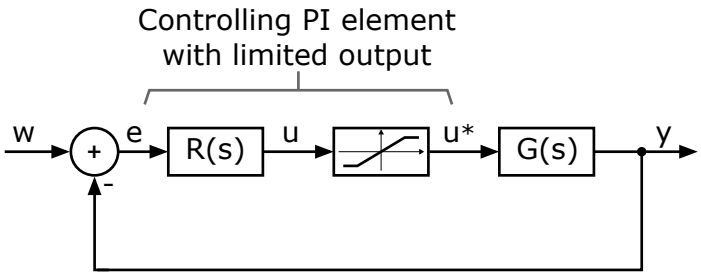


Fig. 3.15: Control loop comprising a PI element with limited output.

sensing methods to detect both derivatives ($\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$) based on the natural differential behavior of capacitance and inductance. Similar techniques are already in use in analog feedback loops regulating $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ [91], [67]. In [92], a technique for current sensing utilizing the emitter lead inductance L_{E} in IGBT modules is presented. The derivatives can be sensed and stored for further digital signal processing by sampling with a high-speed analog-to-digital converter (ADC). In order to achieve an accurate conversion over the full bandwidth, parasitics need to be taken into account and kept small. As the fast switching transients of modern power semiconductor devices come along with higher frequency components, bandwidth optimization is necessary. Therefore, parasitics apparent in the setup are investigated and classified into three domains. Based on these results, guidelines for an optimized printed circuit board (PCB) design are derived, which enables the sensing of steep slopes. In the end of this section, the proposed approach is experimentally verified using a hard-switching IGBT power stage of newest trench-/fieldstop technology. This confirms the ability to effectively record the high slew rates of a modern generation switch.

3.4.1 $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ Sensing

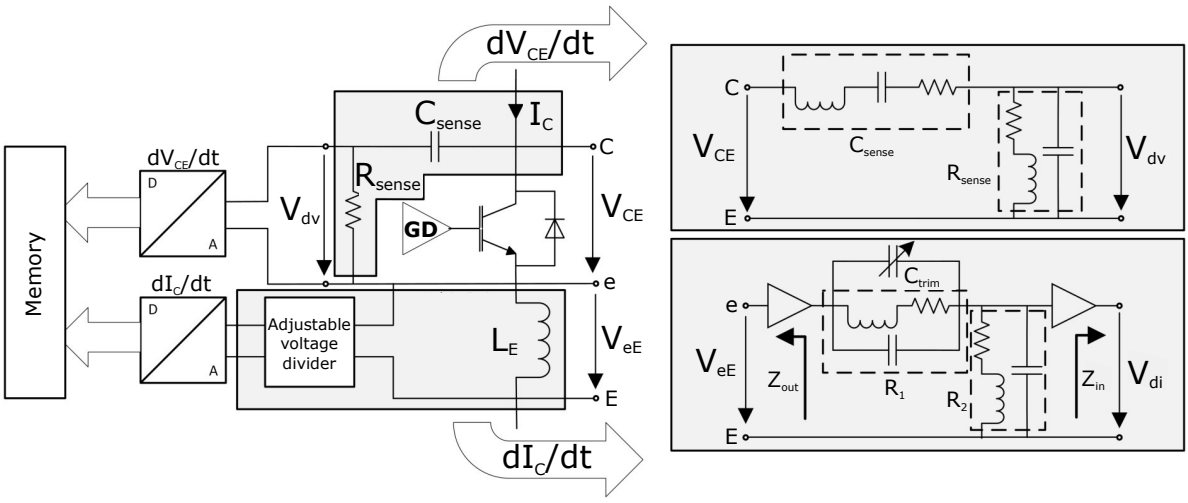


Fig. 3.16: $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ Sensing Concept.

Figure 3.16 shows the sensing circuitry for the case of a low-side IGBT, which can be partitioned into three sub-blocks, the analog sensing network, a high-speed ADC and an static random-access memory (SRAM) memory block, to store the acquired data for further digital signal processing, such as optimization algorithms. The $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ sensing circuit is formed by a RC high-pass connected to the switching node. The ideal transfer function $H(s)$ is represented by

$$H(s) = \frac{V_{\mathrm{di}}}{V_{\mathrm{CE}}} = \frac{s \cdot R_{\mathrm{sense}} C_{\mathrm{sense}}}{s \cdot R_{\mathrm{sense}} C_{\mathrm{sense}} + 1} = \frac{s}{s + \frac{1}{R_{\mathrm{sense}} C_{\mathrm{sense}}}} = \frac{s}{s + s_0}. \tag{3.13}$$

A time derivative is represented by a multiplication with s in the Laplace domain. Hence, Eq. 3.13 indicates

that the linearity of the sensing network is limited due to the pole introduced by the highpass filter. However, in the range below the 3dB corner frequency $s_0 = 1/R_{\text{sense}}C_{\text{sense}}$, the following approximation can be applied:

$$H(s) = \frac{s}{s+s_0} \quad \overrightarrow{s < s_0} \quad H(s) \approx \frac{s}{s_0} = s \cdot R_{\text{sense}}C_{\text{sense}}. \tag{3.14}$$

R_{sense} and C_{sense} are chosen to scale a maximum $\mathrm{d}V_{\text{CE}}/\mathrm{d}t$ to the ADC full-scale input, in order to obtain a good signal-to-noise ratio.

The $\mathrm{d}I_{\text{C}}/\mathrm{d}t$ sensing method utilizes the additional Kelvin-emitter pin, which is available at the latest discrete devices in TO-247-4 packages [93]. The emitter pin can be utilized for both $\mathrm{d}I_{\text{C}}/\mathrm{d}t$ measurement and analog loop feedback without unwanted additional inductance. The sensed voltage at the ADC input is

$$V_{\text{di}}(t) = \delta \cdot L_{\text{E}} \cdot \frac{dI_{\text{C}}(t)}{dt}. \tag{3.15}$$

Table 3.3 shows typical peak $\mathrm{d}I_{\text{C}}/\mathrm{d}t$ values and corresponding peak voltage drops across a typical emitter inductance (L_{E} = 5nH). The voltage exceeds 1 V even for moderate $\mathrm{d}I_{\text{C}}/\mathrm{d}t$ in applications like motor drives. Hence, an attenuation factor δ is added by a subsequent voltage divider to scale the signal swing to the full-scale input range of the ADC. To ensure that no signal information is lost, the Nyquist theorem has to

Tab. 3.3: Typical peak $\mathrm{d}I_{\text{C}}/\mathrm{d}t$ and sensed peak voltage for L_E = 5nH.

Peak $\mathrm{d}I_{\text{C}}/\mathrm{d}t$ (A/ns)	**Peak Voltage** (V)
0.1	0.5
0.5	2.5
1	5

be fulfilled for the highest $\mathrm{d}I_{\text{C}}/\mathrm{d}t$ and $\mathrm{d}V_{\text{CE}}/\mathrm{d}t$ signal frequency component, which puts a requirement on the minimum bandwidth of the sensing network and on the ADC sampling frequency.

3.4.2 Influences of Parasitics in $\mathrm{d}V_{\text{CE}}/\mathrm{d}t$ Sensing

The introduced sensing network in Fig. 3.16 is limited in bandwidth due to parasitics, non-ideal elements and frequency-dependent load (ADC input). This leads to a couple of unwanted effects that attenuate parts of the signal. The parasitics apparent in the setup, can be classified into three domains and are explained below.

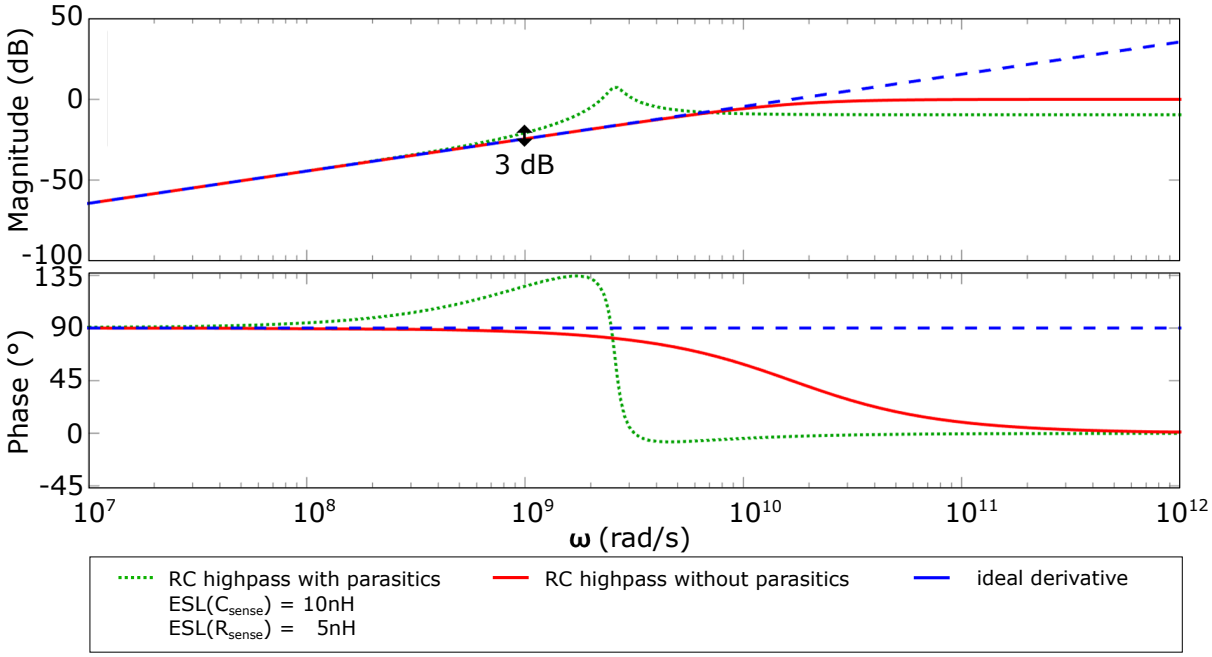


Fig. 3.17: Bode plot: ideal voltage derivative (blue), sensed by ideal high-pass (red) and including parasitics (green) for C_{sense} = 10 pF and R_{sense} = 6 Ω.

Component Parasitics

Equivalent circuit models of utilized passive components R_{sense},C_{sense} have been extracted from s-parameter measurements. They have been de-embedded using a short-open-load-thru (SOLT) technique and a curve-fitting algorithm inside the RF design tool *Keysight Advanced Design System (ADS)*. The circuit equivalent of the models are depicted in Fig. 3.16. The capacitance equivalent series resistance (ESR) and the parasitic capacitance of the resistor were found to be of negligible influence.
Hence, the transfer function $H(s)$ introduced in the previous section (see Eq. (3.13)) changes to

$$H_{\text{par}}(s) = \frac{s \cdot C_{\text{sense}}(sL_{\text{R}} + R_{\text{sense}})}{s^2 \cdot (C_{\text{sense}}L_{\text{C}} + C_{\text{sense}}L_{\text{R}}) + s \cdot R_{\text{sense}}C_{\text{sense}} + 1}. \tag{3.16}$$

Figure 3.17 analyzes the deviations in the sensed $\mathrm{d}V_{\text{CE}}/\mathrm{d}t$ brought in by the parasitic inductances, which lead to a limitation in linearity. As an upper boundary of the linear region, $f_{3\text{dB}}$ refers to the frequency at which the difference from an ideal linear curve (multiplication with s) is equal to 3 dB. Hence, it represents the limit of sensing accuracy and bandwidth. At this point, the measurement circuit leaves its linear operation range. In an optimized setup, parasitic inductance values must be kept below these stated values in order to increase the bandwidth to resolve the highest frequency component.
For a 10 pF capacitor with an equivalent series inductance (ESL) of L_{C} = 10 nH and a 6 Ω resistor with

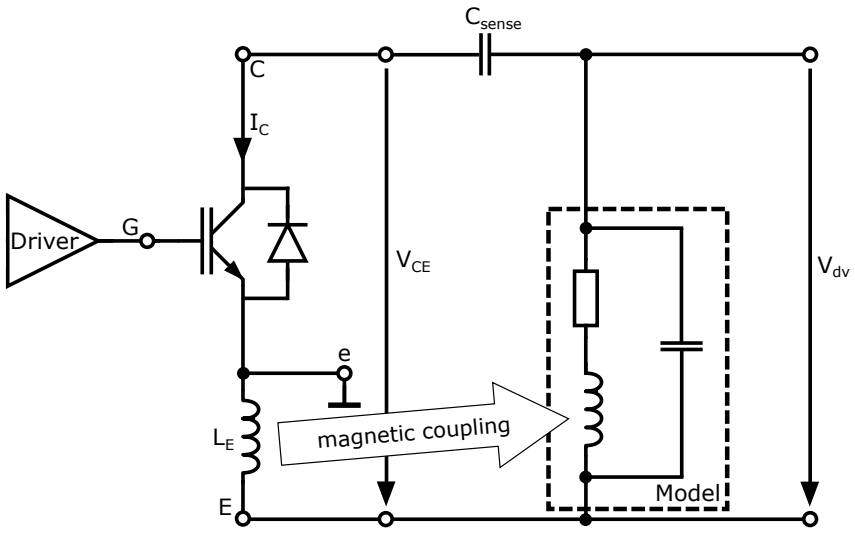


Fig. 3.18: Magnetic coupling in $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ sensing.

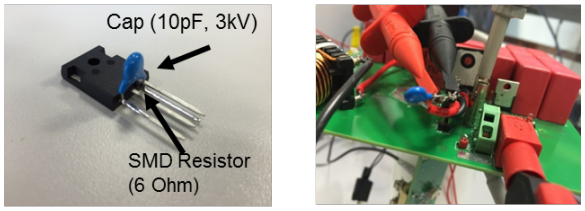


Fig. 3.19: $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ test setups.

$L_{\mathrm{R}} = 5$ nH ESL, the 3dB corner frequency is located approximately at

$$f_{3\mathrm{dB}} = \frac{10^9 \text{ rad/s}}{2\pi} = 159 \text{ MHz}. \tag{3.17}$$

Assuming a sinusoidal waveform, the maximum $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ can be approximated as follows:

$$V(t) = V_0 \cdot \sin(2\pi f t), \tag{3.18}$$

$$\frac{dV(t)}{dt} = 2\pi f \cdot V_0 \cdot \cos(2\pi f t), \tag{3.19}$$

$$\max\left(\frac{dV(t)}{dt}\right) = 2\pi f \cdot V_0. \tag{3.20}$$

From Eq. (3.20), we can postulate that, for $f_{3\mathrm{dB}} = 159$ MHz and $V_{\mathrm{DC}} = 400$ V, accurate and linear sensing is possible up to 400 V/ns. This provides a sufficiently high bandwidth for typical values of $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$, see Fig. 2.4. The bandwidth should be high enough to capture ringing caused by the parasitic device inductances and capacitances [28], which can lead to frequency components in the range of more than 100 MHz for the transients. In order to achieve high linearity, low-inductive Surface-mount device (SMD) components should be used and traces should be kept short. There are ceramic capacitors with linear behavior for

different high voltage levels available on the market [94].

PCB / Circuit Design

At turn-on, the voltage transient does not start before the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ transition has fully completed and the current has reached the level of the load current ($I_\mathrm{C} = I_\mathrm{Load}$) (see Fig. 2.4, interval III). Hence, the $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ signal should stay at zero. In reality, the signal can be different from zero due to magnetic coupling, which results from the current transient apparent through the stray inductance, and it couples to the parasitic inductance of the sense resistor (see Fig. 3.18). Two test setups have been tested in a hard-switched IGBT power stage depicted in Fig. 3.19. In the left one, the passives have been directly mounted on the IGBT pins. Distances and thus parasitic inductances are kept small, but the magnetic coupling effect is very high. Moving the sensing circuitry further away from the IGBT adds parasitic inductance, such that a trade-off has to be found between the amount of equivalent series inductance shrinking bandwidth and lowering this parasitic coupling effect, depending on the application.

Board Interconnections

As the analog circuitry needs to be connected to an external digital signal processing (DSP) unit (FPGA), shielded cables must be used as interconnect to avoid coupling effects, such as coaxial cables (SMA, BNC) or shielded twisted pair (STP). Twisted pair cables are an effective solution at low cost to achieve a trade-off between parasitic effects depending on the application requirements.

3.4.3 Influences of Parasitics in $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ Sensing

Component Parasitics

The series inductance, present between the two emitter pins, has been modeled on the basis of s-parameter measurements (Fig. 3.21). The series inductance value, which consists of a Kelvin emitter part L_e and a power emitter part L_E, can be extracted by converting the s-parameters to y-parameters and applying the following formula [95],

$$L_\mathrm{e}(f) + L_\mathrm{E}(f) = -\mathrm{Im}\left(\frac{1/Y_{21}(f)}{2\pi f}\right). \tag{3.21}$$

In Eq. (3.21), Y_{21} results from the y-parameters achieved through the measurements. The extracted inductance value varies slightly in frequency, but can be approximated by a fixed value, which is 10 nH in this example (Fig. 3.22). As it splits approximately by half due to the geometry considerations (L_e and L_E,

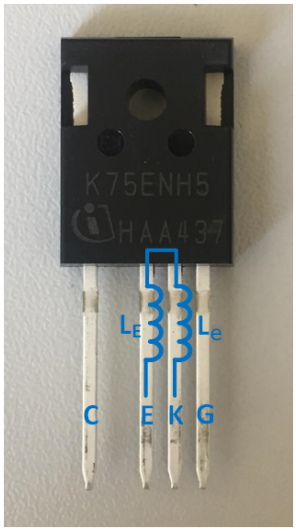


Fig. 3.20: TRENCHSTOP^{TM} 5 IGBT (Infineon) in TO-247-4 package with additional kelvin emitter pin.

cf. Fig. 3.20 and Fig. 3.21), the emitter inductance used for sensing $\mathrm{d}I_C/\mathrm{d}t$ (L_E) can be assumed as 5 nH over a wide bandwidth. It can be assumed, that the value of 5 nH is a good estimation for different kind of TO-247-4 devices. The influence of the gate current magnitude on the $\mathrm{d}I_C/\mathrm{d}t$ measurement turned out to be negligible for the target high power devices.

PCB / Circuit Design

The full-scale input of high-speed ADCs is in the sub-volt region. However, for typical switching speeds, the sensed value will exceed 1 Volt. Hence, a high-bandwidth voltage divider is necessary. The highest frequency component of the $\mathrm{d}I_C/\mathrm{d}t$ waveform is the ringing due to the resonant circuit formed by parasitic emitter inductance and gate-emitter capacitance, which takes place after the reverse-recovery effect has completed (see Fig. 2.4, interval III). Typical values exceed 100 MHz in modern IGBTs and Superjunction MOSFETs. To gain higher bandwidth, the component parasitics are compensated by a trimming capacitor (Fig. 3.16). However, a pure resistive divider with a compensation capacitor is dependent on the input and output impedance and will have to be renewed if the load at the output (ADC, Oscilloscope, etc.) is changed. An optimized solution is to buffer the input in order to protect the signal and provide enough current, while a second buffer at the output is leading to independency of the load in use (see in Fig. 3.16). In this realization, the buffer is formed by an operational amplifier in voltage follower configuration.

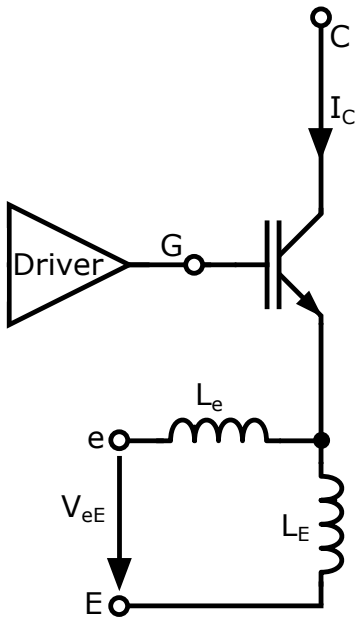


Fig. 3.21: Kelvin-emitter equivalent circuit.

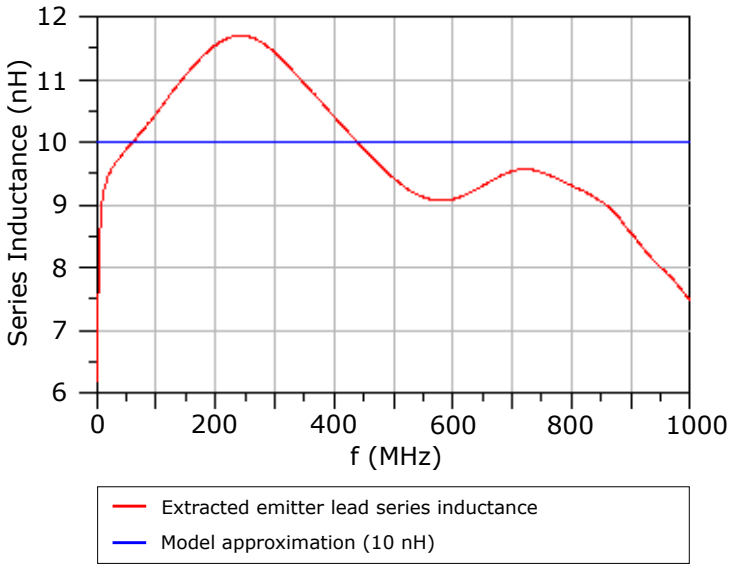


Fig. 3.22: Extracted emitter-inductance (red), 10 nH model approximation (blue).

3.4.4 Optimized Setup

Using the knowledge about the different parasitics as design guidelines, printed circuit boards comprising the $\mathrm{d}I_C/\mathrm{d}t$ and $\mathrm{d}V_{CE}/\mathrm{d}t$ sensing circuitry have been built up, optimized based on the results outlined in the previous sections. To keep the equivalent circuit inductances small, SMD components have been chosen. A trade-off between avoiding $\mathrm{d}I_C/\mathrm{d}t$ coupling and resolution has been found experimentally for the case of a trench-/fieldstop IGBTs. The sensing networks are placed on a separate board in a distance of approximately

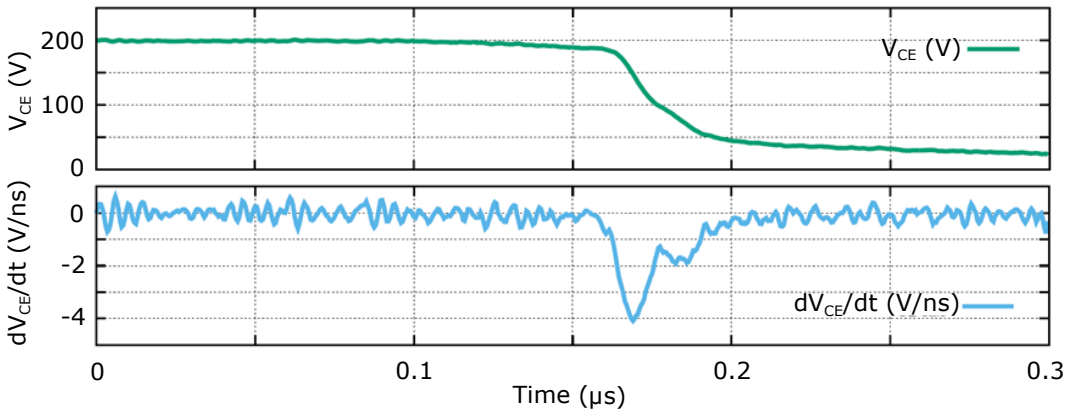


Fig. 3.23: Voltage transient and calculated derivative $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ for a hard-switched IGBT turn-on.

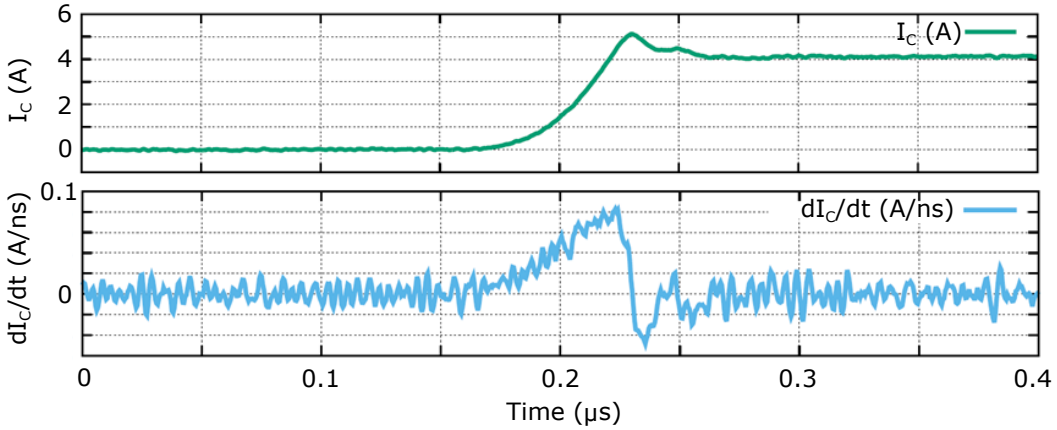


Fig. 3.24: Current transient and calculated derivative $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ for a hard-switched IGBT turn-on.

5-10 cm from the power switch. The power and sensing boards are directly interconnected by twisted pair cables. $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ sensing results of the optimized setup are presented in Figures 3.23 to 3.25. Figures 3.23 and 3.24 show an oscilloscope measurement of the voltage and current transition. The corresponding derivatives are shown below the measurements. They are mathematically calculated from the measured absolute values in MATLAB. Figure 3.25 shows the sampled values with the 8 Bit, 1.5 GSps ADC utilized in the slope shaping system (ADC08D1520), as described in Chapter 5. All relevant signal parts are sensed, including reverse recovery and high frequency emitter ringing.

The optimized sensing network leads to significant improvements compared to reference solutions, like a direct measurement through a bandwidth compensated voltage divider. It avoids DC power consumption and leads to an accurate calculation in the analog domain. Less complex compensation is necessary and DC current paths are avoided.

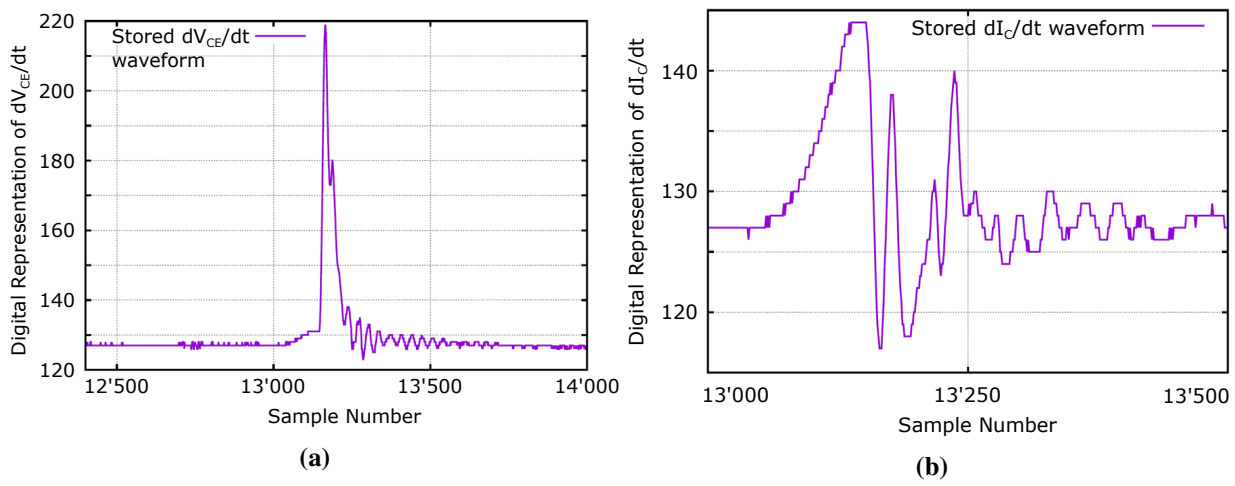


Fig. 3.25: Aquired digital waveforms of $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$.

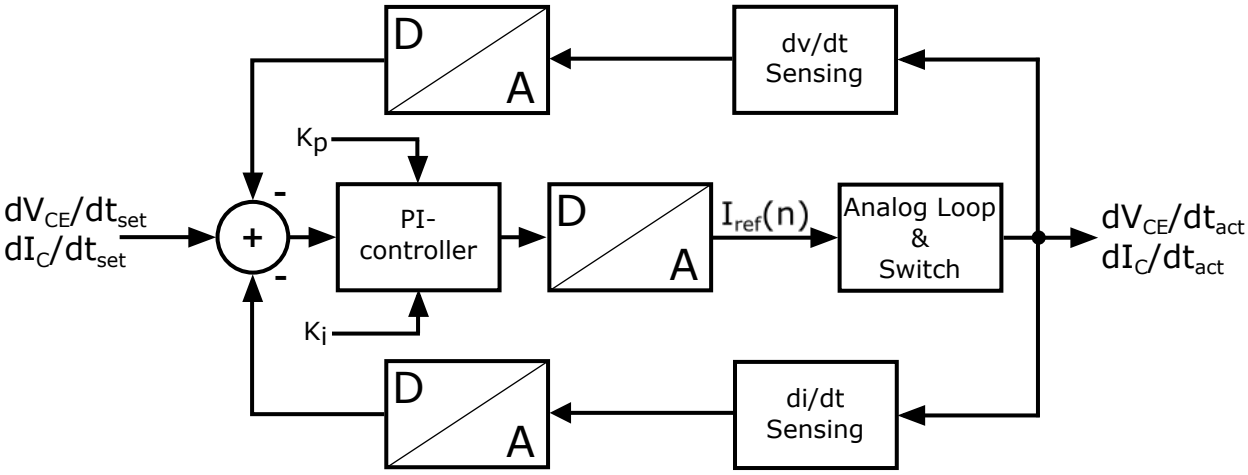


Fig. 3.26: Concept of the digital closed-loop control.

3.5 The Digital Loop Concept

Figure 3.26 shows the concept of the digital loop, derived from Fig. 3.1. The plant consists of the analog loop and the power switch. In this work, the digital signal processing (DSP) has been realized using a standard PI control algorithm. Unlike the analog loop, the digital loop is active between the switching cycles and calculates a new value for reference current I_{ref}, which is fed into the analog loop during the next cycle. The reference current of cycle n is calculated by:

$$i_{\mathrm{ref}}(n) = i_{\mathrm{ref}}(n-1) + K_{\mathrm{p}} \cdot e(n) + K_{\mathrm{i}} \cdot e(n-1) \tag{3.22}$$

If individual control of both $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ is required, the reference current can also be subdivided into different intervals (as described for open-loop gate drive concepts in Sect. 2.3.2). In this case, separate

reference values for current and voltage slew rate are calculated in each cycle.
Due to the adaptive principle, control errors and statistical variations of the analog loop and dependencies on the driven device are compensated. As shown in experiment as part of this work (see Chapter 5), an improvement in precision by more than 10% is achieved in the control compared to the purely analog regulation. Furthermore, analog regulation requires user knowledge about the reference current that must be injected to obtain the desired $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and/or $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$. Hence, some kind of look-up table is necessary to link the reference currents to the corresponding slew rates. In order to shrink the control variation, the reference current needs to be adjusted manually. However, together with the digital loop, no knowledge about the reference current levels is required and no initial condition needs to be set, as the adaptive control will set the programmed values of $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ automatically after few switching cycles. In numbers, this increases the potential for the improvement in precision by far more than the improvement in performance that is claimed in this thesis.

3.6 System Requirements

In the following section, the requirements of the slope shaping system are defined, fitting the system to the application of motor drives. The individual requirements for the particular blocks, such as the driver stage or the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback, are discussed later within Chapter 4.
First, the desired range of $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ has to be defined. In general, it is desired to switch with the highest speed possible, as this will reduce the switching losses. However, higher $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ switching speed increases the voltage and current stress on the semiconductor. Therefore, the SOA of the power device has to be taken into account as a requirement. From the application point of view, the maximum ratings of an electric motor and the influence of long motor cables have to be considered, as well. If the cable between inverter and motor exceeds a critical length, a standing wave and full voltage reflection could occur, which doubles the voltage gradient from the inverter output to the input of the motor [28]. Hence, the requirements of Eq. (2.17) and (2.18), for a maximum $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$, need to be fulfilled.
For the stability of the control loop, it has been postulated in Sect. 3.3.2 that the gate resistor R_{G} is an important factor. The input capacitance C_{GE}, the sum of all parasitic inductances in the gate path $\sum L_{\mathrm{G}}$ and the gate resistor R_{G} form an *RLC* resonant circuit. The minimum value of the gate resistor $R_{\mathrm{G,min}}$, that does not lead to oscillations is defined on the basis of Eq. (3.12), which can be simplified using the following approximation for practical use:

$$R_{\mathrm{G,min}} \geq 2\sqrt{\frac{\sum L_{\mathrm{G}}}{C_{\mathrm{GE}}+C_{\mathrm{GC}}}} \approx 2\sqrt{\frac{\sum L_{\mathrm{G}}}{C_{\mathrm{GE}}}}. \tag{3.23}$$

The closed-loop concept is tested with the IGBT IKW50N60T (600 V, 50 A, trench-/fieldstop technology) [89]. The according values of the IGBT and the test bench are $C_{\mathrm{GE}} = 3.047$ nF and $\sum L_{\mathrm{G}} = 13$ nH. Thus, the minimum theoretical gate resistor can be calculated as

$$R_{\mathrm{G,min}} \geq 2\sqrt{\frac{13\ \mathrm{nH}}{3.047\ \mathrm{nF}}} = 4.13\ \Omega.$$

The actual value for R_{G} is kept higher than $R_{\mathrm{G,min}}$ to prevent oscillations and unstable behavior during the slope control.
The requirements for the digitally controlled current source are suggested as follows:

- Resolution: $\sim$ 5 bit + 1 signature bit (bipolar use as sink/source)
- Full-scale output current: $\pm$1 mA up to $\pm$100 mA
  (depends on the loop gain)
- Output voltage compliance: $\pm$1.65 V up to $\pm$15 V
  (depends on the voltage gain of the driver/buffer stage)
- Current settling time: $<$ 10 ns

The external feedback capacitor needs to have at least the dielectric strength of the power switch that is driven. It is preferred that the voltage class for the capacitor is located 2-3 times above the V_{max} to prevent damages. For the specific application, the external feedback capacitor C_{fb} needs a minimum voltage capability equal to the maximum blocking voltage of the IGBT ($\sim$ 600 V). Furthermore, it can be realized either as a printed circuit board (PCB) integrated capacitor [96] or as discrete element (ceramic capacitor). Feasible values are in the range of 1 pF to 100 pF. The actual size of C_{fb} depends on the loop gain (gain of the driver stage) and thus it will be chosen later. Table 3.4 summarizes the requirements of the system and also lists the requirements of the individual blocks, which will be discussed and analyzed in the following sections.

Tab. 3.4: Requirement list for the slope shaping system core fitted to motor drive application.

Requirement	Quantity	Min	Nom	Max	Unit	Comment
Absolute maximum ratings	V_{CC2} (positive supply)			20	V	Datasheet [89]
	V_{SS2} (negative supply)	-20			V	
	$V_{CC2} - V_{SS2}$		40		V	
Operating range	V_{CC2} (positive supply)			15	V	Datasheet [89]
	V_{SS2} (negative supply)	-15			V	
	$V_{CC2} - V_{SS2}$		30		V	
Slew rate control range	$\mathrm{d}I_C/\mathrm{d}t$ control range	0.1		1.0	A/ns	Table 2.3
	$\mathrm{d}V_{CE}/\mathrm{d}t$ control range	0.5		2.5	V/ns	[40], [16]
Minimum gate resistor	R_G	4.13			Ω	Equation (3.23)
Driver Stage	Driving capability			5.1	A	see Section 4.1
	Output voltage swing	-15		15	V	
	Output slew rate SR_{drv}		1		V/ns	
	DC Voltage gain					
$\mathrm{d}I_C/\mathrm{d}t$ feedback	$\mathrm{d}I_C/\mathrm{d}t$ input range	±0.1		±1.0	A/ns	see Section 4.3.3
	G_{fb}				S	
	Max. signal input voltage				V	
$\mathrm{d}V_{CE}/\mathrm{d}t$ feedback	$\mathrm{d}V_{CE}/\mathrm{d}t$ input range	±0.5		±2.5	V/ns	
	C_{fb}	1		100	pF	Equation (3.3)
	Capacitor voltage rating	600	1200		V	
	Linearity over voltage			1200	V	
	Linearity over frequency			100	MHz	
Digital current source	Full-scale range	±1		±100	mA	bipolar
	Resolution		6		Bit	
	Output voltage compliance	±1.65		±15	V	
	Current settling time			10	ns	
Quiescent current	$I_{q,drv}$			1	mA	

4 Analog Loop Design and Evaluation

In this chapter, the functional blocks of the analog loop, as described and modeled in the previous chapter, are further evaluated for design in hardware.

4.1 Driver Stage Design

4.1.1 Requirement Analysis

Beforehand of the concept evaluation and the circuit design, the requirements of the driver stage are to be defined. The main requirements, summarized in Table 3.4, embrace the following points:

- Control voltage of the power device: output voltage $V_{\text{out,drv,max}}$
- Driving capability: maximum output current $I_{\text{out,drv,max}}$
- Output slew rate SR_{drv} during the settling phase of the slope control
- Operating point of the driver output stage
- Quiescent current $I_{\text{q,drv}}$ during standby condition (IGBT is either in on-state or off-state)

The higher the gate-emitter voltage, the higher the possible collector current, and the lower the resulting collector-emitter saturation voltage and conduction losses in on-state. A common value for the positive control voltage is $+15$ V which is also shown in data sheets as a characteristic value. The absolute maximum value is typically chosen as $V_{\text{Ge,max}} = +20$ V [89].
The IGBT is turned off by applying a negative control voltage. The typical value in datasheets is -15 V and the gate-emitter voltage should not drop below -20 V.
However, in terms of costs, lower values in the range from 0 V to -15 V have established itself in many applications. One reason for lower absolute values of the negative control voltage is the lower required driver power, which is directly proportional to the difference between positive and negative control voltage. Taking voltage tolerances and sufficient safety margin into account, the negative control voltage is

frequently chosen to -5 V or -10 V. Furthermore, there are cost savings for the power supply generation if no negative supply voltage is needed. However, in case that the turn-off control voltage is 0 V, parasitic turn-on may occur (parasitic turn-on due to feedback effect of the Miller capacitance or parasitic turn-on due to the feedback effect of the emitter stray inductance). For low power applications, a trade-off between parasitic turn-on and cost-factor might be tolerable. However, this is not acceptable for high power applications, as parasitic turn-on increases the losses, which may lead to a critical temperature and a reduction of the IGBT's lifetime [28].

In this work, the output voltage of the driver is chosen to $V_{\text{out,drv,max}} = \pm 15$ V. This means that the transistors in the output stage of the driver require a blocking voltage capability of at least 40 V with regard to supply tolerances and safety margin.

The maximum output current of the driver $I_{\text{out,drv,max}}$ is mainly defined by the gate resistance and the difference of the IGBT control voltage. An estimation of the maximum peak current can be done by using the value for $R_{\text{G,min}}$ from Sect. 3.6,

$$\begin{aligned} I_{\text{out,drv,max}} &\approx 0.7 \cdot \frac{\Delta V_{\text{Ge}}}{R_{\text{G,min}}} = 0.7 \cdot \frac{V_{\text{Ge,max}} - V_{\text{Ge,min}}}{R_{\text{G,min}}} \\ &= 0.7 \cdot \frac{30\ \text{V}}{4.13\ \Omega} = 5.1\ \text{A}. \end{aligned} \tag{4.1}$$

The calculated value for $I_{\text{out,drv,max}}$ has not been reached in the test bench simulation with IGBT IKW50N60T, because the gate resistor has to be chosen larger than $R_{\text{G,min}}$ due to stability considerations. However, the closed-loop gate driver should also be applicable with other power devices, which exhibit a larger input capacitance, for instance IGBT modules. Thus, a high driving current is necessary for small switching delays. According to Eq. (3.23), a higher input capacitance leads to a smaller $R_{\text{G,min}}$, and therefore also to a smaller feasible value for R_{G} in the application, which then allows higher peak currents.

Hence, the maximum output current of the driver is set to $I_{\text{out,drv,max}} = 5$ A. The high-voltage transistors of the driver output stage require a large width over length ratio (W/L), in order to maintain large output currents of this level. The large dimensions of the output transistors lead to a large input capacitance of the driver stage. Thus, the slew rate at the output of the driver SR_{drv} is decreased, as the charging of the output transistor's input capacitance takes longer. In consequence, a trade-off between driving capability and SR_{drv} has to be reached. The SR_{drv} defines the settling time of the slope control. It has to be high enough to ensure that the slope control (or rather the amplifier output) is able to settle very fast when the first slope of the switching transition occurs. A feasible value is $SR_{\text{drv}} \approx 1\ \text{V}/\text{ns}$.

The maximum allowable quiescent current is targeted on approximately 1 mA to keep the power dissipation low during the inactive phase of the driver. In case a reduction of $I_{\text{q,drv}}$ is necessary, power down switches can be inserted, that are lowering the currents in the biasing circuits during the standby phase.

4.1.2 General Approaches and Concepts

The primary objective of an output stage is to efficiently drive signals into an output load, which in case of an gate-controlled power device is mainly capacitive. For driving of large capacitances, high sink and source currents are required. In general, there are two main approaches for realizing a Class-B/AB output stage, shown in Fig. 4.1. The configuration of the DC operating point is achieved by the voltage sources V_{shift}.

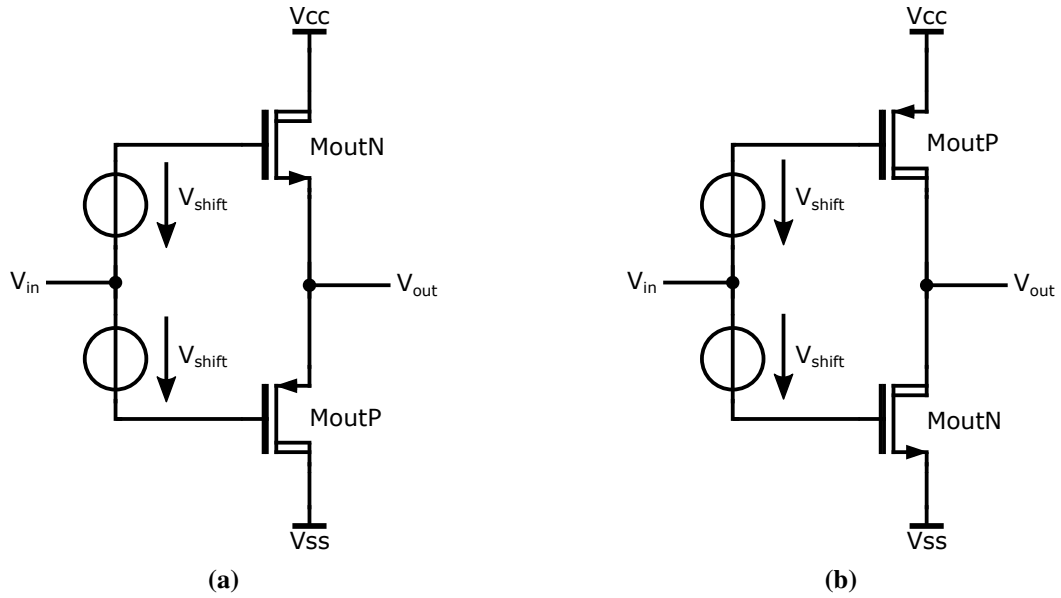


Fig. 4.1: Class-B/AB output stages implemented as (a) push-pull source follower and (b) push-pull common-source amplifier [97].

1. **Push-pull source follower:** One possible solution for an output stage is a pair of source followers (common-drain stages (CD)) connected source to source as shown in Fig. 4.1a. The combination of the two voltage followers enables very large sink and source currents, depending on the transistor size, and a small output impedance. As the output voltage is following the input, the voltage gain is small (≈ 1), but the current gain is large. Only a small input current is needed for charging the capacitance of the source follower gates. The source follower can therefore be used as a single-stage buffer without any complicated preamplifier.

   However, the main disadvantage of the push-pull source follower is that the output voltage is limited by the threshold voltage of $V_{\text{th,MoutN}}$ to

$$V_{\text{out,max}} = V_{\text{CC}} - V_{\text{GS,MoutN}} = V_{\text{CC}} - (V_{\text{th,MoutN}} + V_{\text{ovd,MoutN}}) \approx V_{\text{CC}} - V_{\text{th,MoutN}}. \tag{4.2}$$

   If the threshold $V_{\text{th,MoutN}}$ and the overdrive $V_{\text{ovd,MoutN}}$ were exactly constant, the output voltage would follow the input voltage with a constant difference. However, the overdrive voltage is not constant,

as it varies with the drain current. The same considerations apply for the minimum output voltage $V_{\text{out,min}}$ in dependency of threshold and overdrive of the output transistor MoutP.

2. **Push-pull common-source amplifier:** Another approach for the implementation of an output stage is the use of a push-pull amplifier (two common-source stages (CS)), as shown in Fig. 4.1b. As a result of the common-source configuration, the maximum and minimum output voltage is only limited by the overdrive voltages of the output transistors (voltage drop over $r_{\text{DS,on}}$). Thus, the output voltage swing is nearly rail-to-rail. In case of a capacitive load (switch gate), the output voltage is at its rail during on-state or off-state, as no more current is flowing into the gate and the voltage drop over $r_{\text{DS,on}}$ is zero. This kind of output stage is mainly implemented in two-stage amplifiers, as the output stage itself is inverting. Due to the voltage amplification of the CS stages, the stability of such an output stage has to be verified and is of much higher concern compared to push-pull source followers [97].

4.1.3 Concept Evaluation

The push-pull source follower and common-source amplifier from Fig. 4.1 are considered as possible output stages for the slope shaping gate driver, and are therefore evaluated in the following.
The size of the output transistors is the main factor of the driver that defines area and costs. They should be able to deliver a maximum sink or source current of 5 A, see Eq. (4.1). Based on this requirement, the size can be identified by simulation of a single transistor in the following way. The maximum possible V_{GS} is used in order to deliver the maximum current. V_{DS} is set to 7 V to model the Miller Plateau condition, as the maximum driver current is needed during this period. The output transistors of the common-source stage can be designed smaller than those of the source follower, as V_{GS} can be larger in case of the common-source stage. Due to the voltage following behavior, the maximum V_{GS} of the source follower is rather small (approximately 3.5 V). The maximum V_{GS} of the amplifier is limited by a zener diode protection at the gates to 8 V.
The DC gain of the source follower is slightly smaller than 1. Furthermore, the gain exhibits a high linearity. The maximum output voltage is limited to approximately $V_{\text{GS}} - V_{\text{th}}$. However, simulations show that the maximum output voltage is around 14 V when the IGBT is turned-on and no driving current is needed anymore. Therefore, the output voltage in the real application is acceptable to achieve a low ohmic resistance of the IGBT in conducting state.
In contrast to the source follower, the common-source amplifier output stage has nearly a rail-to-rail output voltage swing. In the closed-loop control during on-state of the IGBT, the driver output voltage reaches 15 V. There is no more current flowing, as there is no voltage drop across the output transistors. Furthermore, the results show that the DC gain of the amplifier is very high and it has less linearity compared to the

DC gain of the source follower. However, the most important aspect for the evaluation of the two approaches relates to their behavior in the closed-loop control. Therefore, simulations have been performed with both approaches (with an ideal voltage controlled current source with constant G_{fb} for the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback). The following reference currents and feedback gains lead to a stable closed-loop behavior and are used in the simulations:

Source follower:	$I_{\mathrm{ref,on}} = I_{\mathrm{ref,off}} = 10\ \mathrm{mA}$	$G_{\mathrm{fb}} = 20\ \mathrm{mA/V}$	$C_{\mathrm{fb}} = 10\ \mathrm{pF}$
Amplifier:	$I_{\mathrm{ref,on}} = I_{\mathrm{ref,off}} = 100\ \mu\mathrm{A}$	$G_{\mathrm{fb}} = 200\ \mu\mathrm{A/V}$	$C_{\mathrm{fb}} = 100\ \mathrm{fF}$

Due to the large forward gain of the common-source stage, the feedback gains and the reference currents are much smaller, than in case of the source follower.

Compared to the source follower, the additional forward gain of the common-source amplifier can be seen as an advantage, but also as a challenge. Advantageous is the fact, that the additional DC gain is another degree of freedom for the closed-loop control, and that the values of the feedback gains and reference currents can be smaller. This is beneficial for the design of the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback, as it is easier to achieve a constant value of G_{fb} for a smaller transconductance, see Sect. 4.3.3. However, the value for the capacitance C_{fb} of the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ feedback has to be at least 1 pF, as there are no smaller discrete high-voltage capacitors available on the market. This results in higher feedback gain for the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$-loop, which in turn leads to an unstable control behavior when the amplifier is used as actuating element. The stability issue can be solved by reducing the gain of the amplifier and will be considered in Sect. 4.1.4. The main advantage of the source follower in comparison to the common-source amplifier is that stability is not a major concern due to the unity gain, as has been pointed out in Sect 3.3.2. However, the control behavior is only tunable via the feedback gains. Thus, there is less flexibility in the system. Furthermore, feasible values for G_{fb} are rather limited to 5 $\mathrm{mA/V}$.

In principle, both approaches show a good transient and dynamic behavior in the closed-loop control and can be implemented as driver output stage. In conclusion, the common-source output stage is more cost-efficient, the maximum output voltage is larger (lower conduction losses in on-state) and the additional forward gain allows more flexibility in tuning of the control behavior. On the other hand, it is challenging to maintain stability when using the amplifier, which is more relaxed in case of the source follower.

Table 4.1 provides a summary on the advantages and disadvantages of both driver output stage concepts. In the hardware evaluation module in chapter 5, a source follower is used to guarantee for stable operation using different gate-controlled devices. Hence, the push-pull amplifier is more an option for an Integrated Circuit (IC) gate driver solution.

Tab. 4.1: Comparison of source follower and common-source driver stage.

	Source follower	Common-source amplifier
Advantages	Stability is relaxed ($A \approx 1$)	Rail-to-rail output $V_{\text{out,drv}}$
	High-impedance input, low-impedance output	Additional tuning parameter for the control loop dynamics (voltage gain A)
		Area-efficient
		Potential for relaxed requirements on I_{ref} current source
Disadvantages	Larger area (limited V_{GS})	Stability is critical
	Feedback networks need to drive a large power stage	
	Only feedback gains as tuning parameters	

4.1.4 Concept of a common-source driver stage

A concept for the common-source amplifier, which is rather suitable if the gate driver is realized on an IC, is shown in Fig. 4.2. It consists of a two-stage topology. The input stage is formed by a current amplifier, known as second-generation current conveyor (CCII) [98]. The output stage is a voltage amplifier with additional resistors for setting the operating point. While the CCII consists of low-voltage transistors, optimized for high bandwidth and linear current gain, the output stage is implemented with high-voltage DMOS transistors, in order to provide an output voltage compliance and driving capability according to the requirements in Table 3.4.

If $V_{\text{in}} > V_{\text{cm}}$, the voltage $V_{\text{GS,M1}}$ decreases and $V_{\text{SG,M3}}$ increases. Consequently, the current from node X1 is flowing into M3 and is amplified by the factor N in the low-side current mirror on the bottom. The amplified current discharges the gate capacitance of the output transistor MoutP and pulls down the gate voltage of MoutP. Thus, MoutP becomes active and sources current into the output.

If $V_{\text{in}} < V_{\text{cm}}$, the input current from X1 is flowing into M1 and the high-side current mirror. Thus, the gate of MoutP is pulled up to V_{CC2}, which turns off MoutP.

The same principle applies for the second CCII which is in parallel to the first one. For $V_{\text{in}} > V_{\text{cm}}$, the node $Z2$ and therefore also the gate of MoutN is pulled down, which turns off MoutN. In case of $V_{\text{in}} < V_{\text{cm}}$, the node Z2 is pulled up to V_{CC2} and MoutN is turned on.

The large signal current gain of the CCII is defined by the ratio 1:N of the low-side and high-side current mirrors. Thus, the factor N impacts the slew rate of the amplifier output, as the provided current charges

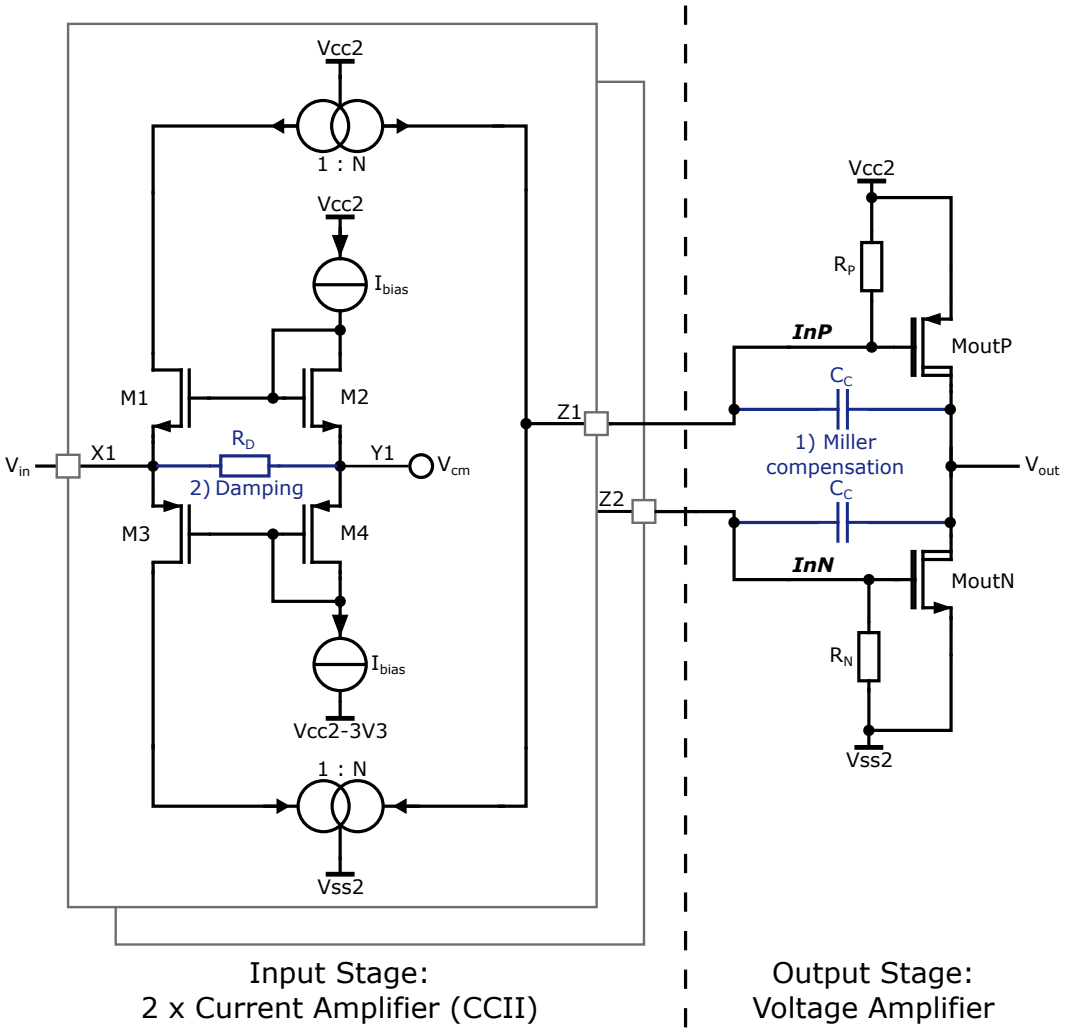


Fig. 4.2: Concept of the amplifier: input stage consisting of two current amplifiers (CCII) [98], and output stage consisting of a common-source voltage amplifier with resistors for setting the operating point. The devices in blue indicate to methods for stabilizing the control behavior of the analog loop: 1) Miller compensation, 2) DC gain reduction

and discharges the high input capacitance of the output transistors. This is the main factor that defines the dynamic transient behavior. Furthermore, N adds to the DC gain factor in the closed-loop control.

If the amplifier of Fig. 4.2 is utilized as part of the analog loop of Fig. 3.2, it may lead to instabilities for specific parameter sets. The amplifier increases the loop gain in the system compared to the small-signal analysis in Sect. 3.3.2. This enhances the gain-bandwidth product and may lead to a reduction of the system phase margin. Hence, mechanisms to optimize the amplifier for stable operation need to be evaluated, such as frequency compensation and DC gain optimization.

For this purpose, the small-signal model from Sect. 3.3.2 is modified in one detail: A single-pole roll-off is

assumed for the amplifier, and its transfer function is modeled by its DC gain A_{DC} and cutoff frequency f_{c},

$$G_{\mathrm{Drv}}(s) = \frac{A_{\mathrm{DC}}}{1 + \frac{s}{2\pi f_{\mathrm{c}}}}. \tag{4.3}$$

The values for A_{DC} and f_{c} have been identified in an AC analysis of the amplifier with an *RLC* load ($R = 10\,\Omega$, $L = 13$ nH and $C = 3.14$ nF), in order to represent the input impedance of the IGBT model. The frequency response for a current mirror ration $N = 30$ is shown in Fig. 4.3. The values are $A_{\mathrm{DC}} = 26.58$ dB and $f_{\mathrm{c}} = 901.8$ kHz.

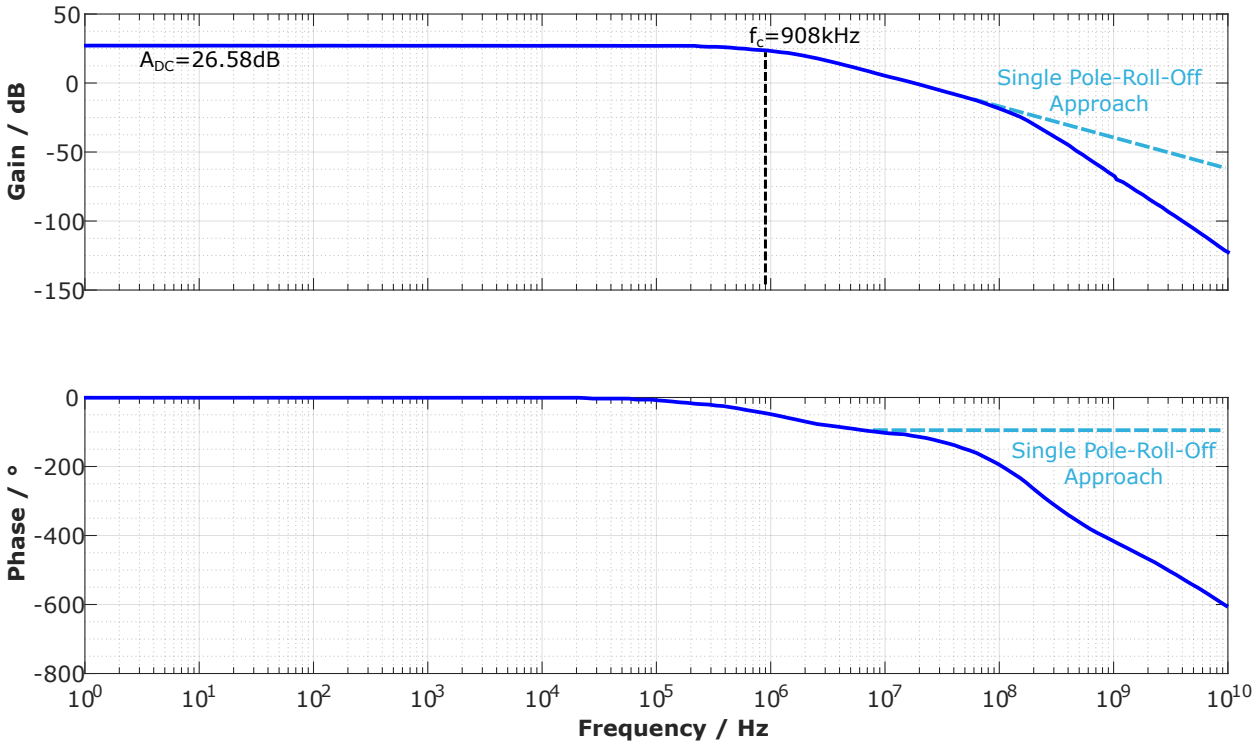


Fig. 4.3: Frequency response (AC sweep from 1 Hz to 10 GHz) of the amplifier with *RLC* load ($R = 10\,\Omega$, $L = 13$ nH and $C = 3.14$ nF).

As a next step, the stability for the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ loop and the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ loop is investigated separately in the small-signal model. The DC gain has to be reduced to 10 dB to achieve a stable control behavior (see Fig. 4.4 for the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ loop and Fig. 4.5 for the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ loop). Lowering the DC gain increases the stability, but also decreases the loop gain at low frequencies, which reduces the dynamic behavior of the amplifier. This leads to longer turn-on and turn-off switching delays of the device under control.

In order to achieve a high loop gain at low frequencies, the control behavior can also be improved by frequency compensation of the amplifier. This means, that the dominant pole f_{c} is shifted to lower frequencies. Reducing the corner frequency to values smaller than 100 kHz leads to a higher phase margin of the closed-loop control and a stable operation (see Fig. 4.6 for the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ loop and Fig. 4.7 for the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ loop).

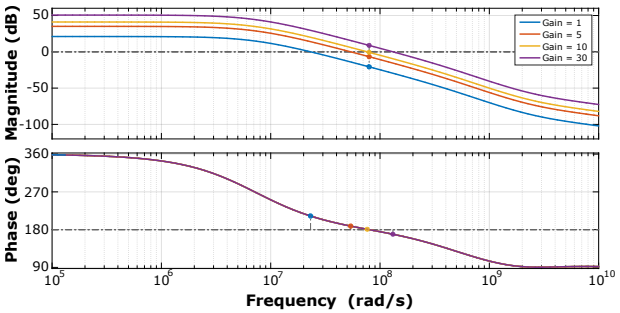


Fig. 4.4: Frequency response of $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ loop at varied DC gain of the amplifier : DC gain = 1...30 dB, $f_{\mathrm{c}} = 900$ kHz.

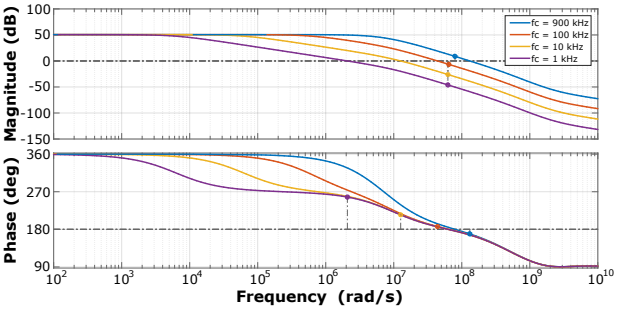


Fig. 4.6: Frequency response of $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ loop at varied corner frequency of the amplifier: DC gain = 30 dB, $f_{\mathrm{c}} = 1...900$ kHz.

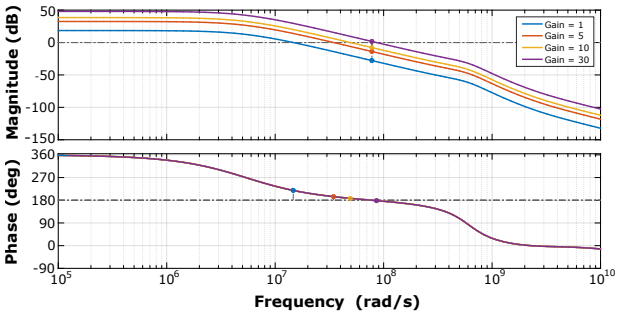


Fig. 4.5: Frequency response of $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ loop at varied DC gain of the amplifier: DC gain = 1...30 dB, $f_{\mathrm{c}} = 900$ kHz.

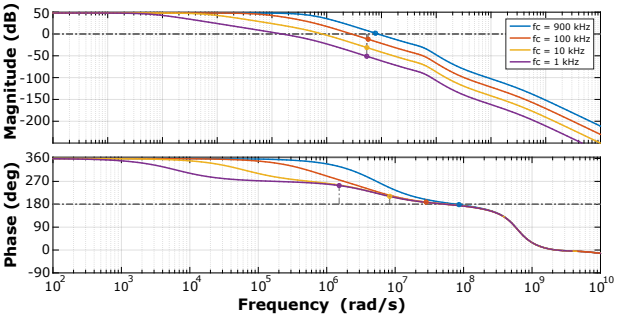


Fig. 4.7: Frequency response of $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ loop at varied corner frequency of the amplifier: DC gain = 30 dB, $f_{\mathrm{c}} = 1...900$ kHz.

The two stabilization measures, which comprise either reducing the DC gain or frequency compensation, are investigated separately for the amplifier design.

Frequency compensation is achieved by shifting of the existing poles. The dominant frequency f_{c} of the amplifier is determined by the highest node impedance, which is the input node of the output stage. This pole can be shifted to lower values by inserting a Miller capacitance C_{C} from the nodes Z1 and Z2 to the output, as indicated in Fig. 4.2. Thanks to the Miller effect, C_{C} can be realized with a comparably small value [99].

The Miller compensation is evaluated in a closed-loop simulation, and the results are shown in Fig. 4.8. Adding C_{C} makes the control more stable, as there are no more oscillations in the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ slope during turn-on for $C_{\mathrm{C}} = 30$ pF. However, the insertion of the Miller capacitance C_{C} strongly reduces the slew rate of the amplifier output. For turn-on, this means that $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ is not controlled, as the output is still in its settling phase. When $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ starts, the output has settled and the slope is well-controlled. For turn-off the behavior is even worse, as the output is far below the control voltage level prior to the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ transition. For $C_{\mathrm{C}} \geq 20$ pF, both switching slopes are not controlled anymore, as the amplifier output is not able to settle to the control voltage level. Thus, Miller compensation is not suitable to ensure stability of the slope shaping concept. Hence, decreasing the amplifier's contribution to the loop gain is a more suitable approach

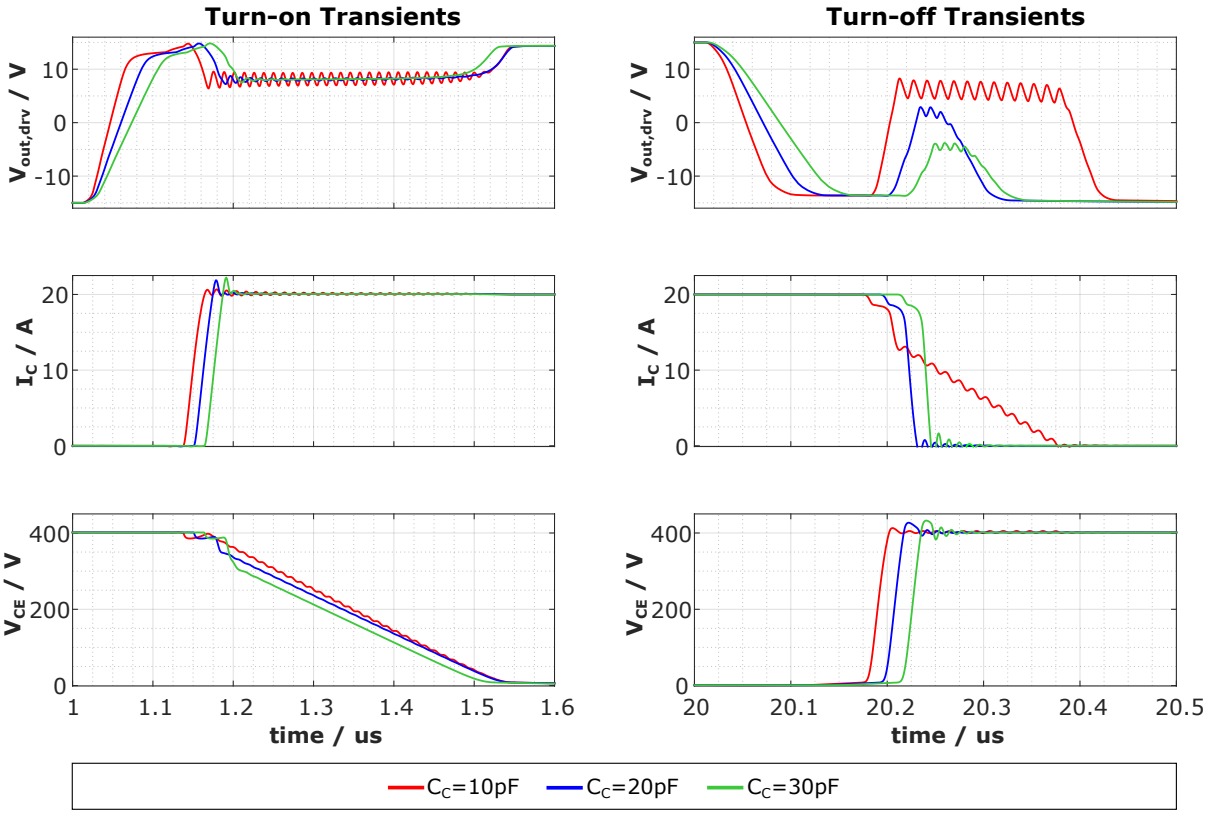


Fig. 4.8: Simulation results closed-loop control with amplifier incorporating Miller compensation ($C_C = 10$ pF, 20 pF and 30 pF).

to guarantee for stable operation.

The reduction of the DC gain of the amplifier can be realized in several ways. It can either be done by insertion of additional resistors, or by decreasing the ratio 1:N of the low-side and high-side current mirrors. These first investigations have shown that reducing the mirror ratio is not beneficial, as this worsens the dynamics and the slew rate of the amplifier output so strong, that the switching transients are not controllable anymore (amplifier output is not able to settle fast enough). An additional damping resistor can be either inserted in series at the input of the amplifier or in parallel to the input transistors, connected to the common-mode voltage V_{cm}. The series resistor has a high impact on the dynamic behavior. Hence, the parallel damping resistor R_{D} as illustrated in Fig. 4.2 is investigated for stabilizing the amplifier in the closed-loop. Without R_{D}, the input resistance of the amplifier is dominated by the transconductances of the four input transistors,

$$R_{\mathrm{in}} = \frac{1}{4 \cdot g_{\mathrm{m}}}. \tag{4.4}$$

The parallel damping resistor R_{D} is low-ohmic ($< 1/(4 \cdot g_{\mathrm{m}})$). Thus, the total input resistance is reduced to a value smaller than R_{D}. In turn, the voltage boost at the input for the same input currents as without R_{D} gets smaller, which reduces the gain of the input stage. The stabilizing effect of R_{D} in the closed-loop control can

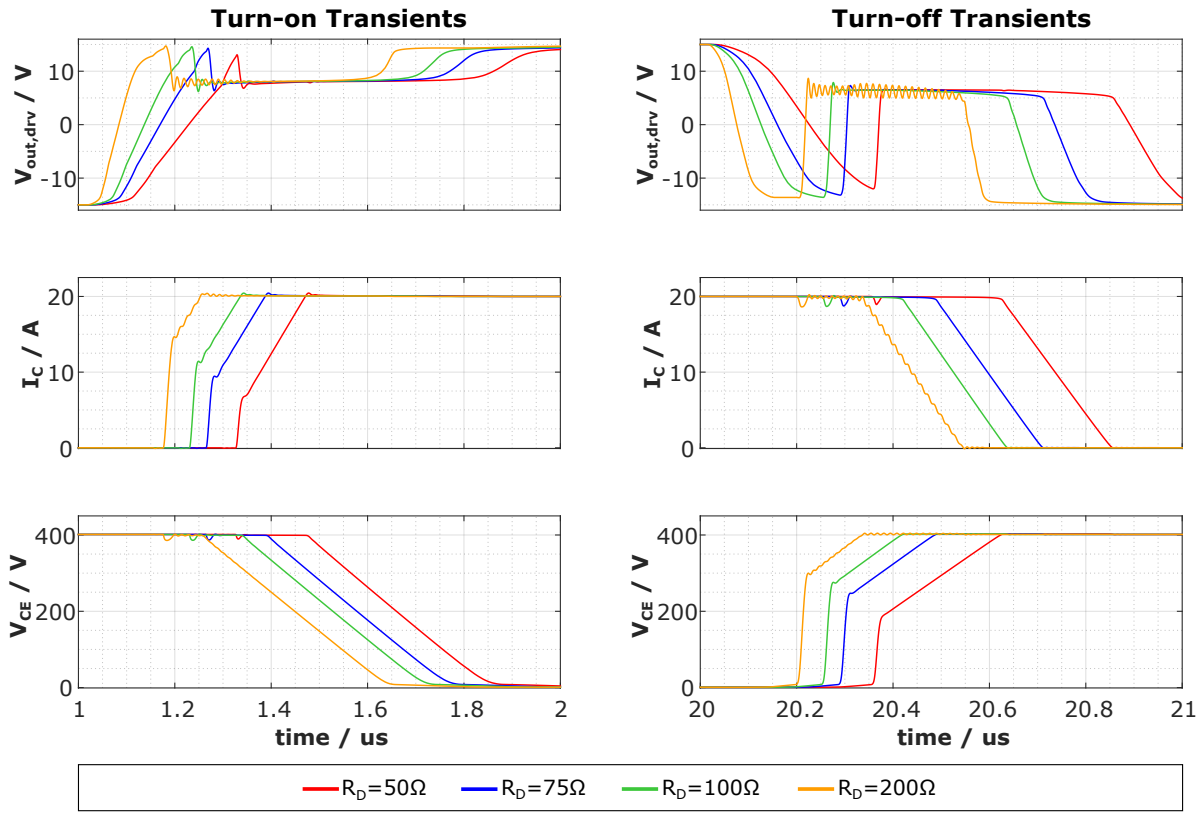


Fig. 4.9: Simulation results closed-loop control with amplifier incorporating a parallel damping resistor R_D in the input stage ($R_\mathrm{D} = 50\ \Omega$, $75\ \Omega$, $100\ \Omega$ and $200\ \Omega$).

be seen in Fig. 4.9. For low-ohmic values of R_D ($\leq 100\ \Omega$), the controlled slopes get more stable. However, the switching delay of the IGBT is increased due to the reduced DC gain of the amplifier. A value of R_D between $75\ \Omega$ and $50\ \Omega$ allows for a good trade-off between high stability and acceptable switching delay. A simulative stability analysis is described in Sect. 4.5 for the the analog control loop, comprising the CS amplifier stage (with real $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback circuit and a control loop model including parasitics).

4.2 Anti-Windup Method to Prevent Non-Linearities

The simulation results in Fig. 4.9 show that the particular switching slope, which occurs first in every transition ($\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ in case of turn-on; $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ in case of turn-off), exhibits a non-linearity at the beginning, in which the slope is not controlled. The non-linear behavior occurs, because the output of the driver stage reaches its limitation (either $+15$ V or -15 V) during the pre-charge intervals, due to the absence of active feedback. When the first transient starts to rise, there is active feedback current into the summing node, and the output voltage of the amplifier has to settle to the control voltage level (≈ 8 V). As the settling of the output is not unlimited fast, overshoots occur during $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ at turn-on and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ at turn-off. During

the settling time, the gate current remains uncontrolled at a too high level, which leads to a steeper slope in the settling interval of the amplifier output (see Eq. (2.6), Eq. (2.10)). As the difference between output voltage and control voltage level is much higher during turn-off settling than during turn-on settling, the non-linearity in $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ during turn-off is more critical compared to $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ during turn-on. The described problem is referred to the limited control range of the actuator (Fig. 4.10a) and has been introduced as the windup effect during the large signal analysis in Sect. 3.3.3.

Reducing the windup effect of the integrating element can be realized by introducing an anti-windup method as shown in Fig. 4.10b. The difference between the signals before and after the saturation ($e_{\mathrm{windup}} = u - u^*$) is fed back to the integrator to limit the integration during windup condition. As long as the actuating element is not in saturation, the error signal $e_{\mathrm{windup}} = 0$ and the additional anti-windup feedback does not influence the normal control operation. The time constant τ_{r} defines how fast a windup of the integrator is counteracted [100]. A proposal for an anti-windup method, for use in an analog slope control, can be

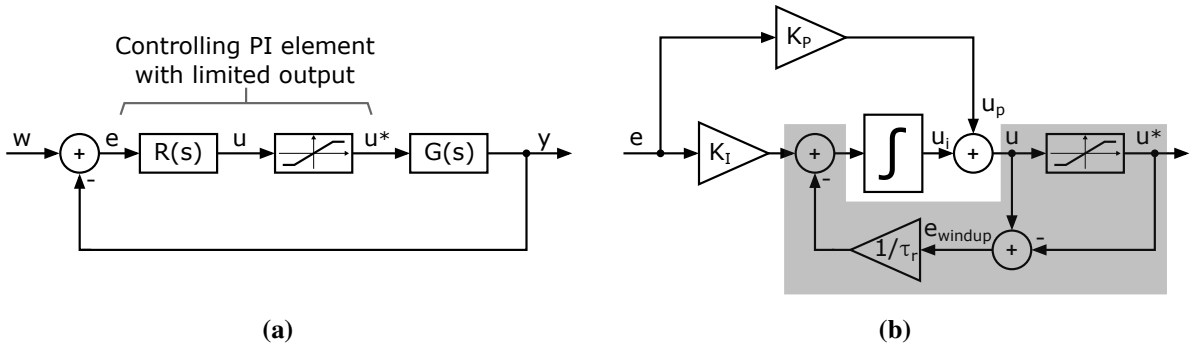


Fig. 4.10: (a) Standard control loop, with PI element and limited output. (b) PI element with anti-windup (in gray) [100].

found in literature [67] and is shown in Fig. 4.11. The windup effect is reduced by active control of the gate current during the turn-on and turn-off switching delay intervals. The gate current control is only activated during these delay intervals via the control signal $V_{\mathrm{ctrl},I_{\mathrm{G}}}$. In consequence, the gate current control has to be deactivated at the current rise during turn-on and the voltage rise at turn-off, respectively. This point in time is detected when the active current or voltage slope feedback exceeds a predefined threshold.

In general, the anti-windup method as depicted in Fig. 4.11 is also applicable for the closed-loop concept in this work. However, the additional fully rail-to-rail operational amplifier, required for measuring the gate current, increases the complexity of the design. In addition, the turn-on and turn-off switching delays are depending on the employed power semiconductor switch. Due to the gate current control, the switching delays vary with the input capacitance of the used power device (see Eq. (2.4), Eq. (2.11) and Eq. (2.12)). Therefore an anti-windup solution, which exhibits less complexity and independency of the controlled device, is pursued. Concerning the dual-loop control concept in this work, the problem can be solved in two ways. Either the amplifier is chosen fast enough to keep the settling interval very small. The second option

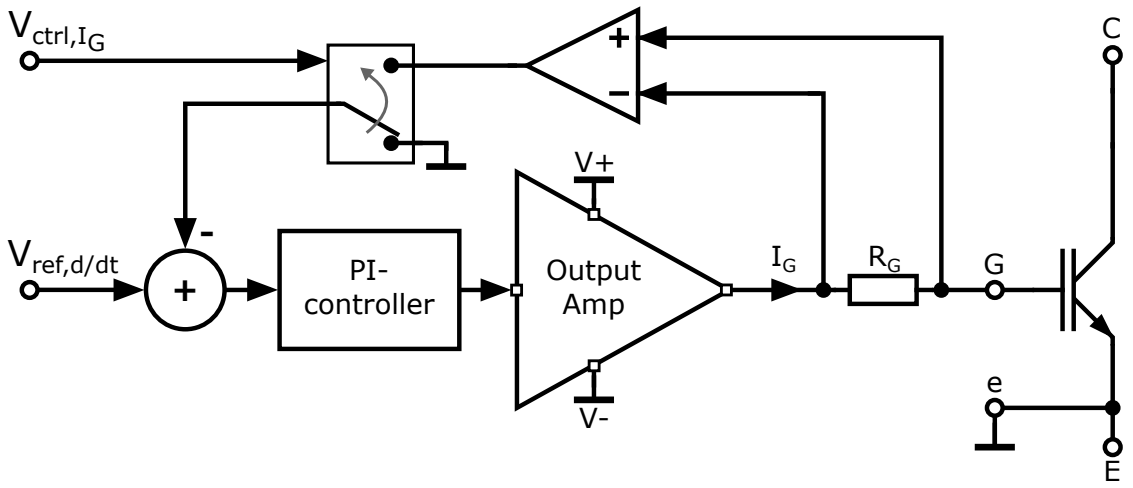


Fig. 4.11: Anti-windup method for an analog slope control: gate current control to define the gate current during the turn-on and turn-off switching delay intervals [67].

is the insertion of additional circuitry to improve the behavior.

Accelerating the output settling is only achievable by decreasing the size of the output transistors, which leads to lower input capacitance, but also to lower current driving capability. A second way is increasing the gain of the second-generation current conveyor (CCII). However, this would demand for a higher damping resistor, which increases the switching delay and also reduces the settling behavior of the output.

A proposal for an innovative, flexible and easy implementable anti-windup method is shown in Fig. 4.12. The fundamental approach is to prevent the amplifier from reaching its limitation by controlling the slew rate of its output voltage ($\mathrm{d}V_{\mathrm{out,drv}}/\mathrm{d}t$) during the turn-on and turn-off switching delays. In turn, the voltage difference which has to be overcome during the settling interval is smaller, and therefore the settling time is reduced. As shown in Fig. 4.12, a displacement current $I_{\mathrm{fb,SR}}$ is generated through the capacitance $C_{\mathrm{fb,SR}}$ as soon as the amplifier output voltage rises,

$$I_{\mathrm{fb,SR}} = C_{\mathrm{fb,SR}} \cdot \frac{\mathrm{d}V_{\mathrm{out,drv}}}{\mathrm{d}t}. \tag{4.5}$$

Using a current mirror, $I_{\mathrm{fb,SR}}$ is amplified by a factor N and it is provided to the input of the amplifier as negative feedback, in order to establish closed-loop control of $V_{\mathrm{out,drv}}$. Consequently, the feedback gain of the control loop is determined by the size of the capacitor $C_{\mathrm{fb,SR}}$ and the ratio 1:N of the current mirror. If the output voltage is falling, the feedback currents $I_{\mathrm{fb,SR}}$ and $I_{\mathrm{fb,SRN}}$ change their direction, and the falling slew rate is controlled.

At turn-on the slew rate $\mathrm{d}V_{\mathrm{out,drv}}/\mathrm{d}t$ can be limited in such a way, that the output voltage overshoot only arises slightly above the Miller Plateau. Thus, the voltage difference during the settling interval is very small and, as a consequence, there is no remaining non-linearity in the transient. Limiting the slew rate in the same way for turn-off, such that the output only goes slightly below the Miller Plateau level, is possible

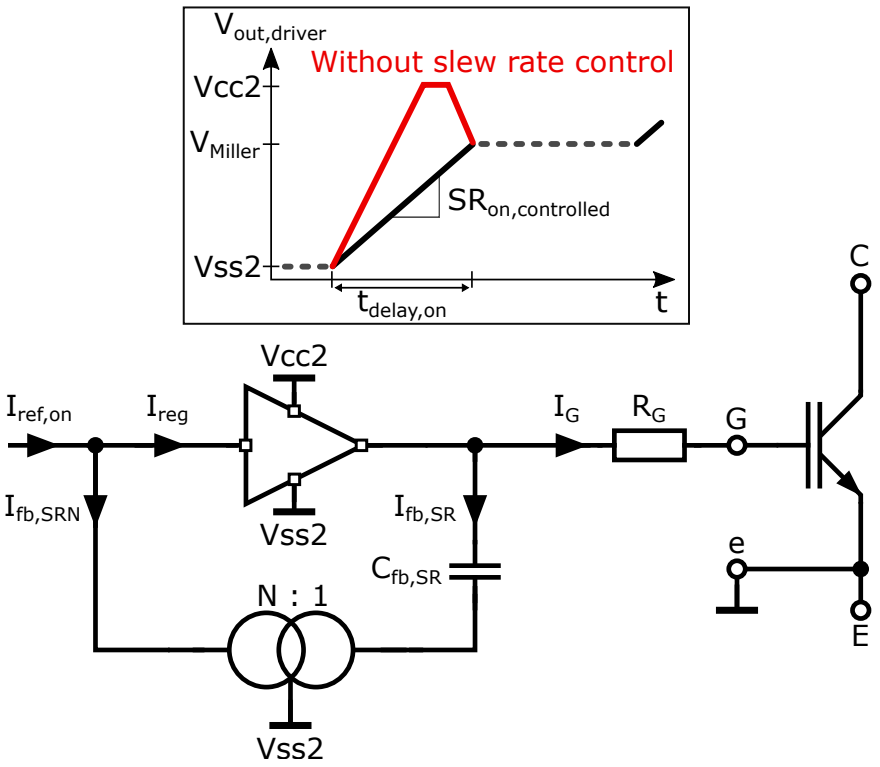


Fig. 4.12: New proposal of an anti-windup method for an analog slope control: slew rate control of the driver's output during the turn-on and turn-off switching delay intervals to prevent the driver from going into its limitation (all currents are shown for the turn-on switching delay, in case of turn-off all currents change in directions).

but typically not favorable, as this leads to a very large turn-off switching delay due to the larger voltage difference compared to turn-on. As mentioned in Sect. 2.2.3, the Miller capacitance at the beginning of turn-off is large due to the low value of V_{CE}. Therefore, a large gate current is required to keep the delay small. Hence, it is preferred that the $V_{out,drv}$ drops down to a value some volts below the Miller Plateau level to pull enough current through the gate resistor.

The circuit implementation of the new anti-windup method is shown in Fig. 4.13. It consists of two feedback loops for controlling the slew rate, one feedback path for the positive slew rate and another path for the negative slew rate. This allows to tune the feedback gains for positive and negative slew rates separately. Only one feedback path is active to enable a fast settling of the amplifier output when the collector current rises during turn-on, or when the collector-emitter voltage starts to rise during turn-off. The active feedback loop can be optionally controlled via the signal $EN_{SR-Ctrl}$ by the transistors MN3 and MP3. During turn-on, the negative $dV_{out,drv}/dt$ feedback path is switched off, and the positive $dV_{out,drv}/dt$ feedback path is switched off during turn-off.

The effect of the slew rate control on the switching slopes and the amplifier output is further investigated in a system simulation. The results are shown in Fig. 4.14.

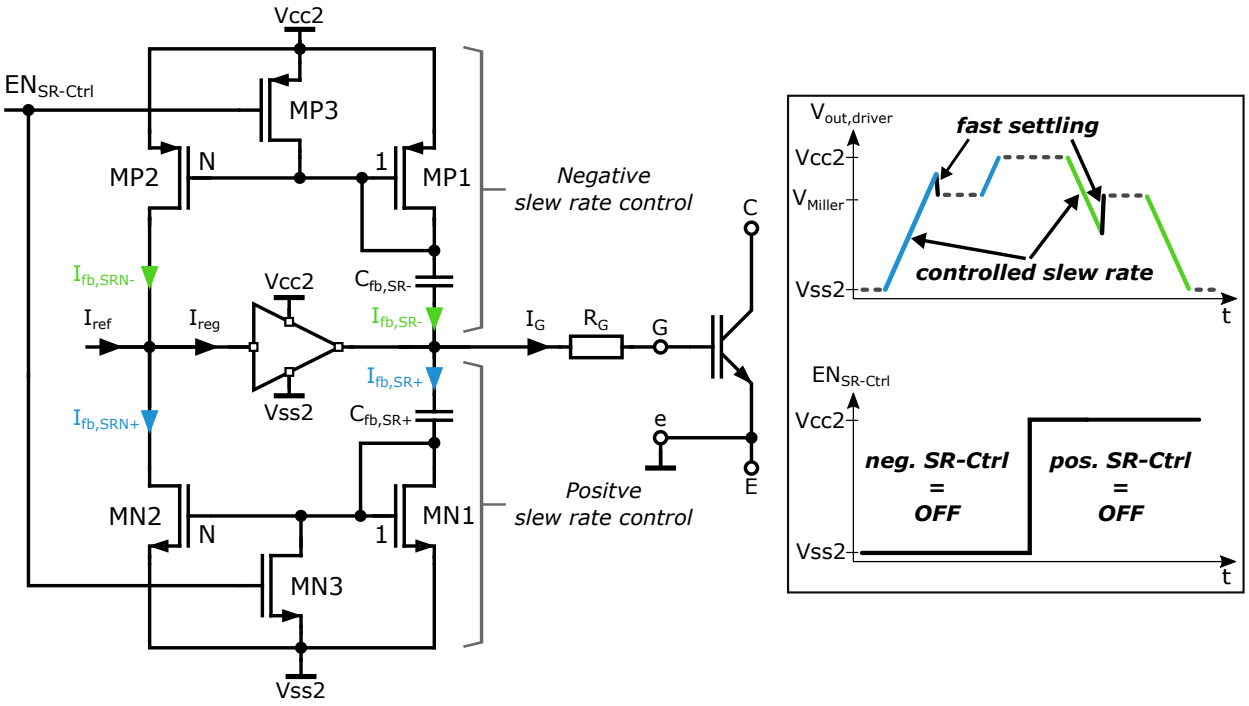


Fig. 4.13: Circuit implementation of the slew rate control. Via the signal $\mathrm{EN_{SR-Ctrl}}$ the negative slew rate control is deactivated during turn-on and the positive slew rate control is deactivated during turn-off to allow a fast settling behavior of the amplifier when the switching slopes start.

Three different configurations are compared:

(1) The reference, which is the closed-loop gate driver without anti-windup, shown in Fig. 4.14a) (red curve).

(2) Permanent slew rate control, where both feedback loops are active all the time (without the switches MN3 and MP3), shown in Fig. 4.14b) (blue curve). No extra control signal $\mathrm{EN_{SR-Ctrl}}$ is required.

(3) Adaptive slew rate control for turn-on and turn-off as previously described in Fig. 4.13, shown in Fig. 4.14c) (green curve). An extra control signal $\mathrm{EN_{SR-Ctrl}}$ is required to deactivate the not required feedback branch, but it leads to an improved regulation bandwidth.

In (1), the missing anti-windup causes non-linearities in parts of $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ at turn-on and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ at turn-off. The slew rate control in (2) and (3) leads to a reduced windup-effect during turn-on. $V_\mathrm{out,drv}$ has almost no overshooting behavior and therefore, the controlled I_C slope is very linear. Due to the limited overshoot, the voltage difference, that has to be settled by the driver output, is very small. Hence, the results for (2) and (3) are identical for turn-on. However, the difference of these two configurations appears in the turn-off switching waveforms. For a small switching delay, the output voltage has to go far below the Miller

Plateau voltage, and the amplifier output has to overcome the voltage difference during the settling when V_{CE} starts to rise. Configuration (3) shows an improved performance as the output is able to settle fast into positive direction (positive slew rate control is disabled). Consequently, the non-linearity in the V_{CE} slope is comparably small.

The main drawback of the $dV_{out,drv}/dt$ control is the larger switching delay. However, the switching delay can be reduced by applying a two-step approach for I_{ref} at turn-on and turn-off, whereas at first a high I_{ref} is applied to reduce the switching delay as a preboost. Thereafter, the control values for I_{ref} are selected, similar as in open-loop gate drivers discussed in Sect. 2.3.2.

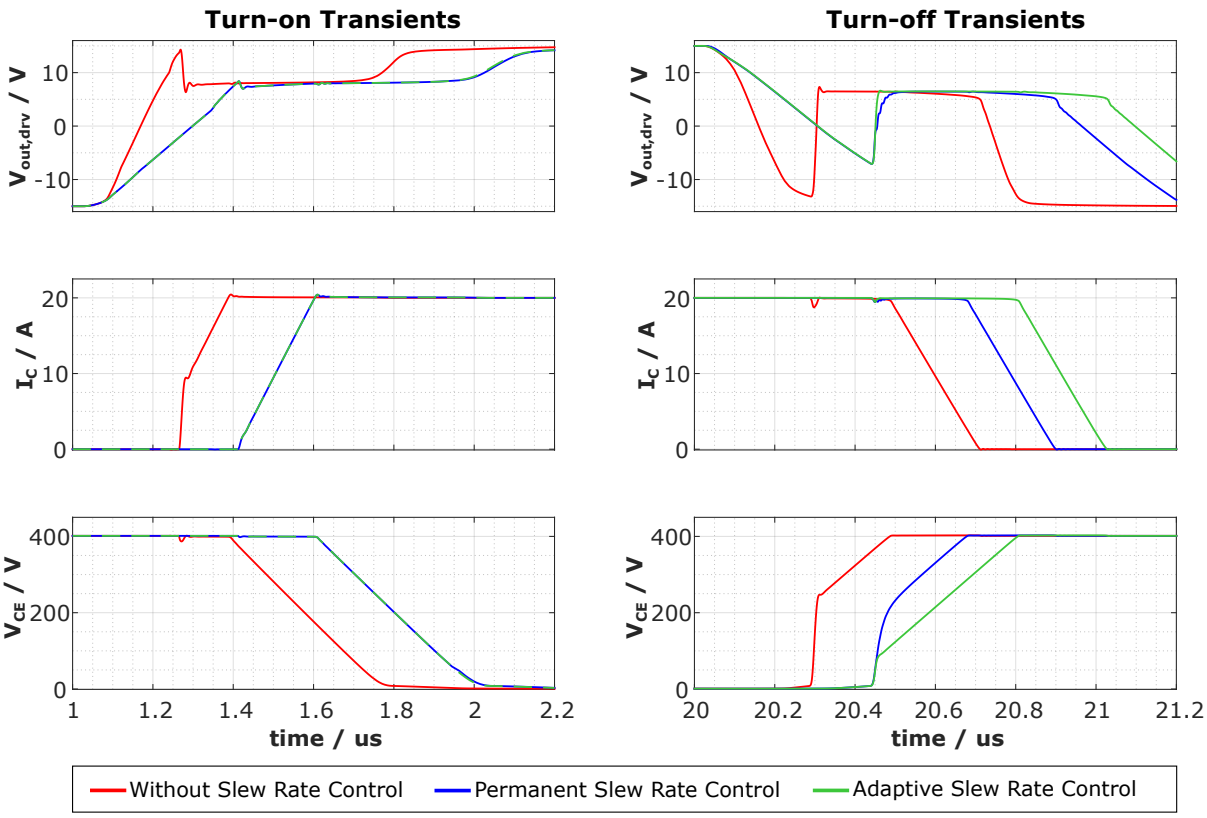


Fig. 4.14: Simulation results closed-loop control with different configurations:
a) Reference: simulation without any slew rate control, shown in red
b) Simulation with permanent slew rate control, where both feedback loops are active all the time (without the switches MN3 and MP3), shown in blue
c) Simulation with adaptive slew rate control for turn-on and turn-off (disable neg. SR control/-pos. SR control during turn-on/turn-off), shown in green.

4.3 Design of the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ Feedback

4.3.1 Requirement Analysis

The $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback senses the voltage drop across the emitter lead inductance according to [25] and converts it into a current. As the analog loop is designed in the current domain, the generated current can be used as a feedback signal. Therefore, the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback block acts as a bipolar voltage controlled current source (VCCS). The main requirements, as introduced in Table 3.4, comprise the following parameters:

- Feedback gain G_fb
- Quiescent current $I_\mathrm{q,didt}$ and operating point
- Maximum signal input voltage $V_\mathrm{in,max} = V_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t,\mathrm{max}}$

The feedback gain G_fb is defined as ratio between the feedback current and the input voltage $V_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t}$ of the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback circuit, which is the induced voltage in the parasitic emitter lead inductance during collector current slopes,

$$G_\mathrm{fb} = \frac{I_{\mathrm{fb},\mathrm{d}V_\mathrm{CE}/\mathrm{d}t}}{V_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t}}. \tag{4.6}$$

G_fb should be designed around 2 mA/V for a reference current $I_\mathrm{ref,on} = I_\mathrm{ref,off} = 1$ mA, in order to achieve a $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ of approximately 0.1 A/ns. As the requirement for the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ range is from 0.1 A/ns to 1 A/ns, the feedback gain G_fb could be decreased in order to increase $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$. However, the value for G_fb should not be too small, as this reduces the feedback current and therefore the amplifier's output slew rate. A good value has been identified to $G_\mathrm{fb} = 1$ mA/V. This value should be constant for arbitrary input voltages, to achieve a linear feedback. The value of G_fb should be constant during the whole current transient, to achieve a constant rate of $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$.

To achieve a constant value of G_fb, the biasing of the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback circuit plays an important role. Class-A biasing allows in general for a more linear gain, as the signal distortion is smaller. However, when the operating point is selected, the quiescent current $I_\mathrm{q,didt}$ has to be considered as well. To keep the efficiency of the analog slope control high and to reduce the power dissipation, the maximum allowable $I_\mathrm{q,didt} = 1$ mA. According to Sect. 3.6, the maximum $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ to be controlled is 1 A/ns. This value determines the maximum input voltage $V_\mathrm{in,max} = V_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t,\mathrm{max}}$ which the feedback circuit should be able to handle and where the feedback current should not be saturated. $V_\mathrm{in,max}$ can be calculated with the size of the parasitic inductance L_E between Kelvin and power emitter. For discrete IGBTs in TO-247-4 packages, it has been demonstrated by s-parameter measurements as part of this work in Sect. 3.4, that L_E is around 5 nH. In case of IGBT

modules, the size of L_E is approximately 10 nH [101]. According to Eq. (3.2), $V_{in,max}$ can be calculated as

$$V_{in,max} = V_{fb,dI_C/dt,max} = 10\,\text{nH} \cdot 1\,\text{A/ns} = 10\,\text{V}.$$

4.3.2 Concept Evaluation

The dI_C/dt feedback circuit represents a voltage controlled current source. It can be implemented as a kind of differential amplifier as shown in Fig. 4.15. The differential pair is formed by the transistors Moff and Mon. The source degeneration resistors $R_{s,Moff}$ and $R_{s,Mon}$ linearize the transconductance of the differential pair. The Kelvin emitter (e) is considered as fixed potential, as it is set to the gate driver ground GND2.

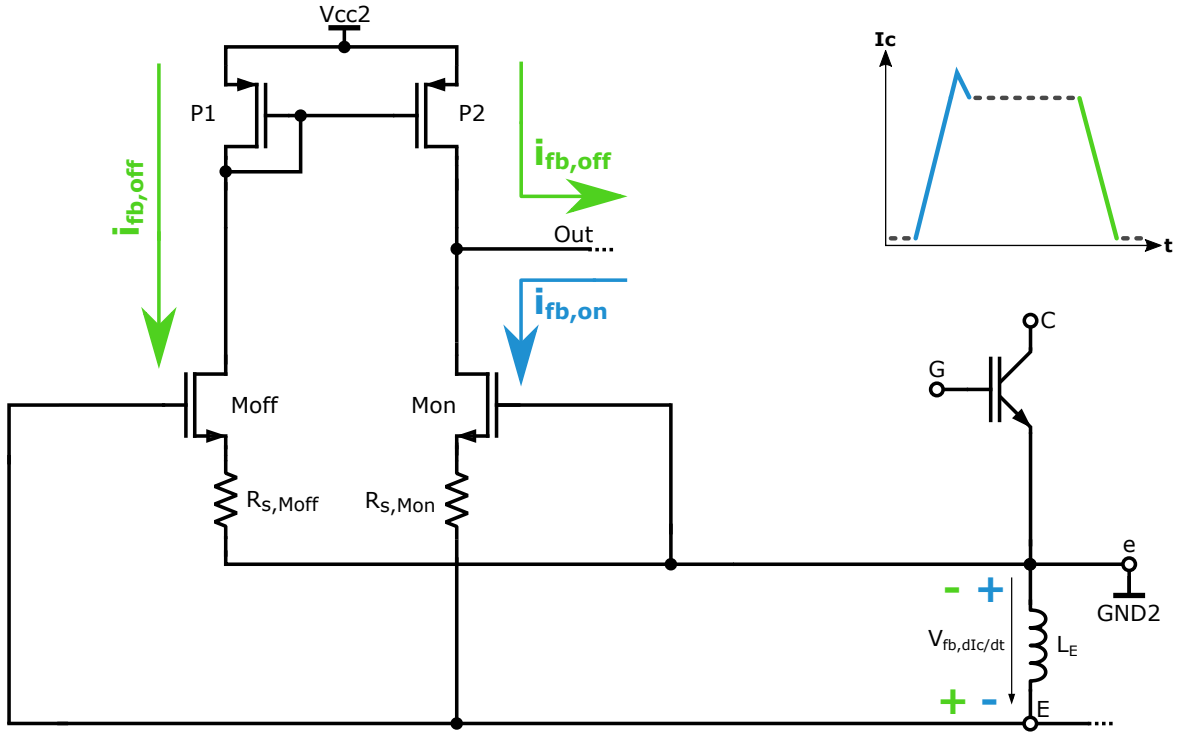


Fig. 4.15: First proposal for dI_C/dt feedback circuit: differential amplifier with source degeneration at the differential pair.

Hence, the power emitter (E) has a moving potential during turn-on and turn-off, depending on the sign of the induced voltage $V_{fb,dI_C/dt}$ over the stray inductance L_E between Kelvin and power emitter.

At turn-on, the collector current is rising and, therefore, a positive $V_{fb,dI_C/dt}$ is induced in L_E. Accordingly, the gate of Moff and the source of Mon are pulled down. As the source of Moff and the gate of Mon are fixed at GND2, Moff is turned-off and Mon is turned-on. Thus, $i_{fb,off} = 0$ and the feedback current $i_{fb,on}$ is drawn from the output.

During turn-off, the collector current is falling. Therefore, the induced voltage over L_E changes its sign. Consequently, Mon is now turned-off, whereas Moff is turned-on and the feedback current $i_{fb,off}$ is pushed

into the output via the matched current mirror consisting of P1 and P2.
The low static current consumption, which is in the range of a few micro amperes as there are only leakage currents that contribute to it, is an advantage of the proposal in Fig. 4.15. However, one major disadvantage of the concept is the limited minimum input voltage. The induced voltage $V_{\mathrm{fb,d}I_\mathrm{C}/\mathrm{d}t}$ in L_E needs to be at least as high as the threshold voltage V_th of the differential pair to generate an active feedback. This drawback can be compensated by adding a level-shifting voltage to the gates of the differential pair as shown in Fig. 4.16. The trade-off in this concept is a higher static current consumption due to the additional biasing and higher quiescent currents through the differential pair.
The level-shifting voltages V_bias1 and V_bias2 are generated by a current source and the voltage drop over a resistor. In general, three different operating points can be set by the voltages $V_\mathrm{bias1,2}$:

$$\begin{aligned} \text{Class-B operation:} \quad & V_\mathrm{bias1,2} < V_\mathrm{th,Moff,Mon} \\ \text{Class-AB operation:} \quad & V_\mathrm{bias1,2} \approx V_\mathrm{th,Moff,Mon} \\ \text{Class-A operation:} \quad & V_\mathrm{bias1,2} \gg V_\mathrm{th,Moff,Mon} \end{aligned}$$

When setting the operating point, it has to be guaranteed that the requirement on the maximum static quiescent current $I_\mathrm{q,didt}$ is fulfilled.
The capacitance C_1 provides additional charge in case of a voltage step. As the gate of Mon is referred to a fixed potential, the capacitance C_2 is inserted to stabilize the gate voltage during the collector current transients and to make the on-side of the feedback circuit symmetrical to the off-side.
The concept with the level shifting of the differential pair's gate voltage offers the advantage of a smaller minimum ascertainable $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$.

4.3.3 Design and Simulation Results

The source degeneration of the differential pair is designed in such a way, that the corresponding transconductance is mainly defined by the degeneration resistors $R_\mathrm{s,Mon}$ and $R_\mathrm{s,Moff}$. This enables a constant and current independent feedback gain G_fb and hence, linear feedback currents.
A series resistor at the source of a single-transistor amplifier acts as local series feedback (see Fig. 4.16). The loop gain is then $g_\mathrm{m}R_\mathrm{s}$ and the resulting transconductance g_mR is reduced to

$$g_\mathrm{mR} = \frac{g_\mathrm{m}}{1+g_\mathrm{m}R_\mathrm{s}} \approx \frac{1}{R_\mathrm{s}} \quad \text{(for large } R_\mathrm{s}\text{)}. \tag{4.7}$$

Thus, for large resistor values, it becomes independent of the drain current in contrast to g_m for a single-transistor stage [102].
Confirmed by simulation, the series resistors $R_\mathrm{s,Mon}$ and $R_\mathrm{s,Moff}$ in the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback design should be at

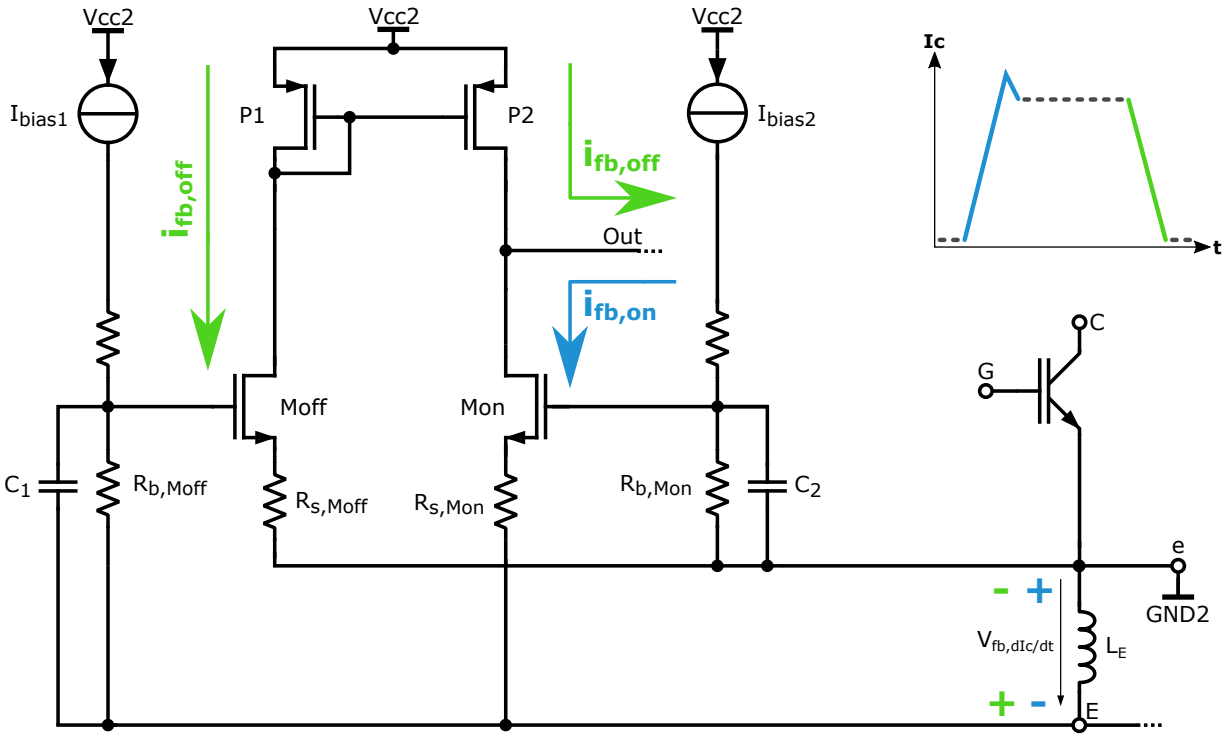
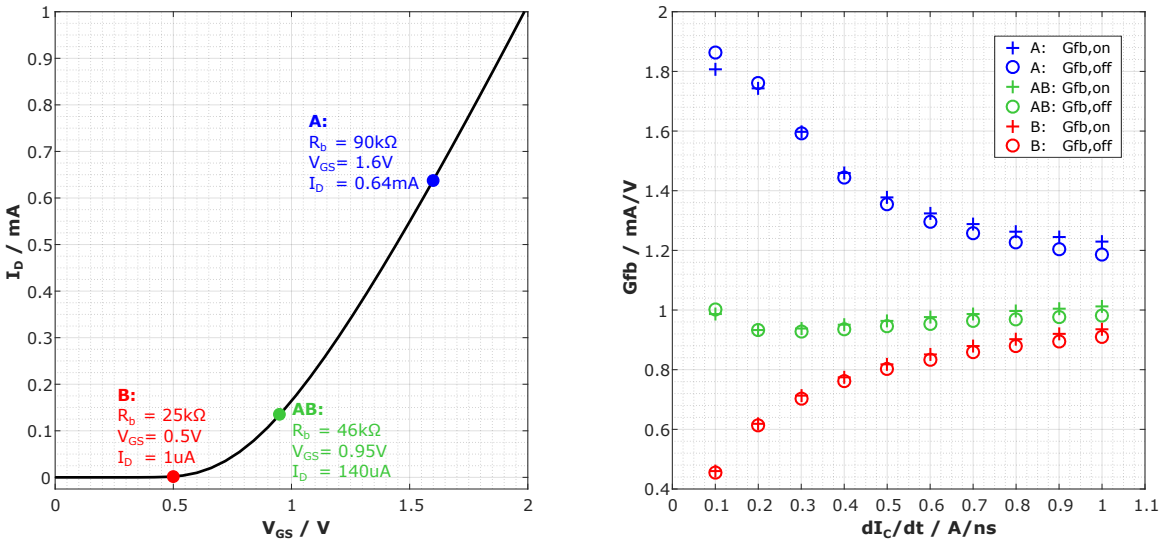


Fig. 4.16: Advanced proposal for $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback circuit: differential amplifier with additional DC level-shifting at the gates of the differential pair.

least 500 Ω to achieve a constant feedback gain G_fb.

Another design parameter for the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback is the operating point of the differential pair, which can be either class-B, AB or A, with consideration of the maximum allowable static current consumption. Class-A operation seems not to be feasible, as the resulting quiescent current $I_\mathrm{q,didt}$ would exceed 1 mA, offending the requirement on the quiescent current (Table 3.4). However, when using the slope control concept with an outer digital loop as shown in Fig. 3.1, the bias current sources setting the operating point of the differential pair can be operated in a pulsed manner and only be active during the switching slopes. The timing information required in this case need to be provided by the digital circuitry. The desired operating points (A, AB, B) with the corresponding values for $R_\mathrm{b,Mon} = R_\mathrm{b,Moff} = R_\mathrm{b}$ are illustrated in the transfer characteristic of a single transistor from the differential pair (see Fig. 4.17a). The three different operating points are further investigated in a transient simulation, where different $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ (from 0.1 A/ns to 1 A/ns) are applied to a 5 nH inductor to generate an input signal for the feedback circuit. The resulting mean value of the feedback gain G_fb for turn-on and turn-off is shown in Fig. 4.17b. In class-B operation, the feedback currents for small $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ (or small V_GS) are not high enough, which results in a small value for G_fb. Class-AB operation shows the best performance over the whole range of $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$. The static current due to the operating point is a constant offset for the feedback current, which can compensate the reduced gain at low V_GS. Furthermore, the non-linear part of the transfer characteristic around $V_\mathrm{GS} = V_\mathrm{th}$ is compensated.



(a) **(b)**

Fig. 4.17: (a) Operating points A, AB, B in the transfer characteristic of Mon, Moff. (b) Mean values of the feedback gain $G_{\mathrm{fb,on}}$, $G_{\mathrm{fb,off}}$ for the three operating points A, AB, B for sweep of ideal $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ (from 0.1 A/ns to 1 A/ns) applied on a 5 nH inductor.

4.4 System Simulation Setup and Influence of Parasitics

The toplevel of the final analog circuit design is shown in Fig. 4.18. The setup for the system simulation of the analog loop is as follows:

- An analog loop model with parasitic elements is used, according to Fig. 3.2, with parasitic inductance in the gate path $L_{\mathrm{G}} = 10$ nH, stray inductance in the power circuit $L_{\mathrm{S}} = 100$ nH. The high-side FWD is replaced by an IGBT in off-state. Similar values for L_{S} and L_{G} can be found in datasheets [89] and literature [32] for testing the switching behavior of power semiconductor devices.
- The common-source amplifier, as designed in Sect. 4.1.4, is used as driver stage with damping resistor $R_{\mathrm{D}} = 55\ \Omega$. The resistors R_{P} and R_{N} are set to 12 kΩ, as these values result in a linear output gain. The mirror ratio 1:N of the high-side and low-side current mirrors is set to 1:30.
- The amplifier is extended by the new anti-windup method (additional closed-loop slew rate control on $\mathrm{d}V_{\mathrm{out,drv}}/\mathrm{d}t$, as shown in Fig. 4.13). As the windup effect is stronger during turn-off than during turn-on, assymetric feedback gain is chosen, which is higher for the negative slew rate control. Both control loops are optimized for small switching delays.
- The differential stage, according to Fig. 4.16, is chosen as $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback with $G_{\mathrm{fb}} = 1$ mA/V
- An ideal capacitor, set to $C_{\mathrm{fb}} = 1$ pF, is used as $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ feedback.

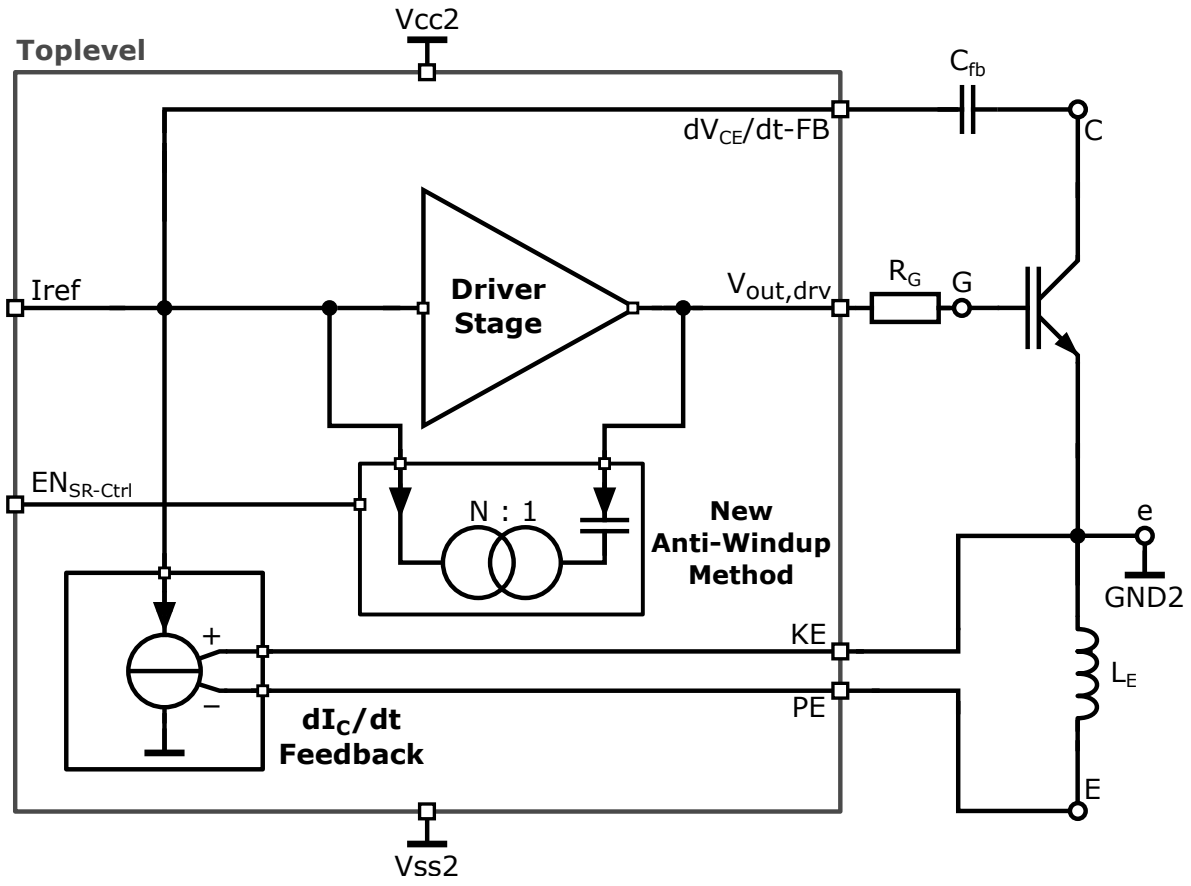


Fig. 4.18: Toplevel of the analog circuit design.

- The reference current value, used for turn-on and turn-off, is chosen to $I_{\mathrm{ref,on}} = I_{\mathrm{ref,off}} = 1$ mA.
- The external gate resistor is $R_{\mathrm{G}} = 7\ \Omega$ to fulfill the stability criteria.
- Two load current levels are analyzed, $I_{\mathrm{Load}} = 20$ A and 50 A.
- The DC link voltage is selected as 2/3 of the IGBT voltage rating,$V_{\mathrm{DC}} = 400$ V
- A SPICE model for the IGBT IKW50N60T (600 V, 50 A, trench-/fieldstop technology) from Infineon is used for the device under test (DUT).

The described setup leads to the following slew rates: $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t \approx 0.2$ A/ns and $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t \approx 1$ V/ns. The influence of the parasitic elements on the control behavior is described below.
The use of the turned-off IGBT as freewheeling diode yields a more realistic representation, as e.g. inverters in motor drive applications are typically configured as a bridge leg, where the IGBTs in one leg are controlled complementarily. In the simulations of the previous chapters, a silicon carbide (SiC) diode has been used as FWD, which exhibits almost no reverse recovery effect [103]. If the SiC diode is replaced by a turned-off IGBT, the anti-parallel diode of the IGBT acts as freewheeling diode. This results in a large

reverse recovery current ($\hat{I}_{\mathrm{rr}} = 14$ A) at the end of the I_{C} transient during turn-on (see Fig. 4.19). As the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ control is still active after the reverse recovery current reached its peak, there is a crosstalk between the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ control and $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ control, at the beginning of the voltage transient. This leads to a very steep voltage slope in the interval where the current decays from its peak value.

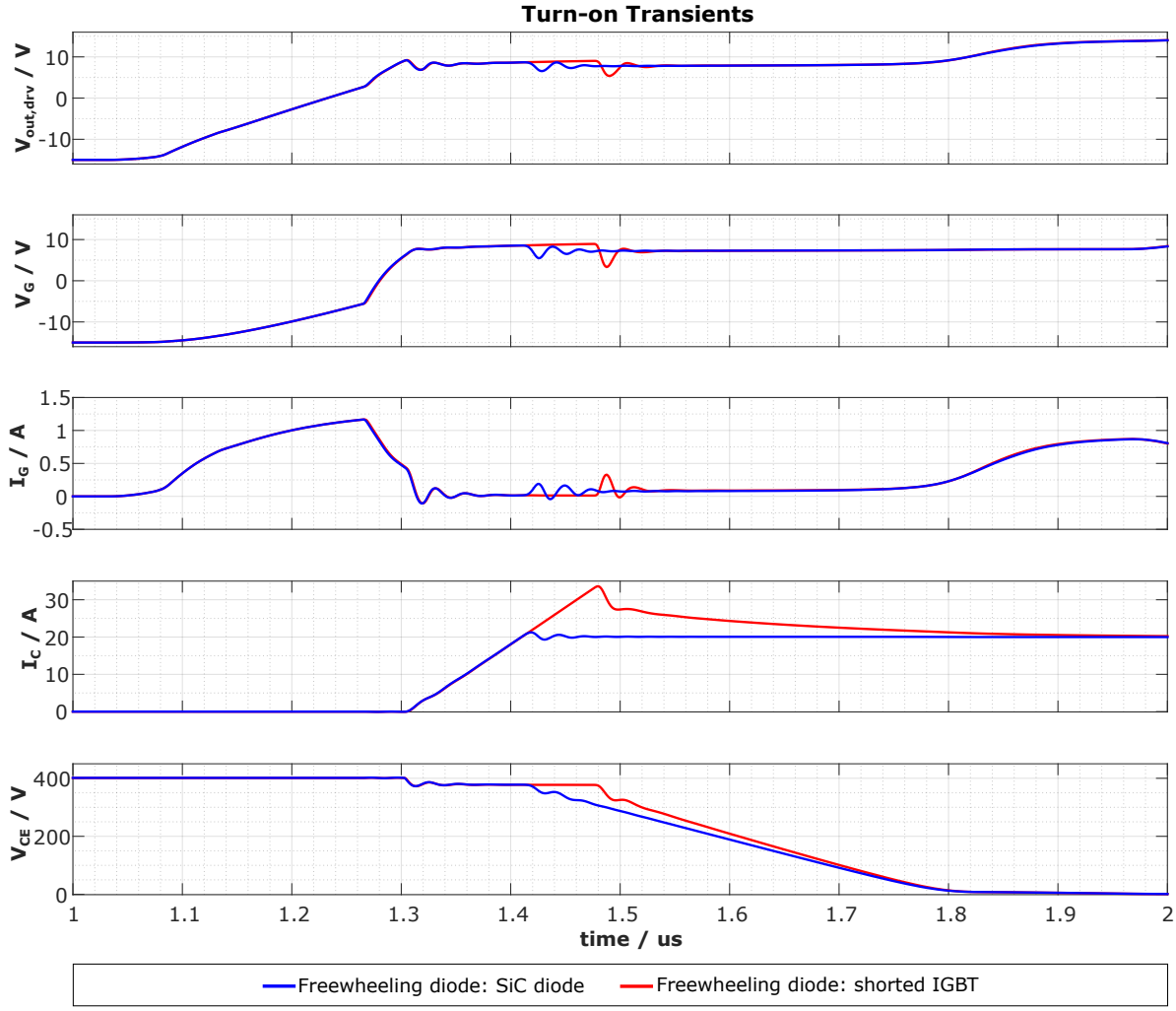


Fig. 4.19: Comparison of turn-on control behavior for ideal freewheeling diode (SiC diode) and freewheeling diode with reverse recovery effect (turned-off IGBT).

The stray inductance L_{S} of the power stage, which comprises the parasitic inductance of the power switch, the DC link and the busbars, is another parasitic element that impacts on the switching transients. When the collector current changes, a voltage is induced across L_{S}, which reduces the voltage drop across the IGBT during turn-on, see Eq. (2.7), and therefore leads to a voltage overshoot during turn-off, see Eq. (2.13). After turn-off, the stray inductance leads to ringing in V_{CE} and I_{C} (see Fig. 4.20).

The parasitic gate inductance has mainly an impact on the stability of the closed-loop control, but the influence can be compensated with a gate resistor that meets the condition in Eq. (3.23).

The influence of parasitic elements in the feedback paths is rather small. Hence, they are negligible in an appropriate analysis of the control behavior.

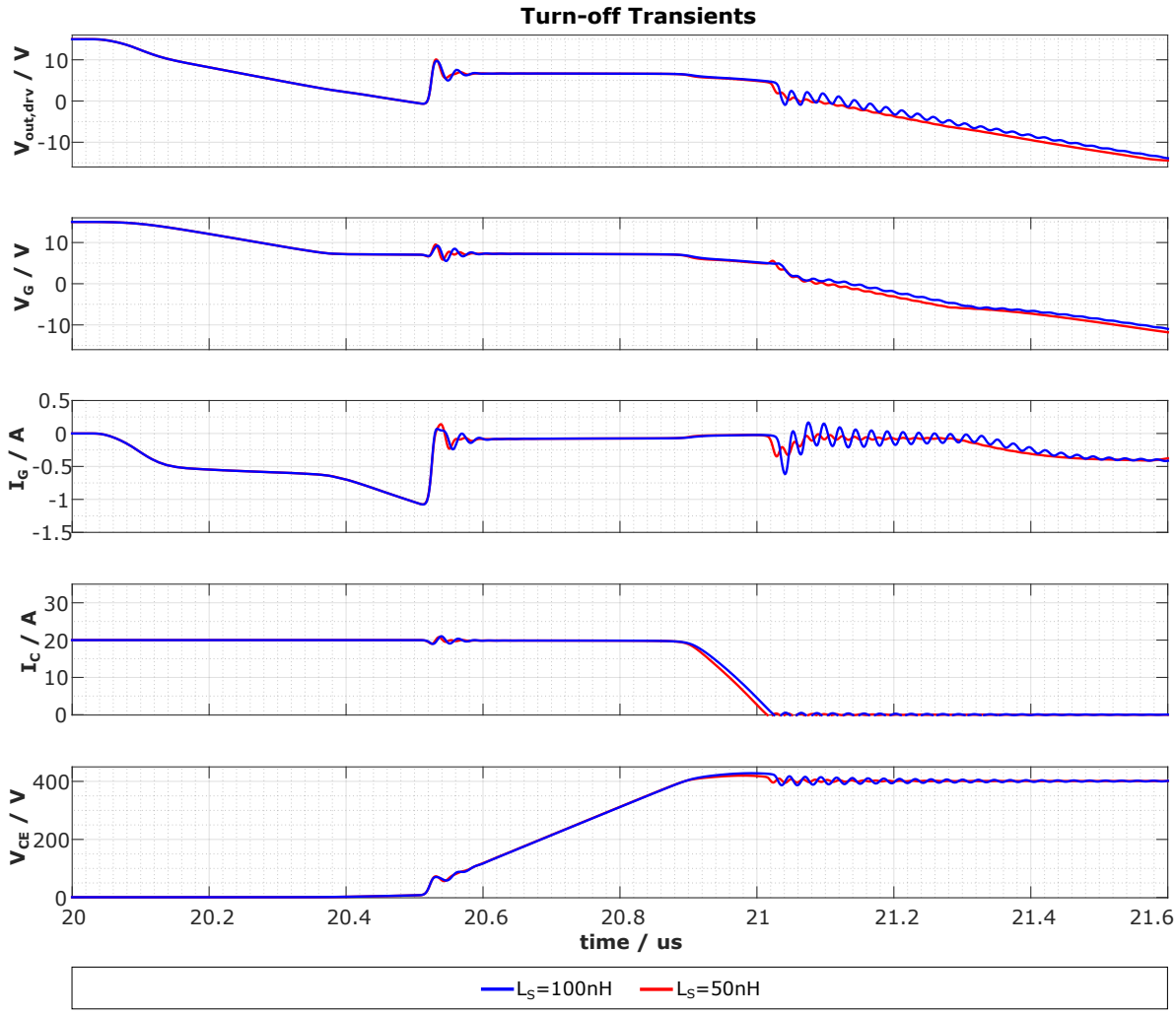


Fig. 4.20: Comparison of turn-off transients and driver output voltage for $L_S = 100$ nH and $L_S = 50$ nH.

4.5 Transient Stability Analysis

4.5.1 Test Bench for the Stability Analysis

The stability of the three control loops (dI_C/dt, dV_{CE}/dt and $dV_{out,drv}/dt$) is investigated separately. A loop cutter is inserted into the feedback of the particular control loop under investigation. Thereby, a transient simulation is performed, and the stability analysis is executed in the DC operating point where the transient simulation has stopped.

The stability analysis is performed manually with a conventional AC sweep and the help of a replica circuit,

in order to use the correct impedances in the nodes of the loop. The principle is shown in Fig. 4.21 exemplary for the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ control loop. Test benches for the other loops are implemented in a similar manner. The impedance of the feedback path is taken in AC from the replica circuit into the original circuit, where the loop is cut. The same is implemented for the impedance of the drive path. Hence, the used impedances for the AC sweep, and therefore the results of the stability analysis, are very accurate.

4.5.2 Analysis of the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ Control Loop

The analytical stability, described in Sect. 3.3, is verified with the method in Fig 4.21. The phase margin is determined for different transient operating points of the closed-loop control.

Figure 4.22 shows the results for the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ control loop for turn-on and turn-off. The feedback current $I_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t}$ is directly proportional to $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$, according to Eq. (3.1) and Eq. (3.2). Therefore, it serves as a good indicator, to check the settling behavior of the control and to identify the critical operating points concerning stability. During turn-on, there are two critical points for the stability of the control loop. One of them is in the beginning when the control loop settles, which causes overshoots in $I_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t}$. The critical operating point is at the point in time when the feedback current has reached its peak and starts to sink (at $t = 1.32\ \mu\mathrm{s}$). The minimum phase margin in this operating point is around 25°. During the settling phase, the phase margin rises until it reaches approximately 60° at the end of the current slope. When the reverse recovery current reached its peak and decays (at $t = 1.50\ \mu\mathrm{s}$), the phase margin goes down to 25° again, until 5 ns later it is back at 60°. Hence, the system is stable in all the operating points of the transition.

During turn-off, the feedback current has no overshooting behavior and consequently, the phase margin is constant at approximately 60°. When the collector current drops below zero (at $t = 21.03\ \mu\mathrm{s}$), a ringing occurs due to the stray inductance L_S. Hence, the feedback current exhibits a ringing behavior, as well. This forces the phase margin down to 20° for a short time period (≈ 10 ns).

The waveforms and the phase margin for the $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ control loop are illustrated in Fig. 4.23. The critical operating points of the $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ control loop are at similar operating conditions of the control as for the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$. During turn-on, the critical operating point occurs when the control settles at $t = 1.49\ \mu\mathrm{s}$. The phase margin at this operating point is approximately 25°. Thereafter, the phase margin rises and, when the control has settled, it is constant at around 60° during the whole remaining voltage transient.

The turn-off exhibits the most critical operating point, as the driver output has to settle a high voltage difference when V_CE starts to rise. This causes high overshoots and a temporarily unstable behavior at $t = 20.52\ \mu\mathrm{s}$. At this point, the feedback current has reached its first peak and starts to sink. The phase margin drops slightly below zero degree. However, a short period later (at $t = 20.53\ \mu\mathrm{s}$), the phase margin reaches 60°, where it stays with some variations until the control is fully settled. At the end of the slope the phase margin is at 60°. When the ringing occurs at $t = 21.03\ \mu\mathrm{s}$, the phase margin exhibits a drop to 20° for

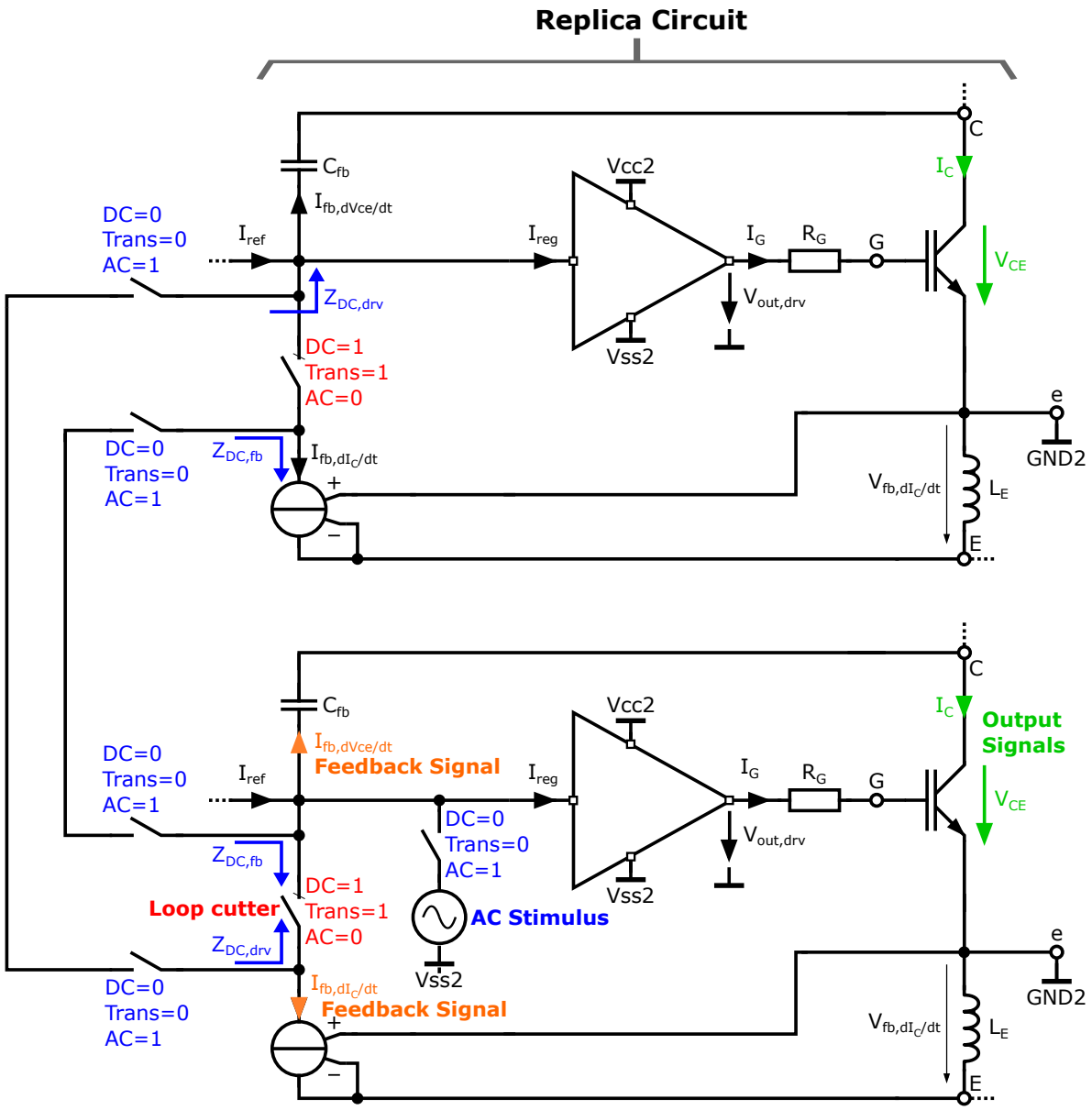


Fig. 4.21: Stability analysis with replica circuit: DC switches are indicated in red and are used to cut the feedback loop, AC switches are indicated in blue. The impedance of the drive path and the feedback path are taken in AC to the point where the feedback loop is cut in the original circuit.

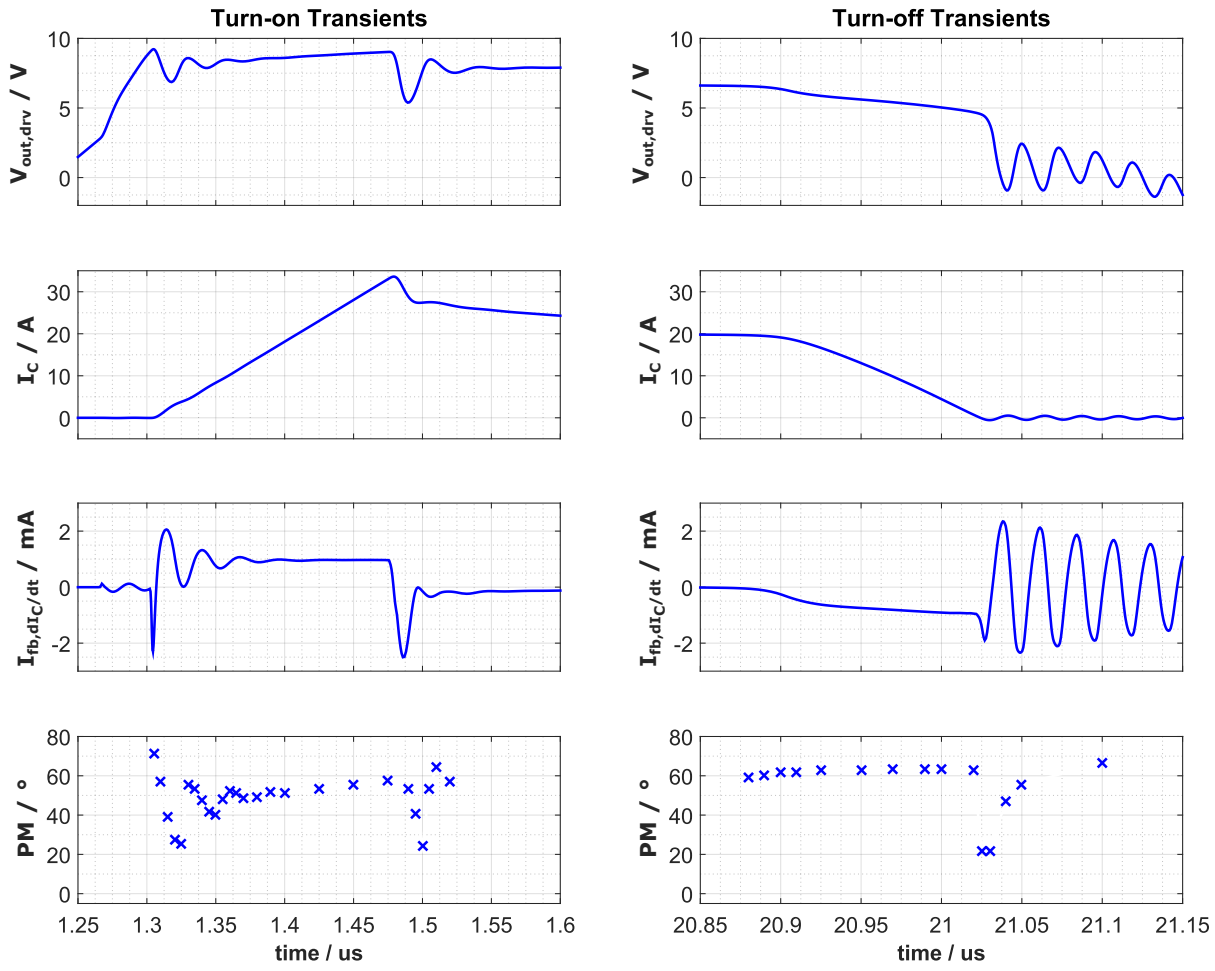


Fig. 4.22: Results of the stability analysis for the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ control loop for turn-on and turn-off. The phase margin is plotted for the different transient operating points.

a short period.

As the $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ control loop is marginally stable, methods for further stabilization are investigated in the following section.

4.5.3 Stability Improvement for the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ Control Loop

In terms of stability, the most critical operating point is during settling of the $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ control. Therefore, some measures for stabilization of this operating point are investigated. As pointed out in Sect. 3.3.2, one possible approach is the use of higher values for the gate resistor, as this potentially dampens the oscillations in the gate path and consequently on the amplifier output. Fig. 4.24a shows the transient waveforms for three different gate resistor values ($R_\mathrm{G} = 7\ \Omega$, $10\ \Omega$ and $15\ \Omega$).

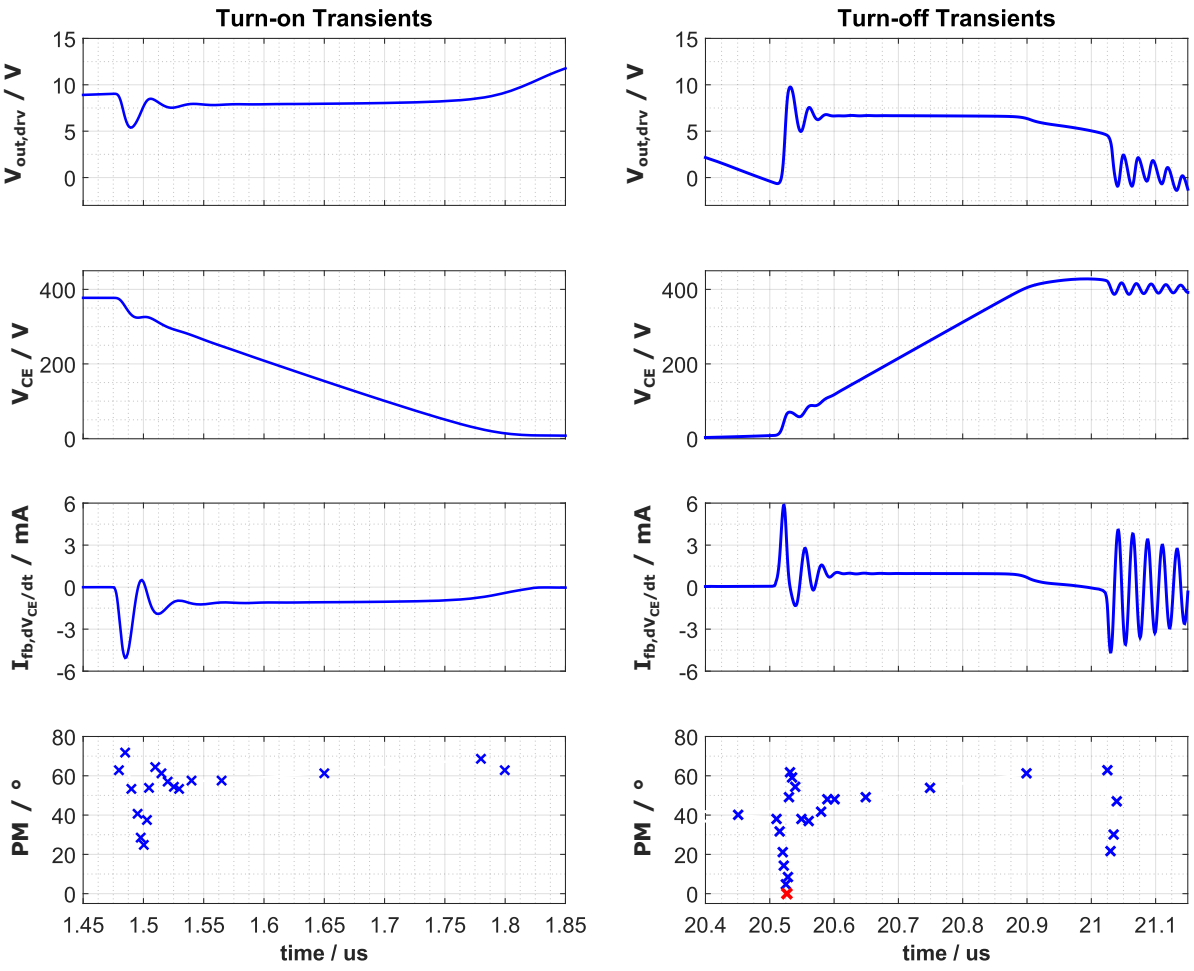


Fig. 4.23: Results of the stability analysis for the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ control loop for turn-on and turn-off. The phase margin is plotted for the different transient operating points.

The transient waveforms exhibit smaller overshoots for larger values of R_{G}. However, it takes longer until the system has settled. For a value of $R_{\mathrm{G}} = 15\ \Omega$, some small oscillations can still be observed on the amplifier output for the whole duration of the V_{CE} transition. However, the transient stability analysis reveals that the phase margin in the critical operating point only varies slightly with higher R_{G} ($\mathrm{PM}_{\mathrm{min}} = -1.2°$ for $R_{\mathrm{G}} = 10\ \Omega$ and $\mathrm{PM}_{\mathrm{min}} = -3.5°$ for $R_{\mathrm{G}} = 15\ \Omega$).

Another approach for stabilization is done by increasing the feedback gain of the negative $\mathrm{d}V_{\mathrm{out,drv}}/\mathrm{d}t$ control ($C_{\mathrm{fb,SR-}} = 1$ pF; N = 35 instead of $C_{\mathrm{fb,SR-}} = 825$ fF; N = 30) in order to reduce the voltage difference that has to be settled by the driver output, when the V_{CE} slope rises (see Fig. 4.24b). Besides that, lowering the DC gain (reducing the damping resistor R_{D} of the amplifier from 55 Ω to 40 Ω) leads to further reduction of the oscillations. The drawback of the stabilizing measures is that the turn-on switching delay is increased from 310 ns to 370 ns and the turn-off switching delay from 500 ns up to 660 ns.

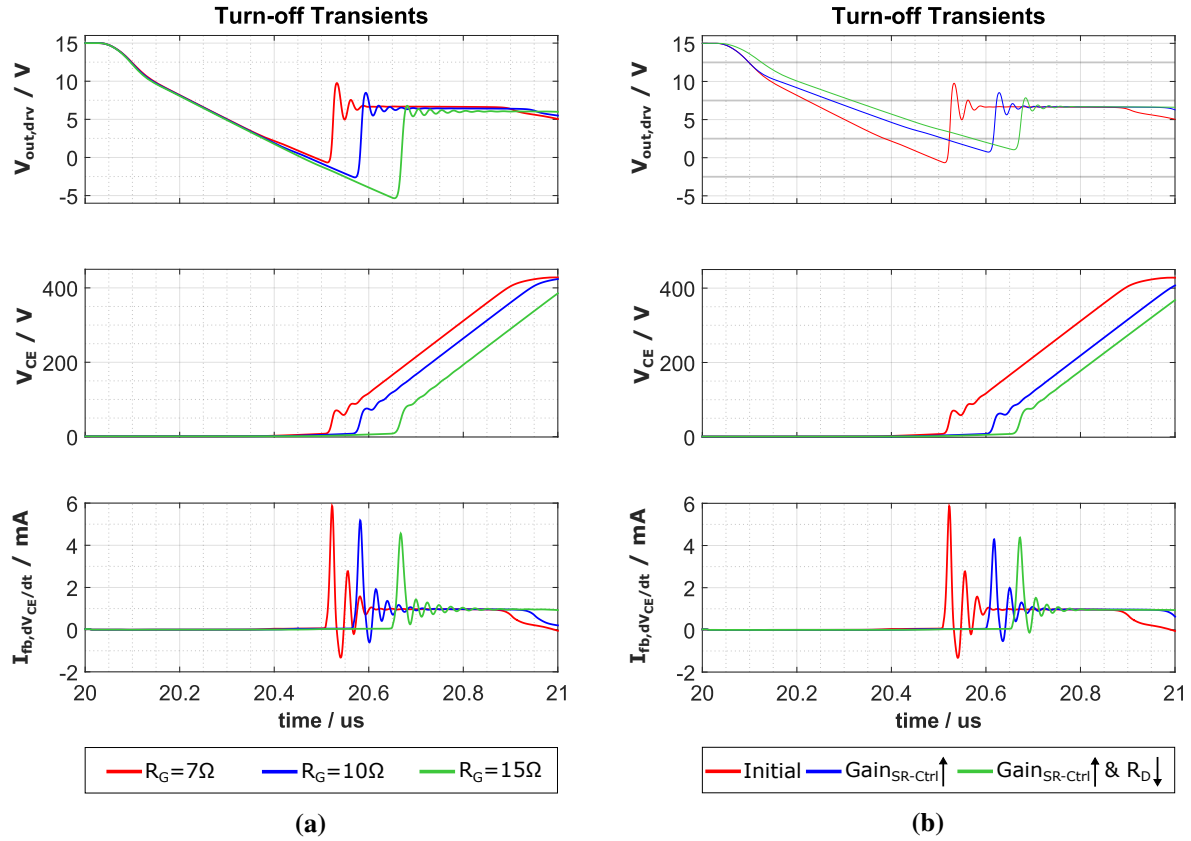


Fig. 4.24: Measures for stabilizing the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ in the critical operating point where the control loop settles: (a) Increasing the gate resistor R_{G} to 7 Ω, 10 Ω and 15 Ω (b) Reducing the DC gain of the amplifier (change R_{D} from 55 Ω to 40 Ω) and increasing the feedback gain of the negative $\mathrm{d}V_{\mathrm{out,drv}}/\mathrm{d}t$ control ($C_{\mathrm{fb,SR-}} = 1$ pF; N = 35 instead of $C_{\mathrm{fb,SR-}} = 825$ fF; N = 30).

The solution with adapted slew rate control and reduced damping resistor is further investigated. The results of a stability analysis for the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ loop are shown in Fig. 4.25. In comparison to the results of Fig. 4.23, the phase margin is higher during turn-on and turn-off. During turn-on, the minimum phase margin is 48° at $t = 1.56$ µs. In addition, the control loop is not unstable anymore during the settling phase at turn-off. The minimum phase margin is 10.3° at $t = 20.53$ µs. However, the phase margin during the ringing for $t > 21.17$ µs is still in the same region as for the results of Fig. 4.23. This ringing is mainly defined by the size of the stray inductance L_{S}. Hence, the phase margin in this region is not affected by the implemented stabilizing measures. As the DC gain is reduced, there is also some stability improvement expected for the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ loop. Hence, the stability is also verified for this control loop. The results for turn-on and turn-off are shown in Fig. 4.26.

Compared to the results of Fig. 4.22 the phase margin is higher and the system is more stable, for both, turn-on and turn-off. The minimum phase margin is around 50°. The only remaining critical point is at the end of the turn-off when the ringing due to the stray inductance occurs. This operating point cannot be influenced by the gate driver, such that a low-inductive design of the power circuitry is inevitable.

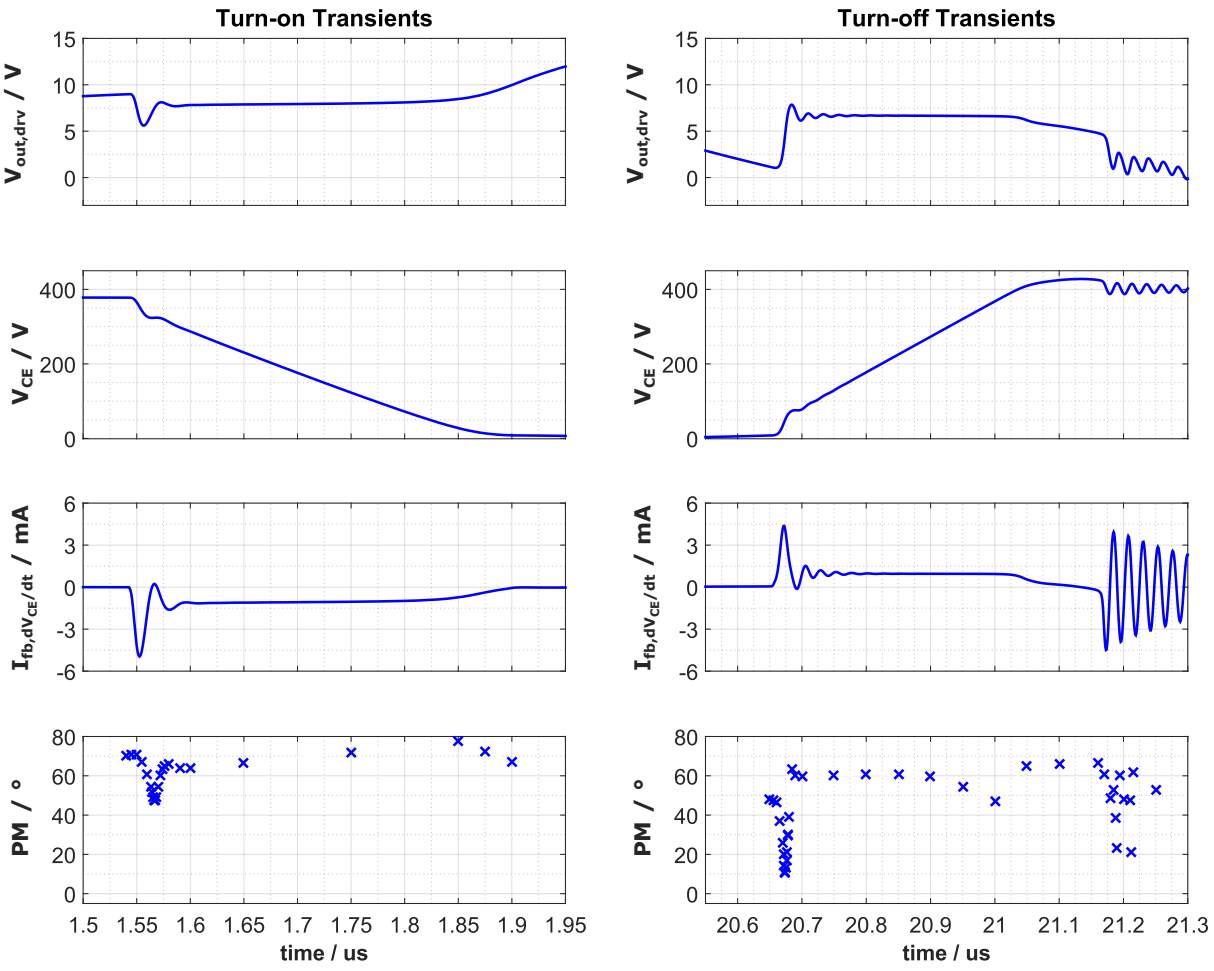


Fig. 4.25: Improved design: results of the stability analysis for the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ control loop for turn-on and turn-off. The phase margin is plotted for the different transient operating points.

4.5.4 Analysis of the Anti-Windup Control Loop

The stability analysis for the anti-windup $\mathrm{d}V_{\mathrm{out,drv}}/\mathrm{d}t$ control loop is done in the same way as for the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ control loops in the recent section. The waveform signals of the amplifier output, the feedback currents and the dedicated results for the phase margin are shown in Fig. 4.27. The positive slew rate control loop during turn-on is stable and the minimum phase margin is at 46° when the feedback currents starts to rise (at $t = 1.11$ µs). Thereafter, the phase margin rises back to 60° and stays there for the remaining turn-on switching delay. During turn-off, the phase margin of the negative slew rate control initially stays around 50°. When the gate reaches the Miller Plateau and the amplifier output settles (at $t = 20.67$ µs), the phase margin temporarily drops to 10° due to the large voltage difference the driver output has to overcome. When the feedback current of the negative slew rate control reaches zero and the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ control of the

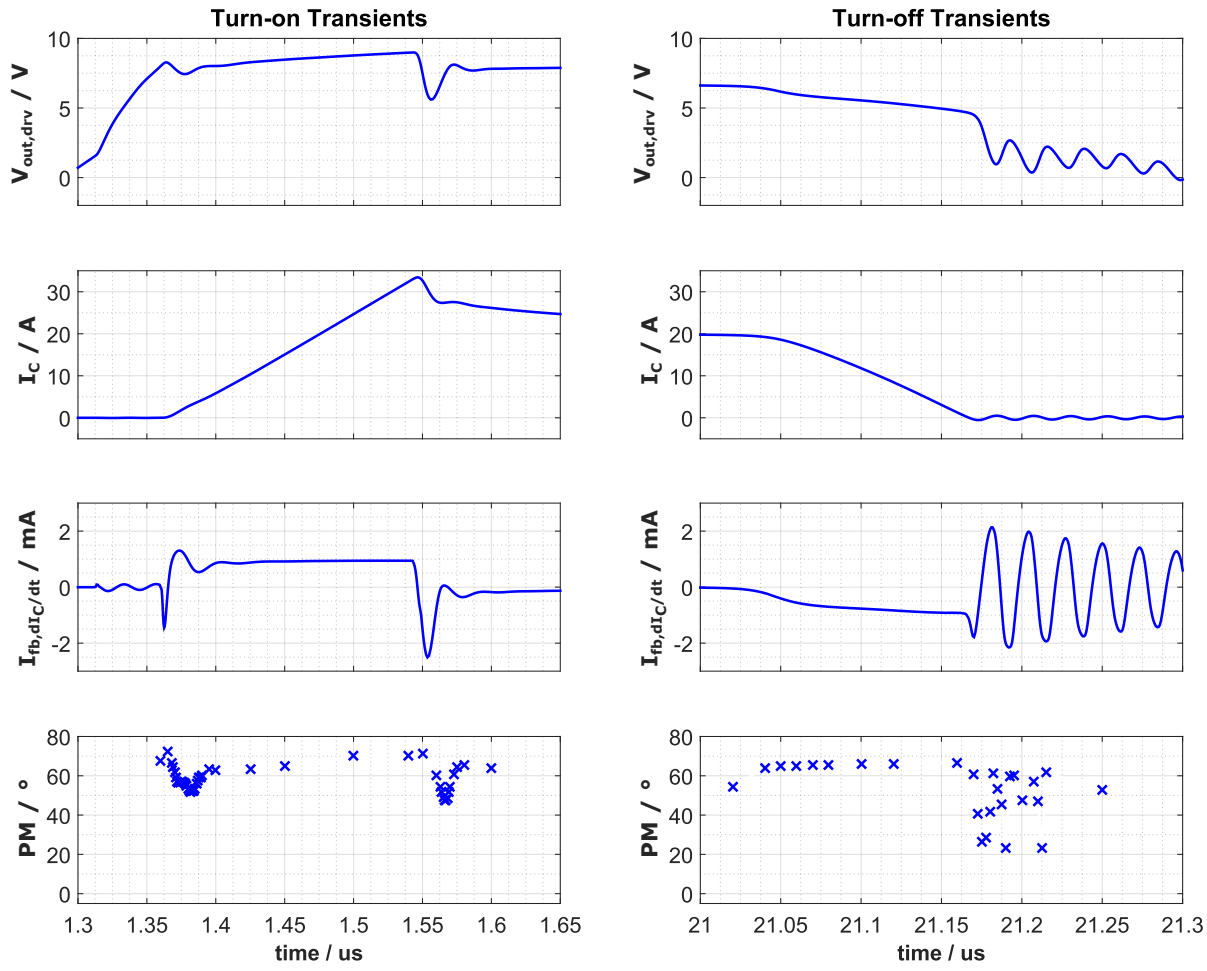


Fig. 4.26: Improved design: Results of the stability analysis for the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ control loop for turn-on and turn-off. The phase margin is plotted for the different transient operating points.

driver becomes active (at $t = 20.67$ µs), the phase margin goes up again and is at 40°.

As both positive and negative $\mathrm{d}V_\mathrm{out,drv}/\mathrm{d}t$ slew rate control loops show a very stable behavior, there are no further measures for stabilization necessary.

4.6 Slope Shaping

Slope shaping of V_CE and I_C can be achieved by adjusting the reference current I_ref. The achievable range of $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ and $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ has been determined using a sweep of $I_\mathrm{ref} = I_\mathrm{ref,on} = I_\mathrm{ref,off}$ from 0.25 mA to 4.5 mA. The results are shown in Fig. 4.28. For turn-on, the rates of $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ are in saturation for $I_\mathrm{ref} >$ 2.63 mA due to the limited voltage swing in the current summing node. This is also visible in Fig. 4.29a,

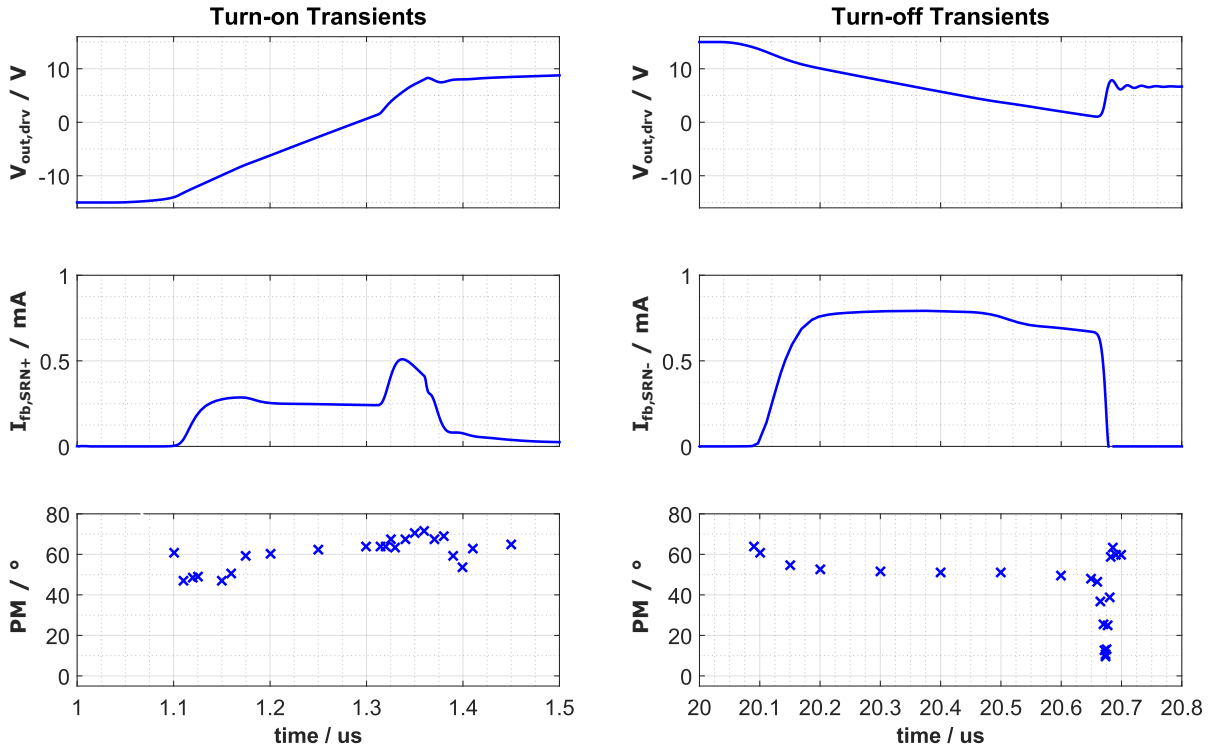


Fig. 4.27: Results of the stability analysis for the slew rate control loop for turn-on and turn-off. The phase margin is plotted for the different transient operating points.

where the transients for $I_{\text{ref}} = 0.63$ mA, 1 mA, 2.63 mA, 4.13 mA are shown. The slopes for $I_{\text{ref}} = 2.63$ mA and $I_{\text{ref}} = 4.13$ mA are almost identical. The slew rate of the transients can be adjusted within the following ranges for turn-on:

$$\mathrm{d}I_{\text{C}}/\mathrm{d}t \approx 0.05\ \text{A/ns} \ \text{ to } \ 0.58\ \text{A/ns}$$
$$\mathrm{d}V_{\text{CE}}/\mathrm{d}t \approx 0.25\ \text{V/ns} \ \text{ to } \ 3.25\ \text{V/ns}.$$

At turn-off, the rates of $\mathrm{d}I_{\text{C}}/\mathrm{d}t$ and $\mathrm{d}V_{\text{CE}}/\mathrm{d}t$ saturate for a reference current $I_{\text{ref}} > 4.13$ mA. The transients of the switching slopes for $I_{\text{ref}} = 0.63$ mA, 1 mA, 2.63 mA, 4.13 mA are shown in Fig. 4.29b. $\mathrm{d}I_{\text{C}}/\mathrm{d}t$ for $I_{\text{ref}} = 4.13$ mA is still well-controlled, whereas $\mathrm{d}V_{\text{CE}}/\mathrm{d}t$ exhibits a huge non-linear part in the beginning for this reference current, which covers more than 50 % of the transient duration. Therefore, the actual limit for $\mathrm{d}V_{\text{CE}}/\mathrm{d}t$ is rather at a reference current of 2.63 mA, where the non-linear part of the slope is comparably small. This leads to the following adjustable ranges of slew rate for the transients during turn-off:

$$\mathrm{d}I_{\text{C}}/\mathrm{d}t \approx 0.05\ \text{A/ns} \ \text{ to } \ 0.65\ \text{A/ns}$$
$$\mathrm{d}V_{\text{CE}}/\mathrm{d}t \approx 0.25\ \text{V/ns} \ \text{ to } \ 2.75\ \text{V/ns}.$$

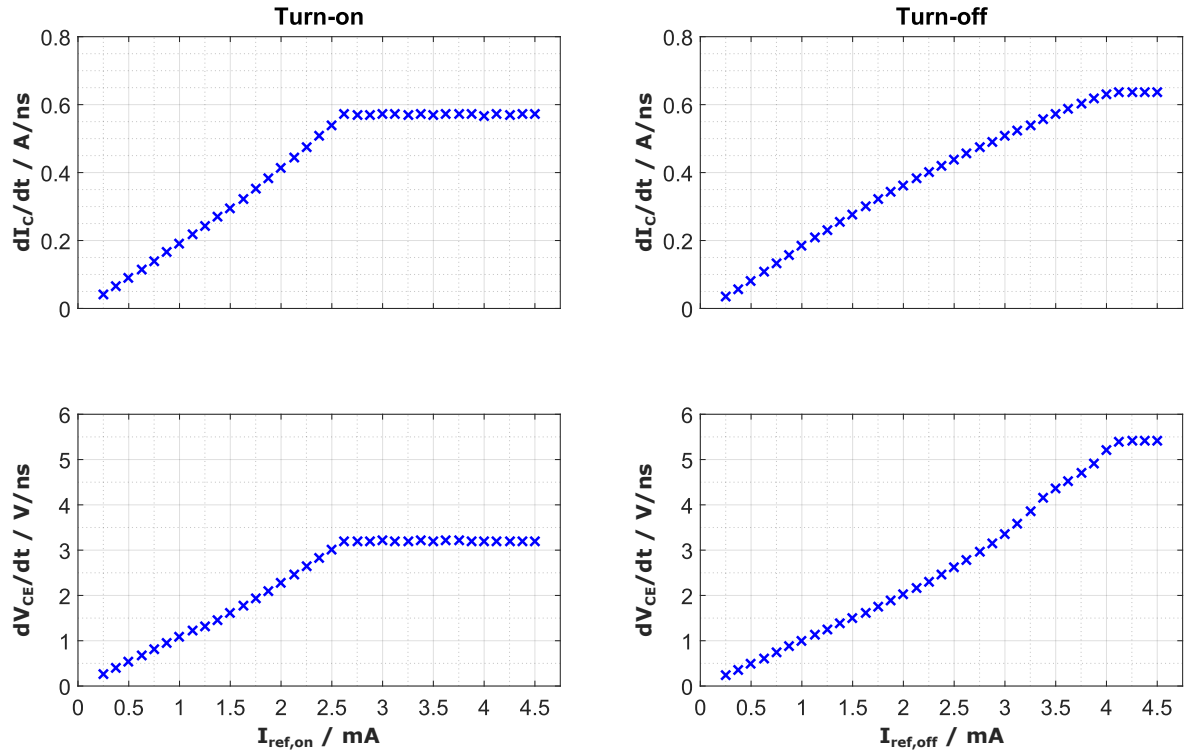


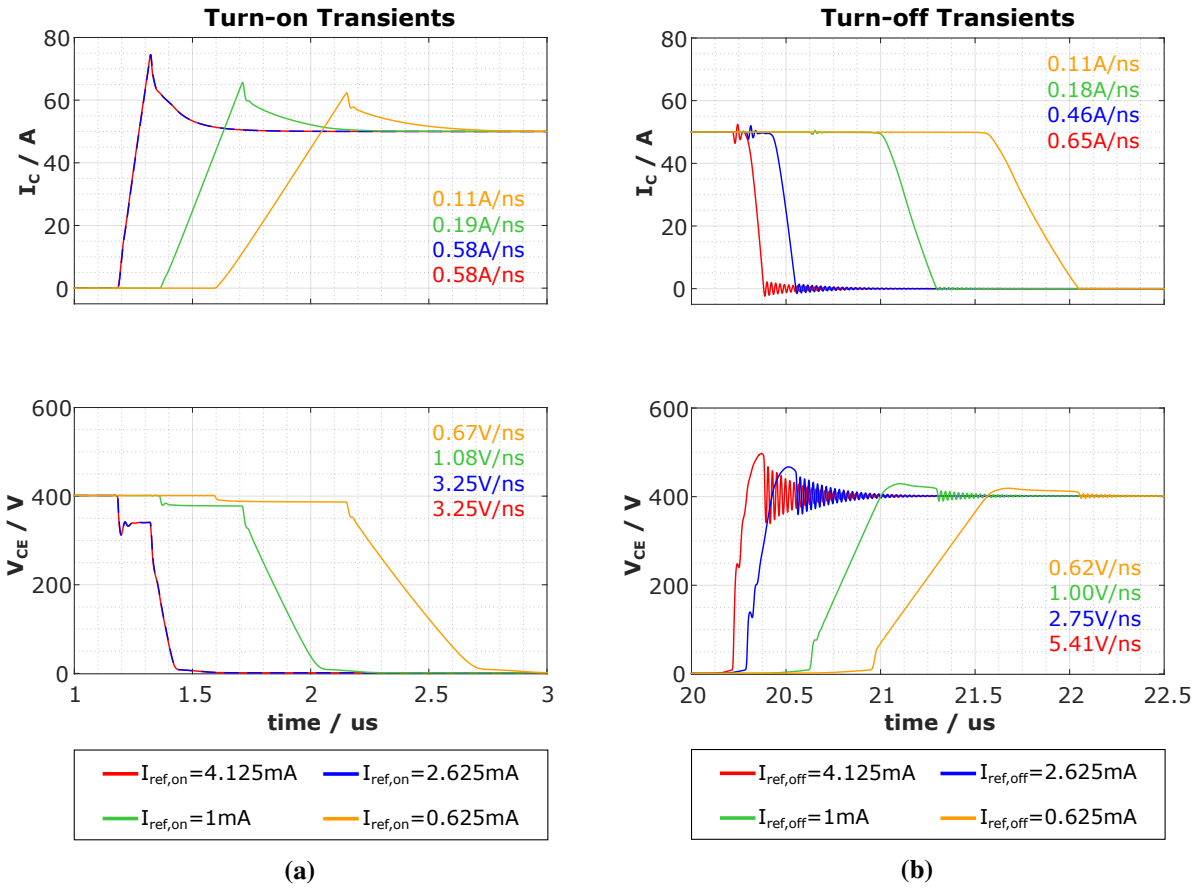
Fig. 4.28: $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ for sweeping the reference currents $I_{\mathrm{ref,on}}$ and $I_{\mathrm{ref,off}}$.

In addition, the switching delay is reduced when the reference current is increased (see Fig. 4.29a and Fig. 4.29b). The minimum switching delay, where all slopes are well-controlled (for $I_{\mathrm{ref}} = 2.63$ mA), is around 200 ns for turn-on and turn-off. Considering the requirements from Table 3.4, the values for $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ are in the specified range. However, this is not the case for the maximum $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$. It would be advantageous if the maximum $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ can be adjusted to approximately 1 $\mathrm{A/ns}$, as this would allow a further reduction of switching losses.

Therefore, the feedback gain G_{fb} of the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback network is decreased. This is done by lowering the *W/L* ratio of the differential pair to 45 µm/1 µm (due to lower maximum feedback currents), and by increasing the source degeneration resistor $R_{\mathrm{s,Mon}} = R_{\mathrm{s,Moff}}$ to 2 kΩ. The resistor $R_{\mathrm{b,Mon}} = R_{\mathrm{b,Moff}}$ for setting the operating point of the differential pair is also slightly reduced to 45 kΩ. The resulting feedback gains G_{fbon} and G_{fboff} for a sweep of $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ (from 0.1 $\mathrm{A/ns}$ to 1 $\mathrm{A/ns}$) is shown in Fig. 4.30. The results in Fig. 4.31, show that the maximum achievable values can be increased. This leads to the following ranges of $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$, which fulfill the specification:

$$\text{Turn-on: } \mathrm{d}I_{\mathrm{C}}/\mathrm{d}t \approx 0.10\ \mathrm{A/ns} \text{ to } 0.87\ \mathrm{A/ns}$$

$$\text{Turn-off: } \mathrm{d}I_{\mathrm{C}}/\mathrm{d}t \approx 0.09\ \mathrm{A/ns} \text{ to } 0.80\ \mathrm{A/ns}.$$



(a) **(b)**

Fig. 4.29: (a) Turn-on switching slopes for $I_{\text{ref,on}} = 0.63$ mA, 1 mA, 2.63 mA, 4.13 mA (b) Turn-off switching slopes for $I_{\text{ref,off}} = 0.63$ mA, 1 mA, 2.63 mA, 4.13 mA.

The corresponding transient waveforms of I_C for different I_{ref} are shown in Fig. 4.32. $\mathrm{d}I_C/\mathrm{d}t$ are well-controlled for turn-on (see Fig. 4.32a) and turn-off (see Fig. 4.32b).

4.7 Comparison with Passive Gate Drivers

In order to demonstrate the benefits of the closed-loop analog control, regarding the trade-off between switching losses, switching delay and SOA, it is compared with passive gate drivers according to Sect. 2.3.1. The first comparison is done with a common resistive driver, in which only the gate resistor is used to define the switching speed. The second comparison is made against an RC-compensated driver, which utilizes both external resistor and capacitor.

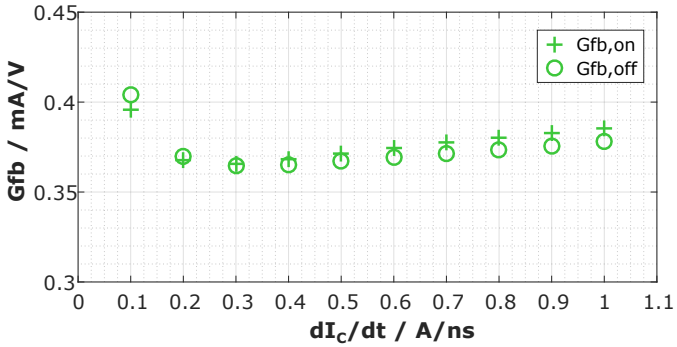


Fig. 4.30: Reduced feedback gain G_{fb}: Mean values of $G_{\mathrm{fb,on}}$, $G_{\mathrm{fb,off}}$ for sweep of ideal $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ (from 0.1 A/ns to 1 A/ns) applied on a 5 nH inductor.

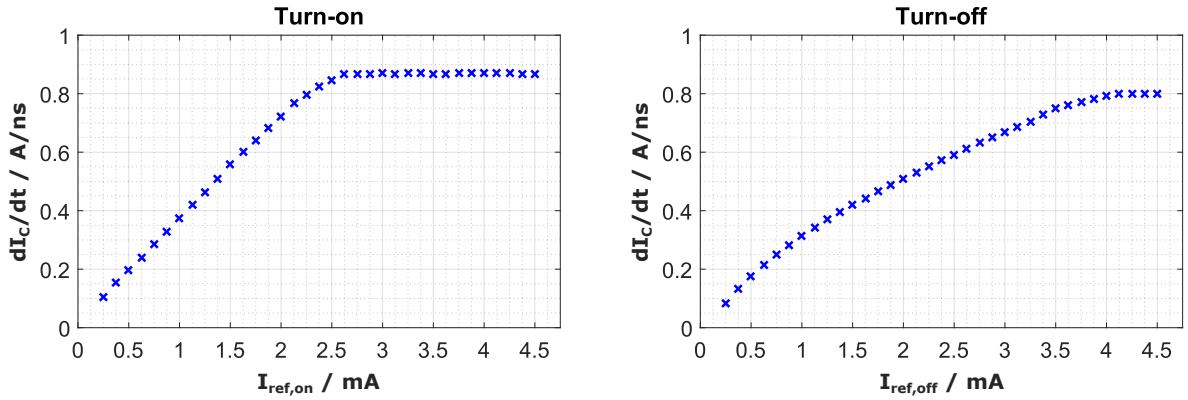
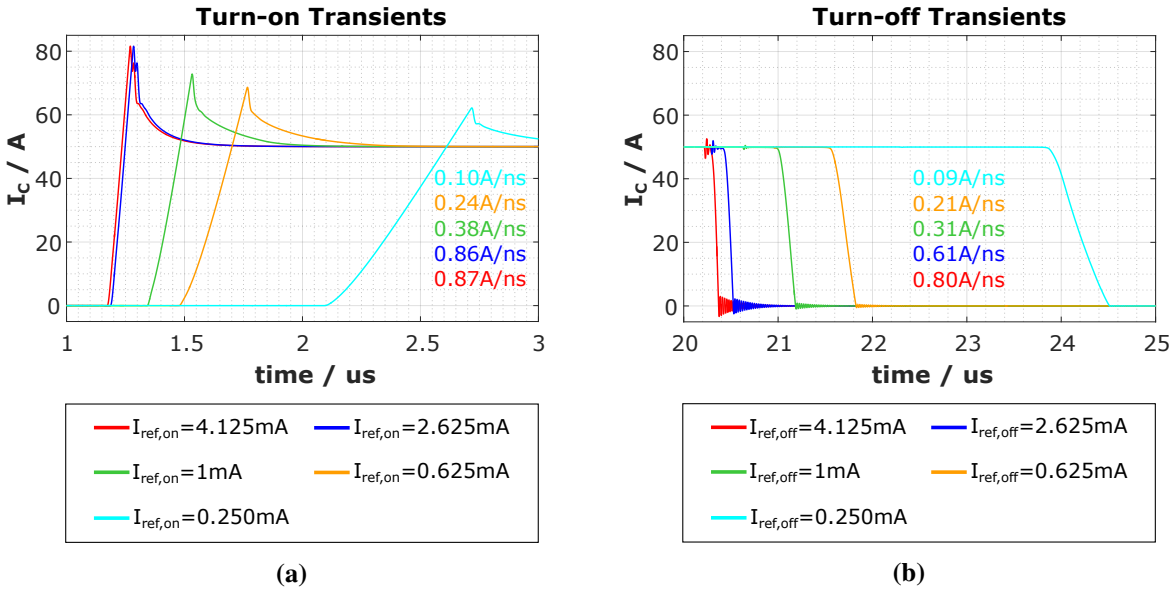


Fig. 4.31: Reduced feedback gain G_{fb}: $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ for sweeping the reference currents $I_{\mathrm{ref,on}}$ and $I_{\mathrm{ref,off}}$.



(a) **(b)**

Fig. 4.32: (a) Turn-on I_{C} slopes for $I_{\mathrm{ref,on}} = 0.25$ mA, 0.63 mA, 1 mA, 2.63 mA, 4.13 mA (b) Turn-off I_{C} slopes for $I_{\mathrm{ref,off}} = 0.25$ mA, 0.63 mA, 1 mA, 2.63 mA, 4.13 mA.

4.7.1 Resistive Gate Driver

The resistive driver uses a resistor for setting the slew rate of both $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$. The load current I_Load is set to the nominal current of 50 A and the DC link voltage V_DC to 600 V. The transients and the corresponding switching power and switching energy for turn-on and turn-off are shown in Fig. 4.33.

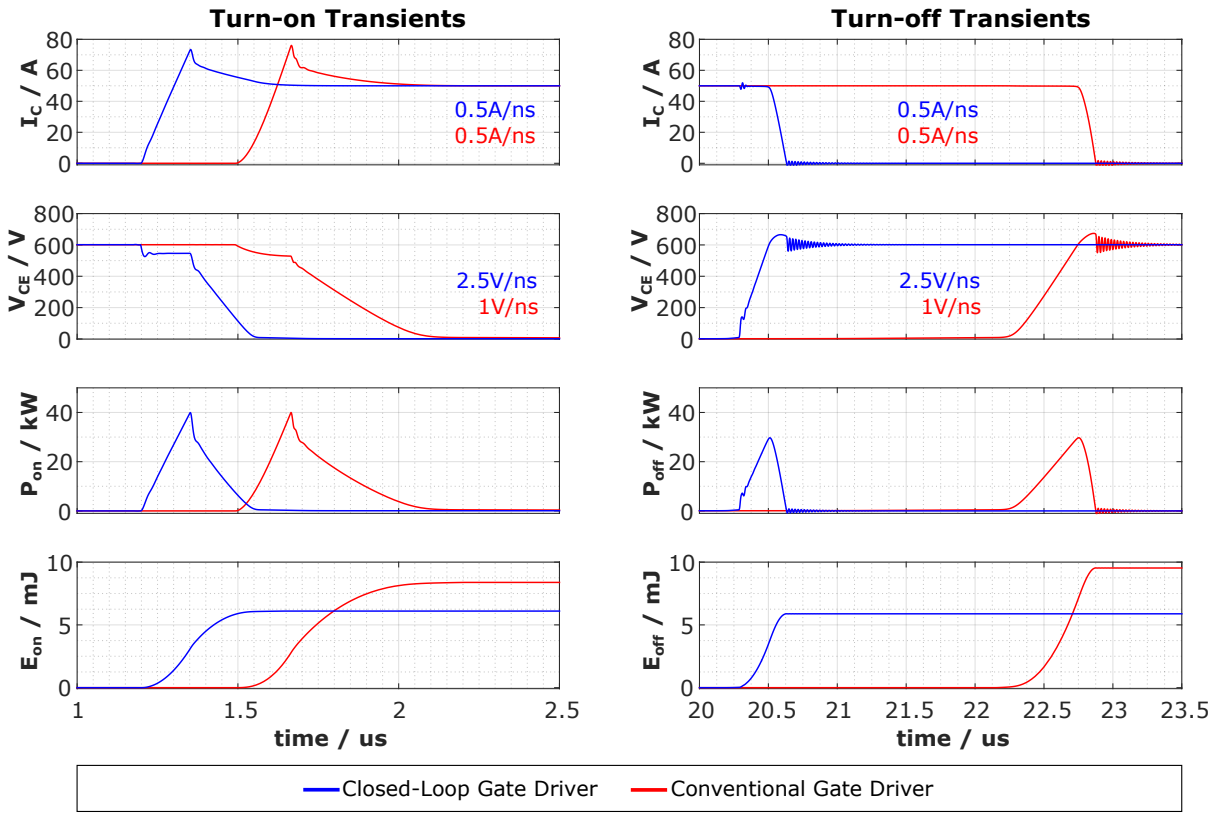


Fig. 4.33: Comparison of turn-on and turn-off switching slopes, switching power and switching energy for a conventional resistive gate driver and the closed-loop gate drive concept.

Both concepts are tuned for the same $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ ($\approx 0.5\ \mathrm{A/ns}$). Consequently, the peak reverse recovery current during turn-on and the turn-off overvoltage are similar for both drivers. The benefit of the closed-loop driver is the ability to control the $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ independently of the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$. Therefore, $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ can be set to a higher level compared to the resistive gate driver (closed-loop gate driver: $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t \approx 2.5\ \mathrm{V/ns}$; conventional gate driver: $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t \approx 1\ \mathrm{V/ns}$). Consequently, the switching losses of the proposed concept are much lower. Using the closed-loop gate driver reduces the switching energy by 2.3 mJ during turn-on and by 3.6 mJ during turn-off (6.1 mJ compared to 8.4 mJ (turn-on) and 9.7 mJ (turn-off) of the conventional driver). This means a reduction of 27% at turn-on and 37% at turn-off. In addition, the switching delays, especially during turn-off, are decreased when using the closed-loop gate driver.

In summary, the analog loop allows for a better trade-off between switching losses, switching delay and

SOA, in cases where the gate resistor of a conventional gate driver cannot be reduced due to limitations in SOA (restricts the maximum allowed $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$).

4.7.2 RC-compensated Gate Driver

If external capacitances $C_{\mathrm{GE,ext}}$ and $C_{\mathrm{GC,ext}}$ are used beside the gate resistor R_G (see Fig. 2.11), passive gate drivers are able to set $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ separately, as it is the case in the closed-loop concept. Therefore, the same level in switching losses can be achieved as in the analog loop concept. This case is illustrated in 4.34, exemplary for the turn-on transition. Both concepts are adjusted for both the same $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ (≈ 0.5 A/ns, as above in the resistive driver) and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ (≈ 1 V/ns and ≈ 2.5 V/ns).

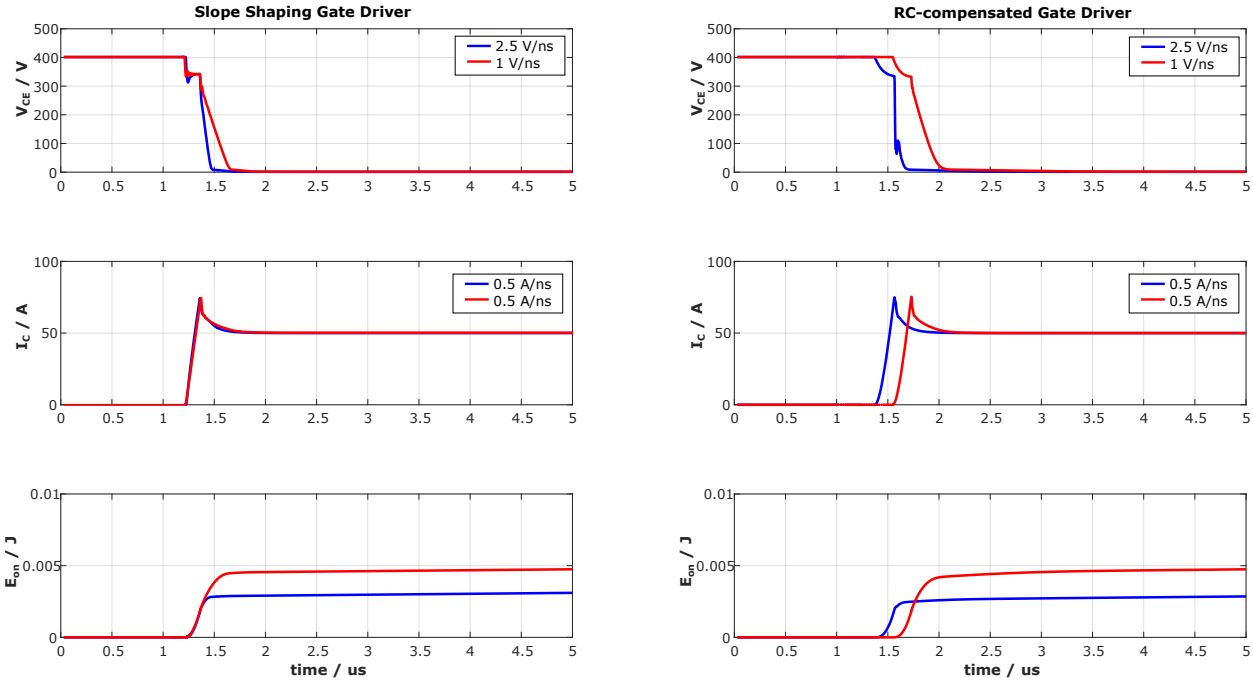


Fig. 4.34: Comparison of switching slopes and switching energy for a conventional RC-compensated gate driver and the closed-loop gate drive concept.

Although the switching losses can be tuned to be the same in both types of gate drivers, the closed-loop driver shows several advantages. The switching delay is smaller in the closed-loop gate drive for both cases shown. There is no recognizable switching delay variation between the different cases in the closed-loop concept. Due to the closed-loop regulation, $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ can be kept constant over the whole switching cycle, resulting in linear transition with a controlled solid waveform. The added capacitance to the conventional resistive drive can result in oscillations, which leads to an unregulated and non-linear behavior (see Fig. 4.34, blue V_CE curve for 2.5 V/ns).

5 Combined Digital and Analog Dual-Loop Slope Shaping

5.1 Introduction and System Overview

Figure 5.1 shows a block diagram of the dual-loop gate driver concept, derived from the fundamental blocks in Fig. 3.1, with a more detailed focus on the digital loop components.

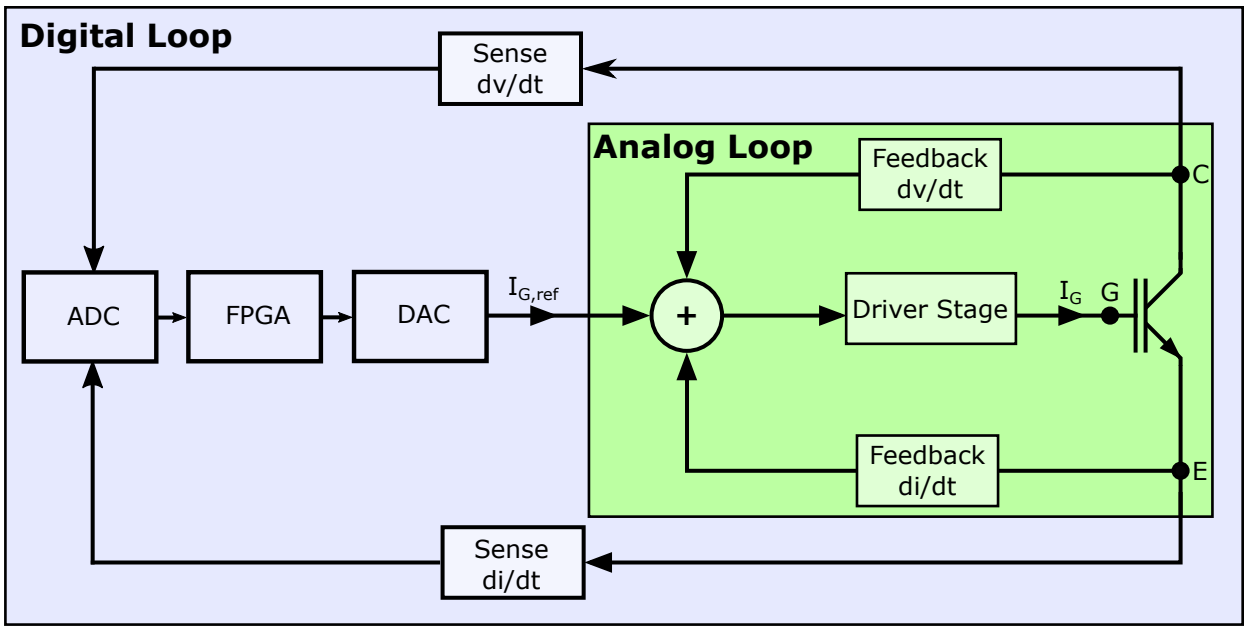


Fig. 5.1: Dual-loop gate driver with combined digital and analog slope shaping.

In the following sections, a full hardware evaluation module of the proposed dual-loop concept, with combined analog and digital closed-loop control of $\mathrm{d}I_C/\mathrm{d}t$ and $\mathrm{d}V_{CE}/\mathrm{d}t$, is developed and analyzed. This evaluation platform can be utilized for verification of the dual-loop system in an arbitrary set of the different loop parameters discussed in the previous chapters.

The analog loop blocks, as derived in Chapter 4, are designed in discrete hardware and built up on a PCB. The digital loop is implemented on an field programmable gate array (FPGA), using a digital PI controller,

and properly interfaced to the analog loop. With help of this hardware evaluation platform, the proposed dual-loop concept is verified and compared to a commercial passive gate driver.
As one of the essential benefits of the proposed driver, it ensures well-defined control, independent of the actual power device. Therefore, functionality of the gate driver is shown for different types of switches, such as IGBT, Superjunction MOSFET, and SiC. Due to the dual-loop combination of continous-time and adaptive regulation, precise slew rate control is enabled for a variety of gate-controlled devices.

5.2 Analog Loop

5.2.1 Analog Loop Hardware Concept

Figure 5.2 shows the concept of the analog $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ feedback loop according to Fig. 3.2. The individual circuit parts (digitally controlled current source, $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback, $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ feedback, driver stage) are now represented in discrete hardware. Every device with a frame in the schematic represents a discrete component with the corresponding type designation.

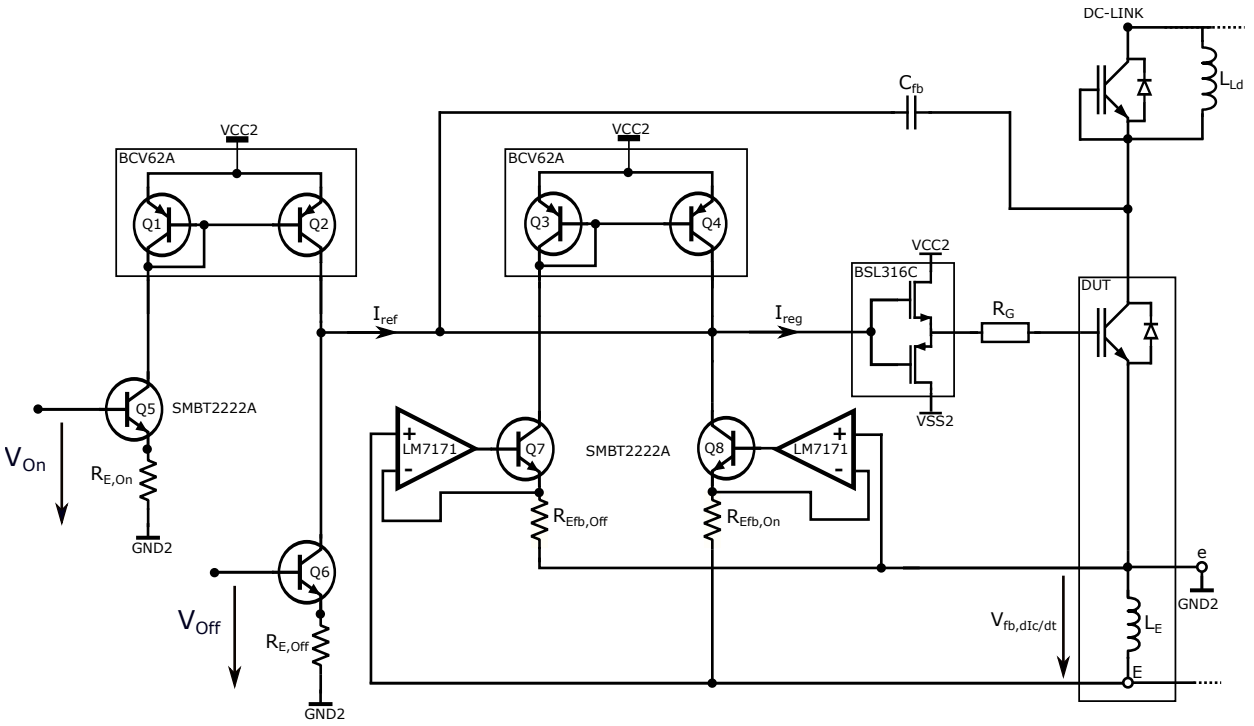


Fig. 5.2: Schematic of the concept with analog $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ feedback.

The reference current I_ref is set using a bipolar current source, consisting of a differential stage, and can be controlled in its magnitude by the voltages V_On and V_Off. The feedback capacitor C_fb, connected to the

drain or collector of the power device, provides negative feedback on $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ during a transition. After being further modulated by the negative $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback stage, the control error signal is represented by I_{reg}. Since the analog loop concept is based on current summation, the gate resistor R_{G} needs to fulfill the minimum gate resistor requirement, as postulated in Sect. 3.3.2, to achieve the stability criteria of the loop. The DUT can be represented by any kind of gate-controlled device. The only criterion for the power switch is an existing kelvin emitter or sense source pin, as it is the case in the newest TO-247-4 packages in four-pin-configuration.
The individual circuit blocks are explained in the following.

5.2.2 Reference Current Source

Fig. 5.3a shows the schematic for the reference current source, which is formed by a voltage controlled current source (VCCS). In order to perform an active turn-on and turn-off, a bidirectional reference current I_{ref} is required. The bipolar current source is controlled by the voltage V_{On} during turn-on and by V_{Off} during turn-off. The reference current generates a reference slew rate in the summing node according to Fig. 5.3b. The current source consists of bipolar differential stages with emitter degeneration, in order to achieve a high voltage swing and linear behavior in the current summing node. Discrete bipolar junction transistor (BJT) SMBT2222A and matched current mirrors BCV62A (both Infineon) are used, which fulfill the requirements on dynamics and voltage capability [104] [105].
In order to achieve a linear voltage-to-current conversion, emitter degeneration resistors $R_{\mathrm{E,On}}$ and $R_{\mathrm{E,Off}}$ are used. For turn-on, a positive voltage is applied to the base of Q5. The matched current mirror circuit injects the selected reference current into the analog loop. Hence, the reference current for turn-on can be described as

$$I_{\mathrm{ref,on}} = \frac{V_{\mathrm{On}} - V_{\mathrm{BE}}}{R_{\mathrm{E,On}}}. \tag{5.1}$$

with the base-emitter voltage $V_{\mathrm{BE}} \approx 0.6\mathrm{V}$ of the BJT.
The same applies to the case of turn-off, in which the transistor configuration behaves like a current sink. This concept is also capable of generating dynamic waveforms, which can be used for open-loop configurations of gate-drive concepts, as introduced in Sect.2.3.2. Therefore, the input voltages V_{On} and V_{Off} are provided by a programmable waveform generator or a digital-to-analog converter (DAC). The choice of the individual components like the bipolar transistors in the current source and the current mirror is justified by the requirements of the application, derived in Table 3.4. Those are shown together with the specifications of the selected parts in Table 5.1 and Table 5.2.

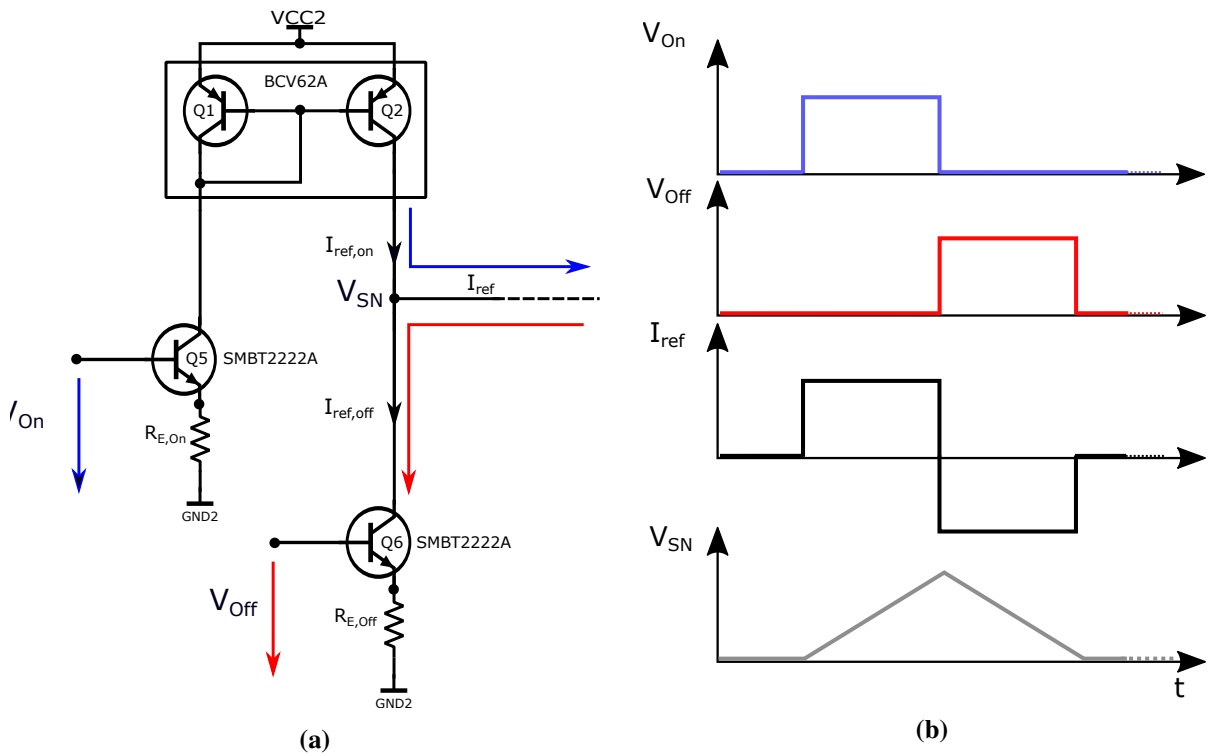


Fig. 5.3: (a) Voltage controlled current source schematic and (b) current source waveforms.

Tab. 5.1: Specification of the matched current mirror BCV62 [105].

Parameter	Requirement	Specification
$V_{CE,max}$	20V	30V
$I_{C,max}$	100mA	200mA
f_T	100MHz	250MHz

Tab. 5.2: Specification of the NPN Silicon Switching Transistor SMBT2222A [104].

Parameter	Requirement	Specification
$V_{CE,max}$	20V	40V
$I_{C,max}$	100mA	600mA
f_T	100MHz	300MHz

5.2.3 $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ Feedback

Fig. 5.4 shows the signal path of the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ feedback. It is implemented by a single high-voltage ceramic capacitor, which exhibits high linearity over a large voltage and frequency range. The 10pF capacitor GRM31A5C3A100JW01 (Murata) [94] fulfills the specifications and is therefore used in the hardware evaluation platform.

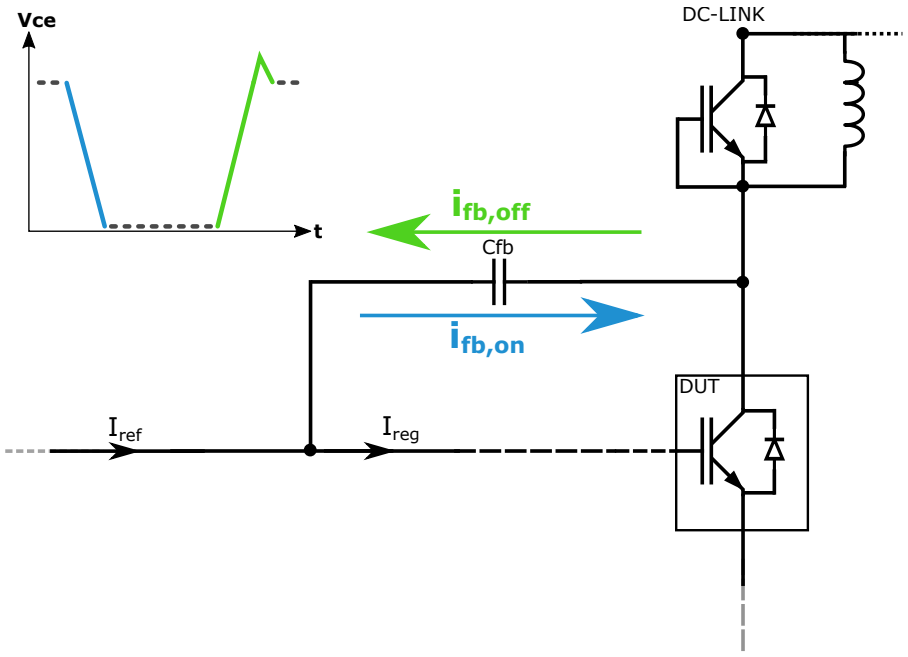


Fig. 5.4: Hardware realization of the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ feedback.

Since the feedback capacitor is directly connected to V_{CE}, its dielectric strength has to reach the value of the application specific DC link Voltage. Further, the value of the capacitance has to be as constant as possible under a wide range of conditions for providing a linear $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ feedback. Thus, the feedback capacitor has been implemented as a multilayer ceramic SMD device with a voltage rating of 1000V.

5.2.4 $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ Feedback

Fig. 5.5 shows the selected components for the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback.

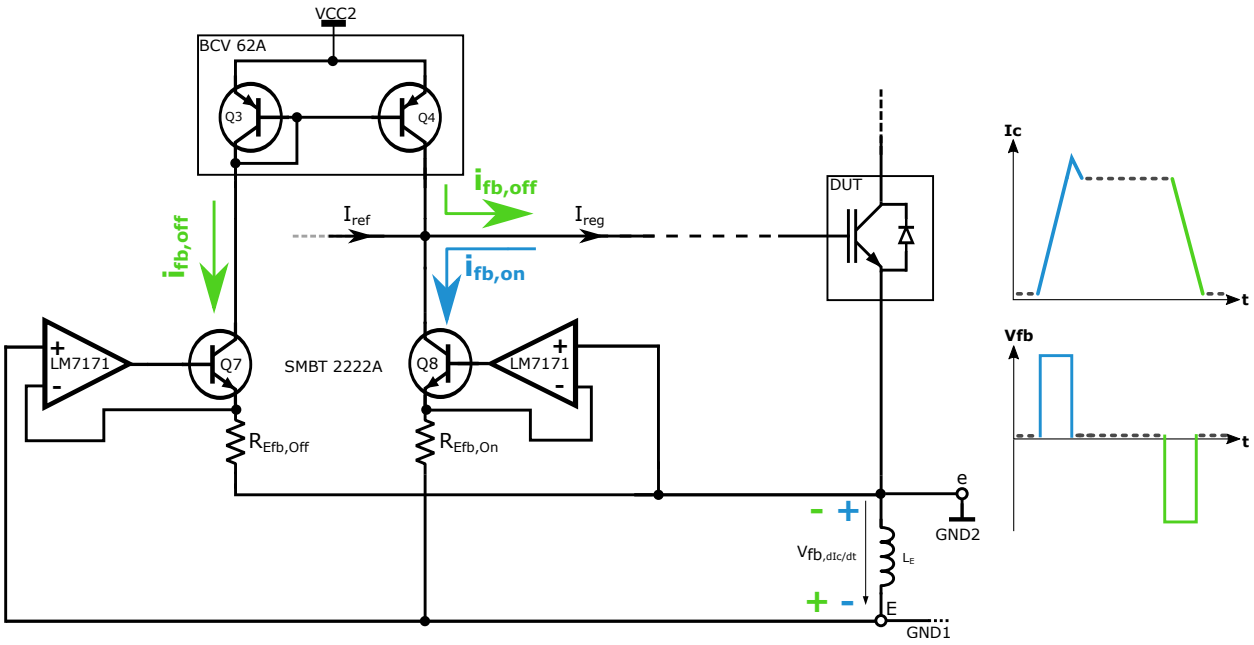


Fig. 5.5: Hardware realization of the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback.

During turn-on, the rising collector current induces a positive voltage $V_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t}$ across L_E. As a consequence, Q8 turns on and draws a feedback current $i_{\mathrm{fb,on}}$ from the output. For Q7, the negative base-emitter voltage turns off the device, resulting in $i_{\mathrm{fb,off}} = 0$. For turn-off, the falling collector current induces a negative voltage $V_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t}$. Hence, Q7 turns on and generates the current $i_{\mathrm{fb,off}}$, which is transferred to the output via the current sourcing mirror circuit formed by Q3 and Q4. During that time, Q8 is turned off due to the negative base-emitter voltage. The gain of the feedback stage can be adjusted by the value of the emitter degeneration resistors independently for turn-off and turn-on.

The generated feedback voltage $V_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t}$ has been measured for different rates of $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$. The results are shown in Fig. 5.6. As expected, an increase of the reference current I_ref results in an increasing rate of $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$. Thus, the amplitude peak of the induced voltage $V_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t}$ represents the maximum $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ during the transition.

5.2.5 Base-Emitter Forward Voltage Compensation

As discussed in Sect. 4.3.2, the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback path exhibits a lower limit set by the transistor threshold voltages, if it is in class-B operation. In the proposed hardware concept, this threshold represents the forward bias voltage V_BE of the base-emitter diode of the bipolar transistors Q7 and Q8. As a consequence, there is no feedback and thus no regulation for values of the feedback voltage $V_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t}$ below V_BE. Hence, the lower bound of the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ control range is limited to a specific value depending on the internal emitter lead inductance of the DUT, and the feedback transistors Q7 and Q8. Since the requirements on $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ are

depending on the application, and the DUT internal emitter lead inductance can vary from device to device, the base-emitter forward voltage V_{BE} is compensated by a local feedback loop, as depicted in Fig. 5.5. As a consequence, the base-emitter voltage is compensated by the negative feedback configuration of the operational amplifier. Additionally, the non-linearities of the bipolar transistor are compensated resulting in a linear dI_C/dt feedback transfer function.

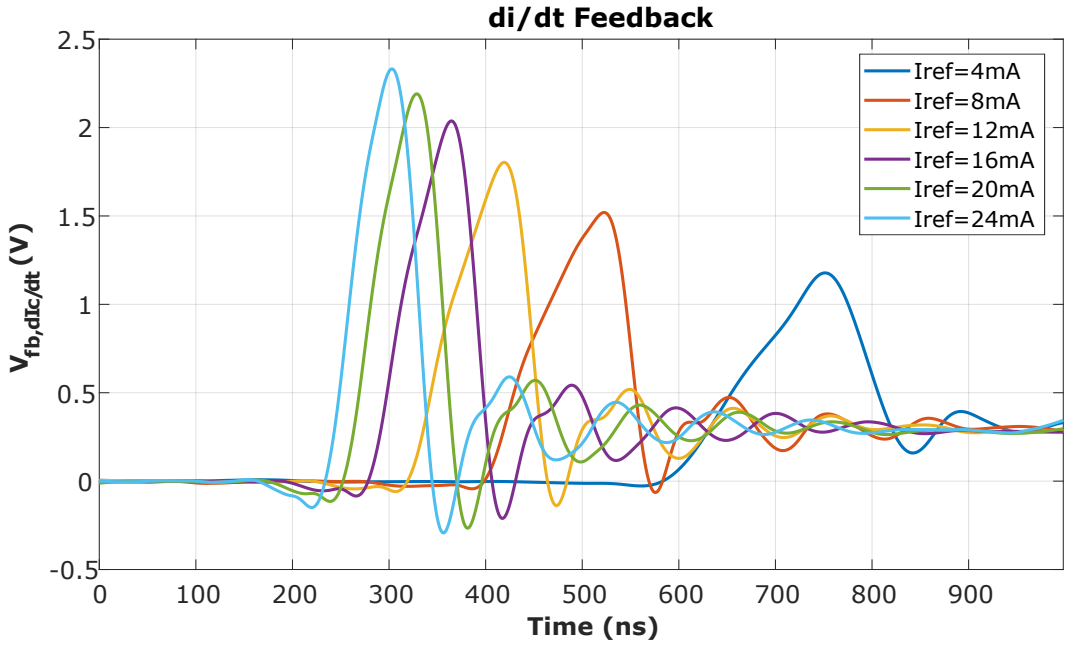


Fig. 5.6: Measured waveforms of the voltage drop across L_E for different reference current levels.

5.2.6 Driver Stage

In order to provide a hardware solution for the driver stage, the requirements, listed in Table 3.4, are shortly revised. The system requirement list demands for a driving capability of 5A, to keep the switching delays short. However, for the purpose of verification of the dI_C/dt and dV_{CE}/dt loop functionality, lower currents in the range of 1-2A are used. Furthermore, the transistors in the output stage require for a voltage capability of 40V in case of a bipolar power supply to fulfill the maximum ratings (see Table 3.4). For verification, a unipolar supply is sufficient, which relaxes the requirement on V_{max} to 20V. According to Sect. 4.1, the driver stage should further act as an impedance converter, which provides a high impedance node to the input and a low impedance node to the output.

A dual-MOSFET BSL316C (Infineon) [106], in source follower configuration, is chosen for the driver stage in this setup. This stage offers a higher input impedance compared to a BJT. The impedance-converting behavior of the source follower offers the required low output impedance. The BSL316C exhibits both an n-channel metal oxide semiconductor (NMOS) and p-channel metal oxide semiconductor (PMOS) transistor

on a single die, which fulfill the required specifications, see Table 5.3. The two transistors can be connected in the desired push-pull configuration for appropriate gate driving.
In contrast to the analysis in Sect. 4.1, the source follower is implemented in Class-B in the hardware evaluation platform. This may lead to distortion in the dead zone between the transistor threshold voltages. However, as the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ control range are outside of the dead zone, the Class-B approach is sufficient for the verification of the proposed dual-loop concept.

Tab. 5.3: Specification of the Dual-MOSFET BSL316C [106].

Parameter	Requirement	Specification
$V_{\mathrm{DS,max}}$	20V	30V
$I_{\mathrm{D,max}}$	1A	1.4A
$-I_{\mathrm{D,max}}$	-1A	-1.5A

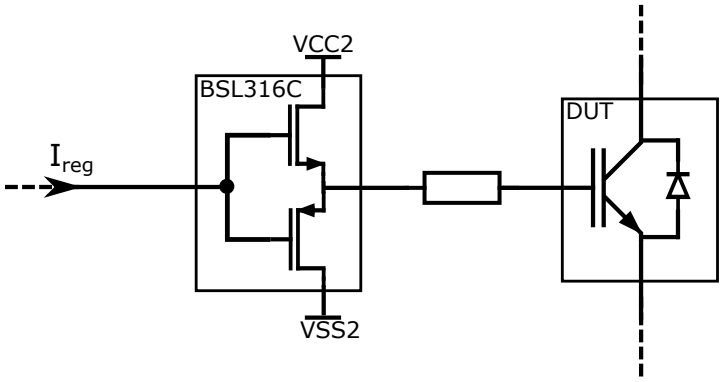


Fig. 5.7: Driver stage of the proposed concept.

5.3 Digital Loop

In this section, the requirements for the digital loop are determined and the selected hardware devices are introduced. Furthermore, the interfacing between the analog and digital loop and their components are discussed in hardware and software. Figure 5.8 shows the hardware for the dual-loop concept. It comprises the signal path for the digital loop with its analog circuit interfaces for the feedback signals and the DSP blocks.

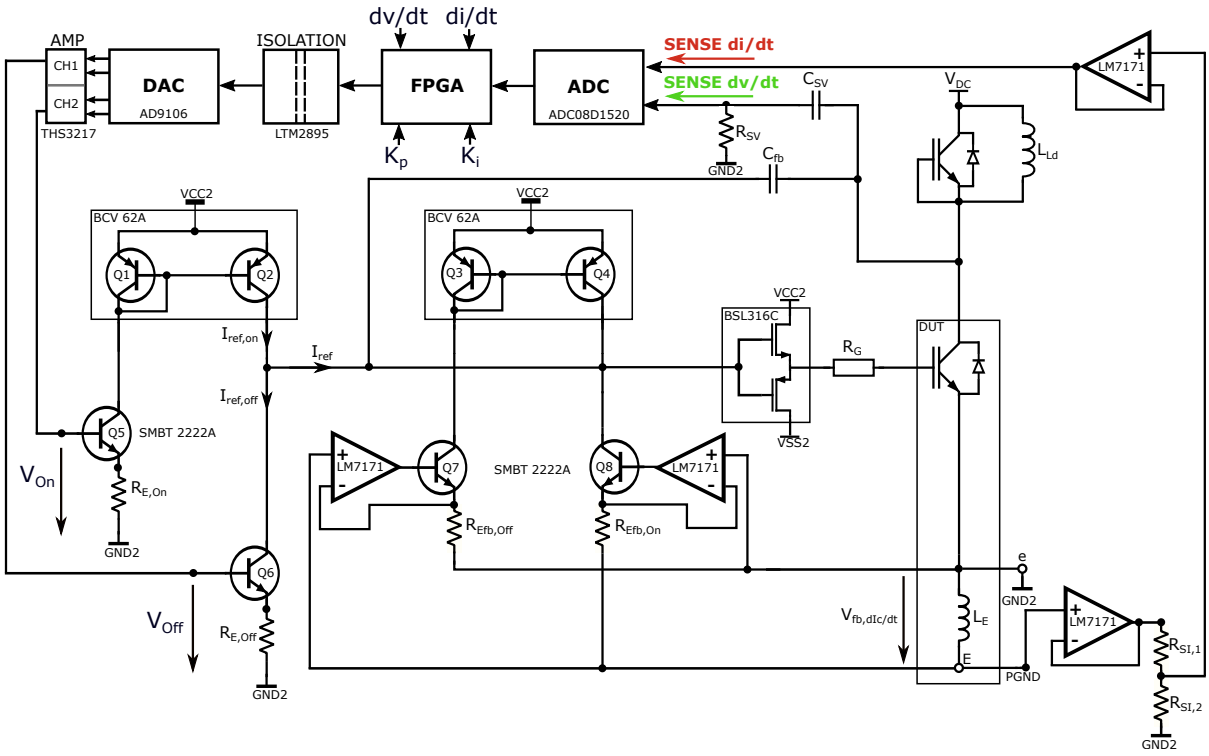


Fig. 5.8: Schematic of the dual-loop hardware concept.

The analog interface for the $\mathrm{d}I_C/\mathrm{d}t$ feedback is implemented with a voltage buffer (LM7171) followed by a resistive voltage divider formed by $R_{SI,1}$ and $R_{SI,2}$, according to the optimized sensing circuitry from Sect. 3.4. The high input impedance of the op-amp ensures that a minimal current is drawn from the source, while the low output impedance of the operational amplifier allows for driving of different loads. The amplitude of the $\mathrm{d}I_C/\mathrm{d}t$ feedback voltage can be adjusted by the voltage divider to the full-scale input range of the ADC. The $\mathrm{d}V_{CE}/\mathrm{d}t$ sensing is done with a high-pass filter formed by R_{SV} and C_{SV}, where the attenuation of the filter is utilized to adjust the amplitude of the feedback voltage, according to Eq. 3.14.

5.3.1 Operating Principle

In order to introduce the operating principle of the digital loop, a more detailed visualization of the proposed hardware and software scheme is shown in Fig. 5.9. The present switching slope of both current and voltage in the DUT is captured by the ADC. After the conversion from the analog to the digital domain, the digitized data is sent to the DSP unit on the FPGA. Depending on the actual rate of $\mathrm{d}I_C/\mathrm{d}t$ and $\mathrm{d}V_{CE}/\mathrm{d}t$, the DSP unit compiles a new waveform for the control voltages V_{On} and V_{Off}. These values are written into a look-up table (LUT) on the FPGA, before it is processed by a serial peripheral interface (SPI). Further supporting parameters, as for instance additional clock signals required for the DAC, are also generated in the within the FPGA.

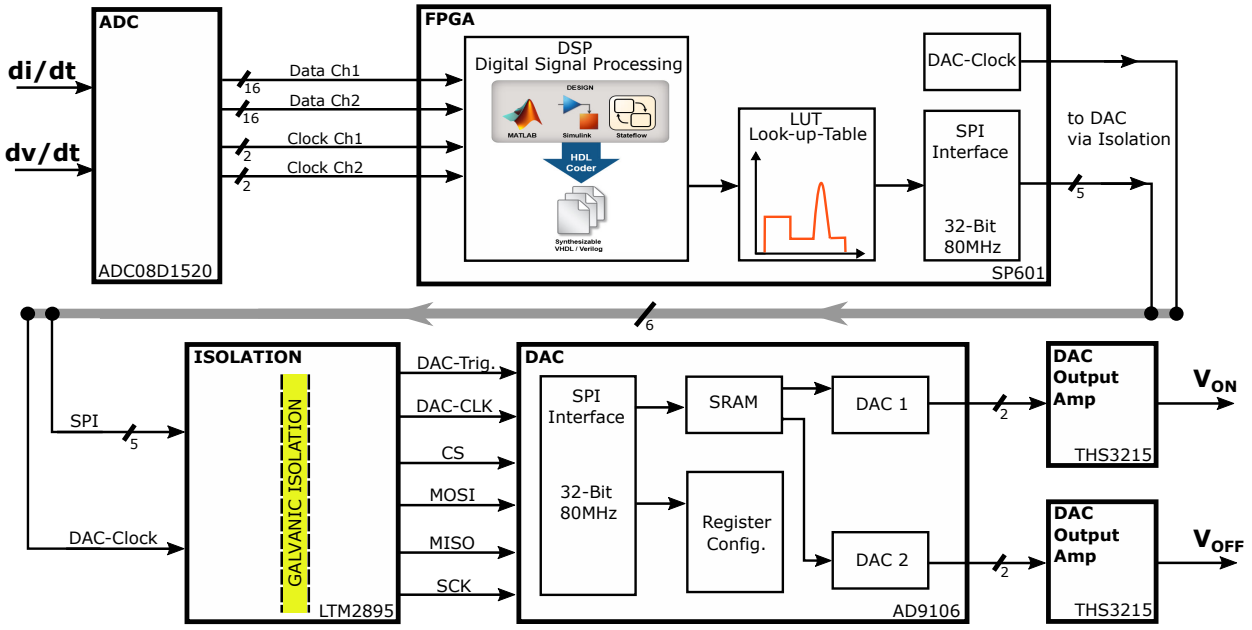


Fig. 5.9: Block diagram of the digital loop.

The SPI represents the communication channel between FPGA and DAC. Thereby, the V_{On} and V_{Off} waveform data and configuration commands are latched into the DAC via a galvanic isolation barrier. Within the dual-channel DAC, the waveform data is written into the SRAM from where it can be accessed by both channels (DAC 1 and DAC 2), which convert the digital waveforms back to the analog domain. Due to limited differential output voltage of the DAC, an amplifier is placed at both outputs. The amplifier converts the differential output signals to amplified single-ended signals, represented by the analog input voltages V_{On} and V_{Off}. The individual hardware blocks, shown in Fig. 5.9, are described in more detail in the following sections.

5.3.2 Analog-to-Digital Converter (ADC)

Since the ADC is responsible for quantizing the feedback signals of $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ for the digital closed-loop control, the requirements can be derived by an analysis of the feedback signal waveform, see Fig. 5.6. Considering the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback, measurements show that the maximum slew rate of $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ is approximately 2.5 A/ns in case of a CoolMOS$^{\mathrm{TM}}$. Thus, the minimum pulse width $t_{\mathrm{di,fd}}$ of the feedback voltage $V_{\mathrm{fb},\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t}$ can be described as

$$t_{\mathrm{di,fd}} = \frac{I_{\mathrm{Load}}}{\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t_{\mathrm{max}}} \approx \frac{50\ \mathrm{A}}{2.5\ \mathrm{A/ns}} = 20\ \mathrm{ns}. \tag{5.2}$$

In order to sample at least 20 points of data within $t_{\mathrm{di,fd}}$, the minimum required sampling rate of the ADC can be calculated to

$$f_{\mathrm{s\ min}} = \frac{\text{Number of samples}}{t_{\mathrm{di,fd}}} = \frac{20\ \mathrm{S}}{20\ \mathrm{ns}} = 1\mathrm{GS/s}. \tag{5.3}$$

As discussed in section 3.4, typical transient ringing is located around 100 MHz. Hence, the Nyquist criterion is fulfilled with the sample rate above. For the simultaneous conversion of $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$, two input channels are required. The full-scale input range of each channel determines the maximum differential voltage of the input signal that can be quantized. In the proposed concept, the feedback voltages can be adjusted with a voltage-divider for the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback, Fig. 5.8, and with a adjustable high-pass for the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ feedback. Thus, the minimum required input range is defined by the minimum values of the passive components that can be purchased. To transmit the quantized data to the FPGA for further signal processing, a standard data-interface such as SPI or low-voltage differential signaling (LVDS) is required.

Tab. 5.4: Requirements for the ADC and specification of the ADC08D1520 [107].

Parameter	Requirement	Specification
Sample Rate	1 GS/s	1.5 GS/s
Resolution	6 Bit	8 Bit
Number of input channels	2	2
Input Range (Vpp)	<1V	0.87V
Interface	SPI or Parallel LVDS	Parallel LVDS

The requirements for the ADC and the specification of the ADC08D1520 are summarized in Table 5.4. Since it is a dual-channel ADC, it enables the simultaneous conversion of two signal-sources ($\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$).

The block diagram of the ADC08D1520 is shown in Fig. 5.10. The input signals are multiplexed by the input multiplexer (INPUT MUX), which results in a time skew among the respective channels as each channel is sampled at a different time. To compensate the time skew, a sample and hold circuit keeps the sampled value and the ADC digitizes the frozen signal. After the conversion to the digital domain, the digitized data is fed into two buses via a selectable de-multiplexer. The data output is in *offset-binary* format and interfaced via LVDS.

The selected ADC is available as a reference board, see Fig. 5.10. This provides the ADC chip with all necessary supporting components like connectors, required clocks and hardware interfaces. Additionally, an on-board FPGA enables a fast data acquisition with the corresponding software which provides signal analysis functions and configurations. The on-board FPGA transfers the acquired data to the auxiliary FPGA mezzanine card (FMC) connector. This feature enables safe data transfer to other devices like external

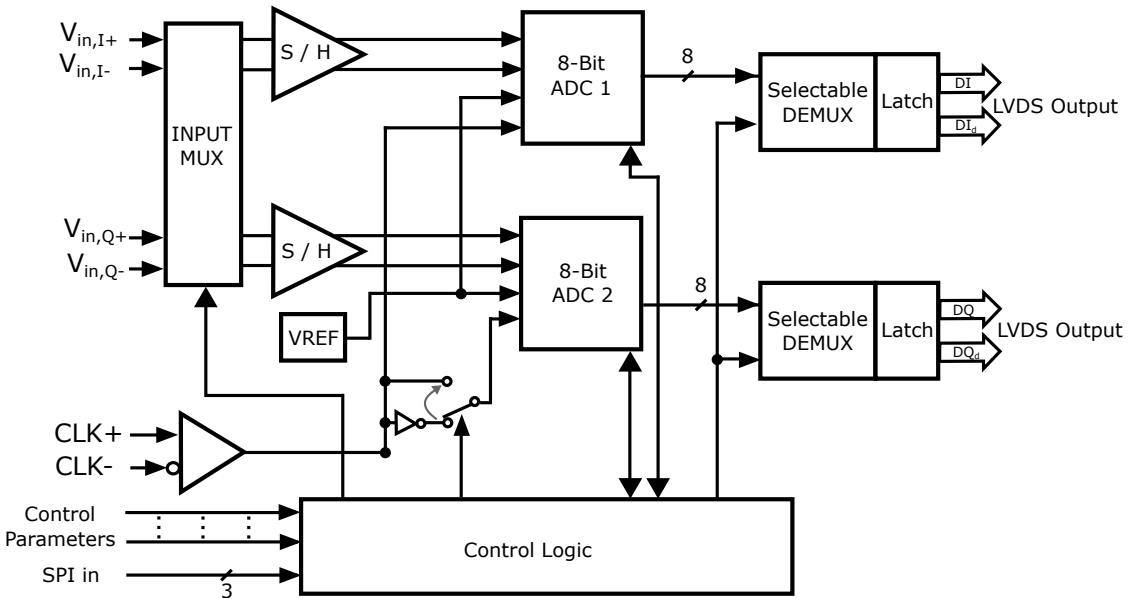


Fig. 5.10: Block Diagram of the ADC08D1520 [107].

FPGAs. As the ADC input is differential, the signals of the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback are connected to the ADC via a Balun (balanced-unbalanced) network, which converts the single-ended signal into a differential signal, as indicated in Fig. 5.11. To prevent a flow of DC signals into the ADC, DC block capacitors are applied which only allow the signals of the switching transients to pass through.

5.3.3 Field-programmable Gate Array (FPGA)

The FPGA represents the digital control unit of the proposed concept. Thereby, it is responsible for a variety of tasks that need to be fulfilled within the digital loop. The major requirements on the FPGA result from the infrastructure that needs to be provided to the digital control loop. Furthermore, the interfaces to the other components, like ADC and DAC, need to be realized. Since the ADC outputs parallel LVDS data through an auxiliary FMC port shown in Fig. 5.11, the FPGA also needs an FMC connector at its input, in order to feed the data from the ADC into the FPGA. Further, general-purpose input outputs (GPIOs) are required for further interface connections and debugging purposes. The selected hardware component for the FPGA is the Xilinx Spartan-6 SP601 Evaluation-Kit. It provides the Spartan-6 XC6SLX16 FPGA in combination with a variety of additional features.

The on-board FMC connector allows for a direct connection to the ADC without the usage of additional cables, see Fig. 5.12. Thus, the two PCBs can be patched together to reduce data loss in the communication path, which comprises 32 lines of data and 4 lines of decoding clocks, as indicated in Fig. 5.9. The further data processing and the implementation of the control system is supported by MATLAB. By using the software *Xilinx System Generator* for DSP and *Xilinx Model Composer*, it is possible to generate code

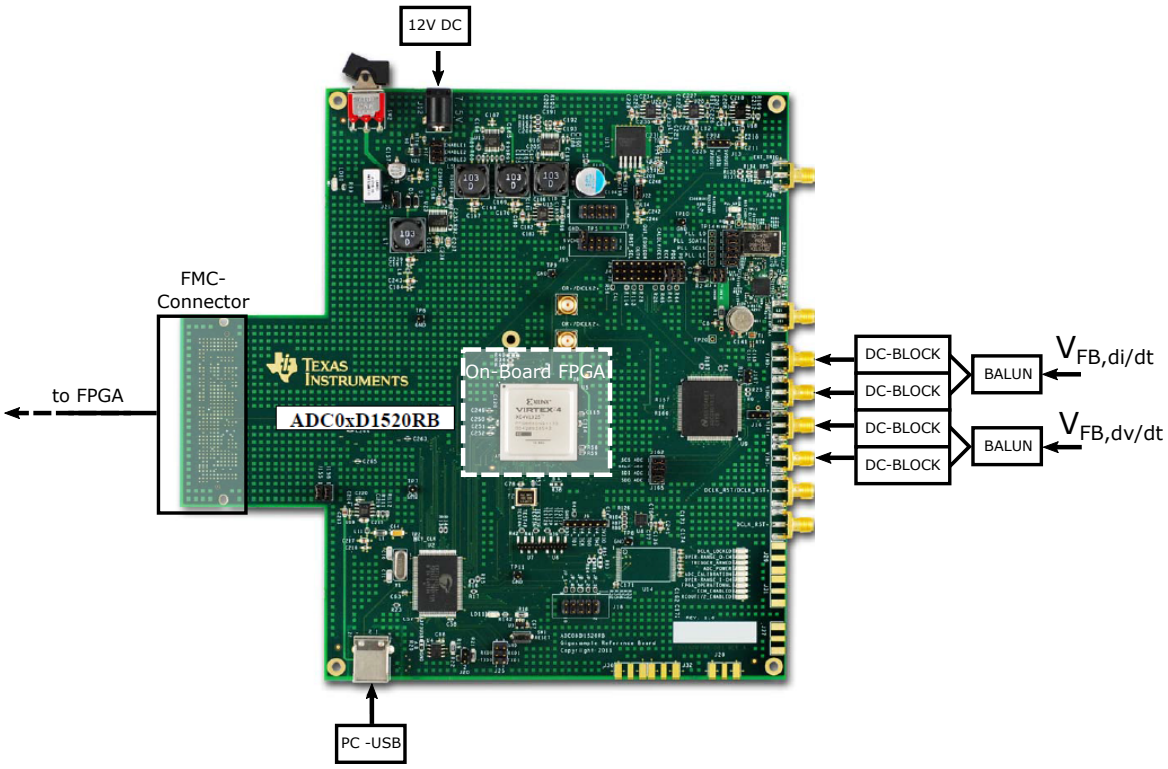


Fig. 5.11: Texas Instruments ADC08D1520 reference board [108].

for Xilinx FPGAs based on Simulink models. Hence, this enables the implementation of complex control algorithms in FPGAs. The implementation of the SPI is realized with the on-board GPIOs, which represent the connection to the DAC. Furthermore, signals for test and debugging purposes can be fed to GPIOs to enable rapid prototyping. In addition, user-buttons are used to initiate trigger signals for implemented state-machines. The programming of the FPGA is realized via an universal serial bus (USB) to joint test action group (JTAG) interface, which enables the connection to a host PC for an on-the-fly monitoring and programming of the control loop parameters during operation.

5.3.4 Gate Driver Isolation

In a gate driver, isolation is required for the electrical separation of the driver output, which exhibits high voltages and currents, and the digital control circuitry [110]. Signals can pass the isolation barrier using inductive, capacitive, or optical methods. Hence, protection is provided, as the isolation barrier blocks electrical power in case of component damage or failure. The requirements for the gate driver isolation can be derived from the respective application parameters. Thereby, the maximum DC link voltage V_{DC} represents the voltage that needs to be isolated. Thus, the rated dielectric insulation voltage has to be higher than the maximum DC link voltage. According to Table 2.1, this requirement is chosen to 1200 V to support

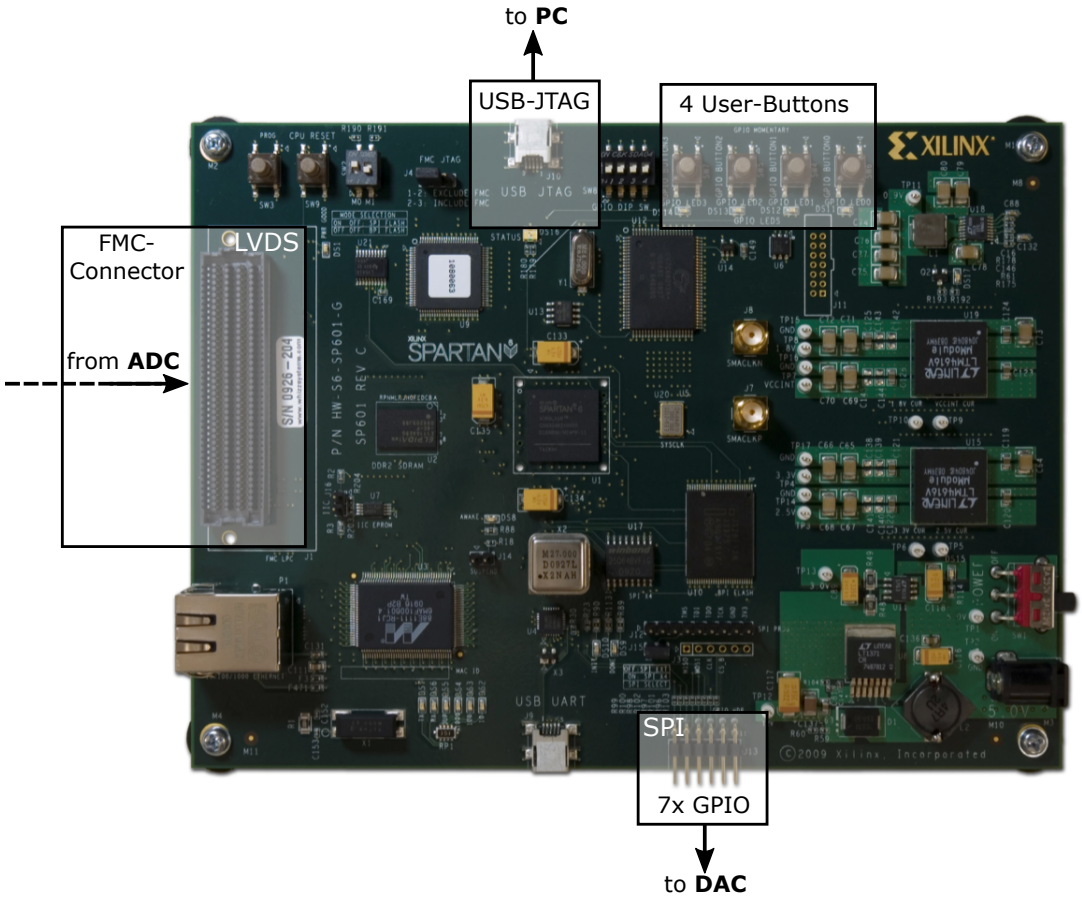


Fig. 5.12: Xilinx Spartan6-SP601 FPGA board [109].

common discrete devices. In the system, the isolation represents the barrier between FPGA and DAC, as indicated in Fig. 5.8. As the interface in use is SPI, the isolation has to support the SPI word length and the number of channels. The bandwidth, and therefore the common-mode transient immunity (CMTI), has to match the requirements of the DAC. For a suitable isolation of the dual-loop gate driver, providing safe and efficient digital slew rate control, the component LTM2895 (Analog Devices) has been identified as target element [111]. The component, which is based on coreless transformer (CT) technology, is commonly used in generic SPI and DAC applications and provides a high-speed isolated SPI interface. The galvanic isolation barrier tolerates large voltage ground variations between the logic interface and the isolated side of the LTM2895. Hence, an uninterrupted communication is maintained during high voltage transients. The isolation device is connected to the FPGA via a 4-wire SPI interface with an additional trigger signal for the DAC, as depicted in Fig. 5.13. The SPI word length can be adjusted in the range from 8 to 32 Bit and the maximum bandwidth is 100MHz. The requirements for the isolation device with the respective specifications of the LTM2895 are summarized in Table 5.5. The device is suitable for use with the FPGA and the DAC, which is described in the following section.

Tab. 5.5: Requirements for the isolation and specification of the LTM2895 [111].

Parameter	Requirement	Specification
Dielectric Insulation Voltage	1200 V	6000 V
Common Mode Transient Immunity	20V/ns	100V/ns
Interface	SPI	SPI
SPI Word Length	32 Bit	32 Bit
Bandwidth	80 MHz	100 MHz
Number of channels	5	5

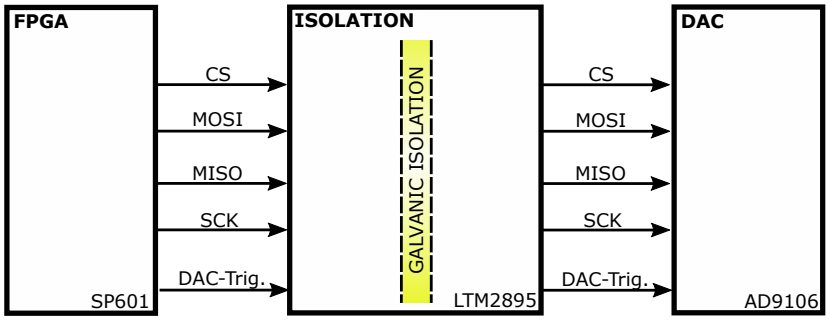


Fig. 5.13: Proposed coreless transformer (CT) isolation for the gate driver.

5.3.5 Digital-to-Analog Converter (DAC)

The DAC converts the digital waveforms of V_{On} and V_{Off} to the analog domain. The sample rate and the resolution are major parameters of digital-to-analog converters. The sample rate determines the temporal resolution, which is corresponding to the switching frequency of the application. In modern half-bridge topologies, the switching speeds are depending on the utilized power switch, as shown in Tables 2.3 and 2.4. For IGBTs, the switching frequency is in the range between between 1 and 60 kHz [112], see Table 2.1. Common switching frequencies for MOSFETs are in the range of 10 to 100 kHz, partially up to 200 kHz, see Tab 2.1.

An exemplary waveform for V_{On} comprising a duty cycle of 0.5, generated as both trigger signal and reference current representation for the nested analog loop, is shown in Fig. 5.14. Based on the maximum switching frequency, which is considered to be 100 kHz to cope with a variety of power switches, the duration of a PWM signal is calculated by

$$t_{\mathrm{SW}} = \frac{1}{100\,\mathrm{kHz}} = 10\,\mu\mathrm{s}. \tag{5.4}$$

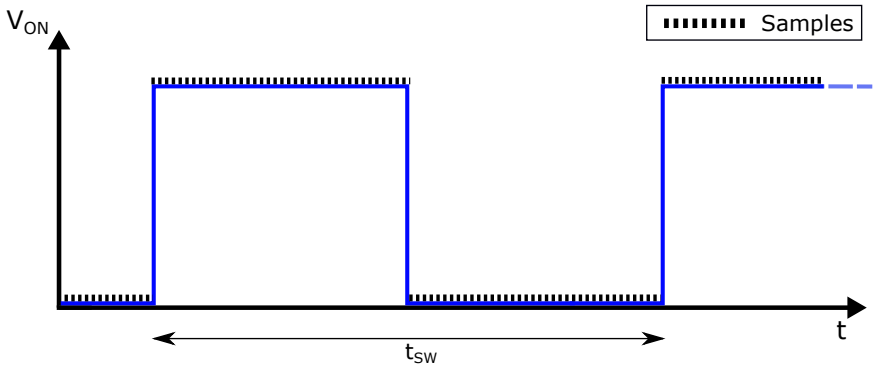


Fig. 5.14: Generation of a V_{On} signal.

To determine the required sample rate for the DAC, it is important to determine the number of sample points within one switching interval, that compose the later analog voltage, as qualitatively indicated in Fig. 5.14. In order to provide a sufficient resolution for the investigated switching times, the distance between two samples should not exceed 10 ns. Hence, 1000 samples are required within a switching interval of $10\mu s$ to obtain a sufficient resolution. The resulting sample rate of the DAC can therefore be calculated as

$$\text{DAC Sample Rate} = \frac{1000\ \text{Samples}}{10\ \mu\text{s}} = 100\ \text{MS/s}, \tag{5.5}$$

in order to achieve 1000 samples per period at a switching frequency of 100 kHz.
Within the digital control loop, the resolution of the DAC must be higher compared to the ADC in order to avoid limit cycle oscillations [113]. Hence, the condition is

$$\text{Resolution(DAC)} > \text{Resolution(ADC)}. \tag{5.6}$$

As the ADC exhibits a resolution of 8 Bit, the DAC requires 9 Bit or more to meet the condition in Eq. (5.6). The DAC needs to provide two single-ended output channels to individually generate the voltages V_{On} and V_{Off}. Therefore, the output voltage range of the DAC is of major concern, since the outputs are directly connected to the inputs of the VCCS, as shown in Fig. 5.9. Considering the range of I_{ref}, in which the analog loop shows linear control behavior, the maximum required value for I_{ref} is 30mA (see measurement results in Fig. 5.25). The minimum value is defined to 1mA in the requirements, see Table 3.4. Since the VCCS generates the reference current depending on the applied input voltage V_{On} and the value of the degeneration resistor ($R_{\mathrm{E,On}} = R_{\mathrm{E,Off}} = 50\Omega$, $V_{\mathrm{BE}} \approx 0.6$ V), the required output voltage range for a static reference current can be calculated as

$$V_{\mathrm{On,min}} = (I_{\mathrm{ref,min}} \cdot R_{\mathrm{E,On}}) + V_{\mathrm{BE}} = (1\ \text{mA} \cdot 50\ \Omega) + 0.6\ \text{V} = 0.65\ \text{V}. \tag{5.7}$$

$$V_{\mathrm{On,max}} = (I_{\mathrm{ref,max}} \cdot R_{\mathrm{E,On}}) + V_{\mathrm{BE}} = (30\ \mathrm{mA} \cdot 50\ \Omega) + 0.6\ \mathrm{V} = 2.1\ \mathrm{V}. \tag{5.8}$$

Thus, the DAC requires an output voltage range of 0.65V - 2.1V, in order to generate a static reference current I_{ref} within the specified range. The reference current range can be changed by exchange of the

Tab. 5.6: Requirements for the DAC and specification of the AD9106 [107].

Parameter	Requirement	Specification
Sample Rate	100MS/s	180MS/s
Resolution	$\leq$ 9 Bit	12 Bit
Number of output channels	2	4
Output Format	Single-Ended	Differential
Output Range (Vpp)	5V	1V
Input Interface	SPI	SPI

degeneration resistor. It has turned out, that a suitable value for the maximum required output range is 5 V, which is frequently used in practice. This allows for tests signals above the specified value of 2.1 V. The selected hardware component for the DAC is the AD9106 (Analog Devices). It provides a sample rate of 180 MS/s and an integrated on-chip pattern memory for waveform generation. The requirements for the DAC and the specification of the selected hardware component are shown in Table 5.6.
The on-board SRAM offers the option to store 4096 waveform data points of 12 Bit width, which can be accessed by each of the four differential DAC outputs simultaneously. There are gain adjustment factors and offset adjustments applied to the digital signals on their way into the four DACs which can be configured by the 128 configuration registers. The configuration access and the load of waveform data into the SRAM is accomplished by the SPI, which is described in the following section. The corresponding evaluation board, shown in Fig. 5.15, provides the AD9106 chipset with all supporting components. The requirements for the output range and the output format cannot be fulfilled by the selected DAC. However, an output amplifier with suitable voltage gain can be employed to meet the requirements. Therefore, the differential outputs are fed into an output amplifier, which is described in Sect. 5.3.6.

The communication between FPGA and DAC is enabled by an SPI interface, and is responsible for the transmission of the configuration and waveform data. The operation principle of the SPI interface is described in detail in the appendix (B). The SRAM is utilized as data pool for the calculated values for V_{On} and V_{Off}. Accordingly, register 3 stays fixed at the respective value in all commands used for the regulation loop. A dedicated space within the SRAM is assigned to the two individual DAC output waveforms (registers 4-7). In order to write data into the SRAM, the status-register (register 8) has to be set accordingly.
An qualitative visualization of the SRAM memory allocation is shown in Fig. 5.16. The whole SRAM is

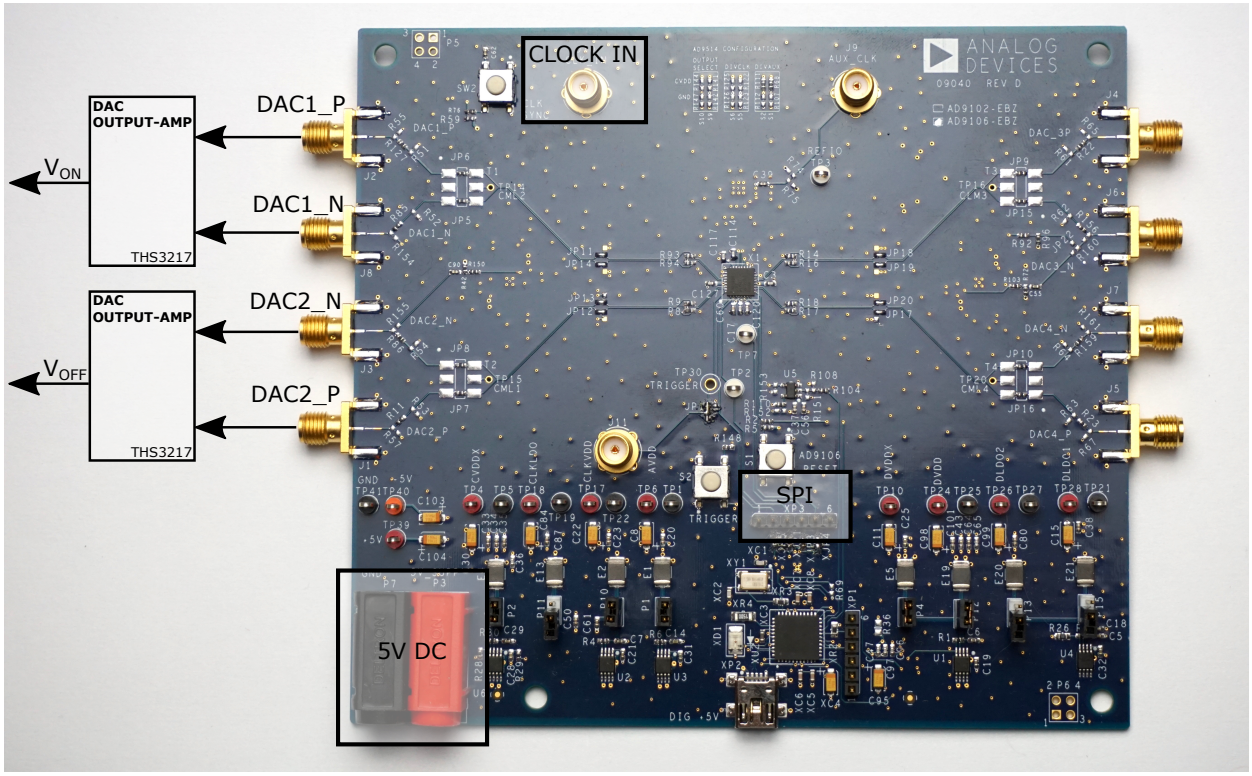


Fig. 5.15: Evaluation board for the DAC AD9106.

partitioned into two specific areas, which represent the dedicated memory locations for the waveforms V_{On} and V_{Off}. By configuring the start and stop address registers for the two DACs individually, by setting the registers 4 to 7 according to Table B.1 in the appendix, the allocated waveform data is accessed by both of the two DACs simultaneously. In this work, the waveform data for DAC1 is allocated between the SRAM addresses $0x6000$ and $0x67FF$, while DAC2 reads the data between $0x67FF$ and $0x6FFF$.
The configuration of the registers and the access to the SRAM is implemented with a state-machine. Therefore, the complete waveform generation has been partitioned into five states, as shown in Fig. 5.17. The state *idle* represents the initial condition, in which the state-machine is waiting for a command to start the generation of a new waveform. This command is provided by the control system implemented on the FPGA. Within the next state, the configuration of the required registers is done, as shown previously. Having finished the configuration, the waveform data for V_{On} and V_{Off} is written from the LUT of the FPGA into the SRAM. After that, a post-configuration is required to update the register values, such that the data in the SRAM can be read out by the individual DAC. Finally, the DAC outputs the analog waveform.

5.3.6 DAC Output Amplifier

According to Table 5.6, two requirements cannot be met by the AD9106, the format of the output signal (single-ended instead of differential), and the output voltage range of the DAC (up to 5 V instead of 1 V).

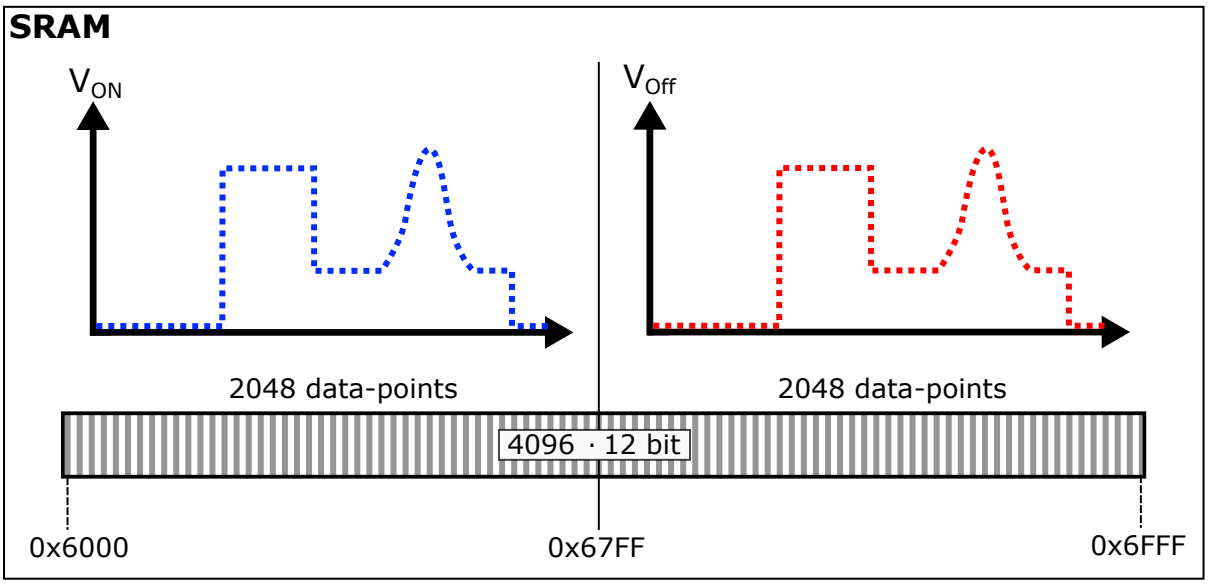


Fig. 5.16: Memory allocation in the SRAM.

Hence, an output amplifier is necessary, to properly provide V_{On} and V_{Off}.

Considering the output of the AD9106, the format is differential (OUTP and OUTN). The difference between those outputs (OUTP-OUTN) represents the single-ended output signal OUTSE, which is required to interface to the analog loop, as indicated in Fig. 5.18. Therefore, the DAC output amplifier has to be capable of converting the output of the DAC from differential to single-ended. Furthermore, the output amplifier must provide sufficient voltage gain to achieve the required voltage level (Table 5.6). Considering the maximum output voltage of the DAC (1 Vpp), the gain of the output amplifier has to be minimum 5 V/V to achieve the required output voltage of 5 Vpp.

A further parameter is the output slew rate. The requirement for the slew rate can be derived from the highest $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ and the appropriate minimum time interval as described in Eq. (5.2). To enable dynamic shaping of the reference current, the output voltage of the DAC, and therefore the input voltage V_{On}, was selected such that a change from 0 to 5 V is possible within 20 ns. This enables at least four different reference current levels during every $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ transition. The required slew rate (SR) can be expressed as

$$SR_{min} = \frac{5\ \mathrm{V}}{5\ \mathrm{ns}} = 1\ \mathrm{V/ns}. \tag{5.9}$$

The amplifier THS3217 copes with the slew rate of the DAC according to 5.9, provides the required gain for the output scaling and converts the signal to single-ended. The specifications of the component are listed in Table 5.7.

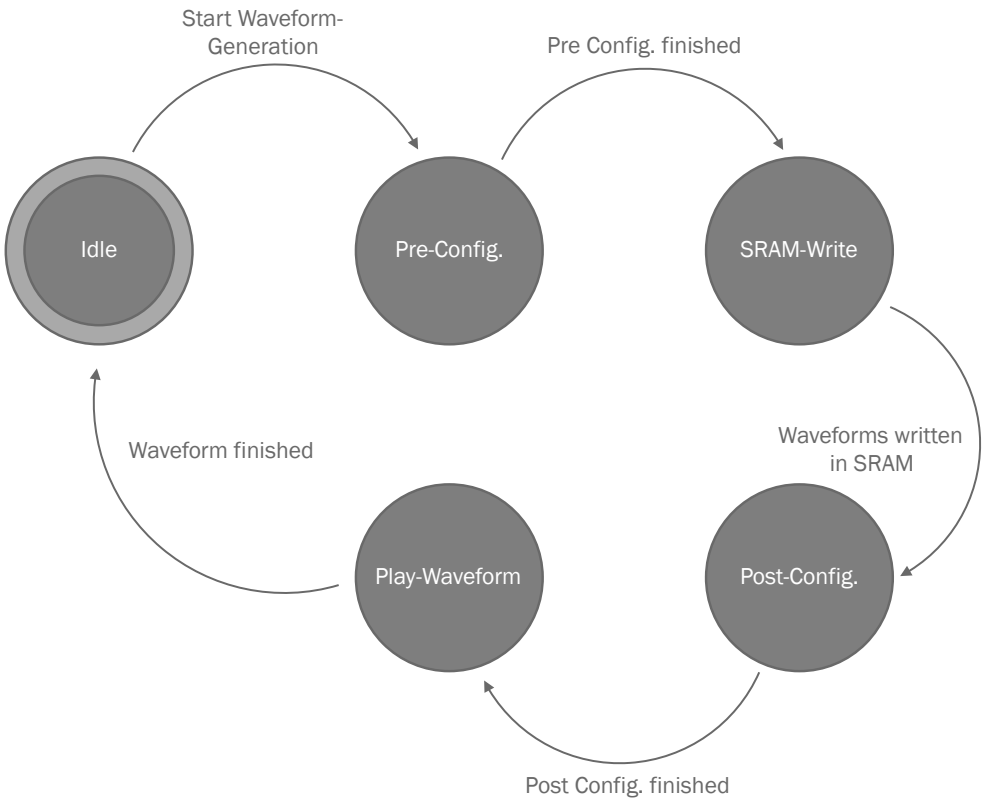


Fig. 5.17: State-diagram of the waveform generation.

5.3.7 Summary

A hardware and software implementation for the digital control loop is developed. The requirements for the individual hardware blocks are derived, depending on the specific application parameters. Components are selected and the respective functionality within the control loop is described. The full signal-path from sensing of the current and voltage slopes ($\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$), for the generation of dynamic reference voltages V_On and V_Off is introduced and interfaces between the hardware devices are described. Together with the analog loop hardware, the result is a full hardware evaluation module, which allows for the operation of the digital control loop, together with the analog control loop. This enables hardware verification of

Tab. 5.7: Requirements for the Output Amplifier and specification of the THS3217 [114].

Parameter	Requirement	Specification
Gain	5 V/V	5 V/V
Slew Rate	1 V/ns	5 V/ns
Input Format	Differential	Differential
Output Format	Single-Ended	Single-Ended

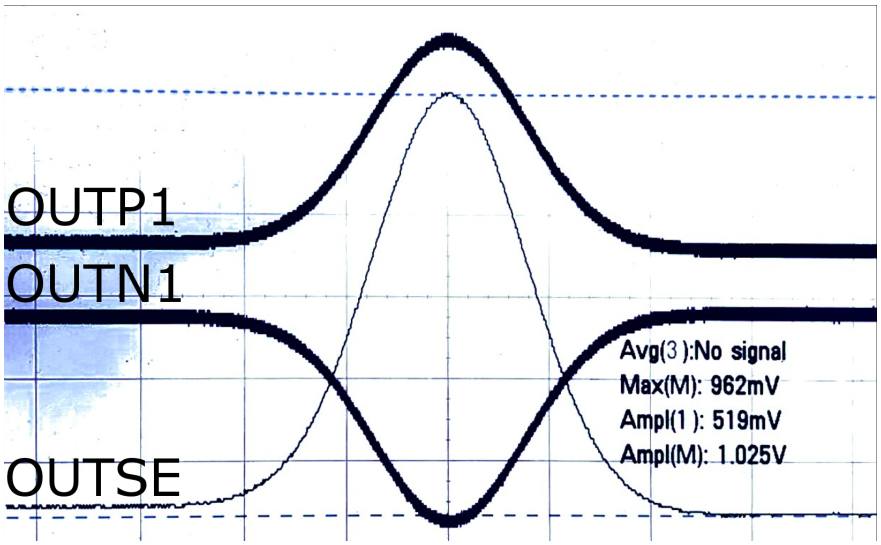


Fig. 5.18: Measured differential and single-ended output format of the DAC.

the full dual-loop concept in arbitrary parameter sets, which will be evaluated in measurements as part of the next section.

5.4 Hardware Verification

5.4.1 Hardware Evaluation Module

As part of this work, the hardware for the analog loop, elaborated in Sect. 5.2, has been built up on PCB as an evaluation board for verification of the dual-loop concept. The analog loop evaluation board, which comprises the full analog loop with $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback and all required interfaces to attach the digital loop, is shown in Fig. 5.19. The components of the digital loop are included into the measurement setup on their corresponding commercial evaluation boards introduced in the previous sections. Table 5.8 gives an overview of the different boards that are part of the evaluation module for the full dual-loop concept.

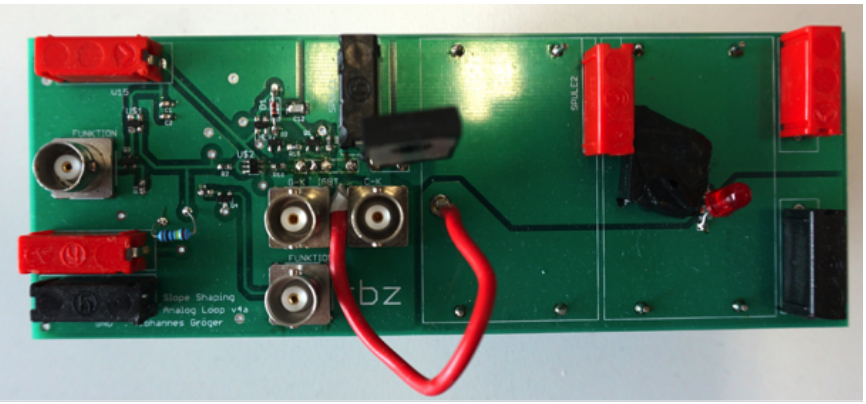


Fig. 5.19: Analog loop evaluation board, including all interfaces for the digital loop.

Tab. 5.8: Overview on the utilized boards as part of the dual-loop evaluation module.

	Hardware Block	Evaluation Board	Picture
Analog Loop		Analog Loop Evaluation Board (own design according to Fig. 5.2)	Fig. 5.19
Digital Loop	ADC	ADC08D1520 Reference Board	Fig. 5.11
	FPGA	Spartan-6 SP601 Evaluation Kit	Fig. 5.12
	Isolation	LTM2895 Evaluation Board DC2589A	
	DAC	AD9106 Evaluation Board	Fig. 5.15

5.4.2 Measurement Setup

The experimental verification of the proposed dual-loop concept is based on the double pulse test (DPT) [115], which is applied to the developed hardware evaluation module. The focus is on the measurement of the current and voltage waveforms and their corresponding switching parameters, such as switching losses of the DUT under inductive load. Therefore, a defined sequence of on- and off-states enables the measurement for the turn-on and the turn-off transition, as shown in Fig. 5.20. During the first on-state, the DUT switch conducts the load current, which ramps up to a predefined value. Next, turn-off occurs and and the predefined current commutates from the DUT to the freewheeling diode. At this instant, the turn-off switching waveforms are measured. In the following off-state, the current stays at its value. Afterwards, turn-on occurs and the predefined current commutates from the freewheeling diode to the DUT. At this point, the turn-on switching waveforms are measured.

As the dynamic turn-on and turn-off switching behavior of the DUT is the major point of interest in this work, the DPT yields a suitable characterization of the switching parameters. Thereby, measurement condi-

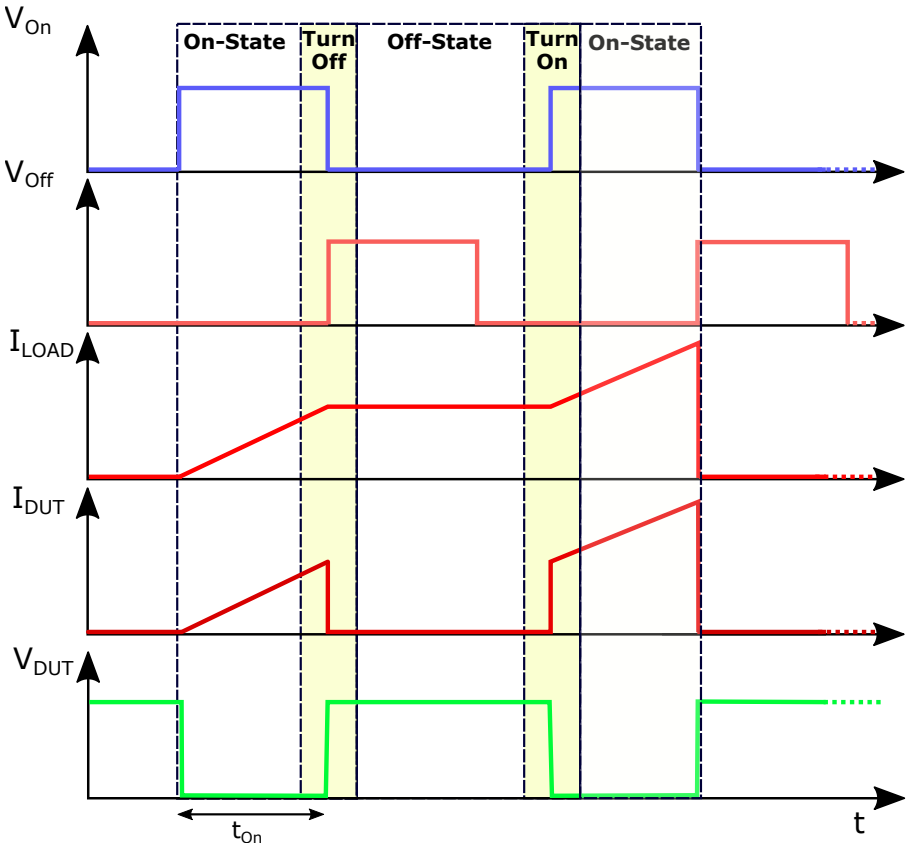


Fig. 5.20: Qualitative waveforms during a double pulse test.

tions are important for the evaluation of different operating points. The two major condition parameters are the DC link Voltage V_{DC}, which can vary from application to application, and the load current I_{Load}, which depends on the DC link voltage, the length of the on state interval t_{On} and the value of the load inductance L_{Load},

$$I_{\mathrm{Load}}(t) = \frac{V_{\mathrm{DC}}}{L_{\mathrm{Load}}} \cdot t_{\mathrm{On}}. \tag{5.10}$$

Using Eq. (5.10), the load current I_{Load} can be controlled by setting the length of the on-pulse t_{On}. This way, the level of I_{Load} is controlled during the DPT by a Matlab script, developed as part of this work. Further parameters, which are important for the experimental verification, are summarized in Table 5.9. The experimental verification of the proposed concept includes an investigation of different power switches. The investigated DUTs are listed in Table 5.10.

Tab. 5.9: Parameter values for the experimental verification.

Parameter	Value	Unit	Power Supply
DC link Voltage	50-389	V	Agilent Technologies AC6801A
Load-Current	5-75	A	-
VCC2	15	V	Agilent E3631A
VSS2	-8	V	Agilent E3631A
Von/Voff	0.6-6	V	Agilent 33522A
$R_{\mathrm{E,On}}/R_{\mathrm{E,Off}}$	10-200	Ω	-
L_{Load}	240	uH	-

Tab. 5.10: Introduction of the investigated power-switches ([116], [90], [118]).

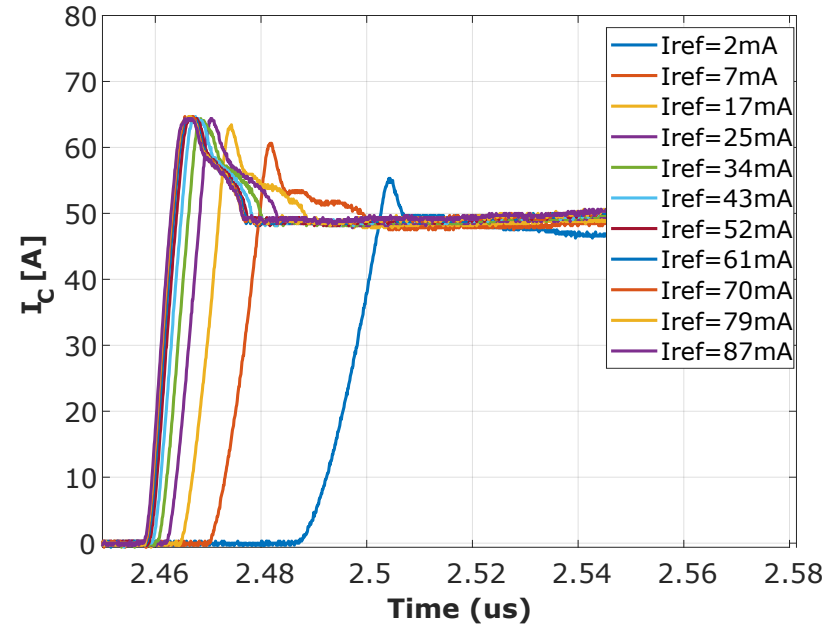
Type	Technology	Company	Name	$V_{\mathrm{CE,max}}$	$I_{\mathrm{C,nom}}$	Package
IGBT	Trench-/Fieldstop	Infineon	IKZ50N65NH5	650V	50A	TO-247 4pin
MOSFET	SJ-MOSFET	Infineon	IPZ65R019C7	700V	75A	TO-247 4pin
SiC	Silicon-Carbide	Cree/Wolfspeed	C3M0030090K	900V	63A	TO-247 4pin

5.4.3 Slew Rate Control Performance

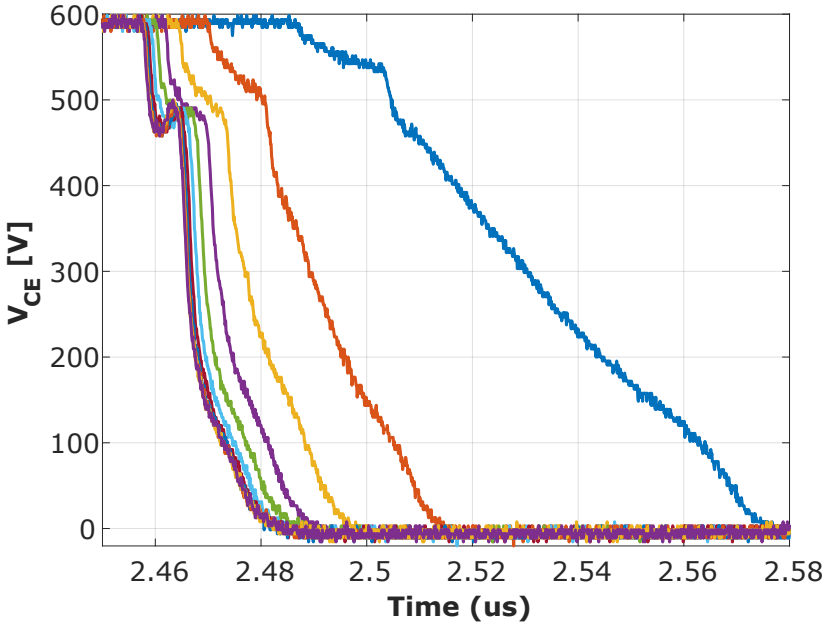
Measurement results of the current and voltage transients are shown in Fig. 5.21 exemplary for a trench-/fieldstop IGBT IKZ50N65NH5 at different injected reference currents I_{ref} into the analog loop. $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ can be controlled effectively using the slope shaping gate driver. The beginning of the voltage transient at turn-on shows limited controllability due to the non-zero parasitic DC bus inductance of the power converter. This is acceptable in practical applications because it does not impact SOA and has negligible effect on EMI for typical current slopes [28] [32].

5.4.4 Comparison with a Passive Gate Driver

In order to demonstrate the benefits of the dual-loop system compared to a passive gate driver (PGD), measurements of the current transients at different load currents at turn-on (Fig. 5.23) and of the voltage transients at different DC link voltages at turn-off (Fig. 5.24) have been performed, with the digital loop settled in steady-state. The 1EDI60N12AF (Infineon), a commercial passive gate driver [44], has been measured as reference according to Fig. 5.22. In the dual-loop system, $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ are linear and



(a)



(b)

Fig. 5.21: Transient waveform of the collector-current I_C and collector-emitter voltage V_{CE} at turn-on for a variation of the reference current I_{ref} in a trench-/fieldstop IGBT (IKZ50N65NH5).

constant over the full range of operating points due to the continous-time regulation of the analog loop, while there are deviations in the conventional driver due to the dependency of $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ on the operating point.

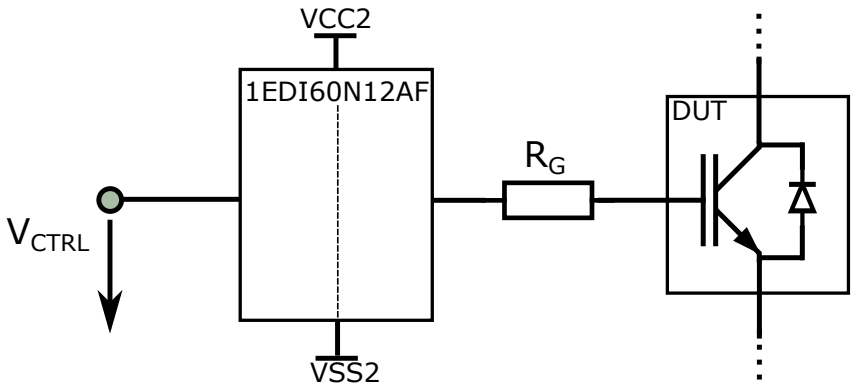


Fig. 5.22: Reference measurement setup using a passive gate driver IC (1EDI60N12AF).

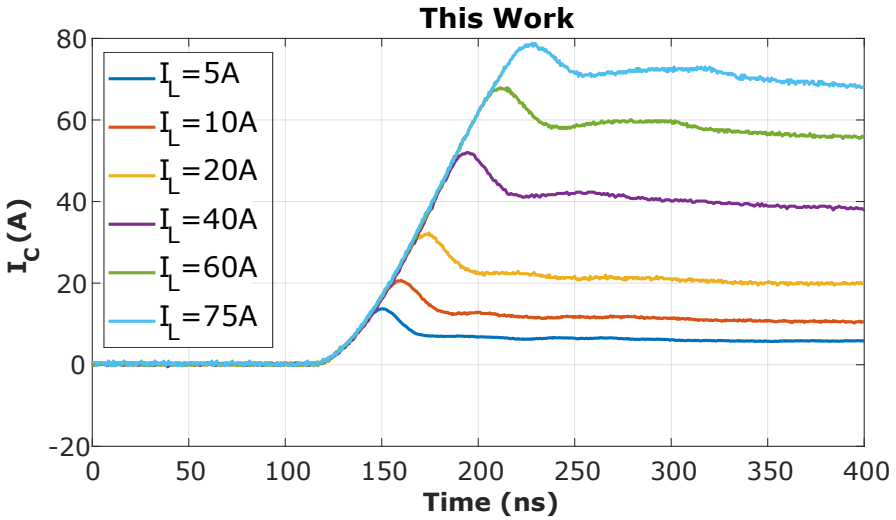
5.4.5 Comparison of Different Power Semiconductor Devices

As one of the essential benefits of the proposed driver, it ensures well-defined control, independent of the actual power devices. In consequence, the driver simplifies the power stage design, as it allows to pick a power device out of a wide range of choices. This is demonstrated in Fig. 5.25, which shows the measured $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ as a function of the reference current I_{ref} for an IGBT (IKZ50N65NH5) and superjunction MOSFET (CoolMOS$^{\mathrm{TM}}$ IPZ65R019C7) of newest generation. For smaller reference currents ($I_{\mathrm{ref}} < 30\mathrm{mA}$), there is a high linearity due to the analog loop. However, at higher references, the curve saturates at different points depending on the individual device parameters. This is due to the limited voltage range in the current summing node.

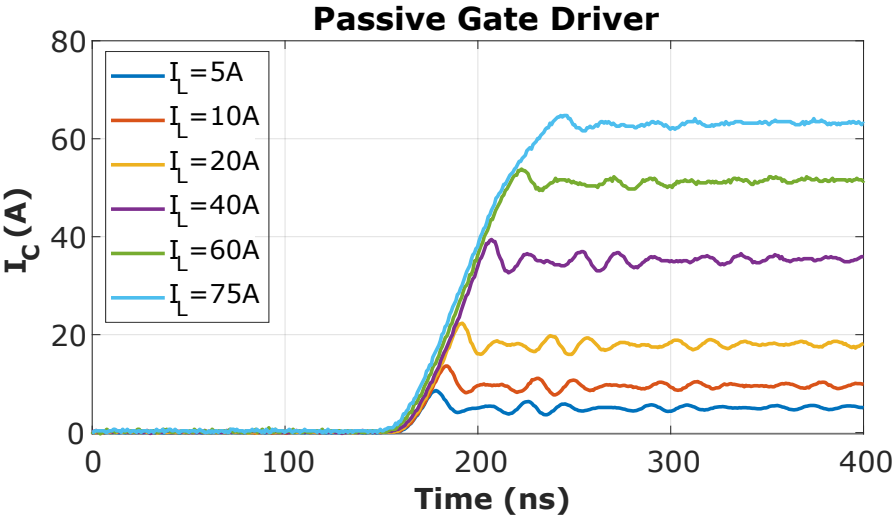
Figure 5.26 shows the adaptive control of the dual-loop over ten switching cycles at a random starting point for CoolMOS$^{\mathrm{TM}}$ C7, trench-/fieldstop IGBT, and SiC. The same analog loop parameters are used for the two different switches and the system shows stable behavior in all operating points. Already after 5 cycles, the error has dropped below 10% and gets close to zero after 10 cycles, demonstrating the precise control of the dual-loop approach for different types of devices.

This experimental verification proves that the technique is attractive for different switch types and power electronics applications. The precise control, which is only possible if the analog loop is combined with an outer digital loop, leads to the following advantages:

1. Modern switches in leading-edge technologies, such as trench-/fieldstop IGBTs, CoolMOS$^{\mathrm{TM}}$ or wide-bandgap devices, can be used in applications with strict requirements on $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and/or $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$



(a)



(b)

Fig. 5.23: Measured switching transients of the collector current I_C for different values of the load-current I_{Load} at turn-on, (a) proposed dual-loop concept and (b) passive gate driver reference. Measurement conditions: V_{DC} = 300V, dI_C/dt=1.0 A/ns, DUT= IGBT IKZ50N65NH5.

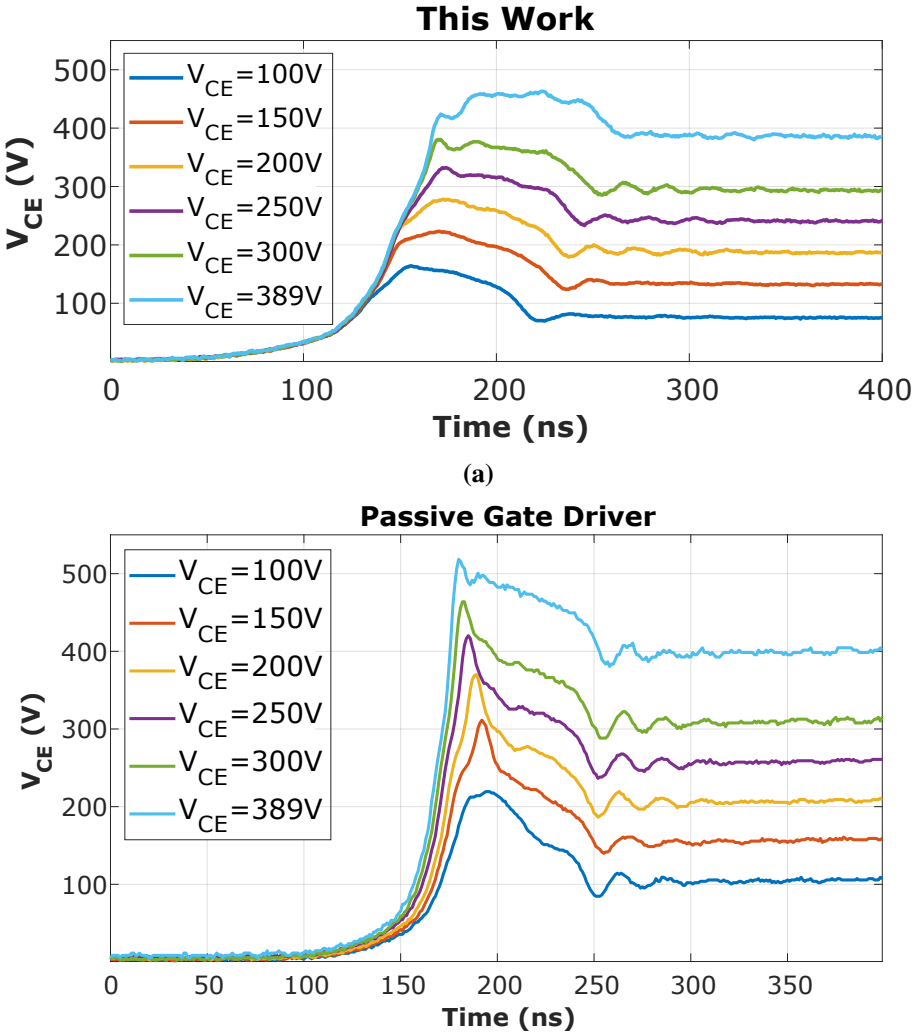


Fig. 5.24: Measured switching transients of the collector-emitter voltage V_{CE} for different values of the DC link voltage V_{DC} at turn-off, (a) proposed dual-loop concept and (b) passive gate driver reference. Measurement conditions: I_{Load}=50A, dV_{CE}/dt=5.0V/ns , DUT= IGBT IKZ50N65NH5.

(for example in motor drives)

2. The number of switches, that can be used for a certain application, increases, as the switching behavior of any device can be optimized to meet the requirements of an arbitrary application (for example a maximum $\mathrm{d}V/\mathrm{d}t$ of a motor drive to avoid destruction of the motor).

3. Especially motor drives applications, with their strict requirements on $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ to protect the bearings, no longer run the risk that they cannot be operated with new power devices. The application becomes independent to the development on the global market of power semiconductor devices.

4. The more accurate control of $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ in motor drives, compared to a pure analog slew rate control loop, opens the field for higher $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ in motor drive applications, because the variations in the slew rate during operation can be assumed as smaller (a design for the worst case is no longer neccessary).

5. $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ can be controlled more accurate with the dual-loop gate driver compared to a pure analog control loop. This yields to a better control of current and voltage peaks, threatening the devices and the electronics, and EMC.

6. A pure digital control loop (without analog loop) might also yield a high accuracy, due to the adaptive principle, but is not able to handle abrupt changes in the operating conditions. As it works cycle-by-cycle, it cannot even react to events and changes that happen between the switching cycles.

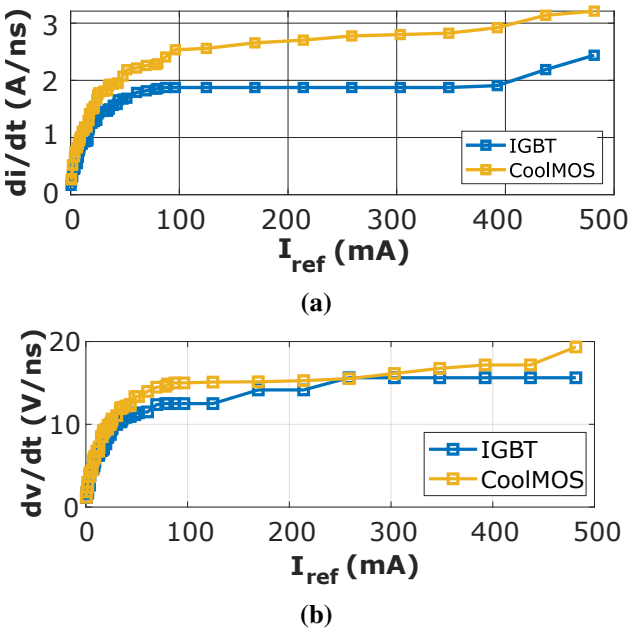


Fig. 5.25: (a) $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ and (b) $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ as a function of the reference current I_{ref} for a new trench-/fieldstop IGBT (blue) and CoolMOS™ C7 (yellow).

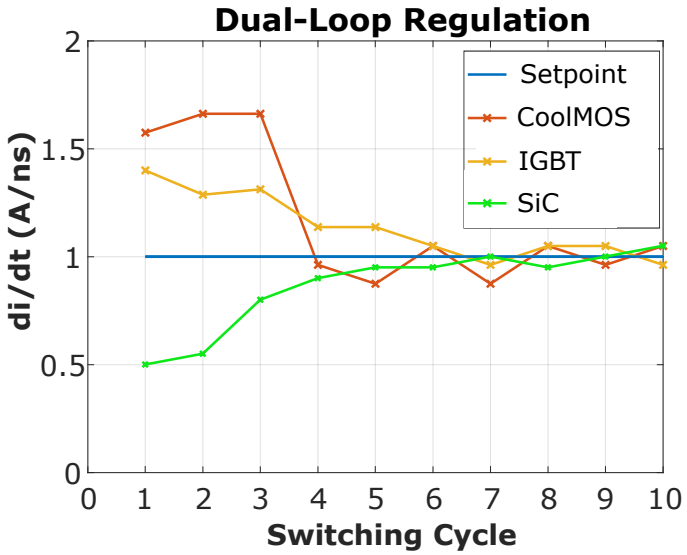


Fig. 5.26: Dual-Loop control of different power semiconductor devices over several switching cycles.

5.4.6 Summary

In this chapter, a closed loop gate-drive concept is presented and evaluated in hardware. Each circuit part is introduced with its respective properties and its resulting discrete hardware component. Furthermore, a hardware evaluation module of the dual-loop concept developed throughout this work is approached and verified. The measurement setup is introduced and the results of the experimental verification were discussed. Additionally, the effectiveness of the dual-loop is verified with different power switches. The proposed concept is capable of adjusting the current and voltage slopes by the variation of the reference current. It is verified that the desired set-point is independent of parameter variations and nonlinearities of the DUT and the load. In a pure analog slew rate control loop, statistical variations lead to different $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ for the same reference current applied. This can lead to a variation of more than 10% over the switching cycles. If the digital loop is added as an outer loop to the analog loop, the statistical variations disappear. The control-range for current and voltage slopes is evaluated for turn-on and turn-off and the respective results are shown in Table 5.11. It is shown that the hardware is able to regulate a wider range of $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ as in the requirement list (Table 3.4), covering even steep slopes up to more than 15 V/ns and 2 A/ns. Hence, the hardware prototype is attractive for a variety of applications.

Tab. 5.11: Control range for voltage and current slopes.

	Turn-On	Turn-Off
$\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$	0.1 - 2.56 A/ns	0.35 - 1.15 A/ns
$\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$	0.42 - 15.14 V/ns	7.6 - 19.5 V/ns

6 Conclusion and Outlook

6.1 Conclusion

An increasing demand for safe and intelligent gate driving is observed due to the upward trend towards fast power switches and wide-bandgap devices (WBG) in numerous applications like motor drives, switched-mode power supplies (SMPS) or power factor correction (PFC) stages. This development is driven by the high volumes of power semiconductor devices, which demand for higher converter efficiencies.

In this work, a dual-loop approach for a slope shaping gate driver has been proposed, which - for the first time - combines the advantages of a closed-loop analog $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ control of a power switch with the ones of a closed-loop digital slew rate control. This gate driving method includes the precision of adaptive control together with the high linearity and robustness of continous-time control in one concept.
The analog loop consists of high-bandwidth analog $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback circuitry based on current signals. It guarantees for linear and regulated $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ transients due to the continous-time control, independent of the actual operating point (DC link voltage and load current). This has been verified by theoretical and experimental work.
The digital loop embraces the analog control loop as a separate outer closed-loop control system, which exhibits digital $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedbacks. It works in a cycle-by-cycle principle. This approach, which adds flexibility for different driving strategies to the control system, has been demonstrated by the implementation of a digital PI-controller.

In contrast to a pure analog loop solution, the digital controller compensates for all kind of statistical variations in the slope shaping system, which are mainly identified in the switching speed of the driven switch and in the parameters of the analog loop. Hence, it enables more precise control. An essential benefit of this multi-domain solution is that the gate driver can be used with an arbitrary unipolar or bipolar gate-controlled power semiconductor device.
Accordingly, the proposed driver is suitable for a variety of power converter applications, especially employing modern devices like trench-/fieldstop IGBTs, CoolMOS$^{\mathrm{TM}}$ or SiC. Any switch type of the required rating can be utilized for instance in industrial motor drives.

Solutions for stable and robust operation of the individual control loops have been provided. This has been done by (1) an analytical stability analysis, based on small-signal models in the Laplace domain created in the framework of this research, and (2) a large signal analysis, which advances the small-signal analysis by investigating remaining non-linearities due to the windup effect. Important control loop parameters, for instance summing node capacitance and gate resistor, have been pointed out. The results of the analyses have been summarized in a list of design requirements, for motor drive applications.

Design concepts for the individual analog system blocks have been proposed for realization in an integrated circuit and in the discrete domain. Furthermore, an evaluation board for the dual-loop system has been built up, which enables the operation in an arbitrary parameter set. Confirmed by system simulations and hardware measurements, the dual-loop concepts exhibits significant improvement as in performance compared to conventional gate drivers.
Accurate linear control has been demonstrated in experiment for steep switching transitions of more than 2 A/ns and 10 V/ns. The digital loop increases the control precision by more than 10%, compared to the use of the analog loop without the digital loop. The control setpoints of $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ are reached in less than 10 switching cycles for three gate-controlled power devices of different technologies (IGBT, CoolMOS$^{\mathrm{TM}}$ and SiC).

The gate driver has been compared to a conventional passive gate driver (Infineon 1EDI60N12AF). The $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ waveforms of the developed concept result show a more linear behavior and no dependency on the operating point. This increases the reliability of the application and the lifetime of the switch. Applications with strong operating point variations, such as motor drives, gain the ability to keep $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ constant during operation, which results in lower average switching losses.

6.2 Outlook

This work focuses on the concept development for a gate driver with precise and device-independent $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ control.

A major limitation in the concept is the sensing of $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ for the digital loop. The measured value of $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ is scaled with the factor of the parasitic emitter lead inductance L_{E}. In Section 3.4, an assumption is made that L_{E} of most common devices can be approximated to $L_{\mathrm{E}} \approx 5$ nH, which has been verified by s-parameter measurements. However, this assumption is only valid for devices in TO-247-4 packages. In different package types, the inductance between the Kelvin and the Emitter pin needs to be re-characterized to ensure reliable $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ sensing. Furthermore, the existing concept is limited to 4-pin power devices and cannot be transfered to 3-pin devices.
An accurate high-bandwidth current sensor, as introduced in [88], could help to solve the challenge of inductance variation and is also transferable to 3-pin devices. Hence, the author recommends to investigate a possible integration of this or a similar sensing concept into the slope shaping system as part of future research.

The dual-loop concept introduced in this work is suitable for integration on an Integrated Circuit (IC), which has been adressed in Chapter 4. This would further accelerate the control behavior of the analog loop and potentially open the concept for new fields like high-speed applications. IC concepts should therefore be adressed in further experimental work.

In this work, the digital loop has been implemented using a standard PI control approach, with focus on verification of the proposed dual-loop concept and to analyze the interaction of the analog and the digital loop. In a future product development, the digital loop is open to be extended by further intelligent monitoring of short circuit events. For instance, one approach that has been filed as a patent as part of this work comprises the detection of overloads by use of time measurements [119]. As $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ and $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ are constant and known due to the dual-loop regulation during the switching event, a time measurement can be utilized to monitor V_{CE} and I_{C}. In case of an overload, a turn-off event is initiated. This conceptual approach can be easily added to the digital circuitry as part of a commercial product development to achieve a robust gate driving scheme.

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List of Abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Converter
ADS	Keysight Advanced Design System
AGD	Active Gate Driver
Balun	Balanced-Unbalanced
BJT	Bipolar Junction Transistor
BNC	BNC (Bayonet Neill–Concelman) connector
CAGR	Compound Annual Growth Rate
CCII	Second-Generation Current Conveyor
CMTI	Common-Mode Transient Immunity
CD	Common-Drain stage
CS	Common-Source stage
CT	Coreless Transformer
DAC	Digital-to-Analog Converter
DDS	Direct Digital Synthesis
DGU	Digital Gate Unit
DMOS	Double Diffused Metal Oxide Semiconductor
DPT	Double Pulse Test
DUT	Device under Test
DSP	Digital Signal Processing
DC	Direct Current
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
EV/HEV	Electric and Hybrid Electric Vehicles
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array

FWD	Free-Wheeling Diode
GaN	Gallium Nitride
GPIO	General-Purpose Input Output
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IGBT	Insulated Gate Bipolar Transistor
IPC	Industrial Power Control
JTAG	Joint Test Action Group
LUT	Look-up Table
LVDS	Low-Voltage Differential Signaling
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MUX	Multiplexer
NMOS	N-Channel Metal Oxide Semiconductor
PC	Personal Computer
PCB	Printed Circuit Board
PFC	Power Factor Correction
PGD	Passive Gate Driver
PI	Proportional-Integral
PMOS	P-Channel Metal Oxide Semiconductor
PWM	Pulse-Width Modulation
RF	Radio Frequency
RHPZ	Right Halfplane Zero
SiC	Silicon Carbide
SMA	SMA (SubMiniature version A) connector
SMD	Surface-mount device
SMPS	Switched-Mode Power Supply
SOA	Safe Operating Area
SOLT	Short-Open-Load-Thru
SPICE	Simulation Program with Integrated Circuit Emphasis
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
STP	Shielded Twisted Pair
UPS	Uninterruptable Power Supply
USB	Universal Serial Bus

VCCS	Voltage Controlled Current Source
VHDL	Very High Speed Integrated Circuit Hardware Description Language
WBG	Wide-Bandgap

List of Symbols

A_{DC}	dB	DC gain class AB amplifier
$C_{buf,in}$	F	INPUT capacitance of the driver/buffer stage
C_C	F	Additional capacitance for Miller compensation in class AB amplifier
C_{CE}	F	Collector-emitter capacitance
C_{fb}	F	Capacitor for generating a feedback current during dV_{CE}/dt
$C_{fb,SR}$	F	Capacitor for generating a feedback current during $dV_{out,drv}/dt$
C_{GC}	F	Gate-collector capacitance
$C_{GC,L}$	F	Gate-collector capacitance approximation valid for $V_{CE}<V_{Ge}$
$C_{GC,S}$	F	Gate-collector capacitance approximation valid for $V_{CE}\geq V_{Ge}$
C_{GE}	F	Gate-emitter capacitance
C_{iss}	F	Input capacitance, output shorted
C_{oss}	F	Output capacitance, input shorted
C_{rss}	F	Reverse transfer capacitance / Miller capacitance
C_{sense}	F	Sensing resistor in the dV_{CE}/dt sensing circuit.
dI_C/dt	A/s	Collector/Drain current time derivative
dV_{CE}/dt	V/s	Collector-emitter/Drain-source voltage time derivative
f_{3dB}	Hz	Maximum frequency for linear dV_{CE}/dt sensing
f_c	Hz	Cutoff frequency class AB amplifier
f_s	Hz	Sample Rate of the ADC
G_{BUF}	V/V	Small-signal transfer function of the driver/buffer stage (Laplace domain)
G_{CAP}	V/A	Small-signal transfer function of the summing node capacitance charging (Laplace domain)
G_{fb}	A/V	Feedback gain (transconductance) of the dI_C/dt feedback circuit
G_I	A/V	Small-signal transfer function of the power switch, with current output (Laplace domain)
G_{IFB}	A/A	Small-signal transfer function of the I_C sensing circuit (Laplace domain)
G_V	V/V	Small-signal transfer function of the power switch, with voltage output (Laplace domain)

G_{VFB}	A/V	Small-signal transfer function of the $\mathrm{d}V_{\mathrm{CE}}/\mathrm{d}t$ sensing circuit (Laplace domain)
g_{m}	A/V	Small-signal transconductance
$g_{\mathrm{m,buf}}$	A/V	Small-signal transconductance of the driver/buffer stage
g_{mR}	A/V	Linearized small signal transconductance by R_{s}
I_{C}	A	Collector current
I_{D}	A	Drain current
I_{G}	A	Gate current
$I_{\mathrm{fb,d}I_{\mathrm{C}}/\mathrm{d}t}$	A	Feedback current during change of I_{C}
$I_{\mathrm{fb,d}V_{\mathrm{CE}}/\mathrm{d}t}$	A	Feedback current during change of V_{CE}
$i_{\mathrm{fb,d}V_{\mathrm{CE}}/\mathrm{d}t}$	A	Small-signal feedback current during change of V_{CE}
$I_{\mathrm{fb,SR}}$	A	Feedback current through $C_{\mathrm{fb,SR}}$ during change of $V_{\mathrm{out,drv}}$
$I_{\mathrm{fb,SRN}}$	A	Amplified feedback current during change of $V_{\mathrm{out,drv}}$
I_{Load}	A	Load current
$I_{\mathrm{out,drv}}$	A	Output current of the gate driver
$I_{\mathrm{q,didt}}$	A	Quiescent current of the $\mathrm{d}I_{\mathrm{C}}/\mathrm{d}t$ feedback circuit during standby
$I_{\mathrm{q,drv}}$	A	Quiescent current of the gate driver during standby
I_{ref}	A	Reference current of the analog control loop
$I_{\mathrm{ref,on}}$	A	Reference current of the analog control loop during turn-on
$I_{\mathrm{ref,off}}$	A	Reference current of the analog control loop during turn-off
$I_{\mathrm{ref,min}}$	A	Minimum Reference current of the analog control loop
$I_{\mathrm{ref,max}}$	A	Maximum Reference current of the analog control loop
I_{reg}	A	Error signal current of the analog loop.
i_{reg}	A	Small-signal error signal current of the analog loop.
$\hat{I}_{\mathrm{rr}}$	A	Peak reverse recovery current
L_{E}	H	Auxiliary inductance between Kelvin and power emitter
L_{G}	H	Gate inductance
L_{S}	H	Stray inductance (sum of parasitic inductances in commutation loop)
L_{Load}	H	Inductive load
Q_{rr}	C	Reverse recovery charge
R_{D}	Ω	Damping resistor for reducing the DC gain of the class AB amplifier
$R_{\mathrm{E,On}}$	Ω	Emitter Resistor in the current source for turn on.
$R_{\mathrm{E,Off}}$	Ω	Emitter Resistor in the current source for turn off.
R_{G}	Ω	Gate resistor
$R_{\mathrm{G,min}}$	Ω	Minimum required gate resistor to prevent oscillations on the gate
R_{N}	Ω	Resistor for operating point setting of MoutN in class AB amplifier

R_P	Ω	Resistor for operating point setting of MoutP in class AB amplifier
R_s	Ω	Source degeneration resistor
R_sense	Ω	Sensing resistor in the $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ sensing circuit.
$t_\mathrm{d,Gc}$	s	Turn-on gate charge delay
$t_\mathrm{d,GC}$	s	Miller capacitance charge delay
$t_\mathrm{d,Gd}$	s	Turn-off gate discharge delay
$t_\mathrm{di,fd}$	s	Duration of the di/dt feedback voltage.
t_On	s	Length of the On State during DPT
t_SW	s	Length of a switching operation
T_j	s	Junction Temperature
V_BE	Ω	Base Emitter Voltage of a Bipolar Transistor.
v_buf	V	Small-signal input voltage of the driver/buffer stage.
V_CC2	V	Positive supply voltage of the analog control circuit (nom: 15 V)
V_CE	V	Collector-emitter voltage
v_ce	V	Small-signal collector-emitter voltage
V_cm	V	Common-mode voltage of the class AB amplifier (nom: 13.35 V)
V_DC	V	DC-link voltage
V_di	V	Output voltage of the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ sensing circuit.
V_DS	V	Drain-source voltage
V_di	V	Output voltage of the $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t$ sensing circuit.
$V_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t}$	V	Feedback voltage induced over L_S during change of I_C
V_GC	V	Gate-collector/Gate-drain voltage of a power switch
V_Ge	V	Gate-emitter/Gate-source voltage of a power switch
$V_\mathrm{Ge,L}$	V	Minimum gate-emitter/gate-source voltage at I_C=I_Load
$V_\mathrm{Ge,th}$	V	Gate-emitter/Gate-source threshold voltage of a power switch
V_GS	V	Gate-source voltage
V_On	V	Control Voltage at Turn On
$V_\mathrm{On,min}$	V	Minimum required control voltage for Turn-On
$V_\mathrm{On,max}$	V	Maximum required control voltage for Turn-On
V_Off	V	Control Voltage for Turn Off
$V_\mathrm{out,drv}$	V	Output voltage of the gate driver
V_OV	V	Overshoot voltage during turn-off
V_SS2	V	Negative supply voltage of the analog control circuit (nom: -15 V)
V_+	V	Positive gate drive voltage
V_-	V	Negative gate drive voltage

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Appendix

A Additional Results

A.1 Additional Results Class AB Source-Follower

Schematic Class AB Source-Follower

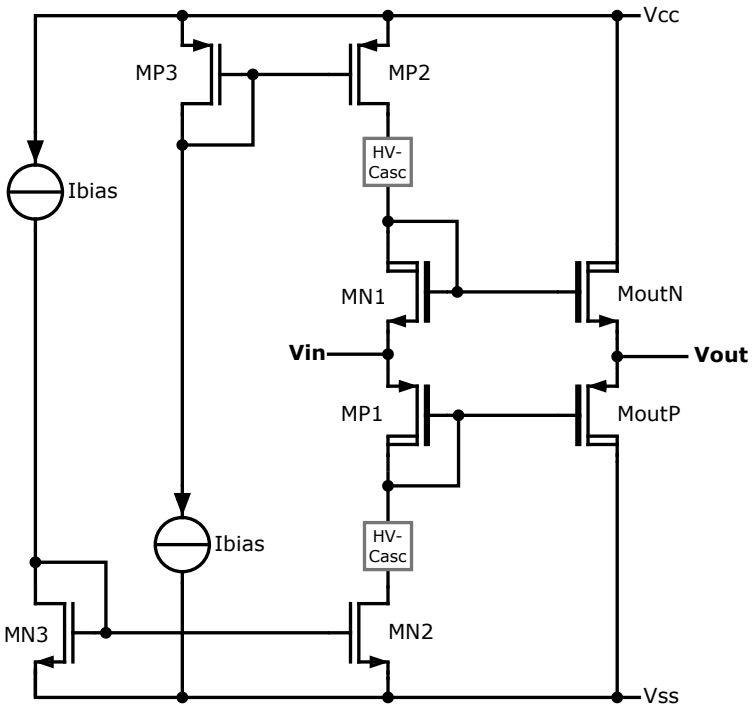

Fig. A.1: Schematic of the class AB source-follower.

Closed-Loop Simulation Results with Source-Follower as Driver Stage

Simulation setup:

- Closed-loop model with parasitics is used: parasitic bond wire inductances ($L_B = 3$ nH) and parasitic bond pad capacitances ($C_B = 20$ fF) of the driver IC's pins, parasitic inductances in the gate path

(trace inductance $L_T = 5$ nH and gate lead inductance $L_{G,lead} = 5$ nH), stray inductance $L_S = 100$ nH in the power circuit and shorted IGBT as freewheeling diode.

- Source-follower from Fig. A.1 is used as driver stage.
- dI_C/dt feedback: ideal voltage controlled current source with $G_{fb} = 20$ mA/V
- dV_{CE}/dt feedback: ideal capacitor with $C_{fb} = 10$ pF
- $I_{ref,on} = I_{ref,off} = 10$ mA
- Gate resistor $R_G = 10\ \Omega$
- $I_{Load} = 20$ A; $V_{DC} = 400$ V (V_{DC} is selected as 2/3 of the rated IGBT voltage)
- IGBT model: IKW50N60T (600 V, 50 A, TRENCHSTOP^{TM} technology) from Infineon

Results:
Fig. A.2 shows the results from the closed-loop simulation with a source-follower as driver stage (with parasitics). The voltage following behavior of the driver output is good and the maximum output voltage is approximately 14 V.
In general the switching slopes are well controlled. The controlled part of the switching slopes exhibits the following rates:

$$dI_C/dt \approx 0.1\ \text{A/ns}$$
$$dV_{CE}/dt \approx 1\ \text{V/ns}$$

However, in the switching slope which occurs first (dI_C/dt in case of turn-on; dV_{CE}/dt in case of turn-off) there is an interval in the beginning where the slope is not controlled, which leads to a nonlinearity. This is mainly due to a wind-up effect of the driver stage which goes into its limitation (either $+14$ V or -14 V) during the pre-charge interval, as there is no active feedback. When the first switching slope starts to rise (active feedback current into the summing node), the driver's output has to settle to the control voltage level. During this settling time a high gate current is flowing which in turn leads to a very steep slope.
In the next section the influence of the source-follower's input capacitance on its output and the settling behavior of the control is investigated.

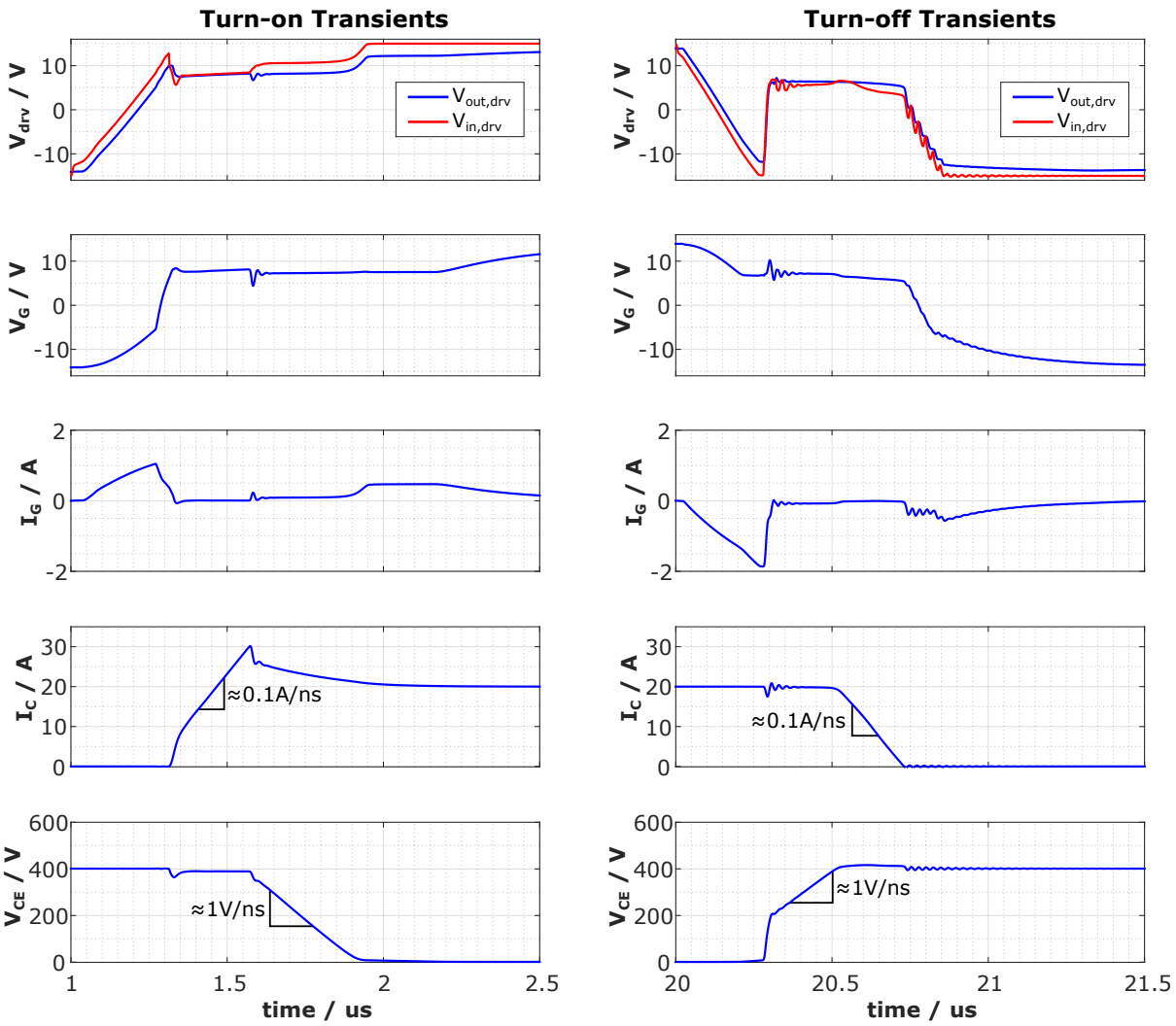

Fig. A.2: Turn-on and turn-off transient signals (V_{CE}, I_C, $V_{in,drv}$, $V_{out,drv}$, V_G, I_G) with source-follower as driver stage.

A.2 Additional Results $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ Feedback

V_in Sweep $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ Feedback

A DC simulation of the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback network (Fig. 4.16) for $V_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t} = V_\mathrm{in} = \pm V_\mathrm{in,max} = \pm 10\,\mathrm{V}$ is performed to check whether the feedback network is working for the whole input voltage range without going into saturation. The design parameters of the differential pair are as follows $R_\mathrm{b,Mon} = R_\mathrm{b,Moff} = 46\,\mathrm{k\Omega}$ (AB operation), $R_\mathrm{s,Mon} = R_\mathrm{s,Moff} = 700\,\Omega$ and Mon,Moff with $\mathrm{W/L} = 90$. The results can be seen in Fig. A.3.

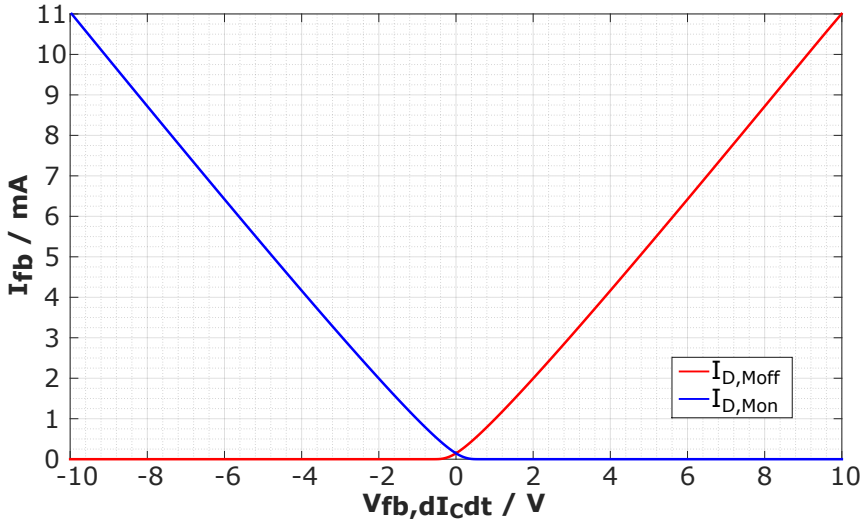

Fig. A.3: Feedback currents of Mon and Moff for a DC sweep of $V_{\mathrm{fb},\mathrm{d}I_\mathrm{C}/\mathrm{d}t} = V_\mathrm{in}$ ($V_\mathrm{in} = -V_\mathrm{in,max} \ldots + V_\mathrm{in,max} = -10\,\mathrm{V} \ldots + 10\,\mathrm{V}$).

Concept $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ Feedback for Class A Operation

Figure A.4 show a proposal for the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback network where both gates of the differential pair are referred to the fixed potential of the Kelvin emitter (e). The operating point for Mon and Moff is set very high (class A), that the static current through Mon and Moff is approximately half of the maximum desired feedback current. In this case only Mon is actively triggered during the collector current transients and the current through Mon is either increased (IGBT turn-on) or decreased (IGBT turn-off). The difference between the current through Mon (i_Mon) and the constant current through Moff ($i_\mathrm{bias,Moff}$) is then the actual feedback current on the output of the $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback.

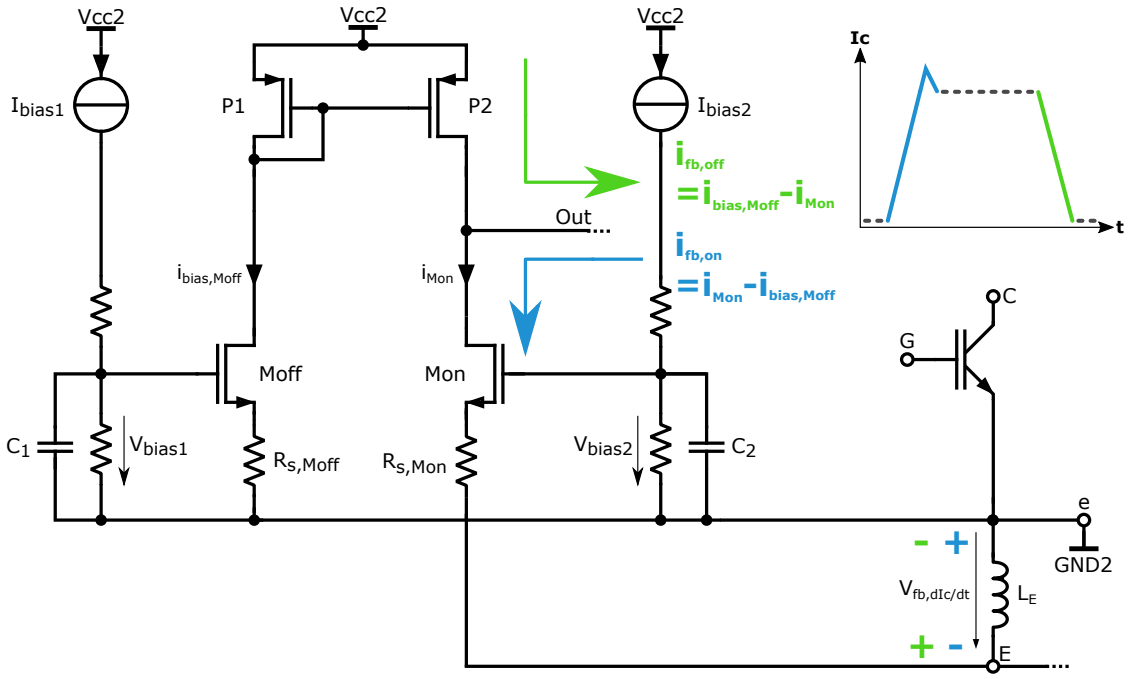

Fig. A.4: Proposal for $\mathrm{d}I_\mathrm{C}/\mathrm{d}t$ feedback network, where the operating point of Moff and Mon is class A and only Mon is actively triggered during the collector current transients.

A.3 Additional Results System Simulation

IGBT Operating Point Compensation: Varying Load Currents

The closed-loop control is simulated with the simulation setup from Section 4.4 and varying load currents from 10 A to 50 A. The results for turn-on and turn-off are illustrated in Fig. A.5. The closed-loop control shows a good compensation behavior for different operating points of the IGBT, as the rates of the controlled switching slopes stay at constant values ($\mathrm{d}I_\mathrm{C}/\mathrm{d}t \approx 0.2\ \mathrm{A/ns}$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t \approx 1\ \mathrm{V/ns}$).

IGBT Operating Point Compensation: Varying DC Voltages

The closed-loop control is simulated with the simulation setup from Section 4.4 and and varying DC voltages from 200 V to 600 V. Figure A.6 shows the results for turn-on and turn-off. The closed-loop control exhibits a good compensation behavior for different operating points of the IGBT, as the rates of the controlled switching slopes stay at constant values ($\mathrm{d}I_\mathrm{C}/\mathrm{d}t \approx 0.2\ \mathrm{A/ns}$ and $\mathrm{d}V_\mathrm{CE}/\mathrm{d}t \approx 1\ \mathrm{V/ns}$).

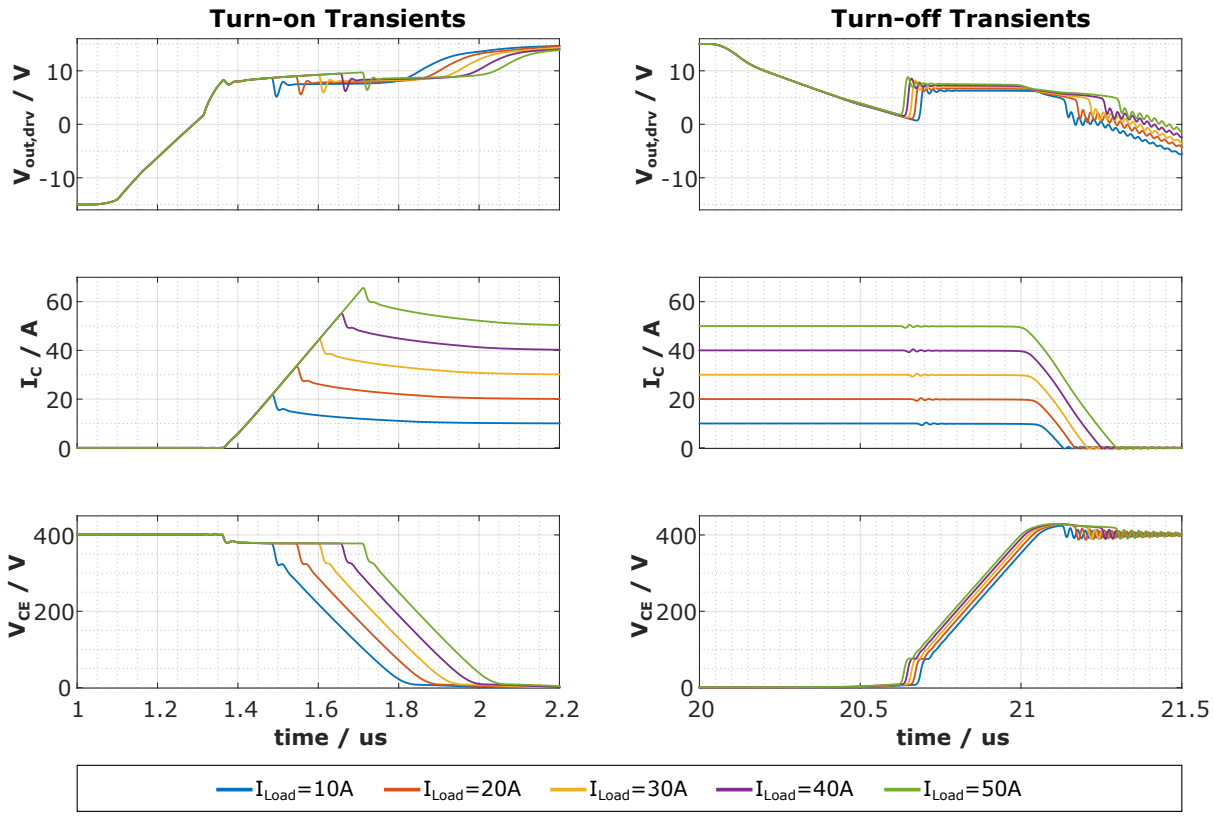

Fig. A.5: Simulation of the closed-loop gate driver for varying load currents from 10 A to 50 A.

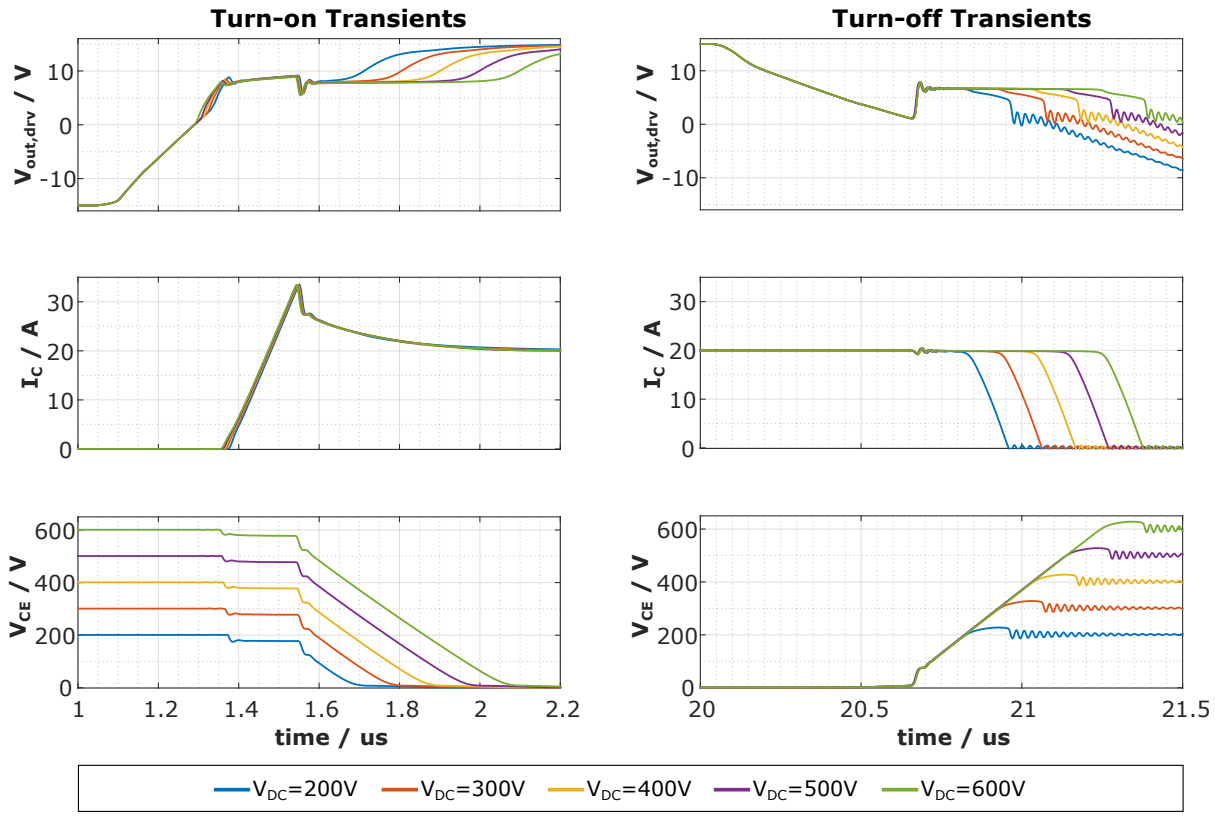

Fig. A.6: Simulation of the closed-loop gate driver for varying DC voltages from 200 V to 600 V.

B SPI Interface

The serial peripheral interface (SPI) interface enables the communication between field programmable gate array (FPGA) and digital-to-analog converter (DAC), and is responsible for the transmission of the configuration and waveform data. It has been implemented on the FPGA in Very High Speed Integrated Circuit Hardware Description Language (VHDL).
The requirements for the SPI protocol are determined by the interfaced slave, which is represented by the DAC. The 32-bit transmission word is subdivided in two basic areas, as indicated in Fig. B.7. The first bit characterizes the following command as read or write (R/W). The next 15 control bits (CB15-CB1) represent the command cycle, consisting of the address of the register to be configured. The last 16 data bits (DB16-DB1) define the data cycle. A 16-bit data word represents the value which is written to the register address defined in the command cycle. The AD9106 offers 128 configuration registers that enable a variety of adjustments of the DAC. An extract of the most important registers, utilized in this work, are shown in Table B.1. Hence, it is possible to adjust the gain of each DAC output channel independently (registers 1 and 2). Further, it can be determined from where the waveform-data is drawn with the options direct digital synthesis (DDS) or static random-access memory (SRAM).

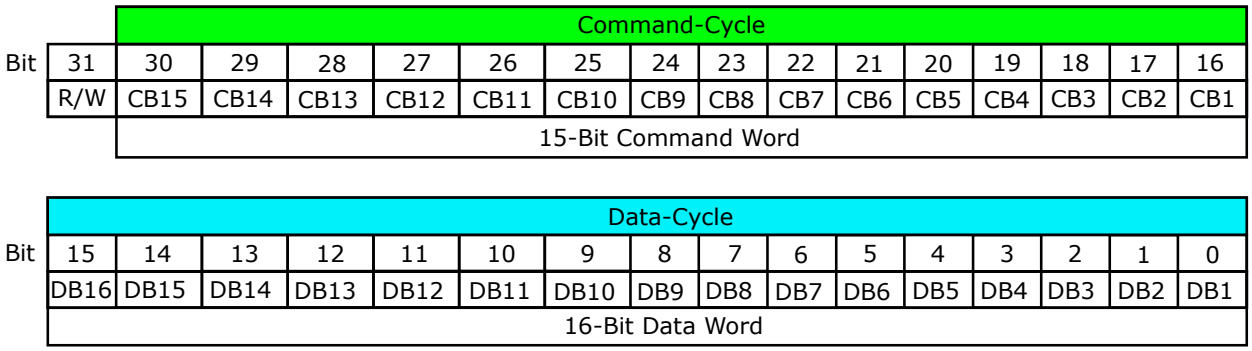

Fig. B.7: 32-Bit SPI transmission word with command and data cycle [120].

Tab. B.1: Extract of the most important configuration Registers [120].

Nr	Register Address	Register Name	Description
1	*X*"0007"	DAC1 Analog Gain	Analog Gain of DAC1
2	*X*"0006"	DAC2 Analog Gain	Analog Gain of DAC2
3	*X*"0027"	WAV2-1CONFIG	Data from DDS or SRAM
4	*X*"005*d*"	START-ADDR1	SRAM Start Address for DAC1
5	*X*"005*e*	STOP-ADDR1	SRAM Stop Address for DAC1
6	*X*"0059"	START-ADDR2	SRAM Start Address for DAC2
7	*X*"005*a*"	STOP-ADDR2	SRAM Stop Address for DAC2
8	*X*"001*e*"	PATSTATUS	SRAM Write Active

List of Publications, Patents, Presentations

Conference Papers

- N. P. Aryan, J. Groeger, and A. Rothermel, “Passive amplification of supply voltage in an implantable chip,” in *PRIME 2012; 8th Conference on Ph.D. Research in Microelectronics and Electronics*, June 2012, pp. 1–4.
- J. Groeger, A. Schindler, B. Wicht, and K. Norling, “Optimized dv/dt, di/dt sensing for a digitally controlled slope shaping gate driver,” in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 3564–3569, **(Outstanding Presentation Award)**.
- J. Groeger, B. Wicht, and K. Norling, “Dynamic stability of a closed-loop gate driver enabling digitally controlled slope shaping,” in *2017 13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, June 2017, pp. 61–64, **(Silver Leaf Award)**.
- A. Schindler, B. Koeppl, B. Wicht, and J. Groeger, “10ns Variable current gate driver with control loop for optimized gate current timing and level control for in-transition slope shaping,” in 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), 2017, pp. 3570–3575.
- T. Funk, J. Groeger, and B. Wicht “An Integrated and Galvanically Isolated DC-to-15.3 MHz Hybrid Current Sensor,” in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, 1010-1013.

Patents

- "Method of over current and over voltage protection of a power switch in combination with regulated di/dt and dv/dt," filed on September 7, 2017, U.S. Patent Application.
- "System and method of driving a power switch in combination with regulated di/dt and/or dv/dt," filed on June 18, 2018, U.S. Patent Application.

Workshops and Presentations

- "Use Case of AMS Designer & Simulink Co-Simulation," *MASC Workshop: Knowledge Exchange on Behavioral Modeling and Simulation*, November 29, 2016, Infineon Technologies Behavioral Modeling Community, Infineon Technologies AG, Neubiberg.
- "A Closed-Loop Gate Driver with Digitally Controlled Slope Shaping," Invited Presentation, September 8, 2017, Infineon Technologies Austria AG, Villach, Austria.
- "A Closed-Loop Gate Driver with Analog and Digitally Controlled Slope Shaping," IPC Colloquium (Invited Presentation), September 24, 2018, Infineon Technologies AG, Neubiberg.
- "A Closed-Loop Gate Driver with Analog and Digitally Controlled Slope Shaping," Invited Presentation, February 8, 2019, Infineon Technologies Austria AG, Villach, Austria.

Awards

- Outstanding Presentation Award, *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa/FL, USA, March 30, 2017.
- Silver Leaf Award, *2017 13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Taormina, Italy, June 15, 2017.

List of Student Theses Supervised by the Author

Ann-Christin Koellner: Analog-to-Digital Converters for Digital Slope Shaping in Gate Drivers for Various Power Transistors, Research Paper, University of Stuttgart, 2016

Alexander Schreiber: Design of an Integrated High-Voltage Gate Driver with Analog Slope Control, Master's Thesis, Reutlingen University, 2017

Benjamin Richter: Hardware Evaluation of Gate Driver Concepts with Digital and Analog Slope Shaping for Industrial Applications, Master's Thesis, Reutlingen University, 2018

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