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Electrostatic Self-Assembly Technique for Parallel Precision Alignment of Optical Devices

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Abstract

In precision assembly, the cost of machine technology increases significantly when high assembly accuracy is required (<15 µm). One reason is that higher accuracy with conventional automation technology requires much more precise and expensive machine components, such as bearings and actuators. Electrostatic self-assembly is a technique for the automatic alignment of micro-components without the need for precise machines and thus has the potential to reduce fabrication costs significantly. With this technique, electrodes are placed on the micro-components and the substrate. A low viscosity fluid is applied to the substrate and the components are roughly positioned. One pair of electrodes on the component faces one pair of electrodes on the substrate, equivalent to plate capacitors connected in series. If an alternating voltage is applied to the substrate electrodes, an electric field is formed. This results in electrostatic attraction in the transversal and lateral direction, which leads to an alignment of the components on the substrate. In this paper, we describe the structure design process for electrostatic self-assembly. Instead of micro-components, we use a rectangular glass wafer with a length of 125 mm. Within two test series, we prove that the existing technique is also suitable for a larger scale.

Keywords

Precision Alignment; Self-Assembly; Parallel Assembly

1. Introduction

Optical systems, in combination with electronic circuits, are becoming increasingly important. Growth markets are camera technology for smartphones and autonomous driving or sensors for consumer electronics. More than twenty percent of US citizens are currently using wearables, mostly with integrated optical heart rate sensors for health monitoring [1]. This is just one example of a rapidly spreading technology in recent years, and several research groups are currently working on the development of new optical systems in the fields of sensor technology, signal processing and health care [2–4]. Efficient production technology is important for further mainstreaming these new technologies. The production of semiconductor materials and silicon are incompatible with the manufacturing processes of many optical devices. For example, the 3D shape of almost all lenses conflicts with the pure surface technology of the LIGA process. For this reason, separate processes are necessary for assembly and connection [5].

Sequential assembly and positioning in the micrometre range with the aid of positioning devices is very time-consuming and the machine technology expensive [6]. For this reason, several years ago, research groups researched parallel assembly of micro parts without direct handling and published under the term

electrostatic self-assembly. Primarily, fluidic and electrostatic driven mechanics were in the focus of the experimental research for microelectromechanical systems (MEMS) [6] and DALIN et al. build a simulation, based on experimental data [7,8]. Within the Cluster of Excellence PhoenixD, the Institute of Assembly Technology develops handling processes for optical devices and micro parts. Within a new approach, we adapt the electrostatic self-assembly concept for aligning whole pre-processed wafers instead of the single handling of small parts like MEMS or chips. Due to the novelty of this approach, the focus of this paper is to present the concept for the full-wafer alignment, the development of a structure design and to prove the suitability of the process for a different scale.

2. Concept of electrostatic Self-Assembly

The term self-assembly is mainly used in chemistry, e.g. when nanoparticles selectively localize within a particular microdomain, to form patterns or nano-structured coatings on a surface [9,10]. In the engineering or production context, self-assembly is a method to align components without direct handling. In this paper, we address electrostatic self-assembly as a system consisting of a substrate (bottom wafer) and a component (top wafer) separated by a fluid. This fluid serves several functions: it reduces friction and thus enables movement in the lateral direction. In addition, it acts as a dielectric for the electric field [6]. On both wafers, conductive structures are deposited. These structures consist of conductive tracks and surfaces called pads. Two facing pads form a plate capacitor [8,11]. If a pad is electrically polarised, e.g. negatively charged, an opposite charge is attracted to the facing pad due to the Coulomb force. This leads to a locally induced charge shift on the secondary conductive structure. This means the transfer of electric potential between the pads is capacitive and therefore only one side needs a galvanic connection to the power supply. Due to the design of the plate capacitor, an electrostatic attraction takes place between the pads. As a result, forces act in the lateral and transverse directions. The component starts to moves within an electric potential field towards the energetically most favourable state (Figure 1). We artificially create the electrostatic field and define the position with the lowest potential as the assembly position with the structure design [12,13]. Once the assembly position is reached, the component is trapped within an equilibrium of the interacting forces.

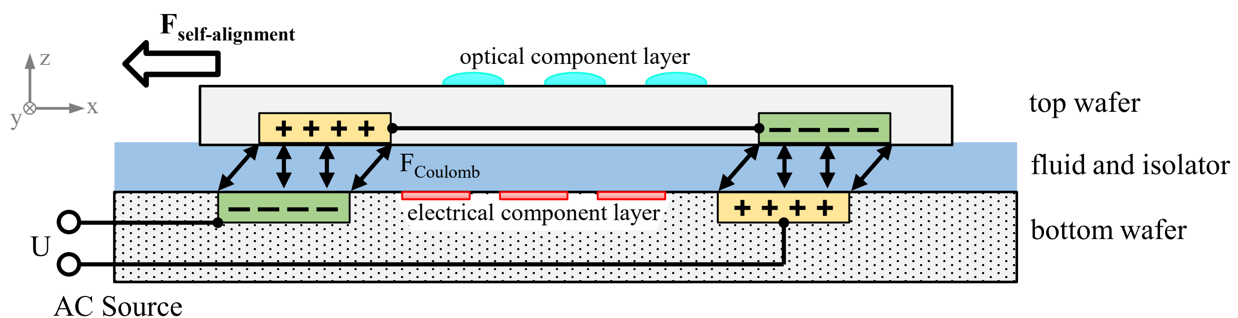

Figure 1: Concept for self-assembly of parts with electrostatic attraction

3. Full-wafer approach and structure design

Electrical components, such as CMOS sensors, are manufactured on wafers with a high degree of precision. A similar process is possible for optical components on glass wafers. Instead of assembling these electrical and optical components individually with a high-precision pick-and-place process, it is more economical to perform parallel alignment and bonding. The possibility of aligning small chips with electrostatic self-assembly has already been demonstrated [8]. Nevertheless, the parallel assembly of already diced microsystems still requires a sequential pre-positioning of the individual parts. To bypass this time-consuming placing process, this article took a novel approach to achieve the alignment of an entire wafer.

Figure 2 shows the concept of this approach. In the centre of the wafer, functional component layers can be applied using standardized micro-processing techniques. Electrically conductive structures are deposited outside or between the components for the alignment process. When aligning the upper wafer via electrostatic self-assembly, the two component layers are precisely positioned on top of each other. Then the two wafers are bonded together over their entire surface. In the following cutting process, the two bonded wafers can be separated into individual modules and used for further applications.

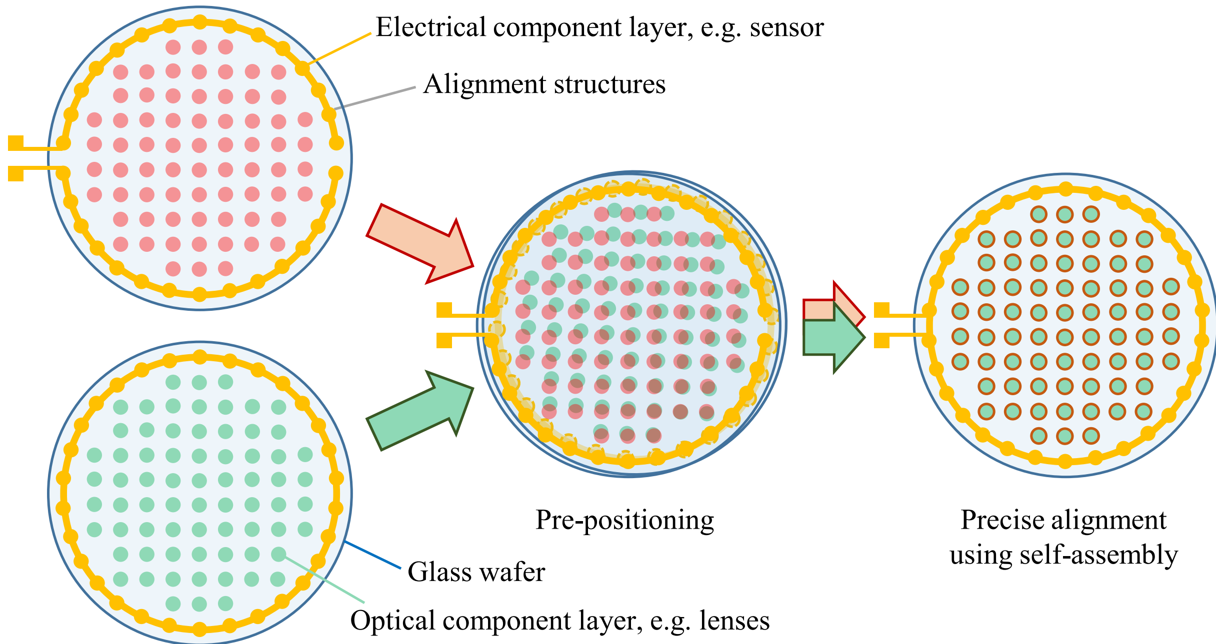

Figure 2: Novel approach for full-wafer alignment via self-assembly

3.1 Systematic structure design

The first step in building a self-assembly system is the structure design. This involves determining the geometry and arrangement of the conductive structures. Although the individual sub-steps have already been applied several times [7,8,11,6], a systematic process description has not been established yet. For this reason, we present a systemic development process. This process includes three steps, which are illustrated in Figure 3:

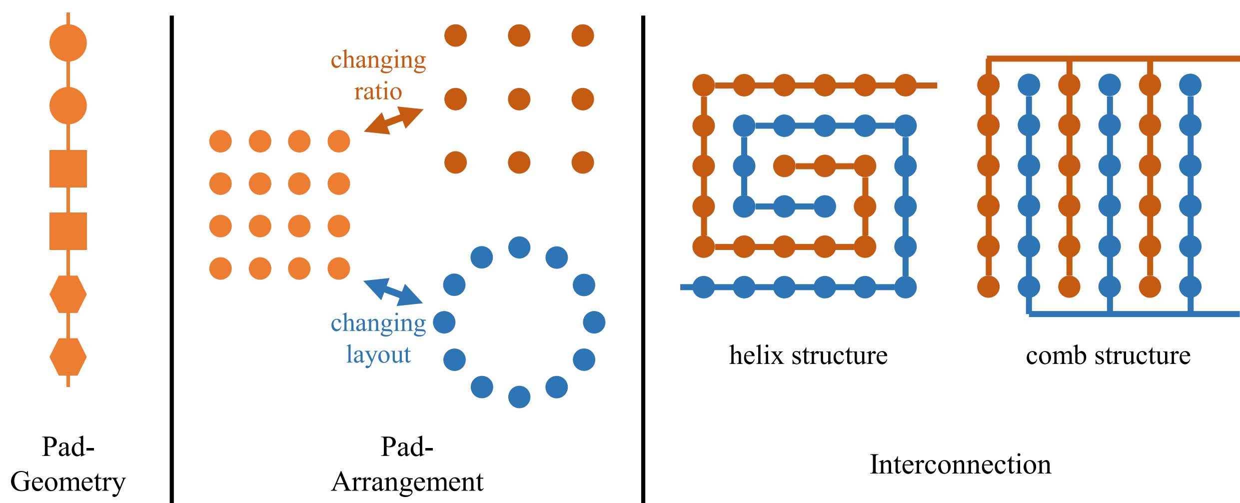

Figure 3: The three steps of structure design

Pad-Geometry:
Pad geometry describes the geometric shapes of the individual opposing active surfaces. These surfaces were build up as squares, rectangles, circles or hexagons [14,11]. In principle, however, any geometry is possible.

Pad-Arrangement:
Pad arrangements are about the spatial positioning of the individual pads on the surface. In previous work, the only arrangement found is in a square [6]. The square shape is derived from the geometry of silicon chips. In addition, in the arrangement step, the pad distance and pad size are defined. These parameters are relevant because two closed by pads can influence each other's electric field. TONDORF and WILDE [6] have taken the ratio of these two values as the decisive parameter.

Interconnection:
Even if the arrangement is already fixed, the pads can be connected in different ways. For electrostatic self-assembly, at least two adjacent pads must have different potentials in at least one direction. For example, in a square arrangement, parallel comb structures or helix structures are possible [6].

3.2 Structure design for full-wafer alignment

Our novel approach for full wafer alignment requires a significant adaptation of the structure design used for the alignment of micro parts. Firstly, due to the significantly larger surface area, the geometry of the structures must be resized to ensure that there is enough active surface to achieve an alignment. Secondly, wafers are round due to the production process, and therefore, the arrangement of individual pads must also be changed to create the maximum possible usable area for the application. We chose a rectangular pad geometry for the experiments (1 x 5 mm²) and arranged 76 pads in a circle with a diameter of 105 mm to leave space in the centre for electrical and optical components in the planned application. The pad distance is on average 3 mm (ratio 1:3) and was specified based on [6]. The pads are connected alternately. In this way, two adjacent pads always have a different electrical potential. We positioned measurement structures in the centre of the wafer. Conductive tracks link the pads on the top wafer. Figure 4 shows the developed structure design.

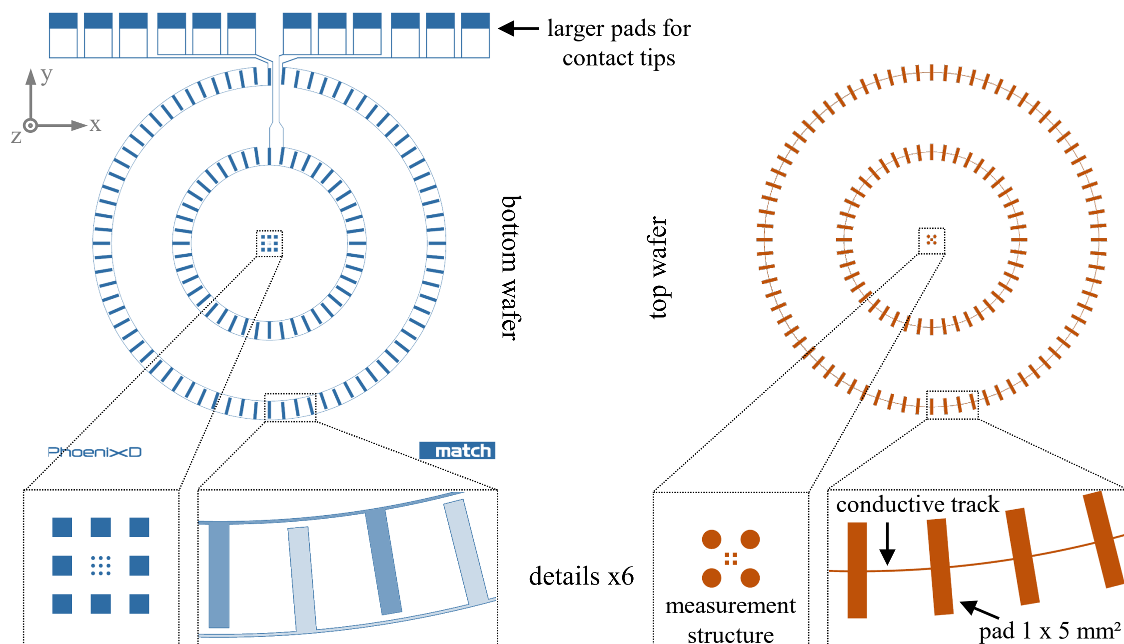

Figure 4: Structure design for full-wafer alignment

The conductive structures were deposited on rectangular exposure masks. The bottom wafer has an edge length of 15.25 cm (~6 inches). The top wafer has an edge length of 12.7 cm (~5 inches) and a thickness of 560 µm. The material in both cases is soda-lime glass with a chromium layer of 0.1 µm, with a thin oxide layer on the surface. On the top side of the bottom wafer, there are large rectangular areas for galvanic contact with contact tips. There is a second circular arrangement of pads with a smaller diameter, but they are not used in the experiments.

4. Experimental setup

We build the experimental setup on a damping plate to reduce mechanical vibrations that would affect the measurement. The bottom wafer lies on a backlight and is illuminated from below. A camera (IDS 3880 CP-6.4 MP) with a 4x telecentric zoom lens and additional coaxial illumination is mounted in the middle above the measurement structures. We can observe the relative position via a monitor in situ. A confocal distance sensor (microEpsilon IFS2405-3) measures the relative distance of the surface below. Two contact tips connect the structures on the bottom wafer to the voltage source. A function generator (GW-Insteck ASR 2050) directly supplies the voltage up to 350 VAC. For higher voltages, a transformer is interposed.

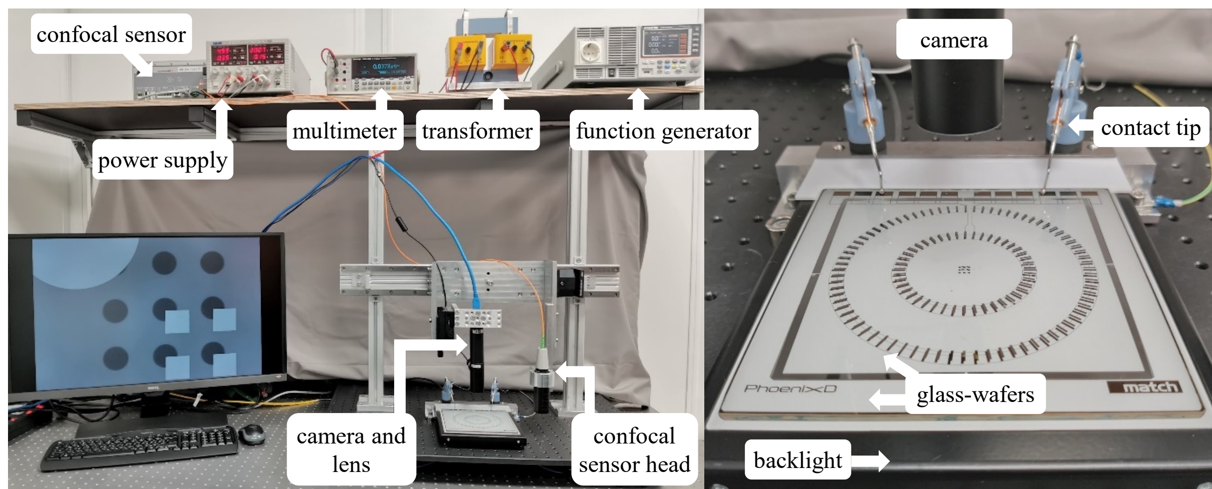

Figure 5: Experimental setup: overview (left) – detail (right)

4.1 Experimental procedure

Two larger test series were carried out for this paper. The first series deals with the influence of voltage, the second with the frequency of the alternating current.

First, the fluid is applied between the substrate and the component. In our experiments, we use the acrylic-based UV adhesive Sicuwell 7043-N, which can be activated by UV light. The curing process is not part of our test. The thickness of the adhesive layer varies between 70 µm and 100 µm in the experiments. Manual pre-positioning takes place before the electrostatic alignment. The initial positioning error is between 450 µm and 700 µm in x- and y-direction. After activating the voltage, the movement of the top wafer starts without any measurable delay. When the component has reached the final position, the voltage is deactivated. The camera documents the movement during the entire alignment process focusing on the measuring structure in the centre of the wafer alignment, the top wafer is pre-positioned again, and the tests are repeated 10 times per parameter set. The camera images allow measurement of the top wafer's relative position during the entire process.

Combined, the camera with the telecentric lens system has a resolution of 0.6 µm/px, which was confirmed by a separate measurement. The evaluation is done automatically via the measurement structures using the Open Source Computer Vision Library (OpenCV). Within OpenCV, we used algorithms for greyscale

analysis to detect the structures and enhance the measuring system's overall resolution by using sub-pixel interpolation and mean values.

4.2 Evaluation criteria for the process

The assessment of the results can be done based on several criteria. The first criterion is the success rate of the positioning. The success rate quantifies the rate of a successful alignment, independent of the achieved accuracy. The most important criterion for our research is the absolute positioning error d. It is defined as the absolute distance between the target position and the achieved alignment position. It is calculated as the vector length of the positioning errors in x-direction e_x and y-direction e_y.

5. Results and Discussion

In both test series – voltage and frequency – we evaluate the effect of the input parameter on the positioning error. Figure 6 shows a typical measurement curve. Placed in the diagram are the position error e_x and e_y, the length of the resulting vector d (absolute position error) and the velocity v in µm/s, as median over 10 values.

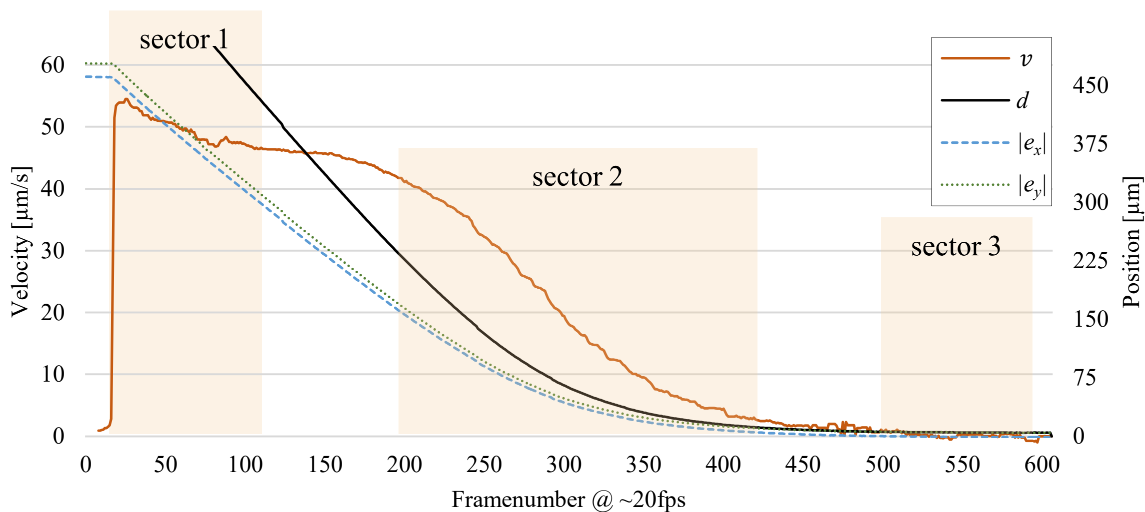

Figure 6: Diagram of the positioning errors e_x, e_y, d and the velocity v

We classified the measurement into several sectors:

Sector 1 (start): at the beginning, the voltage is activated, and the velocity increases rapidly. The movement in x and y is almost linear, which corresponds to an almost constant velocity.

Sector 2 (middle): as the top wafer approaches the assembly position, the velocity reduces. The position ascends asymptotically to the final value.

Sector 3 (end): at the end of the measurement, there is no measurable motion. The measured values only fluctuate within the range of measurement accuracy. At this point, the position error is calculated as an average of 10 measured values.

This observation fits into the theoretical model developed by DALIN et al. [14,7,8]. There is only a small overlap of the pads initially, but the pads are still in the electric field range. During the alignment, the overlap of the pads increases. According to the model by DALIN et al., the lateral alignment force decreases with the overlap, i.e. the force decreases during the alignment. At the assembly position, the overlap is 100%, and the force becomes zero. This description corresponds with the measurement curve. The velocity decreases within the process, and movement stops when the assembly passion is reached.

5.1 Influence of the voltage level

The first series of experiments investigates the influence of the voltage level between 250 VAC and 1250 VAC (sine wave, 50 Hz). Figure 7 shows the correlation between the positioning error and the applied voltage.

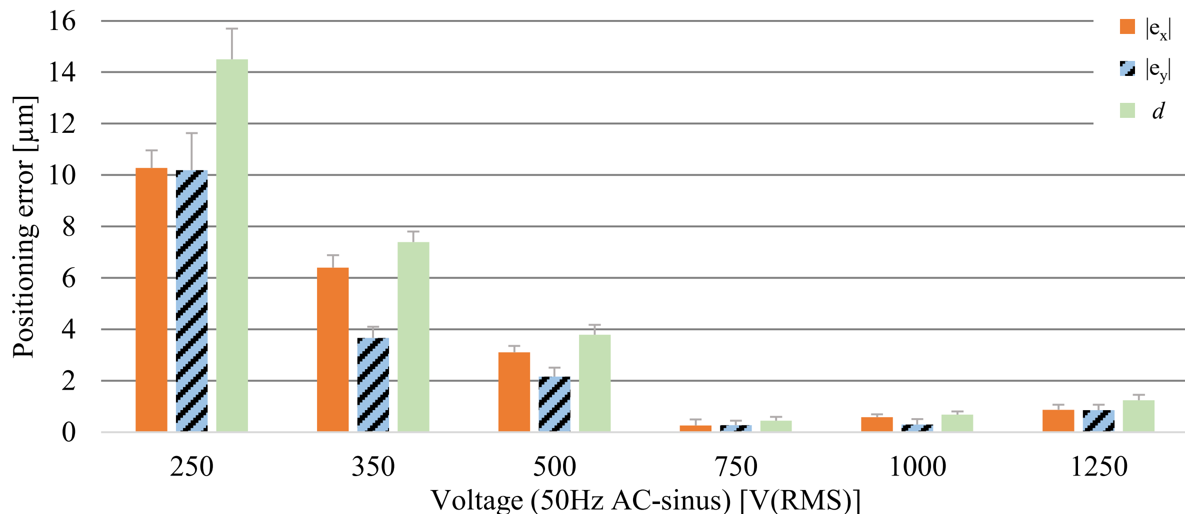

Figure 7: Correlation of the positioning error on the AC-voltage

In this series, the success rate is 100%. This value must be set in relation to the high deviation of up to 700 µm in the pre-positioning. Nevertheless, the top wafer was successfully aligned in every case.

Between 250 VAC and 750 VAC, the positioning error decreases significantly. With 750 VAC, the positioning error *d* is 0.4 µm with a standard deviation of 0.2 µm. However, the measuring method limits the measurement resolution of the positioning error.

At a voltage of over 750 VAC, the positioning error increases again. This indicates that above 750 VAC a different equilibrium of forces is established. With the voltage, the transverse force also increases, i.e. in the *z*-direction. As a result, the upper wafer is attracted and the adhesive layer between the glass wafers is reduced, which leads to an increase in the frictional force. Since an in situ measurement of the adhesive layer's thickness is not possible in the given experimental setup, further investigation is necessary to assess this relationship.

5.2 Influence of the frequency

The second series of experiments investigates the influence of the frequency. With the best results at 750 VAC, the positioning error has reached the limit of our measuring method. To detect a change in the positioning error caused by the frequency, we had to decrease the voltage. Additionally, up to 350 VAC we can use the function generator directly within the setup and the waveform and frequency is not influenced by the transformer. Therefore, the voltage is set to a constant sinus wave at 350 VAC.

The experiments are done in a range of 2 Hz to 200 Hz. Figure 8 shows the correlation between the positioning accuracy and the frequency. As in the first series, the success rate is 100%. The results show that the frequency influences the positioning error. The best result is achieved with 25 Hz. Here the positioning error *d* is 1.5 µm with a standard deviation of 0.5 µm. Increasing the frequency leads to an increase in the positioning error.

It is noticeable that the position error e_y is significantly higher than e_x. This indicates higher friction in the *y*-direction. The effect is likely caused by deviations in the angle of the setup. On the one hand, even with a precise experimental setup, there are still small errors in the levelling, resulting in a gravitational force acting

against the alignment. On the other hand, uneven distribution of adhesive between the wafers leads to tilting between the glass surfaces that affects the homogenous distribution of capillary forces. This effect has not yet been observed in the research carried out on micro components. Due to the smaller geometric dimensions, the error influence would be small relative to the force equilibrium.

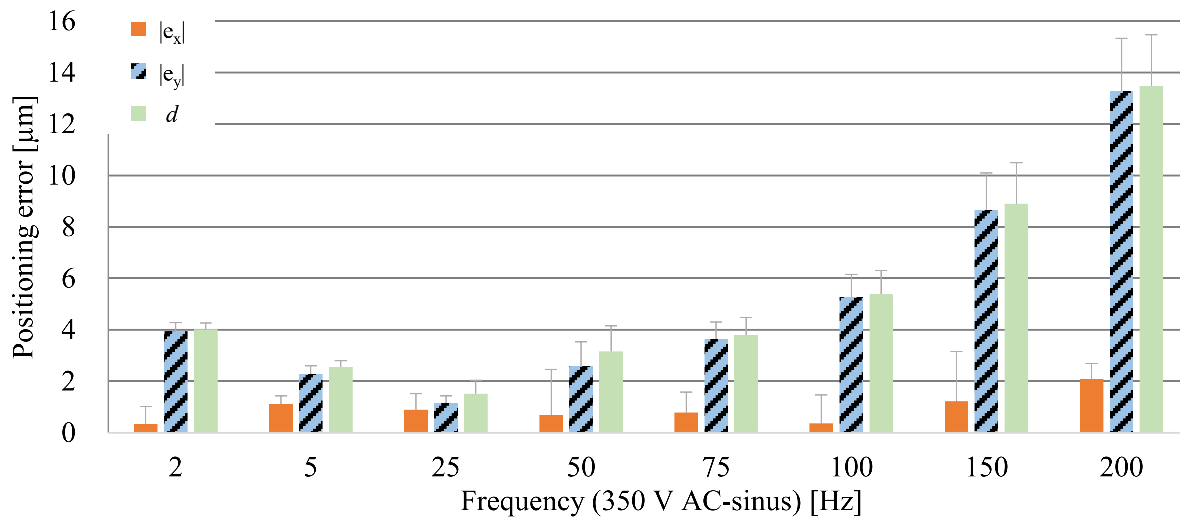

Figure 8: Dependence of the positioning error on the AC-frequency

6. Conclusion and outlook

Aligning components sequentially with high accuracy is time-consuming, expensive and requires special machine technology. In the past, there have been several approaches to address these problems. One of them is electrostatic self-assembly. We adopted this concept to develop assembly strategies for optical devices. This paper introduces a novel concept for full-wafer alignment with electrostatic self-assembly. The predicted application is the high-precision parallel assembly of optical devices.

The focus of this paper was to demonstrate the suitability of electrostatic self-assembly for large parts. Therefore, we combined the individual steps for a structure design in a consistent methodology. Using this methodology, we developed a structure design for the full-wafer alignment. In a new constructed experimental setup, we did several tests for the validation of the concept. During the test, we positioned a 125 mm glass wafer with a success rate of 100%. The experimental results prove that the electrostatic self-assembly, which was previously only used on millimetre-sized MEMS, can be successfully transferred to higher scales.

Two larger test series were carried out for this paper. In the first series, we achieved a positioning error *d* of 0.4 µm with 750 VAC, using a 105 mm alignment structure and 50 Hz alternating current. In the second series, we achieved a positioning error *d* of 1.5 µm with 25 Hz and 350 VAC. One additional finding is that on large scales, small deviations in the angle between the components have a significant influence on the positioning error and can lead to an uneven distribution of forces. To gather more data about the process, the distance between the glass surfaces must be measured in situ. Further development of the structure design also offers excellent potential. Specially designed pad arrangements can lead to better force distribution in a specific direction or block movement in specific directions. We plan to enhance the structure design with a corresponding simulation.

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Biography

Martin Stucki (*1986) studied mechanical engineering at Leibniz University Hannover (LUH) and graduated with a diploma in 2014. Since 2015, he has been a research associate at the Institute of Assembly Technology at LUH (match) where he researches in the field of precision assembly.

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Annika Raatz (*1971) has been the head of the Institute of Assembly Technology (match) since its establishment in 2013. Prof. Dr.-Ing. Annika Raatz is a member of the Society for Assembly, Handling and Industrial Robotics (MHI) and the Academic Association for Production Technology (WGP). Her main research topics are robot aided handling processes, machine concepts for handling, assembly and production automation and soft material robotic systems.