Integrated Switched-Mode Power Supplies with Digital Control Enabling Fast Transient Responses and Parameter Identification

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Abstract

Integrated switched-mode power supplies benefit from innovative digital control loop designs and implementations, fast and goal-oriented parameter identifications, and from robust and fast transient controls of this work. A digital control loop comprises an ADC, a digital controller, and a digital pulse-width modulator / DAC. The ADC and the DPWM / DAC are required to operate with high sample rates, minimum conversion delay, monotonic transfer characteristics, and high resolution. The control loop components of this work extend the application range to SMPS with output voltages higher than 3.3 V of prior publications. A presented delay line ADC (6 bit, 9.5 MSps, 90 ns latency, 1.2 V dynamic operation range) enriches the standard window concept with a live-tracking functionality, which is firstly proposed in this work. This functionality increases the resolution and enlarges the dynamic operation range. A charge pump DAC design offers 40x higher resolution compared to prior art. It guarantees monotonicity and low conversion time, enabling high-bandwidth digital control, along with low steady-state current consumption (20 µA). Large output voltages (>3.3 V) are supported with a high resolution in the order of 15 bits. A comparison of digital control to analog control demonstrates that digital control can be fully integrated. In contrast, this is not guaranteed for analog control and, if possible, chip area is significantly larger. Operating parameters in an SMPS may change significantly, together with its transfer behavior. SMPS passives face production tolerances, temperature dependencies, and aging. An adaption to varying operating conditions and actual values of the passives improves the SMPS behavior, ensures reliability, and saves cost. However, it requires an identification of the present operating conditions and parameters. A parameter identification concept yields results within less than 85 µs in startup and 2 µs in operation, which is 12x and 7000x shorter than prior art. It concentrates on and accurately identifies the most influential parameters of the SMPS, the inductor and the capacitor. A lossless load current identification runs without interruption of ongoing operation with only 3 % maximum identification inaccuracy. A controller adapts to a right half plane zero, that limits the converters' control bandwidths. With the proposed adaption, maximum bandwidth is achieved. Output voltage deviations are reduced by a factor of 2.4 and recovery times by a factor of 1.5 in case of load transients. For the first time, this work introduces a $\Delta V/\Delta t$-intervention control concept, which is applicable, as add-on, to any standard controller. The voltage deviations are reduced by a factor of 2.8, which allows for downscaling the output capacitor by the same factor. The proposed innovative digital control loop designs, fast and

goal-oriented parameter identifications, and robust fast transient controls, meet the needs of small cost, high reliability and flexibility in electronics, that are driven by a rising number of functionalities and features.

Index terms— integrated switched-mode power supplies, fast transient digital control, parameter identification

Zusammenfassung

Integrierte, getaktete Spannungswandler profitieren von den neuartigen Designs und Implementierungen der digitalen Regelschleife, den schnellen und zielorientierten Parameteridentifizierungen und den robusten und schnellen Regelkonzepten dieser Arbeit. Eine digitale Regelschleife setzt sich aus einem ADC, einem digitalen Regler und einem digitalen Pulsweitenmodulator oder einem DAC zusammen. ADC und DPWM / DAC müssen mit hohen Abtastraten, kleinen Wandlungszeiten, monotonem Übertragungsverhalten und hoher Auflösung arbeiten. Die in dieser Arbeit vorgestellten Blöcke erweitern den Anwendungsbereich der getakteten Spannungswandler mit digitaler Regelung auf Ausgangsspanungsbereiche größer als 3.3 V aus früheren Veröffentlichungen. Ein Delay Line ADC (6 bit, 9.5 MSps, 90 ns-Wandlungszeit, 1.2 V dynamischer Wandlungsbereich) erweitert das herkömmliche Fensterkonzept um ein Live-Tracking, das erstmalig in dieser Arbeit gezeigt wird. Es erhöht die Auflösung und vergrößert den dynamischen Wandlungsbereich. Ein Charge Pump DAC Design verbessert die Auflösung früherer Veröffentlichungen um den Faktor 40. Es garantiert Monotonie und geringe Wandlungszeiten, wodurch Regelungen mit hoher Bandbreite unterstützt werden, und auch die Stromaufnahme is niedrig (20 µA). 15 bit Auflösung machen den Einsatz in Spannungswandlern mit hoher Ausgangsspannung (>3.3 V) möglich. Ein Vergleich zwischen digitaler und analoger Regelung von integrierten Spannungswandlern zeigt, dass digitale Regelungen ausnahmslos integriert werden können. Bei analogen Regelungen ist das nicht garantiert. Falls es möglich ist, ist die Chipfläche, die zur Integration benötigt wird, deutlich größer. Die Arbeitsparameter von Spannungswandlern ändern sich und mit ihnen auch das Übertragungsverhalten. Passive Bauelemente weisen Produktionstoleranzen, Temperaturabhängigkeiten und Alterungseffekte auf. Eine Anpassung an die veränderlichen Arbeitsparameter und an die tatsächlichen Werte der Bauelemente verbessert die Spannungswandler-Performance, erhöht die Verlässlichkeit und spart Kosten. Dafür ist eine Identifizierung der vorliegenden Arbeitsbedingungen und Parameter nötig. Ein Konzept zur Parameteridentifizierung liefert Ergebnisse in weniger als 85 µs beim Startup und 2 µs im Betrieb. Das ist 12- und 7000-fach schneller als bisher veröffentlichte Konzepte. Das Konzept legt den Fokus auf und identifiziert die einflussreichsten Parameter des Spannungswandler: Spule und Kondensator. Eine verlustfreie Laststromidentifizierung arbeitet ohne Unterbrechung des regulären Betriebs mit einer maximalen Abweichung von 3 %. Ein Regler wird präsentiert, der sich an eine Nullstelle der rechten Halbebene anpasst. Diese begrenzt die Regelbandbreite des Wandlers. Mit der Anpassung werden maximale Bandbreiten erreicht. Abweichungen der Ausgangsspan-

nung werden um den Faktor 2.4 und die Ausregelzeit um den Faktor 1.5 verkleinert. In der Arbeit wird ein ΔV/Δt-Regelkonzept vorgestellt, das einem beliebigen Regler als Add-on hinzugefügt werden kann. Die Spannungsabweichungen werden 2.8-fach reduziert, wodurch der Ausgangskondensator um demselben Faktor kleiner gewählt werden kann. Die neuartigen Designs der digitalen Regelschleifenblöcke, die schnellen, zielorientierten Identifizierungsmethoden und die robusten, schnellen Regelungen erfüllen die Kosten-, Zuverlässigkeits-, und Flexibilitätsanforderungen moderner Elektronik, die die steigende Anzahl an Funktionen und Features mit sich bringt.

Schlagworte— integrierte getaktete Spannungswandler, digitale Regelung mit schnellen Transienten, Parameteridentifikation

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Contents

1 Introduction

'Digital Transformation', 'Internet of Things', 'Industry 4.0', 'Big Data', 'Autonomous Driving', 'Machine Learning', 'Artificial Intelligence' - these buzzwords are used to describe the transformation of today's way of living [1–6]. All of these topics are strongly linked to electronics and therefore, show the massive impact of electronics on people's lives.

Electronic devices used in these areas get smart, connected, and more powerful [7]. At the same time they become smaller. This effect can well be underlined with the following consideration. The global temperature is rising, drastically [8]. In order to stop global warming, CO_2 emissions are aimed to become small. Since cars are a major contributor to overall emissions, the goal of car manufacturers is to reduce fuel consumption / CO_2 emission. This goal can be achieved by more light-weighted and smaller devices. Simultaneously, the automotive industry experiences a strong push towards autonomous and electrical driving. This is only achievable and comfortable for the drivers with plenty of smart and connected electrical devices, which make safety, comfort, entertainment and communication available.

Integrated circuits offer a possibility to combine high functionality and small volume. Therefore, integrated circuits (ICs) find their way into many electronic devices. They are applied in consumer electronics, e.g. in laptops, smartphones, and tablets. Also, the number of ICs in cars will further increase [9, 10].

Every electronic device and every IC relies on a power supply. The power supply is responsible for voltage and current supply. The current has to be provided according to the demand of the electronic device, whereas the voltage has to be constant at all times. Switched-mode power supplies (SMPS) are well suited to meet this requirement, as they offer high power efficiency along with precise output voltage control. To keep track with the challenging developments of the electronic devices in general, the switched-mode power supply (SMPS) needs to improve, as well. Key elements for the improvement are low cost, high reliability and flexibility. Digital controls offer a solution to increase the performance of the SMPS in terms of these issues and, therefore, show great future potential.

Digital control of SMPS in integrated circuits found distribution beginning in 2001, when the prices for digital CMOS silicon dropped as a consequence of the telecom crash. Since then digital control has evolved and advanced, but there are still things to improve [11].

1.1 Scope of This Work

The focus of this work are SMPS with digital control on IC-level. Figure 1.1 shows a structural diagram which summarizes the scope of this work in detail. It is driven by recent trends towards an increasing number of features and functionalities, and growing complexities, for example due to comfort, safety, and diagnostics requirements in various applications, such as automotive or consumer electronics.

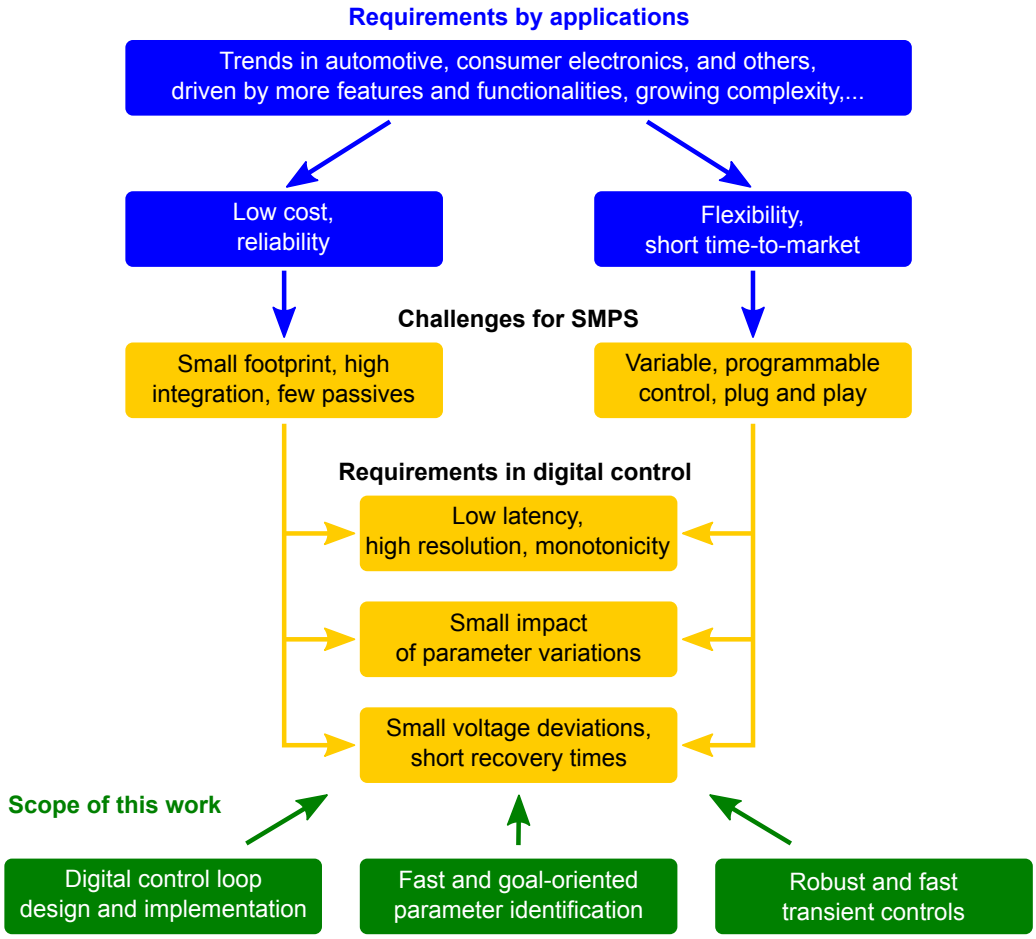

Fig. 1.1: Summary of the scope of this work.

These trends lead to demands on the SMPS, which include low cost, high reliability, short time-to-market, and high flexibility. Cost pressure and safety rules make products with small cost and high reliability necessary. Short time-to-market is essential for business success. Besides, the variety of applications and functionalities leads to a demand for systems that are able to adapt to the respective application. SMPS with the described characteristics can be realized with the help of digital control as integrated circuits.

In order to provide the described characteristics the integrated circuits are required to have small integration areas and a small number of passives in order to be fabricated with small footprint and a high level of integration. Thus, cost can be reduced and reliability enhanced. In order to keep track with the demanded

high flexibility and short time-to-market, variable and programmable controls together with plug and play features are the challenges for SMPS.

As a first topic this work covers digital control loop component designs and implementations operating with low latency, high resolution, and guaranteed monotonicity. Secondly, the impact of parameter variations is reduced to a minimum by fast and goal-oriented parameter identification concepts. Thirdly, this work presents robust and fast transient controls enabling innovative voltage supply with small output voltage deviations and short recovery times.

1.2 Outline

Chapter 2 describes the applications of SMPS and the motivation for this work. SMPS serve as voltage supplies for electronic devices. It is demonstrated for exemplary applications, that they are facing more frequent and more intense disturbances as a result from the increased system functionalities (Section 2.1). These challenges are addressed in this work by the usage of digital control, which comes along with numerous advantages. Section 2.2 describes why the variability of the controller coefficients of a digital controller meets the desire for low-cost systems and for plug and play functionality.

In Chapter 3 the fundamentals of SMPS are given and special requirements of digital controls are explained. Different SMPS topologies and operating principles are reviewed and the pros and cons of miscellaneous control concepts are discussed (Section 3.1). Also, the parameters of the converter predominantly used in this work and a plant model are defined. The digital control loop structure is outlined in Section 3.2. Special challenges of digitally controlled SMPS are explained. It is pointed out why low dead times, proper resolution and monotonicity are of great importance.

Chapter 4 deals with the control loop component designs. Suitable topologies for guaranteeing small overall loop latency, proper resolution, and monotonicity are presented. A focus is set to high resolution, enabling operation with higher output voltages than prior art in integrated solutions. Section 4.1 presents architectures for analog-to-digital conversion of the output voltage. For Delta-Sigma analog-to-digital converters (ADCs), it is demonstrated how to design the converter in order to achieve good resolution and proper conversion time for control bandwidths up to 10 kHz. A delay line ADC is introduced that works with a live-tracking window concept, which achieves excellent resolution over a wide voltage range. It is further shown how to implement digital controllers in Section 4.2. Section 4.3 reviews architectures for digital-to-analog conversion and shows a digital pulse-width modulation (DPWM) architecture with zero latency, 12-bit resolution, and measured monotonicity. Further, an R-2R digital-to-analog converter (DAC) is designed according to the resistor mismatch of the technology used. Also, the maximum conversion rate and DAC bandwidth are

analyzed. In addition, this work presents a high resolution, wide-range charge pump DAC. It is shown for the charge pump DAC design how the high resolution can be ensured by dedicated differential switches, and how high leakage can be prevented by proper switch design and biasing. Section 4.4 presents the results of a comparison of the digital control to conventional analog control regarding chip area and further aspects.

Chapter 5 explains why parameter identification is beneficial and shows concepts with small identification times. As part of this work, a study of the variations of the inductance and the capacitance of standard inductors and capacitors is presented in Section 5.1. It is analyzed, why a standard off-the-shelf 10 µF-capacitor may either be 6 µF or 14 µF, unpredictably. Parameter identification concepts of prior art are reviewed and it is explained, why they are not suitable in numerous applications, Section 5.2. Therefore, in Section 5.3 alternative identification methods are proposed, that concentrate on relevant converter parameters and prioritize a key parameter for application: small identification duration. A simple, purely digital and lossless concept for live identification of the load current is presented (Section 5.3.2). An analysis shows that it works well over a wide range of converter operating points. Section 5.3.3 introduces a combined identification concept for the inductor and the capacitor. For identification during startup, it is explained how the innovative identification scheme, presented in this work, can be extended for higher identification accuracies.

Chapter 6 explores control concepts for improved transient responses. On the basis of the prices for capacitors and of the current development in voltage supply levels, it is explained, why fast transient controls are very important for future SMPS. Especially for boost converters, it is essential to provide fast transient controls, as they suffer from a bandwidth limitation due to the right half plane zero (RHPZ). Section 6.2 shows that with simple controller adaption the bandwidth of boost converters can be enlarged. Further, in Section 6.3 a very robust control concept is proposed. This $\Delta V/\Delta t$-intervention control concept significantly improves the transient behavior. It is explained how any conventional controller benefits from the simplicity of the concept and that an intervention within only one computation cycle is effective.

Chapter 7 summarizes and concludes the results of this work and further, shows approaches for future work.

1.3 Contributions of This Work

The main outcome and contributions of this work are described in the following.

1. **Digital control loop design and implementation:**
   The proposed designs of integrated control loop components, such as the ADC, the digital controller, and the DAC with small conversion times, high resolution, and guaranteed monotonicity, allow to operate SMPS with stable control at high bandwidth. These blocks enable an operation at high

output voltages (higher than the 1-3.3 V of prior publications) and high control bandwidths (higher than 100 kHz).

Recent ADCs for digital controls are limited in resolution and only cover the voltage range around the control set point. They can only be used in SMPS with small output voltages. High output voltages require superior resolution of the ADC. To apply parameter identification methods, the ADC needs to cover the full voltage range at the same time. This work first proposes a live-tracking functionality, which allows for an operation over the full voltage range with significantly enlarged resolution by following the output voltage dynamically. Experimental results demonstrate a delay line ADC with live-tracking, that achieves 0.5 mV voltage resolution (6-bit), 90 ns conversion time, and 1.2 V dynamic conversion range. It was published at ESSCIRC 2018 [12].

This work proposes a charge pump DAC design with (1) high resolution for accurate output voltage regulation and for avoiding limit cycle oscillations (LCO), with (2) short conversion time for control stability, and with (3) inherent monotonicity for preventing oscillations. With these three features the DAC qualifies for use in automotive and other high-voltage applications. Measurement results confirm the short conversion time of 128 ns. The very high resolution of 53.8 µV, which is equivalent to a 15-bit full-range DAC, is enabled by special design actions. This was not achieved by prior art DACs. Monotonicity is guaranteed by concept. The steady-state current consumption (20 µA) is very low. With an extremely small leakage based drift of 0.076 µV per switching cycle a 1 LSB output voltage change is first observed after several thousand switching cycles in standard converters. The proposed DAC was published at ESSCIRC 2018 [12].

A Delta-Sigma ADC with small layout area is optimized for low conversion time (3 µs) and sufficient resolution (9.5-bit). A hybrid DPWM for direct digital pulse-width modulation signal generation is developed with zero latency, 12-bit resolution, and guaranteed monotonicity. Further, a R-2R DAC with 10-bit resolution is shown. Investigations with special focus on digital control comprehensively derive the design requirements for guaranteed monotonicity of the R-2R DAC. Also, the conversion time for control stability analysis is derived.

A performance comparison of the presented control loop components to analog control shows that smaller output voltage deviation and shorter recovery times are achieved with digital controls. Beyond that, a chip comparison to commercial automotive products demonstrates that digital control saves cost. An automotive airbag chip comprising a boost converter can be fabricated with digital control at 2.5 times smaller chip area. Full-integration is achievable with digital control in an automotive power IC, which is not possible with analog control. Through the full-integration one pin less is required. The electromagnetic compatibility (EMC) requirements are met, since there is no pin sensitive to electromagnetic interferences. Automotive safety rules are followed more easily, as no external component loss detection must be implemented.

2. **Fast and goal-oriented parameter identification:**

   As part of this work, a study on parameter variations of the main components of an SMPS points out that cost is reduced and availability ensured when passives with production tolerances are accepted. Low-cost standard capacitors easily vary by around $\pm 40\,\%$, if production tolerances, temperature variations and aging are taken into account. The influence of such parameter variations on the transfer behavior of SMPS is immense: the control bandwidth varies by a factor of five and the phase margin uncertainty endangers stability with up to 70° variation. Standard control designs have to provide large margins to ensure stability. In order to fulfill a given maximum output voltage deviation specification with any parameter variation, the output capacitor value needs to be chosen five times higher than without parameter variations. It is demonstrated that inductor, output capacitor, and load have the largest impact on the transfer behavior of an SMPS. Existing parameter identification solutions propose identification with continuous output voltage disturbances. Complex sets of equations are solved at the expense of extensive hardware effort. Identification times are in the range of several milliseconds. This is limited in automotive and other applications, as no in-operation output voltage disturbances are allowed and also startup time is smaller than 1 ms including converter soft-start.

   In this work, a combined inductor and capacitor identification is shown for the first time. It works both before startup and during operation. The startup identification comprises a very short 3-pulse identification scheme for identification of the most influential converter parameters. Experimental results confirm an accurate identification within $85\,\mu s$, which is 12x shorter than prior art [13]. This enables the usage in applications with limited startup times, e.g. automotive applications. Measurement results indicate a low maximum identification inaccuracy of about 5 % for the inductor and 13 % for the capacitor, respectively. The identification during operation leads to the same accuracies and is finished after at most $2\,\mu s$ (7000x shorter than prior art [14, 15]). Due to the high identification accuracy and the low overall implementation effort of the presented identification an accurate controller adaption to the actual capacitor and inductor value is enabled. It allows for autotuning in current mode controlled converters, which was not published before. The proposed identification was published at APEC 2019 [16].

   This work proposes a load identification method which is of great relevance for advanced control concepts and adaptive voltage positioning. In contrast to prior art, it works at high accuracy without additional circuitry and power losses. Experimental results show very small identification inaccuracies of 3 % and below. It was first presented at PRIME 2016 [17].

   In the proposed solutions the load, the inductor value, and the capacitor value, are determined. That is why the control success of advanced control concepts, that strongly relies on these values, can be significantly increased.

3. **Robust and fast transient controls:**

   The supply voltages of electronic devices decrease to lower values along with smaller voltage margins. A study of capacitor volume sizes and prices shows that smaller capacitors are more economical. Smaller voltage deviations and smaller capacitors can only be achieved with intelligent controls.

   In boost converters, the RHPZ limits the maximum control bandwidth. Various adaptive controls, maximizing the bandwidth and stabilizing the control, are proposed in this work. An adaptive control, which chooses the best fitting controller configuration according to the load situation, improves the output voltage deviations by a factor of 2.4 and the recovery time by a factor of 1.5 in case of load transients. Extending the controller adaption also to the input voltage, the control behavior is improved in 93 % of the operating points of the presented boost converter. The control concept was presented at PRIME 2016 [17].

   Further, a robust digital control technique, which is referred to as $\Delta V/\Delta t$-intervention control in this work, is proposed for the first time. It improves the output voltage deviations by a factor of 2.8, and the recovery time by a factor of 1.8. Thus, the capacitor becomes cheaper and high-frequent load transients are well handled. The control technique is widely applicable, as it supports constant switching frequencies, allows for duty cycle limitations, and does not require fast inductor current sensing or high-performance analog-to-digital conversion. The proposed $\Delta V/\Delta t$-intervention digital control technique relies only on few parameters that are most likely subject to variations and, therefore, it is usable without any self-tuning procedure or calibration routine. For digitally controlled boost converters in automotive applications with high safety requirements, this control is well suitable, because it does not face mode or configuration transitions, guarantees stability, and effectively improves the transient behavior with low implementation effort. The $\Delta V/\Delta t$-intervention control was published at APEC 2018 [18].

2 Motivation for Digital Control of Switched-Mode Power Supplies

2.1 Applications

With the increasing number of electronic devices in every imaginable field of living voltage supply generation from various energy sources is required. An SMPS generates proper voltages for operation of the electronics from the corresponding energy source. In the following an overview of exemplary SMPS applications is given, Fig. 2.1. [19, 20] present plenty more application fields of SMPS with both boost and buck functionality.

Figure 2.1 shows that SMPS are used in cars, laptops, smart phones, tablets, TVs, and e-bikes. They are inserted for supplying infotainment systems with human-machine interfaces (HMIs) in cars, for supplying board computers and sensors in e-bikes, or for supplying various microcontrollers, central processing units (CPUs), and application-specific integrated circuits (ASICs) with enormous computation capabilities in all applications. These examples live from a variety of energy sources. In cars, there is the car battery (see below for more information about the power supply and distribution in cars), which exhibits varying voltage values due to different charging states and load situations. Therefore, SMPS provide constant voltages to the electronic sub-blocks. In other applications, the energy sources are regular, smart phone, rechargeable batteries or intermediate DC voltages generated from the AC grid.

USB has become a standard interface in electronics for both data and power transfer. Applications comprising a universal serial bus (USB) require both step-up (boost) and step-down functionality (buck), e.g. smart phones or tablets. When the smart phone / tablet needs to get charged, the SMPS works with step-down functionality converting the 5 V from the USB port to the lower voltage of the lithium battery. In contrast, when any peripheral, such as a mice or a keyboard, is plugged in, the SMPS operates with step-up functionality converting the lithium battery voltage to the 5 V required by the peripheral.

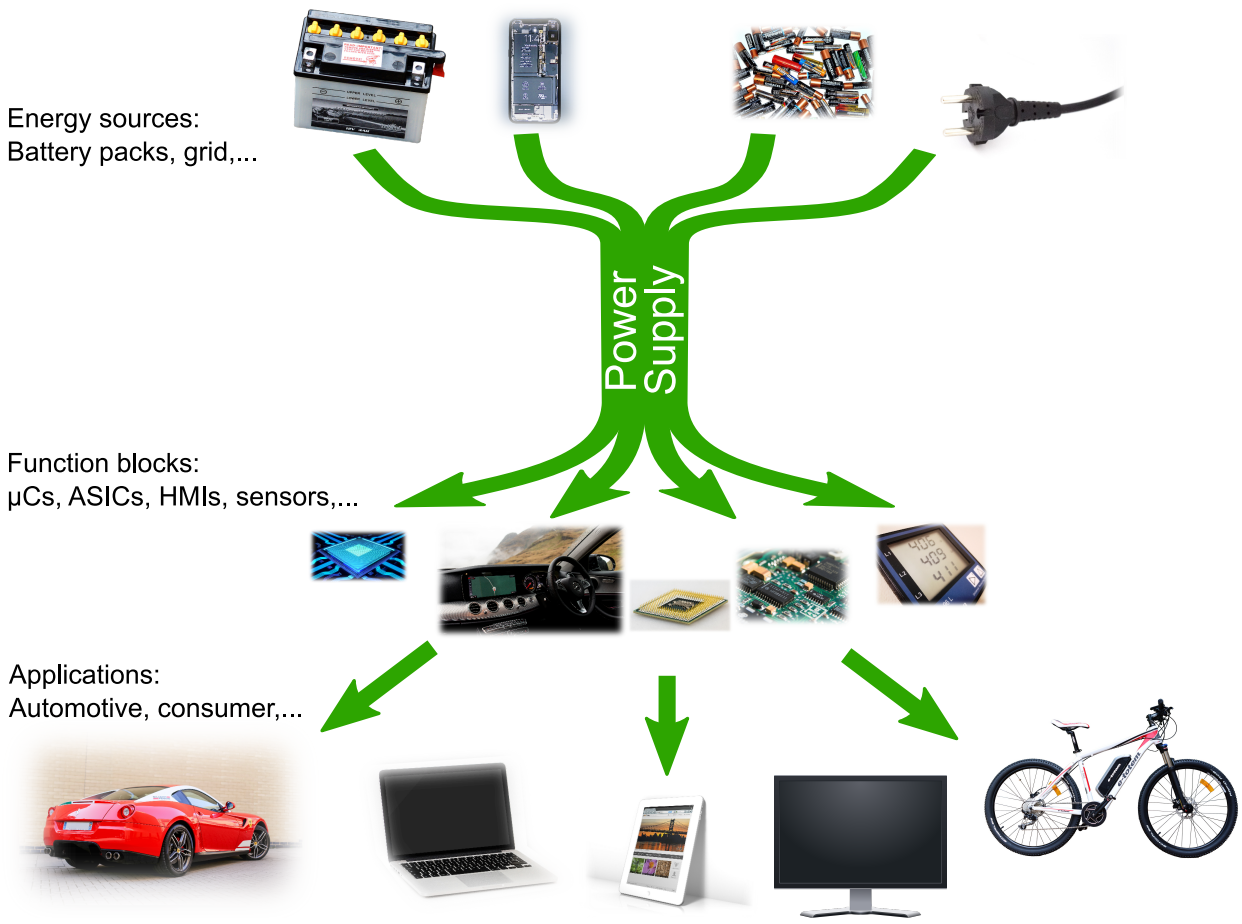

Fig. 2.1: Applications of SMPS.

In robotics and drone applications, SMPS are used for converting the battery voltages, which are multi-cell lithium battery packs with typical voltages ranging from 6 V to 25 V, down to 5 V for motion and flight controllers.

There are many more fields, where SMPS are applied, e.g. aircraft, satellites, data centers, energy harvesting, implantable devices, among others.

This work covers, but is not limited to the standard applications as mentioned above. Further, it focuses in particular on quality applications, which come along with enlarged safety and reliability requirements. Therefore, these applications, where automotive applications stand out, are discussed in more detail in the following. These applications are highly relevant for future SMPS, since their markets, in particular the automotive market, are expected to be the next big semiconductor markets [10]. The forecast of [21] shows that the automotive IC market is awaited to be the fastest growing IC market with an annual growth rate of 12.5 % till 2021.

Modern cars already contain many electronic devices and applications. Autonomous driving enables the end-user to utilize more comfort, communication, and entertainment features. This development and recent

trends towards hybrid and electric vehicles continuously enlarge the number of electronics and electric functionalities. At the same time, the number of electronic control units (ECUs) and sensors grows strongly, as they are required for assisted or autonomous driving. Still, safety is very important in cars which explains an impressive number of electronic devices for airbags, intelligent light systems, collision prevention systems, and driver assistance systems. Further, actual mechanical systems are replaced by electrical components, e.g. braking, steering, among others. To sum up, there is already an impressive number of electronics in a car and the number is still rising.

The enormous number of electronics makes the energy supply and distribution a challenging task. For this reason, nowadays cars often have two energy sources, a 12 V- and a 48 V-battery, Fig. 2.2. From these energy sources the voltage supplies for the electronics are generated. High power loads are connected to the 48 V-battery for reasons of efficiency. Light loads and many traditional 12 V-loads remain with the common 12 V-battery. Figure 2.2 shows such a system with the many DC-DC converters (SMPS), which are used for generation of various voltage supply levels. There are SMPS necessary for decreasing voltages to lower output voltages (buck) and also for increasing voltages to higher output voltages (boost). In opposite to other applications, there are various voltage supplies required in a car not only at low voltages levels (1 V-3.3 V), but also up to 48 V, and higher. Typical loads are human-machine interfaces, sensors, motor and valve drivers, network interfaces (CAN, etc.), displays, and many others which are used for infotainment, heatings, lighting, air condition, and so on.

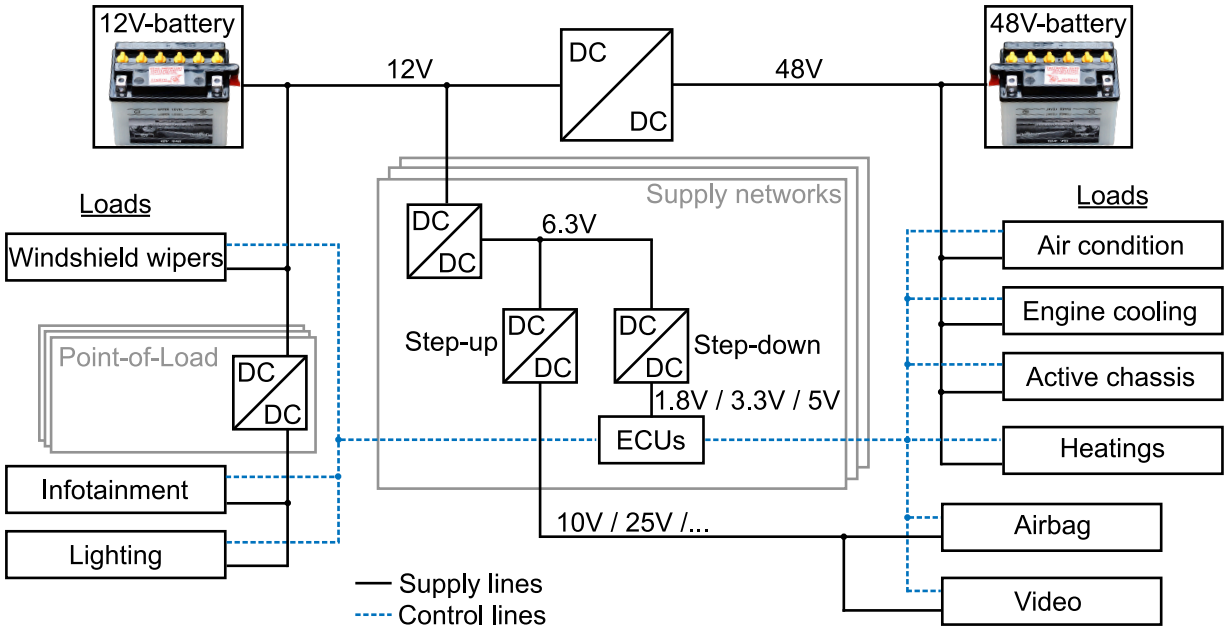

Fig. 2.2: Energy distribution and voltage supply in modern cars.

In order to safely operate all the electronic loads, several SMPS are implemented, as point-of-load converters for the generation of voltage supplies directly at the load or as supply networks for the generation of sub-

voltages. An electronic control unit (ECU) is used for the control of electrical systems in a car, such as the airbags, etc. The block 'ECUs' (Fig. 2.2) combines microcontrollers, ASICs, or field programmable gate arrays (FPGAs), among others. Due to the increasing functionalities of the electronic loads and due to the rising computing effort of these ECUs, SMPS have to operate at high performance for providing constant voltage supplies. They have to counteract load transients, which occur more often and are more heavy. Simultaneously, the voltage margins for regulation shrink due to increased supply voltage requirements of the ECUs. This means, that load transients have to be regulated with smaller voltage deviations than before. Further, the SMPS are aimed to be small and light-weighted for fuel savings and low CO_2 emissions.

In automotive, numerous diagnostics and protection features are mandatory, such as short circuit to ground detection, open load detection, power limitation indication, external components loss detection, over and under voltage protection, among others. Consequently, also for SMPS such functionalities are relevant. This applies in particular to external passives that need to be identified in value or in availability [22].

Enhancing passenger safety is a main goal for future car development. New intelligent lightings, such as adaptive front light systems turning on and off the high beam dynamically or in segments with a camera based technology, improve the road illumination and, therefore, the passenger safety. In these lighting systems, boost converters are necessary for increasing the 12 V-battery voltage to a higher voltage level demanded by the high beams. Due to the new segmented turn-ons, the boost converters recently face an increased number of load transients with different intensities. Also, the camera used for control of the high beams requires a supply. Typically this supply is in the range of 10 V. Again, a supply network, including buck and boost converters, is necessary generating the 10 V-supply, see Fig. 2.2.

Also, in other mobility applications the number of and the requirements of SMPS rise. Sales figures for e-bikes show a steep upward trend [23]. Here, SMPS provide the supply voltages for the head unit and the board computer with HMIs. Typical voltages are 36 V or 48 V for the battery pack, which are converted into lower voltages for the loads in a e-bike. Also in these applications, safety features gain in importance, anti-lock braking systems (ABS) were lately presented [24]. In case of a dangerous driving situation the ABS ensures safe breaking. For a short time, great computational effort is generated, which again requires the SMPS to operate with high performance to instantly provide the high additional supply current demanded in such a situation.

Furthermore, there are a lot of other mobility applications that require SMPS operating at high-performance in terms of wide current ranges support, fast regulation of large load transients, and small deviations from the nominal voltages. These applications include for example e-scooters, pedelecs, drones, segways, e-wheels, among others.

2.2 Digital Control Benefits

SMPS require a control to ensure constant output voltages even when the SMPS is disturbed. Traditionally, these controls were made of analog components. On the one side, this is reasonable as the analog control loops have a simple structure and analog controls, in general, are well understood. On the other side, analog controls face some significant limitations. In 2004, Maksimović, Zane, and Erickson summarized previously published digital controls and also introduced new practical ones [25]. They demonstrated that performance improvements are achievable and new capabilities are enabled by digital controls. As these features are difficult or impractical to realize with analog controls, digital controls gained in popularity ever since. The significant advantages and new possibilities are explained in detail in the following subsection. Finally, the advantages of digital controls are summarized in a comparison to analog controls in Table 2.1.

Variability of Controller Coefficients

Improved control performance. SMPS are expected to provide constant voltages regardless of the intensity of the load transients to regulate. This task is demanding, as they are getting more and more intense, see Section 2.1. Using digital control, it is simple to vary or to exchange the controller coefficients with other stored coefficients. This enables the use of adaptive and smart controls. These controls allow for performance improvements in terms of small output voltage deviations and short recovery times. Thus, the limits of standard controls can be broken and cost can be reduced, which is not possible with analog controls.

Variable controller adaption. End-users demand for low-cost systems and highly prefer plug and play solutions. Digital controls of SMPS show great potential to make these features available by reason of variable controller coefficients. When parameter identification is applied, the system can adapt its controller by itself. Also, in operation such an adaption to the actual situation, called autotuning, is achievable. Since in analog control the controller is built with passives, such as resistors and capacitors, the implementation of advanced controls, plug-and-play features, and autotuning is only possible with significant hardware effort.

Enhanced programmability and flexibility. Manufacturers like to use as few platforms as possible to develop the SMPS products, since this reduces the design effort. With the great programmability and flexibility of digital controls they can greatly reduce the number of platforms still meeting all customers requirements. A single digital control design enables programmability of the nominal output voltage, the controller coefficients, startup behavior, and many other key parameters. Consequently, development cost is significantly reduced.

Digital Design Advantages

No parameter variations of compensation devices. SMPS designers are required to keep the passives of the SMPS small in order to save cost. Yet, stability takes precedence under all circumstances. Ensuring stability with small passives is difficult and therefore, is already a challenging task for SMPS designers. Additionally, with analog control they have to take into account large margins for the parameter variations of the passives used. This means that the nominal values of the passives need to be chosen larger, because resistors and capacitors underlie production tolerances, temperature dependencies, and aging. Through these effects, the actual value of such a device quickly varies by approximately $\pm 50\%$ of its nominal value. The variation is not predictable. Since the passives of the controller are not the only ones in an SMPS system, they add up to an immense overall variation of the transfer function, see Section 4 and 5. The control design gets simplified and cheaper by digital control, as there are fewer passive components.

Good design portability. Time-to-market is essential for the success of a product. Consequently, short development cycles are a great challenge to bear in development. In electronics, digital control designs are very high speed integrated circuit hardware description language (VHDL) based. Therefore, the controller design is independent on the implementation platform, it can be implemented in any FPGA, µC, or IC. Especially, in integrated solutions the design portability is high compared to analog controls. VHDL based designs are independent on the technology used, whereas an analog design shows dependencies on the technology used. With good design portability shorter development cycles are enabled, e.g. in consumer electronics and automotive electronics.

Shrinking process technology nodes. In cost-driven applications, chip area is required to be as small as possible. Digital designs for integrated solutions benefit from shrinking process technology nodes, which become smaller from one process generation to the other. With shrinking nodes the digital design needs less chip area, which saves cost. In contrast, the cost savings of the analog counterpart are relatively small, since analog structures most often do not scale down by the same factor as digital structures do. The reasons are design difficulties due to lower voltage rails and a massive increase in physical effects in the layouts [26,27].

Simple monitoring and diagnostics. Due to the growing complexity of modern electronic systems, monitoring, diagnostics and communication features are highly demanded. They enable safe operation and indication of system status including failures during operation and simplify maintenance. With a digital core the implementation of these features becomes simple. Low power modes for energy saving, e.g. pulse skipping or segmented field-effect transistor (FET), can be realized much easier than with analog systems, as the control of the modes can be implemented digitally [28,29].

Adaptive voltage positioning. To follow the strict voltage margin specifications of modern electronic devices, adaptive voltage positioning is implemented [30, 31]. In adaptive voltage positioning, the set point of the control is modified according to the load situation. When the load is already high, load transients to higher loads, which would lead to a voltage drop, can be excluded. Therefore, the control set point is moved to a lower value. Thus, for a subsequent load transient to low load, more voltage headroom is available for regulation of the voltage overshoot. Thus, this helps to fully exploit the specified output voltage margin in an SMPS in case of load transients. In consequence, the output capacitor values can be chosen lower. Adaptive voltage positioning can be implemented digitally without complex current sensing and analog position control.

Feasibility of parameter identification. Cheap inductors and capacitors for building the SMPS come together with great parameter variations. The realization of parameter identification is comfortable in digital systems, as stimulation, observation, and analysis of the SMPS for identification can be executed digitally with low effort. This becomes even more relevant when thinking of more complex converter topologies, as there is a larger number of passives used. Therefore, the controller design is more difficult and can be simplified by means of parameter identification.

Cost Savings Through Area and Footprint Minimization

Area minimization. In integrated chip development, integration area equals cost. With digital control the chip area required for the integration can be smaller than with analog control. The area savings depend on the control method and further on the size of the analog passives required for building the analog controller. In turn, this size depends on the converter topology, power class, and control bandwidth. The size of the digital implementation is nearly constant as almost always the same ADC, DAC or DPWM, and digital controller can be used regardless of the aforementioned factors.

No pin and external components. Ensuring reliable system operation is often difficult in harsh environments. This accounts in particular for external components, which are expected to work across a whole operating spectrum of temperature, vibration, moisture or even contaminations. A great advantage of the digital implementation is that full-integration is always achievable. In analog control, if the passive device values are too large, they cannot be integrated. Hence, they are applied externally. Therefore, an additional pin including ESD protection has to be spent. In applications with strict EMC requirements this very sensitive pin is unfavorable. It may prevent that direct power injection (DPI) tests will not be passed. Also, loss / short-circuit detection for the external devices is necessary and causes additional cost. Further, externally mounted passives face parasitics, while this is negligible for integrated passives.

Table 2.1 summarizes the advantages of digital control and compares it to analog control. The comparison refers to integrated solutions.

Tab. 2.1: Digital control benefits compared to analog control in integrated SMPS.

Parameter	Digital	Analog
Control performance	Low effort for advanced controls due to variable controller coefficients, simple load identification and position control for adaptive voltage positioning	High effort for advanced controls due to non-variable compensation devices, complex current sensing and position control for adaptive voltage positioning
Configurability / flexibility	Simple controller adaption and system configuration (Section 5 and 6)	Controller adaption and system configuration only with large hardware effort
Parameter variations	Not critical, as no compensation devices required (Section 6) + identification of SMPS passives (Section 5)	Critical, compensation devices and SMPS passives required
Time-to-market	Short, due to few production platforms, high design portability, and feasibility of plug- and play features	Long, due to individual control design for each application
Production aspects	High design portability, benefit from shrinking process technology nodes, simple monitoring and diagnostics, low test cost	Moderate design portability, no benefit from shrinking process technology nodes, limited monitoring and diagnostics, relatively high test cost
Application range	Prior art (ICs): limited to $V_{\text{out}} < 3.3\,\text{V}$, this work: enlarged V_{out}-range (Section 4)	Large V_{out}-range in integrated solutions
Design challenges	High resolution and monotonicity of ADC and DAC for preventing oscillations, low conversion times for control stability (Section 3.2)	Parameter variations of passives, prevention of controller wind-up, meeting EMC requirements, etc.
Full-integration	Always achievable, no external components, no pin for their connection (Section 4.4)	Achievable only in few applications, most often external devices with pin for their connection
Footprint / chip area	Constantly small, depends on application (Section 4.4)	Large, depends on application (Section 4.4)

In conclusion, digital control of SMPS benefits from the variability of controller coefficients, general digital design advantages, and area and footprint minimization. The variable controller coefficients enable im-

proved control performance through smart and adaptive controls, variable adaption of the controller used for autotuning and plug-and-play functionality, and enhanced programmability and flexibility for low development cost. General digital design advantages include that there are no parameter variations, which are caused by the compensation devices in case of analog control. Once the design platform has been developed, the good design portability leads to short development cycles. The digital design benefits from shrinking technology nodes expected in future fabrication technologies. Diagnostics and monitoring can be implemented easily, which allows for predictive maintenance and safe operation. Parameter identification is enabled through the digital design. Therefore, cheap inductors and capacitors can be used. The area and footprint minimization leads to cost savings and high reliability by eliminating external components and the corresponding pin.

3 Fundamentals of Switched-Mode Power Supplies with Digital Control

Electronic devices rely on voltage supplies. In a typical electronic system, the power supply, i. e. a battery, does not deliver the appropriate voltage necessary for operation of the device, as the output voltage of the battery does not match to the supply voltage required by the device. Further, the battery voltage varies according to its charging status or in consequence of load changes, while the electronic device requires a constant voltage. Therefore, an intermediate stage - a switched-mode power supply (SMPS) - is used in order to convert the battery voltage into the appropriate supply voltage level for the electronic device.

3.1 Switched Mode Power Supplies

SMPS is the umbrella term for various topologies of voltage conversion, from relatively simple topologies like buck converters to highly complex resonant converters. This work focuses on the control of these converters, in particular of boost and buck converters.

A boost converter converts an input voltage V_{in} into a higher output voltage V_{out}. The boost converter operates in two phases. In a first phase, energy is stored, and in a second phase, energy is transferred. In the following, the working principle of a boost converter is explained on the basis of these two phases. A buck converter converts an input voltage V_{in} into a lower output voltage V_{out}. The working principle is similar to the working principle of a boost converter. Fundamentals of buck converters can be found in Appendix A.1.

The converters operate either in continuous conduction mode (CCM), where the inductor current does never reach 0 A, or in discontinuous conduction mode (DCM), where the inductor current partially reaches 0 A. In the following, the inductor current characteristics, and also voltage characteristics, are shown for CCM.

For constant and stable output voltage under all operation conditions a control is used. Typically, one of the two standard control methods is applied: voltage mode control (VMC) or current mode control (CMC). For controller design, no matter if analog or digital, a plant model is required.

In the following the fundamentals of a boost converter are shown and a plant model is defined.

Topology and Working Principle

Figure 3.1 shows the topology of a boost converter. The boost converter is controlled with the help of a PWM signal controlling the switch. The output voltage is set by the duty cycle $D = t_{on}/T_{sw}$. The switch on-time is t_{on}, the switch off-time is t_{off}, and $T_{sw} = t_{on} + t_{off}$ is the switching period.

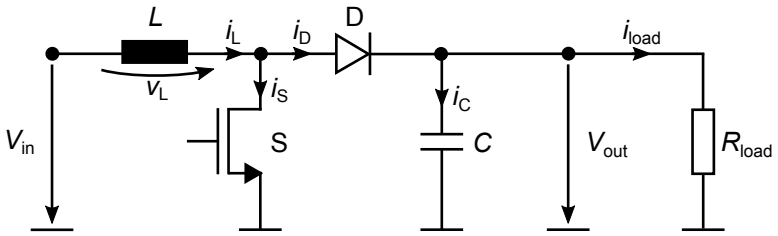

Fig. 3.1: Boost converter topology.

In the following part, the output-to-input voltage ratio is derived assuming CCM and steady-state operation. Parasitic effects have only minor influence and, thus, are disregarded for the explanation of the working principle. The relevant current and voltage characteristics are shown in Fig. 3.2.

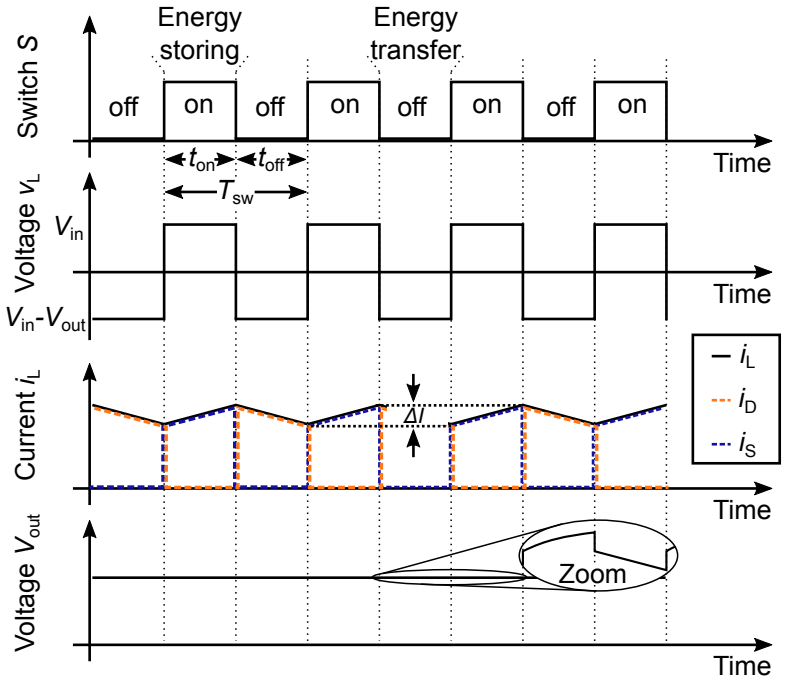

Fig. 3.2: Boost converter waveforms.

In the phase of energy storing the switch S is conducting. Consequently, the inductor current i_L is rising, whereas the diode D is blocking. The load, which is modeled by an ohmic resistance R_{load}, is solely supplied from the output capacitor. Since parasitics are neglected, the inductor voltage V_L is described by:

$$V_L = L \cdot \frac{di_L}{dt} \rightarrow V_{in} = L \cdot \frac{\Delta I}{t_{on}} \tag{3.1}$$

ΔI is the current amount by which the inductor current rises during the phase of energy storing.

In the phase of energy transfer the switch S is blocking. Consequently, the energy stored in the inductor is transferred to the output. Thus, the output capacitor is charged and the inductor current decreases. The following equation describes the inductor voltage:

$$V_{\mathrm{L}} = L \cdot \frac{di_{\mathrm{L}}}{dt} \rightarrow V_{\mathrm{in}} - V_{\mathrm{out}} = L \cdot \frac{\Delta I}{t_{\mathrm{off}}} \tag{3.2}$$

In this phase, the inductor current decreases by the current amount ΔI, Fig. 3.2.

In steady-state, ΔI of the energy storing phase and of the energy transfer phase are equal. By combining equations (3.1) and (3.2) the output-to-input voltage ratio can be derived:

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{1}{1-D} \tag{3.3}$$

There is no continuous current provided to the output capacitor in a boost converter, which can be seen by the 0 A-portion of the diode current i_{D}, Fig. 3.2. As the capacitor current i_{C} is described by $i_{\mathrm{C}} = i_{\mathrm{D}} - i_{\mathrm{load}}$, the current steps in the diode current waveform are propagated to the output capacitor. Consequently, the output voltage ripple can get relatively large. This is shown in the zoomed part of Fig. 3.2. While the switch S is on, V_{out} decreases linearly, because a constant current is drawn from the capacitor. While the switch is off, the output voltage ripple V_{out} is determined by the values of C and its parasitic resistance R_{C}.

Control Concepts

The main goal of SMPS is to provide a constant output voltage, which is immune to disturbances, e.g. input voltage or load variations. Therefore, the duty cycle is not kept constant, but controlled. There are two common control methods: voltage mode control (VMC) and current mode control (CMC).

VMC is well suited for straight-forward control loop design and implementation, as it comprises only a single control loop, which is adequate to analyze and implement, Fig. 3.3. First, the analog output voltage is sensed with the help of a high-ohmic resistor feedback divider and then converted into a digital signal. This resistor feedback divider is in particular necessary with relatively high output voltages, which are the scope of this work. It is required, as the ADC is working in a low-voltage supply domain. The digital signal is used for the calculation of the control deviation, which in turn is used to determine the controller command. This digital controller command is then converted into a pulse-width modulation (PWM) signal with a duty cycle proportional to the controller command. The PWM signal controls the switch S.

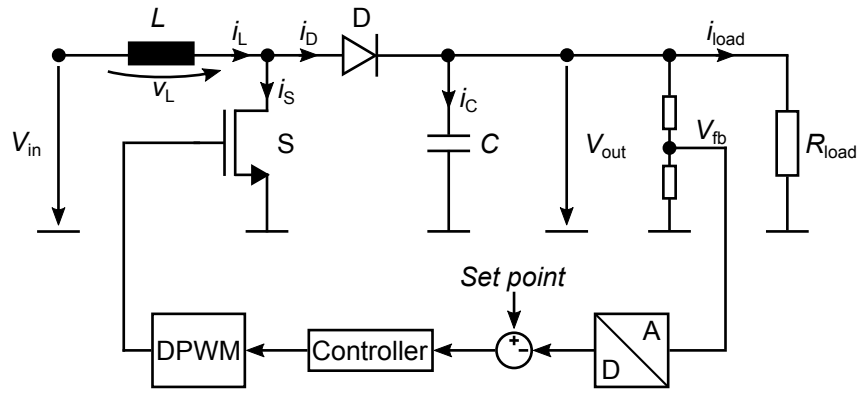

Fig. 3.3: Boost converter with voltage mode control (VMC).

VMC suffers from poor line regulation, as any input voltage change has to be first sensed as output voltage change before it can be counteracted by the control. Further, the output filter of the boost converter adds two poles to the plant and consequently, requires complex compensation of both poles.

Current mode control (CMC) addresses these drawbacks by adding a second control loop, Fig. 3.4. The line regulation gets excellent and the compensation less complex. Since the rising slope of the inductor current, that depends on the input voltage, is used for generating the PWM signal, any input voltage variation is immediately counteracted. Besides, the second control loop moves one plant pole to a non-relevant high frequency range. Thus, only the compensation of one pole is necessary, which simplifies the controller design. In addition, inductor overcurrent can be prohibited by limiting the controller output at no cost.

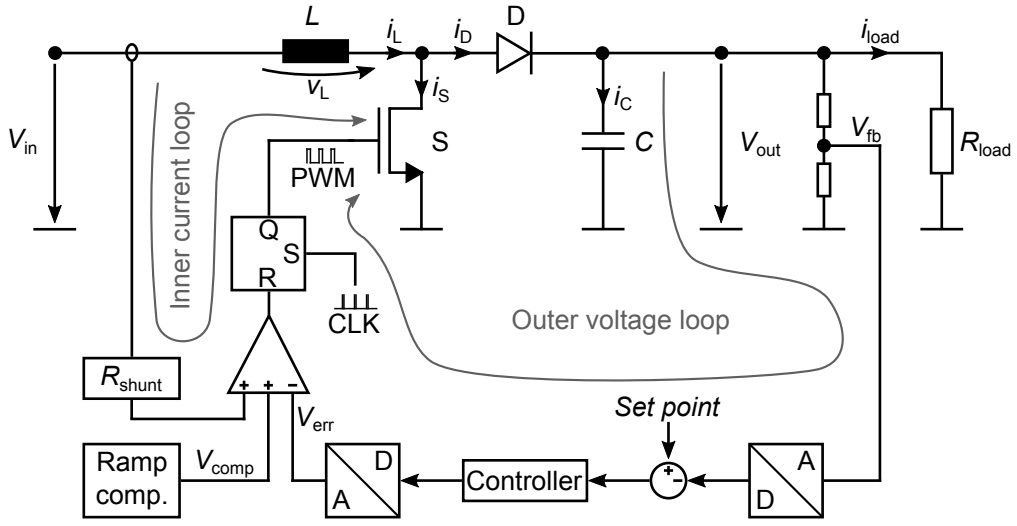

Fig. 3.4: Boost converter with current mode control (CMC).

The basic implementation of CMC is similar to VMC, but the generation of the PWM signal is different, Fig. 3.4. In CMC, the controller command is compared to the inductor current, which is inherently triangular. There are three common possibilities to use the inductor current: in peak CMC the maximum inductor

current value is controlled, in valley CMC the minimum inductor current value is controlled, and in average CMC the average inductor current value is controlled. In case of peak CMC, a flip-flop is set every clock cycle. The comparison of the controller command and the inductor current is used for reseting this flip-flop. Thus, the two control loops are combined: the inner current loop and the outer voltage loop.

In peak CMC, the SMPS can face unwanted output voltage oscillations (subharmonic oscillations) at duty cycles above 50 %. In valley CMC, this can already occur at duty cycles below 50 %. They can be prevented by adding a ramp compensation to the sensed inductor current [32], as indicated by V_{comp} in Fig. 3.4.

Plant Model

For the design of a suitable controller, a plant model is required. In control design, the plant model is preferably built with linear time-invariant systems, because many standard control design methods are applicable to these systems. Unfortunately, there are nonlinear components in a boost converter, i.e. the diode and the switch. Consequently, the plant has to be linearized in its operating point. The PWM switch model of Dr. Vorpérian [33], which replaces the switch-diode combination by linear components, such as a transformer, a current source, and a voltage source, enables the linearization.

The following plant model is valid for a boost converter with CMC and comprises a quadratic term in the denominator, modeling the subharmonic oscillations. Also, the current control loop for the generation of the PWM signal is modeled. The controller command V_{err} (after digital-to-analog conversion) is the input signal and the converter output voltage V_{out} (before analog-to-digital conversion) is the output signal.

$$T(s) = \frac{V_{\mathrm{out}}(s)}{V_{\mathrm{err}}(s)} = \underbrace{\frac{R_{\mathrm{load}}}{R_{\mathrm{shunt}}} \cdot \frac{1}{2M + \frac{R_{\mathrm{load}} T_{\mathrm{sw}}}{LM^2} \cdot \left(\frac{1}{2} + \frac{S_{\mathrm{e}}}{S_{\mathrm{n}}}\right)}}_{K} \cdot \underbrace{\frac{1 + \frac{s}{\omega_{\mathrm{z1}}}}{1 + \frac{s}{\omega_{\mathrm{p1}}}}}_{z1\ \&\ p1} \cdot \underbrace{\frac{1 - \frac{s}{\omega_{\mathrm{z2}}}}{1 + \frac{s}{\omega_{\mathrm{n}} Q_{\mathrm{p}}} + \frac{s^2}{\omega_{\mathrm{n}}^2}}}_{z2\ \&\ p2\ \&\ p3} \tag{3.4}$$

with

$$\omega_{\mathrm{z1}} = \frac{1}{R_{\mathrm{C}} C} \qquad \omega_{\mathrm{p1}} = \frac{1}{C} \cdot \left(\frac{2}{R_{\mathrm{load}}} + \frac{T_{\mathrm{sw}} m_{\mathrm{c}}}{LM^3}\right) \qquad m_{\mathrm{c}} = 1 + \frac{S_{\mathrm{e}}}{S_{\mathrm{n}}}$$

$$\omega_{\mathrm{z2}} = \frac{R_{\mathrm{load}} (1-D)^2}{L} \qquad M = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} \qquad S_{\mathrm{e}} = \frac{f_{\mathrm{sw}} V_{\mathrm{comp,pp}}}{R_{\mathrm{shunt}}}$$

$$\omega_{\mathrm{n}} = \frac{\pi}{T_{\mathrm{sw}}} \qquad Q_{\mathrm{p}} = \frac{1}{\pi (m_{\mathrm{c}} \cdot (1-D) - 0.5)} \qquad S_{\mathrm{n}} = \frac{V_{\mathrm{in}}}{L}$$

It models the behavior of the boost converter for frequencies up to $f_{\mathrm{sw}}/2$ and considers all major influencing parameters of the converter.

The nominal parameters for the boost converter predominantly used in this work are shown in Table 3.1.

Tab. 3.1: Standard parameters in this work.

Parameter	Value
Input voltage	$V_{\text{in}} = 3.5\,\text{V}$
Output voltage	$V_{\text{out}} = 6.3\,\text{V}$
Switching frequency	$f_{\text{sw}} = 500\,\text{kHz}$
Switching period	$T_{\text{sw}} = 2\,\mu\text{s}$
Inductance	$L = 20\,\mu\text{H}$
Inductor equivalent series resistance	$R_{\text{L,eq}} = 100\,\text{m}\Omega$
Capacitance	$C = 20\,\mu\text{F}$
Capacitor equivalent series resistance	$R_{\text{C}} = 10\,\text{m}\Omega$
Load resistance	$R_{\text{load}} = 20\,\Omega$
Ramp compensation voltage	$V_{\text{comp,pp}} = 300\,\text{mV}$
Shunt resistance	$R_{\text{shunt}} = 500\,\text{m}\Omega$

Figure 3.5 shows the bode diagram resulting from the control to output transfer function shown in (3.4).

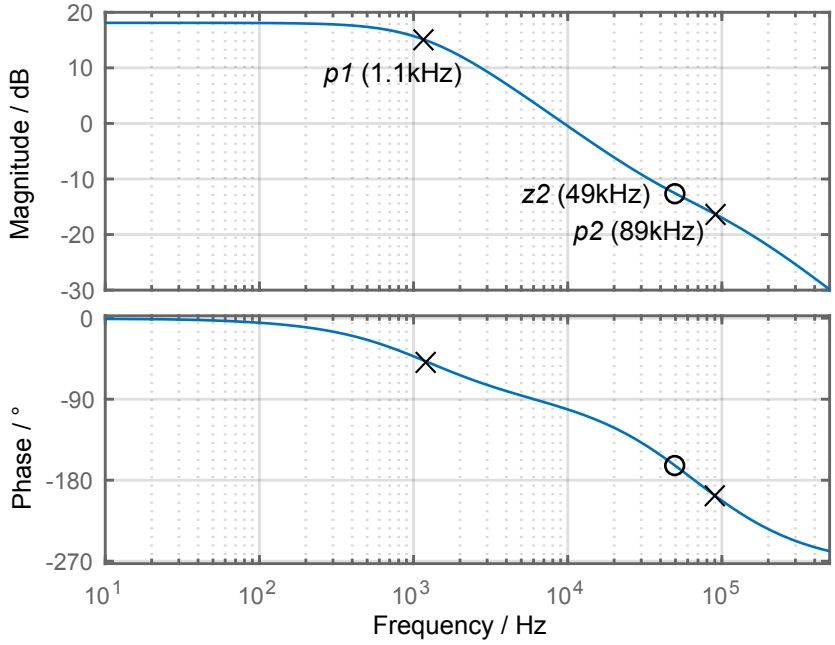

Fig. 3.5: Bode plot of the boost converter transfer function.

The pole frequencies f_{p1} and f_{p2} are marked with x. The zero frequency f_{z2} is marked with o. f_{p3} and f_{z1} lay outside the modeled frequency range and, therefore, are not visible in this diagram.

Right-Half Plane Zero

The second zero f_{z2} is a right half plane zero. RHPZs enhance the amplitude and, simultaneously, increase the negative phase shift of the open loop. It models a behavior, which is specific for boost converters and also other converter topologies, which do not work with continuous energy transfer to the output.

In case of a load step, demanding a higher load current, the controller reacts by enlarging the duty cycle, temporarily. Thus, the inductor current increases. With greater duty cycle the period of conducting switch becomes longer and the period of delivering current to the output capacitor becomes shorter. Consequently, despite the fact that the inductor current has increased, even less charge may be provided to the output capacitor. For a short time, the requested effect (more charge) is opposed to the actual effect (less charge). This behavior corresponds to a RHPZ.

Wrong cause-effect relationships are dangerous in control loops, since they lead to instability. In a boost converter control loop, this instability can occur when the output voltage decreases due to a load step from low to high load. The controller tries to counteract by requesting a higher duty cycle in order to compensate for the output voltage drop and, thus, increases the inductor current. If the duty cycle is greatly increased, current is delivered to the output capacitor only within a short period of time. Consequently, the boost converter does not benefit from the higher inductor current. The output voltage drops even more. Logically, the controller will demand an additional increase of the duty cycle and the period of delivering current to the output capacitor gets even shorter. This may in particular happen for very fast controllers. The control loop can get unstable. The practical solution to prevent this instability is to limit the control bandwidth. Thus, the boost converter gains time to benefit from the increased inductor current and the output voltage rises before the controller counteracts more drastically.

In the frequency domain, this means to choose the crossover frequency of the control much lower than the RHPZ, because the phase lag becomes large at the RHPZ frequency. The maximum crossover frequency $f_{c,max}$ is most commonly chosen not higher than one third of the right-half-plane zero f_{RHPZ}.

$$f_{c,max} = 1/3 \cdot f_{RHPZ} \tag{3.5}$$

3.2 Digital Control

3.2.1 Control Loop Architecture

The digital control loop comprises an ADC, a digital controller, and a unit for generation of a PWM signal. In case of VMC, this unit is most often a digital pulse-width modulation (DPWM), and in case of CMC, a digital-to-analog converter (DAC) is used. The structures are shown in Fig 3.3 and Fig. 3.4. The ADC is used for conversion of the analog output voltage into a digital value, which in turn is used in the digital part for calculation of the control deviation. A digital control algorithm calculates a control command, which is converted directly into the corresponding duty cycle with the help of a DPWM. A DPWM generates a pulse-width modulated signal with a duty cycle correlating to its input. With CMC the controller command is converted by a DAC into a corresponding inductor current command for the inner current control loop.

No matter which control method is used, digital control loops face some challenges, which analog control loops do not. These challenges arise from the time and amplitude quantization associated with the components required for digital control, namely the ADC and the DPWM (or the DAC). This is covered in the next Section 3.2.2. Suitable designs for the ADC and DAC, addressing these challenges, are proposed in Section 4.

3.2.2 Challenges

Dead Times

For stable control, low dead times are necessary. Large dead times reduce the phase of the control loop resulting in a less damped or even unstable control. This is in particular relevant in digital control loops, as there are additional delay sources, contributing to the overall dead time in the loop. The ADC needs time for the conversion of the analog output voltage into a digital value. The same holds for the DAC. These conversion times appear as dead times for the control loop. Another source of a dead time is the calculation time of the controller command.

The relation of dead time T_D, crossover frequency f_c, and phase margin shift $\Delta\varphi$ is:

$$\Delta\varphi = -360^\circ \cdot f_\mathrm{c} \cdot T_\mathrm{d} \tag{3.6}$$

Figure 3.6 shows the phase margin shift as a function of dead time and crossover frequency. An exemplary digital control loop, consisting of a pipeline ADC, requiring 5 µs for conversion and a resistor-string DAC

with 5 µs settling time already reduces the phase margin by 35° at $f_c = 10\,\text{kHz}$. Thus, the control suffers from reduced damping or even instability.

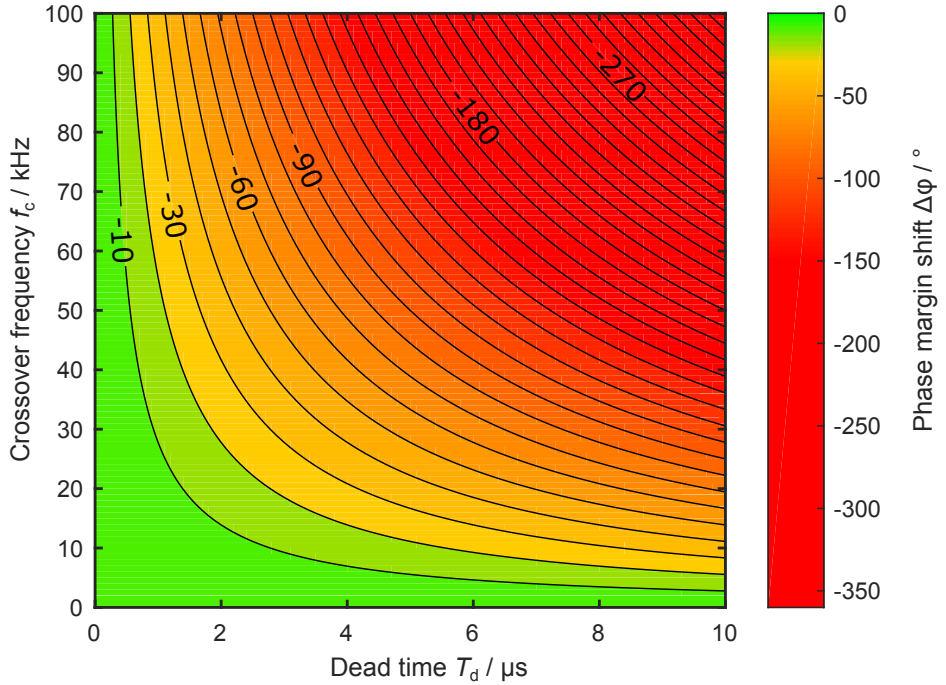

Fig. 3.6: Phase margin shift as a function of the dead time and the crossover frequency of the converter.

It is possible to compensate for some phase margin shift with proper controller design. That is why a phase margin shift of 10° is tolerated in this work as this can be compensated by an appropriate controller design.

Limit Cycle Oscillations

The quantization introduced through the ADC and the DAC can lead to unwanted oscillations, called limit cycle oscillations (LCO). LCO are steady-state oscillations of the output voltage at frequencies lower than the switching frequency of the converter [34]. They are undesirable as both frequency and magnitude of the oscillations are difficult to anticipate. Therefore, LCO consume an unknown part of the specified output voltage margin of the later product and the electromagnetic interference (EMI) is hard to predict.

The ADC quantizes the output voltage. Consequently, there is an analog voltage range with the width of 1 LSB, hereinafter called bin, for each digital value. Also, for the digital set point an analog voltage range defined by its mid-value V_{sp}, the 0-bit-error-bin, exists. Once, the output voltage is located within this bin, the control error is zero. Premise for permanent elimination of any non-zero control error is that there is a DAC value which forces the output voltage to the 0-bit-error-bin, steadily. This premise will be fulfilled

when the DAC resolution referred to the output voltage is higher than the resolution of the ADC referred to the output voltage:

$$Resolution(DAC) > Resolution(ADC) \tag{3.7}$$

Figure 3.7(a) shows what will happen, if this condition is not considered. There is no DAC-value, which corresponds to an analog voltage within the 0-bit-error-bin. That is why the output voltage V_{out} does not stay permanently within the 0-bit-error-bin and LCO arise.

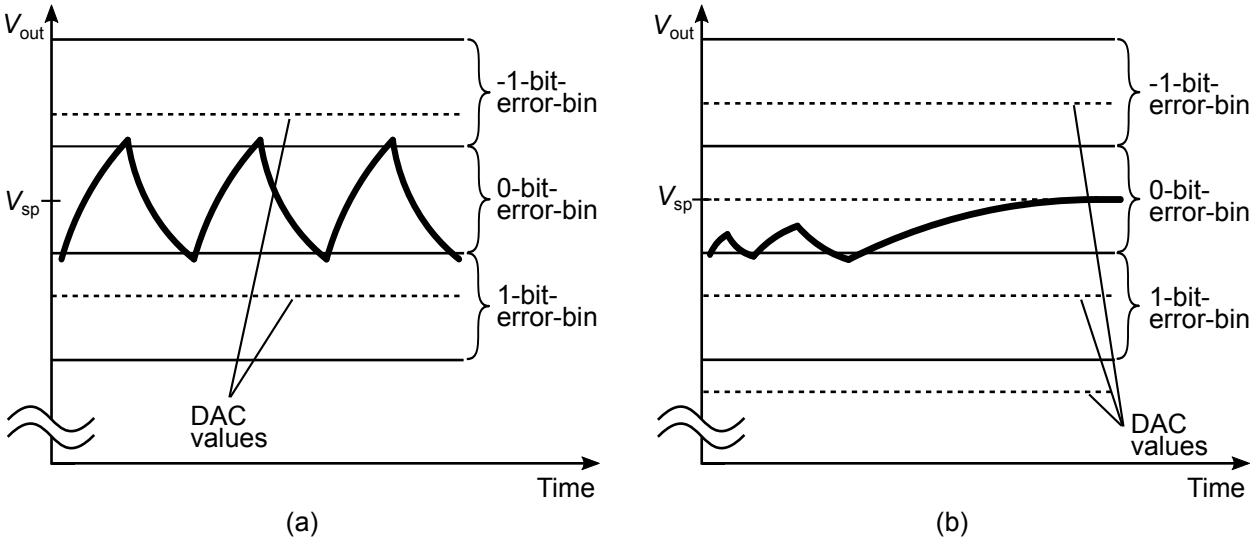

Fig. 3.7: Converter facing (a) LCO due to insufficient resolution and (b) no LCO due to proper resolution choice.

If all conditions are met, the output voltage will stay within the 0-bit-error-bin in steady-state, without limit cycle oscillations, Fig. 3.7(b).

In controllers without integral term, LCO occur regardless of the condition given in Eq. (3.7). To avoid this kind of oscillations the control laws require to have an integral term.

Beside the shown conditions, [34–36] show further special cases, that lead to limit cycle oscillations along with conditions to avoid them.

Controller Windup

The use of an anti-windup structure in the control law is recommended in digital controls. Otherwise, controller windup may occur, resulting in regulation delays and large control deviations [37].

In a digital control loop the controller output is converted into an analog signal by a DAC. This DAC has an operation range with a maximum and a minimum value that can be converted. Thus, it can happen that

the controller demands a value outside of the operation range of the DAC. This is most likely the case for large control deviations. The controller tries to counteract the large control deviation by a large controller command. If this controller command is outside of the operation range, it is ineffective. The output voltage does not move back to the desired value as fast as the controller scheduled it. Thus, a control deviation is present for a long time. Due to the integrating part of the controller, the present control deviation is integrated. Consequently, the controller output value increases further. But the DAC still does not provide a higher analog output voltage. Once the control deviation is counteracted and changes in sign, the large controller output value has to be integrated into the opposite direction in order to get back into the operation range of the DAC. This delaying effect leads to long lasting and huge control deviations.

Controller windup is prevented with only a slight modification of the integrator in a standard controller, Fig. 3.8. The saturation function is the difference to a standard controller. The limits of the saturation in the integrator have to be chosen according to the limits of the operation range of the DAC (or other blocks limiting the controller command). Thus, an integration is stopped once the upper or lower limit of the saturation is reached.

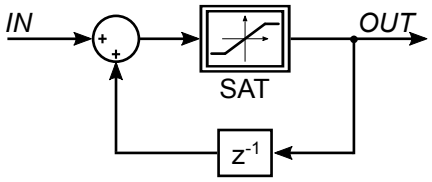

Fig. 3.8: Digital integrator with anti-windup structure.

In [37–39] various other anti-windup controller implementations are shown and discussed.

Monotonicity

In digital control loops, guaranteed monotonicity of ADC and DAC is essential for non-oscillating operation. An ADC is monotonic if, for increasing analog input voltage, the digital output increases, and vice versa. A DAC is monotonic, if for increasing digital input values, the analog output voltage increases, and vice versa. For both, the ADC and the DAC, monotonicity can be examined from the differential nonlinearity (DNL). A $DNL > -1$ guarantees monotonicity. With a voltage V_z corresponding to a digital value Z, and a voltage V_{z+1} corresponding to the subsequent digital value Z+1 the DNL is defined by:

$$DNL = (V_{z+1} - V_z)/V_{LSB} - 1 \tag{3.8}$$

Figure 3.9(a) shows the output voltage behavior of a boost converter with monotonic ADC and DAC. In contrast, Figure 3.9(b) shows the output voltage with non-monotonic ADC. The ADC was modified in a

way, that the transition from value '0' to '1' is non-monotonic. All other value transitions are monotonic. Oscillations arise, which are different before and after the load transient. This confirms that it is hard to predict the amplitude and frequency of the oscillations. Also, a non-monotonic DAC leads to oscillations. Consequently, in order to avoid them ADC and DAC monotonicity is mandatory.

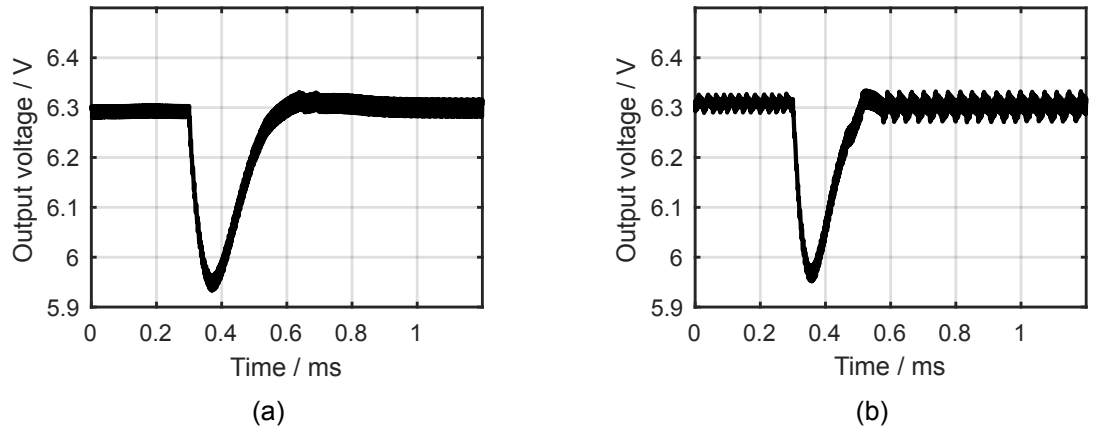

Fig. 3.9: Simulation of a boost converter with (a) monotonic ADC and (b) non-monotonic ADC.

4 Design of Digital Control Loop Blocks

An analog PI controller can be built with a Type-II compensation network, Figure 4.1. A PI controller is a common controller type, which provides corrective actions based on a proportional and an integrating term. The analog Type-II compensation controller generates the controller command, in terms of the error voltage V_{err}, from the converter output voltage V_{out} and the control set point V_{sp}. The implementation of the Type-II compensation controller comprises only few resistors and capacitors. Often, in analog control more complex controllers are used, which comprise more passives [40]. For illustration of the variation of the transfer behavior of the analog controller, it is assumed that R_1, C_1, and C_2 vary by $\pm 30\,\%$, unpredictably. According to Section 5.1, the assumed variation is moderate and may be higher in actual analog designs.

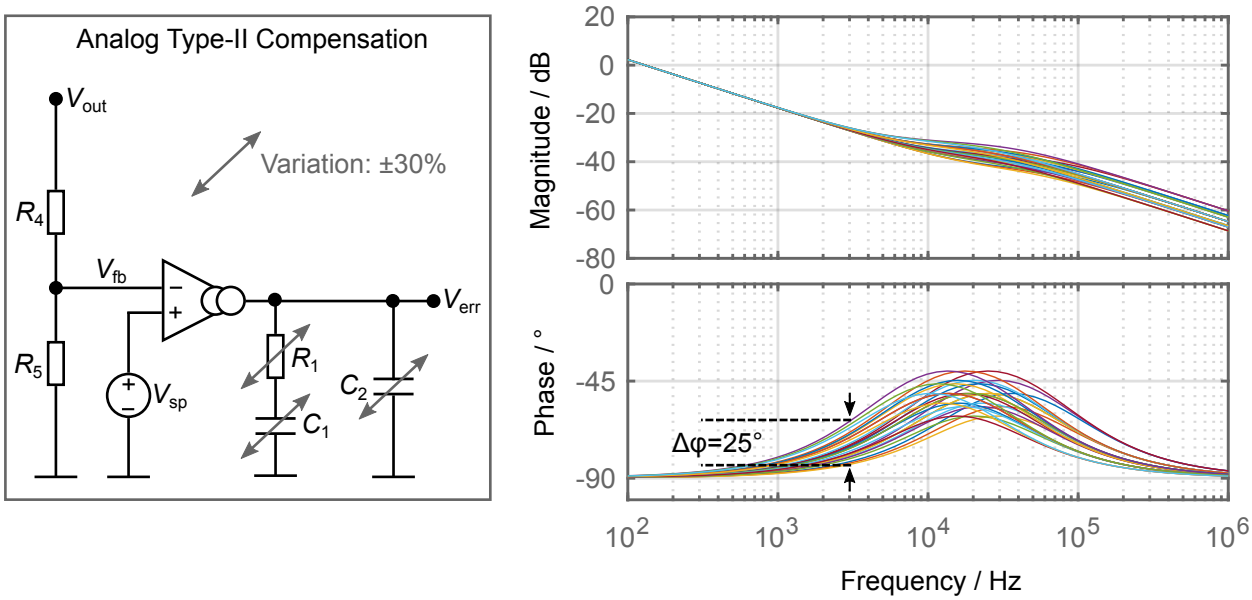

Fig. 4.1: Analog Type-II compensation controller and its bode plot with 30 % parameter variation of the resistor R_1 and the capacitors C_1 and C_2.

If a control with a bandwidth of 3 kHz is designed, solely the analog controller contributes to a phase margin variation with 25°, Fig. 4.1. This variation has to be added to the variation caused by the converter passives, which is discussed in Section 5.1. Therefore, the overall variation becomes immense. In contrast, a digital controller achieves a defined and known controller transfer behavior. Consequently, the controller does not add to the overall phase margin variation. Further, digital control enables parameter identification of

the converter passives to be performed, which is shown in Section 5. Thus, the overall transfer behavior becomes well-known.

In addition to this advantage of significantly lower parameter variations in a digital control loop, digital controls benefit from numerous other advantages, such as improved control performance, great flexibility, and increased reliability, compare Section 2.2.

This work concentrates on digitally controlled SMPS fabricated as ICs in standard silicon technologies. In particular, digital control in boost and buck converters is realized with an ADC and a DAC for current mode control, and with an ADC and a DPWM for voltage mode control, respectively. The concepts presented in prior art are most often targeted for relatively low output voltages, Fig. 4.2. In contrast, this work is aimed to provide solutions also for higher voltages. This higher voltage range comes along with particular design requirements. The major difference is, that the digital resolutions are required to be higher, i.e. the output voltage quantization step is required to be smaller. The output voltages in such converters are scaled down with the help of feedback dividers, as formed by R_4 and R_5 in Fig. 4.1. Feedback dividers scale down the resolution, too. For example, a feedback divider ratio of 1:5 is required in a 6.3 V output voltage converter, which is the output voltage of the boost converter shown in Section 6. If the resolution of the ADC is designed to 10 mV/LSB, the effective output voltage resolution is insufficiently low (5·10 mV/LSB = 50 mV/LSB). With high ADC resolution, a high resolution of the DAC is necessary for avoiding LCO, see Section 3.2. Further, due to the large output voltages high resolution of the DAC is required for accurate output voltage regulation.

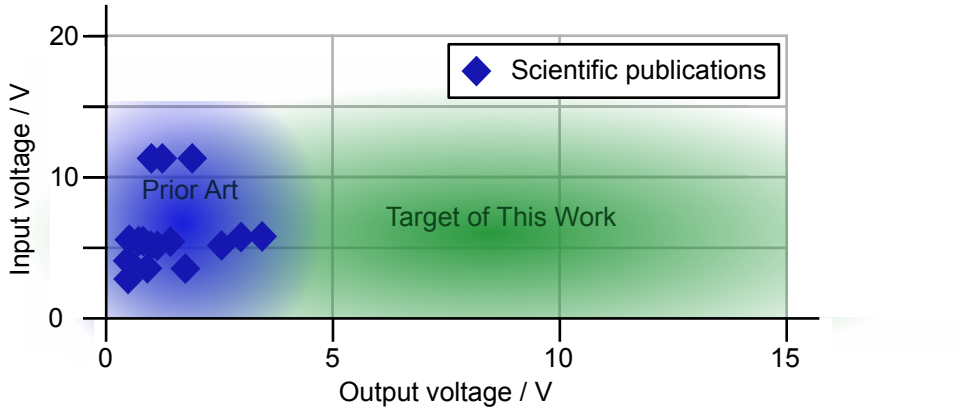

Fig. 4.2: Prior scientific publications of SMPS with digital control comprising an integrated ADC and DAC.

This work shows control loop block solutions addressing the common SMPS challenges of small size and high integration. Further, for the demanding higher voltage applications, such as automotive, high resolution ADC and DAC designs are proposed. In Section 4.1, a Delta-Sigma ADC is shown and a delay line ADC with live-tracking is introduced. Section 4.3 presents a DPWM, a R-2R DAC, and a high resolution charge

pump DAC. Finally, a comparison to analog control is shown in Section 4.4.

4.1 Analog-to-Digital Converter

The ADC samples the output voltage of an SMPS and produces a corresponding digital signal. The conversion time of the ADC appears as delay in the control loop. According to Section 3.6, this conversion delay is aimed to be minimal. Also, monotonic transfer characteristic is necessary to prevent output voltage oscillations. The higher the resolution of the ADC, the more accurate output voltage deviations from the set point can be detected and eliminated permanently. High sample rates support high switching frequency converters. They enable sequencing, which allows to operate several control loops simultaneously or sense multiple signals with only one ADC. The sample rate of the ADC in an SMPS is typically chosen equal to the converter switching frequency. Then, the high-frequent output voltage ripple, which is caused by the switching behavior of the converter, is filtered. The high frequency information is non-relevant for the control. Sampling at frequencies higher than the switching rate, called multisampling, can also be practiced in order to reduce DPWM delays [41, 42]. When multisampling is applied, the injected high-frequency disturbances have to be filtered in the digital part avoiding malfunction of the closed-loop system. Allowing for higher sampling rates than the converter switching frequency is further beneficial for parameter identification, see Section 5.

In the following, converter architectures for analog-to-digital conversion are discussed. It is proven that a standard Delta-Sigma ADC with small area effort provides good resolution at adequate conversion time and, thus, is well suited for analog-to-digital conversion in medium bandwidth converters, e.g. boost converters. Furthermore, a delay line ADC with live-tracking window concept is introduced, providing high resolution at high sampling rate with small conversion time. Consequently, it supports likewise high-bandwidth controls with its excellent performance.

4.1.1 Converter Architectures

Digital control requirements, i.e. high resolution, monotonicity, and small conversion times at the same time, are opposed to many other applications' requirements. For example, in sensor signal processing the conversion time of the ADC is of minor interest, whereas high resolution is important. Various ADC architectures are available for these applications: pipeline ADCs and successive approximation ADCs, which provide high resolutions but suffer from slow conversion times. Flash ADCs, which operate with short conversion times but are limited in resolution, are required in other applications, like radar and optical communication.

Despite standard ADC architectures [43–46], dedicated architectures for digital control in SMPS were proposed. [47–49] explore voltage controlled oscillator based architectures. The converter output voltage is used for varying a ring oscillator frequency. This ring oscillator frequency, in turn, is converted into a digital signal with the help of multiple counters and consequently, requires plenty of chip area in an integrated solution. In [47] the absolute output voltage is used for the ring oscillator input, which requires the ADC to cover a wide voltage range. In [48, 49] the wide input voltage requirement is relaxed by using the window concept, which is explained below. This window concept is also used in [45, 46], since the reference voltage of a flash converter equals the set point of the control in these proposals. Consequently, the difference of the set point of the control and of the output voltage is converted. Delay line based ADC architectures [25, 50–54] do not include area-intensive counters. They also make use of converting only the difference of set point and output voltage. The design effort of delay line ADCs is reasonable, as inverters are the basic elements and are inserted multiple times. Inverter based ADC architectures are well suited for fulfilling the requirement of short conversion times in digital controls.

Window Concept

Unlike standard full-range analog-to-digital conversion, in the window concept the output voltage is solely converted within a small voltage range (= window) around the control set point, Fig. 4.3. This is suitable in stable controls, as the output voltage stays within small distance from the set point at all times and thus, the window range can be small. Therefore, high output voltage resolution can be achieved without a high-performance ADC, that would be necessary for high resolution over the full voltage range in conventional operation. The window range is typically chosen to cover the highest output voltage deviations of the application. Unfortunately, the use of the window concept is disadvantageous when parameter identification coming with great voltage variations before operation is applied to the SMPS. Then the output voltage information is lost due to the small conversion range.

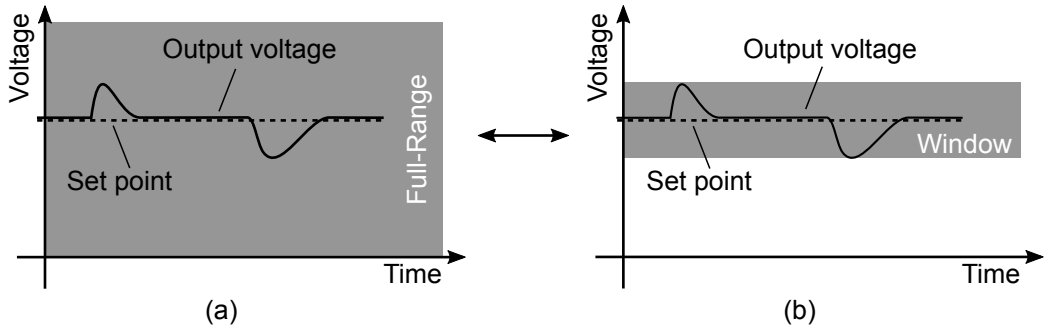

Fig. 4.3: Analog-to-digital conversion: (a) standard conversion and (b) conversion with window concept.

4.1.2 Delta-Sigma Analog-to-Digital Converter

Delta-Sigma ADCs reach high resolutions due to their oversampling nature. They benefit from the possibility of noise shaping and qualify for use in integrated digital controls due to their simple architecture and small chip area required for integration. [55] presents a digitally controlled buck converter with Delta-Sigma ADC operating at 100 kHz switching frequency. In [56, 57] a Delta-Sigma based ADC is extended by two voltage controlled oscillators in order to use the window concept in a digitally controlled buck converter.

Design

Figure 4.4 shows the block diagram of a Delta-Sigma ADC. In the modulator, the analog input voltage is converted into a high-frequent digital bitstream whose average equals the analog input voltage. The primary task of the decimation filter is to determine the input voltage from the high frequent bitstream in form of a digital value. Further, it is supposed to suppress high frequency noise.

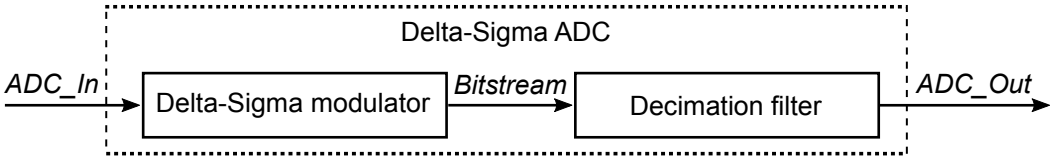

Fig. 4.4: Delta-Sigma ADC structure.

A (first order) Delta-Sigma modulator consists of a subtractor, followed by an integrator, a comparator, and a DAC, Fig. 4.5. The input signal *ADC_In* is first compared to the latest output value (*Bitstream*). The resulting difference is integrated. The integrated signal, in turn, is converted into a boolean signal with the help of a comparator. The high frequent sequence of the boolean values is the bitstream, whose average matches the analog input voltage. Higher modulator and decimation filter orders can be used for higher resolutions.

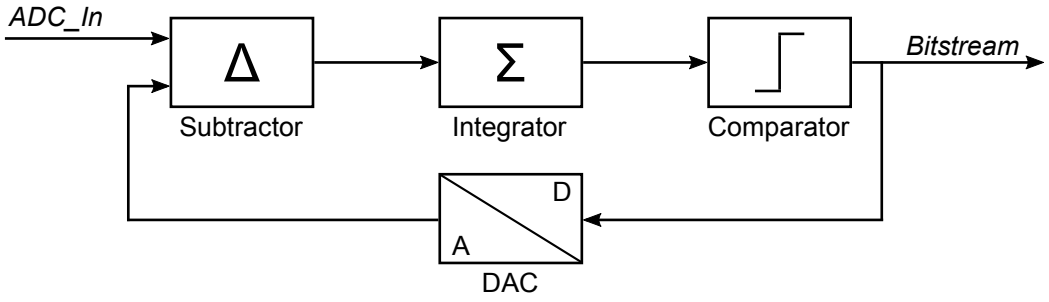

Fig. 4.5: First order Delta-Sigma modulator.

A cascaded integrator comb (CIC) filter is implemented for decimation. It is preferably used, as it can be built with only simple adders and memories, which allows for small chip area in integrated solutions. The

filter is composed of an integrator, followed by a decimation stage, which reduces the sample rate, and a differentiator, which works at the reduced sample rate, Fig. 4.6.

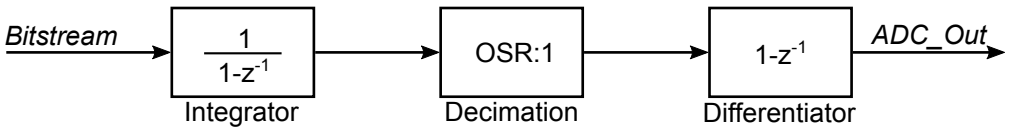

Fig. 4.6: First order Delta-Sigma decimation filter.

The transfer function of a first order CIC filter with an oversampling ratio $OSR = f_{\text{in}}/f_{\text{out}}$, where f_{in} is the high input sample rate and f_{out} is the low output sample rate, is:

$$ADC\_Out(z) = Bitstream(z) \cdot \frac{1}{1-z^{-1}} \cdot [1-z^{-\text{OSR}}] \tag{4.1}$$

Conversion Time

The overall conversion time of Delta-Sigma converters is dominated by the calculation time of the decimation filter. The calculation time of the modulator is of minor interest, as it works at much higher frequencies than the decimation filter. In the decimation filter only the differentiator operates at low frequency. Consequently, the calculation time of the decimation filter is dominated by the calculation time of the differentiator $D(z)$. The group delay describes the calculation time. It will be exemplary calculated for a first order CIC filter, as shown in Fig. 4.6, with the output sample rate T_{s}. The differentiator transfer function $D(z)$ is expressed by:

$$D(z) = 1-z^{-1} = 1-e^{-j\omega T_{\text{s}}} = e^{-j\omega T_{\text{s}}/2} \cdot (e^{j\omega T_{\text{s}}/2} - e^{-j\omega T_{\text{s}}/2}) = e^{-j\omega T_{\text{s}}/2} \cdot (2j \cdot \sin(\omega T_{\text{s}}/2)) \tag{4.2}$$

The group delay T_{group} is defined by $T_{\text{group}} = -\frac{d\varphi}{d\omega}$. The phase of the differentiator φ_{D} derived from (4.2) is:

$$\varphi_{\text{D}}(\omega) = 90^{\circ} - \omega T_{\text{s}}/2 \tag{4.3}$$

Consequently, the group delay T_{group} of a first-order CIC filter is calculated by:

$$T_{\text{group}} = -\frac{d\varphi_{\text{D}}}{d\omega} = T_{\text{s}}/2 \tag{4.4}$$

It can further be shown that the group delay of a K^{th}-order CIC filter is calculated by $T_{\text{group}} = K \cdot T_{\text{s}}/2$.

For sufficient suppression of noise, the order of the decimation filter is chosen an order higher as the modulator [58]. The oversampling ratio and the order of modulator and decimation filter define the resolution of the ADC. The higher the orders and the higher the oversampling ratio, the higher the resolution. Since Equation (4.4) indicates that the conversion time also increases with these parameters, high resolution and low conversion time cannot be obtained, simultaneously. A trade-off between resolution and conversion time is investigated in this work and shown in the following.

Experimental Results

A second order Delta-Sigma modulator is used to study for this work. The decimation filter is chosen to a third order CIC filter. The maximum input sample rate for the available ADC is 8 MHz. For a 500 kHz-converter the oversampling ratio is 16.

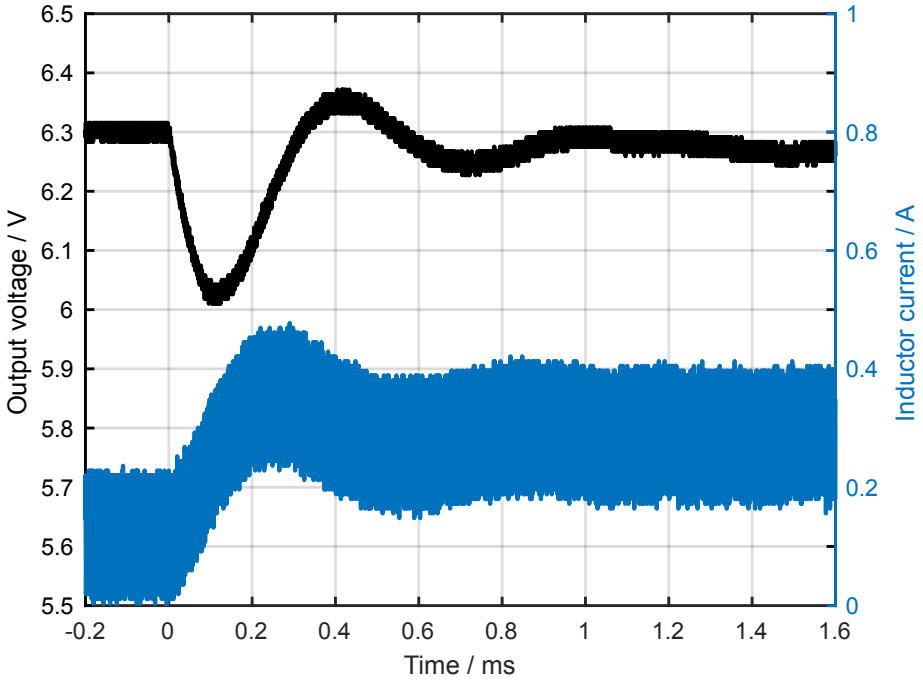

Fig. 4.7: Load step response of a boost converter with Delta-Sigma ADC proving closed loop stability.

This configuration of the Delta-Sigma ADC leads to 9.5 effective number of bits, which equals an voltage resolution of 2.5 mV, and a conversion time of 3 µs. According to Fig. 3.6 this leads to 10.8° negative phase shift in a control loop with 10 kHz crossover frequency. Recent automotive boost converters' crossover frequencies are in between 1 kHz and 10 kHz, because they suffer from the RHPZ, see Section 3.1. Consequently, the presented Delta-Sigma ADC is suited for use in these boost converters, which is confirmed by

the closed-loop load step response measurement of such a boost converter, Fig. 4.7. The experimental setup for this measurement is shown in Section 5.4 and the boost converter parameters are given in Table 3.1.

As the main limitation of Delta-Sigma converters for use in SMPS is the high conversion time, the decimation filter order can be reduced. Then, the conversion time becomes smaller. With a second order decimation filter it is reduced to 2 µs and the effective number of bits is still 7.5 bits, which equals a voltage resolution of 10 mV. However, this approach is limited as for high voltage boost converters feedback dividers are used, which scale the resolution. A feedback divider ratio of 1:5 would lead to only 50 mV effective converter output voltage resolution. Further reducing the decimation filter order lowers the conversion time, but is not reasonable, as the effective number of bits will drop to 3.75 bits (first order decimation filter) [59].

4.1.3 Delay Line Analog-to-Digital Converter

Delay line ADCs stand out due to their excellent resolution and low latency. The high resolution is offered with the help of the window concept. The low latency is a result from their time-to-digital architecture. They provide inherent monotonicity because of their sequential signal propagation [50]. Time-to-digital converters, like the delay line ADC, mainly rely on digital components, which are subject to miniaturization due to technology scaling. Consequently, these converter types show great potential for growing future use [60, 61].

Design

The proposed delay line ADC comprises three low complexity circuits: an operational transconductance amplifier (OTA), a delay stage, and a conversion stage, Fig. 4.8.

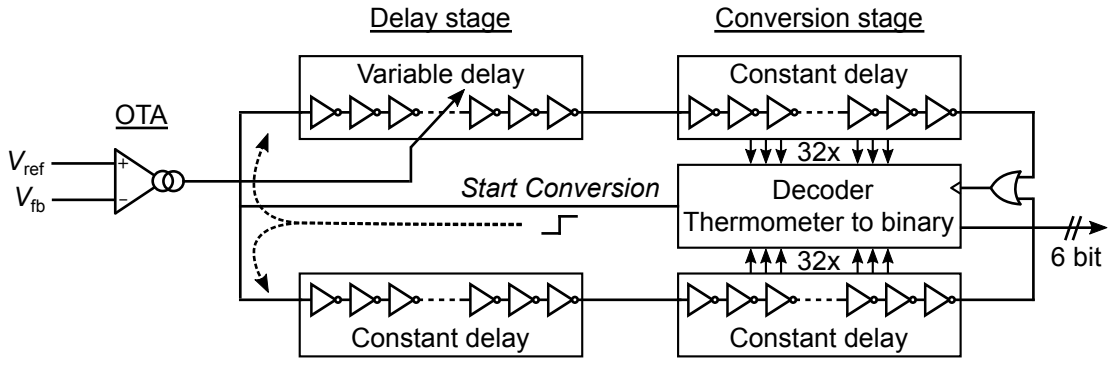

Fig. 4.8: Block diagram of the delay line ADC.

The input OTA provides a bias current, which is proportional to the difference of the reference V_{ref} and the output voltage after feedback divider V_{fb}. The delay stage is composed of one delay block with constant

delay and another which provides variable delay inversely proportional to the bias current generated by the OTA. The conversion stage includes two delay blocks with constant delay and state evaluation outputs for the decoder. The delay blocks are composed of multiple equal current controlled double inverters, Fig. 4.9.

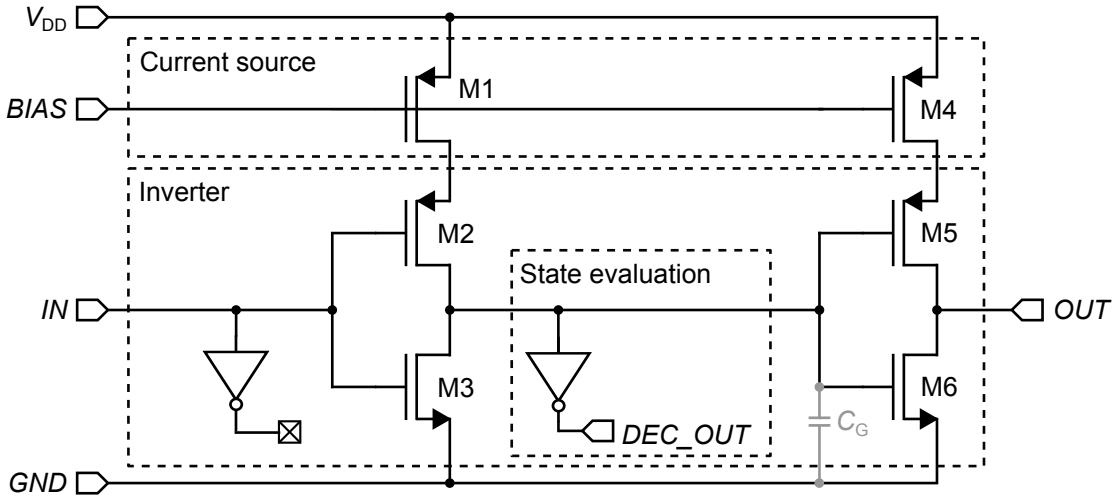

Fig. 4.9: Design of a current controlled double inverter.

In the current controlled double inverter, a step signal applied to the *IN*-port propagates through the two inverters. A high-to-low transition at the *IN*-port will be inverted in the first inverter, whereas the inversion speed is controlled by the pmos current source (M1 and M4, respectively). A temperature compensated biasing allows for constant delay times. By variation of the biasing the delay time can be manipulated, as required in the delay block of the delay stage. In contrast, a low-to-high transition at the inverter input flips the inverter output without speed control, as there are no nmos current sources. They are not used for reasons of area minimization. Still, through the pmos current sources the propagation speed can be controlled.

In the presented design, the delay blocks in the delay stage consist of 144 double inverters each. In the conversion stage, a delay block includes 32 double inverters. The core of the delay line ADC is a decoder which first generates a step signal triggering a conversion. Then, it evaluates the inverter states in the conversion stage and converts the obtained 64 bit thermometer code to 6 bit binary code. The latency and maximum sample rate of the delay line ADC depend mainly on the number of inverters in the delay blocks.

Operating Principle

An analog-to-digital conversion is started by a step signal *StartConversion*, see Fig. 4.8. This signal propagates through the delay stage: with constant delay in the lower delay block, and with variable delay in the upper delay block. The variable delay is inversely proportional to the difference of reference voltage V_{ref}

and output voltage after feedback divider V_{fb}. In case that reference and output voltage are equal the delays in the upper variable delay block and in the lower constant delay block match. Otherwise, the step signals propagate with different speed. The delay line ADC is able to work with the window concept. This is achieved, when the set point of the control equals the reference voltage. Thus, the delay block propagation speed depends on the difference of the set point of the control and the output voltage. After propagating through the delay stage, the signals reach the conversion stage which is required for the evaluation of the propagation delays. The faster signal triggers the evaluation of the propagation delays by the decoder. The decoder obtains a thermometer coded signal from the inverter states in the delay blocks, and converts it to a binary output signal.

The maximum conversion time of the delay line ADC equals the duration of the step signal propagation in the constant delay block path. The conversion time can be lower, if the step signal propagates through the variable delay path with higher speed, but it will never be larger.

Live-Tracking

The presented solution enriches the standard window concept by a live-tracking functionality, which is proposed in this work, Fig. 4.10. This is helpful for applying parameter identification, increasing the effective output voltage resolution, reducing nonlinearity-effects of the delay line ADC, and minimizing the converter power consumption and chip area.

The output voltage varies over a wide voltage range when applying parameter identification during converter startup. As standard window concept ADCs convert the output voltage solely around the set point of the control, which is zero before operation, they are not suitable. Full-range ADCs get around this problem, but are expensive. Therefore, the use of a live-tracking window ADC is proposed, which tracks the output voltage over a wide operation range, maintaining window concept operation.

Live-tracking allows for further shrinking the conversion range of the ADC. Thus, the number of bits can be spread over a smaller voltage range increasing the output voltage resolution without area or latency penalty. Alternatively, the chip area and the converter power consumption can be reduced, while keeping the effective output voltage resolution.

With live-tracking the window is not linked to the set point, permanently. The reference voltage and the set point of the control may differ, temporarily. When deviations from the set point occur, the output voltage is instantly tracked by the ADC, Fig. 4.10. Consequently, the window can even be reduced to a range smaller than the maximum output voltage deviations of the converter. This is useful for applications with unknown load steps, leading to unpredictable output voltage deviations or if the initial output voltage is unknown and

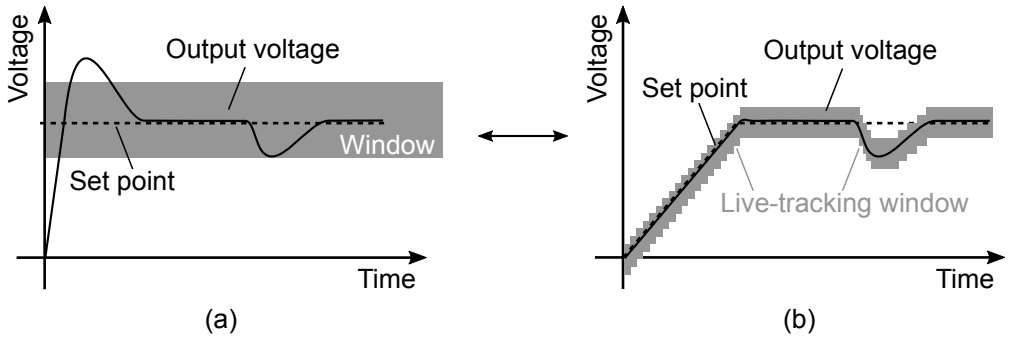

Fig. 4.10: Analog-to-digital conversion: (a) standard window concept and (b) window concept with live-tracking.

needs to be detected. For this functionality and for converter soft-start, a high 1.33 MHz bandwidth R-2R DAC, which is chosen because of its small implementation area, generates the reference voltage V_{ref} for the analog-to-digital conversion, compare Fig. 4.8. This DAC has to provide high bandwidth in order to shift the reference voltage within one conversion period. 95 % of the final reference voltage is reached after 350 ns with a 1.33 MHz DAC when shifting the reference voltage. Thus, the reference voltage is updated in time before the next conversion in a 2 µs-switching frequency converter. In a basic implementation, it becomes active once a control deviation of $\pm$16 LSB occurs, Fig. 4.10. The $\pm$16 LSB boundary ensures stable control as it does not react to minor deviations. The reference voltage V_{ref} is offset by -16 LSB or +16 LSB, respectively, before the next ADC conversion starts. The controller is notified and compensates the newly measured control deviation by adjusting the offset at the beginning of the next ADC conversion.

Experimental Results

Figure 4.11 shows the measured transfer behavior of the delay line ADC without live-tracking functionality activated. The reference voltage of the delay line ADC is $V_{\text{REF}} = 530\,\text{mV}$, constantly. Consequently, the digital value '0' can be found at this voltage. The effective output voltage resolution of 0.5 mV is measured at the same value, as this value describes the zero-error-bin of the ADC. This high resolution enables the usage in converters with higher output voltages than prior art, compare Fig. 4.2. The transfer function is strictly monotonic, which is mandatory in control loops, and nonlinear. The nonlinear transfer behavior is caused by the inversely proportional correlation of bias current I_{bias} and the delay T_{D} of the inverters in the delay block:

$$T_{\text{D}} = C_{\text{G}} \cdot \frac{V_{\text{DD}}}{I_{\text{bias}}} \tag{4.5}$$

The delay results from charging the parasitic capacitance C_{G}, composed of the gate capacitances of the

subsequent inverters, with constant bias current, Fig. 4.9. In order to avoid this nonlinearity, [48] shows a subthreshold biased ring oscillator structure with linear bias current dependency.

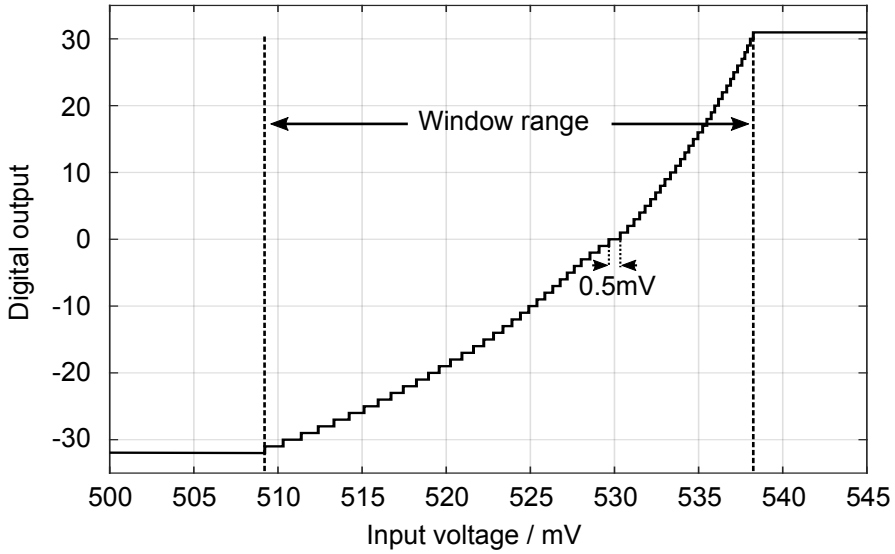

Fig. 4.11: Measured delay line ADC transfer function with $V_{\mathrm{REF}} = 530\,\mathrm{mV}$ (disabled live-tracking).

The digital signal from the ADC can be used directly (without correction) in the digital control loop. In this case, the open loop gain varies as a function of the output voltage. For small output voltages, the gain is small. And for high output voltages, the gain is higher. Alternatively, the digital values can be corrected with the help of a correction formula or a look-up table based correction. With such an approach the nonlinearity of the transfer behavior is corrected, but the resolution still varies: The resolution is fine at high input voltages and coarse at low input voltages, which is not a limitation for digitally controlled SMPS.

Figure 4.12 shows the 90 ns conversion time of the delay line ADC. The ADC *Start Conversion* signal triggers the analog-to-digital conversion. The ADC *Conversion Ready* signal indicates a finished conversion. Consequently, the delay in a double inverter is approximately 510 ps. A maximum sample rate of 9.5 MSps was measured and can be confirmed theoretically by the conversion duration (90 ns) plus reseting duration (16 ns): $T_{\mathrm{sample}} = 1/(90\,\mathrm{ns} + 16\,\mathrm{ns}) = 9.43\,\mathrm{MSps}$.

Closed loop measurement results can be found in Section 6.

Comparison to Prior Art

Table 4.1 shows a comparison of the presented delay line ADC to prior art. The number of bits, the effective resolution, and the high dynamic conversion range are superior to the other ADCs and allow for use of the ADC in high-voltage applications. In these applications resistor feedback dividers are used for sensing the output voltage. These resistor feedback dividers scale the resolution. The higher the feedback divider ratio,

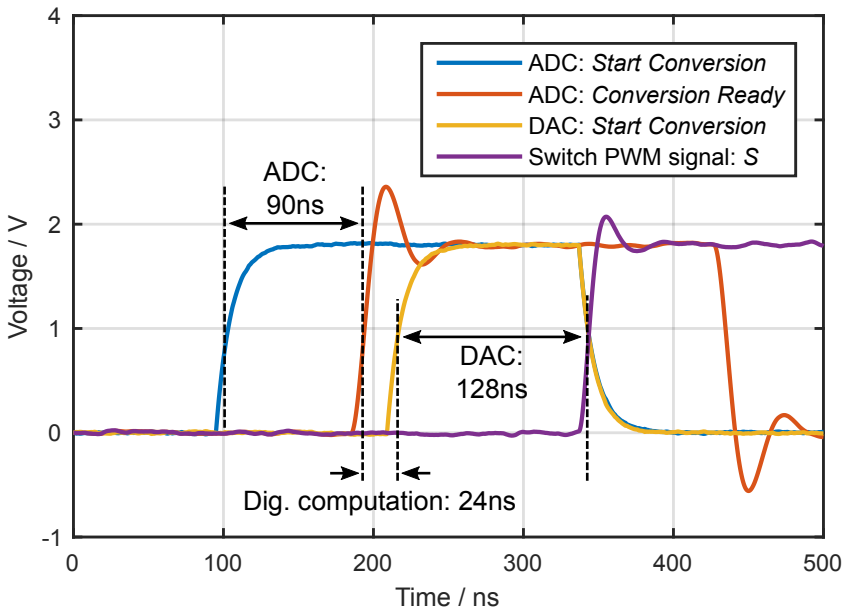

Fig. 4.12: Measured delay line ADC latency.

the larger the output voltage quantization step is. Thus, high ADC resolutions are required. With a feedback divider ratio of 15:1, still, a comfortable effective output voltage resolution of 7.5 mV is achieved in a 15 V output voltage converter with the presented delay line ADC. This resolution is 20x higher than in the state-of-the-art. The dynamic conversion range is more than 3x larger than in prior solutions. This is essential for parameter identification. Both, sample rate and conversion time enable high-bandwidth controls for SMPS.

Tab. 4.1: Comparison of the proposed delay line ADC and prior art.

	[50]	[62]	[52]	[54]	[51]	**This Work**
Number of Bits	3.1 bit	4 bit	3.1 bit	3.1 bit	3.1 bit	**6 bit**
Voltage Resolution	53 mV	12.5 mV	20 mV	>15 mV	10 mV	**0.5 mV**
Sample Rate	1 MSps	16 MSps	1.5 MSps	10 MSps	1 MSps	**9.5 MSps**
Conversion Time	750 ns*	62.5 ns	150 ns	<50 ns	420 ns	**90 ns**
Dyn. Conversion Range	360 mV	200 mV	180 mV**	160 mV**	90 mV	**1.2 V**

*Extracted from timing diagram. **Extracted from figure.

In conclusion, the presented solution provides superior resolution over a wide dynamic conversion range and, therefore, enlarges the application range of conventional delay line ADCs to high output voltage, high bandwidth converters with digital control.

4.2 Digital Controller

An advantage of a digital controller, also referred to as a compensator, in comparison to an analog controller is that there are no passive devices, hence, no parameter variations, as outlined in the beginning of Section 4. In analog control, these parameter variations complicate the control design and require a worst-case approach with safety margins. Further, flexibility is higher in digital control as controller coefficients can be altered with low effort. This makes it much easier to implement advanced controls or autotuning.

The digital controller calculates the controller command on the basis of the control deviation. It can be designed either with quasi-continuous design or with direct digital design approaches. Ragazzini compensation controllers or dead beat controllers are developed with the direct digital design approach, where a controller is designed directly in the digital domain [39, 63]. Alternatively, in the quasi-continuous controller design, an analog controller design forms the basis. Once this analog controller is found with known analog design methods it is converted into a digital controller using the Laplace-to-Z correspondence:

$$z = e^{sT_\mathrm{s}} \rightarrow s = \frac{1}{T_\mathrm{s}} \ln(z) \tag{4.6}$$

A digital controller, which is converted with this correspondence, behaves similar to the corresponding analog one in the frequency range much smaller than the Nyquist rate $f_\mathrm{Nyquist} = 2/T_\mathrm{s} = f_\mathrm{s}/2$. The Laplace-to-Z correspondence is of nonlinear characteristics. Thus, a controller, calculated from the correspondence of (4.6), is non-linear and its implementation requires excessive computational effort due to complex mathematical operations. Therefore, a linear correspondence is preferred to obtain linear controllers. There are various linear approaches for the transformation: Euler methods, bilinear transformation, and pole-zero matching. [64] recommend to use bilinear transformation for Type-II compensation, which is the analog realization of a PI controller, and pole-zero matching for Type-III compensation, which is the analog realization of a PID controller.

Figure 4.13 shows three digital PID control law implementation with comparable hardware effort, which are the parallel, the direct, and the cascaded implementation. Any implementation of the control law is subject to variations of its transfer function due to coefficient quantization. Coefficient quantization arises due to the limited number of bits used for storing the coefficient. In general, the higher the number of bits used for the coefficients, the less the variation of the transfer function. A detailed analysis of the variation of the transfer function depending on the coefficient resolution and implementation form is beyond the scope of this work. In [65] such an analysis is shown for the aforementioned implementations.

In order to avoid control delays due to controller windup any of the implementation forms has to be implemented with anti wind-up structure, see Section 3.2.2.

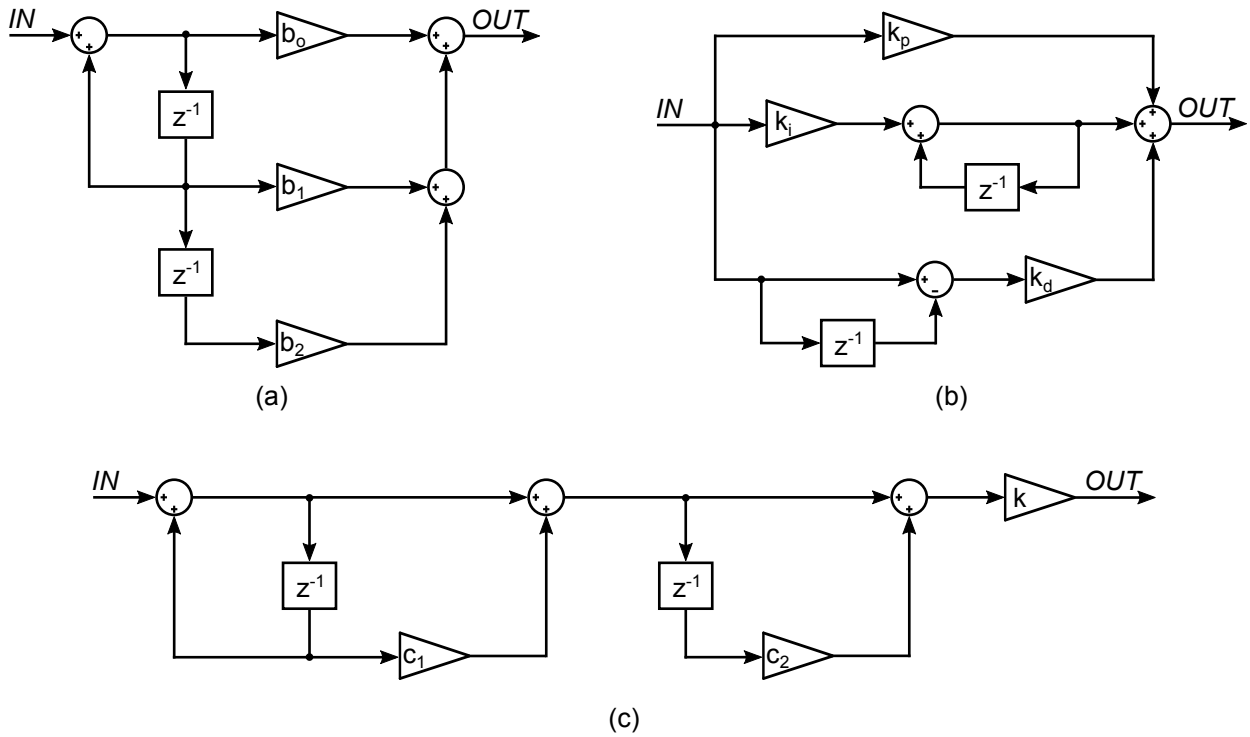

Fig. 4.13: Digital PID controller forms: (a) parallel implementation, (b) direct implementation, and (c) cascaded implementation.

4.3 Digital-to-Analog Converter

A digital-to-analog conversion is required for processing the controller command in a digitally controlled SMPS. Either it is directly converted into a PWM signal or first converted into an analog voltage and then converted into a PWM signal in a second step. High resolution of the DAC is necessary for accurate output voltage regulation and for avoiding limit cycle oscillations. Low conversion times are essential for stable control. Monotonicity is required for oscillation-free output voltage behavior in digital control for SMPS.

This work shows that a hybrid DPWM architecture is an appropriate solution for VMC converters. Alternatively, two architectures for digital-to-analog conversion are considered. A R-2R DAC qualifies for use in digital control loops due to its low implementation effort and repeated basic elements. It is derived in this work, which resolution is achievable without loosing guaranteed monotonicity. A charge pump DAC design is proposed in this work that provides very high resolution.

4.3.1 Converter Architectures

One option for the digital-to-analog conversion is the direct conversion into a PWM signal, called digital pulse-width modulation. Standard topologies for conversion of a digital value into an analog voltage are

the resistor string architecture with its low conversion time but high area effort (2^N resistors) for N-bit resolution, the binary weighted resistor architecture which tends to be non-monotonic with high resolution, and the current steering architecture with its high current source matching requirement.

All architectures allow for further improvement of the resolution by dithering [34, 45, 47, 64, 66] and Delta-Sigma approaches [54, 67, 68].

4.3.2 Digital Pulse-Width Modulation

The digital pulse-width modulation signal generation reduces the number of analog circuit components, as the DPWM signal is built in the digital domain, directly. Most often, DPWM is used together with VMC as there is no need for a digital representation of the inductor current in this control method. Contrarily, in CMC the use of a DPWM is less likely, because a low latency, high-bandwidth inductor current analog-to-digital conversion would be required in order to convert the fast-changing inductor current waveform. Predictive digital current mode control is proposed, bypassing the demanding requirements for the analog-to-digital conversion of the inductor current [69].

A simple solution for digital PWM signal generation is a counter based architecture. A PWM signal is generated by comparing the controller command to a counter value. This requires a high frequent digital clock, e.g. for a 10-bit resolution DPWM in a 500 kHz-converter the time resolution has to be $2\,\mu s/2^{10} = 2\,ns$. Therefore, a digital clock with $f_{clk} = 1/2\,ns = 500\,MHz$ is necessary. Since such a high-frequency digital clock is most often not available or too power hungry, other solutions were presented. [70] reviews various architectures. Often, the proposed solutions are based on delay lines [46, 71–73]. Hybrid architectures combining a counter with a delay line are proposed, demonstrating a good trade-off between clock frequency and required layout area for integration of the delay line [50, 74–76].

Design

Figure 4.14 shows a hybrid DPWM generation concept with 12-bit resolution. The hybrid DPWM generation concept is composed of a counter based part for the most significant bits (MSBs) and a delay locked loop (DLL) based part for the least significant bits (LSBs).

In the counter based part a counter is increased with each positive edge transition of a reference clock Ref_Clk. The counter value is compared to the MSBs of the DPWM input $DPWM\_In < 11:7 >$. This part of the DPWM determines the coarse resolution of the DPWM signal, Fig. 4.15. The fine resolution is determined with the help of a DLL. The DLL works with the Ref_Clk as reference frequency. A MUX

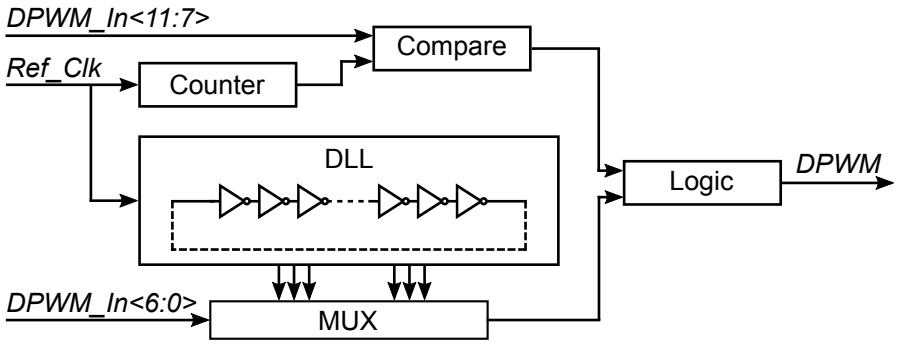

Fig. 4.14: DPWM architecture.

chooses the right signal out of the inverter chain in the DLL according to the LSBs of the input signal $DPWM\_In < 6:0 >$.

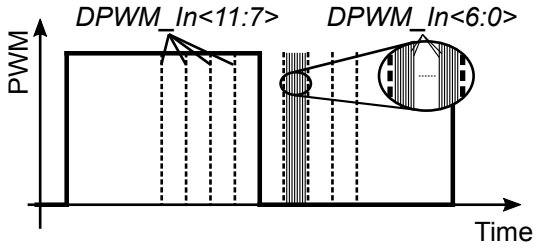

Fig. 4.15: DPWM signal generation.

Experimental Results

The presented DPWM provides 12 bit resolution and zero latency as the latest controller command is immediately used for the generation of the DPWM signal. Monotonicity is of further importance in a digital control loop. If the DNL is greater than -1 LSB for all digital value transitions, the DPWM is strictly monotonic, see also Section 3.2.

Measurement results for the presented solution confirm the strictly monotonic behavior, Fig. 4.16. The measured transfer characteristics shows an offset error of around 3 %, which results from the digital part of the DPWM design. Here, one clock cycle of the reference clock must be waited for, before the DPWM signal can first go low. This is of minor interest, as in the control loop, any offset error of the DPWM will be counteracted by the controller and therefore has no effect. Due to the offset, the minimum duty cycle is 3.1 %, which equals 62 ns. Anyway, a blanking time for avoiding non-intended turn-offs due to switching disturbances applies in SMPS in this time frame. During this blanking time, the switch must generally not be turned off.

Further, there are single DNL values, that are much higher than most of the others. These values occur at

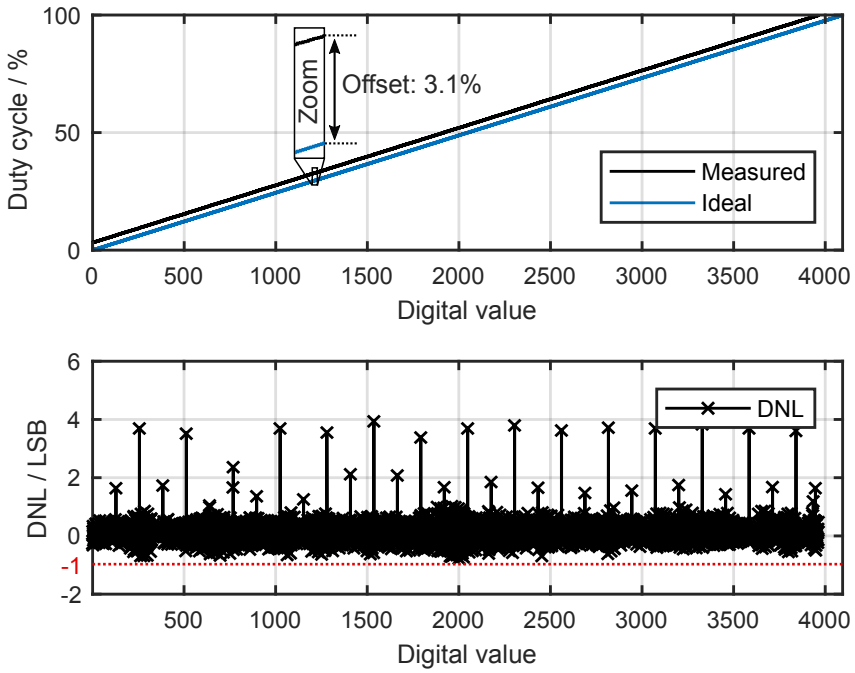

Fig. 4.16: Measured DPWM transfer characteristics.

the LSB transitions of the counter based part (not the overall LSBs). The signal propagating through the DLL has to pass some additional logic gates at the end of the DLL, before starting again at the beginning of the DLL. The propagation delay of these logic gates is visible as enlarged DNL values. In a future design, the logic gates can be bypassed and, therefore, this effect can be eliminated.

Figure 4.17 shows the closed-loop load step response of a 50 kHz-bandwidth digitally controlled buck converter. It converts 14 V to 6 V and comprises the presented DPWM. The results are obtained from mea-

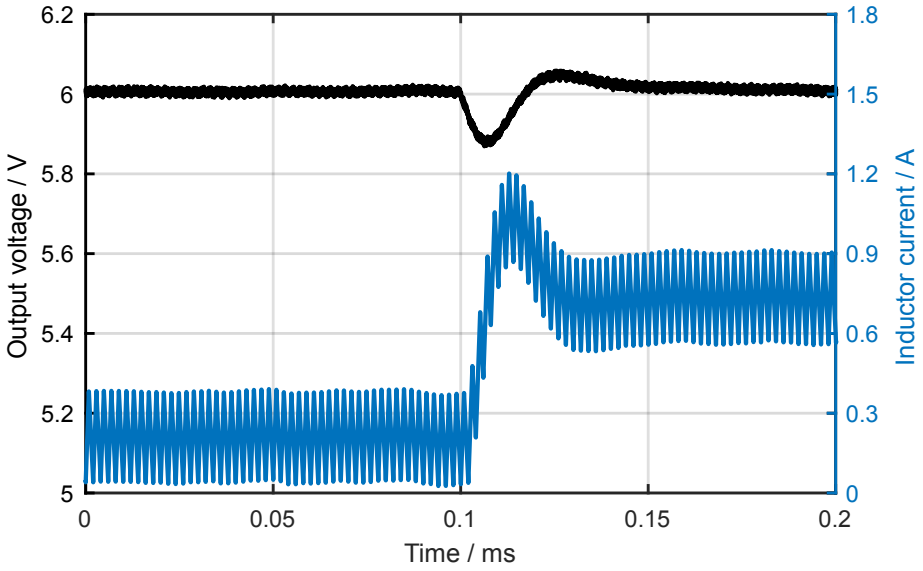

Fig. 4.17: Closed-loop load step response of a buck converter with DPWM.

surements with the experimental setup shown in Fig. 5.23. The closed-loop measurement confirms that the DPWM is well suitable for high-bandwidth SMPS with voltage mode control.

4.3.3 R-2R Digital-to-Analog Converter

R-2R DACs provide high resolution with small area effort in integrated solutions. The working principle relies on resistor ratios, which is in particular beneficial in integrated solutions. Integrated resistors face large parameter variations due to production tolerances. But, on one chip the resistance variation is similar. Consequently, ratio based designs compensate for the variations. Although, the R-2R DAC comes along with the drawback of DC current consumption, it is widely applied for reasons of high linearity and monotonicity. Furthermore, the conversion rate is very high, and the conversion time very low, respectively.

Figure 4.18(a) shows an N-bit R-2R DAC with a sample-and-hold stage, which is used in order to avoid transient disturbances resulting from parasitic capacitances and short switching delays. If Z is the N-bit digital input, the output voltage V_{out} equals:

$$V_{\text{out}} = \frac{Z}{2^{\text{N}}} \cdot V_{\text{ref}} \tag{4.7}$$

For each bit of the digital input Z one resistor branch is available. The branches are either connected to ground or to a reference voltage V_{ref} depending on the digital input Z. Every branch connected to V_{ref} increases the output voltage V_{out}. With voltage superposition, the resulting output voltage can be calculated.

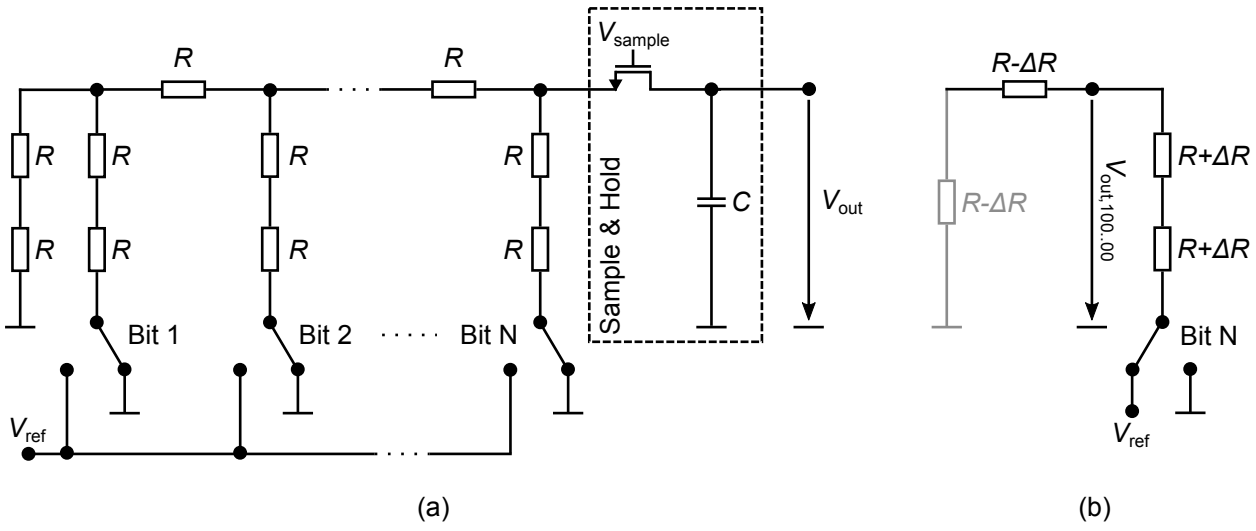

Fig. 4.18: R-2R DAC (a) architecture and (b) equivalent circuit diagram for $Z = 100..00$ with random resistor mismatch (for reasons of clarity without sample-and-hold).

Monotonicity

Even though theoretically an endless number of resistor branches can be added to the R-2R DAC for enhancing the resolution, this is not feasible. The maximum resolution with guaranteed monotonicity depends on the resistance variation from one to another resistor on the same chip, called random resistor mismatch. Although the resistors on the same chip are identical in first order, local parameter variations, e.g. through variation of the doping when fabricating an integrated circuit, lead to the random resistor mismatch.

The most critical transition regarding the monotonicity is the transition from all logical ones except for the MSB to all logical zeros except for the MSB ("011..11" $\rightarrow$ "100..00"). With random mismatch it can happen that only resistors with high resistance ($R+\Delta R$) dominate before transition, while after transition only resistors with small resistance ($R-\Delta R$) dominate. The equivalent circuit diagram after transition is shown in Fig. 4.18(b). The resistor branch, drawn in gray, is obtained from aggregating the resistor branches connected to ground (the LSB branches). The output voltage after transition (corresponding to "100..00") calculates to:

$$V_{\text{out,100..00}} = \frac{2(R-\Delta R)}{2(R+\Delta R)+2(R-\Delta R)} \cdot V_{\text{ref}} = \frac{R}{2R} \cdot V_{\text{ref}} - \underbrace{\frac{\Delta R}{2R} \cdot V_{\text{ref}}}_{\Delta V_{\text{out,100..00}}} \tag{4.8}$$

In this equation, $R/2R \cdot V_{\text{ref}}$ is the ideal set value and $\Delta R/2R \cdot V_{\text{ref}}$ is the the deviation $\Delta V_{\text{out,100..00}}$ from the nominal value due to random mismatch.

In a similar way, it can be shown, that the voltage before transition (corresponding to "011..11") is higher by $\Delta V_{\text{out,00..001}} = \Delta R/R \cdot V_{\text{ref}} \cdot Z/2^{\text{N}}$ compared to the nominal voltage. For high resolutions, $\Delta R/R \cdot V_{\text{ref}} \cdot Z/2^{\text{N}}$ can be approximated by $\Delta R/2R \cdot V_{\text{ref}}$.

For guaranteed monotonicity the voltage after transition must be higher than before transition. Consequently, the voltage of the "100..00"-value must be higher than the voltage of the "011..11"-value. This is related to the definition of the DNL, which is $\text{DNL} = (V_{\text{Z+1}} - V_{\text{Z}})/V_{\text{LSB}} - 1$, in particular $\text{DNL} = (V_{\text{out,100..00}} - V_{\text{out,00..001}})/V_{\text{LSB}} - 1$. Further, the condition for guaranteed monotonicity, which is $\text{DNL} > -1$ (Section 3.2), is taken into account. Thus, when $\Delta V_{\text{out,00..001}} + \Delta V_{\text{out,100..00}} < V_{\text{LSB}}$ is fulfilled, the voltage of the "100..00"-value is higher than the voltage of the "011..11"-value:

$$\frac{\Delta R}{2R} \cdot V_{\text{ref}} + \frac{\Delta R}{R} \cdot V_{\text{ref}} \cdot \frac{Z}{2^{\text{N}}} \sim 2 \cdot \frac{\Delta R}{2R} \cdot V_{\text{ref}} = \frac{\Delta R}{R} \cdot V_{\text{ref}} < V_{\text{LSB}} \tag{4.9}$$

With $V_{\text{LSB}} = V_{\text{ref}}/2^{\text{N}}$:

$$\frac{\Delta R}{R} < \frac{1}{2^{\text{N}}} \tag{4.10}$$

Equation (4.10) relates the random mismatch factor $\Delta R/R$ of the technology to the maximum resolution N of the R-2R DAC. According to (4.10) a 9-bit resolution R-2R DAC can not be fabricated with guaranteed monotonicity in a technology with a higher random resistor mismatch than 0.2 %. Table 4.2 shows the requirement for the random mismatch factor $\Delta R/R$ for different resolutions N. The random mismatch factor means that the resistor's value can vary from $R-\Delta R/R$ to $R+\Delta R/R$.

Tab. 4.2: Maximum random resistor mismatch requirement of the technology used for different resolutions N.

N	8	9	10	11	12	13	14
$\Delta R/R$	0.39 %	0.20 %	0.10 %	0.05 %	0.02 %	0.01 %	0.005 %

The presented R-2R DAC is designed with 10-bit resolution. The random mismatch factor of the technology used and the dimensions of the resistors used lead to $\Delta R/R = 0.18\,\%$. Consequently, monotonicity is guaranteed up to 9.2-bits resolution. This value refers to the standard deviation (1 σ). Consequently, the actual random resistor mismatch may also be lower. Such a design is critical without experimental validation of the monotonicity. The experimental verification of the DAC, used in this work, confirms monotonic transfer behavior, see the experimental verification of this section.

Resolution and monotonicity of the DAC can be improved with segmented designs at the expense of chip area and power consumption [77]. The idea of segmented DAC designs (hybrid DAC) is to conduct the digital-to-analog conversion with two sole DACs, one of them is responsible for the MSBs, the other one is responsible for the LSBs. After each of them finished its conversion, their outputs are combined in order to have one common output voltage.

Conversion Time and Rate

The conversion rate of the R-2R DAC is mainly dependent on the sample and hold (Fig. 4.18).

The settling of the output voltage is dominated by the resistors of the R-2R DAC and the capacitor of the sample and hold. In this design, the settling is considered to be finished once an error of less than 0.5 LSB is achieved. The output voltage V_{out} as a function of the time for a voltage step applied to such an RC element is described by:

$$V_{\text{out}}(t) = V_{\text{out,end}} \cdot (1 - \mathrm{e}^{-\frac{t}{RC}}) \tag{4.11}$$

When applying a full-range voltage step, which requires the longest conversion time, the target voltage is $V_{\text{out,end}} = V_{\text{Ref}}$. An error of less than 0.5 LSB is achieved with an output voltage of $V_{\text{out}} = V_{\text{Ref}} - 0.5 \cdot V_{\text{LSB}} = V_{\text{Ref}} - 0.5 \cdot V_{\text{Ref}}/2^N$. Consequently, the settling time t_{settling} and the conversion rate f_{max} of the R-2R DAC in general can be calculated based on (4.11):

$$t_{\text{settling}} = R \cdot C \cdot \ln(2^{N+1}) \rightarrow f_{\text{max}} = \frac{1}{t_{\text{settling}}} = \frac{1}{R \cdot C \cdot \ln(2^{N+1})} \tag{4.12}$$

For modeling the behavior and for determining the stability in the control loop a PT1 transfer behavior with a corner frequency of $f_1 = 1/(2\pi \cdot R \cdot C)$ can be assumed. The design of this work uses resistors with $R = 10\,\text{k}\Omega$ and $C = 12\,\text{pF}$. This results in a corner frequency of $f_1 = 1.33\,\text{MHz}$.

Experimental Verification

Figure 4.19 shows the measured transfer characteristics of the 10-bit DAC.

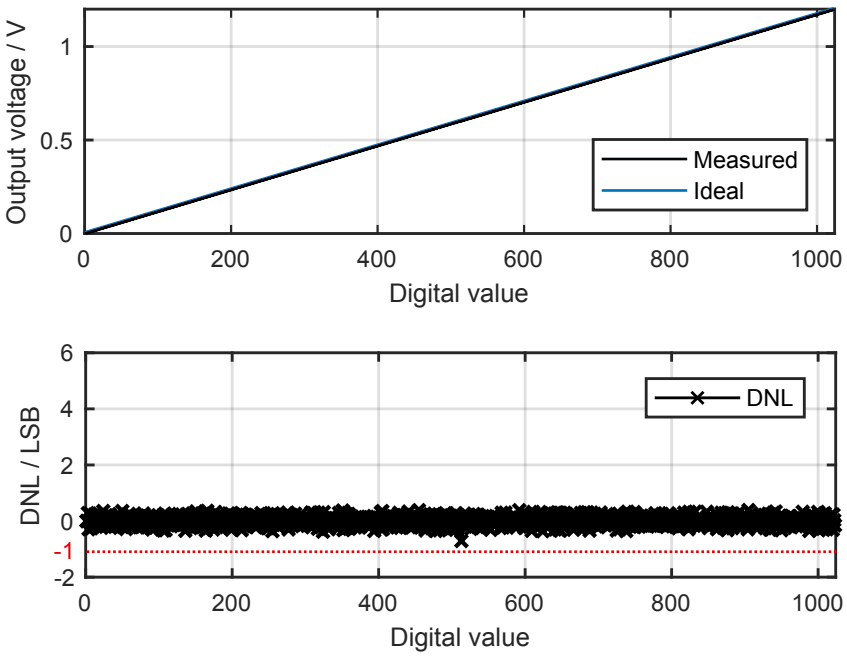

Fig. 4.19: Measured R-2R transfer characteristics.

The measured transfer characteristics indicates that the DAC is strictly monotonic, since the DNL is larger than -1 for all signal transitions. The corner frequency of the DAC is $f_1 = 1.33\,\text{MHz}$. The phase degrades in a PT1 transfer block starting from one tenth of its corner frequency. This allows a usage of the DAC in converters with a crossover frequency of up to 133 kHz without lag of phase.

The measurement results in Section 6 confirm proper closed-loop operation.

4.3.4 High-Resolution Charge Pump Digital-to-Analog Converter

A high-resolution, wide-range DAC can be built with the charge pump architecture [78]. In order to achieve excellent dynamic behavior, advanced SMPS controls require the DAC to deliver large output voltage changes within one conversion cycle, see Section 6. The proposed DAC supports this with the help of an extra wide differential conversion range, as will be described below. It guarantees monotonicity, along with low steady-state current consumption.

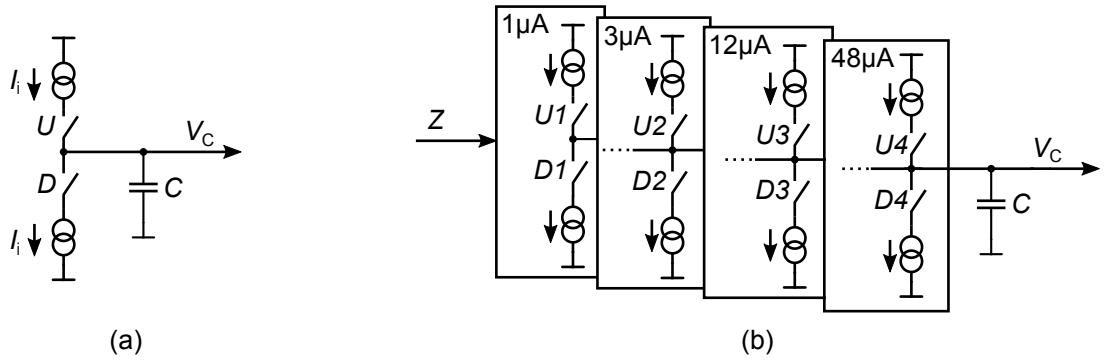

Fig. 4.20: Charge pump DAC (a) working principle and (b) implementation.

The working principle and the implementation of the charge pump DAC is shown in Fig. 4.20. The output capacitor C is charged or discharged in order to provide an output voltage V_c. While dis-/charging, the output voltage changes by $\Delta V_C = \Delta Q/C = (I_i \cdot \Delta t)/C$. The longer the charging interval Δt, and the higher the charging current I_i, the higher the voltage change ΔV_C. The implementation has four differently scaled current sources (1 µA, 3 µA, 12 µA, and 48 µA) for small and large changes of the output voltage. The output voltage can be increased and decreased, respectively. In each conversion cycle, these current sources are activated during a certain time interval Δt. This time interval can be chosen in 0.5 ns-steps and can be as long as 128 ns. When activating all current sources at the same time, the maximum time interval can be 512 ns for providing extra large voltage changes. A digital control logic chooses the current source I_i and the Δt according to the DAC input signal Z.

The charge pump DAC works with a differential input command, which controls the output voltage change. This is appropriate in a control loop. In a conventional controller, first the output change and, in a second step, the absolute controller output value is calculated. Therefore, the second calculation step is omitted for the charge pump DAC, as the absolute controller output value equals the capacitor voltage V_c. Thus, controller calculation effort is reduced.

Design

The charge pump design, which is shown in full detail in Fig. 4.22, is composed of the following blocks:

- A capacitor C, serving as charge storage, generating the output voltage V_c
- Current sources in four different sizes
- Switches, that are turned-on in order to dis-/charge the output capacitor, controlled by $D1 - D4$ and $U1 - U4$
- A pulse generation block, which generates turn-on pulses of varying length for the control of the switches
- A logic block, which chooses the current sources and determines the length of the turn-on pulses

In the charge pump DAC design, two different switch topologies are used, which are designed with regard to high resolution and low leakage. Figure 4.21 shows the charge pump output capacitor voltage when demanding a small voltage change by activating an $I_i = 1\,\mu A$ current source for the period of $\Delta t = 1\,ns$. The output voltage is shown for the simple switch architecture and for the dedicated differential switch architecture. With the simple switch architecture significant charge injection into the output capacitor occurs. It leads to a total output voltage change of $-220\,\mu V$. In contrast, the differential switch causes only $-60\,\mu V$ total output voltage change. The discharging of the current source dominates the output voltage change. With the differential switch the current sources are continuously kept in their operating point by drawing the current with a dummy load (M16, M26, M36, M46). Once the switch is turned on, the current is redirected to the output capacitor with reduced charge injection.

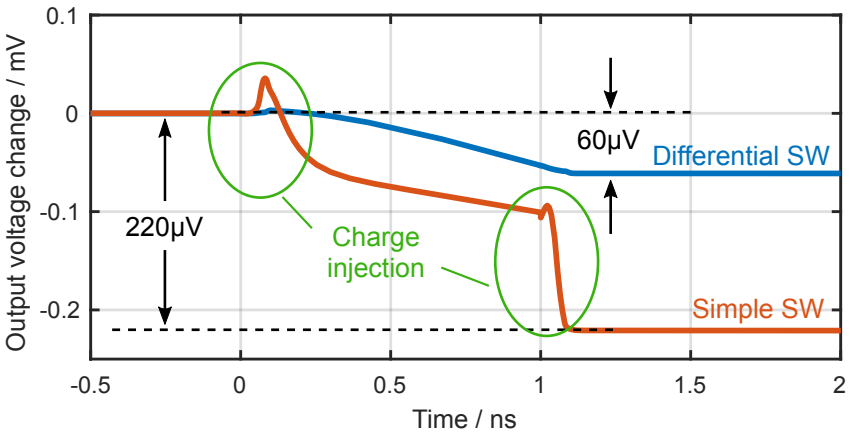

Fig. 4.21: Simulated charge injection at the charge pump DAC output voltage for a simple switch architecture and for a dedicated differential switch architecture.

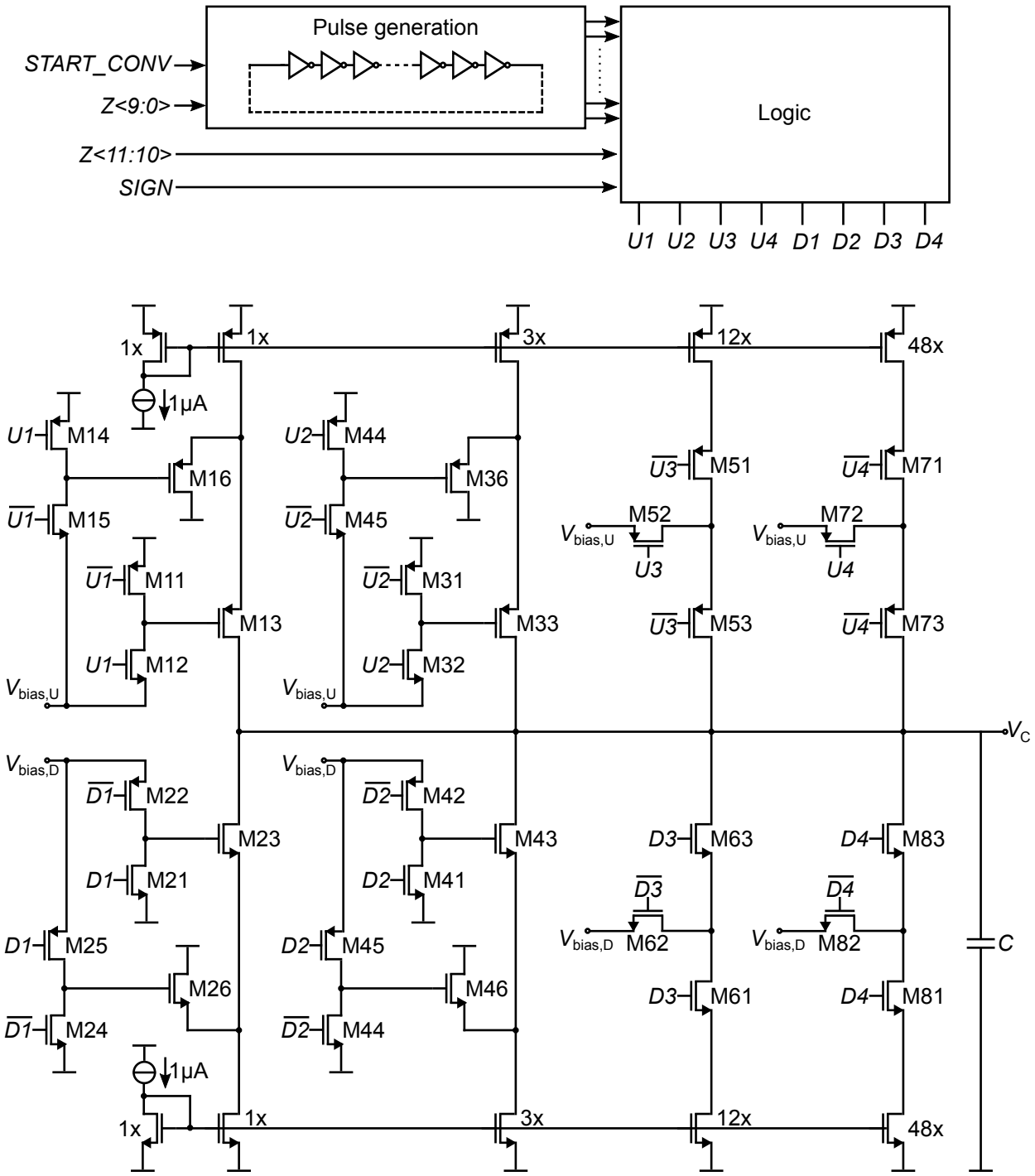

Fig. 4.22: Charge pump DAC design.

The differential switch architecture (M11–M16; M21–M26; M31–M36; M41–M46 in Fig. 4.22) in the charge pump design is inserted for the low current sources. It enables very small voltage changes of the output voltage V_c and therefore, supports high resolution charge pump digital-to-analog conversion. For the higher current sources, the simple switches (M61–M63; M71–M73; M71–M73; M71–M73 in Fig. 4.22) are implemented in order to minimize the steady-state current consumption. The charge injection effect on the

output voltage change is relatively low, as the voltage change due to the dis-/charging of the large current sources is high.

For low leakage currents, the channel length of the FETs, directly connected to the capacitor, are chosen well above the minimum length of the technology in order to minimize channel leakage. Further, when turned-off, their source potential is connected to a bias voltage $V_{\text{bias,U}} = 3.4V$ / $V_{\text{bias,D}} = 1.0V$. Thus, the drain-source voltage is kept low, which further reduces leakage currents and charge injection.

Experimental Results

From Fig. 4.12 (Section 4.1) the maximum conversion time of the charge pump DAC is known to be 128 ns. If a large voltage swing is required within one conversion cycle of the DAC, an extra long conversion with up to 512 ns is possible, exceptionally. For stability considerations the standard conversion time has to be considered, as the long conversion time is only necessary in a single conversion cycle, whereas the following conversion cycles work with short conversion time again.

The output capacitor node of the charge pump DAC is sensitive and non-accessible off-chip. Therefore, the resolution of the charge pump DAC is measured indirectly after a following buffer block. Figure 4.23 shows a burst measurement with a sequence of 1000 conversions.This burst measurement is necessary in

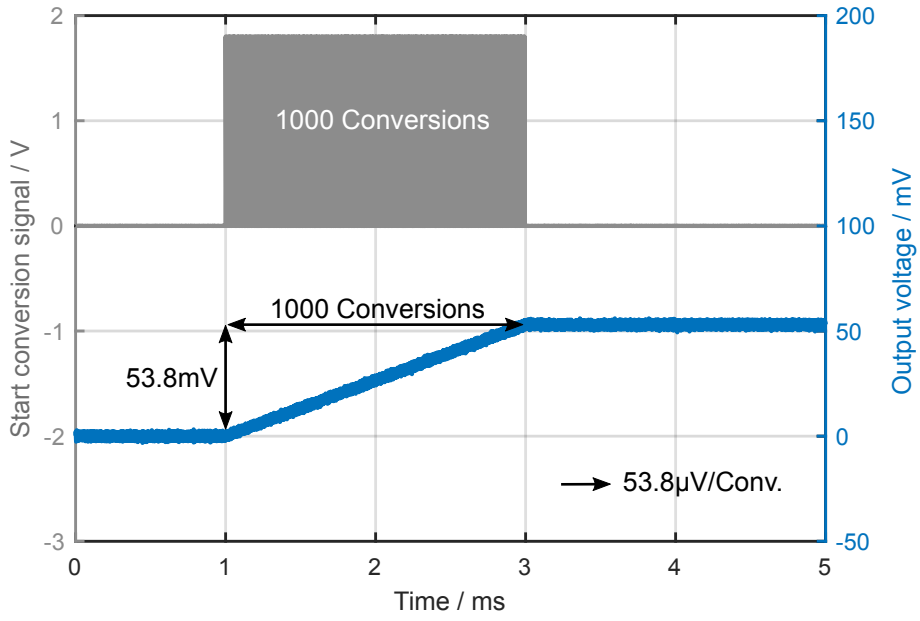

Fig. 4.23: Charge pump DAC resolution measurement: 1000 conversions in a row in order to obtain a well-measurable signal.

order to obtain a well measurable signal amplitude. A new DAC conversion is started every 2 µs. With each conversion the smallest voltage change is applied. The voltage change after 1000 conversions is 53.8 mV, which indicates that the smallest applicable voltage change is 53.8 µV. Therefore, limit cycle oscillations are prevented in a control loop. SMPS with large output voltages, which operate with the fine resolution of the delay line ADC of Section 4.1, are covered. The maximum voltage change was measured to be 1.6 V. A conventional full-range DAC, achieving the same performance, would require a resolution of 15-bit ($1.6\,\mathrm{V}/53.8\,\mu\mathrm{V} = 29739 = 2^{14.8}$).

The output capacitor of the charge pump DAC may face leakage currents, therefore the presented architecture is designed with regard to low leakage currents. Figure 4.24 shows a measurement of the leakage current based voltage drift. It indicates 228 mV output voltage change in 6 seconds. Hence, the output voltage drift is only 76 nV per 2 µs-switching period. This is a very low value, since in an exemplary converter with a plant DC gain of 10 and with an ADC output voltage resolution of 2.56 mV, a change by 1 LSB of the output voltage ADC is first observed after $2.56\,\mathrm{mV}/(76\,\mathrm{nV}\cdot 10) = 3368$ switching periods. The 1 LSB-deviation is counteracted by the controller, subsequently.

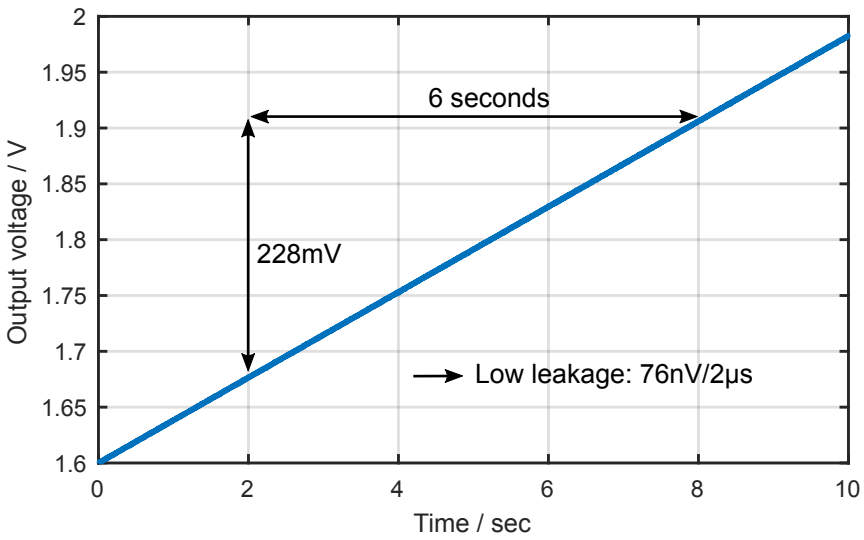

Fig. 4.24: Charge pump DAC leakage current based voltage drift measurement.

Stable closed-loop performance of a boost converter with a digital control loop, composed of the charge pump DAC and of the live-tracking delay line ADC (Section 4.1), is shown in Fig. 4.25. The experimental setup is shown in Chapter 5 in Fig. 5.23. Although the ADC output voltage resolution is as low as 2.54 mV, the charge pump DAC enables to operate this boost converter without limit cycle oscillations due to its excellent resolution.

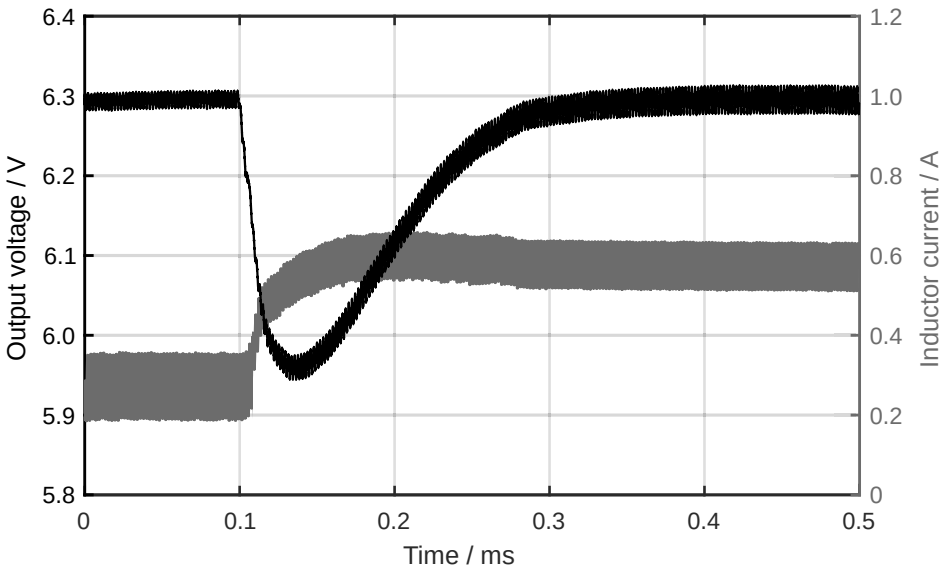

Fig. 4.25: Closed-loop operation of a boost converter with charge pump DAC and delay line ADC.

Comparison to Prior Art

The charge pump DAC of this work offers the highest resolution (15-bit) among the DACs listed in Table 4.3. It improves the leakage by a factor of 4000 compared to the charge pump design of [78]. Also, the maximum conversion rate of 7.8 MHz is higher compared to other solutions and supports digital controls in converters with high switching frequencies. It guarantees monotonicity, along with low steady-state current consumption (20 µA). The conversion time is as low as 128 ns, which enables high-bandwidth digital control. The charge pump DAC qualifies for use in automotive applications with high output voltages due to its high resolution of 53.8 µV/LSB, which is necessary for accurate output voltage regulation and for avoiding limit cycle oscillations.

Tab. 4.3: Comparison of the proposed charge pump DAC with prior art.

	[79]	[78]*	**This Work**
Equivalent Resolution	10 bit	10 bit	**15 bit**
Voltage Resolution	3.2 mV**	2.11 mV	**0.054 mV**
Maximum Conversion Rate	1 MHz	n.r.	**7.8 MHz**
Conversion Time	8 µs	n.r.	**128 ns**
Leakage	n.a.	-300 µV/2 µs	**0.076 µV/2 µs**

*First presented in [80]. **Estimated from figure.

4.4 Comparison to Analog Control

This section compares the digital controls, built with the control loop blocks presented in Section 4.1 and 4.3, to analog controls. The comparison is based on SMPS examples, extracted from existing automotive products.

The dynamic and static performance, achieved in a closed-loop system, with standard digital control is equal to analog control. When applying advanced controls, the closed loop performance is improved in terms of small voltages deviations and fast regulation in case of disturbances. Advanced controls can be realized in a digital solution with low effort by varying the controller coefficients, as described in [50] and in Section 6. Also, in analog control it is possible to apply more advanced control concepts, but only at the expense of significant chip area [81–87]. Digital testing is less expensive than testing of complex analog circuits. Although, the digital control loop comprises analog elements, e.g. within the ADC and the DAC, test cost is considered to be lower in digital control than in analog control [88].

The following comparison focuses on chip area of integrated solutions. Since chip area is costly, any overhead required for the implementation of digital control in comparison to analog controls is not desirable. The comparison considers a digital controller including the fast transient control presented in Section 6.2. In the analog solution, only a standard controller without fast transients is regarded.

Figure 4.26 shows the photograph of the IC, which was developed and fabricated in a 180 nm-technology as part of this work. The IC is intended to be used with different converter topologies and control concepts. Therefore, the Delta-Sigma ADC, the delay line ADC, the DPWM, the R-2R DAC, and the charge pump DAC are implemented in the test chip. Also, other blocks necessary for implementing the converter are available, such as the low-side FET, the current sensing, the ramp compensation, the gate driver, and the PWM generation. Block sizes are marked and given in the drawing.

Figure 4.27 shows a comparison, that considers the parts of the converters, that are different in analog and digital control. For the realization of an analog control, an OTA is required together with capacitors and resistors as compensation devices. Thus, in the digital control the blocks equivalent to the OTA and compensation devices are taken into account. Three different SMPS examples are compared: (1) a standard buck converter of an automotive power IC, (2) a boost converter of the same IC (Boost 2), as well as (3) a boost converter of an airbag application IC (Boost 1). The chip areas of the SMPS with analog controls are extracted from existing automotive products.

The chip areas required for integration of the controls for the buck converter are similar in analog and digital. The analog controller has small compensation device values due to a high control bandwidth and, therefore, consumes only small area. The boost converter of the airbag application (Boost 1) has relatively small

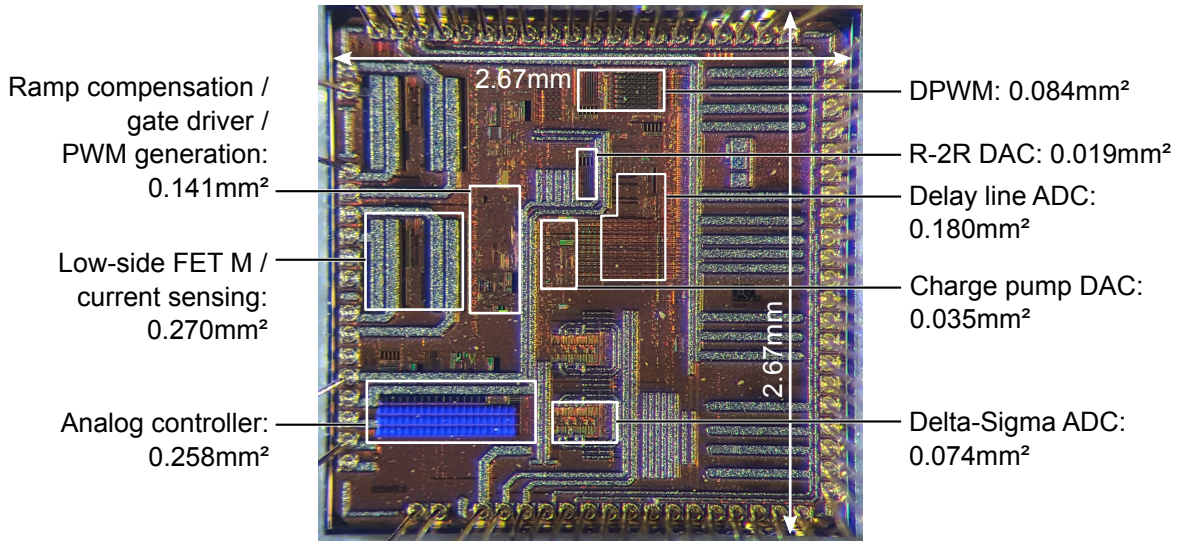

Fig. 4.26: Test chip photograph with control loop blocks.

compensation devices, as well. Consequently, full-integration of the analog control is possible. However, the digital control can be fully-integrated with 2.5 times smaller chip area. The boost converter of the automotive power IC (Boost 2) has large compensation device values, which prevent an integration of the resistor and capacitors, as they would consume a large chip area. Consequently, they are applied off-chip as discrete components. In contrast, the integration area of the digital controller is not affected by the values of the coefficients in the control law. Therefore, digital controllers can be integrated, unconditionally.

For comparison of the total chip area of the converters, also the remaining integrated blocks, i.e. low side FET, current sensing, PWM generation, gate driver and ramp compensation, must be taken into account. These blocks add up to another 0.411 mm^2 chip area. Consequently, the boost converter of the airbag implementation (Boost 1) can be integrated on a total chip area of 0.797 mm^2 with analog control and on

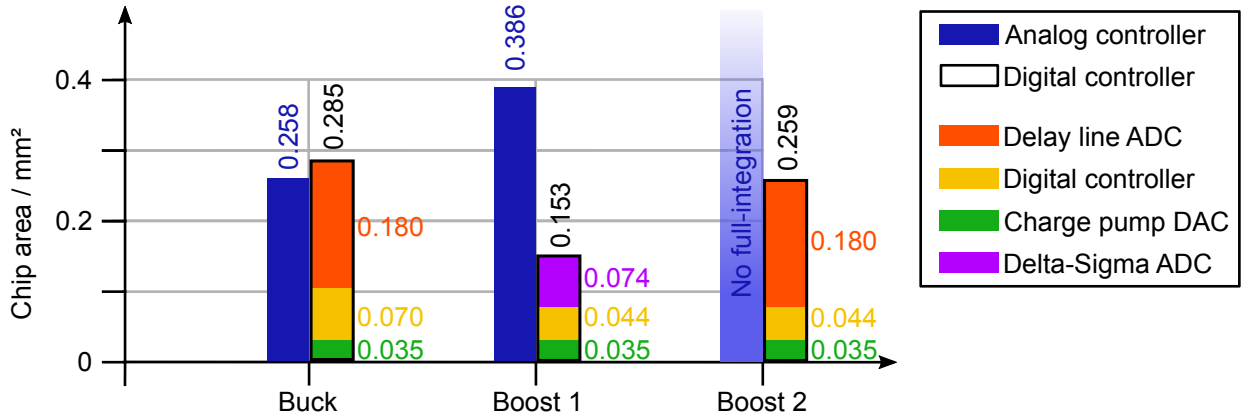

Fig. 4.27: Chip area comparison.

0.564 mm^2 with digital control, respectively. Still, discrete components are necessary for realization of the entire converter, i.e. the diode, inductor, and capacitor, see Fig. 3.4.

When the compensation devices are mounted off-chip in analog solutions, an additional pin is required for their connection, see Section 3.2. This pin is very sensitive and EMC requirements, such as DPI, may not be met. Further, automotive safety rules require for loss / short-circuit detection of the external devices. Digital control solutions can always be fully-integrated no matter of the application. Consequently, the drawbacks of the discrete compensation devices of analog controls are avoided.

5 Parameter Identification

Parameters in SMPS vary for multiple reasons. For example, the loads may turn on unpredictably, the input voltage changes, and the inductor and the capacitor underlie variations due to production tolerances, temperature dependencies, and degradation, among others. Parameter variations change the behavior of the SMPS fundamentally. If parameters are known from a parameter identification, controller design is simplified and new features like diagnostics and autotuning are enabled. Parameter identification is beneficial for plug and play solutions, which allow to choose practically any inductor or capacitor for the SMPS, that meets the application, cost and quality requirements. Thus, the customer's flexibility is enlarged. Further, control loop design skills are not required in the application, anymore.

In this section, the advantages and requirements of parameter identification are discussed. Then, prior art is examined with regard to accurate and fast identification and other requirements. Identification concepts for load, inductor, and capacitor are proposed and, finally, compared to prior art.

5.1 Motivation

Parameter Variation of Standard Components

In modern cost-driven applications passive components with the lowest price are preferably used. Most often the cheapest components underly the greatest parameter variations. Figure 5.1 confirms this on the example of a 10 µF multilayer ceramic capacitor (MLCC) from Kemet. In case of this capacitor, which can be implemented as a standard output filter capacitor, the price for a ±20%-production tolerance version is 28% lower than for the ±5%-tolerance version. Consequently, the price difference of capacitors with different tolerances may be significant.

Besides, the availability of different inductor and capacitor models from different suppliers is important for reliable manufacturing. Figure 5.2 shows the available inductor and capacitor models for different production tolerances from a large distributor of passive electronic components. There is a much larger supply of capacitors available with ±20%- and ±10%-tolerance. In contrast, there is only a limited choice

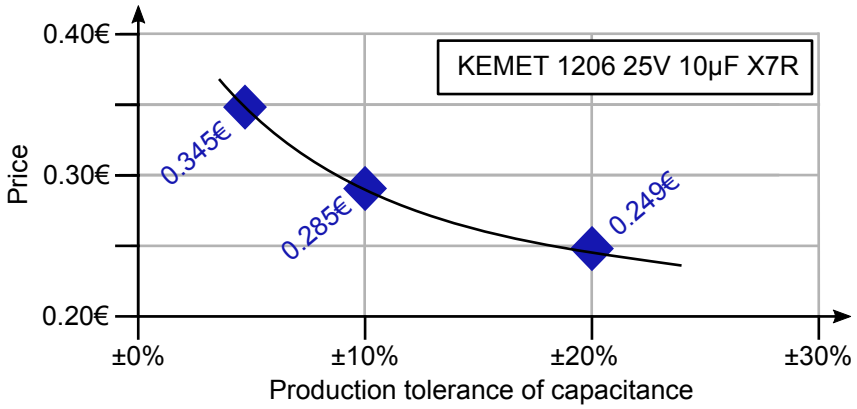

Fig. 5.1: Capacitor prices of a distributor of electronic components for various production tolerances [89].

of inductors, which have production tolerances smaller than ±20%. Only few inductors and capacitors are available with production tolerances smaller than ±10%.

Passive components underly not only production tolerances, but show also temperature effects, and aging. Figure 5.3 shows the actual capacitance of a standard 10 µF MLCC, exemplary. The production tolerance of the presented device is ±20%. An additional ±15% capacitance temperature variation has to be added to the production tolerance (temperature range: -55°C...125°C). Aging results in -3 % capacitance loss per decade hour of use. Consequently, the value of an off-the-shelf 10 µF-capacitor may vary between 6 µF and 14 µF. This variation is to a great extent unpredictable. Figure 5.3 does not even take into account the variations resulting from voltage and frequency dependencies, as covered in Section 5.4. Thus, the overall variation may exceed +40 % / -65 %.

The effect of temperature variations will even increase in future automotive and consumer products as the operating temperature ranges will get larger due to smaller size packaging and higher power dissipation at the same time.

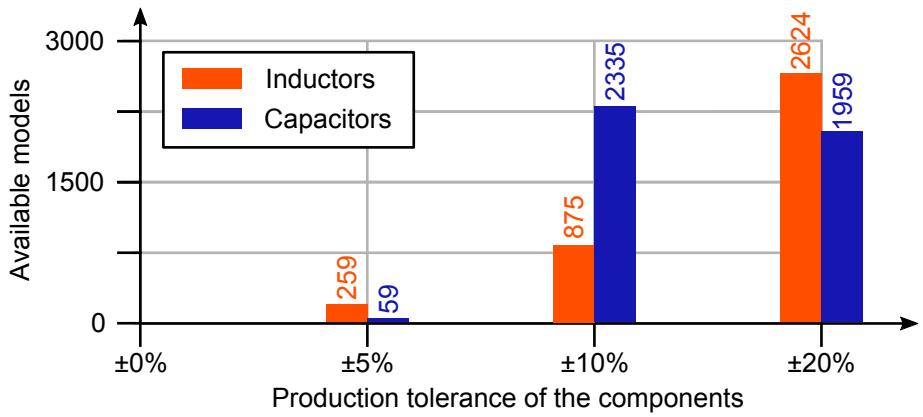

Fig. 5.2: Number of models with different inductance and capacitance tolerances available at a large distributor of electronic components [90].

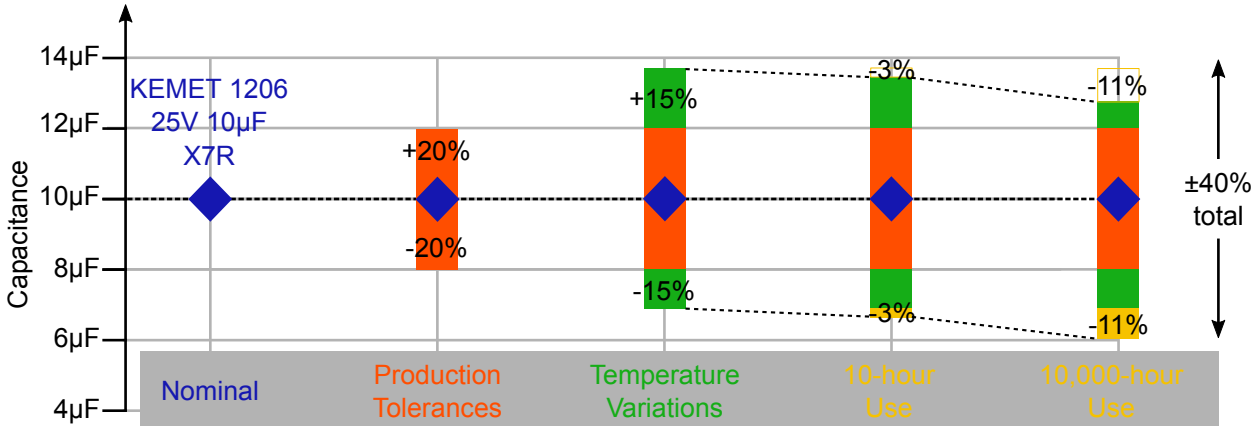

Fig. 5.3: Parameter variations of a standard 10 µF-capacitor [89].

In conclusion, available models, prices, and the variety of effects, causing parameter variations, require to deal with unpredictable inductor and capacitor values. This is increasingly challenging for SMPS design.

Impact on the Transfer Function

The result of parameter variation in SMPS is a change of the behavior, which becomes visible in the control-to-output transfer function. Figure 5.4 shows transfer functions of a current mode controlled boost converter with a ±50%-variation of the nominal inductance and capacitance values. This variation is chosen according to the investigations shown in the previous subsection. The boost converter parameters are given in Table 3.1. In the bode plot of Fig. 5.4 also the operating range for parameters, such as $V_{\text{in}} = 3\,\text{V}...5\,\text{V}$, and $I_{\text{load}} = 75\,\text{mA}...1\,\text{A}$ are considered.

In worst case, this variation results in crossover frequencies from 1.7 kHz to 8.7 kHz, and phase margins from 27° to 98°, respectively. Thus, the control speed as well as stability and damping vary, significantly. The output voltage deviations in case of a load transient differ by a factor of five for the same load steps due to the crossover frequency variation. In order to fulfill a given maximum output voltage deviation specification with any parameter variation, the output capacitor value needs to be chosen five times higher than without parameter variations. The higher the capacitance needs to be, the higher the price of the capacitor gets, see Fig. 6.1. Thus, this increases the cost, drastically. Control slow down or instability is avoided at the cost of either transient performance or additional hardware.

More complex converter topologies, as single ended primary inductance converters (SEPIC), Zeta, or multiphase converters, are composed of more passive components than standard converter topologies. Consequently, the parameter variations of all passives add up and the overall parameter variation becomes extremely large in these converter types. Hence, they are designed for worst-case, requiring high margins.

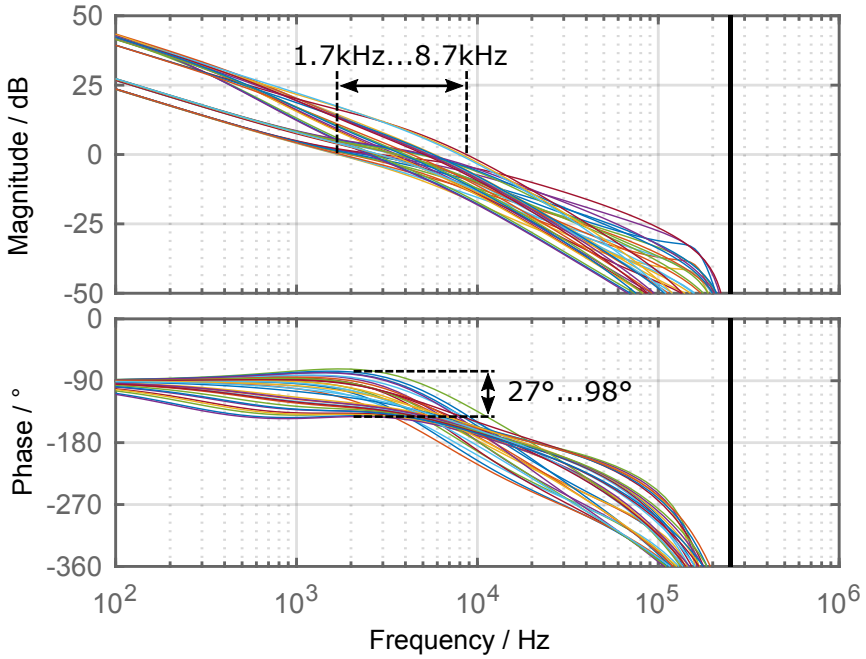

Fig. 5.4: Variation of the boost converter transfer function for variation of the inductor and the capacitor by ±50%.

Consequently, they would benefit even more from parameter identification, since it allows to relax the design specifications.

Advantages Resulting from Identification

With system identification, executed continuously or at regular intervals, an accurate knowledge of the system parameters is available at all times. Thus, worst-case design can be avoided and instead, the controller parameters can be automatically set to optimal values. Consequently, the control loop can operate with optimum performance at all times. This results, in particular, in minimum output voltage deviations from the set point in case of load or input voltage transients.

System identification makes plug and play systems feasible. In this scenario, any inductor and any output capacitor are chosen for the SMPS, which fit to the target application and meet the cost and quality requirements. The SMPS identifies itself by means of system identification and sets its controller parameters accordingly at the beginning and during SMPS operation (autotuning). The components can be selected with respect to the recent price and availability. As an additional advantage, the user of the SMPS is not responsible for the control loop design. Thus, there is no need for control loop design skills in the application, anymore. The application of SMPS is simplified.

When identifying individual converter parameters, the identification can serve as a safety feature, because

it enables to evaluate, whether safe converter operation is possible or not. For instance, it can be monitored, if the output capacitor does still have the minimum capacitance required.

Both entire system and single parameter identification lead to cost savings. On the one hand, additional hardware, such as redundant output capacitors applied for safety reasons, becomes obsolete. On the other hand, maintenance cost is reduced and predictive maintenance is enabled. Any failure is found within shorter time. This improves the reliability. It also reduces cost, in particular, because parameter identification results directly indicate, which component of the system failed. With predictive maintenance, the SMPS can indicate imminent failure and corrective actions can be taken before failure (health monitoring).

A further advantage is that the inductor and capacitor value can be provided to the implemented control concepts [18, 91, 92]. This is beneficial as the control success of these advanced concepts strongly relies on the accurate knowledge of these values. Besides, parameter identification results enable the detection of mode transitions from continuous conduction mode (CCM) to discontinuous conduction mode (DCM) and, thus, minimize transition effects and bypass stability issues [93].

The identification of the load or the input voltage, which have significant influence on the RHPZ and on the maximum control bandwidth in a boost converter, can be used for controller adaption. Thus, output voltage disturbances can be regulated fast (Section 6.2), the power efficiency of the converter can be maximized [94], and adaptive voltage positioning can be applied, see [30] and Section 2.2.

Requirements for Identification Concepts

Identification is required within short time, with low hardware effort, with small perturbation level, and with high identification accuracy.

The identification process can be performed during startup of the converter or during ongoing operation. In many applications, e.g. automotive, the converter has typically around one millisecond to ramp up its output voltage to the operating point. Consequently, the identification should be performed within that time. A suitable approach could be 500 µs for identification, so the converter has another 500 µs for the output voltage ramp-up, which is shown in detail in Fig. 5.6 (Section 5.3.1). If the identification process takes place during ongoing operation, its duration should be as short as possible, because usually perturbation of the steady state is required to identify the converter parameters. In addition to that, unpredictable load steps within long identification periods disturb the identification.

For cost reasons, hardware effort for identification is aimed to be kept small. Consequently, it is best to use already available hardware and control possibilities. In particular, the output voltage and the inductor current of a converter can be controlled in a wide range before operation / during startup.

The inductor current can be manipulated randomly up to its overcurrent limit. Also the output voltage can be disturbed, but should keep distance to the nominal output voltage in order to avoid that supplied loads start operating. Typically, for operation there is an output voltage margin specified for the SMPS. For example, the output voltage has to stay within this output voltage margin under all circumstances in operation. Consequently, when applying identification, the voltage margin available for regulating load steps shrinks, Fig 5.5. Thus, the converter needs to operate with the lowest disturbance possible caused by the identification during operation.

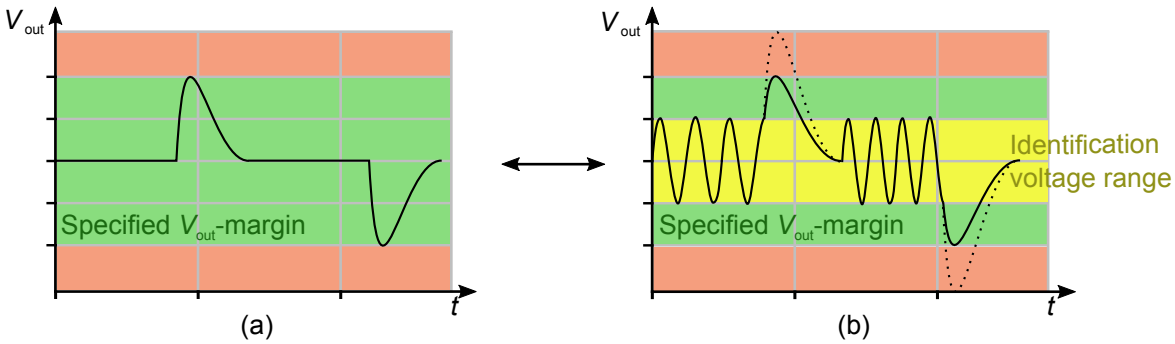

Fig. 5.5: Output voltage behavior (a) without identification and (b) with identification.

The higher the identification accuracy is, the more precise the controller configuration can be matched to the converter in plug and play solutions or autotuning, and the more accurate any health monitoring can be applied.

The requirements, i.e. short identification duration, low hardware effort, small output voltage disturbances, and high identification accuracy, are often not considered in prior art. This is explored in the following section.

5.2 Review of Prior Art

There are multiple common system identification concepts for digitally controlled SMPS: Load identification based on analog sensing circuitry [95–103], system identification by cross-correlation [104–111], oscillation-based autotuning [13, 108, 112–116], or adaptive tuning of the phase margin and the crossover frequency [14, 15, 117, 118]. These system identification concepts are described and discussed in the following section.

Parameter Identification Based on Analog Sensing Circuitry

There are various approaches for a load current measurement based on analog sensing circuitry. A commonly used and simple solution for determining the load are shunt resistor or hall measurements. Also, current transformers are applied, but they do not provide the dc information [119, 120]. Thus, an accurate load current measurement is possible, but losses are notably increased or dc information is missing at the same time. Further, [121] proposes several other current sensing techniques, which rely on additional hardware. Current sensing techniques for the inductor current are proposed, which is not directly useful for load identification, since the inductor current is not equal to the load current [122].

In [95, 96] a lossless load current sensing circuitry is presented. This approach aims to identify relevant SMPS system parameters, such as the inductance and the latest load current. They can be used to select predefined controller coefficients, minimizing the closed-loop response variation due to the load-current deviation.

In that concept the equivalent series resistance of the inductor R_L is utilized for lossless load current determination by an average current sensing technique. Some additional analog circuitry is necessary to built a current sensing network, which in turn feds voltage controlled oscillators. After delta-sigma signal processing and decimation filtering, the inductance and the load current are calculated. A built-in self test (BIST) functionality improves the load identification accuracy by characterizing the widely varying equivalent series resistance of the inductor R_L during startup.

The inductance can be identified with a maximum identification error of 6 % and the load current can be identified with a maximum sensing error of 3 % [95, 96]. Additional analog circuitry is required for identification.

System Identification by Cross-Correlation

The discrete-time impulse response of a observed system can be identified by stimulating the system with white noise and cross-correlating the output and the input signal. In [104–111,123] identification approaches based on cross-correlation with the goal to identify the frequency response of the system are presented.

The duty cycle of the converter in open loop is perturbed with a pseudo-random binary sequence (PRBS), which is a good approximation of white noise as shown in [107]. The output voltage of the converter is recorded and cross-correlated with the PRBS input signal. After performing a discrete fourier transformation of the cross-correlation result, the converter transfer function is obtained. From this the crossover frequency f_c and the phase margin φ_M are calculated, indicating the performance and stability of the closed-loop control system. If necessary, the controller parameters can be tuned in order to improve performance and stability.

In [107] the perturbation causes an additional output voltage ripple of $\pm 0.6\,\mathrm{V}$, which equals $\pm 4\,\%$ of the nominal output voltage. The identification duration is around 123 ms. The data processing algorithm is implemented offline in Matlab Simulink. In [109] an integrated identification of the frequency response is shown with a huge number of 28,100 gates, 9.0 kB random-access memory (RAM) and 1.5 kB read-only memory (ROM). No information about the identification accuracy is given.

Autotuning by Oscillation Analysis

In [13, 108, 112–116, 124] autotuning is performed based on injecting and analyzing an output voltage oscillation. The main idea is to generate an oscillation and then measure its amplitude and / or its frequency, which contains information about the system.

The concept of [114] utilizes the relay feedback method. The autotuning process is performed during converter soft-start and divided into three phases. In phase A an oscillation at the LC resonance frequency ω_o is introduced and the first controller parameter is set accordingly. In phase B a phase margin tuning algorithm is performed by iteratively adjusting the second controller parameter. In the final phase C the gain of the controller is set in order to obtain the desired bandwidth.

The autotuning process is performed during soft-start and thus the peak-to-peak perturbation voltage of around 100 mV does not cause any harm. The autotuning procedure has a long duration of about 8 ms. An acceleration of the identification is not possible, since it is physically limited by the LC resonance frequency. It is not stated how many logic gates are needed to implement this autotuning concept. In [13] a similar approach is presented and implemented with 18,000 gates.

Adaptive Tuning System of Phase Margin and Crossover Frequency

In [14, 15, 117, 118] adaptive autotuning systems are presented. The goal of these autotuning concepts is to continuously control the crossover frequency and the phase margin of the system. The control system is excited with a frequency equal to the latest crossover frequency. In order to find this frequency, the injected frequency is iteratively adjusted until its amplitude matches the amplitude of the measured frequency. Then, the phase delay at this frequency, which equals the phase margin of the control, is measured. An adaptive tuning algorithm adjusts the PID controller parameters such that the crossover frequency and the phase margin meet their pre-set values.

In [14] a square wave signal is injected and chosen such that only one LSB of the output voltage ADC (20 mV) is triggered. This equals $\pm 0.4\%$ of the nominal output voltage. The tuning of the controller is performed during ongoing operation and is implemented with a total number of 12,270 gates. The identification takes approximately 20 ms.

The prior art system identification approaches are all relevant and useful, but their implementation effort is significant and the identification times are long. That is why, there is a need for new concepts addressing these drawbacks. Fast and low effort parameter identification concepts are proposed in the following section.

5.3 Proposed Fast and Low Effort Parameter Identification Concepts

In this section the identification strategy of the proposed concepts is explained, as it differs significantly from concepts shown in other publications. After that, the identification of dynamic parameters, such as the input voltage and the load current, is discussed. Finally, a combined identification concept for the most influential static parameters, the inductance and the capacitance, is shown.

5.3.1 Identification Strategy

System identification in SMPS is the process of identifying the system characteristics of an entire power converter. In contrast, the identification of individual parameters of a power converter is called parameter identification. Usually, parameter identification can be done with lower effort, and can be very effective when identifying the most influential parameters.

Identification approaches are classified in parametric or non-parametric identification [109,125]. Parametric identification is based on a model whose parameters are identified. Consequently, a basic system model, matching the system behavior, is chosen at the beginning. During identification the model parameters are determined. The autotuning by oscillations analysis, the parameter identification based on analog sensing circuitry, both explained in Section 5.2, and the approach proposed in this work belong to this identification class. In contrast, the transfer function of a system is identified in non-parametric approaches by means of transient-response analysis, correlation analysis, and frequency-response analysis without initially specifying a model. The system identification by cross-correlation approaches and the adaptive tuning system for phase margin and crossover frequency, outlined in Section 5.2, belong to this identification class.

This work proposes identification concepts, which differ significantly from the concepts in prior art. This is because most existing concepts are limited by at least one of the following drawbacks:

1. Output voltage disturbances are applied continuously during operation, which makes the design process for the SMPS more difficult [14, 15, 109]. This is because the specified output voltage margin has to be partly reserved for the identification. Consequently, less voltage headroom is available for the regulation of disturbances, Fig 5.5.

2. Design of the control loop is more complex since multiple interacting control loops are added [14,15, 117,118].

3. Complex sets of equations are solved at the expense of extensive hardware overhead [13, 15, 109]. The logic for algebraic operations requires large area in integrated solutions. In [109] a parameter identification concept using cross-correlation and fast fourier transformation (FFT) is implemented with 28,100 gates, which needs already around 1 mm^2 chip area in an ASIC fabricated in a 180 nm BCD technology.

4. Open loop operation or duty cycle freeze during identification interrupt normal operation [104–111, 123].

5. The desired crossover frequency needs to be specified a priori [14, 15, 117, 118]. In boost converters (RHPZ, see Section 3.1), this requires a worst case approach although autotuning is done. The reason is that the maximum crossover frequency is dependent on varying parameters, including the inductance.

6. The identification times are long, during startup (>1 ms) and in operation (>15 ms) [13–15, 109]. In most applications, this is not reasonable, as the output voltage is permanently disturbed. Also, startup time is limited, e.g. in automotive applications typically only 1 ms is available before regular operation including a soft-start output voltage ramp-up, which already takes ∼0.5 ms, Fig. 5.6.

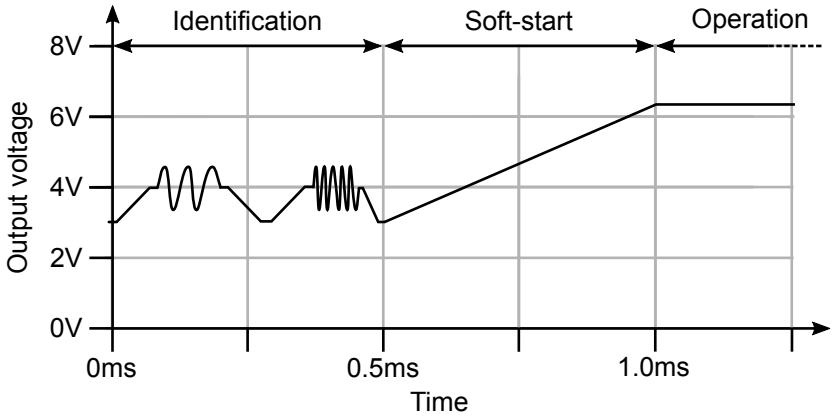

Fig. 5.6: Typical startup sequence of a boost converter in an automotive application: Soft-start with preceding identification period.

A minor additional effort lowers the threshold to apply identification concepts. Therefore, it is beneficial to rely on already available measured parameters. The output voltage V_{out} is digitized with an ADC for the voltage control loop (see Section 4.1) and can be reused for parameter identification. Also, the input voltage V_{in} is often sensed with an ADC for voltage feedforward or sophisticated control concepts [126–128]. The inductor peak current $I_{\text{L,peak}}$ is also available in peak CMC, as it is set by the controller $CtrlOut$. In addition to these available measurements, the on- and off-times of the switch, which are not available in CMC, can be measured by means of digital counters with low hardware effort.

This work aims to identify the most influential parameters in the frequency range of the crossover frequency f_c. Parameters that have only minor influence on the system in this frequency range are neglected. The influential parameters already allow for deriving controller configurations and other actions with sufficient accuracy. In the following it is derived which parameters have the greatest impact on the system in the frequency range of f_c. This is done by analyzing the control-to-output transfer function of the boost converter, which is given in Section 3.1. The analysis is likewise available for buck converters, see Appendix B.1.

Influential Parameters

The influence of individual parameter variations on the control-to-output transfer function T for boost converters is shown in Figures 5.7 to 5.9. In each plot one parameter is subject to variation, all other parameters are considered with nominal values. In a boost converter the maximum crossover frequency f_c is usually chosen not higher than 30 % of the RHPZ, which limits the bandwidth of the control system, see Section 3.1. In Figures 5.7 to 5.9 the targeted crossover frequency range is shaded in gray.

Figure 5.7 shows that inductance variations lead to a negative phase shift in the crossover frequency range endangering control stability. In contrast, the transfer function is not affected by a variation of the inductor series resistance R_L.

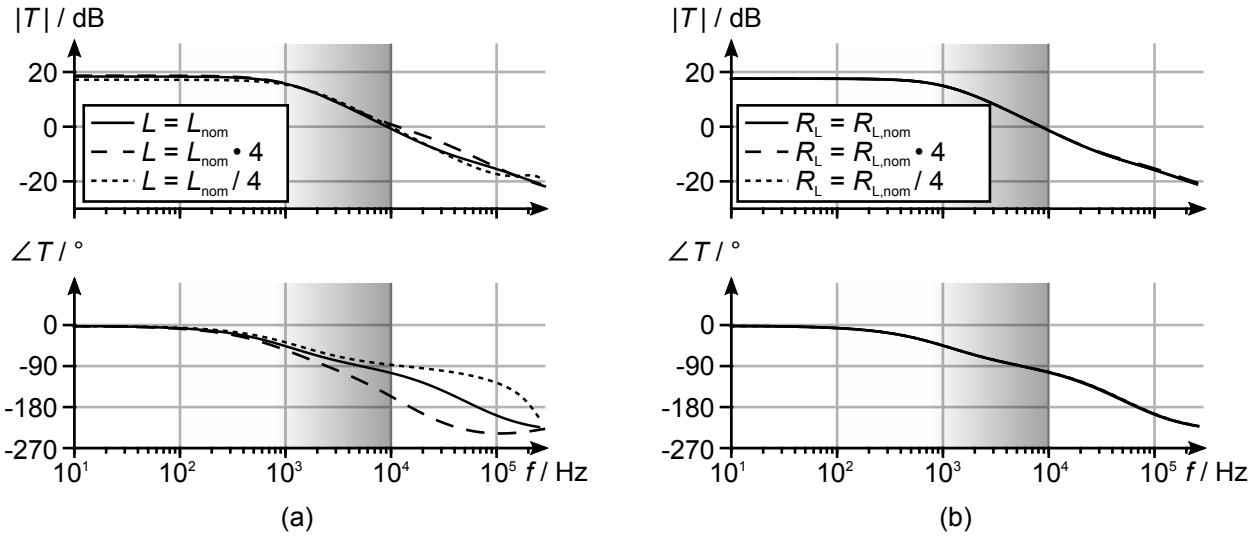

Fig. 5.7: Bode plot of the boost converter control-to-output transfer function for nominal parameters and for a variation (a) of the inductance L and (b) of the series resistance of the inductor R_L by a factor of 4 and 1/4, respectively.

Figure 5.8 indicates that capacitance variations influence the magnitude and, consequently, move the crossover frequency, which impacts control stability and may slow down the control. The capacitor series resistance R_C does not influence the converter behavior.

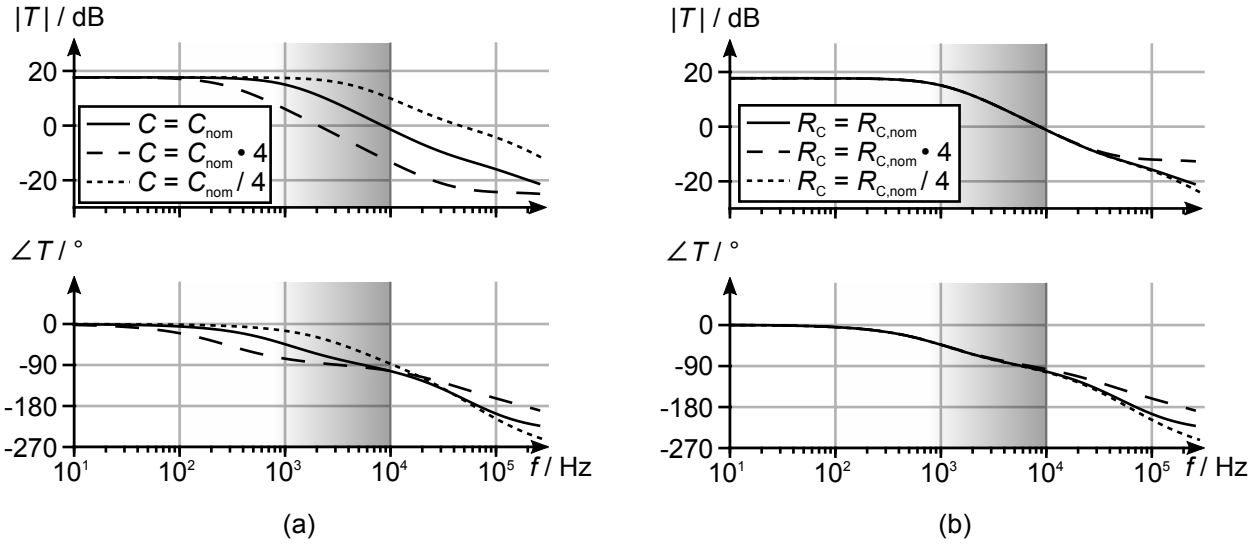

Fig. 5.8: Bode plot of the boost converter control-to-output transfer function for nominal parameters and for a variation of (a) the capacitance C and (b) the capacitor series resistance R_C by a factor of 4 and 1/4, respectively.

As displayed in Fig. 5.9, the influence of the input voltage is only minor, whereas the load resistance R_{load} influences both the magnitude and the phase in the frequency range of interest.

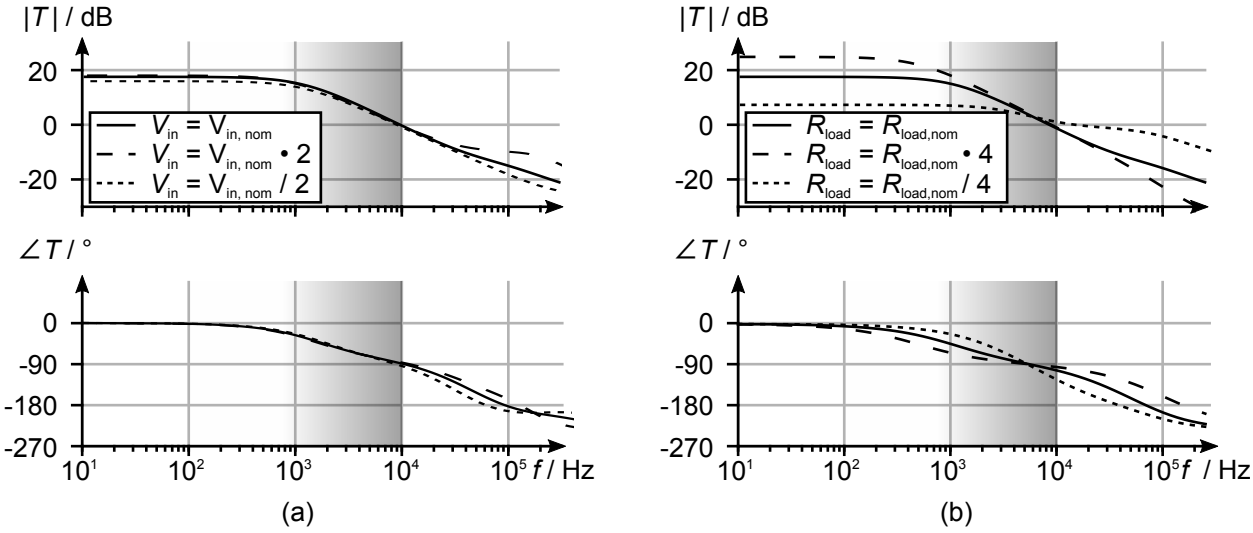

Fig. 5.9: Bode plot of the boost converter control-to-output transfer function for nominal parameters and for a variation of (a) the input voltage V_{in} by a factor of 2 and 1/2 and (b) the load resistance R_{load} by a factor of 4 and 1/4, respectively.

Table 5.1 summarizes the influence of each parameter on magnitude and phase in the investigated frequency range. A '+' denotes that a parameter has a relevant impact on the control-to-output transfer function T, an 'o' indicates small impact, and a '–' that a parameter has only minor or no influence.

Tab. 5.1: Influence of parameters on the boost converter control-to-output transfer function.

Parameter		L	C	R_L	R_C	V_in	R_load
Influence on magnitude	$\lvert T(s)\rvert$	o	+	–	–	o	+
Influence on phase	$\angle T(s)$	+	+	–	–	–	+

In conclusion, the shown figures prove that apart from the operating parameters (V_in, R_load), the inductance L and the capacitance C dominate the transfer function in the frequency range of interest, while other SMPS parameters are of minor influence.

For the sake of completeness according to (3.4), the switching frequency and the shunt resistor for the inductor current measurement in current mode controlled converters (see Fig. 3.4) must be analyzed, too. The switching frequency is either constant or its variation is controlled and, therefore, known. The shunt resistor is designed to provide an accurate current information. Thus, its variation is small, typical commercial shunt resistors show only $\pm 1\,\%$-variation. Thus, their influence on the behavior of the converter is only minor and, therefore, can be neglected.

In the following, concepts for identification of the load, inductance and capacitance are presented. No identification concept is proposed for the input voltage V_in, as digitally controlled SMPS most commonly use a dedicated ADC for this purpose. The knowledge of V_in is useful for input voltage feedforward, for obtaining fast dynamic response, and for improving the power efficiency [126–128]. It is beneficial for improving the bandwidth of a boost converter, as the input voltage influences the RHPZ, which determines the maximum bandwidth, see Section 6.2. Additionally, the input voltage information is valuable for parameter identification concepts for other converter parameters (compare [98] and Section 5.3.3).

The typical input voltage dynamics is slow compared to the output voltage dynamics, i.e. around $1\,\mathrm{V/ms}$ in automotive battery powered applications [129] or even more slow in portable applications [130]. Consequently, in contrast to the output voltage ADC, the sampling rate and latency requirement for the input voltage ADC is minor. Therefore, the use of a $\Delta\Sigma$ ADC is proposed, providing high resolution with small hardware effort, see Section 4.4.

5.3.2 Load Identification

Not only because of the great overall impact on the transfer function of a boost converter, accurate load information is required, but also because of its massive impact on the RHPZ (see Section 6.2.3). Load identification allows for controller adaption and maximized control bandwidth. Besides, it is valuable in temperature monitoring [98] and also for adaptive voltage positioning (Section 2.2 and [101, 131]).

This work proposes a simple, purely digital and lossless load identification, which can be implemented without any additional measurement effort.

The typical inductor and diode current steady-state characteristics of a boost converter is shown in Fig. 5.10. With the help of this current characteristics it is possible to determine a correlation of the controller output signal and the load, which is represented by the load resistance $R_{\text{load}} = V_{\text{out}}/I_{\text{load}}$. The correlation is shown for peak current mode control, it can be similarly derived for valley or average current mode control.

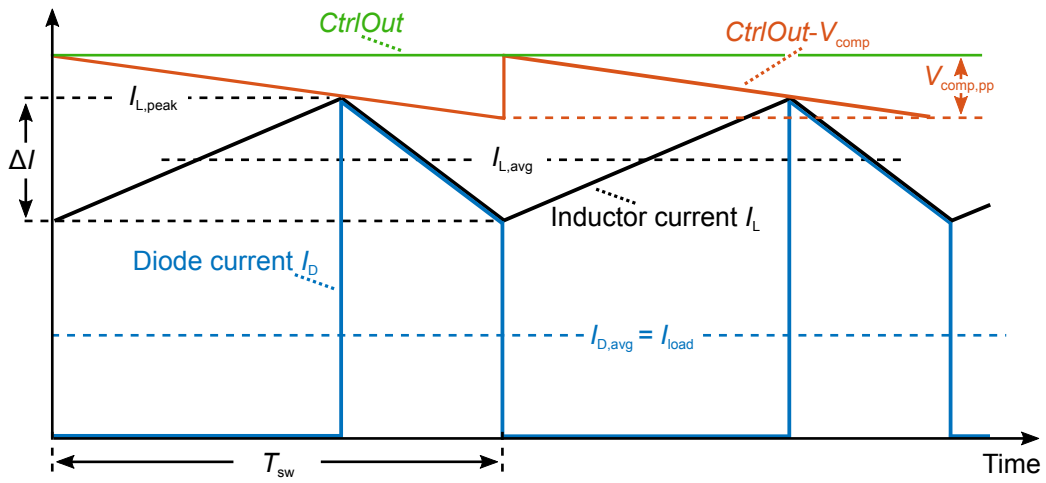

Fig. 5.10: Waveforms of a peak current mode controlled boost converter.

In peak current mode control, the controller output signal *CtrlOut* correlates with the peak inductor current $I_{\text{L,peak}}$. For the current control loop, an inductor current measurement is required. The proposed load identification is independent on the measurement method. Hereafter, a measurement with an equivalent shunt R_{shunt} is assumed. With these quantities the duty cycle D is built in a current mode controlled boost converter, as explained in Section 3.1. If a ramp compensation V_{comp} with a peak-to-peak voltage $V_{\text{comp,pp}}$ is used to prevent subharmonic oscillations [32], the controller output signal correlates with the peak inductor current:

$$I_{\text{L,peak}} = \frac{CtrlOut - V_{\text{comp,pp}} \cdot D}{R_{\text{shunt}}} \tag{5.1}$$

The average inductor current $I_{\mathrm{L,avg}}$ can be expressed with the help of the maximum inductor current $I_{\mathrm{L,peak}}$:

$$I_{\mathrm{L,avg}} = I_{\mathrm{L,peak}} - \frac{\Delta I}{2} \tag{5.2}$$

The current ripple ΔI of a boost converter is a function of the input voltage V_{in}, the duty cycle D, the switching period T_{sw}, and the inductance L:

$$\Delta I = \frac{V_{\mathrm{in}} \cdot D \cdot T_{\mathrm{sw}}}{L} \tag{5.3}$$

In a current mode controlled boost converter the load current I_{load} is equal to the average diode current $I_{\mathrm{D,avg}}$. The average diode current, in turn, is $I_{\mathrm{D,avg}} = (1-D) \cdot I_{\mathrm{L,avg}}$. Therefore, the load resistance $R_{\mathrm{load}} = V_{\mathrm{out}}/I_{\mathrm{D,avg}}$ can be described by:

$$R_{\mathrm{load}} = \frac{V_{\mathrm{out}}}{(1-D) \cdot I_{\mathrm{L,avg}}} \tag{5.4}$$

Hence, it is possible to determine a correlation of the load resistance and the controller output signal with (5.4) by inserting (5.1)-(5.3) for the averaged inductor current $I_{\mathrm{L,avg}}$:

$$R_{\mathrm{load}} = K' \cdot \frac{1}{CtrlOut - A} \tag{5.5}$$

K' and A are defined as:

$$K' = \frac{V_{\mathrm{out}} \cdot R_{\mathrm{shunt}}}{1-D} \tag{5.6}$$

$$A = D \cdot \left(V_{\mathrm{comp,pp}} + \frac{V_{\mathrm{out}} \cdot T_{\mathrm{sw}} \cdot R_{\mathrm{shunt}} \cdot (1-D)}{2L} \right) \tag{5.7}$$

Equation (5.5) allows to determine the latest load of boost converters. A similar expression can be derived for other topologies, e.g. buck converters. The adaption of the controller to the latest load allows for dynamic performance improvement of the control.

Analysis of the Application Range - Load Identification

In this section the most relevant parameters for an accurate identification of the load are derived. Further, it is shown which identification accuracies can be expected depending on the different operating points of the converter, i.e. different input voltages or load currents.

The calculation of the load current I_{load} depends on several parameters as shown in (5.5): $I_{\text{load}} = f(V_{\text{out}}, R_{\text{shunt}}, t_{\text{on}}, T_{\text{sw}}, V_{\text{comp,pp}}, L, CtrlOut)$. In the following, the influence on load identification accuracy is discussed for each parameter, individually.

The output voltage needs to be determined for the control of the SMPS. It is measured with the help of an ADC. Therefore, the measurement inaccuracy is very small. For example, 0.05 % with the 6-bit delay line live-tracking window concept ADC at an output voltage of 6.3 V of this work, see Section 4.1.

A shunt resistor is used for the inductor current measurement. Typical shunt resistors have a maximum inaccuracy not larger than 1 %, which translates into a load identification error with the same relative inaccuracy. Due to the small expected inaccuracy this factor can be neglected.

The on-time measurement is based on digital counters with finite time resolution. Therefore, a load current identification inaccuracy occurs. In the Appendix B.2, this inaccuracy is displayed for different values of the load current to be identified, the present input voltage and the inductance, Fig. B.8. The time measurement inaccuracies only cause approximately 1 % or less error in all operating points and, hence, can be neglected.

The ramp compensation may introduce peak-to-peak inaccuracies. Figure 5.11(a) depicts the influence of an extreme 15 % inaccuracy of the compensation ramp peak-peak voltage with respect to V_{in} and I_{load}. With high load currents and low input voltages the relative identification inaccuracy of the load current is low. For load currents higher than 500 mA the identification inaccuracy is less than 5 % for all input voltages. Compensation ramp trimming reduces the peak-to-peak inaccuracies. If this trimming is applied, the accuracy of the peak-to-peak voltage is significantly increased, which ensures an accurate load identification.

According to Section 5.1, the inductance L underlies variations due to production, temperature, and aging effects. The influence of the inductance inaccuracy on the load current calculation is depicted in Fig. 5.11(b) with respect to the nominal L_{nom} and I_{load}. This analysis assumes an inductance uncertainty of 15 % with respect to the nominal inductance. The relative I_{load} identification inaccuracy caused by inductance variations is low, if the nominal inductance is high and/or the load current is high. For an inductor of a nominal inductance of 5 µH, underlying 15 % inductance inaccuracy, and a load current of 200 mA a maximum load current identification inaccuracy of around 11 % is obtained. For the nominal inductance of 20 µH the load current inaccuracy is less than 3 % for all load currents higher than 200 mA. A concept for inductance iden-

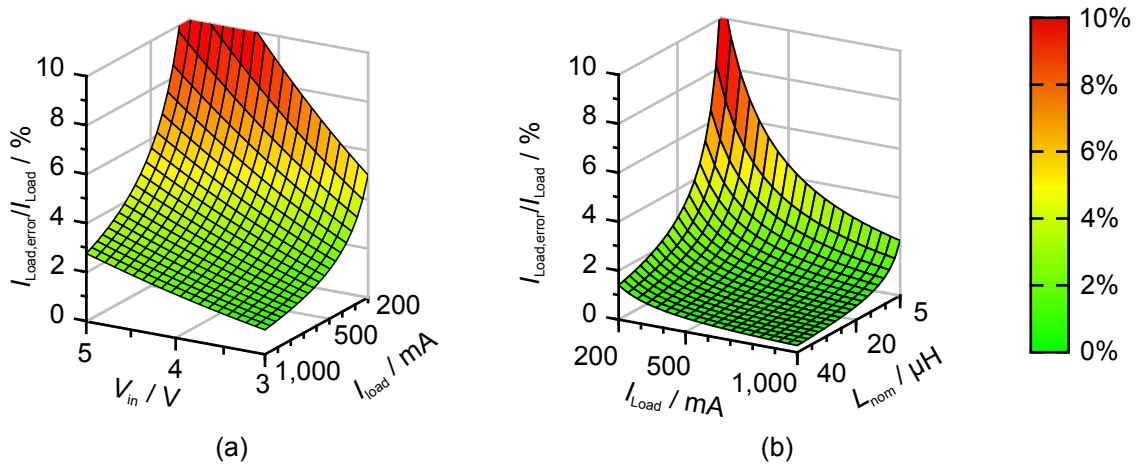

Fig. 5.11: Relative I_{load} identification inaccuracy (a) caused by 15 % compensation ramp inaccuracy as function of the input voltage V_{in} and the load current I_{load} and (b) caused by 15 % inductance inaccuracy as function of the inductance L and the load current I_{load}.

tification is shown in the following section. The load identification works with very small inaccuracies at high load currents and high inductor values.

In the proposed identification method, *CtrlOut* is used to set an peak inductor current. While setting it, offset errors may apply, since there are transfer blocks used, such as a DAC. Offset trimming allows for eliminating any offset errors of these transfer blocks, including the DAC. Therefore, the setting of the peak inductor current does not contribute to inaccuracies of the load identification. Thus, it can be neglected.

In summary, the proposed load identification relies on several parameters. The analysis of this section has shown that an accurate identification is possible, as many parameters are well-known or are accurately determined by simple actions, such as inductance identification and ramp compensation trimming. This will be confirmed experimentally, see Section 5.4.3.

5.3.3 Combined Inductance and Capacitance Identification

According to Section 5.3.1 the inductance and the capacitance are the most influential static parameters of SMPS. Consequently, the identification of these parameters is most important. The following inductance and capacitance identification concept is shown for boost converters. It can also be applied to buck converters with even simpler implementation, see Appendix B.1. Since the identification algorithm is developed for a common identification, the concept allows for an identification of both, the inductance and the capacitance, at the same time.

Startup Identification Scheme

The inductance identification approach is to evaluate the inductor current ramp-up with turned on switch and calculate the inductor $L = V_L \cdot \frac{t_{on}}{I_{L,peak}}$. Therefore, a peak inductor current $I_{L,peak}$ is set by the controller, which leads to the ramp-up.

The capacitance identification approach is to evaluate the output voltage increase resulting from delivering a known amount of charge to the output capacitor.

In Fig. 5.12 the proposed identification algorithm is shown in a flowchart. Figure 5.13 depicts the switch signal S, the inductor current i_L, and the output voltage V_{out} for the startup identification. The identification is composed of two identification phases (① and ②). The first identification phase is started by setting the inductor peak current $I_{L,peak1}$. The switch is turned on and the inductor current i_L increases from a DC current $i_{L,DC}$ to $I_{L,peak1}$ and is then turned off. After the switch is turned off, the inductor current i_L commutates from the switch to the diode and the output capacitor is charged. During this process the inductor current i_L decreases. The output voltage increases until i_L reaches its DC value $i_{L,DC}$ again. At this point of time no further charge is provided to the output capacitor and the output voltage reaches its maximum value $V_{out,max1}$ after the time Δt_1. Times t_{on1}, Δt_1, and $V_{out,max1}$ are measured. After the first identification phase, the output capacitor is discharged slowly, as there are typically high ohmic loads during

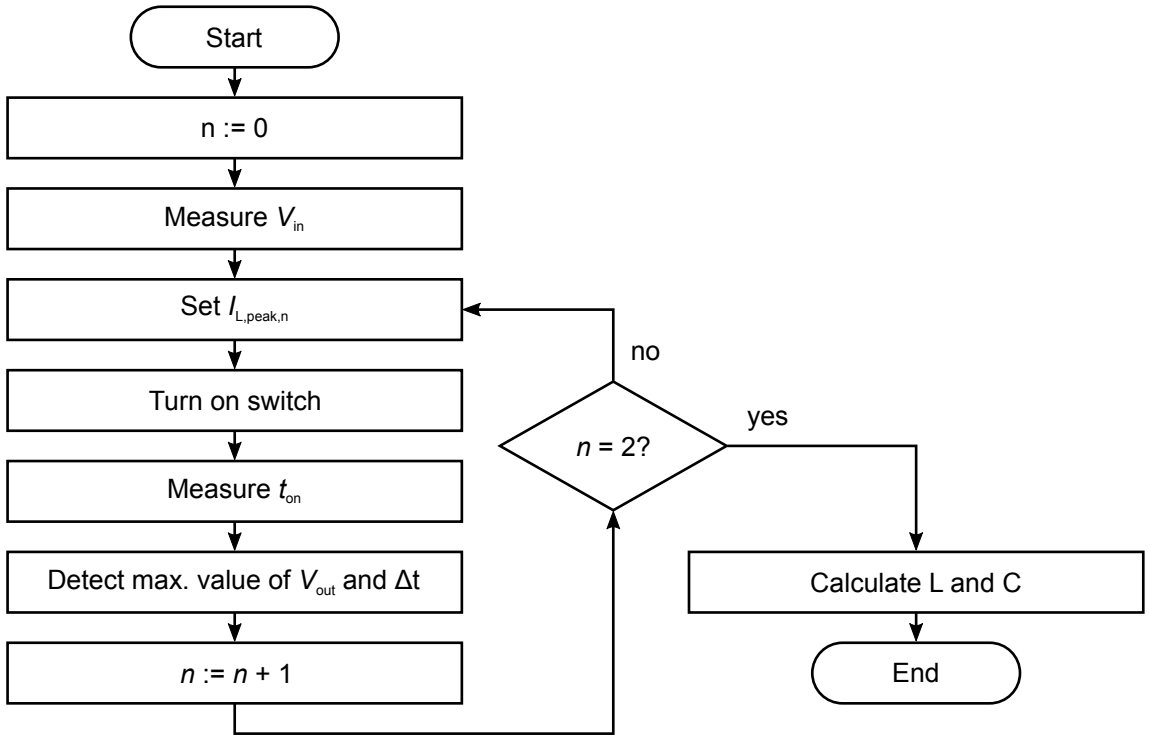

Fig. 5.12: Two pulse startup characterization flowchart.

startup (load not activated). In the second phase, a higher inductor peak current $I_{\mathrm{L,peak2}}$ is chosen. Again, quantities are measured (t_{on2}, Δt_2, and $V_{\mathrm{out,max2}}$).

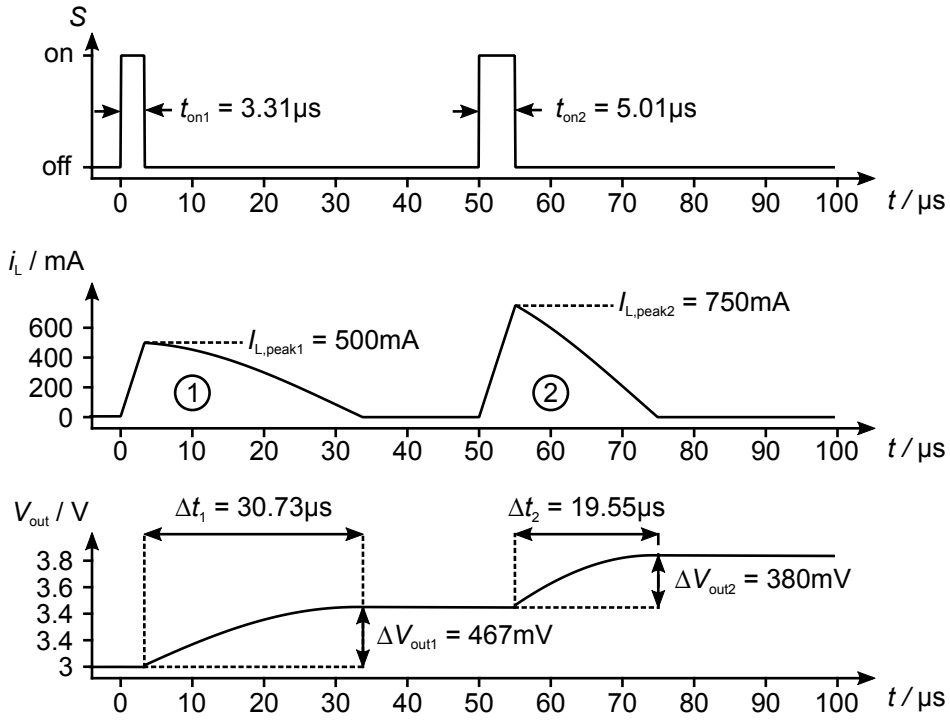

Fig. 5.13: Switch state S, inductor current i_{L} and output voltage V_{out} during the two pulse startup identification process.

The peak inductor current $I_{\mathrm{L,peak}}$ is set in order to ramp up the inductor current. Inductor current measurement, digital-to-analog conversion, and comparator may contribute to peak inductor current offset errors. For compensation of these offset errors the inductor current is ramped up two times (① and ②), consecutively. Consequently, the calculation of the inductance L considers the difference of two peak inductor current values ($\Delta I_{\mathrm{L,peak}} = I_{\mathrm{L,peak2}} - I_{\mathrm{L,peak1}}$) eliminating any offset errors and follows:

$$L = V_{\mathrm{L}} \cdot \frac{t_{\mathrm{on2}} - t_{\mathrm{on1}}}{\Delta I_{\mathrm{L,peak}}} \tag{5.8}$$

In good approximation, it can be assumed that the inductor voltage V_{L} is equal to V_{in}. However, $R_{\mathrm{DS,on}}$ causes a voltage drop that leads to a reduced and non-static inductor voltage V_{L}, which, in turn, influences the inductor current slope:

$$V_{\mathrm{in}} = R_{\mathrm{DS,on}} \cdot i_{\mathrm{L}} + L \cdot \frac{di_{\mathrm{L}}}{dt} \tag{5.9}$$

This effect needs to be incorporated in order to achieve a sufficiently precise identification result. As part of

this work, a simple compensation of the voltage drop across $R_{\mathrm{DS,on}}$ is proposed. While the switch is turned on, the inductor current i_{L} is increasing almost linearly, which leads to a linearly increasing voltage drop. The inductor voltage can be well approximated by its average value $V_{\mathrm{L,avg}}$ during the identification:

$$V_{\mathrm{L,avg}} = V_{\mathrm{in}} - R_{\mathrm{DS,on}} \cdot \frac{I_{\mathrm{L,peak1}} + I_{\mathrm{L,peak2}}}{2} \tag{5.10}$$

Equation (5.8) changes to:

$$L = \frac{V_{\mathrm{in}} - R_{\mathrm{DS,on}} \cdot \dfrac{I_{\mathrm{L,peak1}} + I_{\mathrm{L,peak2}}}{2}}{I_{\mathrm{L,peak2}} - I_{\mathrm{L,peak1}}} \cdot (t_{\mathrm{on2}} - t_{\mathrm{on1}}) \tag{5.11}$$

This equation is used for identification of the inductance.

In the following, the capacitance identification algorithm is described. When the switch is turned off, the inductor current is delivered to the output capacitor and to the load. In good approximation, the inductor current follows a triangle shape and its average value (minus I_{load}) supplies the capacitor: $I_{\mathrm{C}} = \frac{I_{\mathrm{L,peak}}}{2} - I_{\mathrm{load}}$. The charging of the output capacitor leads to an increase of the output voltage ΔV_{out} until the inductor current equals the load current. This point in time is determined with the standard output voltage measurement, as at this instant the output voltage reaches its maximum value after Δt:

$$\Delta V_{\mathrm{out}} = \frac{I_{\mathrm{C}}}{C} \cdot \Delta t = \frac{I_{\mathrm{L,peak}}/2 - I_{\mathrm{load}}}{C} \cdot \Delta t \tag{5.12}$$

By charging the output capacitor two subsequent times, two output voltage differences ΔV_{out} are measured. By considering both output voltage differences, the load term in (5.12) disappears. Consequently, the need for an additional measurement of the load current is avoided. Let the voltage increase resulting from the first charging be ΔV_{out1} and the voltage increase resulting from the second charging be ΔV_{out2}. By rearranging (5.12) and considering the double charging, the capacitance identification formula becomes:

$$C = \frac{I_{\mathrm{L,peak2}} - I_{\mathrm{L,peak1}}}{2 \cdot \left(\dfrac{\Delta V_{\mathrm{out2}}}{\Delta t_2} - \dfrac{\Delta V_{\mathrm{out1}}}{\Delta t_1} \right)} \tag{5.13}$$

Equation (5.11) allows for identification of the inductance and (5.13) for the capacitance, respectively.

The identification of both the inductance and the capacitance can be improved by adding a third phase to the identification pattern. For this reason, one additional current triangle ① is placed in front of the first

actual identification phase. Figure 5.14 shows the switch signal S, the inductor current i_L and the output voltage V_{out} for this case. The first current increase ① is not used for identification purposes, but in order to obtain a short overall identification time. This is because the current triangles can be applied with shorter time delay after each other. A more accurate inductance and capacitance identification is obtained, too.

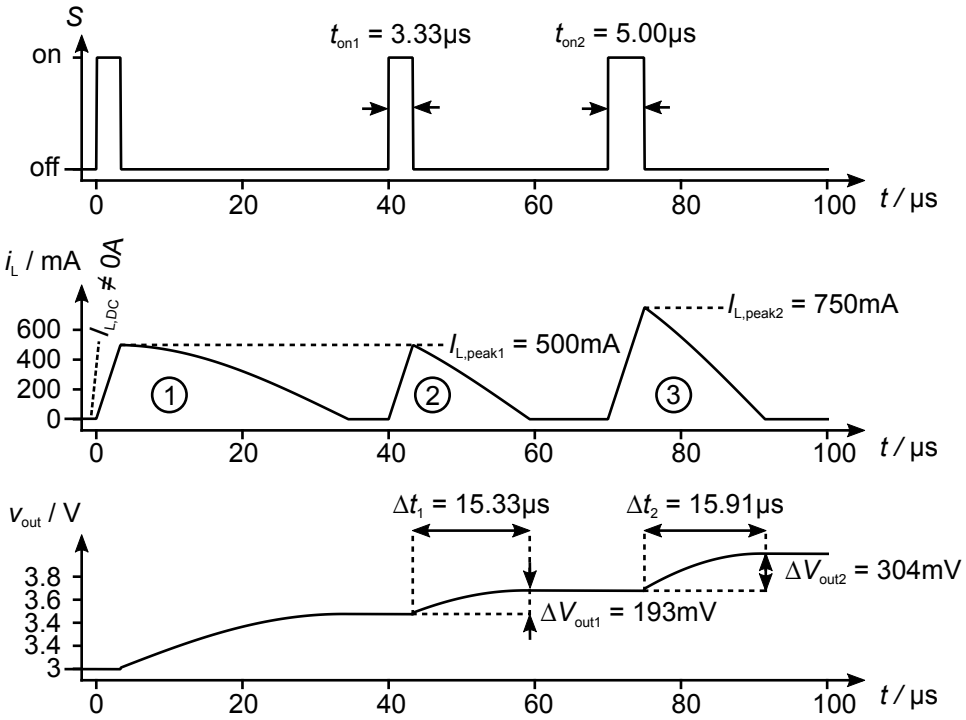

Fig. 5.14: Switch state S, inductor current i_L and output voltage V_{out} during the three pulse startup identification process.

A DC current $I_{L,DC}$ may flow in the inductor before operation, since there might be a small resistive load, Fig. 5.14. With a third current triangle, the inductor current starts from 0 A in the two subsequent identification ramp-ups ② and ③, as the output voltage is increased through this first current ramp-up ① due to the light load in startup. Thus, the diode D blocks, once the inductor current has ramped down as the output voltage is higher than the input voltage of the converter. Consequently, the inductor current starts from 0 A in every subsequent ramp-up. Therefore, the inductor current start value is equal and independent of the load. Thus, the inductance identification precision is improved.

The capacitor identification relies on a linear decrease of the inductor current. Any parasitic resistance in the inductor current path causes a slight nonlinearity. A more precise capacitance identification is achievable for increased output voltage, because the resistive voltage drop becomes negligible compared to the inductor voltage drop. This reduces the nonlinearity. This is why the first inductor current ramp-up ① is applied in addition to the advantages of equal inductor current starting values for the identification and short identification duration.

Analysis of the Application Range – Startup Inductance Identification

This subsection derives, which parameters are most relevant for an accurate inductance identification. Further, it is shown which identification accuracies can be expected depending on the operating points of the converter, i.e. different input voltages and inductance values.

The inductance identification is dependent on the inductor voltage, the difference of two measured switch on-times, and the difference of two set inductor peak currents: $L = f(V_\mathrm{L}, \Delta t, \Delta I_\mathrm{L,peak})$. Each inaccuracy in the measurement or setting of these parameters contributes to an inaccuracy of the inductance identification and is discussed below.

The inductor voltage, in turn, depends on the input voltage, the chosen inductor peak current, and the switch on-resistance: $V_\mathrm{L} = f(V_\mathrm{in}, I_\mathrm{L,peak}, R_\mathrm{DS,on})$. The input voltage V_in is usually measured with high ADC resolution. When utilizing a 0-to-6 V ADC with 10-bit resolution ($6\,\mathrm{V}/2^{10} = 6\,\mathrm{mV/LSB}$) in an application with an input voltage of $V_\mathrm{in} = 3\,\mathrm{V}$, a measurement inaccuracy well below 1 % is obtained ($1\,\%\,\mathrm{of}\,3\,\mathrm{V} = 30\,\mathrm{mV}$). Consequently, the inaccuracy caused by the input voltage measurement can be neglected.

The inductor voltage V_L is described by a differential equation (5.9), which can only be solved at the expense of extensive hardware. Thus, an approximation (5.10) is introduced, which naturally leads to an inaccuracy. This inaccuracy is investigated with an assumed current slope from 0 A to $I_\mathrm{L,peak}$. The differential equation (5.9) is solved. With this solution, a reference value for the inductance is determined. This value is compared to the inductance, which is obtained from the identification using the approximated voltage $V_\mathrm{L,avg}$, introduced in (5.10). Figure 5.15 shows the inductance identification inaccuracy caused by the inductor voltage approximation for different inductor peak currents $I_\mathrm{L,peak}$, the present input voltage V_in and the switch on-resistance $R_\mathrm{DS,on}$.

Figure 5.15(a) proves that for $R_\mathrm{DS,on} = 500\,\mathrm{m\Omega}$ (and smaller) the inductor identification inaccuracy, resulting from the inductor voltage approximation, is less than 1.5 % for all depicted combinations of V_in and the chosen $I_\mathrm{L,peak}$. Figure 5.15(b) indicates that the approximation becomes inaccurate for a combination of high peak inductor current choices and high on-resistances of the switch. This is because the resistive voltage drop at the on-resistance of the switch is high in these cases. Hence, the inductor voltage approximation becomes inaccurate.

The accuracy of $\Delta I_\mathrm{L,peak} = I_\mathrm{L,peak2} - I_\mathrm{L,peak1}$ depends on the accuracy of the setting of the peak currents. This is determined by the DAC resolution and the shunt resistance R_shunt. Typically, the set peak current may show an offset error, which is non-relevant due to the used current difference in (5.11). Consequently, the inaccuracy of the setting of the peak inductor current contributing to inductance identification inaccuracies is of minor influence and can be neglected.

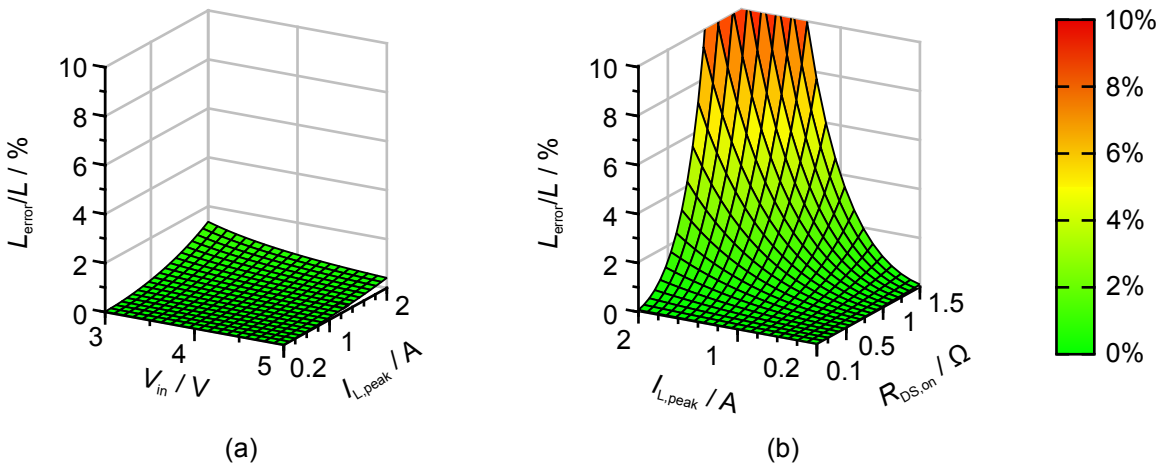

Fig. 5.15: Maximum relative inductance calculation inaccuracy caused by inductor voltage approximation as a function of (a) $I_{\mathrm{L,peak}}$ and V_{in} with $R_{\mathrm{DS,on}} = 500\,\mathrm{m\Omega}$ and (b) $I_{\mathrm{L,peak}}$ and $R_{\mathrm{DS,on}}$ with $V_{\mathrm{in}} = 3\,\mathrm{V}$.

The on-time difference $\Delta t_{\mathrm{on}} = t_{\mathrm{on2}} - t_{\mathrm{on1}}$ is measured with digital counters. These counters operate based on a clock $f_{\mathrm{clk}} = 1/T_{\mathrm{clk}}$ and, thus, have a finite resolution. A high resolution is favorable, but increases the power consumption. In worst-case, the time measurement of t_{on1} has an error of $+T_{\mathrm{clk}}/2$ and t_{on2} has an error of $-T_{\mathrm{clk}}/2$, or vice versa. Hence, the term $t_{\mathrm{on2}} - t_{\mathrm{on1}}$ has a maximum absolute error of $t_{\mathrm{error}} = 1 \cdot T_{\mathrm{clk}}$. A digital clock of $f_{\mathrm{clk}} = 125\,\mathrm{MHz}$ for operating the counters for the time measurements is assumed in the following. The absolute value of $t_{\mathrm{on2}} - t_{\mathrm{on1}}$, which has to be measured, varies depending on the input voltage V_{in}, the inductance L and the inductor peak current difference $\Delta I_{\mathrm{L,peak}} = I_{\mathrm{L,peak2}} - I_{\mathrm{L,peak1}}$. Figure 5.16 shows the inductance identification inaccuracy resulting from the time measurement inaccuracy. It is plotted (a) as function of $\Delta I_{\mathrm{L,peak}}$ and L with constant input voltage $V_{\mathrm{in}} = 3\,\mathrm{V}$ and (b) as function of $\Delta I_{\mathrm{L,peak}}$ and V_{in}, assuming a constant inductance $L = 20\,\mu\mathrm{H}$. In order to obtain a small worst-case inductance identification

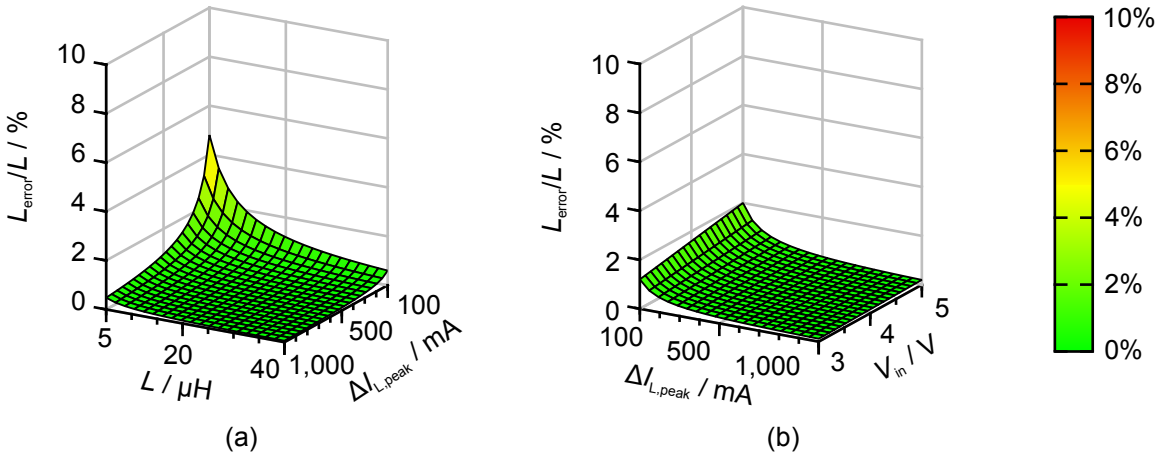

Fig. 5.16: Relative inductance measurement inaccuracy caused by a time measurement inaccuracy as a function of (a) L and $\Delta I_{\mathrm{L,peak}}$ with $V_{\mathrm{in}} = 3\,\mathrm{V}$ and (b) V_{in} and $\Delta I_{\mathrm{L,peak}}$ with $L = 20\,\mu\mathrm{H}$.

inaccuracy of less than 2 % at all depicted inductances and input voltages, it is recommended to choose $\Delta I_{\mathrm{L,peak}} \geq 250\,\mathrm{mA}$.

Figure 5.17 shows the worst-case inductance identification inaccuracy caused by a time measurement inaccuracy as function of the clock frequency f_{clk} used for the on-time measurement, the input voltage V_{in} and the inductance L. The inductor peak current difference $\Delta I_{\mathrm{L,peak}}$ equals 250 mA as recommended above. With a clock frequency of 50 MHz, a relative time measurement inaccuracy of up to 5 % has to be considered. At 125 MHz the maximum relative inaccuracy is lower than 2 %.

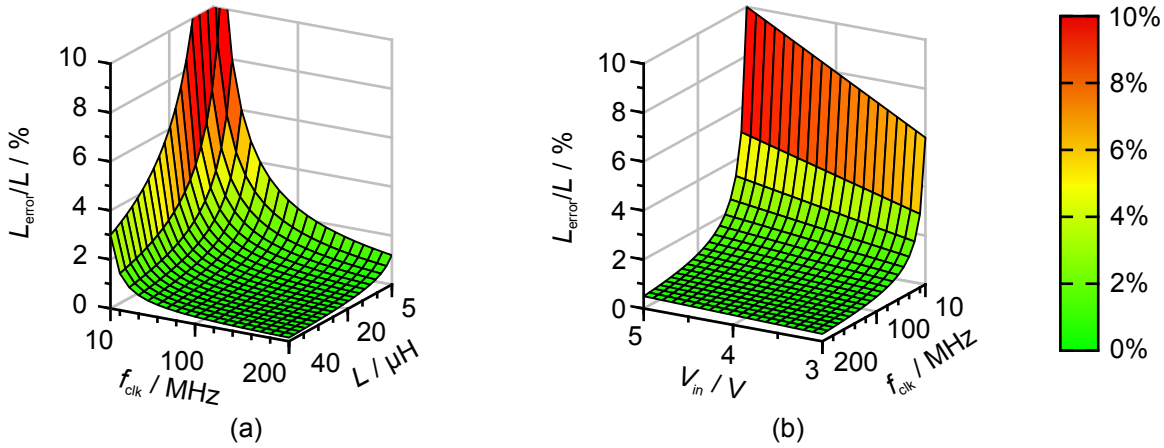

Fig. 5.17: Relative inductance measurement inaccuracy caused by a time measurement inaccuracy as a function of (a) L and f_{clk} with $V_{\mathrm{in}} = 3\,\mathrm{V}$ and (b) V_{in} and f_{clk} with $L = 20\,\mu\mathrm{H}$.

In conclusion, the inductance identification inaccuracy is dominated by the time measurement and the proposed approximation of the inductor differential equation. The inductor peak currents $I_{\mathrm{L,peak1}}$ and $I_{\mathrm{L,peak2}}$ can be chosen deliberately. A difference greater than or equal to 250 mA (Fig. 5.16) and absolute values lower than 1 A (Fig. 5.15(b)) leads to high identification accuracy. Therefore, $I_{\mathrm{L,peak1}} = 250\,\mathrm{mA}$ and $I_{\mathrm{L,peak2}} = 750\,\mathrm{mA}$, which results in $\Delta I_{\mathrm{L,peak}} = 500\,\mathrm{mA}$, is recommended. Further, a high resolution for the time measurement leads to the best identification results, but increases the power consumption. Offset errors of the inductor peak current setting do not contribute to identification inaccuracies due to the smart identification scheme.

Analysis of the Application Range – Startup Capacitance Identification

This section investigates which parameters are most relevant for an accurate capacitance identification. Further, it is shown which identification accuracies can be expected depending from the different operating points of the converter. The calculation of the capacitance is based on (5.13). Thus, $C = f(\Delta I_{\mathrm{L,peak}}, \Delta t, \Delta V_{\mathrm{out}})$ accounts.

The inaccuracy of the inductor peak currents $\Delta I_{\mathrm{L,peak}}$ is discussed in the previous subsection. It has minor influence, since offset errors are eliminated by concept. Therefore, it can be neglected. Consequently, for the analysis of the expected identification accuracy, the influence of Δt and ΔV_{out} must be investigated.

The time measurement Δt is based on digital counters using a clock, as explained in the previous subsection. For the capacitance identification, the time of the falling inductor current slope is measured. The resulting inaccuracy as a function of the inductor L and the digital clock f_{clk} is shown in Fig. 5.18. The peak inductor currents are chosen to $I_{\mathrm{L,peak1}} = 250\,\mathrm{mA}$ and $I_{\mathrm{L,peak2}} = 750\,\mathrm{mA}$, which is suitable for the inductance identification (see previous subsection). The analysis shows that the identification inaccuracy is lower than 2 % for a clock higher than 100 MHz for all inductances within the depicted range.

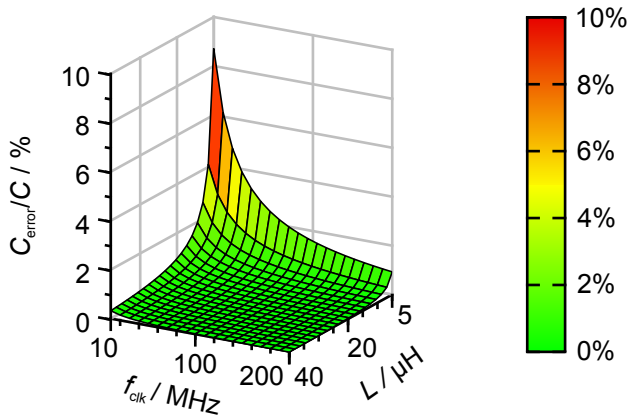

Fig. 5.18: Capacitance identification inaccuracy caused by a time measurement inaccuracy for different inductors L and various counter clocks f_{clk}.

The output voltage V_{out} is measured with an ADC. Typical output voltage swings of 200 mV to 400 mV have to be measured during the identification, see Fig. 5.27. An inaccuracy of $\pm\mathrm{LSB}/2$ may occur in an absolute voltage measurement. Consequently, the maximum voltage difference measurement error is $1 \cdot \mathrm{LSB}$. This leads to a relative voltage measurement inaccuracy of up to 1.5 % with $V_{\mathrm{LSB}} = 3\,\mathrm{mV}$, which is the resolution of the used delay line ADC, see Section 4.1. ADCs with lower resolution lead to worse identification results. In case of $V_{\mathrm{LSB}} = 8\,\mathrm{mV}$ the maximum inaccuracy already reaches 4 %.

A further inaccuracy may result from nonlinearities of the inductor current falling slope due to resistive parasitics in the inductor current path. They lead to a voltage drop comparable to the inductor identification case with rising inductor current, see (5.9). Typically, the equivalent series resistance of the inductor is the main contributor to resistive parasitics, which is still relatively low. A more precise capacitance identification is achievable for larger output voltages. Thus, the resistive voltage drop becomes negligible compared to the inductor voltage drop. The maximum output voltage depends on the application and is determined by the loads, which must not start operation. However, it can be assumed that the inductor voltage drop is multiple times higher than the resistive voltage drop. Thus, the inaccuracy from this nonlinearity can be

considered low and negligible in most cases.

Summarizing all capacitance identification uncertainties, the accuracy is dominated by the output voltage and time measurement resolution. The delay line ADC in this work achieves very small identification inaccuracies smaller than 1.5 % and is, hence, well suitable. With a moderately high digital clock for time measurement, such as 100 MHz, the identification of the capacitor is expected to be very accurate.

Ongoing Operation Identification Scheme

This section presents an inductance and capacitance identification, which can be applied during operation. The concept is similar to the startup identification. The hardware effort is low, as well, since the equations used for identification are derived from the same basis, which will be explained in detail in this subsection. It measures the same quantities as the startup identification. The identification happens even faster than in startup. The identification duration can be as low as one switching cycle (e.g. 2 µs for $f_{\mathrm{sw}} = 500\,\mathrm{kHz}$). This is 7000 times shorter than in prior art in-operation identification concepts. Furthermore, the output voltage disturbance is low.

The proposed concept aims to identify the inductance and the capacitance by manipulating the controller output. A known offset $\Delta I_{\mathrm{L,peak}}$ is added to the controller, which results in an increased inductor peak current in the next switching cycle. The increased inductor peak current is accompanied by a duty cycle increase, which is evaluated and used for the inductance calculation. In the meantime, the output capacitor can be identified by evaluation of the output voltage change over time.

Figure 5.19 displays the identification algorithm in a flowchart, while Fig. 5.20 shows the timing diagram. In the first phase of the concept, starting at $t = -T_{\mathrm{sw}}$, the input voltage V_{in} and the on-time of the switch t_{on1} are measured as a reference. Further, the load current I_{load} is determined by measurement or by the identification shown in Section 5.3.2.

The controller output manipulation takes place at $t = 0$. If the controller output is manipulated by a specified value $\Delta CtrlOut$, the inductor peak current manipulation $\Delta I_{\mathrm{L,peak}}$ can be calculated. Therefore, the duty cycle difference between steady state and manipulated state is measured. The inductance in boost converters can then be calculated using:

$$L = \frac{V_{\mathrm{L}} \cdot (t_{\mathrm{on2}} - t_{\mathrm{on1}})}{\Delta I_{\mathrm{L,peak}}} \tag{5.14}$$

The inductor voltage V_{L} equals the input voltage V_{in} with compensation of the switch on-resistance voltage drop. Thus, it is chosen according to (5.10). If a ramp compensation preventing subharmonic oscillations

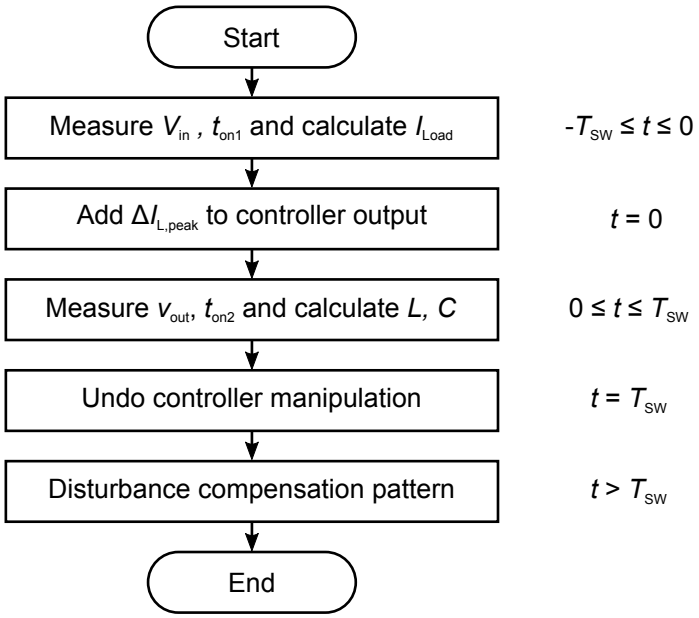

Fig. 5.19: In-operation identification flowchart.

is used, its impact on the peak inductor current has to be considered similar to Section 5.3.2. The ramp compensation voltage can be derived from known parameters during operation.

The capacitor identification approach, which is explained in the following, shares the identification pattern used for the inductor identification.

When the switch in a boost converter is turned on, the load current is provided from the output capacitor. Assuming that the load current is constant during one switching cycle, the output voltage decreases linearly as shown in Fig. 5.20 and the capacitance can be calculated according to:

$$C = \frac{I_{\text{load}}}{dV_{\text{out}}/dt} \tag{5.15}$$

The load current I_{load} is dependent on the absolute output voltage V_{out}. Equation (5.15) assumes a constant load current. This approximation is adequately useful for short time intervals (e.g. few switching cycles), since the load current changes only slightly within one interval. Therefore, the approximation causes only minimum inaccuracy in the proposed identification within one switching cycle. The load current of current mode controlled converters can be either measured or more easily determined from the controller output, as presented in Section 5.3.2.

For identification, multiple output voltage samples are recorded to determine the output voltage-time derivative, Fig. 5.20. This is challenging, as it might be inaccurate due to the limited ADC resolution and the short measurement period. Therefore, a linear regression algorithm is proposed, that helps improving the accu-

racy, see Appendix B.3. Any high-frequency output voltage disturbances are eliminated by the anti-aliasing low-pass filter characteristics of the OTA of the input stage of the ADC, see Fig. 4.8.

At $t = T_{\mathrm{sw}}$ the controller output manipulation is stopped, such that the inductor peak current equals its steady state value $I_{\mathrm{L,peak1}}$ again. The manipulation period inherently leads to an increased output voltage, because the current carried to the output capacitor is increased by the manipulation process, while the load can be assumed to be constant during the identification period. There are two ways to handle the output voltage increase. A first approach lets the controller bring the output voltage back to its set point, which is appropriate as the output voltage deviation is small. The controller senses the increased output voltage and counteracts by decreasing its output $CtrlOut$. The second approach is to introduce a compensation pattern immediately after the manipulation period. The controller output manipulation can be reversed ($-\Delta CtrlOut$) in the switching period after the identification. The inductor peak current is thus reduced for one cycle and the output voltage increase is reversed more quickly than in the first approach. This is recommended for small output voltage disturbances and used in this work.

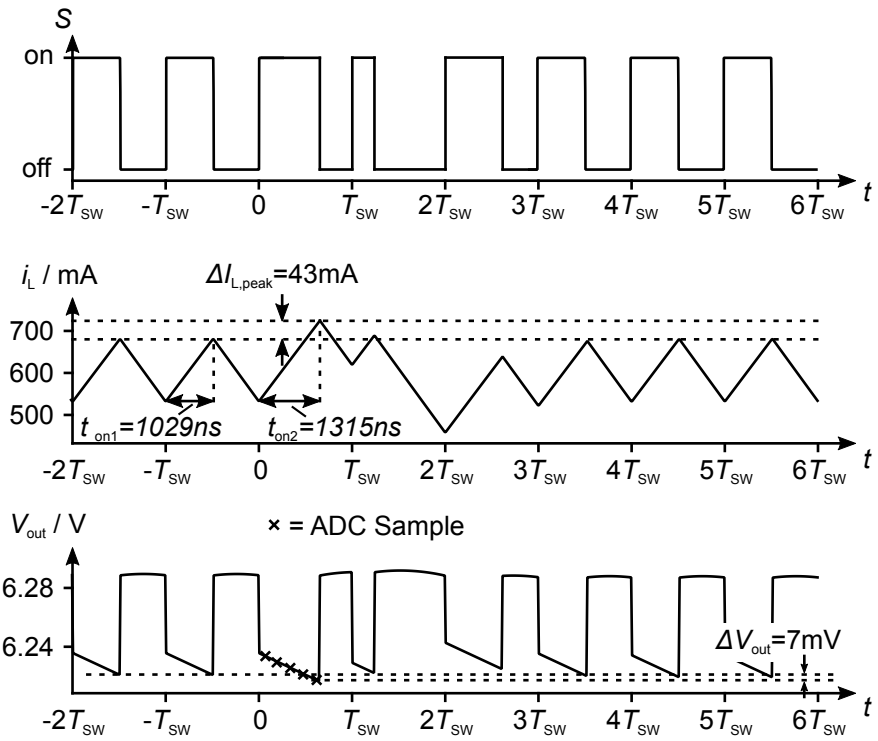

Fig. 5.20: Switch control S, inductor current i_{L}, and output voltage V_{out} during the inductance identification process.

Figure 5.20 confirms that the output voltage is perturbed only slightly. The controller output is manipulated with $-\Delta CtrlOut$ in the period subsequent to the identification period. The inductor peak current in this compensation period, however, is not lower than the steady state peak current (see Fig. 5.20). This can be explained by the influence of the ramp compensation. With smaller duty cycle, the influence of the

ramp compensation is smaller. Figure 5.21 illustrates this issue by means of the inductor current i_L, the demanded current $i_{DAC} = V_{DAC}/R_{shunt}$ and the reference current $i_{ref} = i_{DAC} - V_{comp}/R_{shunt}$. In a current mode controlled boost converter, the reference current i_{ref} is compared to the inductor current i_L and their intersection determines the turn-off of the switch. In the compensation phase starting from $t = T_{sw}$ until $t = 2T_{sw}$, the inductor peak current is similar to the switching cycle before. This is caused by the ramp compensation, although the demanded current value is significantly lower than in the switching cycle before.

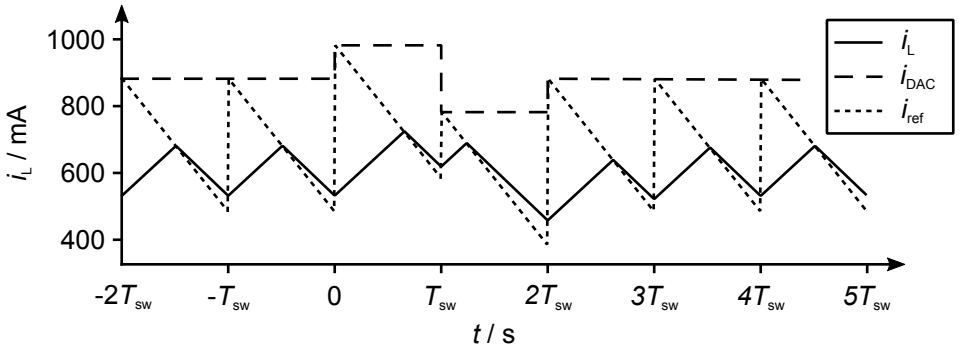

Fig. 5.21: Inductor current i_L, DAC set point i_{DAC} and reference current i_{ref} during the identification process.

In conclusion, the proposed identification pattern can be used for both the inductor and the capacitor, at the same time. Further, a one-cycle compensation pattern is recommended, as it reduces the output voltage disturbance, although the ramp compensation weakens the effect.

Analysis of the Application Range – Inductance Identification

The most relevant parameters for an accurate inductance identification are investigated in this section. Further, it is shown which identification accuracies can be expected depending on the operating points of the converter, i.e. different input voltages and inductance values.

According to (5.14) the inductance is identified on the basis of multiple parameters during operation: $L = f(V_L, \Delta t, \Delta I_{L,peak})$. The influences of these parameters are discussed below.

The input voltage V_{in} minus switch on-resistance voltage drop represents the inductor voltage V_L in (5.14), like for the inductance identification during startup. An approximation for the inductor voltage V_L is introduced in (5.10). It has been shown that the approximation yields accuracies better than 1.5 %, if the on-resistance of the switch $R_{DS,on}$ is smaller than 0.5 Ω.

The accuracy of $\Delta I_{L,peak} = I_{L,peak2} - I_{L,peak1}$ was already analyzed earlier in this section. There has been shown that the inaccuracy of the setting of the peak inductor current contributing to inductance identification inaccuracies is negligible.

The on time difference Δt can be analyzed similar to the startup identification. Only, the $\Delta I_{\mathrm{L,peak}}$ is smaller during operation. A large $\Delta I_{\mathrm{L,peak}}$ leads to a large output voltage disturbance and is, therefore, not wanted. Figure 5.22 displays the inductance identification inaccuracy in a boost converter depending on the choice of $\Delta I_{\mathrm{L,peak}}$, the inductance L to be identified and the input voltage V_{in} during identification. In Fig. 5.22(a) the inductance identification inaccuracy is plotted as function of $\Delta I_{\mathrm{L,peak}}$ and L with constant input voltage $V_{\mathrm{in}} = 3\,\mathrm{V}$. In Fig. 5.22(b) the inductance identification inaccuracy is plotted as function of $\Delta I_{\mathrm{L,peak}}$ and V_{in} with constant inductance $L = 20\,\mu\mathrm{H}$.

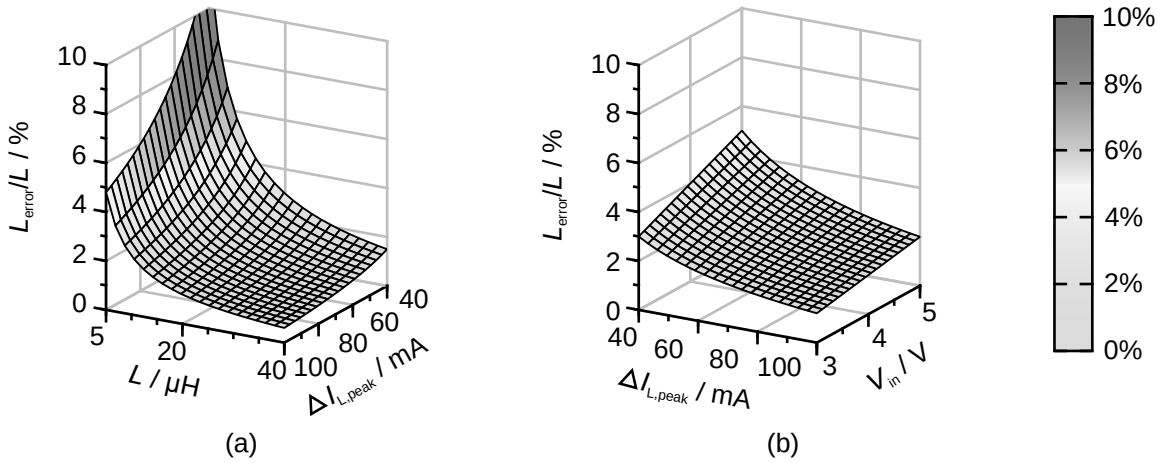

Fig. 5.22: Inductance identification inaccuracy caused by a time measurement inaccuracy as a function of (a) L and $\Delta I_{\mathrm{L,peak}}$ with $V_{\mathrm{in}} = 3\,\mathrm{V}$ and (b) V_{in} and $\Delta I_{\mathrm{L,peak}}$ with $L = 20\,\mu\mathrm{H}$.

In conclusion, the larger the inductor L, the lower the identification inaccuracy. However, the inductance L is given by the application. Also, the input voltage V_{in} is given. A low input voltage promises high identification accuracies. The inductor peak current difference $\Delta I_{\mathrm{L,peak}}$ can be chosen in the algorithm and should be as large as possible according to the graphs. However, a large $\Delta I_{\mathrm{L,peak}}$ also correlates with a high perturbation level. A good trade-off, leading to low inaccuracy and acceptable perturbation level, depends on the application. In the boost converter, whose parameters are listed in Table 3.1, $\Delta I_{\mathrm{L,peak}} = 66\,\mathrm{mA}$ causes only 10 mV output voltage disturbance, which equals less than 0.2 % of the nominal output voltage (6.3 V) at $I_{\mathrm{load}} = 250\,\mathrm{mA}$.

Analysis of the Application Range – Capacitance Identification

The capacitance identification is based on I_{load} and dV_{out}/dt: $C = f(I_{\mathrm{load}}, dV_{\mathrm{out}}/dt)$. The load current I_{load} can be directly measured with high accuracy but also high effort. Alternatively, the load identification in Section 5.3.2 achieves high accuracy. Nevertheless, any load identification inaccuracy maps to a capacitor identification inaccuracy.

As the voltage drop is low and the time period is short, a high resolution and high sample rate ADC is required for good identification results. The delay line ADC, presented in Section 4.1, is well suitable.

When applying several identification runs in a row, the voltage-time derivative dV_{out}/dt can be determined with a linear regression algorithm improving the accuracy of the capacitance identification. Appendix B.3 shows, how a linear regression works, and determines the improvements dependent on the number of samples and identification runs.

Summarizing all uncertainties, both a dV_{out}/dt measurement inaccuracy and a load identification inaccuracy make an accurate identification challenging. However, a linear regression for the output voltage slope measurement and an accurate load identification improve the capacitance identification in operation. In particular, monitoring of the output capacitor, serving as a safety feature, can be implemented with small effort on the basis of the capacitance identification proposed in this work.

5.4 Experimental Verification

This section shows the experimental results for the load, inductor and capacitor identification. For this reason, first, the experimental setup in general is introduced. After that, the dedicated evaluation of the parameter identification concepts is explained.

5.4.1 Test Setup

In this section the test setup is presented, which is used for the parameter identification verification and, also, for the experimental verification of Section 6. The test setup is composed of an IC, fabricated in a 180 nm BCD technology, together with its peripherals, i.e. the filter passives of the various converter configurations, and an FPGA. The IC contains the ADCs, the DACs / DPWM, the FETs, the current sensing for CMC, the ramp compensation, the gate driver, and the analog PWM signal generation, see Fig. 4.26. The digital part is implemented in a Xilinx Spartan-6 FPGA, which is targeted for low-cost applications and has over 100 I/O pins. The digital part could likewise be integrated in the IC. The power path inductors and capacitors (filter passives) of the converters are applied externally, Fig. 5.23.

For the experimental verification, the inductor and the output capacitor can be either set to fixed values or, for parameter identification, set to different inductances and capacitances. Five different inductors (22.0 µH, 11.0 µH, 4.7 µH, 2.0 µH and 1.3 µH) are available and can be put together in any combination. Thus, 29 different inductances from 3.3 µH to 41.0 µH can be utilized. Three different capacitors (22.0 µF, 10.0 µF and 4.7 µF) are available and six different capacitances from 10 µF to 36.7 µF can be applied.

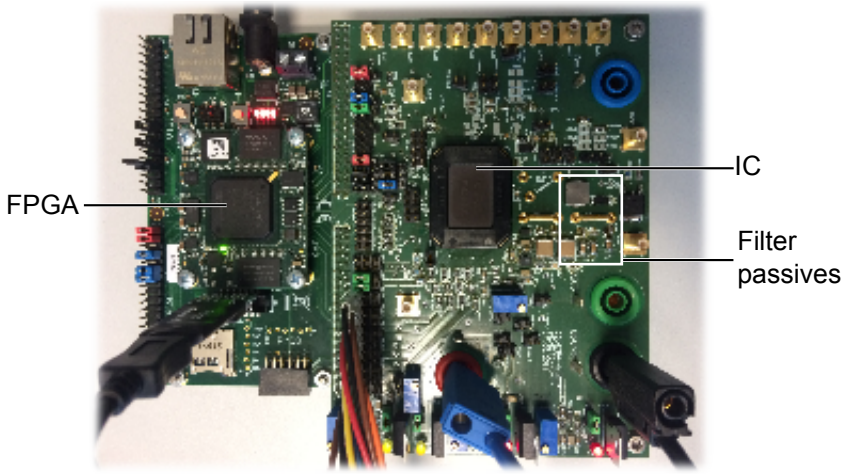

Fig. 5.23: Test setup for experimental verification.

In order to have an exact identification reference both the inductors and the capacitors are characterized with an impedance analyzer. Figure 5.24 shows the frequency characteristics of an exemplary inductor with a nominal inductance $L_{\text{nom}} = 22\,\mu\text{H}$ (type: WE-HCI Flat 1365 from Wurth Electronics). Further, the frequency characteristics of an exemplary capacitor with a nominal capacitance $C_{\text{nom}} = 22\,\mu\text{F}$ (MLCC-SMD from Murata) is depicted.

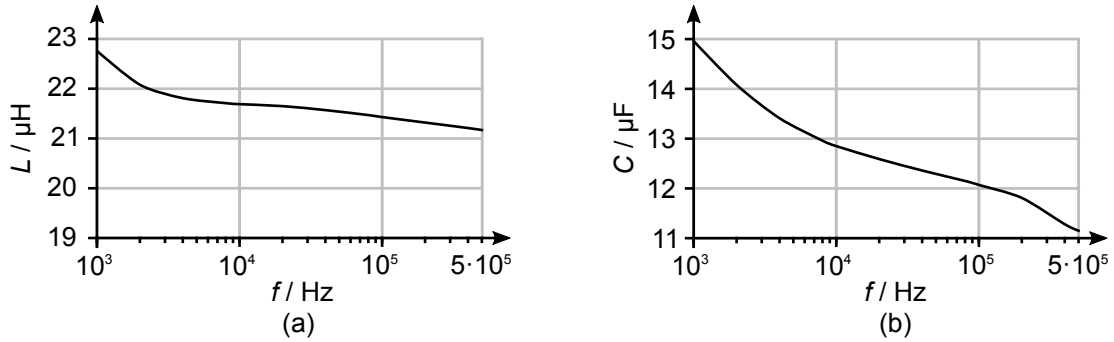

Fig. 5.24: Measured frequency characteristics of (a) an inductor with $L_{\text{nom}} = 22\,\mu\text{H}$ at $I_{\text{bias}} = 0\,\text{A}$ and (b) a capacitor with $C_{\text{nom}} = 22\,\mu\text{F}$ at $V_{\text{bias}} = 6.3\,\text{V}$.

The inductance and the capacitance should be identified at the crossover frequency f_{c}, because stability and performance of the control loop are determined at this frequency. For boost converters, f_{c} is usually chosen not higher than 30 % of the RHPZ, see Equation (3.5). In this work, the RHPZ is $f_{\text{RHPZ}} = 49\,\text{kHz}$ for nominal parameters, see Table 3.1. Therefore, the identification reference measurement is conducted at $f_{\text{c}} = 10\,\text{kHz}$.

In the identification concept for ongoing operation, the inductor is stimulated at the switching frequency ($f = 500\,\text{kHz}$) and not in the crossover frequency range of $f = 10\,\text{kHz}$. Therefore, a measurement inaccuracy is obtained. However, according to the frequency characteristics of the used inductor, Fig. 5.24(a), the

inductance value at $f = 500\,\text{kHz}$ only deviates from the inductance value at $f = 10\,\text{kHz}$ by 2 %.

The inductance of an inductor is not only influenced by the frequency, but also by its DC bias current. The higher the DC current is, the lower the inductance becomes, since the core material tends to saturate with higher currents. There is no nominal value for the inductor DC current in a converter, as it strongly depends on the load situation. Therefore, the inductors used in this work are chosen with regard to constant inductance up to 2 A.

The bias voltage of the capacitors has to be considered as influencing variable. High voltage leads to lower capacitance, mainly because of the dielectric. Figure 5.25 shows the capacitance as a function of the bias voltage V_{bias}. An exemplary 22 µF capacitor is used and the stimulation frequency is set to 1 kHz.

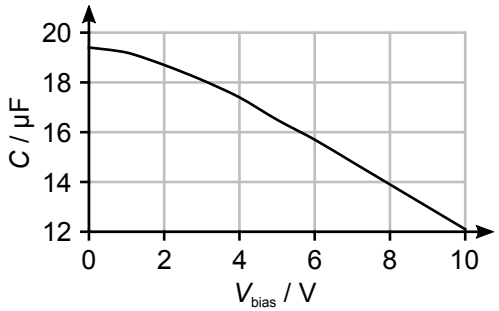

Fig. 5.25: Voltage characteristics of an MLCC-SMD capacitor (Murata) with $C_{\text{nom}} = 22\,\mu\text{F}$ at $f = 1\,\text{kHz}$
.

The reference measurement uses $V_{\text{bias}} = 6.3\,\text{V}$, which is the nominal output voltage of the boost converter. This also explains that the measured capacitance in Fig. 5.24(b) is much lower than its nominal value.

All results of the reference measurement are shown in Appendix B.4. The inductors and capacitors are evaluated at the appropriate frequencies and voltages / currents. Consequently, the measured values deviate from the nominal values. The identification results in the following sections are evaluated based on these reference measurement results.

5.4.2 Load Identification

The relative error of the measured load identification $e = (I_{\text{load,ident}} - I_{\text{load,ref}})/I_{\text{load,ref}}$ is shown in Fig. 5.26. The load current $I_{\text{load,ref}}$ was measured separately as a reference. The inductance is set to 22 µH for all measured data points, since this fits to the standard parameters of the boost converter used in this work, Table 3.1. The experimental results are provided for small load currents, as according to Section 5.3.1 the identification error is higher at small currents. For higher currents the identification is more accurate. The identification error is less than 3 % over the entire current range shown in Fig. 5.26.

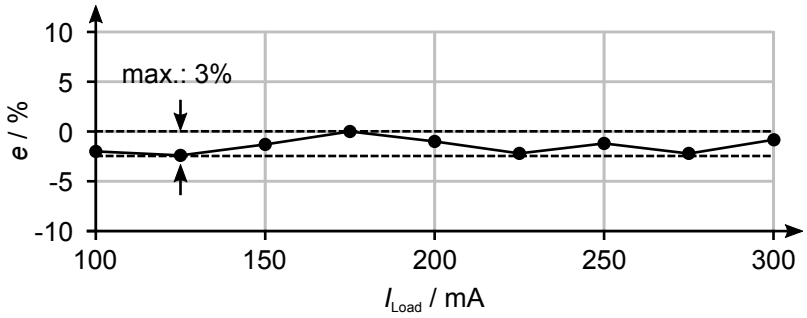

Fig. 5.26: Deviation of the load current identification results from the actual current I_{load}.

5.4.3 Combined Inductance and Capacitance Identification

Startup Identification

Figure 5.27 shows the measurement of the startup identification pattern for the boost converter. The measurement was conducted with $V_{in} = 3.5\,V$, $L_{nom} = 22\,\mu H$, $C_{nom} = 22\,\mu F$ and the parameters of Table 3.1.

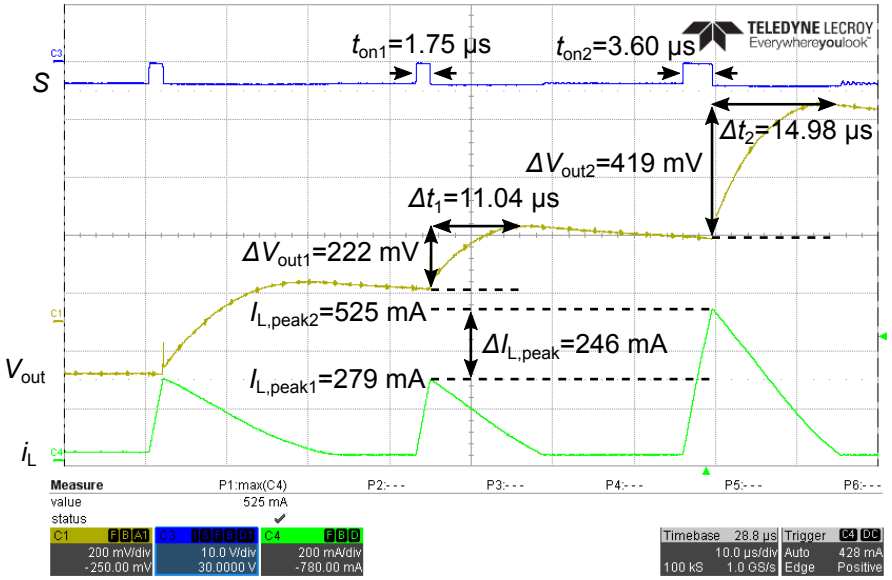

Fig. 5.27: Pulsed startup identification in a boost converter with $V_{in} = 3.5\,V$, $R_{DS,on} = 1.1\,\Omega$, $L = 22\,\mu H$ and $C = 22\,\mu F$.

In the first and the second phase $I_{L,peak}$ is set to 250 mA, in the third phase $I_{L,peak}$ is set to 500 mA. The inductor current is expected to increase until $I_{L,peak}$ is reached. Due to an offset error of the $I_{L,peak}$ setting, discussed in Section 5.3.3, $I_{L,peak}$ deviates from its set value in all three phases. However, the difference between the $I_{L,peak}$ values in phase two and three is 246 mA, which is close to the expectation of 250 mA.

Exemplarily for the shown measurement, the identified inductance can be calculated with the help of the measured values given in Fig. 5.27 and Equation (5.11), derived in Section 5.3.3:

$$\begin{aligned} L &= \frac{V_{\text{in}} - R_{\text{DS,on}} \cdot \dfrac{I_{\text{L,peak1}} + I_{\text{L,peak2}}}{2}}{I_{\text{L,peak2}} - I_{\text{L,peak1}}} \cdot (t_{\text{on2}} - t_{\text{on1}}) \\ &= \frac{3.5\,\text{V} - 1.1\,\Omega \cdot \dfrac{250\,\text{mA} + 500\,\text{mA}}{2}}{500\,\text{mA} - 250\,\text{mA}} \cdot (3.60\,\mu\text{s} - 1.75\,\mu\text{s}) = 22.8\,\mu\text{H} \end{aligned} \tag{5.16}$$

Thus, the inductance is identified to $L = 22.8\,\mu\text{H}$, which equals a deviation of 5 % from the reference value of $L = 21.7\,\mu\text{H}$ (see Fig. 5.24).

Further, the identified capacitance can be calculated based on (5.13), derived in Section 5.3.3:

$$C = \frac{I_{\text{L,peak2}} - I_{\text{L,peak1}}}{2 \cdot \left(\dfrac{\Delta V_{\text{out2}}}{\Delta t_2} - \dfrac{\Delta V_{\text{out1}}}{\Delta t_1} \right)} = \frac{500\,\text{mA} - 250\,\text{mA}}{2 \cdot \left(\dfrac{419\,\text{mV}}{14.98\,\mu\text{s}} - \dfrac{222\,\text{mV}}{11.04\,\mu\text{s}} \right)} = 15.9\,\mu\text{F} \tag{5.17}$$

The identified value is $C = 15.9\,\mu\text{F}$, which deviates by 10 % from the reference value of $C = 14.4\,\mu\text{F}$ (see Fig. 5.25).

The identification results of this concept for different inductors and capacitors are shown in Fig. 5.28 and Fig. 5.29, respectively. The inductance identification is performed for a fixed capacitance of $C_{\text{nom}} = 22\,\mu\text{F}$. The capacitance identification is performed with $L_{\text{nom}} = 22\,\mu\text{H}$. The deviation of each identification is calculated with $e = \frac{p_{\text{ident}} - p_{\text{ref}}}{p_{\text{ref}}}$ where p_{ident} is the identified value (L, C) and p_{ref} is the reference value from the reference measurement (refer to Appendix B.4).

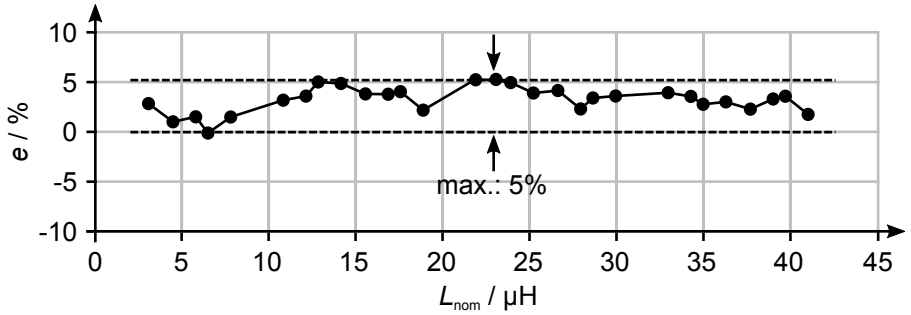

Fig. 5.28: Measured identification deviation of different inductors during startup.

The inductance is identified with less than 5 % identification error across all measured inductances, which is expected according to the analysis of Section 5.3.3. The analysis forecasts small identification errors

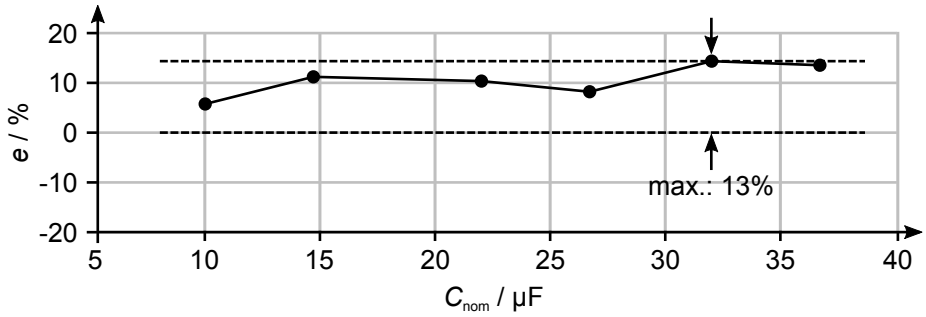

Fig. 5.29: Measured identification deviation of different capacitors during startup.

with good time resolution for the measured switch on-time. A digital clock $f_{\mathrm{clk}} = 125\,\mathrm{MHz}$ is used. Small identification errors can be expected, when the peak inductor values are well below 1 A. They are chosen, accordingly. The capacitance identification has an inaccuracy of $6-13\,\%$. The constant inaccuracy for the capacitances can be explained by the fact that the capacitances are not identified at their nominal output voltage. The exemplary voltage characteristics in Fig. 5.25 show that the 22 µF capacitor has a capacitance of 17.8 µF at 3.5 V and 15.7 µF at 6 V, which equals a deviation of around 13 % and, therefore, explains the identification inaccuracy. Apart from this deviation, the identification is accurate, since the delay line ADC for the output voltage provides high resolution. Precise output voltage measurement is required for accurate identification according to the analysis of Section 5.3.3.

In the following, the inaccuracies resulting from the excitation signal shapes are analyzed for both the inductor and the capacitor identification. The inductor is stimulated with a voltage pulse of around 2 µs to 4 µs. The pulse length depends on the input voltage V_{in}, the inductance L and the inductor peak current $I_{\mathrm{L,peak}}$. Assuming a pulse length of 4 µs, Fig. 5.30(a), the single-sided stimulation frequency spectrum looks as shown in Fig. 5.30(b). The frequency spectrum is generated by a numerical computation in MATLAB. The inductor is stimulated in a broad range of frequencies and not explicitly at the crossover frequency, which may lead to identification inaccuracies. As shown exemplarily in Fig. 5.24(a) the inductance of a 22 µH inductor lies between 21 µH and 23 µH in the frequency range from 1 kHz to 500 kHz, which equals a deviation of $\pm 5\,\%$ from the nominal value.

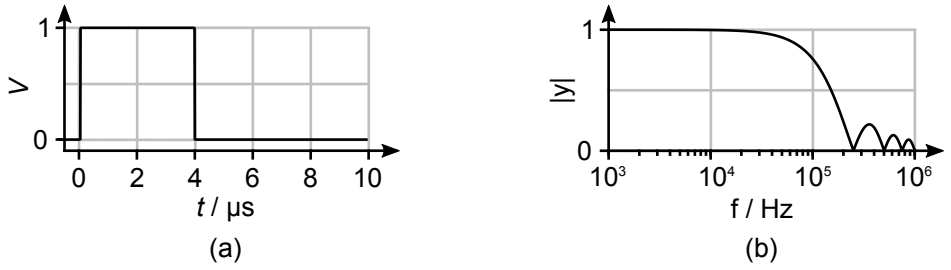

Fig. 5.30: Normalized voltage pulse (a) in time domain and (b) in frequency domain.

The capacitor is stimulated with a characteristic current triangle, Fig. 5.31(a), which simulates the linear inductor current decrease. It is around 10 µs to 20 µs long. The length depends on the input voltage V_{in}, the inductance L, the capacitance C and the inductor peak current $I_{\text{L,peak}}$. Assuming a pulse length of 20 µs, the single-sided stimulation frequency spectrum looks as shown in Fig. 5.31(b). The capacitor is also not explicitly stimulated at the crossover frequency, which leads to measurement inaccuracies. In Fig. 5.24(b) it is shown that the capacitance of a 22 µF capacitor, biased with 6 V, lies between 11 µF and 15 µF in the frequency range from 1 kHz to 500 kHz.

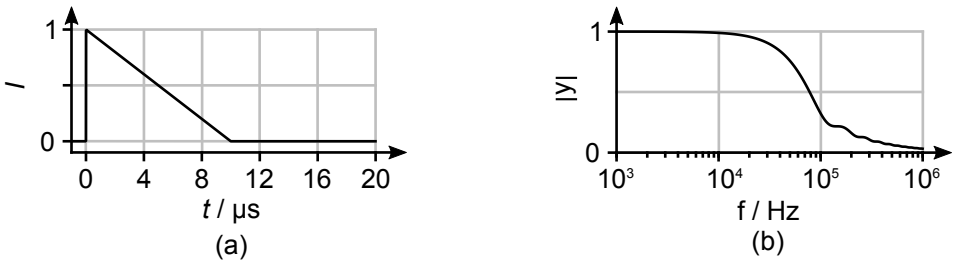

Fig. 5.31: Normalized current triangle (a) in time domain and (b) in frequency domain.

Ongoing Operation

Figure 5.32 shows a measurement of the inductance identification by manipulation of the controller output for $V_{\text{in}} = 3.5\,\text{V}$, $L_{\text{nom}} = 22\,\mu\text{H}$, $C_{\text{nom}} = 22\,\mu\text{F}$, $I_{\text{load}} = 225\,\text{mA}$ and $R_{\text{DS,on}} = 1.1\,\Omega$.

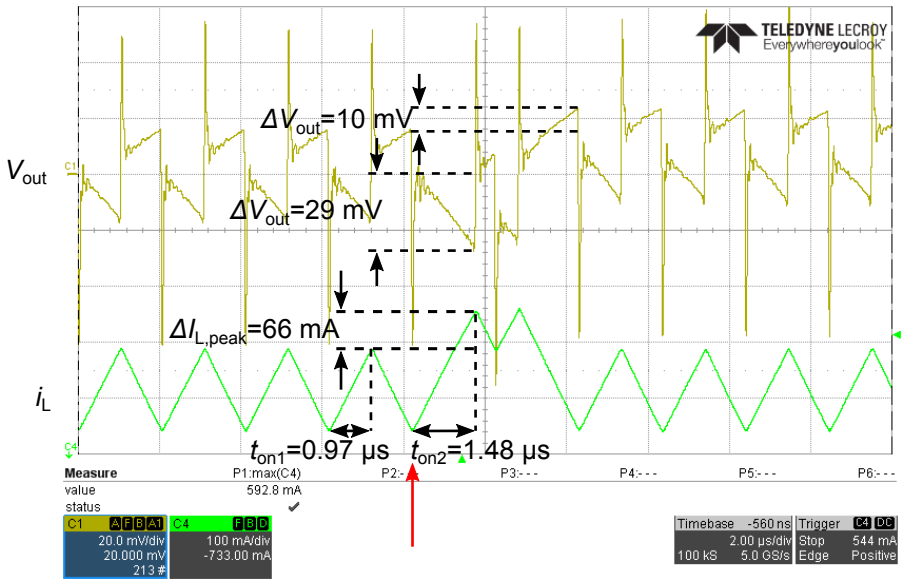

Fig. 5.32: Inductance and capacitance identification during operation.

The red arrow marks the point of time when the controller output is manipulated. A current increase of 125 mA is requested and an increase of around 66 mA is obtained. The difference can be explained by the

influence of the ramp compensation and is considered in the calculation. The duty cycle is measured in the last period before and in the first cycle after the intervention. Combining $\Delta I_{\mathrm{L,peak}}$, V_{in} and the two measured times t_{on1}, t_{on2}, the inductance can be calculated based on (5.14), see Section 5.3.3:

$$\begin{aligned} L &= \frac{V_{\mathrm{in}} - R_{\mathrm{DS,on}} \cdot \dfrac{I_{\mathrm{L,peak1}} + I_{\mathrm{L,peak2}}}{2}}{I_{\mathrm{L,peak2}} - I_{\mathrm{L,peak1}}} \cdot (t_{\mathrm{on2}} - t_{\mathrm{on1}}) \\ &= \frac{3.5\,\mathrm{V} - 1.1\,\Omega \cdot \dfrac{593\,\mathrm{mA} + 527\,\mathrm{mA}}{2}}{66\,\mathrm{mA}} \cdot (1.48\,\mu\mathrm{s} - 0.97\,\mu\mathrm{s}) = 22.3\,\mu\mathrm{H} \end{aligned} \tag{5.18}$$

The identified inductance $L = 22.3\,\mu\mathrm{H}$ is only 3 % higher as the reference value of $L = 21.7\,\mu\mathrm{H}$.

The capacitor can be calculated based on (5.15):

$$C = \frac{I_{\mathrm{load}}}{dV_{\mathrm{out}}/dt} = \frac{225\,\mathrm{mA}}{29\,\mathrm{mV}/1.48\,\mu\mathrm{s}} = 11.5\,\mu\mathrm{F} \tag{5.19}$$

The capacitance is identified to $C = 11.5\,\mu\mathrm{F}$ based on (5.15), see Section 5.3.3, which is 11 % lower than the reference value of $C = 12.9\,\mu\mathrm{F}$.

As the concept takes only one period, the output voltage perturbation level is approximately 10 mV, which is as low as 0.2 % of the nominal output voltage.

Figure 5.33 shows the identification results for various inductors. The capacitance is constantly set to 22 µF for this identification. The results indicate that all inductances are identified with less than ±5 % identification error. Large inductances are identified more accurately, which is in line with the analysis in Section 5.3.3. A minor inaccuracy of approximately 2 % results from the excitation with a frequency not equal to the crossover frequency, which is used in the reference measurement, see Section 5.4.1.

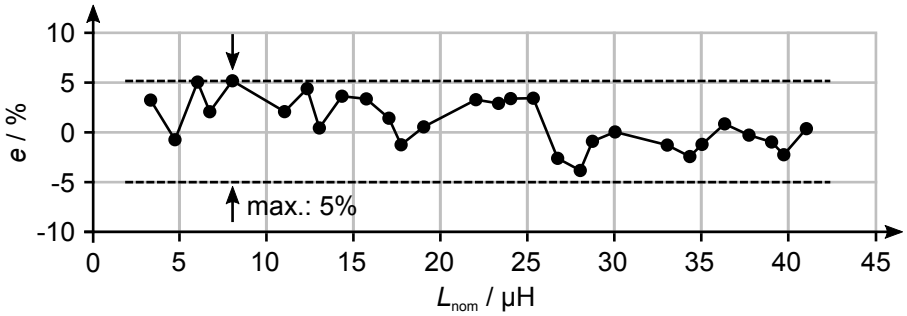

Fig. 5.33: Identification results of the inductances during operation.

Figure 5.34 shows the identification results for different capacitors. The inductance is constantly set to 22 µH. All capacitances are identified within $-10\,\%$ to $-13\,\%$ inaccuracy. The offset is explained by the fact that the capacitances are not identified at the crossover frequency of around 10 kHz, but close to the switching frequency of 500 kHz, see Section 5.4.1. Figure 5.24(b) shows that the capacitance decreases from 12.9 µF at 10 kHz to 11.2 µF at 500 kHz ($-15\,\%$). Consequently, considering the frequency and voltage characteristics of the inductor and capacitor according to the product data sheet, will improve the identification accuracy.

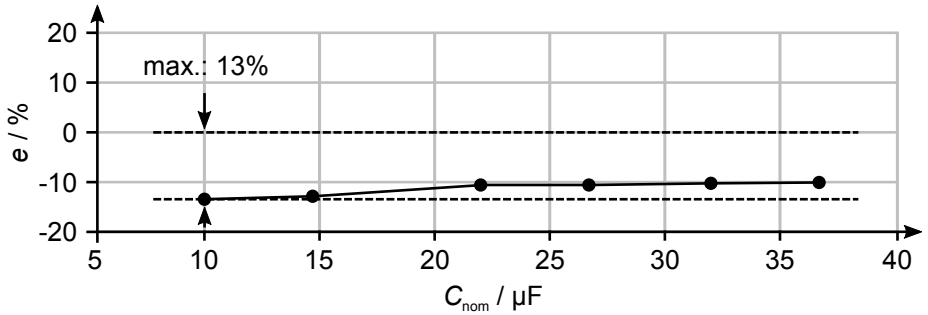

Fig. 5.34: Identification results for the capacitances during operation.

5.5 Comparison to Prior Art

Load Identification

Various load identification concepts exist [95–103]. In [95] a current sense amplifier (CSA) for the inductor current is used, where the resulting analog signals are converted into digital signals with the help of two ADCs. [101] use ohmic parasitics, i.e. the printed circuit board (PCB) trace resistance, for the load identification. Analog or digital RC-filters, modeling the inductor characteristics, are used in [100, 103].

Most concepts need additional analog circuitry for identification, losses occur and, partially, calibration routines are mandatory. In contrast, this work proposes a load current identification, which runs without interruption of the ongoing operation. Hence, the output voltage is not disturbed. Table 5.2 shows a comparison of the proposed concept to prior art. The operating parameters of the converters, the identification is applied to, are listed. [101, 103] provide identification over a wide load current range. However, the identification accuracy is limited. The concept of this work greatly benefits from the fact, that there is no need for additional analog circuitry, which is the case in prior art. The identification occurs losslessly, as no resistive elements are placed in the load path. Measurements show that the load current is identified with only 3 % inaccuracy, which is better than the accuracies achieved by the other concepts.

Tab. 5.2: Comparison of the proposed load identification with prior art.

	[95]	[100]	[101]	[103]	**This Work**
Input voltage	5 V	10 V	12 V	12 V	**3.5 V**
Output voltage	3.3 V	3.3 V	1.2 V	1.5 V	**6.3 V**
Load current range	0.1-0.75 A	not reported	0-50 A	0-10 A	**0-1 A**
Identified parameter	I_{load}	I_{L}	I_{load}	I_{load}	$\boldsymbol{I_{\mathrm{load}}}$
Additional circuitry	Yes	Yes	Yes	Yes	**No**
Maximum inaccuracy	3 %	5 %	8 %	6 %	**3 %**

Combined Inductor and Capacitor Identification

The identification method of this work differs from the methods commonly used in prior art. It analyzes the most important parameters of the system, i. e. the inductance L and the capacitance C, instead of identifying the overall system transfer behavior by means of frequency analysis [15, 109], oscillation analysis [13] or crossover frequency and phase margin control [14] (see also Section 5.2). Therefore, the implementation

effort is greatly reduced, i.e. 8800 NAND gates for an implementation of an autotuning with eight predefined controller configurations. This improvement allows for cost reduction. Unlike [13, 14, 109, 110], this work combines an identification during startup of the converter and during ongoing operation. This enables permanent tracking of SMPS parameter variations. In particular, oscillation analysis [13] is only executed during startup of the converter, Table 5.3.

Tab. 5.3: Comparison of the proposed inductor and capacitor identification to prior art.

	[13]	[14]	[15]	[109]	**This Work**
Identification method	Oscillation analysis	Control of f_c & φ_m	Frequency analysis	Frequency analysis	**Parameter analysis**
Application	Startup	Operation	Operation	Startup & Operation	**Startup & Operation**
Identification time	1 ms	20 ms*	15 ms	120 ms*	**85 µs / 2 µs**
Gate count (# NAND)	18,000	12,300	12,800***	28,100**	**8,800**
Output voltage perturbation	not applicable	±0.4 %	±0.3 %	±3 %	**±0.4 %**
Identification inaccuracy	$\frac{\Delta f_c}{f_c} = 3.7\,\%$ $\frac{\Delta \varphi_m}{\varphi_m} = 22\,\%$	$\frac{\Delta f_c}{f_c} = 0.6\,\%$ $\frac{\Delta \varphi_m}{\varphi_m} = 2.5\,\%$	$\frac{\Delta f_c}{f_c} = 12.5\,\%$ $\frac{\Delta \varphi_m}{\varphi_m} = 14.5\,\%$	not reported	$\mathbf{\frac{\Delta L}{L} = 5\,\%}$ $\mathbf{\frac{\Delta C}{C} = 13\,\%}$

*Continuous identification, estimated from figure. **Additional: 10 k memory.

***Additional: 2x32-bit multipliers.

This work significantly reduces the identification time to 85 µs during startup and 2 µs during ongoing operation, which is an improvement by a factor of 12 (startup) and 7000 (operation), respectively. Typical identification times in the other concepts are in the range of 1 ms up to 120 ms. Thus, the presented concept widely enlarges the application range of parameter identification. In particular, it enables use in applications with limited identification time.

As an additional advantage, this work does not need an open loop configuration or duty cycle freeze. Consequently, converters with multiple load transients at frequent intervals are covered. The identification allows for autotuning in current mode controlled converters, which was not published before. Further, the crossover frequency does not need to be specified a priori in boost converters. Thus, control bandwidths are enlarged.

6 Advanced Digital Controls

The main target of an SMPS is to provide a constant and stable output voltage at all operating conditions. This is challenging, as many parameters vary in operation, e.g. the input voltage and the load situation. Constant output voltages can be achieved with very large output capacitor values, as large capacitances compensate load variations with their large energy reservoir. However, large output capacitors are expensive, which is verified by the study of capacitor prices shown in Fig. 6.1. Further, the study indicates that the device size of capacitors with high values is larger than the size of capacitors with lower values. Thus, the footprint is larger and the mechanical robustness is reduced, e.g. vibration sensitivity increases. Besides, ceramic capacitors are limited to values in the low µF-range, see Fig. 6.1. For higher capacitance values, electrolytic capacitors must be used. These capacitors show significantly larger aging effects. Consequently, their use is aimed to be avoided.

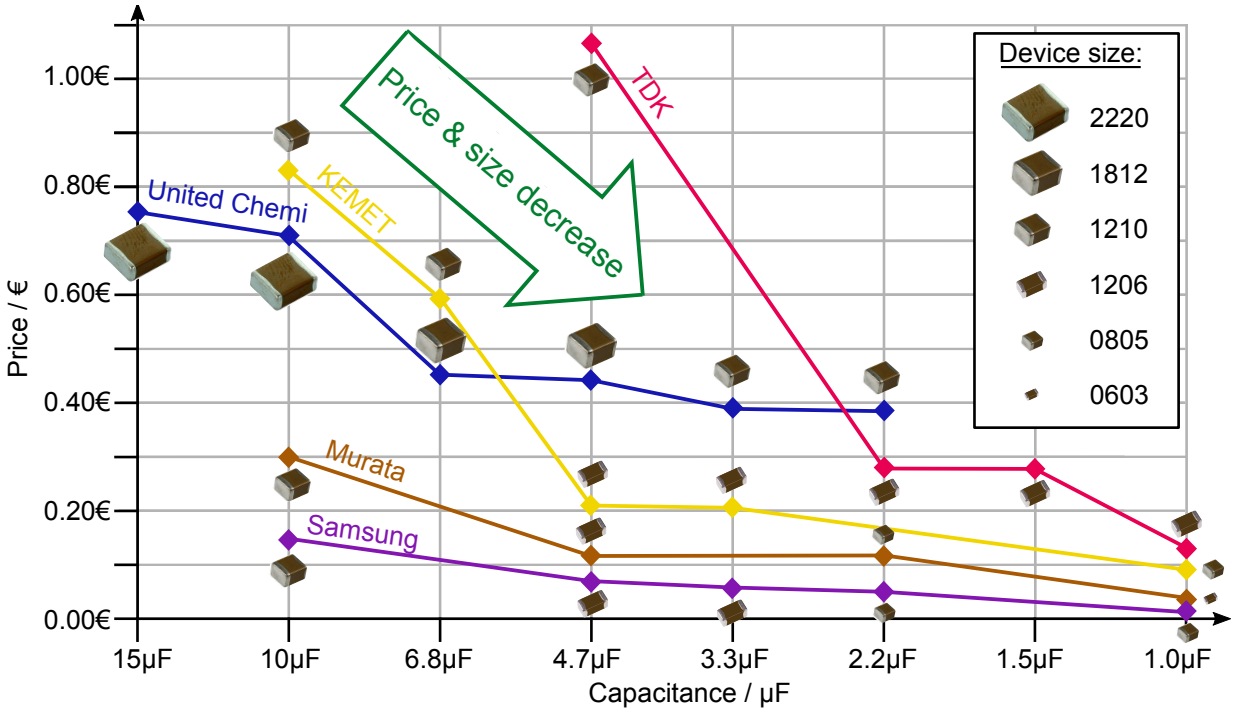

Fig. 6.1: Prices and device sizes of capacitors with varying capacitance sorted by vendors, available at [132].

Consequently, in order to reduce cost the output capacitor is aimed to be small, which, in turn, endangers the target of a constant output voltage.

Further, this target can be achieved by usage of high bandwidth controls. This is possible within certain limits in standard controls: the upper limit for the bandwidth is given by 1/5th of the converter switching frequency in direct energy transfer converters, e.g. buck converters, and the upper limit is given by 1/3 of the RHPZ in indirect energy transfer converters, e.g. boost converters, see Section 3.1.

The power consumption, the size, and the weight of electronic devices are aimed to become continuously smaller, e.g. due to the increasing demand for lower CO_2 emissions in cars [133]. As one major trend in electronics, supply voltages decrease to lower values in order to support these goals. The power dissipation of digital designs shrinks due to the lower voltages. This trend also applies to ICs and is shown in Fig. 6.2. With smaller process technology nodes the supply voltages decrease. Consequently, the SMPS have to provide smaller supply voltages. With smaller voltages also the allowed voltage deviations from the nominal value become smaller [134]. Unfortunately, the output voltage deviations due to load transients stay constant regardless of the nominal voltage. Consequently, for fulfilling the requirement of smaller output voltage deviations solely the output capacitor can be chosen larger. Further, the load current gets constantly larger due to more functionalities of the electronic devices and ICs, see also Section 2. This enlarged current range leads to stronger load transients, which counteracts the target of small output voltage deviations [135].

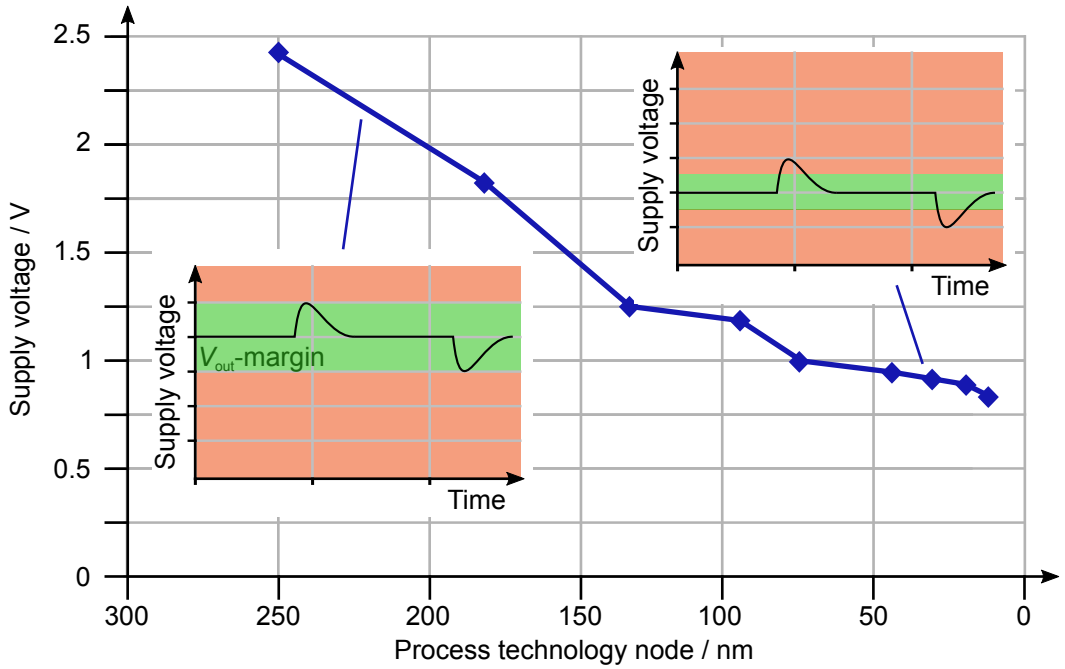

Fig. 6.2: Recent trend of supply voltages in ICs with shrinking process technology nodes, data based on [136, 137].

The challenges resulting from the described trends can be addressed by fast transient controls, which deviate from standard linear controls. These advanced, sophisticated controls can be realized efficiently by digital control. This work focuses on fast transient controls for boost converters, as their upper bandwidth limit is lower than in buck converters. Still, they require tight voltage regulation and fast recovery from disturbances. This superior dynamic behavior is necessary in order to avoid abnormal operation of portable devices [138], to support status changes between idle and active modes in portable devices [139], to properly control the brightness of LEDs [84, 140], and to retain a stable power supply in automotive environments [129].

In conclusion, small voltage deviations and short recovery times in case of disturbances can be provided by large capacitors or large control bandwidths. The output capacitor is aimed to be small for cost, reliability and device size reasons. Standard linear controls are limited in bandwidth. At the same time, shrinking supply voltages increase the requirement for small voltage deviations significantly. Consequently, fast transient controls, deviating from standard linear controls, are required in order to enable small capacitors, short recovery times, and small voltage deviations. Therefore, fast transient controls of prior art are reviewed and discussed in Section 6.1. New control methods with low computational effort are proposed Section 6.2 and Section 6.3.

6.1 Fast Transient Controls

There are multiple control concepts aiming to improve the transient behavior of SMPS compared to standard linear controls in prior art. There have been several attempts to improve the transient behavior in analog controlled SMPS by hysteretic controls. Hysteretic control works properly for buck converters. However, for boost converters only few hysteretic control concepts have been proposed [81–83]. Furthermore, adaptive control with variable analog compensation devices and new boost converter topologies have been proposed [84–87]. These concepts, as well as the hysteretic concepts, improve the transient behavior at the cost of greatly augmented circuit effort. Others propose techniques to improve the transient response by adjusting compensation poles and zeros of the boost converter with analog control. In these concepts a load transient is detected with a threshold detector monitoring the output voltage. The compensation poles and zeros are modified with a variable compensation resistance and a variable compensation capacitance, accordingly [84, 85].

There are multiple proposals for improved transient behavior with advanced digital control. This work reviews and explains earlier presented control methods comprehensively and introduces new control methods. Finally, the improvement potential, the implementation effort, the stability, and the applicability of the presented methods are evaluated.

Nonlinear PID Control

A well-known method to improve the transient behavior of SMPS is nonlinear control [141–146]. Nonlinear control improves the transient behavior by weighting the parts of the controller dependent on the control deviation. This is typically done in a way, that for large control deviations the controller is able to counteract fast, e.g. the crossover frequency is high. On the contrary, with low control deviations the controller is able to accurately adjust the output voltage, i.e. the crossover frequency is low and an appropriate phase margin ensures good steady-state stability, Fig. 6.3.

The reported nonlinear controllers are based on a PID (proportional-integral-derivative) control law. In [141], the proportional, integral and derivative gains are modified in a very sophisticated manner. The different controller gains are implemented such that there are no steps in their functions, which is important for avoiding configuration transition problems. But the computational effort is high.

A simpler solution with three different controller configurations can decide according to the control deviation, which controller configuration has to be used. Such an adaption scheme is shown in Fig. 6.3. As the integrator slows down the controller, the controller configurations are chosen such that the integrator is less dominant at larger control deviations. Hence, the controller gets faster, while the crossover frequency increases with the control deviation. This is the reason, why the transient response is superior to a conventional controller. The drawback is that the phase margin is close to instability, e.g. as low as 10°.

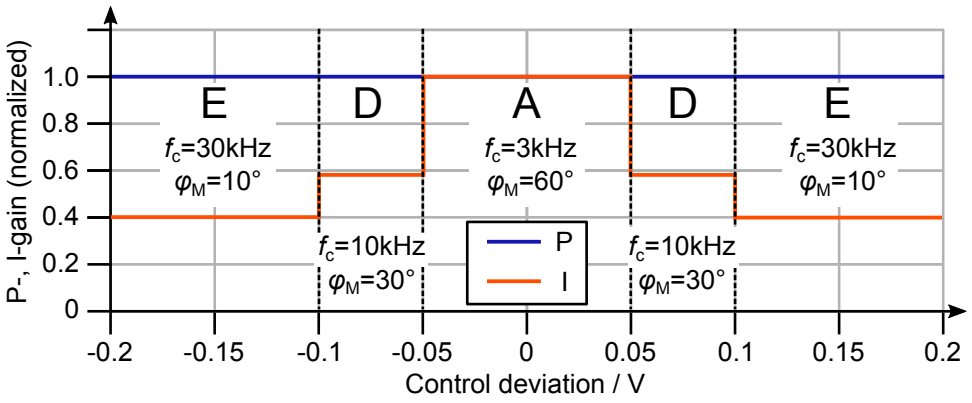

Fig. 6.3: P- and I-gain of a nonlinear controller.

In order to enable a comparison of the concepts proposed in this work to the nonlinear control, it is applied to the boost converter used for experimental verification, see Section 6.3.4. The used nonlinear controller adaption is aimed both to improve the transient behavior and to achieve low implementation effort. It has a similar controller structure as shown in Fig. 6.9, see Section 6.2.2. Unlike Fig. 6.9, the configuration selector decides based on the control deviation, which controller configuration has to be used. The nonlinear controller is composed of three configurations (A, D, and E), which differ in their integral part, see

Fig. 6.3. Controller configurations D and E are designed to offer a good trade-off between speed and stability (D: $f_c = 10\,\text{kHz}, \varphi_M = 30°$ and E: $f_c = 30\,\text{kHz}, \varphi_M = 10°$). The crossover frequency increases with the control deviation. This is the reason, why the transient response in case of a load transient is superior to a conventional controller, see experimental results in Appendix C. As a drawback, the phase margin is close to instability.

Time-Optimal and Minimum Deviation Control

The minimum deviation control is another well-known control method [91, 147, 148]. This control method is derived from the time-optimal control method [83, 91, 147–157]. Time-optimal control methods aim to counteract voltage deviations in optimum time, i.e. with the shortest recovery time possible. Thus, small output voltage deviations in case of load transients are achieved. This works well in particular for buck converters [83, 149–156]. In boost converters, a drawback of time-optimal control is, that, while the inductor current increases, no charge is provided to the output capacitor. Consequently, a long switch on-time (which is necessary in the time-optimal control approach), leads to a huge output voltage deviation. The compensation of a load transient in boost converters can, therefore, not achieve both minimum recovery time and minimum output voltage deviation due to the indirect energy transfer topology. Nevertheless, there are time-optimal control solutions for boost converters [91, 147, 148, 157].

In contrast, minimum deviation control focuses on small output voltage deviations, whereas a short recovery time is less important [91, 147]. [148] proposes a concept with a trade-off between minimum voltage deviation and minimum recovery time. After a load transient, which disbalances the output capacitor charge, time-optimal and minimum deviation controls try to balance the output capacitor charge in a very short time. While the output capacitor charge is not balanced, an output voltage deviation is present.

A minimum deviation controller works as shown in principle in Fig. 6.4 in case of a low-to-high load transient. After the load transient, the switch (Fig. 3.1) is immediately turned on, which increases the inductor current, while no charge is brought to the output capacitor. Hence, the output voltage decreases with a down slope proportional to the new load current. When the output voltage reaches a pre-calculated maximum deviation voltage ΔV_{max}, the switch is turned off again in order to stop the output voltage deviation from further growing. Now, the inductor current starts decreasing, until it reaches an inductor current limit I_{th}, which is set by the controller. This limit is slightly above the steady-state inductor valley current $I_{L,SS}$, since the present output voltage deviation needs to be counteracted. The steady-state inductor current is estimated in the first instant after the load transient, see Fig. 6.4. The sequence is repeated until the output capacitor charge is balanced.

Minimum deviation controllers have two different operation modes, a conventional controller for steady-

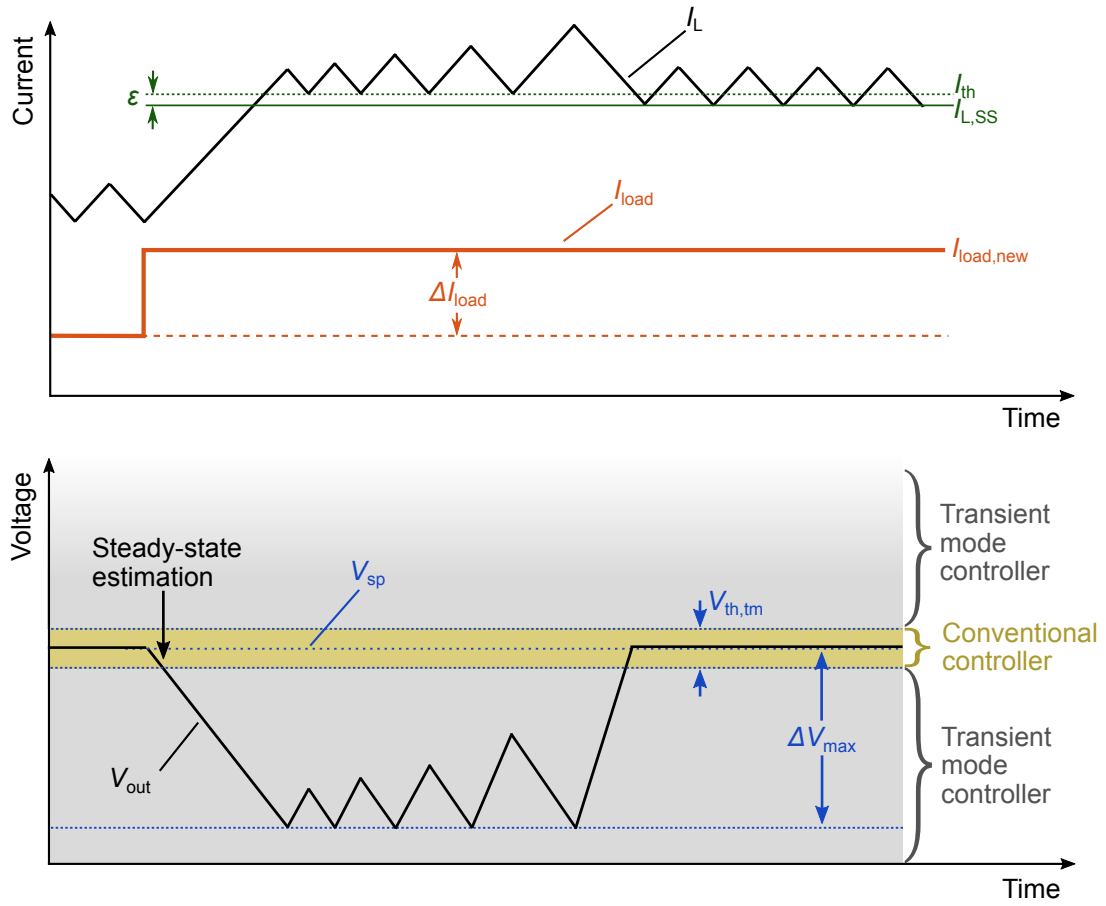

Fig. 6.4: Output voltage V_{out}, inductor current I_L, load current I_{load}, and operation ranges of the conventional controller and the transient mode controller in minimum deviation control.

state operation and further, a transient mode controller for transient operation. The transient mode controller is activated once the output voltage crosses a voltage threshold $V_{th,tm}$. As soon as the output voltage rises above the voltage threshold $V_{th,tm}$ again, the conventional controller re-starts working with an initial value. This initial value is set to the steady-state value according to the estimated inductor current value $I_{L,SS}$. This may lead to transition effects, as the initial value is dependent on several quantities, (1) the new load current $I_{load,new}$, which is estimated from the output voltage down slope dV_{out}/dt and (2) the capacitor C, (3) the inductor L, (4) the input voltage V_{in}, and (5) the duty cycle D. As this information is used within the regulation process of the transient mode controller as well, the effectiveness of the regulation relies on the exact knowledge of these quantities. Therefore, the parameter identification proposed in Section 5.3 is useful and can be combined very well.

The transient mode controller must be able to optionally switch between peak current and valley current mode control (depending on the load transient). Otherwise, the transient mode controller does not support the regulation of both low to high load transients, and high to low load transients, respectively. Further, the transient mode controller operates at variable switching frequency and does not support duty cycle

limitations. With duty cycle limitations the long switch on- or off-times, demanded by the transient mode controller, are not feasible. This limits the use of the minimum deviation control method in a wide range of practical applications.

Experimental results of the minimum deviation control are required for comparison to the control concepts proposed in this work. However, due to application requirements (automotive in this case) the available boost converter IC is not allowed to have variable switching frequencies, to switch between peak and valley current mode control, and it operates with duty cycle limitations. Thus, for minimum deviation control, simulation results are presented, see Appendix C. The simulation model uses the same converter parameters for the analog-to-digital converter, and the digital-to-analog converter, but without the above mentioned limitations.

6.2 Control with Adaption to the Right-Half-Plane Zero

As the control bandwidth of boost converters is limited by the RHPZ, as described in Section 3.1, an adaption of the controller to the parameters (L, V_{in}, I_{load}), which define the RHPZ frequency, is valuable. With such an adaption the controller can operate at higher bandwidths most of the operation time.

With the identification of the inductor value, shown in Section 5.3, an adaption of the controller is possible to achieve superior dynamic behavior. Therefore, a plug and play unit can be formed, where the controller adapts to any inductor applied by the customer. Also, while in operation, the controller can be optimized with regard to the present inductance value.

Changing operation conditions, i.e. load and input voltage changes, can be compensated in order to optimize the control bandwidth. This is especially helpful in systems with many loads. By smart management of the loads in the system, the higher bandwidth can be utilized in order to achieve small voltage deviations. When turning on several loads in a short time, it is beneficial to first turn on high current loads, as they lead to high voltage deviations. The high bandwidth, that is allowed at the low loads, leads to an improved output voltage regulation.

6.2.1 Variation of the Right-Half-Plane Zero

Influence of the Inductor

Figure 6.5 shows the varying frequency of the RHPZ, the maximum crossover frequency, and the worst-case-design crossover frequency as a function of the inductor value, respectively. The maximum crossover

frequency is given with respect to the rule given in Section 3.1. It must be smaller than 1/3 of the RHPZ frequency. Conventional linear control circuits have an invariable controller configuration. The used inductor may depend on the application. It underlies parameter variations due to production tolerances, temperature effects, and aging, as discussed in Section 5.1. The controller must fit for the highest inductance, which is the worst case. Thus, the resulting crossover frequency is constantly low.

Figure 6.5 indicates that the maximum allowed crossover frequency gets higher with decreasing inductances. A controller modification, increasing the crossover frequencies and adjusting the phase margins at lower inductances, would be possible. This is advantageous because the control circuit gets faster and voltage over-/undershoots decrease. The adaptive approach proposed in Fig. 6.5 (on the right) provides significant improvement potential compared to conventional designs.

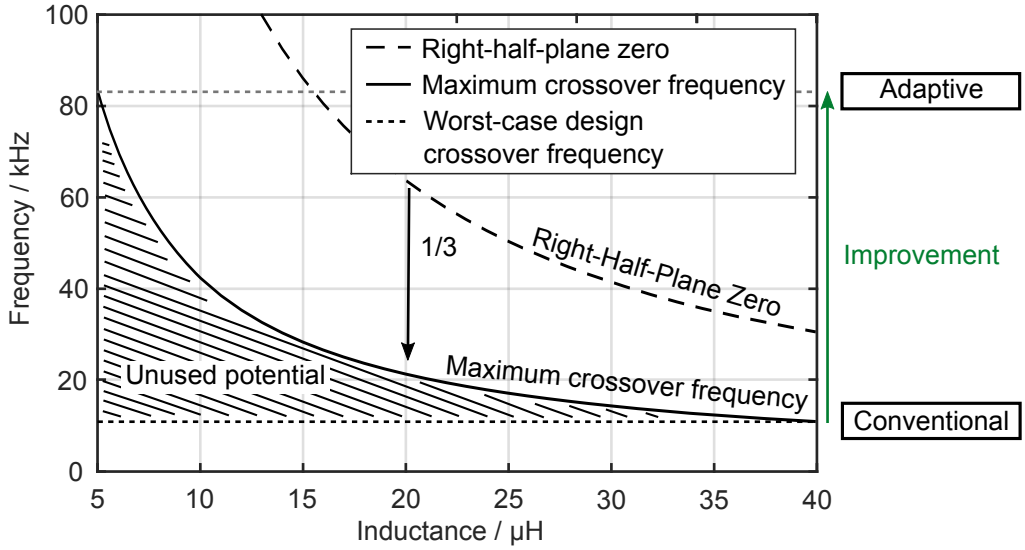

Fig. 6.5: Right-half-plane zero, maximum crossover frequency, and worst-case design crossover frequency as a function of the inductance with plant parameters $R_{\text{load}} = 20\,\Omega$, $V_{\text{in}} = 4\,\text{V}$ and $V_{\text{out}} = 6.3\,\text{V}$.

This approach offers further potential for compensating aging effects. Typically, capacitor values become lower over time, see Fig. 5.3. The smaller the capacitor value is, the higher the voltage deviations for the same load steps become. Similarly, the inductor value decreases due to aging effects, as well. This, in turn, allows for a higher crossover frequency, which can be used to compensate the higher output voltage deviations.

For this controller modification the actual inductance needs to be known, which is obtained from the parameter identification proposed in Section 5.3.3.

Influence of the Load

Figure 6.6 shows the varying frequency of the RHPZ, the maximum crossover frequency, and the worst-case-design crossover frequency as a function of the load resistance. The invariable controller of conventional linear control has to be designed for worst-case to be suitable for the lowest load resistance, which corresponds to the lowest frequency. The resulting crossover frequency is unnecessarily low.

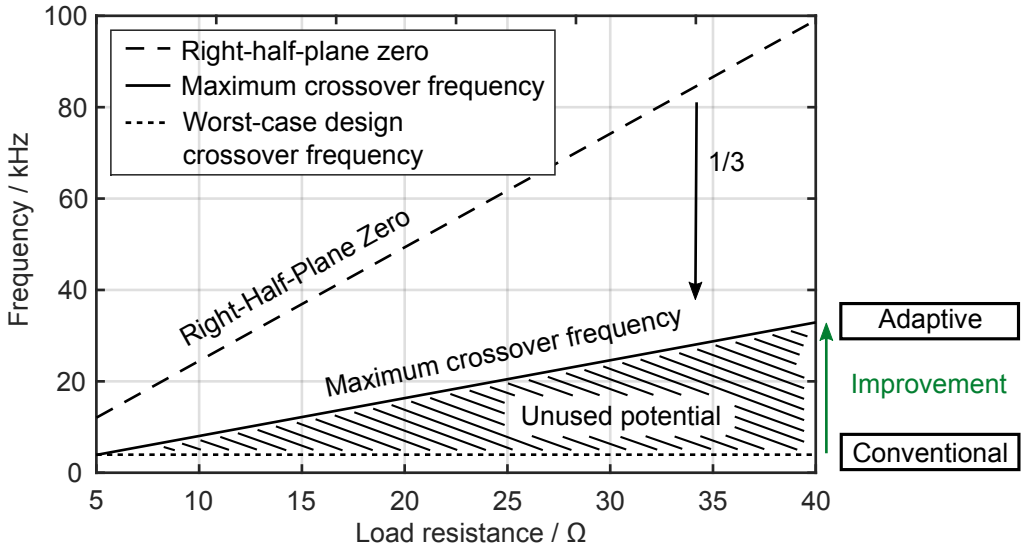

Fig. 6.6: Right-half-plane zero, maximum crossover frequency, and worst-case design crossover frequency as a function of the load resistance with plant parameters $L = 20\,\mu\text{H}$, $V_{\text{in}} = 4\,\text{V}$ and $V_{\text{out}} = 6.3\,\text{V}$.

The maximum crossover frequency gets higher with increasing load resistances, Fig. 6.6. A controller modification increasing the crossover frequencies and adjusting the phase margins at higher load resistances is possible. This is advantageous because the control circuit gets faster and voltage over-/undershoots decrease. Especially, in applications with a wide load range this adaption is very effective. The adaptive approach, proposed in Fig. 6.6, provides significant improvement potential compared to conventional designs. This approach is implemented in Section 6.2.2 and experimental results, shown in Section 6.2.3, confirm its effectiveness. For this controller modification the recent load resistance needs to be known, which can either be obtained from a measurement or be estimated. An accurate, lossless load identification without additional measurement circuitry is proposed in Section 5.3.2.

Figure 6.7 indicates an additional drawback of conventional controls. It shows the crossover frequency along with the phase margin for the boost converter with invariable controller configuration as a function of the load resistance. The modest increase of approximately 1 kHz in the crossover frequency is due to the variation of the plant, as a consequence of the load variation. The phase margin varies by approximately 30° in the shown range of load resistances. Both, the low crossover frequency and the unsuitable phase margin, lead to slow transient responses and wide voltage over-/undershoots. Consequently, beyond the increase of

crossover frequency, the adaptive approach proposed in this section is valuable, since the phase margin is set appropriately.

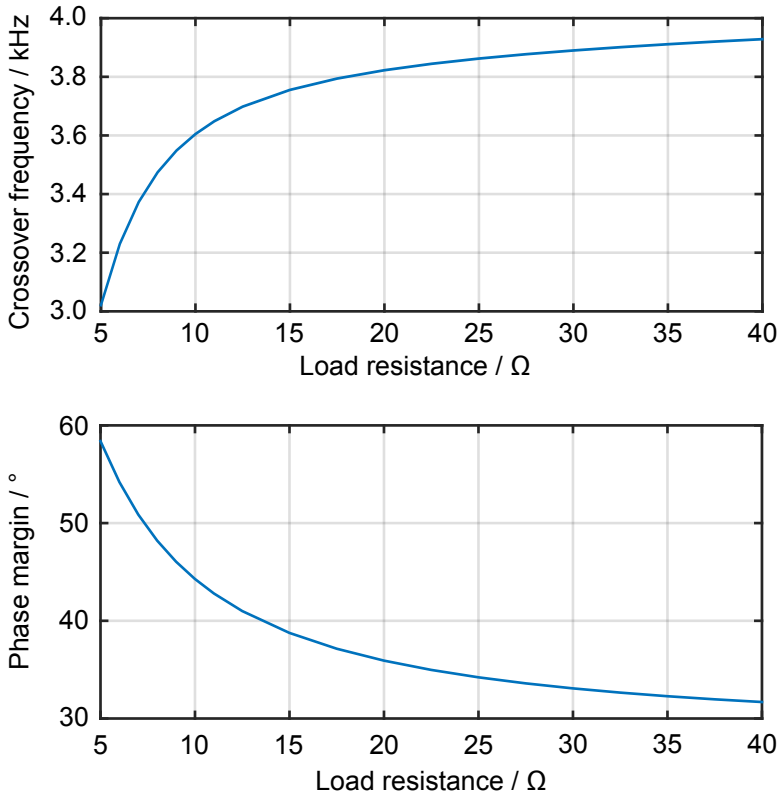

Fig. 6.7: Crossover frequency and phase margin of a conventional boost converter with invariable controller as a function of the load resistance.

Influence of the Input Voltage

Figure 6.8 shows that the higher the input voltage is, the higher the crossover frequency f_c can be chosen. Although, the variation of the plant as consequence of rising input voltages leads to an increase of the crossover frequency, inherently, an adaption to the input voltage allows for further increasing the crossover frequency. Consequently, an adaption of controller coefficients to both the load resistance and the input voltage allows for high crossover frequencies in a wide range of operating points. When combining the information of Fig. 6.6 and Fig. 6.8, the crossover frequency can be doubled (from 3 kHz to 6 kHz) compared to a conventional controller in more than 93 % of all operating points (3-6 V input voltage and 5-40 Ω load resistance).

The technique is very attractive with an integrated input voltage measurement, which is either already present [126, 127, 158, 159] or can be implemented with low effort [128].

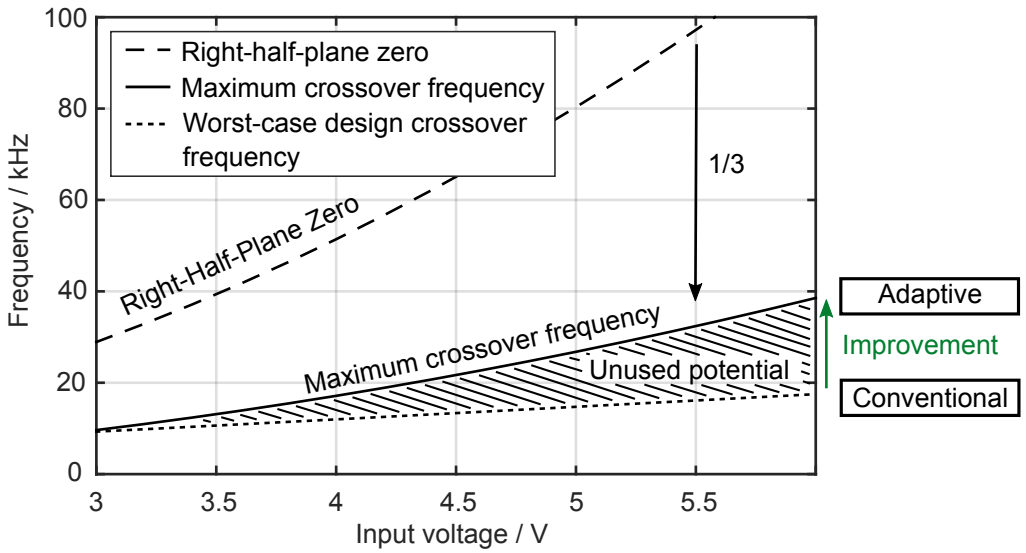

Fig. 6.8: Maximum crossover frequency as a function of the input voltage with plant parameters $L = 20\,\mu\text{H}$, $R_{\text{load}} = 20\,\Omega$ and $V_{\text{out}} = 6.3\,\text{V}$.

6.2.2 Controller Adaption

Figure 6.9 shows a PI (proportional-integral) controller, which has the possibility to switch between three different configurations (A, B, and C). A PI controller is well suitable for control of the boost converter with current mode control, whose parameters are listed in Table 3.1.

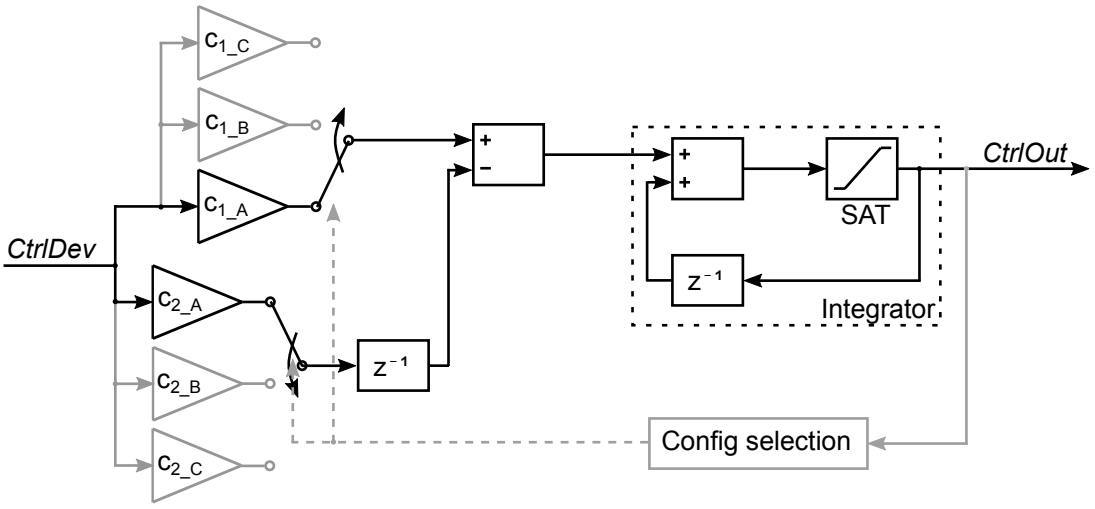

Fig. 6.9: PI controller structure with three different controller configurations (A, B, and C), which share the same integrator with anti-wind-up structure.

Equation (6.1) shows the standard PI control law for controller configuration A:

$$D(z) = \frac{c_{1\_\text{A}} - c_{2\_\text{A}} \cdot z^{-1}}{1 - z^{-1}} = \frac{1.703 - 1.619 \cdot z^{-1}}{1 - z^{-1}} \tag{6.1}$$

The gray part in Fig. 6.9 indicates the controller parts, which are placed in addition to a conventional controller. The three different controller configurations share the same integrator. This saves hardware effort and allows to change the controller configuration without pre-charging the integrator, which avoids potential disturbances caused by inaccurate pre-charging. The controller coefficients are varied such that for higher load resistances, on the one hand, the magnitude of the controller rises and, on the other hand, a suitable phase boost at the crossover frequency is reached. For reasons of simplicity and low hardware effort, a controller adaption with three different controller configurations (A, B, and C) is proposed. The coefficients of controller B and C are $c_{1\_B} = 19.223$, $c_{2\_B} = 18.626$, $c_{1\_C} = 27.756$, and $c_{2\_C} = 26.490$, respectively. The adaption technique is not necessarily limited to three configurations, more controller configurations can lead to better control results.

Load Adaption

Figure 6.10 illustrates, which controller configuration is utilized across a given load range. Controller configuration A, see Equation (6.1), is designed to fit for the maximum crossover frequency at 5 Ω load resistance (i.e. I_{load}=1.2 A), configuration B for 20 Ω (i.e. I_{load}=300 mA), and configuration C for 40 Ω (i.e. I_{load}=150 mA).

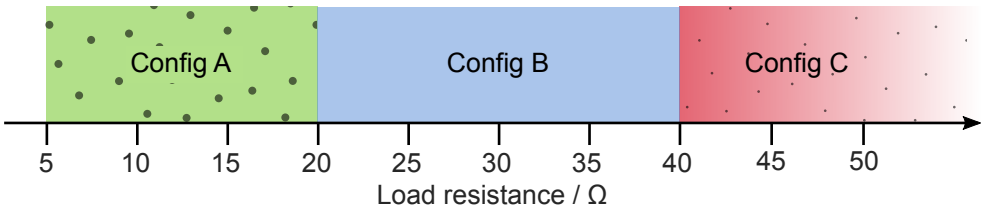

Fig. 6.10: Choice of the controller configurations for different load resistances.

Table 6.1 shows the resulting crossover frequencies and phase margins for the different controller configurations. The crossover frequencies of the adaptive controller rise for higher load resistances. They are more than five times enlarged, compared to the boost converter with conventional controller. The phase margin, in opposite to a conventional controller (Fig. 6.7), does not lag at high load resistances. It is adapted to 60°, which is typically desired in controls.

The simplicity of this modified controller allows an implementation in an IC, FPGA, digital signal processor (DSP) or µC with low effort, with small additional chip area, and low power consumption due to its simple and purely digital nature. As a result, the bandwidth is enlarged and the transient behavior of the converters is effectively improved.

Tab. 6.1: Resulting crossover frequencies f_c and phase margins φ_M at different load resistances of the proposed adaptive controller and of the conventional controller with configuration A.

Load	Conventional Controller	Adaptive Controller
5 Ω	A: $f_c = 3\,\text{kHz}$ / $\varphi_M = 60°$	A: $f_c = 3\,\text{kHz}$ / $\varphi_M = 60°$
20 Ω	A: $f_c = 4\,\text{kHz}$ / $\varphi_M = 35°$	B: $f_c = 16\,\text{kHz}$ / $\varphi_M = 55°$
40 Ω	A: $f_c = 4\,\text{kHz}$ / $\varphi_M = 30°$	C: $f_c = 23\,\text{kHz}$ / $\varphi_M = 55°$

Combined Input Voltage and Load Adaption

An adaption to the input voltage, comparable to the adaption to the load, shown in the previous subsection, improves the dynamic behavior of the boost converter over a wide range of input voltages. However, an adaption to both the load and the input voltage simultaneously is more rational, since the load current information is available in a current mode controlled boost converter, anyway. The controller used for this input voltage and load dependent adaptive control can be designed according to the controller shown in Fig. 6.9. Figure 6.11 illustrates an exemplary adaption of the controller configuration to the load resistance and the input voltage.

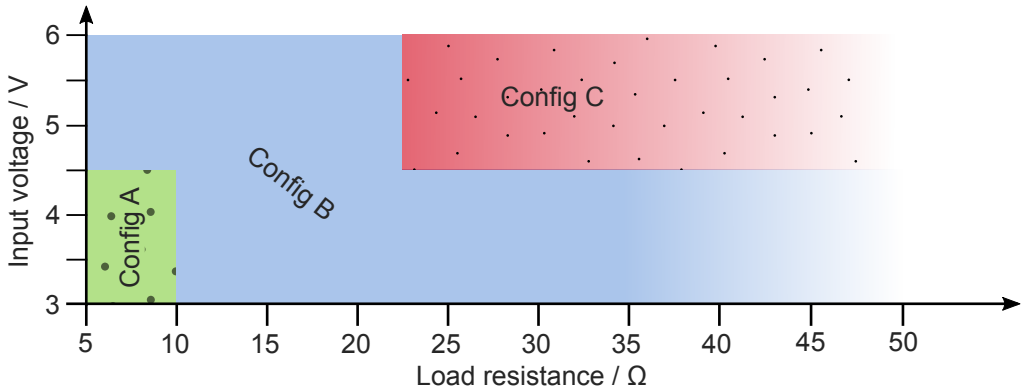

Fig. 6.11: Controller configurations for different load resistances and input voltages.

This adaption results in crossover frequencies and phase margins, which are listed in Table 6.2. The controller adaption mechanism enlarges the crossover frequency (more than six times) and further adjusts the phase margin to approximately 60° over all operating points, which is recommended in control systems. Consequently, output voltage deviations can be counteracted with up to six times smaller voltage deviations.

Tab. 6.2: Resulting crossover frequencies f_c and phase margins φ_M at different load resistances and input voltages of the proposed adaptive controller with configurations A, B and C and of the conventional controller with configuration A.

Load, V_{in}	Conventional Controller	Adaptive Controller
5 Ω, 3 V	A: $f_c = 2.5\,\text{kHz}$ / $\varphi_M = 60°$	A: $f_c = 2.5\,\text{kHz}$ / $\varphi_M = 60°$
10 Ω, 4.5 V	A: $f_c = 4\,\text{kHz}$ / $\varphi_M = 50°$	B: $f_c = 15\,\text{kHz}$ / $\varphi_M = 60°$
22.5 Ω, 4.5 V	A: $f_c = 4\,\text{kHz}$ / $\varphi_M = 45°$	C: $f_c = 25\,\text{kHz}$ / $\varphi_M = 55°$

6.2.3 Experimental Verification

The parameters of the boost converter used for the experimental verification are listed in Table 3.1, while the experimental setup is shown Fig. 5.23. Further, the ADC and DAC parameters are shown in Table 6.3. All measurement results are compared to a conventional controller (configuration A) which serves as reference. Such a controller is invariable and worst-case designed for stable operation under all conditions.

Tab. 6.3: Parameters of the ADCs and the DAC.

V_{out}-Analog-to-Digital Converter	
Architecture	Delay Line
Output voltage resolution	20 mV
Sampling rate	500 kSps
Conversion time	90 ns
Digital-to-Analog Converter	
Architecture	R-2R
Resolution	12 mV
Conversion rate	500 kHz
V_{in}-Analog-to-Digital Converter	
Architecture	ΔΣ
Input voltage resolution	24 mV
Sampling rate	800 kSps
Conversion time	1.875 µs

Load Adaption

Figures 6.12 and 6.13 show load transient responses of the conventional controller (configuration A) and the proposed load dependent adaptive controller. The output voltage deviations are reduced by a factor of two (and higher) in case of load transients at load resistances higher than 20 Ω. Also, the recovery time is reduced by a factor of 1.5 at high load resistances.

As only three controller configurations are used and the load is identified without additional circuitry, the load adaptive control benefits from the very low overall effort and simplicity.

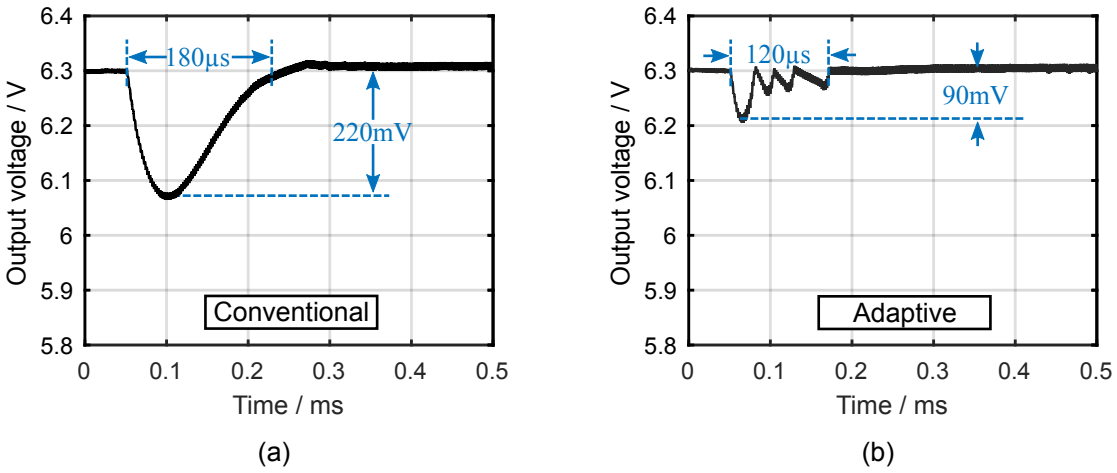

Fig. 6.12: Load dependent adaptive control: Measurement of the output voltage response to a load transient from 80 Ω to 40 Ω.

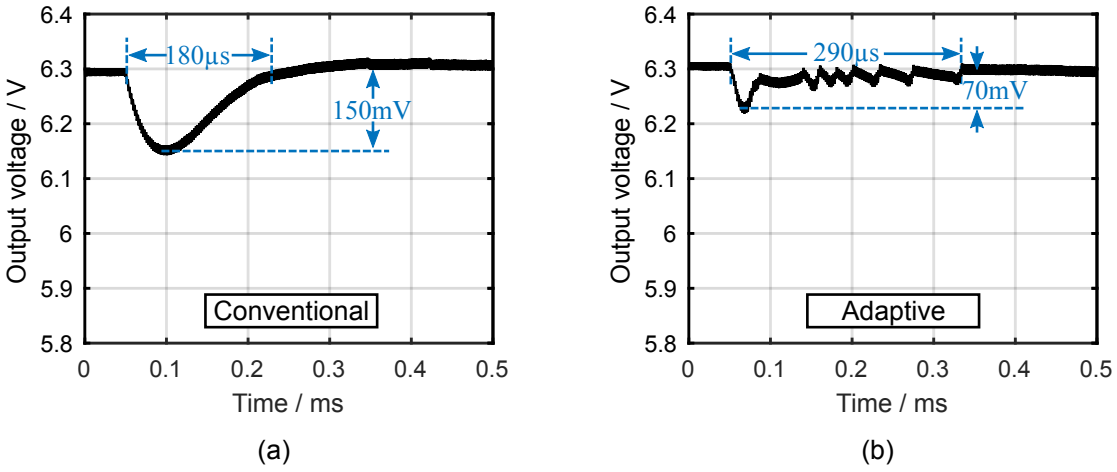

Fig. 6.13: Load dependent adaptive control: Measurement of the output voltage response to a load transient from 40 Ω to 30 Ω.

Combined Input Voltage and Load Adaption

Figures 6.14 and 6.15 show load transient responses of a conventional controller (configuration A) and the proposed load and input voltage dependent controller. The output voltage deviation at $V_{\text{in}} = 5\,\text{V}$ is reduced by a factor of about 1.9 in case of a load transient from 40 Ω to 20 Ω. The transient responses are greatly improved over a wide range of operating points.

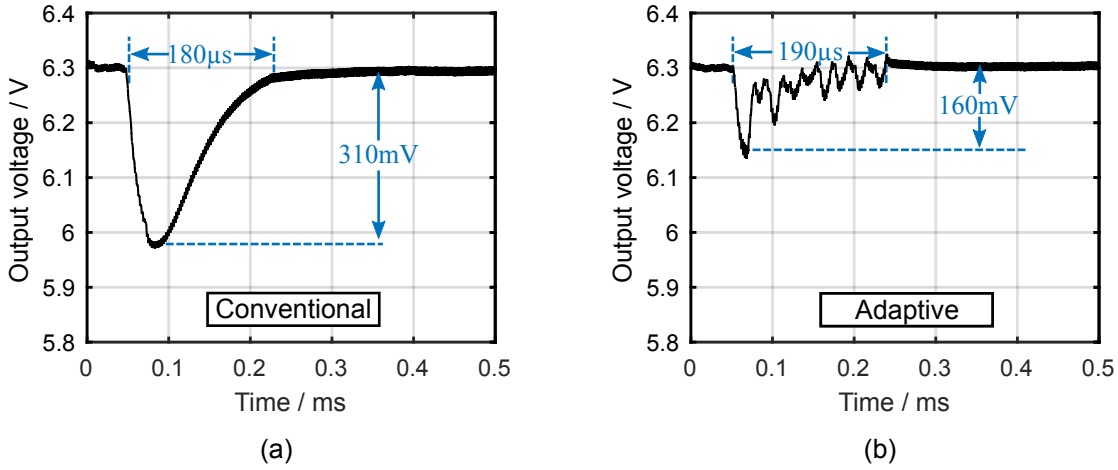

Fig. 6.14: Load and input voltage dependent adaptive control: Measurement of the output voltage response to a load transient from 40 Ω to 20 Ω at 5 V input voltage.

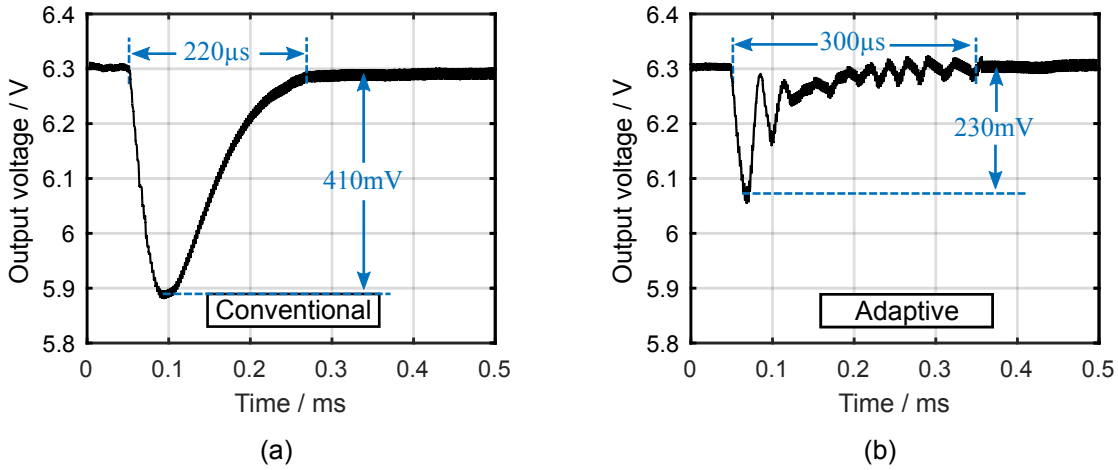

Fig. 6.15: Load and input voltage dependent adaptive control: Measurement of the output voltage response to a load transient from 22 Ω to 12 Ω at 5 V input voltage.

Both, the experimental results of the load adaptive control and the control with adaption to the load and the input voltage show that significant improvement is achieved, although moderate resolution ADC and DAC are used (the delay line ADC is operated in a low resolution mode for this section). Consequently, the shown controls do not come with special system requirements.

6.3 ΔV/Δt-Intervention Control

The adaptive control, proposed in the previous section, improves the transient behavior of boost converters in a wide range of operating points, i.e. at low loads and high input voltages. This section introduces an advanced control concept, which works independent from the converter operating points.

6.3.1 Motivation

There are plenty of control concepts, which improve the transient behavior of boost converters. Most often, their controllers require fairly demanding computational algorithms, they rely on full flexibility of the system (no inductor current limitations, no minimum switch on- and off-times,...), they cause configuration or mode transition effects, and require high resolution ADCs for good control success [91, 141–148, 157, 160].

In this section a control concept is proposed, which addresses these drawbacks by a simple controller adaption with low computational effort, and a continuously working standard controller, and a concept whose control success is only relying on few parameters. Furthermore, the method can be applied to boost converters with (1) limitation of the maximum duty cycle, e.g. for avoiding lossy operating points, for avoiding subharmonic oscillations or for bootstrapping of a high-side switch gate driver, with (2) limitation of the minimum duty cycle, e.g. for blanking of switching disturbances, with (3) limitation of the maximum inductor current, e.g. for avoiding coil saturation or overheating, with (4) limitation of the minimum inductor current, e.g. in an asynchronous topology, with (5) a ramp compensation preventing subharmonic oscillations, with (6) mandatory constant switching frequency, and with (7) subsequent load transients occurring with very short time distance. Finally, the control does not interrupt the conventional controller operation. As a consequence, steady-state stability is evaluated identically to a conventional control.

The controller output signal changes from a state S1 to another state S2 in case of a load transient in current mode controlled boost converters, Fig. 6.16. Starting from the load transient until reaching state S2 stationary, a control deviation exists. Therefore, this time equals the recovery time in case of a load transient. Despite the fact, that in boost converters both minimum recovery time and minimum output voltage deviation cannot be obtained at the same time [160], an acceleration of the transition reduces both the recovery time and the output voltage deviation in opposite to conventional control.

A superior transient performance is achieved when the controller output $CtrlOut$ immediately changes from state S1 to state S2. As the key idea of the proposed concept, the difference of the two states $\Delta CtrlOut = CtrlOut_2 - CtrlOut_1$ is added to the controller output signal, exactly in the moment a load transient is

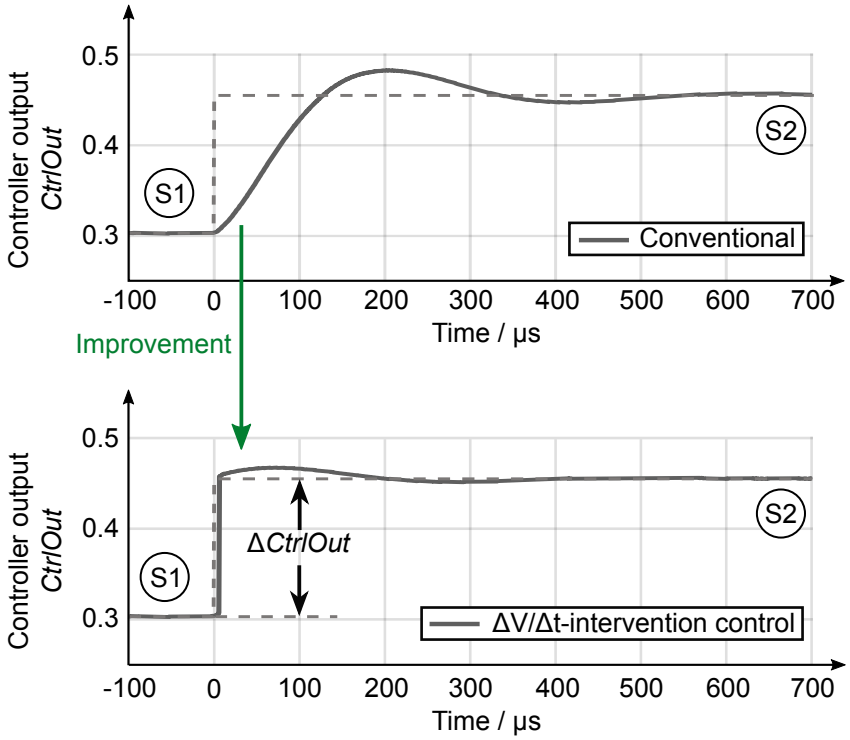

Fig. 6.16: Controller output transitions of a conventional controller and of a controller with the proposed ΔV/Δt-intervention in case of a load transient.

occurring. However, this is limited, because the moment the load transient happens and its intensity are not predictable.

6.3.2 Derivation of the Proper Controller Intervention

In equilibrium state, Fig. 6.17(a), the average of the diode current $I_{\mathrm{D,avg}}$ equals the load current I_{load} in a boost converter and the average capacitor current $I_{\mathrm{C,avg}}$ is zero. Once a load transient occurs, in the first instant the additional load current ΔI_{load} is provided solely from the output capacitor. The average diode current stays equal, as the bandwidth of the control is not high enough to instantly counteract the load transient, because the RHPZ limits the bandwidth of the control of the boost converter. Thus, the duty cycle remains equally in the beginning. This causes the output capacitor getting discharged by ΔI_{load}, Fig. 6.17(b).

By sampling the output voltage periodically once per switching cycle the output voltage derivation in case of a load transient can be calculated, Fig. 6.18. Consequently, the difference in load ΔI_{load} can be determined:

$$\Delta I_{\mathrm{load}} = \frac{C \cdot \Delta V_{\mathrm{out}}}{\Delta t} \tag{6.2}$$

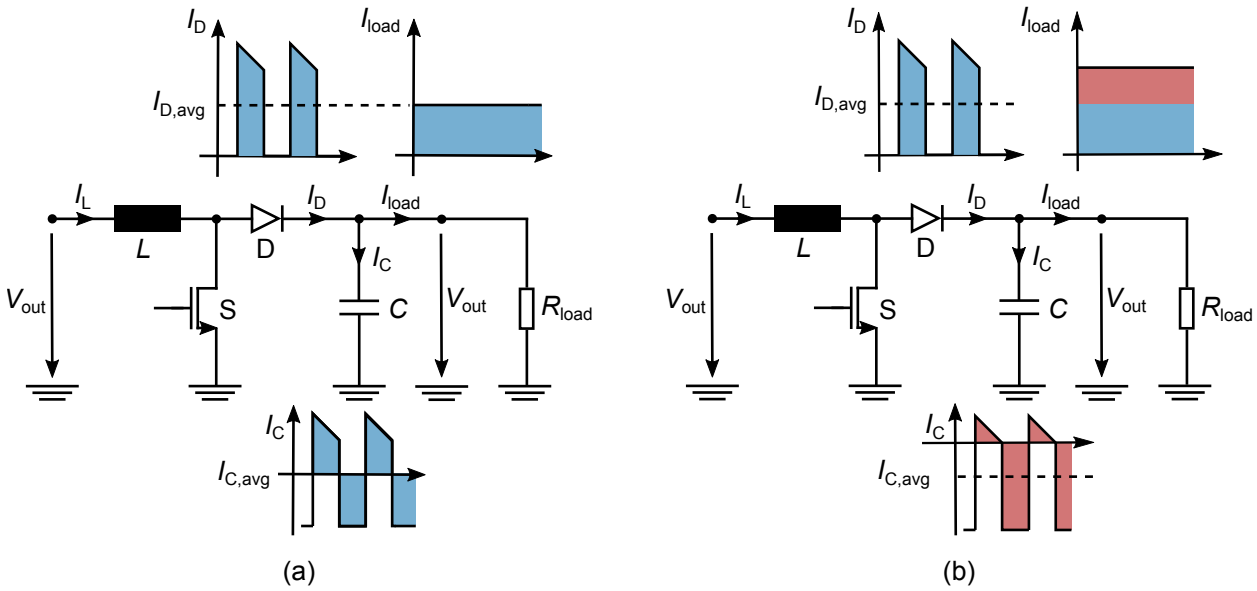

Fig. 6.17: Boost converter currents in (a) equilibrium state and (b) immediately after a load transient.

Due to the sampling theorem the switching related frequency parts of the signal are removed by sampling once per switching period. This leads to a reliable calculation of the load difference with negligible inaccuracies resulting from (dis-)charging the output capacitor with the switching frequency or resulting from the equivalent series resistance of the output capacitor, see the zoomed part of Fig. 6.18.

In Section 5 in (5.5), (5.6), and (5.7) the correlation of the load resistance, and consequently, of the load current and the controller output signal for a current mode controlled boost converter is given, resulting in:

$$R_{\text{load}} = \frac{V_{\text{out}} \cdot R_{\text{shunt}}}{1-D} \cdot \frac{1}{CtrlOut - A} \tag{6.3}$$

Parameter A is defined in (5.7). By inserting $V_{\text{out}}/R_{\text{load}} = I_{\text{load}}$ and rearranging (6.3), the controller output signal $CtrlOut$ can be calculated by:

$$CtrlOut = \frac{R_{\text{shunt}}}{1-D} \cdot I_{\text{load}} + A \tag{6.4}$$

The key idea of the concept is to add the calculated difference between state S1 and state S2 to the controller output. Using (6.4), the state difference can be determined immediately after a load transient:

$$\Delta CtrlOut = CtrlOut_2 - CtrlOut_1 = \frac{R_{\text{shunt}}}{1-D} \cdot \Delta I_{\text{load}} \tag{6.5}$$

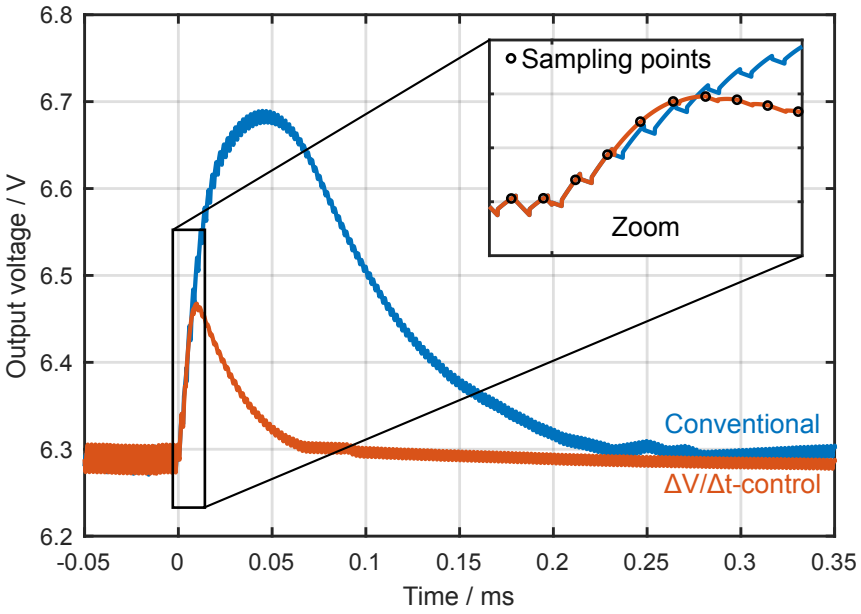

Fig. 6.18: Output voltage behavior in case of a load transient with zoom of the first instant after the load transient.

By combining (6.5) and (6.2) the final equation for calculation of $\Delta CtrlOut$ can be derived:

$$\Delta CtrlOut = \frac{R_{\text{shunt}}}{1-D} \cdot \frac{C \cdot \Delta V_{\text{out}}}{\Delta t} \tag{6.6}$$

Thus, $\Delta CtrlOut$ can be derived from known quantities and can be added to the controller output during normal controller operation, resulting in improved transient performance. Hence, the ΔV/Δt-intervention effectively counteracts load transients.

6.3.3 Controller Adaption

For the ΔV/Δt-intervention any controller can be used, for example a standard PI controller as shown in Fig. 6.19. In this work, the coefficients for this controller are chosen according to the controller configuration A given in (6.1).

The $\Delta CtrlOut$ is calculated based on the output voltage change over time, see (6.6), and fed into the integrator as an additional input signal. In a practical realization, the output voltage change over time can be determined in two different ways from the values of the output voltage ADC. It may be useful to rather determine the change of the output voltage within a pre-defined number of samples, than counting the number of samples until reaching a pre-defined output voltage deviation. A settled number of samples avoids a

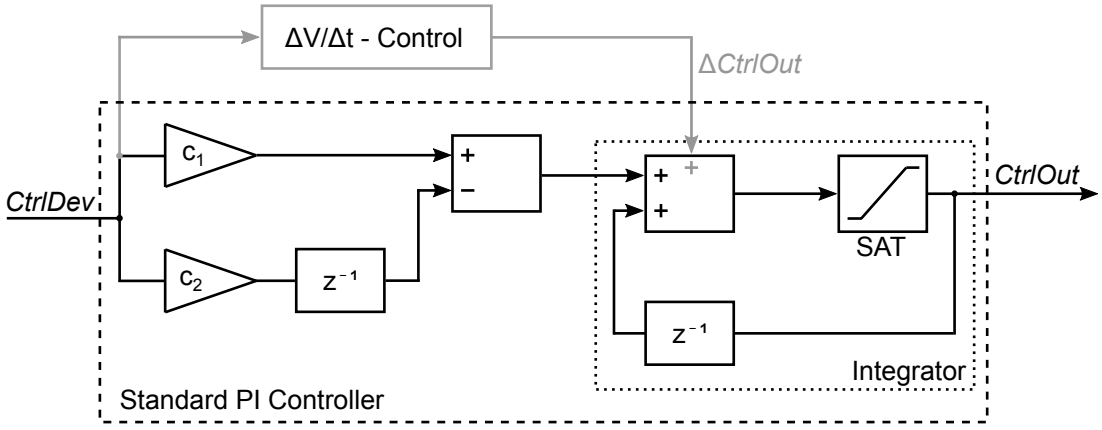

Fig. 6.19: Standard PI controller with ΔV/Δt-intervention: The integrator has an additional input for the calculated $\Delta CtrlOut$.

division by a variable time, since the time is in the denominator of (6.6). Thereby, the implementation effort is noticeably reduced in an FPGA, µC, or IC.

6.3.4 Experimental Verification

The parameters of the boost converter used for the experimental verification are equal to the parameters given in Table 3.1. The experimental setup is depicted in Fig. 5.23 and the ADC and DAC parameters are shown in Table 6.3.

Figures 6.20 and 6.21 present the transient improvements of the controller (configuration A) with ΔV/Δt-intervention compared to the same controller (configuration A) without intervention. The load transients are conducted with 20 ns step rise time. The output voltage deviations are lowered up to 2.8x. The recovery

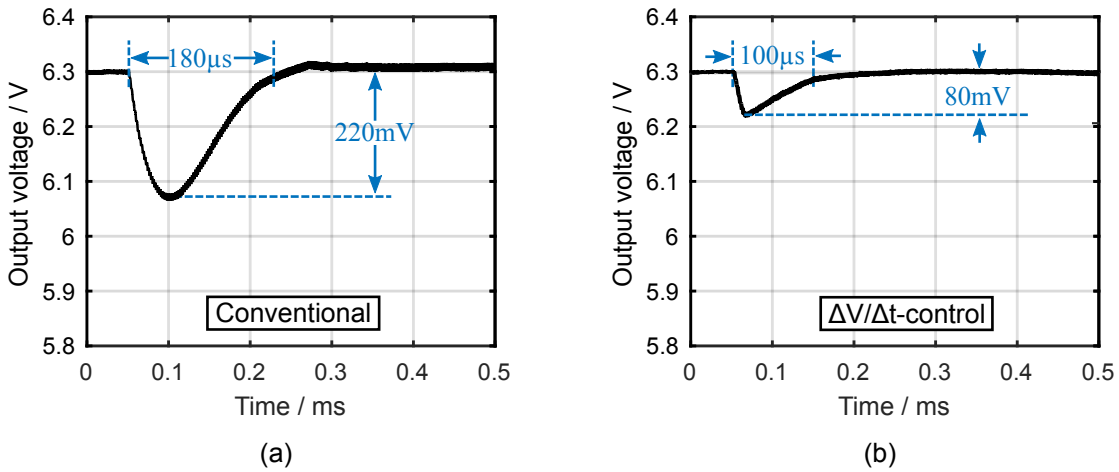

Fig. 6.20: ΔV/Δt-control: Measurement of the output voltage response to a load transient from 80 Ω to 40 Ω.

times can be shortened by a factor of 1.8. The controller with ΔV/Δt-intervention shows improvements in output voltage deviation and recovery time for any load transient. The controller with ΔV/Δt-intervention breaks the bandwidth limitation brought by the RHPZ, but has the stability characteristics of a continuously working controller with configuration A.

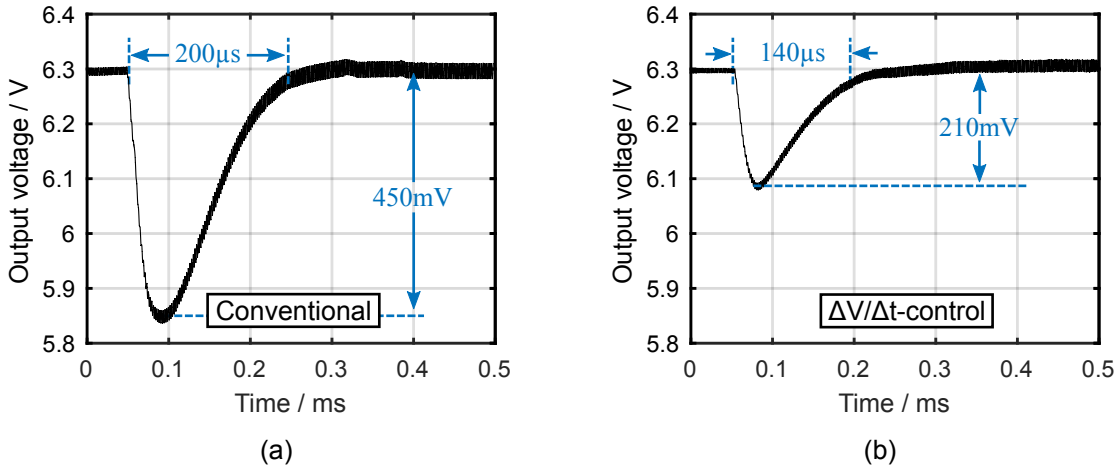

Fig. 6.21: ΔV/Δt-control: Measurement of the output voltage response to a load transient from 40 Ω to 20 Ω.

6.4 Comparison to Prior Art

In order to allow for a comparison of the proposed control concept with prior art also nonlinear control and minimum deviation control (Section 6.1) were implemented in the available test setup of this work. Measurement results for the nonlinear control, as well as simulation results for the minimum deviation control, can be found in Appendix C. For the minimum deviation control no experimental results can be presented, since the test setup does not support variable switching frequencies, optional usage of peak and valley current mode control, and operation without duty cycle limitations, which is mandatory for this control concept.

Dynamic Improvement

Table 6.4 shows a comparison of the proposed control methods regarding their transient improvements. The controller with ΔV/Δt-intervention and the minimum deviation controller show the largest improvements in voltage deviation and recovery time. The voltage deviations can be reduced by a factor of approximately 3, which allows for downscaling the output capacitor by the same factor. Also, other control methods, namely the nonlinear control and the minimum deviation control, improve the transient response in all operating points.

Tab. 6.4: Comparison of the dynamic improvements regarding the voltage deviations and recovery time with respect to a conventional controller.

Control Method	Voltage Deviation Improvement	Recovery Time Improvement
Nonlinear	220 mV/110 mV = 2.0	180 µs/110 µs = 1.6
Minimum Deviation	450 mV/140 mV = 3.2	200 µs/140 µs = 1.4
Load Adaptive	220 mV/90 mV = 2.4	180 µs/120 µs = 1.5
Load and V_{in} Adaptive	310 mV/160 mV = 1.9	180 µs/190 µs = 0.9
ΔV/Δt-Intervention	220 mV/80 mV = 2.8	180 µs/100 µs = 1.8

Application Range and Requirements

Figure 6.22 shows a comparison of the implementation efforts for the different controllers in the FPGA. In Xilinx FPGAs, the implementation effort is counted in number of look-up tables, which are used to implement boolean functions or small memories. The load adaptive controller works with very low effort (3566 look-up tables). The minimum-deviation controller uses 4776 look-up tables for its implementation.

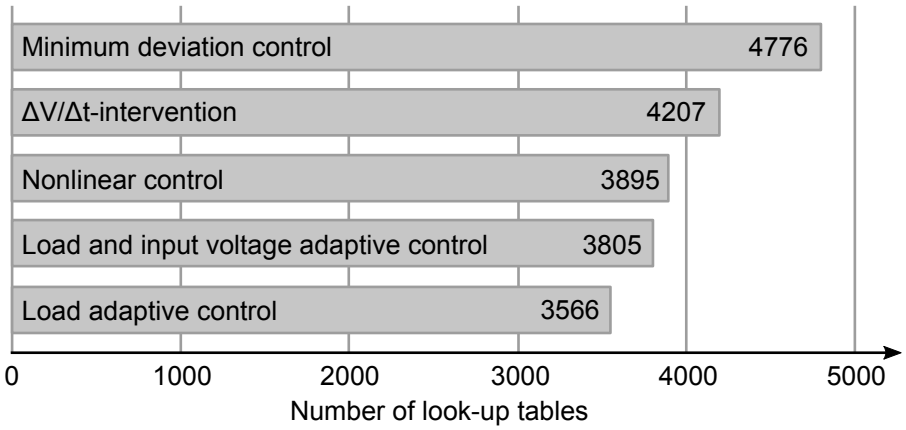

Fig. 6.22: Number of look-up tables used for the implementation of the different control methods.

Table 6.5 presents and compares further aspects of the different control methods. The column 'Relevant Parameters' refers to parameters used in the calculation formulas of the control methods, that are most likely subject to variations. Minimum deviation control has the most dependencies, the input voltage V_{in}, the output voltage resolution ΔV_{out} of the analog-to-digital converter, the inductor value L, and the capacitor value C. Accurate knowledge of these quantities is of particular interest, as the stability of the control depends on calculations based on these quantities. That is why [91] additionally proposes a self-tuning procedure and a calibration routine during start up. In contrast, the conventional controller with ΔV/Δt-intervention, which is dependent on the same parameters but the inductor value L, stability is not endangered. The conventional controller itself ensures steady-state stability. In nonlinear control, variations of plant parameters are critical, as there is a controller configuration, which is designed for high bandwidth, but close to instability. This controller can easily loose stability with varying plant parameters. Load and input voltage adaptive control are solely strongly dependent on the inductor value L, as an inaccurate inductance

Tab. 6.5: Comparison of application aspects.

Control Method	System Requirements	Relevant Parameters	Mode / Configuration Transitions	Dynamic Stability
Nonlinear	standard	V_{in}, L, C	configuration	small φ_{M}
Minimum Deviation	f_{sw} variable no duty limits peak & valley CMC	V_{in}, ΔV_{out}, L, C	mode	φ_{M} n.a.
Load Adaptive	standard	L	configuration	good φ_{M}
Load and V_{in} Adaptive	V_{in}-ADC	L	configuration	good φ_{M}
ΔV/Δt-Intervention	standard	V_{in}, ΔV_{out}, C	-	good φ_{M}

value distorts the load estimation used for control.

The column 'Transitions' refers to configuration or mode transitions, which can be visible on the output voltage during the regulation of load transients. Load (and input voltage) dependent adaptive control, nonlinear control and minimum deviation control face configuration or mode transitions. They can prolong the output voltage recovery process. Minimum deviation control suffers from several limitations, e.g. variable switching frequency, which is not feasible in many applications, and needs the highest number of look-up tables for its implementation in a FPGA.

Load adaptive (and V_{in}) dependent controls are well suitable for low effort improvement in boost converters, a combination of these controls with nonlinear control can optimize the dynamic improvement at almost no additional cost.

The $\Delta V/\Delta t$-intervention control provides a robust method for improving boost converters in various applications. The improvement potential is high without relying on too many parameters. In direct comparison to minimum deviation controls, which also lead to very good transient improvements, it does not suffer from any limitations regarding duty cycle or inductor current and it neither requires special system design actions.

7 Conclusion and Outlook

This chapter concludes the research presented in this work. In the end, an outlook is given, which describes possibilities on how digitally controlled SMPS can be improved in future work.

7.1 Conclusion

Modern life is dominated by electronic devices, which can be found everywhere, e.g. in cars, laptop and tablet computers, smartphones, TVs, and e-bikes. They are getting smart, connected, more powerful, and smaller at the same time. This development creates challenges for the power supplies used in the electronic devices. Load transients occur more often and are more heavy. Simultaneously, the voltage margins for regulation shrink. Integrated switched-mode power supplies with digital control offer high functionality and small solution size.
End-users demand for low-cost systems and many applications prefer plug and play solutions. Digitally controlled SMPS show great potential to make these features available by utilizing variable controller coefficients. In cost-driven applications, chip area is required to be as small as possible. With shrinking technology nodes, digital designs need smaller chip area and save cost. They offer good design portability and, thus, enable short development cycles and short time-to-market, which are essential for SMPS product success. Cheap inductors and capacitors within the SMPS come along with large parameter variations. Parameter identification can handle these variations in digital systems in a comfortable way. External components are expected to work reliably across a whole operating spectrum of temperature, vibration, or even contaminations. A great advantage of digital implementations over analog control is that controller full-integration without external passives is always achievable.

This work addresses the challenges of future SMPS by (1) the presentation of digital control loop designs and implementations, operating with low latency, high resolution, and guaranteed monotonicity. Further, the impact of parameter variations is reduced to a minimum by (2) the development of fast and goal-oriented parameter identification concepts. Finally, innovative voltage supply with small output voltage deviations and short recovery times is enabled by (3) robust and fast transient controls. The achievements of this work regarding these three aspects are briefly summarized in the following.

A digital control loop consists of an ADC, a digital controller, and a DPWM / DAC. For stable control, low dead times in the control loop are mandatory. Large dead times reduce the phase of the control loop, resulting in an under-damped or even unstable control. The quantization introduced through the ADC and the DAC can lead to unwanted limit cycle oscillations (LCO). Non-monotonic ADC and DAC transfer characteristics lead to oscillations, too. In conclusion, the ADC and the DAC are required to operate with high sample rates, minimum conversion delay, monotonic transfer characteristics, and high resolution.

A Delta-Sigma ADC is optimized to 9.5 effective number of bits and a conversion time of 3 µs. This leads to 10.8° negative phase shift in a control loop with 10 kHz crossover frequency. Thus, the presented Delta-Sigma ADC is suitable for state-of-the art automotive boost converters with crossover frequencies up to 10 kHz.

Delay line ADCs stand out due to their excellent resolution and low latency. The presented delay line ADC (6 bit, 9.5 MSps, 90 ns latency, 1.2 V dynamic operation range) enriches the standard window concept by a live-tracking functionality, proposed in this work. The use of a live-tracking window ADC is recommended when applying parameter identification during converter startup, as it tracks the output voltage over the entire operation range. Further, it allows for spreading the number of bits over a small voltage range, increasing the output voltage resolution without area or latency penalty. Thus, it enlarges the application range of any window ADC to high-bandwidth converters with high output voltages.

A digital pulse-width modulator or a digital-to-analog converter makes the control command available to the SMPS. DPWM is an appropriate solution for VMC converters. This work presents a 12 bit, zero latency, and monotonic design. R-2R DACs qualify for use in digital control loops with either VMC or CMC due to their small implementation effort and regular structure. A 10 bit, 1.33 MHz bandwidth DAC is designed as part of this work. The resolution of an R-2R DACs is derived, which is achievable without loss of monotonicity with regard to the matching properties of the technology.

A very high resolution DAC can be built with a charge pump architecture. The charge pump DAC of this work offers 40x higher resolution and 4000x lower voltage drift compared to prior art. It guarantees monotonicity and low conversion time, enabling high-bandwidth digital control, along with low steady-state current consumption (20 µA). The charge pump DAC qualifies for use in applications with large output voltages due to its high resolution in the order of 15 bits, which is necessary for accurate output voltage regulation and for avoiding limit cycle oscillations.

An analog controlled boost converter of an automotive airbag application has relatively small compensation devices (i.e. low resistances and capacitances). This enables a full-integration of the analog controller. In comparison, the digital control, proposed in this work, can be fully-integrated with 2.5 times smaller chip area, including the control loop components. A boost converter of an automotive power IC requires large compensation device values used for the analog controller, which do not allow a full-integration, as they would require too large chip area. In contrast, digital control solutions can be fully-integrated independent

of the digital control coefficients. Consequently, a sensitive pin is eliminated, the footprint of the SMPS is minimized, and reliability is improved.

Parameters in an SMPS underlie significant variations. Loads are turned on and off or the input voltage changes, unpredictably. It is important for product success to rely on components with ensured availability and small prices. Therefore, it is mandatory to allow for production tolerances, temperature dependencies, and degradation of the passive devices in the SMPS. Consequently, it is required to deal with unpredictable inductor and capacitor values. The variations of the load, the input voltage, inductance, and capacitance change the behavior of the SMPS, fundamentally. Identification of the actual parameters adds degree of freedom during design and enables new features like diagnostics and autotuning. Parameter identification is beneficial for plug and play solutions, which allow to choose practically any inductor or capacitor for the SMPS that meet the application, cost and quality requirements.
A proposed parameter identification concept for SMPS yields results within less than 85 µs in startup and 2 µs in operation, which is 12x (startup) / 7000x (in-operation) shorter than prior art. It concentrates on the most influential parameters of the SMPS, namely the inductance, the capacitance and the load. The inductance is identified with a maximum inaccuracy of 5 % and the capacitance with a maximum inaccuracy of 13 %, respectively. The inaccuracies result from the voltage and frequency characteristics of the passives. Considering these characteristics, the identification is much more precise. During operation, the output voltage perturbation is as low as ± 0.4 % of the nominal value. In contrast to prior art, the presented concept enables autotuning in current mode controlled converters and avoids a priori worst case crossover frequency specification. As the values of the capacitance and inductance are actually determined, they can be used for advanced control concepts (e.g. $\Delta V/\Delta t$-intervention control, minimum deviation control, etc.), whose control success strongly relies on these values.
Furthermore, this work proposes a load current identification, which runs without interruption of ongoing operation. In contrast to prior art, there is no need for additional analog circuitry and it is lossless. Measurement results show an identification with only 3 % maximum identification error.

Constant output voltages can be achieved easily with very high output capacitor values. But, they are expensive and the device size is large. In modern applications, the allowed SMPS output voltage deviations from the nominal value get smaller. At the same time, load currents get constantly larger due to an increased number of functionalities. The enlarged current range leads to higher load transients and makes it more difficult to reach the target of smaller output voltage deviations.
In boost converters and also in other indirect energy transfer converter topologies, a particular effect occurs, which sets an upper limit to conventional control bandwidths. It is modeled by a right half plane zero and impacts control stability. An adaption of the controller to the parameters defining the RHPZ frequency is proposed. The control bandwidth is doubled in more than 93 % of all operating points in the presented boost

converter when an adaption to the input voltage and the actual load is implemented. With only the adaption to the actual load, the output voltage deviations can be reduced by a factor of 2.4 and the recovery time by a factor of 1.5.
This work presents also a ΔV/Δt-intervention control concept, which is applicable to any standard controller. The control does not interrupt conventional controller operation. Consequently, steady state stability is identical to a conventional control. The voltage deviation is reduced by a factor of 2.8, which allows for downscaling the output capacitor by the same factor. The improvement potential is high without relying on too many parameters. The ΔV/Δt-intervention control does not suffer from any limitations regarding duty cycle or inductor current and does not require particular system design actions.

In conclusion, this work meets the needs of small cost, high reliability, and high flexibility in electronics that are driven by the rising number of features and functionalities and the grown complexity. They are addressed by SMPS including innovative digital control loops, fast and goal-oriented parameter identifications, and robust and fast transient controls.

7.2 Outlook and Future Work

In this work, the SMPS including the digital control loop is integrated in a 180 nm BCD technology. In this technology area advantages apply compared to analog solutions. More benefits can be expected from smaller technology nodes. The digital implementation will become even smaller and also the delay line ADC and the DPWM / DAC will benefit in terms of chip area.

The delay line ADC is not yet fully optimized with regard to resolution, area and power consumption. The live-tracking, proposed in this work, allows for reduction of the number of bits maintaining equal output voltage resolution. Simulations show that the live-tracking delay line ADC still works properly with only 2.3 bits, i.e. five digital values (-2; -1; 0; 1; 2). Furthermore, area and power consumption of the ADC can be reduced by abandoning the variability of the ADC, i.e. the choice between eight different sensitivities, which was taken into account in the design of this work.

This work achieves a low overall control loop dead time of 242 ns (latency). This value opens up the possibility to operate SMPS with crossover frequencies higher than 100 kHz. Consequently, the control loop block designs are also suited for future SMPS with higher switching frequencies enabled by fast SiC and GaN power switches.

The parameter identification presented in this work allows for identification of multiple parameters, i.e. the inductance, the capacitance, and the load. Consequently, a control loop adaption to these parameters would

be achievable. Further work needs to find out, if a continuous controller adaption or an adaption with a fixed number of controller configurations is most suitable.

More complex converter topologies, such as single ended primary inductance converter (SEPIC), Zeta converters, and multiphase converters, are composed of more passive components than standard converter topologies. In these topologies, the parameter variations of each single passive component add up. Therefore, the unpredictable variation of the transfer behavior may be large. Consequently, the application of the proposed parameter identification to these converters is of huge benefit and relaxes the design process.

The identification concept proposed in this work can be transferred to other applications, as for example to smart cables, where it is relevant to know parameters as inductance, capacitance, and resistance. Also, discrete inductors may benefit from a parameter identification.

While this work has concentrated on boost converters, an application of the proposed control concept with adaption to the RHPZ brings advantages to other converter topologies with RHPZ, such as Cuk, SEPIC, and flyback.

Adaptive voltage positioning helps to fully exploit the output voltage margin in an SMPS. Thus, the output capacitor values can be chosen lower. In adaptive voltage positioning, the set point of the control is modified according to the load situation. An implementation together with the presented load identification is simple and does not require for a load current measurement.

With this work full-integration of an entire SMPS including inductor and output capacitor is one step closer. Very large variations of the inductance are expected when integrating the inductor. They can be handled with the proposed parameter identification. Further, the output capacitor has to be very small for integration, which requires for ultra-fast controls, where the $\Delta V/\Delta t$-intervention control together with a high bandwidth standard controller (enabled by the shown control loop designs) represents a suitable control option.

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List of Abbreviations

ABS	Anti-Lock Braking System
ASIC	Application-Specific Integrated Circuit
ADC	Analog-to-Digital Converter
BIST	Built-In Self Test
CCM	Continuous Conduction Mode
CIC	Cascaded Integrator Comb
CMC	Current Mode Control
CMOS	Complementary Metal Oxide Semiconductor
CSA	Current Sense Amplifier
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DCM	Discontinuous Conduction Mode
DLL	Delay Locked Loop
DNL	Differential Nonlinearity
DPI	Direct Power Injection
DPWM	Digital Pulse-Width Modulation
DSP	Digital Signal Processor
ECU	Electronic Control Unit
EMI	Electromagnetic Interference
EMC	Electromagnetic Compatibility
FET	Field-Effect Transistor
FFT	Fast Fourier Transformation
FPGA	Field Programmable Gate Array
HMI	Human-Machine Interface
IC	Integrated Circuit
LCO	Limit Cycle Oscillations
LSB	Least Significant Bit
MLCC	Multilayer Ceramic Capacitor

MSB	Most Significant Bit
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PRBS	Pseudo-Random Binary Sequence
PWM	Pulse-Width Modulation
RAM	Random-Access Memory
RHPZ	Right Half Plane Zero
ROM	Read-Only Memory
SEPIC	Single Ended Primary Inductance Converter
SMPS	Switched-Mode Power Supply (Switched-Mode Power Supplies)
USB	Universal Serial Bus
VHDL	Very High Speed Integrated Circuit Hardware Description Language
VMC	Voltage Mode Control

List of Symbols

A		Parameter
C	F	Output filter capacitor in Switched-Mode Power Supplies (SMPS)
C_1	F	Capacitor 1 of a Type-II compensation controller
C_2	F	Capacitor 2 of a Type-II compensation controller
C_G	F	Gate capacitor
C_{nom}	F	Nominal value of a capacitor
$CtrlOut$		Controller output value
$CtrlOut_1$		Controller output value in state 1
$CtrlOut_2$		Controller output value in state 2
d		Number of distinct samples
D		Duty cycle of a pulse-width modulated signal
$\Delta CtrlOut$		Difference of two controller output values
ΔI	A	Inductor current difference between minimum and maximum current
ΔI_{load}	A	Load current difference
$\Delta I_{L,peak}$	A	Peak inductor current difference
$\Delta\varphi$	°	Phase margin shift
ΔR	Ω	Resistance difference
Δt	s	Time difference
Δt_{on}	s	On-time difference
ΔV_{max}	V	Maximum deviation voltage
ΔV_{out}	V	Output voltage difference
e		Deviation
f	Hz	Frequency
f_1	Hz	Corner frequency of a PT1 transfer system
f_c	Hz	Crossover frequency
f_{clk}	Hz	Clock frequency
$f_{c,max}$	Hz	Maximum crossover frequency
f_{in}	Hz	Input frequency

f_{max}	Hz	Maximum conversion rate
$f_{Nyquist}$	Hz	Nyquist rate
f_{out}	Hz	Output frequency
f_{p1}	Hz	Frequency of a pole 1
f_{p2}	Hz	Frequency of a pole 2
f_{p3}	Hz	Frequency of a pole 3
f_{RHPZ}	Hz	Frequency of the right half plane zero (RHPZ)
f_s	Hz	Sample rate
f_{sw}	Hz	Switching frequency
f_{z1}	Hz	Frequency of a zero 1
f_{z2}	Hz	Frequency of a zero 2
I_{bias}	A	Bias current
$I_{C,avg}$	A	Average capacitor current
i_D	A	Diode current
i_{DAC}	A	Current set by a digital-to-analog converter (DAC)
$I_{D,avg}$	A	Average diode current
i_L	A	Inductor current
$i_{L,DC}$	A	DC current in the inductor
$I_{L,avg}$	A	Average inductor current
I_{load}	A	Load current
$I_{load,new}$	A	New load current
$I_{load,ident}$	A	Identified load current
$I_{load,ref}$	A	Reference load current
$I_{L,peak}$	A	Peak inductor current value
$I_{L,peak1}$	A	First set peak inductor current value
$I_{L,peak2}$	A	Second set peak inductor current value
$I_{L,SS}$	A	Steady-state inductor valley current
i_{ref}	A	Reference current
I_{th}	A	Inductor current limit
K		Filter order
K'		Parameter
L	H	Output filter inductor in SMPS
L_{nom}	H	Nominal value of an inductor
m		Slope
n		Number of data points

N		Natural variable
OSR		Oversampling ratio
φ_D	°	Phase of a differentiator
φ_M	°	Phase margin
p_ident		Identified value of a parameter
p_ref		Reference value of a parameter
Q_C	C	Capacitor charge
R	Ω	Resistance
R_1	Ω	Resistor 1 in a type 2 compensation controller
R_4	Ω	Resistor of a feedback divider network
R_5	Ω	Resistor of a feedback divider network
$R_\mathrm{DS,on}$	Ω	On resistance of a field-effect transistor (FET)
R_C	Ω	Parasitic resistance of a capacitor
R_L	Ω	Parasitic resistance of an inductor
$R_\mathrm{L,eq}$	Ω	Equivalent resistance combining R_L, $R_\mathrm{DS,on}$, and the diode resistance
R_load	Ω	Load resistance of an SMPS
R_shunt	Ω	Shunt resistor for current measurement
s	$1/\mathrm{s}$	Laplace variable
t	s	Time
T		Transfer function of an open control loop
T_clk	s	Period of a clock
T_D	s	Dead time / delay
t_error	s	Time measurement error
T_group	s	Group delay
t_off	s	Off-time of a PWM signal
t_on	s	On-time of a PWM signal
t_on1	s	On-time of a first period
t_on2	s	On-time of a second period
t_settling	s	Settling time
T_s	s	Sampling time
T_sw	s	Switching period of SMPS
V_bias	V	Bias voltage
$V_\mathrm{bias,D}$	V	Lower bias voltage
$V_\mathrm{bias,U}$	V	Higher bias voltage
V_c	V	Capacitor voltage

V_{comp}	V	Compensation ramp voltage
$V_{\text{comp,pp}}$	V	Compensation ramp peak-to-peak voltage
V_{DAC}	V	Output voltage of a DAC
V_{err}	V	Error voltage
V_{fb}	V	Feedback voltage
V_{in}	V	Input voltage
V_{L}	V	Inductor voltage
$V_{\text{L,avg}}$	V	Average inductor voltage
V_{LSB}	V	Voltage of the least significant bit (LSB)
V_{out}	V	Output voltage
$V_{\text{out,max}}$	V	Maximum output voltage
$V_{\text{out,max1}}$	V	Maximum output voltage after first excitation
$V_{\text{out,max2}}$	V	Maximum output voltage after second excitation
$V_{\text{out,end}}$	V	Target output voltage
V_{sp}	V	Set point voltage
$V_{\text{th,tm}}$	V	Threshold voltage for transient mode controller
V_{ref}	V	Reference voltage
V_{z}	V	Voltage corresponding to a digital value Z
$V_{\text{z+1}}$	V	Voltage corresponding to a subsequent digital Z+1
ω	$1/\text{s}$	Angular frequency
ω_{o}	$1/\text{s}$	Resonance frequency
x_{i}		ADC sample points
Z		Digital (input) value

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Appendix

A Buck Converter Fundamentals

In addition to the boost converter fundamentals, this appendix shows the fundamentals for buck converters.

The purpose of a buck converter is to convert a DC input voltage V_{in} into a lower DC output voltage V_{out}. In order to realize this voltage conversion the circuit shown in A.1 is used. The main circuit components are a switch S, a diode D, an inductor L and a capacitor C. The output voltage V_{out} is used to supply a load, modeled by the resistance R_{load}.

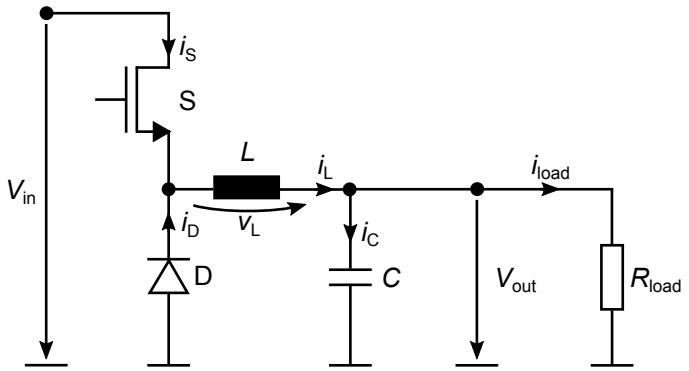

Fig. A.1: Buck converter topology.

Inductor Current and Input to Output Transfer Function

The behavior of the inductor L can be described by the following equation, where V_{L} is the voltage difference between the two inductor ports:

$$V_{\text{L}} = L \cdot \frac{di_{\text{L}}}{dt} \tag{7.1}$$

Voltage conversion is achieved by controlling the switch S and thus V_{L}. When S is turned on equation (7.1) changes to (7.2), because L is directly connected to V_{in} and V_{out}. When S is turned off the input voltage

source is disconnected from the inductor and the diode becomes conductive. Assuming an ideal diode the following equation is obtained:

$$V_{\text{in}} - V_{\text{out}} = L \cdot \frac{di_{\text{L}}}{dt} \tag{7.2}$$

$$-V_{\text{out}} = L \cdot \frac{di_{\text{L}}}{dt} \tag{7.3}$$

With turned on switch, the current i_{L} increases, because L is constant and V_{in} is greater than V_{out} by definition in the buck converter. Otherwise, when the switch is off, V_{L} is negative and i_{L} continuously decreases, assuming that the inductor current does not reach zero. This operation mode is called continuous conduction mode.

V_{in} and V_{out} are DC voltages, so the current-time differential is constant in both (7.2) and (7.3). Thus, the inductor current is triangle-shaped when the converter is in steady state. The absolute difference between the maximum and the minimum current value is called ΔI. Let the on-time of S be t_{on} and the off-time be t_{off}. Equations (7.2) and (7.3) result in equations (7.4) and (7.5), respectively.

$$V_{\text{in}} - V_{\text{out}} = L \cdot \frac{\Delta I}{t_{\text{on}}} \tag{7.4}$$

$$-V_{\text{out}} = L \cdot \frac{-\Delta I}{t_{\text{off}}} \tag{7.5}$$

Figure A.2 displays the described characteristics.

The switching period T_{sw}, the switching frequency f_{sw} and the duty cycle D are defined as:

$$T_{\text{sw}} = t_{\text{on}} + t_{\text{off}} = \frac{1}{f_{\text{sw}}} \tag{7.6}$$

$$D = \frac{t_{\text{on}}}{T_{\text{sw}}} \tag{7.7}$$

With equations (7.4)-(7.7) the steady-state input to output transfer function of the buck converter in continuous conduction mode (CCM) can be derived:

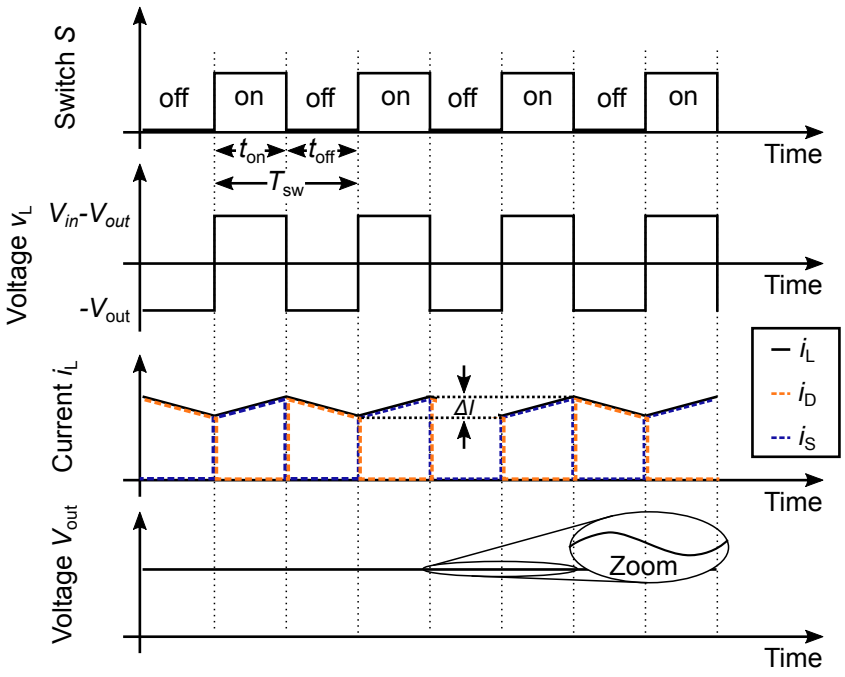

Fig. A.2: Buck converter waveforms.

$$\frac{V_{\text{out}}}{V_{\text{in}}} = D \tag{7.8}$$

Control-to-Output Transfer Function

In order to investigate the behavior of a SMPS in a control loop it is required to know the control to output transfer function of the respective converter. The control to output transfer function describes the output of a system when stimulated at its control input. In case of SMPS the control input is the switch S and the output is the output voltage V_{out}.

In addition to the parameter definitions given in Section 3.1 the following definitions are needed here: S_{e} is the artificial compensation ramp slope and S_{n} is the inductor on-slope, both in amperes per second. $V_{\text{comp,pp}}$ is the compensation ramp peak-to-peak voltage in volts. In all transfer functions the angular frequency ω is used, as is usual in the Laplace transform ($s = \text{j}\omega$). The switching frequency and root frequencies etc. are given as frequency f. The conversion formula of those symbols is $\omega = 2\pi f$.

The following control to output transfer function for the buck converter (7.9) models the behavior of the buck converter for frequencies up to $f_{\text{sw}}/2$ and considers all major influencing parameters of the converter. The ESR of the inductor R_{L} and the on-resistance of the switch $R_{\text{DS,on}}$ are not modeled. However, models that consider those parameters, such as in [161], show that they have no significant influence on the transfer function of the buck converter.

$$T(s) = \underbrace{\frac{R_{\text{Load}}}{R_{\text{shunt}}} \cdot \frac{1}{1 + \frac{R_{\text{Load}} T_{\text{sw}}}{L} \cdot (m_{\text{c}} \cdot (1-D) - 0.5)}}_{K} \cdot \underbrace{\frac{1 + \frac{s}{\omega_{\text{z1}}}}{1 + \frac{s}{\omega_{\text{p1}}}}}_{z1\ \&\ p1} \cdot \underbrace{\frac{1}{1 + \frac{s}{\omega_{\text{n}} Q_{\text{p}}} + \frac{s^2}{\omega_{\text{n}}^2}}}_{p2\ \&\ p3} \tag{7.9}$$

with

$$\omega_{\text{z1}} = \frac{1}{R_{\text{C}} C} \qquad m_{\text{c}} = 1 + \frac{S_{\text{e}}}{S_{\text{n}}}$$

$$\omega_{\text{p1}} = \frac{1}{R_{\text{Load}} C} + \frac{T_{\text{sw}}}{LC} [m_{\text{c}} \cdot (1-D) - 0.5] \qquad S_{\text{e}} = \frac{f_{\text{sw}} V_{\text{comp,pp}}}{R_{\text{shunt}}}$$

$$\omega_{\text{n}} = \frac{\pi}{T_{\text{sw}}} \qquad S_{\text{n}} = \frac{V_{\text{in}} - V_{\text{out}}}{L}$$

$$Q_{\text{p}} = \frac{1}{\pi (m_{\text{c}} \cdot (1-D) - 0.5)}$$

In this work the nominal parameters of the buck converter are as follows: $V_{\text{in}} = 14\,V$, $V_{\text{out}} = 6\,V$, $f_{\text{sw}} = 500\,kHz$, $T_{\text{sw}} = 2\,\mu\text{s}$, $V_{\text{comp,pp}} = 300\,mV$, $R_{\text{shunt}} = 500\,m\Omega$, $L = 20\,\mu H$, $C = 20\,\mu F$, $R_{\text{C}} = 25\,m\Omega$ and $R_{\text{Load}} = 20\,\Omega$. Calculating the frequencies of the roots results in

$$f_{\text{z1}} = 318\,kHz$$

$$f_{\text{p1}} = 800\,Hz$$

$$f_{\text{p2}} = 250\,kHz$$

$$f_{\text{p3}} = 250\,kHz$$

Figure A.3 shows the bode diagram resulting from the control to output transfer function shown in (7.9). The pole frequencies are marked with x. The zero frequency lays outside the modeled frequency range ($f_{\text{z1}} > f_{\text{sw}}/2$) and is therefore not shown in this diagram.

$p1$ is the dominant pole of the system and also $p2$ and $p3$ have essential influence especially on the phase behavior for higher frequencies. The zero $z1$ has only low impact on the transfer function in the shown frequency range. These insights will help to evaluate the influence of different circuit components in later chapters.

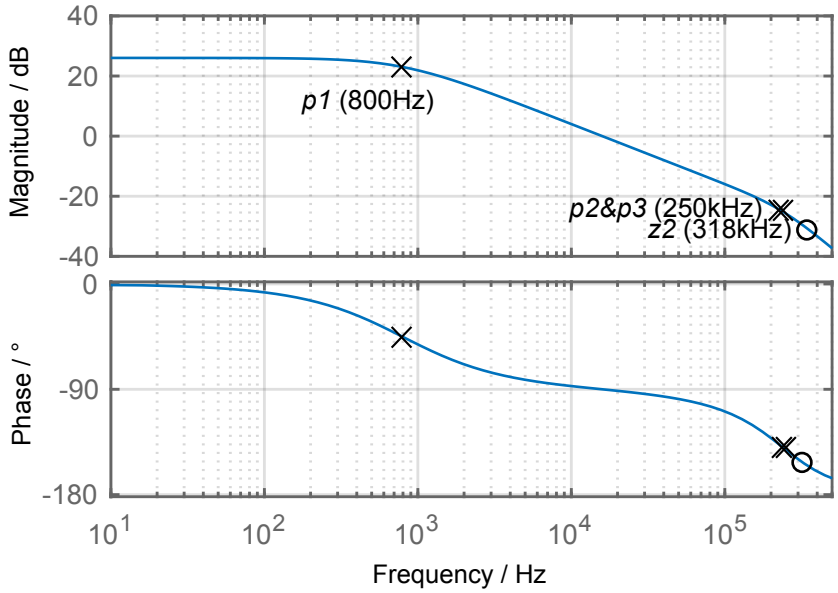

Fig. A.3: Bode plot of a buck converter.

B Parameter Identification

B.1 Identification Strategy in Buck Converters

This appendix derives that also for the buck converter the load, the inductor, and the capacitor are the relevant parameters for identification.

Relevant Parameters

The inductance L, its equivalent series resistance R_L, the capacitance C, its equivalent series resistance R_C and the load resistance R_Load underlie great variations. With the aid of bode diagrams the influence of individual parameter variations on the control-to-output transfer function T are evaluated. Figures B.4-B.6 show bode plots. In each plot one parameter is subject to variation, all other parameters have nominal values. In order to cover a broad variation range, three bode plots are shown for each parameter: $p = p_\mathrm{nom}$, $p = p_\mathrm{nom} \cdot 4$ and $p = p_\mathrm{nom}/4$, where p is the respective parameter and p_nom is its nominal value.

In a buck converter the crossover frequency f_c is usually chosen lower than $f_\mathrm{sw}/5$. In this work the switching frequency f_sw equals 500 kHz and hence, the maximum crossover frequency $f_\mathrm{c,max}$ is 100 kHz. The bode plots are investigated in the frequency range of $f_\mathrm{c,max}$ and lower. In Figs. B.4-B.6 the relevant frequency range is shaded in gray.

Figure B.4 shows that a variation of the inductance L leads to changes of magnitude and phase in the shaded frequency range. The ESR of the inductance R_L does not influence the transfer function.

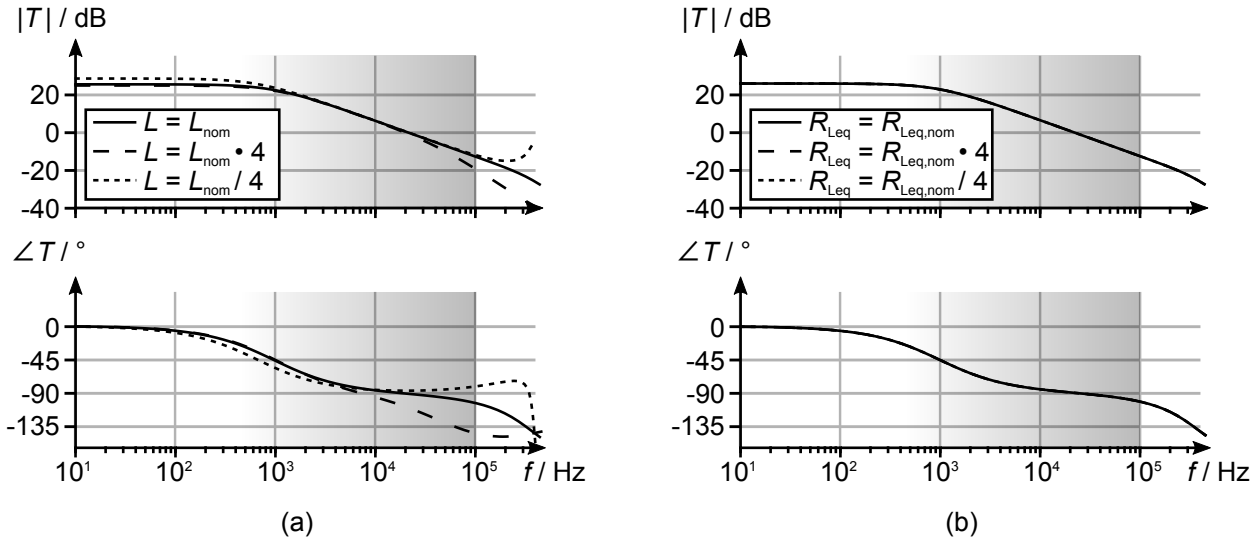

Fig. B.4: Bode plot of CMC buck converter control-to-output transfer function for nominal parameters (solid line) and for a deviation of the inductance L (a) and the ESR R_L (b) by a factor of 4 (dashed line) and 1/4 (dotted line), respectively.

Figure B.5 shows that variation of the capacitance C leads to deviations of magnitude and phase in the observed frequency range. The mainly positive phase rotation resulting from R_C variation is neglected, as this work aims to decrease the hardware effort as much as possible. This is well acceptable as positive phase rotations are irrelevant for control loop stability and bandwidth.

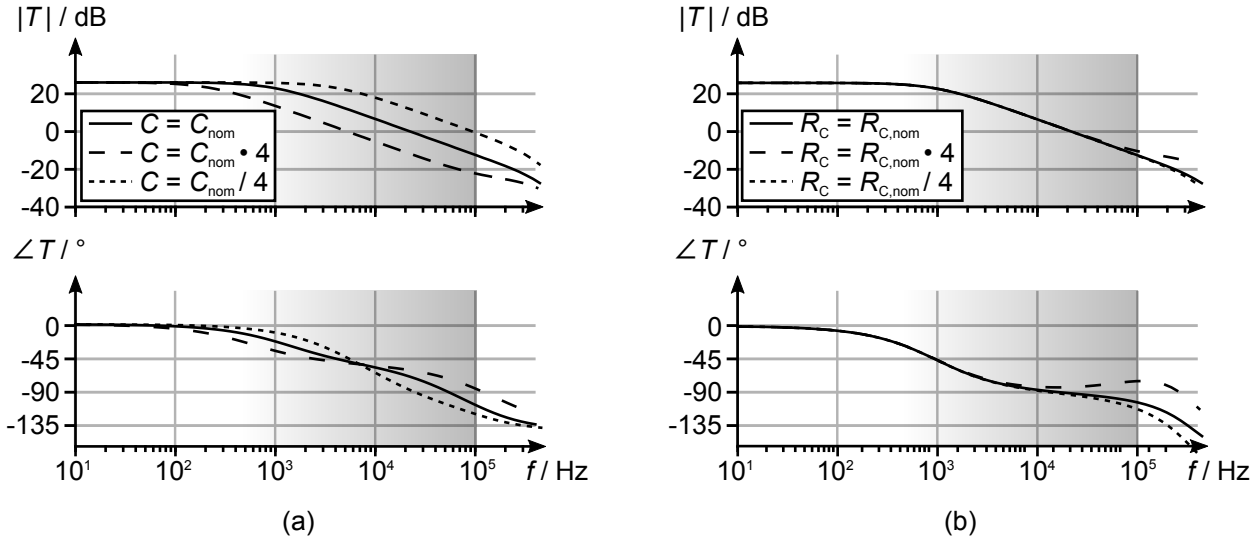

Fig. B.5: Bode plot of CMC buck converter control-to-output transfer function for nominal parameters (solid line) and for a deviation of the capacitance C (a) and the ESR R_C (b) by a factor of 4 (dashed line) and 1/4 (dotted line), respectively.

In Fig. B.6 it is shown that the load resistance has only minor influence on the magnitude in the valid frequency range. However, in the area of 1 kHz to 10 kHz the phase is clearly influenced by variation of the load resistance.

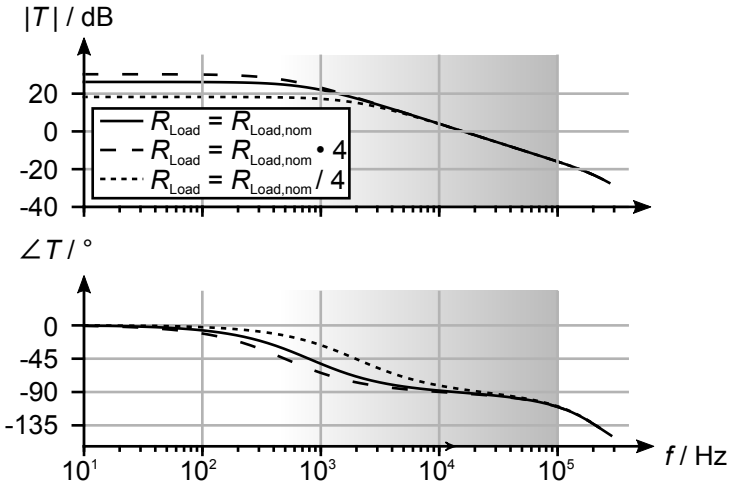

Fig. B.6: Bode plot of CMC buck converter control-to-output transfer function for nominal parameters (solid line) and for a deviation of the load resistance R_{Load} by a factor of 4 (dashed line) and 1/4 (dotted line), respectively.

Table B.1 summarizes the influence of each investigated parameter on magnitude and phase in the valid frequency range. A '+' denotes that a parameter has a relevant impact on T and a '–' indicates that a parameter has only minor or no influence.

Tab. B.1: Influence of parameters on the buck converter control-to-output transfer function.

Parameter		L	C	R_{L}	R_{C}	R_{Load}
Influence on magnitude	$\lvert T(s)\rvert$	+	+	–	–	–
Influence on phase	$\angle T(s)$	+	+	–	–	+

The inductance L, the capacitance C and the load resistance R_{Load} are the most influential parameters of a CMC buck converter in the region of the crossover frequency f_{c}.

Pulsed Startup Identification

In the initial state of a buck converter the inductor current i_{L} is equal to 0 A. The inductance can be identified by ramping up the inductor current to the inductor peak current $I_{\mathrm{L,peak}}$, specified by the digital controller. At first, a defined peak current value $I_{\mathrm{L,peak}}$ is set at the controller output, followed by turning on the switch.

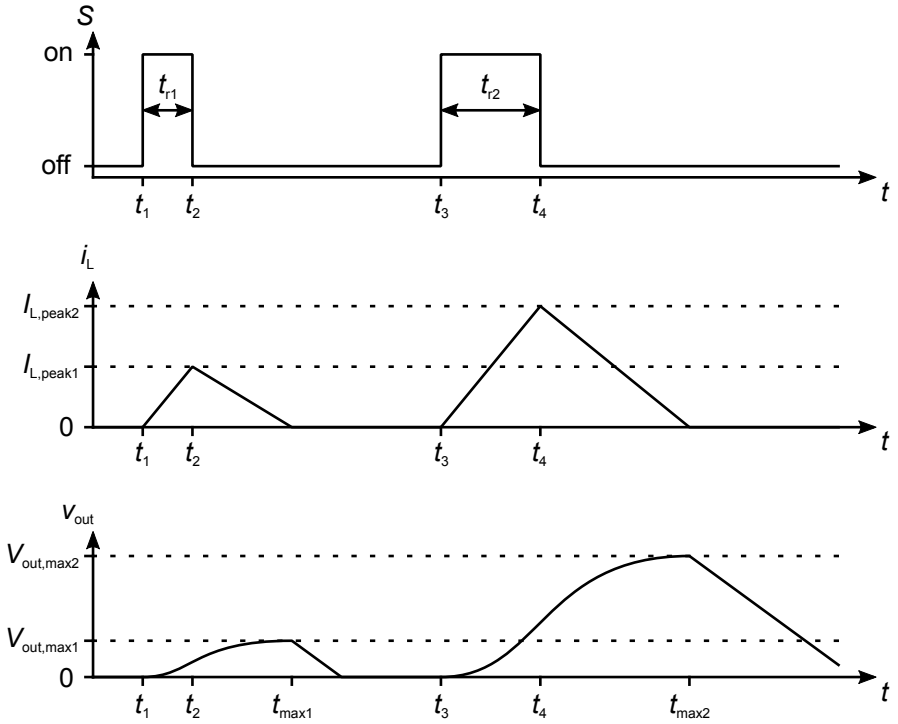

Fig. B.7: Switch state S, inductor current i_L and output voltage v_{out} during buck converter startup identification.

When the inductor current reaches $I_{L,peak}$ the switch is turned off. Figure B.7 shows the described current ramp-up from zero current at $t = t_1$ to $I_{L,peak}$ at $t = t_2$.

In order to identify the inductance, the on-period of the switch has to be measured. The calculation of the inductance value follows the basic inductor equation (7.1). Solving the equation for L and applying the actual values for v_L, di_L and dt leads to:

$$L = \frac{V_{in}}{I_{L,peak}} \cdot t_{on} \tag{7.10}$$

The identification can be improved by a second inductor current ramp-up compensating offset errors, as shown in Fig. B.7. Therefore, the identification equation changes according to the boost converter identification shown in Section 5.3.1.

For calculation of the capacitance also the inductor current ramp-up can be used. Since the inductor current always flows towards the capacitor if there is no considerable load current, the total charge flowing onto the capacitor Q_C can be calculated with:

$$Q_C = \frac{I_{L,peak}}{2} \cdot (t_{max} - t_1) \tag{7.11}$$

Measuring the output voltage $V_{\text{out,max}}$ at the time when the inductor current reaches 0 A, i.e. when the output voltage reaches its maximum value, the capacitance can be calculated by:

$$C = \frac{I_{\text{L,peak}}}{2 \cdot V_{\text{out,max}}} \cdot (t_{\text{max}} - t_1) \tag{7.12}$$

The described inductor current and output voltage behavior can be seen in Fig. B.7 above.

B.2 Analysis of the Application Range - Load Identification

The on-time t_{on} is measured with digital counters that are based on a digital system clock $f_{\text{clk}} = 1/T_{\text{clk}}$ and thus have a finite resolution. Consequently, the maximum on-time measurement error is $T_{\text{clk}}/2$, as the actual time may be longer or shorter by $T_{\text{clk}}/2$ than the measured time. The time measurement inaccuracy results in a load current identification inaccuracy. In the Appendix B.2, this inaccuracy is displayed for different values of the load current to be identified, the present input voltage and the inductance, in Fig. B.8. All other parameters are kept at their nominal values. The graph show that the time measurement inaccuracies only cause approximately 1 % or less error in all operating points and can hence be neglected.

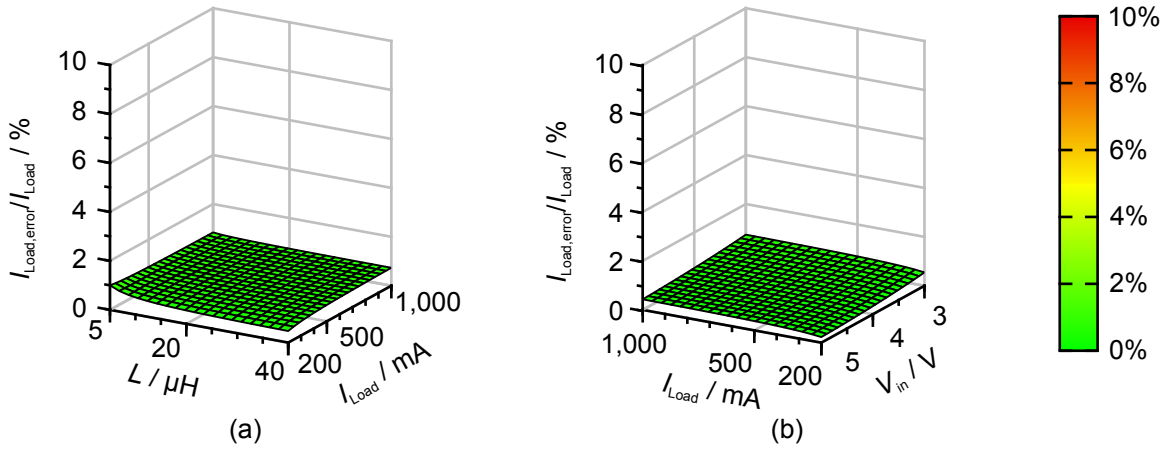

Fig. B.8: Relative I_{load} identification inaccuracy caused by a maximum 8 ns time measurement inaccuracy ($f_{\text{clk}} = 62.5\,\text{MHz}$) (a) as function of the absolute I_{load} and L with $V_{\text{in}} = 3\,\text{V}$ and (b) as function of the absolute I_{load} and V_{in} with $L = 20\,\mu\text{H}$.

B.3 Linear Regression Algorithm for Output Voltage Slope Measurement

Conventional ADCs in digital control of SMPS usually operate with limited resolution, sampling once per converter switching period. Higher sampling rates can be achieved with the delay line ADC proposed in this work. For the output capacitor identification the slope of the output voltage within one converter switching

cycle has to be determined, see Section 5.3.3. With a sufficient amount of samples a linear regression algorithm helps improving the accuracy of the dV_{out}/dt measurement.

During the linear voltage decrease the ADC samples the output voltage V_{out} with its maximum sampling rate and collects as much samples as possible. The recorded samples are forwarded to a linear regression algorithm. In linear regression a linear equation is estimated from a number of data points using the method of least squares. In this case only the slope m of the linear equation is of interest. The slope can be calculated with:

$$m = \frac{n \cdot \sum_{i=1}^{n} x_{\text{i}} y_{\text{i}} - \sum_{i=1}^{n} x_{\text{i}} \cdot \sum_{i=1}^{n} y_{\text{i}}}{n \cdot \sum_{i=1}^{n} x_{\text{i}}^2 - \left(\sum_{i=1}^{n} x_{\text{i}} \right)^2} \tag{7.13}$$

x_{i} are the time points of the ADC samples. If linear regression is performed with fixed time samples (7.13) can be simplified to:

$$m = a_1 \cdot \sum_{i=1}^{n} x_{\text{i}} y_{\text{i}} + a_2 \cdot \sum_{i=1}^{n} y_{\text{i}} \tag{7.14}$$

with

$$a_1 = \frac{n}{n \cdot \sum_{i=1}^{n} x_{\text{i}}^2 - \left(\sum_{i=1}^{n} x_{\text{i}} \right)^2} = const. \tag{7.15}$$

$$a_2 = \frac{-\sum_{i=1}^{n} x_{\text{i}}}{n \cdot \sum_{i=1}^{n} x_{\text{i}}^2 - \left(\sum_{i=1}^{n} x_{\text{i}} \right)^2} = const. \tag{7.16}$$

In case of n data points (7.14) can be calculated using only $2n+1$ summations and $n+2$ multiplications.

The result m of (7.14) is a good estimate of the voltage-time derivate dV_{out}/dt. With dV_{out}/dt and I_{load} the capacitance C can be calculated according to Eq. (5.15).

The voltage-time derivative dV_{out}/dt is calculated with the linear regression Eq. (7.13). The error of the linear regression equation is dependent on the number of samples n and the number of distinct samples d. For several combinations of n and d more than 100,000 different linear equations are generated, digitized

and inserted into the linear regression equation. Then, the output of the linear regression is compared to the actual slope and the error is determined.

In Fig. B.9 six histograms are shown. They show the relative density D of how often a certain calculation error occurred in the 100,000 test cases. For instance, Fig. B.9(a) shows that in case of a linear regression with eight samples and three distinct samples a calculation error of 0 %-2 % occurred in around 7 % of all test cases. Additionally, it is stated how many of the test cases lay in the window of $\pm 5\,\%$ error ($p_{\pm 5\%}$) and in the window of $\pm 10\,\%$ error ($p_{\pm 10\%}$).

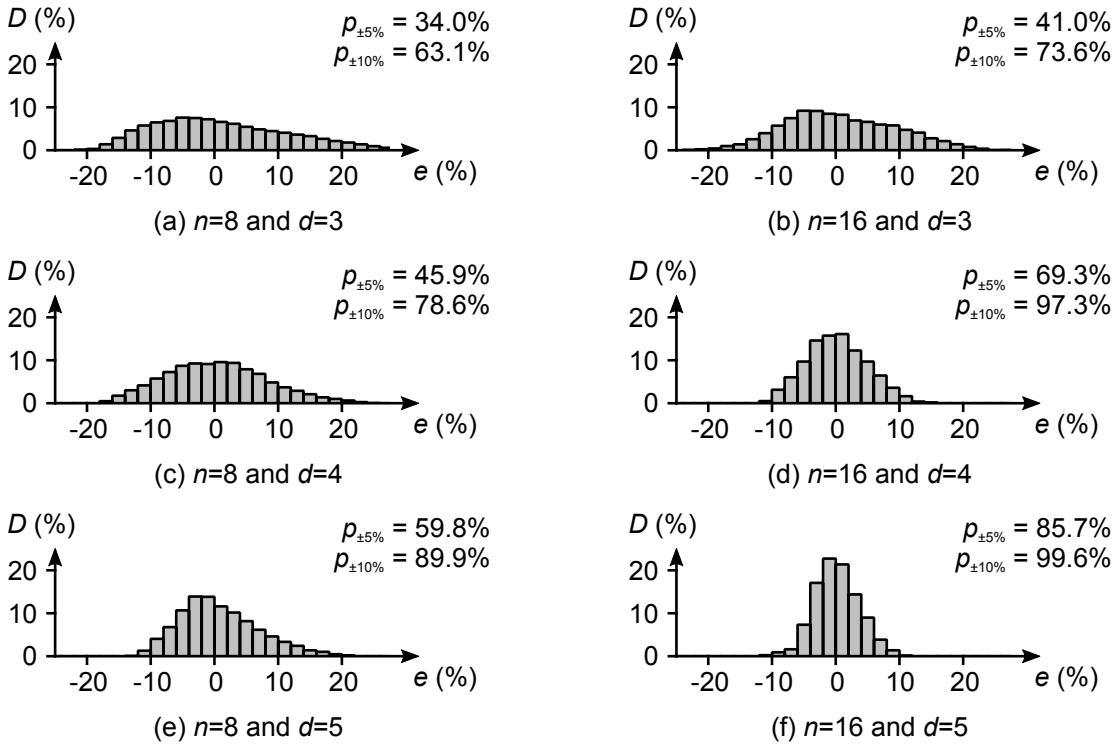

Fig. B.9: Error distribution for different combinations of number of samples n and number of distinct samples d.

The linear regression equation yields a low error for a large number of samples n and for a large number of distinct samples d. The number of samples n can be increased if the ADC sampling rate is increased or if the switch is forced to stay on for a longer time, e. g. two switching cycles. A large number of distinct samples is obtained if the load current is high and hence the voltage-time derivative is large and/or if the ADC resolution is high. When the switch is forced to stay on for two switching cycles ($n = 16$) and four distinct samples are recorded a calculation error of less than 10 % is expected.

B.4 Inductor and Capacitor Reference Measurements

Table B.2 shows the inductances measured with the help of an impedance analyzer. The inductors are examined at $f = f_c = 10\,\text{kHz}$ and at $f = f_{sw} = 500\,\text{kHz}$.

Table B.3 shows the inductances measured with the help of an impedance analyzer. The inductors are examined at different excitation frequencies and with different bias voltages.

C Experimental Verification of Fast Transient Controls

C.1 Nonlinear Control

Figures C.10 and C.11 show load transient responses of the conventional controller (configuration A) and the nonlinear controller. The output voltage deviations are reduced by up to a factor of 2 in case of load transients. Also, the recovery time is reduced by a factor of 1.6.

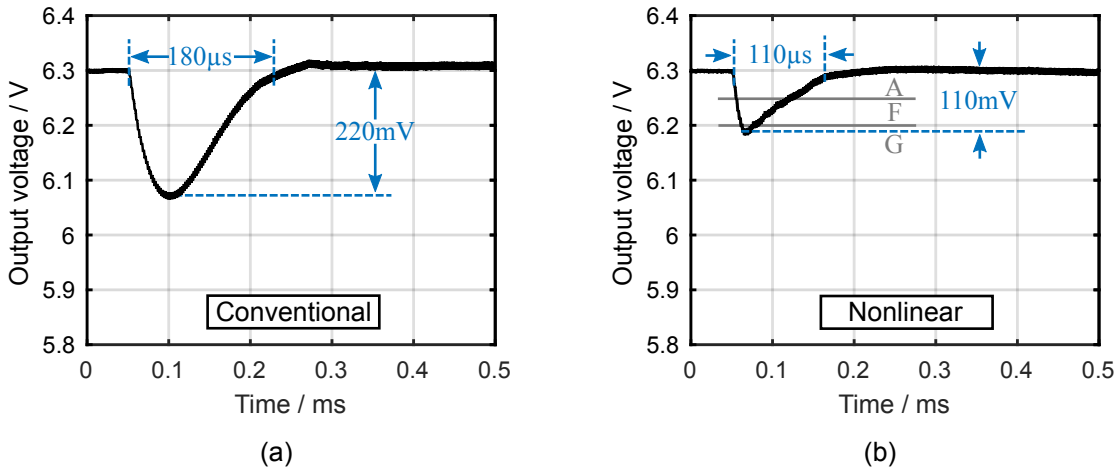

Fig. C.10: Nonlinear control: Measurement of the output voltage response to a load transient from 80 Ω to 40 Ω.

C.2 Minimum Deviation Control

Figures C.12 and C.13 show load transient responses of the conventional controller (configuration A) and the minimum deviation controller. The output voltage deviations are reduced by up to a factor of 3.2 in case of load transients. Also, the recovery time is reduced by a factor of 1.4.

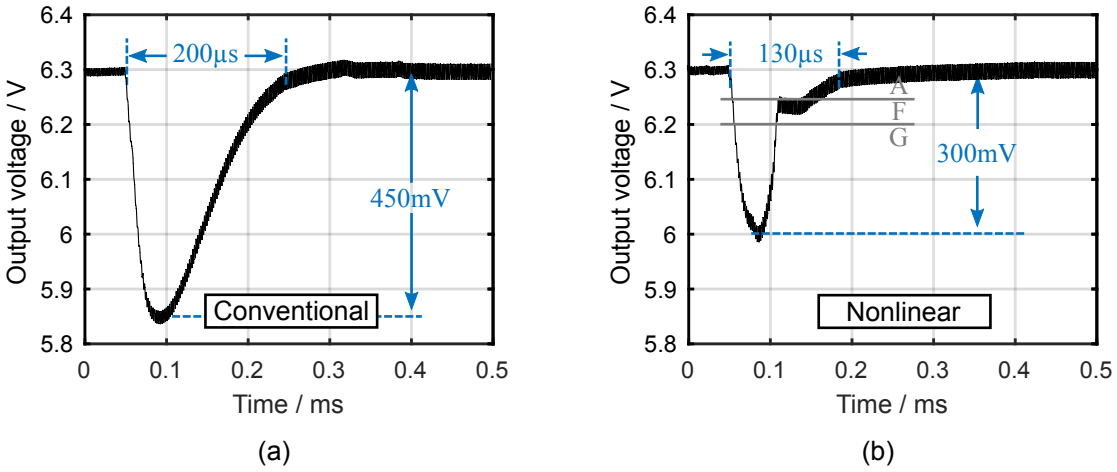

Fig. C.11: Nonlinear control: Measurement of the output voltage response to a load transient from 40 Ω to 20 Ω.

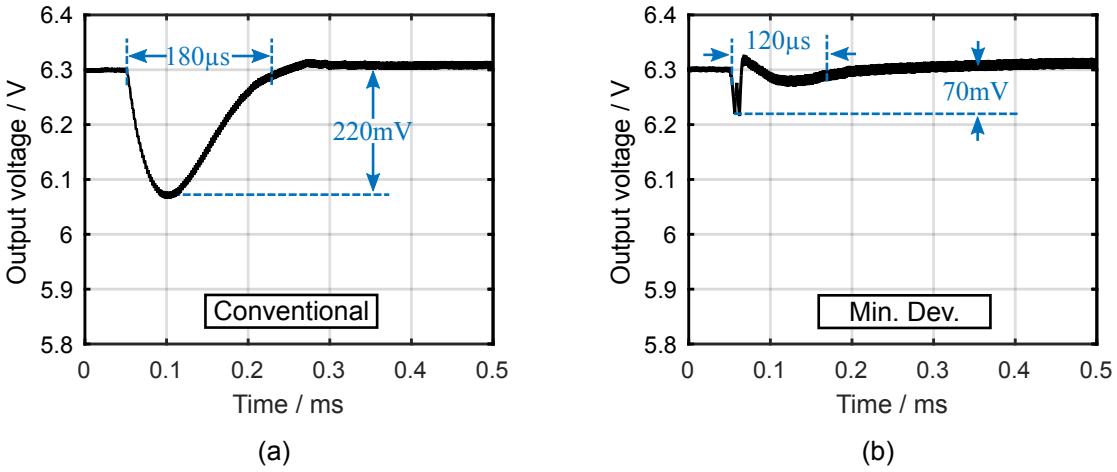

Fig. C.12: Minimum deviation control: Measurement of the output voltage response to a load transient from 80 Ω to 40 Ω.

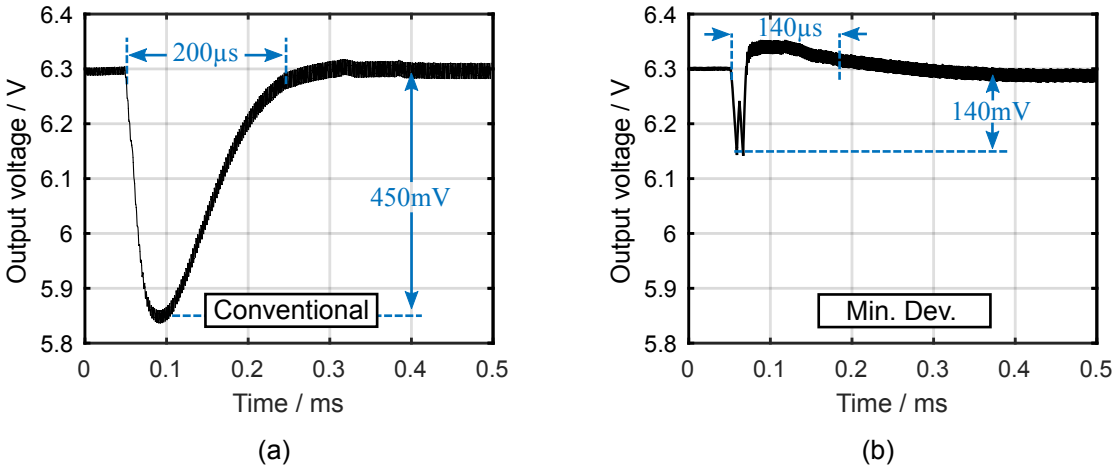

Fig. C.13: Minimum deviation control: Measurement of the output voltage response to a load transient from 40 Ω to 20 Ω.

Tab. B.2: Inductor array reference measurement results.

L_{nom} (µH)	L_{ref} (µH) @ $f = f_{\mathrm{c}} = 10\,\mathrm{kHz}$	L_{ref} (µH) @ $f = f_{\mathrm{sw}} = 500\,\mathrm{kHz}$,
1.3	1.72	1.65
2.0	2.29	2.20
3.3	3.71	3.61
4.7	5.32	5.18
6.0	6.75	6.59
6.7	7.29	7.11
8.0	8.71	8.51
11.0	12.05	11.75
12.3	13.48	13.16
13.0	14.04	13.70
14.3	15.46	15.11
15.7	17.04	16.63
17.0	18.47	18.04
17.7	19.00	18.56
19.0	20.42	19.96
22.0	21.69	21.17
23.3	23.13	22.59
24.0	23.69	23.12
25.3	25.12	24.53
26.7	26.71	26.08
28.0	28.15	27.49
28.7	28.68	28.01
30.0	30.11	29.41
33.0	33.36	32.54
34.3	34.79	33.96
35.0	35.35	34.49
36.3	36.79	35.91
37.7	38.34	37.42
39.0	39.77	38.83
39.7	40.30	39.35
41.0	41.74	40.75

Tab. B.3: Capacitor array reference measurement results.

C_{nom} (µF)	C_{ref} (µF) @ $f = f_{\text{sw}} = 10\,\text{kHz}$ $V_{\text{bias}} = 6\,\text{V}$	C_{ref} (µF) @ $f = f_{\text{sw}} = 500\,\text{kHz}$ $V_{\text{bias}} = 6\,\text{V}$	C_{ref} (µF) @ $f = f_{\text{sw}} = 10\,\text{kHz}$ $V_{\text{bias}} = 3\,\text{V}$
4.7	4.45	4.40	4.51
10.0	8.63	8.64	9.02
14.7	13.08	13.04	13.53
22.0	12.85	11.15	14.36
26.7	17.30	15.55	18.87
32.0	21.48	19.79	23.38
36.7	25.93	24.19	27.89

List of Publications by the Author

IEEE Publications

S. Quenzer-Hohmuth, J. Messner, S. Ritzmann, T. Rosahl, and B. Wicht, "Accelerated Low Gate Count Parameter Identification for Integrated Switched-Mode Power Supplies with Digital Control," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, 2019, pp. 2952-2956. **(Outstanding Presentation Award)**

S. Quenzer-Hohmuth, S. Ritzmann, T. Rosahl, and B. Wicht, "A Boost Converter with 3-6V Input and Fast Transient Digital Control Comprising a 90 ns-Latency Live-Tracking Window ADC," *ESSCIRC 2018 - IEEE 44th European Solid State Circuits Conference (ESSCIRC)*, Dresden, 2018, pp. 130-133.

S. Quenzer-Hohmuth, S. Ritzmann, T. Rosahl, and B. Wicht, "ΔV/Δt-Intervention Control Concept for Improved Transient Response in Digitally Controlled Boost Converters," *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 316-322.

S. Quenzer-Hohmuth, S. Ritzmann, T. Rosahl and B. Wicht, "Boost Converter with Load Dependent Adaptive Controller for Improved Transient Response," *2016 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Lisbon, 2016, pp. 1-4.

Other Publications

S. Quenzer-Hohmuth, C. Jiago, T. Rosahl, S. Ritzmann, and B. Wicht, "Delay-Line Analog-Digital-Wandler mit geringer Latenzzeit für digital geregelte Schaltwandler," *56th MPC Workshop*, Ravensburg, Germany, pp. 13-18, July 8, 2016, ISSN 1868-9221. **(Best Paper Award)**

S. Quenzer-Hohmuth, T. Rosahl, S. Ritzmann, and B. Wicht, "Challenges and Implementation Aspects of Switched-Mode Power Supplies with Digital Control for Automotive Applications," *Adv. Radio Sci.*, 14, 85-90, doi:10.5194/ars-14-85-2016, 2016.

Talks and Contributions to Talks

T. Rosahl, S. Ritzmann, and S. Quenzer-Hohmuth, "Digitally Controlled Switched-Mode Power Supplies," *3rd World Wide Bosch Design Summit* (Invited Talk), Reutlingen, Germany, October, 2018.

S. Quenzer-Hohmuth, "Digital Switched-Mode Power Supplies for Automotive Applications," *Digital Hardware Colloquium* (Invited Talk), Robert Bosch GmbH, Renningen, Germany, February, 2017.

B. Wicht, "Power Management Design for Highly Integrated Automotive ICs," *Tutorial at ESSCIRC 2017, 43th IEEE European Solid-State Circuits Conference*, Leuven, Belgium, Sept. 11-14, 2017.

Patents

"Vorrichtung und Verfahren zum Bestimmen eines Spulenwertes eines Spannungswandlers" ("Device and method for determination of a capacitor value in direct voltage converters"), patent pending.

"Vorrichtung und Verfahren zum Bestimmen eines Kondensatorwerts eines Spannungswandlers" ("Device and method for determination of a capacitor value in direct voltage converters"), patent pending.

"Live-Tracking Fensterkonzept für die Analog-Digital-Wandlung in digital geregelten Gleichspannungswandlern" ("Live-tracking window concept for analog-to-digital conversion in direct voltage converters"), filing date: 03/02/16, patent pending.

"Verfahren zur Regelung eines stromgesteuerten Gleichspannungswandlers und stromgesteuerter Gleichspannungswandler" ("Method for controlling a current-controlled direct voltage converter and current-controlled direct voltage converter"), filing date: 01/31/18, patent numbers: PCT/EP2018/052376, WO2018149643.

"Verfahren zur Optimierung des Betriebs eines in einem Regelkreis für einen Aufwärtswandler vorgesehenen digitalen Reglers sowie ein Regelkreis und ein Computerprogrammprodukt" ("Method for controlling a current-controlled direct voltage converter and current-controlled direct voltage converter"), filing date: 03/02/16, patent numbers: DE102016203366A1, WO2017148605A1.

Awards

Outstanding Presentation Award at APEC 2019: 'Accelerated Low Gate Count Parameter Identification for Integrated Switched-Mode Power Supplies with Digital Control', March 21, 2019 (Best presentation in a session with 24 presentations).

Best Paper Award of IEEE Solid-State Circuit Society, German Section, Workshop of Multi-Project-Chip-Group Baden-Württemberg: 'Delay-Line Analog-Digital-Wandler mit geringer Latenzzeit für digital geregelte Schaltwandler', July 8, 2016.

VDE-Award 2015: Year's Best Student of the Master's programm Power and Micro-Electronics at Reutlingen University.

List of Master Theses Supervised by the Author

Jonas Messner: *Parameter Identification for Integrated Switched-Mode Power Supplies with Digital Control*, 2018.

Heiko Bürkle: *Konzepte zur Digital-Analog-Umsetzung in digital geregelten Schaltwandlern*, 2017.

Cedric Leonel Jiago Teffo: *Analog-Digital-Wandlung in digital geregelten Schaltwandlern*, 2016.

Andreas Schmid: *Low Power Konzepte für Abwärtswandler*, 2015.

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Professional Experience

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	Research Topic:	Integrated Switched-Mode Power Supplies
	Focus:	Robust Digital Control, Parameter Identification
	Teaching:	Design of Integrated Analog Circuits (Lab Courses)
11/2010 – 09/2012	**Robert Bosch GmbH - Various Assignments**	
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	Body Electronics, Automotive Electronics, Clayton, Australia	
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Studies

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