Heteroepitaxy of semiconductor–insulator layers and their interface properties

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Abstract

The epitaxial growth of Ba_2SiO_4 thin films on Si(001) by co-deposition of Ba and Si in an oxygen background pressure is systematically investigated with a focus on the epitaxial interface. A structural investigation is performed by employing x-ray photoelectron spectroscopy (XPS), low energy electron diffraction (LEED) and aberration-corrected scanning transmission electron microscopy (STEM). The stoichiometry at the interface turns out to be critically dependent on the oxygen background pressure during deposition. The key to the calibration of the oxygen pressure and the determination of the saturation point for a complete oxidation of the film is the line shape of the O 1s peak in XPS. Using a two-step approach, in which a crystalline 1 nm thick film is prepared first before the rest of the film is deposited, the successful growth of epitaxial films with a thickness of up to 16 nm is demonstrated. An annealing step at $670 - 690\,^\circ\mathrm{C}$ is needed to form the epitaxial interface. Films grown with a minimized oxygen pressure, i.e. an oxygen pressure just above the saturation point for a complete oxidation of the film, still feature 1/4 ML of O atoms in Si-O-Si bonding states. In comparison, the Ba_2SiO_4 bulk structure has only O atoms in Si-O-Ba bonding states. STEM shows that these films form an atomically sharp interface to Si(001) and that the Ba_2SiO_4 bulk structure is maintained up to the penultimate layer at the interface. Only one silicate layer is changed to a (2×3) structure, which is also observed in LEED, to match the (2×1.5) bulk structure to Si(001), neglecting relaxations. An interface model is proposed for the films grown with a minimized oxygen pressure, which features a pseudo-(2×1) reconstruction of the Si surface and helps to understand the formation process of the epitaxial interface in greater detail.

An electrical characterization is done using MOS test capacitors. A dielectric constant of $k = 22.5 \pm 1.1$ is found for Ba_2SiO_4 in agreement with Ref. [1], as well as band offsets to Si(001) larger than 1.8 eV for crystalline layers. Moreover, leakage current densities as low as $2 \cdot 10^{-6}$ A/cm^2 at -1 V are measured for a 10 nm thick film. Interface trap densities at midgap of $(1.14 \pm 0.78) \cdot 10^{12}$ eV^{-1}cm^{-2} are measured for crystalline layers with an abrupt interface. Amorphous films show slightly higher interface trap densities of $(2.72 \pm 0.82) \cdot 10^{12}$ eV^{-1}cm^{-2} at midgap. A further reduction of the interface trap density is possible by incorporating a Si-rich silicate layer at the interface, thus bringing the conditions at the interface closer to those of the SiO_2/Si(001) interface. Crystalline films with such an interfacial layer have interface trap densities of $(3.32 \pm 0.45) \cdot 10^{11}$ eV^{-1}cm^{-2} at midgap, which is more than one order of magnitude lower than for films grown by Si diffusion from the substrate [1]. Moreover, the Fermi level of the Ba_2SiO_4 films appears to be pinned by surface states. However, even though no SiO_2 forms at the interface, the epitaxial interface still seems to contribute an offset of (0.56 ± 0.08) nm to the overall CET, which greatly limits the achievable minimum CET of the gate stack.

Contents

List of abbreviations

CB	Conduction band
CEM	Channel electron multiplier
CET	Capacitance-equivalent thickness
CL	Core level
CMOS	Complementary metal-oxide-semiconductor
DFT	Density-functional theory
EOT	Equivalent oxide thickness
fb	Flat band
FIB	Focused ion beam
FinFET	Fin field-effect transistor
HAADF	High-angle annular dark-field
HMDS	Hexamethyldisilazane
LEED	Low-energy electron diffraction
ML	Monolayer
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field-effect transistor
NIST	National Institute of Standards and Technology
QCM	Quartz crystal microbalance
rpm	Revolutions per minute *(unit)*
RSF	Relative sensitivity factor
RT	Room temperature
SEM	Scanning electron microscopy/microscope
SPA-LEED	Spot profile analysis low energy electron diffraction
STEM	Scanning transmission electron microscopy/microscope
TEM	Transmission electron microscopy/microscope
UHV	Ultra-high vacuum
VB	Valence band
VLSI	Very large-scale integration
XPS	X-ray photoelectron spectroscopy/spectroscope

1. Motivation and introduction

The complementary metal-oxide-semiconductor (CMOS) transistor is the fundamental switching device in micro- and nanoelectronic circuits. Over the years its dimensions have been continuously reduced in order to keep increasing the performance of the integrated circuits by increasing the number of active components per area and lowering the switching times of the transistors. However, there is a physical limit to this process due to the tunneling leakage currents that occur at low thicknesses of the gate dielectric. When the SiO_2 layer, which was originally used as the gate dielectric, became only about 1 nm thick, an unacceptably high density of power dissipation due to tunneling leakage currents occurred [2, 3], which lead to the search for an alternative material with a higher dielectric constant k [4, 5]. These so-called high-k materials offer the same capacitance at a higher physical layer thickness, thus greatly reducing the tunneling leakage currents, which are exponentially dependent on the layer thickness.

The high-k research was focused mainly on amorphous oxides, out of which HfO_2 has emerged as the best suited material for practical applications [4, 6, 7, 8, 9]. However, even the scaling with these high-k materials in planar transistor structures has reached a limit and in order to keep increasing the density of active components, three dimensional transistor structures, in particular the FinFET design [10], that focus on reducing the active area of the transistors by changing the fundamental structure of the transistor instead of simply reducing the thickness of the gate dielectric, have been developed. The main obstacle to a further reduction of the physical layer thickness of the gate dielectric is the formation of a well-defined, abrupt interface between the high-k material and silicon. The interface between the amorphous high-k oxides and silicon are typically rather defectious. In the case of HfO_2, low interface trap densities are achieved due to an interfacial SiO_2 layer, which arises naturally during the device processing [11]. However, such an intermediate layer reduces the total capacitance, since the capacitances of the HfO_2 and SiO_2 layers add up reciprocally, thus severely limiting the scaling at very low thicknesses. The initial thickness of this SiO_2 layer is also rather difficult to control, which is why scavenging techniques have been developed in order to reduce its thickness retroactively [12].

A continuation of the scaling to the lowest possible layer thickness of the gate dielectric requires the formation of an atomically sharp interface with an extremely low defect density surpassing even the SiO_2/Si interface. This can be achieved by implementing crystalline gate oxides [6, 13, 14]. McKee et al. have already shown that epitaxial $BaTiO_3$ can be grown on Ge(001) with an interface trap density $D_{it} < 10^{10}$ $eV^{-1}cm^{-2}$ by using a layer sequencing technique to manipulate the interface [15]. Nevertheless, a system with a crystalline oxide that fulfills this requirement while also meeting all other requirements for high-k gate dielectrics [4] has not been found. The band gap of $BaTiO_3$ is too small for practical application. Epitaxial $Ba_{0.7}Sr_{0.3}O$ lattice matched to Si(001) is thermodynamically unstable in contact with silicon and reacts with the substrate to form silicate at temperatures above 400 °C [16].

Crystalline Ba_2SiO_4 is a candidate that could potentially fulfill all requirements for a crystalline gate oxide. Even tough Ba_2SiO_4 has a tetragonal crystal symmetry, it grows epitaxially on Si(001), whereby its longest crystal axis grows perpendicular to the Si(001) surface, while the lattice constants in the other two crystal directions are approximately equivalent to 2 and 1.5 times the Si lattice constant in [110] direction, respectively [17, 1]. Ba silicates are thermodynamically stable, i.e. the reaction of the oxides SiO_2 and BaO to silicate is exothermic [18]. Moreover, silicates are in general also kinetically stable up to their desorption temperature above 750 °C [17, 19, 20, 21], making their thermal stability comparable to that of SiO_2. In addition, Ba_2SiO_4 also fulfills other important requirements placed upon high-k materials. Epitaxial films have shown a dielectric constant of 22.8 ± 0.2, band offsets to p-Si(001) of over 2 eV and an acceptable leakage current of 3 mA/cm^2 at -1 V [1]. The main problem that remains is that these films featured a high density of interface traps of $D_{it} = (1 \pm 0,5) \times 10^{13}$ eV^{-1}cm^{-2} [1]. One of the primary factors contributing to this is most likely the growth process, which relied upon the diffusion of Si from the substrate into a deposited BaO layer in order to form the silicate layers. The diffusion leads to an atomically rough interface and since it requires concentration gradients, it may introduce local disorder and variations of the chemical composition.

In order to avoid the diffusion problem, a co-deposition growth method, in which Ba and Si are evaporated simultaneously in an oxygen atmosphere, is implemented in this thesis. The expectation is that this will reduce the interface trap density. Also, this will hopefully allow for a reduction of the annealing temperature required to grow epitaxial films, since the diffusion of Si from the substrate is not required anymore. The films grown by Si diffusion from the substrate required a rather high annealing temperature of around 670 °C [1]. The main goal of this thesis is to gain an understanding of the intricacies of the epitaxial growth process of Ba_2SiO_4 on Si(001), in particular with respect to the formation of the epitaxial interface, in order to enable the purposeful manipulation of the interface. Therefore, the scope of this thesis is not limited to the search for alternative gate dielectrics, but also encompasses a contribution to the physical understanding of the formation of epitaxial semiconductor-insulator interfaces, which are of scientific and technological interest for various reasons beyond the use as a gate dielectric, e.g. as wave guides [22], barriers for tunnel junctions and spin filters [23].

A structural investigation of the Ba_2SiO_4 films and their epitaxial interface to Si(001) is performed by employing x-ray photoelectron spectroscopy (XPS), low energy electron diffraction (LEED) and aberration-corrected scanning transmission electron microscopy (STEM). MOS test capacitors are prepared in order to perform an electrical characterization. Parts of this thesis were already published in [24].

2. Scientific background

2.1. High-k materials

2.1.1. The MOSFET

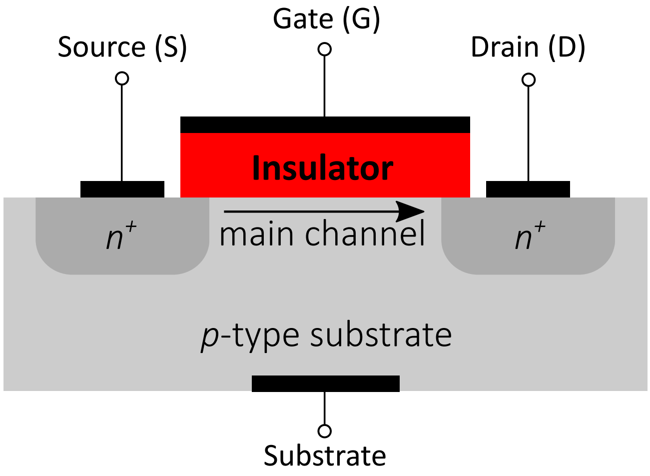

Figure 2.1.: Illustration of an n-channel metal-oxide-semiconductor field-effect transistor (MOSFET). Based on Ref. [25].

The metal-oxide-semiconductor field-effect transistor (MOSFET) is a voltage-controlled resistor. As illustrated in Fig. 2.1, it consists of a low doped semiconductor substrate, typically silicon, a source and a drain contact for the main current, a gate contact that is insulated from the source-drain-channel by a thin oxide layer and, optionally, a substrate contact at the back [25, 26]. In the case of a p-type substrate, as shown in the figure, the source and drain contacts are highly doped n-type regions. This creates an npn structure, so that the current flow from source to drain is inhibited due to the formation of depletion zones at the transitions of the doping regions. By applying a voltage to the gate contact so that the band edges of the silicon substrate bend down at the interface to the insulator until the Fermi level is close to the conduction band edge, thus populating the region close to the insulator with electrons, an inversion layer or n-channel is created between the source and drain contacts enabling a current flow [25] (see also section 2.5.1). The electron density in the inversion layer and thus the source-drain-current can be controlled with the gate voltage.

If an n-type substrate is used, the source and drain contacts are highly doped p-type regions and a p-channel is created between them by bending the band edges of the silicon up at the interface until the Fermi level is close to the valence band edge. Moreover, by doping the region of the substrate close to the insulator opposite to the rest of the substrate, a transistor is created that allows current flow between source and drain if no gate voltage is applied and can be switched off by applying a gate voltage.

In this work, only the middle part of the MOSFET without the source and drain contacts, i.e. MOS-capacitors, will be manufactured in order to characterize the Ba_2SiO_4 thin films.

2.1.2. Requirements for high-k materials

The gate stack works like a parallel-plate capacitor with the insulator as the dielectric. Its capacitance can be described by [4]:

$$C = \varepsilon_0 k \frac{A}{d}, \tag{2.1}$$

with ε_0 being the vacuum permittivity, k being the dielectric constant of the insulating layer, d being its thickness and A being its area. For a long time SiO_2 was used as the gate dielectric. In order to increase the density of the active elements as well as the switching speeds, the dimensions of the transistors have been continuously reduced. During this process, the thickness of the dielectric has to be reduced by the same factor as the area, i.e. the *square* of the gate length, to keep the same capacitance (see equation 2.1). Eventually, when the SiO_2 layer was only a few nanometers thick, the tunneling leakage currents became so large that they resulted in an unacceptably high density of power dissipation [2, 3]. It follows from equation 2.1 that the only way to increase the thickness of the dielectric and thereby reducing the tunneling currents, while keeping the active area and the capacitance of the gate stack unchanged, is to increase the dielectric constant of the gate insulator. Therefore, the search for suitable alternative gate insulators with a higher dielectric constant than SiO_2 ($k = 3.9$), so-called high-k materials, began [4, 5].

To characterize the high-k materials, the equivalent oxide thickness (EOT), which is the thickness that an SiO_2 layer with the same capacitance per area would have, is defined [4]:

$$EOT = \frac{3.9}{k} \cdot d, \tag{2.2}$$

where 3.9 is the dielectric constant of SiO_2, k is the dielectric constant of the high-k material and d is its thickness.

While a high dielectric constant is needed to reduce the tunneling leakage currents, there is a limit to the possible increase due to the inverse relationship between k and the band gap of the insulator (see Fig. 2.2). A large band gap is the prerequisite for large band offsets to silicon, which are required to inhibit carrier injection from the silicon into the insulator, since this would lead to leakage currents through the insulator. Moreover, there are several requirements for alternative gate dielectrics with regard to

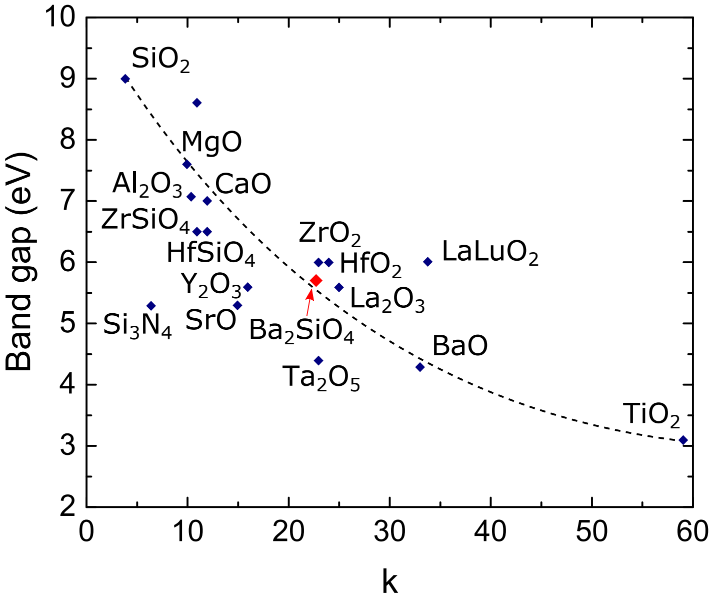

Figure 2.2.: Band gap vs. dielectric constant *k* for candidate gate insulators [4, 27]. Ba_2SiO_4 data taken from [1].

its interface to silicon, since this is where the main source-drain current flows, and its thermodynamic and kinetic stability. The requirements for practical application can be summed up as follows [4]:

1. The dielectric constant *k* must be high enough so that the material can be used for multiple scaling cycles. It should be at least greater than 12 and preferably greater than 25.
2. The material must function as an insulator. In particular, this means that the conduction and valence band offsets between the gate dielectric and silicon must be at least greater than 1 eV in order to minimize charge carrier injection into the gate dielectric [28]. Since the band offsets are usually not symmetrical, the material should ideally have a band gap greater than 5 eV, which limits the the maximum dielectric constant to about 30 due to the correlation shown in Fig. 2.2 [4, 28]. Furthermore, no other parasitic conduction mechanisms should occur.
3. It must form a high quality electrical interface with silicon, i.e. low interface roughness, no interface states or defect states in the Si band gap [29] and high charge carrier mobility.
4. Low density of electrically active defects, i.e. interface traps, fixed charges and bulk traps.
5. Thermodynamic stability in contact with Si: The material must not react with the silicon substrate, since this would result in the formation of a different chemical compound at the interface, which can affect the properties of the gate stack, in particular the effective k-value, negatively.

6. Kinetic stability: It has to be possible to process the material at 1000 °C for 5 s, so that it is compatible with the standard CMOS processing. This requirement can be circumvented by using a gate last process [30, 31].

The dielectric constant is the sum of an electronic and a lattice contribution. The electronic contribution k_e is the same as the optical dielectric constant and therefore the refractive index squared, which is typically 4-5 and at a maximum 8 [32]. Hence, the majority of the dielectric constant has to come from the lattice contribution k_l, which is given by [33, 32]

$$k_l = \frac{Ne^2 Z_T^{*2}}{m\omega_{TO}^2}, \tag{2.3}$$

where N is the number of ions per unit volume, e is the elementary charge, Z_T^* is the transverse dynamic effective charge, m is the reduced ion mass and ω_{TO} is the frequency of the transverse optical phonon. In order to obtain large values of k_l, Z_T^* has to be large and/or ω_{TO} has to be small. The variation of these two parameters with the band gap also explains the variation of the dielectric constant seen in Fig. 2.2 [32]. On the one hand, Z_T^* is due to the rearrangement of the electronic charge as a consequence of ion movement. Since this rearrangement requires the electrons to be mobile and the minimum energy that the electrons in the valence band have to overcome in order to become mobile is the band gap, Z_T^* increases with decreasing band gap. On the other hand, the transverse optical phonon frequency ω_{TO} is directly related to the energy of the transverse optical phonon by $E_{TO} = \hbar\omega_{TO}$. If this energy is larger than the band gap, the phonon can be absorbed by the solid. Consequently, the maximum ω_{TO} decreases with decreasing band gap.

2.1.3. Overview of the high-k material selection

Of the extensively studied candidates for an alternative gate oxide, HfO_2 ($k = 25$) has emerged as the best suited for practical applications. Compared to HfO_2, ZrO_2, while having the same k-value, is more reactive in contact with Si and can easily form a silicide [34]. Some of the oxides of the lanthanides have a higher dielectric constant and lower leakage currents than HfO_2, but they are hygroscopic [35, 36, 37]. Y_2O_3 is also a possible candidate, but is has a lower k-value, namely $k = 15$ [4], than HfO_2.

The silicates of the aforementioned oxides were also investigated, since they have higher crystallization temperatures [38, 39, 40]. However, their k-value is significantly reduced as compared to the respective high-k oxide (e.g. $HfSiO_4$: $k = 11$ vs. HfO_2: $k = 25$). Furthermore, in contrast to Ba_2SiO_4, which for thermodynamic reasons guarantees the absence of SiO_2 at the interface to Si (see section 2.2.1), the silicates of Y [41, 42], Hf, Zr and La [43, 44, 45] form interfacial SiO_2 layers.

HfO_2 has, however, also several drawbacks as a high-k gate oxide. Firstly, O vacancies lead to trap states close to the silicon conduction band [4]. Moreover, a SiO_2 layer forms at the interface to silicon due to the diffusion of O-atoms through the HfO_2 layer [11]. Although the SiO_2 layer has the upside of forming a well-defined interface to silicon with a low defect concentration and can therefore be desirable in low thicknesses, it ultimately represents a serious limitation for the scaling to EOTs below 1 nm due to the associated decrease of the effective dielectric constant.

The search for alternative gate dielectrics is mainly focused on amorphous materials. The argument against polycrystalline layers is that the grain boundaries might lead to higher leakage currents and that they can furthermore serve as diffusion paths for dopants from the silicon making it easier for an electrical breakdown to occur [4]. However, most of the oxides that are considered as alternative gate dielectrics have crystallization temperatures well below 1000 °C, so that nanocrystalline layers can easily form during the device processing [4, 46]. In particular, HfO_2 crystallizes at 400 °C [4]. In order to increase the crystallization temperatures nitrogen is built into the oxides, which also lowers the diffusion rates of atoms inside the layers [47]. Nevertheless, no difference in the leakage currents of amorphous and nanocrystalline HfO_2 layers was found experimentally [48, 49].

2.2. Barium silicates

Barium silicates are ionic compounds with Ba-ions as cations and anions consisting of SiO_4-tetrahedra. The various compounds are a mixture of BaO and SiO_2 in different ratios. Out of all the barium silicates, Ba_2SiO_4, which is the focus of this work, is the one with the highest Ba concentration. Its anions are single SiO_4-tetrahedra, while the anions of the compounds with higher Si concentrations all consist of multiple SiO_4-tetrahedra that are connected by an O-bridge, i.e. two tetrahedra share one O atom.

2.2.1. Thermodynamic stability

Ba_2SiO_4 is thermodynamically very stable. In particular, the reaction of the oxides SiO_2 and BaO to silicate is exothermic, i.e. the heat of formation ΔH from the oxides at room temperature (RT) is negative [18]:

$$2\ \mathrm{BaO} + \mathrm{SiO_2} \ \rightarrow\ \mathrm{Ba_2SiO_4}, \quad \Delta H_{298\,K} = -64.48\ \mathrm{kcal/mol}$$

Moreover, it is generally thermodynamically more favorable to form a silicate than to keep SiO_2 in the system:

$$\begin{aligned}
2\ \mathrm{BaO} + 4\ \mathrm{SiO_2} &\rightarrow \mathrm{Ba_2SiO_4} + 3\ \mathrm{SiO_2}, && \Delta H_{298\,K} = -64.48\ \mathrm{kcal/mol}\\
&\rightarrow 2\ \mathrm{BaSiO_3} + 2\ \mathrm{SiO_2}, && \Delta H_{298\,K} = -76.06\ \mathrm{kcal/mol}\\
&\rightarrow \mathrm{Ba_2Si_3O_8} + \mathrm{SiO_2}, && \Delta H_{298\,K} = -82.42\ \mathrm{kcal/mol}\\
&\rightarrow 2\ \mathrm{BaSi_2O_5}, && \Delta H_{298\,K} = -82.56\ \mathrm{kcal/mol}
\end{aligned}$$

With respect to the growth of Ba_2SiO_4 thin films on Si(001) this guarantees the absence of SiO_2 at the interface. However, excess SiO_2 does of course result in the formation of a silicate with a higher Si concentration than Ba_2SiO_4, which can impede the epitaxial growth and could impact the performance of the thin films negatively. Therefore, the oxidation of the Si substrate cannot be disregarded. From the above data, the energy gain from the incorporation of SiO_2 into the silicate seems to saturate at $Ba_2Si_3O_8$, at least at room temperature. However, for the growth of Ba_2SiO_4 this would already represent an extreme SiO_2 surplus of more than three times the necessary amount, so that is unlikely to have an effect in this case.

The incorporation of BaO into the silicate is also generally thermodynamically favorable:

$$\begin{aligned}
12\,\mathrm{BaO} + 6\,\mathrm{SiO_2} &\rightarrow 3\,\mathrm{BaSi_2O_5} + 9\,\mathrm{BaO}, & \Delta H_{298\,K} &= -123.84\ \mathrm{kcal/mol}\\
&\rightarrow 2\,\mathrm{Ba_2Si_3O_8} + 8\,\mathrm{BaO}, & \Delta H_{298\,K} &= -164.84\ \mathrm{kcal/mol}\\
&\rightarrow 6\,\mathrm{BaSiO_3} + 6\,\mathrm{BaO}, & \Delta H_{298\,K} &= -228.18\ \mathrm{kcal/mol}\\
&\rightarrow 6\,\mathrm{Ba_2SiO_4}, & \Delta H_{298\,K} &= -386.88\ \mathrm{kcal/mol}
\end{aligned}$$

Since Ba_2SiO_4 is, however, the barium silicate with the highest Ba concentration, excess BaO during the growth of Ba_2SiO_4 would remain as BaO.

The heats of formation for the various silicate formations above were determined using the data from Barany *et al.* [18]. These considerations also demonstrate that for the growth of Ba_2SiO_4 it is important to adjust the ratio of at least two of the three elements to avoid the formation of a different type of silicate.

2.2.2. Crystal structure and matching of Ba_2SiO_4 to Si(001)

The crystal structure of Ba_2SiO_4 is shown in Fig. 2.3a). As stated above, this is the only barium silicate crystal structure that has exclusively single SiO_4-tetrahedra as anions. As an example the crystal structures of $BaSiO_3$, which has infinite SiO_4-tetrahedra chains, and $Ba_2Si_3O_8$, which has chains of six SiO_4-tetrahedra, are shown in Figs. 2.3b) and c), respectively, for comparison. This means that all O atoms in Ba_2SiO_4 form exactly one bond to Si and one bond to Ba, while the other barium silicates all have a proportion of O atoms that form two bonds to Si. This fact can be used to calibrate the system by XPS (see sections 4.1 and 4.4).

Ba_2SiO_4 grows epitaxially on Si(001) with its c-axis normal to the surface [17, 1]. Disregarding the (2×1) reconstruction, the Si(001) surface has a square symmetry with a lattice constant of $a_{\mathrm{Si(001)}} = 3.84$ Å in [110] direction. The lattice constants of Ba_2SiO_4 along the a and b-axes are approximately equivalent to 2 and 1.5 times the Si(001) lattice constant, respectively. This means that, in principle, the Ba_2SiO_4 lattice constant in a-direction fits approximately 1:1 with the (2×1) reconstruction of the Si(001) surface, although it is not clear whether this reconstruction is maintained at the interface between an epitaxial Ba_2SiO_4 film and Si(001). The exact lattice mismatch between Ba_2SiO_4 and Si(001) depends on the source of the Ba_2SiO_4 lattice constants. A comparison of different sources is done in table 2.1.

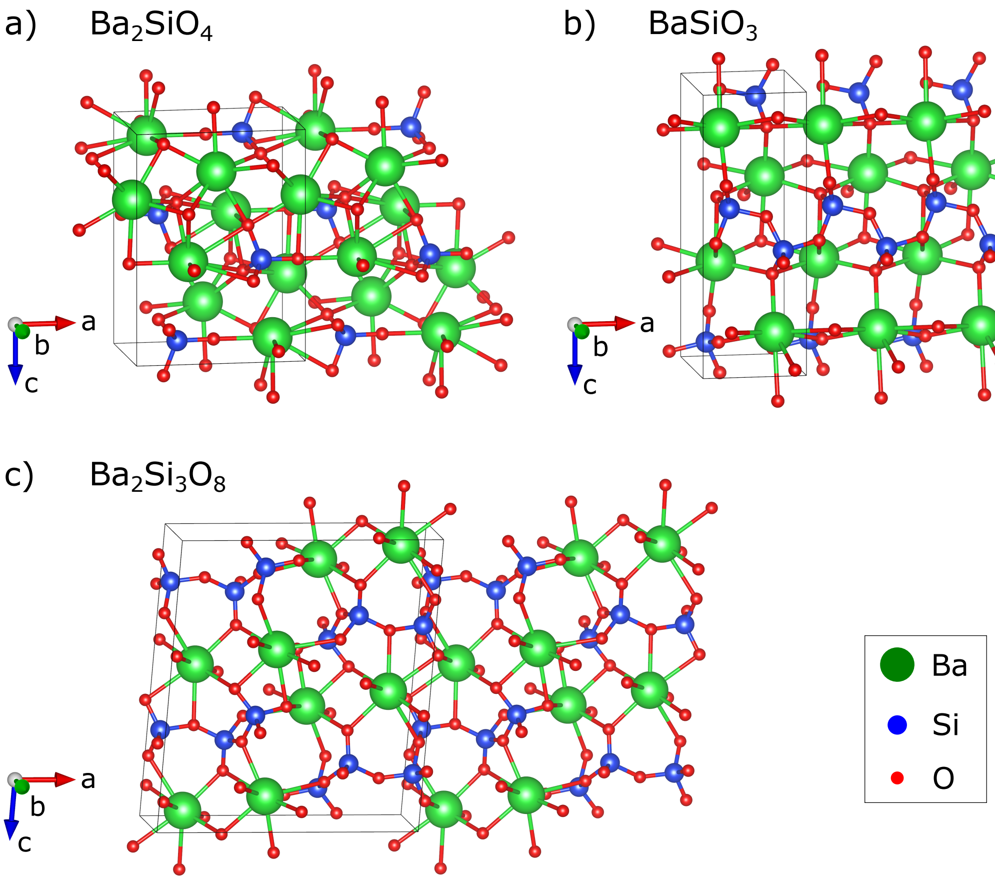

Figure 2.3.: Crystal structures of (a) Ba_2SiO_4 ($a = 7.602$ Å, $b = 5.884$ Å, $c = 10.413$ Å, $\alpha = \beta = \gamma = 90°$), (b) $BaSiO_3$ ($a = 4.638$ Å, $b = 5.692$ Å, $c = 12.708$ Å, $\alpha = \beta = \gamma = 90°$), (c) $Ba_2Si_3O_8$ ($a = 12.665$ Å, $b = 4.756$ Å, $c = 14.149$ Å, $\alpha = \gamma = 90°$, $\beta = 93.472°$). The wire boxes mark the unit cells. Drawn with VESTA [50] with data from [51, 52, 53].

a / Å	**$a/a_{Si(001)}$**	**b / Å**	**$b/a_{Si(001)}$**	**Source**
7.602	**1.9797**	5.884	**1.5323**	Materials Project [51]
7.69	**2.0026**	5.86	**1.5260**	Springer Materials [54]
7.51	**1.9557**	5.81	**1.5130**	Norton *et al.* [17]
7.498	**1.9526**	5.805	**1.5117**	Pieper *et al.* [55]

Table 2.1.: Lattice constants a and b of Ba_2SiO_4 in Å and in multiples of the Si(001) lattice constant $a_{Si(001)} = 3.84$ Å from different sources

2.3. Low energy electron diffraction

Low energy electron diffraction (LEED) is a method for studying the structure and morphology of surfaces. It was discovered by Davisson and Germer in 1927 [56] and has since become one of the most important surface science techniques. The technique is based on the analysis of the interference pattern created by the elastic scattering of electrons on a crystal lattice. Monochromatic electrons are accelerated onto the sample and the resulting diffraction pattern is either made visible with a fluorescent screen or recorded with a channel electron multiplier (CEM). A retarding grid ensures that only elastically scattered electrons reach the screen or the CEM.

Low energy electrons with energies between $50-200$ eV are used for two reasons: First, their de Broglie wavelength [57]

$$\lambda(\text{Å}) = \sqrt{\frac{150.4}{E(\text{eV})}} \tag{2.4}$$

is between 0.9 Å (200 eV) and 1.7 Å (50 eV), and therefore in the dimensions of the typical lattice constants in crystals, making it possible for diffraction phenomena to occur. Second, due to the short mean free path between approximately 0.4 and 0.9 nm, which corresponds to about two to four monolayers, of the electrons in this energy range they are highly surface sensitive [58].

2.3.1. Kinematic approximation and Ewald construction

The kinematic approximation is a simple method to describe the diffraction on a crystal, that only considers single scattering. The diffraction from the atoms at the positions $\vec{r}(n)$ can be described as a sum of electron wave functions with the incident wave vector $\vec{k}_i$ and the scattering vector $\vec{K}$, which is defined as the difference of the incident wave vector and the final wave vector $\vec{k}_f$, as follows [57]

$$\Psi(\vec{K},\vec{k}_i) = \sum_n f(n,\vec{K},\vec{k}_i)\exp\left(i\vec{K}\cdot\vec{r}(n)\right), \tag{2.5}$$

where $f(n,\vec{K},\vec{k}_i)$ is the structure factor at the positions $\vec{r}(n)$. The absolute square of this wave function gives the intensity of the diffraction spots [57]

$$I(\vec{K},\vec{k}_i) = |\Psi(\vec{K},\vec{k}_i)|^2 = \sum_{n,m} f(n,\vec{K},\vec{k}_i)f^*(m,\vec{K},\vec{k}_i)\exp\left(i\vec{K}\cdot(\vec{r}(n)-\vec{r}(m))\right) \tag{2.6}$$

This also means that the phase information is unfortunately lost in the diffraction experiment, so that an unambiguous reconstruction of the real space structure is not possible.

The diffraction spot intensity assumes a local maximum, i.e. diffraction spots are observed, when the Laue condition

$$\vec{K} = \vec{k}_i - \vec{k}_f = \vec{G} \tag{2.7}$$

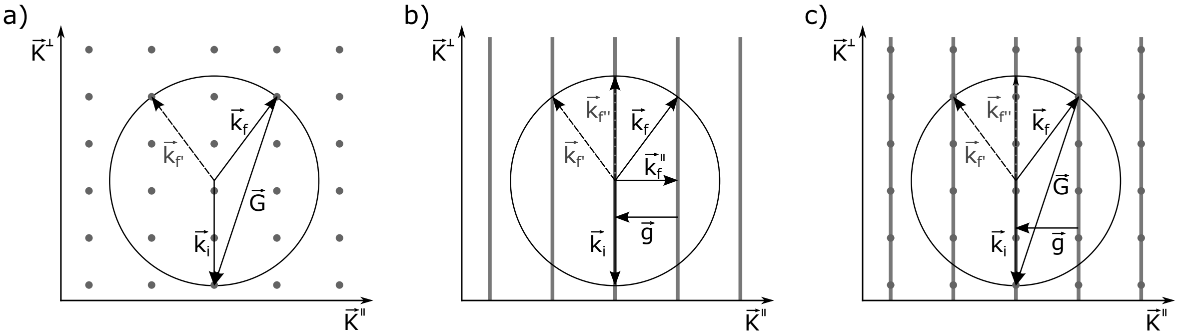

Figure 2.4.: Ewald construction for the scattering on a 3D crystal (a), a 2D crystal (b) and the scattering of low energy electrons on a real surface (c). There are multiple final wave vectors $\vec{k}_f$ for a given incident wave vector $\vec{k}_i$. The reciprocal lattice vector is only drawn for one final wave vector.

is fulfilled, where $\vec{G}$ is a reciprocal lattice vector, for which $\vec{G}_a \cdot \vec{R}_b = 2\pi\delta_{a,b}N$, $a, b = 1, 2, 3$ holds, with $\vec{R}$ being a real space lattice vector, $\delta_{a,b}$ being the Kronecker delta and N being an integer. A graphic determination of all occurring $\vec{k}_f$ for a given $\vec{k}_i$ is possible with the Ewald construction (see Fig. 2.4a)), which is obtained as follows: The vector $\vec{k}_i$ is drawn into the reciprocal lattice in such a way that its end point coincides with a reciprocal lattice point. Then a sphere with the radius $|\vec{k}_i|$, which represents the conservation of energy during the elastic scattering process, is drawn around the starting point of the vector. Every reciprocal lattice point intersected by this sphere becomes the end point of a final wave vector $\vec{k}_f$, whose common starting point is the same as that of the incident wave vector.

In the case of the scattering on a two-dimensional lattice, the Laue condition only applies to the components of the wave vectors parallel to the surface

$$\vec{K}^{\parallel} = \vec{k}_i^{\parallel} - \vec{k}_f^{\parallel} = \vec{g}, \tag{2.8}$$

where $\vec{g}$ is the reciprocal lattice vector of the two-dimensional crystal. Since the periodicity perpendicular to the surface is infinite, the distance between the reciprocal lattice points becomes infinitely small, resulting in Ewald rods and a modified Ewald construction as shown in Fig. 2.4b). As a consequence, the diffraction on a two-dimensional lattice leads to generally more diffraction spots than the diffraction on a three-dimensional lattice.

The diffraction of low energy electrons on a real surface, while dominated by the surface, is still affected by the first few atomic layers below the surface due to the small penetration depth. This leads to an intensity modulation of the Ewald rods as indicated in Fig. 2.4c). A diffraction spot is observed when the Laue condition is fulfilled for the components of the wave vectors parallel to the surface. If it is also fulfilled for the vertical component, the intensity of the diffraction spot assumes a maximum.

The kinematic approximation is sufficient to describe the positions of the diffraction spots. However, the strong interaction of the electrons with the solid necessary for the high surface sensitivity also results in strong multi scattering effects, which are not considered in the kinematic approximation [59]. Therefore, a detailed description of the spot intensity, which in needed in particular for the determination of the positions of the atoms in the unit cell, requires the more sophisticated dynamic LEED theory, which takes multi scattering into account (see e.g. [60, 61]).

2.3.2. The SPA-LEED instrument

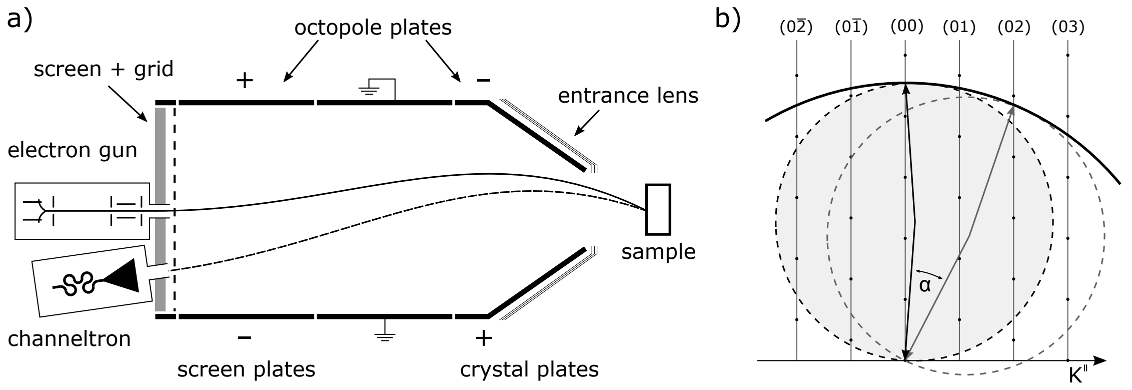

Figure 2.5.: The Spot Profile Analyzing LEED: (a) Illustration of a SPA-LEED instrument with an octupole deflection unit. (b) Modified Ewald construction in the case of the SPA-LEED in reciprocal space. As the deflection voltage is changed, the incident and final wave vectors move together drawing a circle (thick black line) around the starting point of the incident wave vector. The dashed lines mark the size of the regular Ewald sphere (see Fig. 2.4). [62, 63, 57]

In this work a Spot Profile Analyzing LEED (SPA-LEED), which is illustrated in Fig. 2.5a), is used to record LEED patterns. Electrons with energies between 10 and 500 eV are accelerated onto the sample surface by an electron gun. The scattered electrons are detected with a channel electron multiplier, also referred to as a channeltron, which is mounted at an angle of 4° to the electron gun. A grid in front of the detector ensures that only elastically scattered electrons are detected.

Between the electron gun and the sample sits the octupole deflection unit, which consists of three octupoles in series. Each octupole in turn consists of four plate capacitors arranged in angles of 45° to each other around the electron path. All plates of the middle octupole are grounded. The outer octupoles are polarized opposite to each other, thereby forcing the electrons on a parabolic path if a deflection voltage is applied. By varying the deflection voltages, the angle in which the electrons hit the surface, and thus the component of the respective wave vector parallel to the surface, can be changed, both in x and in y direction, making it possible to scan the reciprocal space [62, 63].

As the deflection voltage is changed, both the incidence and the reflection angle are varied by the same amount. As a result, in reciprocal space the incident wave vector and the final wave vector are turned together, with the angle between them remaining constant, which creates a modified Ewald construction with twice the radius of the regular Ewald sphere [57] as illustrated in Fig. 2.5b). Consequently, at the same energy the SPA-LEED measures a larger area of the reciprocal space than the conventional LEED. Moreover, the (00)-spot is recorded by the SPA-LEED, which is covered by the shadow of the electron gun in a conventional LEED.

If the deflection unit is switched off, the SPA-LEED can be used like a regular LEED by using the built-in screen instead of the channeltron to detect the electrons. This mode is mainly meant for maintenance. Moreover, there is an entrance lens that can be used to focus the electron beam on the sample, in order to correct for an inaccurate sample position.

2.3.3. Interpretation of LEED patterns

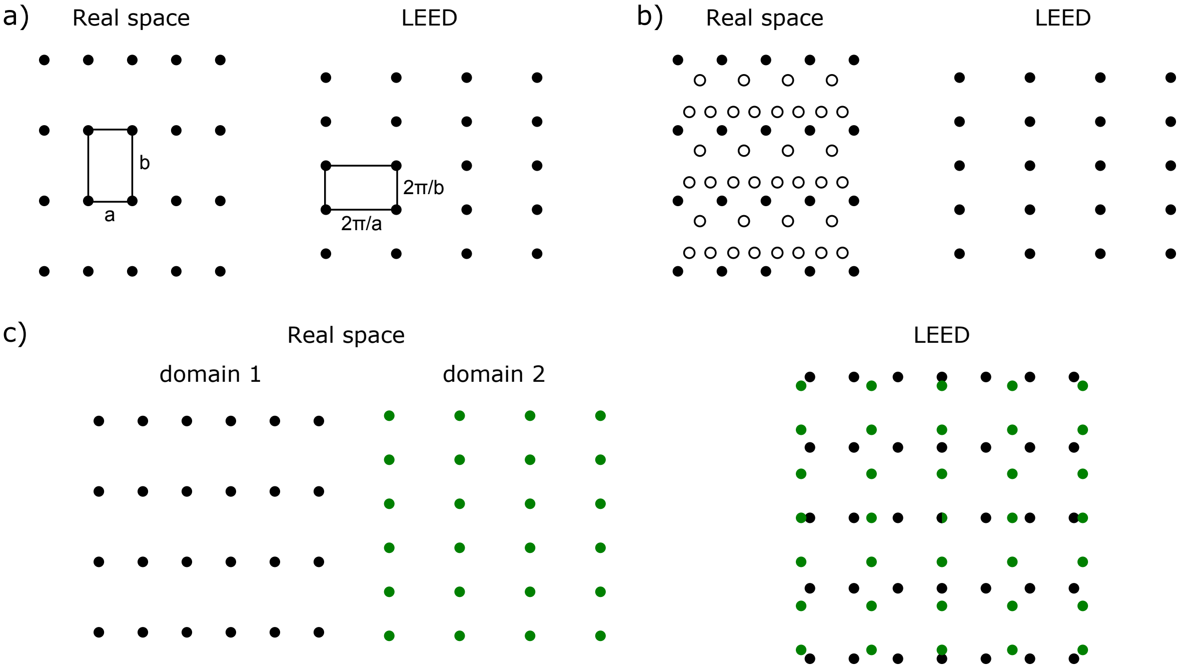

Figure 2.6.: Interpretation of LEED patterns: (a) A rectangular lattice in real and in reciprocal space. (b) The content of the unit cell, indicated with unfilled circles, does not affect the positions of the diffraction spots, only the intensities. (c) Two domains with rectangular lattices, turned by 90° to each other. The LEED image is a superposition of the corresponding reciprocal lattices.

The LEED pattern represents the reciprocal lattice of the investigated surface. With a regular LEED this is achieved by choosing an angle of incidence of 0° to the surface normal, so that $|\vec{k}_i^{\parallel}| = 0$. From equation 2.8 it then follows that the final wave vectors $\vec{k}_f^{\parallel}$ that lead to diffraction spots are equal to reciprocal lattice vectors. Hence, the LEED pattern becomes a representation of the reciprocal lattice. With a SPA-LEED this is achieved with the octupole deflection system. The joint rotation of the incident and final wave vectors in reciprocal space shown in Fig. 2.5b) can also be viewed as the rotation of the scattering vector $\vec{K}$, i.e. varying the deflection voltage of the octupole plates changes $\vec{K}^{\parallel}$. Thus, according to equation 2.8 the diffraction spots sit at the endpoints of reciprocal lattice vectors that start at the origin.

In the LEED pattern, a real space length a is represented by the reciprocal length $2\pi/a$. As illustrated in Fig 2.6a), this means that, while a rectangular real space lattice remains rectangular in the LEED pattern, the shorter side becomes the longer side and vice versa. Moreover, the arrangement of the LEED spots only represents the lattice of the investigated crystal. The contents of the unit cell, which are indicated in Fig 2.6b) with unfilled circles, do not affect the spot positions, but only their intensities. Lastly, real surfaces often feature more than one crystal domain, e.g. two rectangular lattices with the same lattice constants but at an angle of 90° to each other as illustrated in Fig 2.6c). In that case, the LEED pattern is a superposition of the reciprocal lattices.

2.4. X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) is a type of photoelectron spectroscopy that uses photons with energies in the $1-2$ keV range, which is high enough to release electrons from the atomic core levels. For this reason, the energies of the ejected electrons are characteristic of the chemical element they originate from, which enables a determination of the chemical composition of a sample by comparing the energies of the elastic peaks in the XPS spectrum with literature (for example Refs. [64, 65]). Moreover, small shifts of the elastic peaks depending on the chemical environment allow for a determination of the chemical bonding state of the respective atoms.

XPS is a surface sensitive technique, which is a result of the mean free path of the ejected photoelectrons. However, it is not quite as surface sensitive as SPA-LEED, due to the generally higher kinetic energy of the electrons. The contribution of each layer below the surface to the overall signal decreases exponentially with the combined thickness of the overlying layers, with the first approximately 6 nm contributing 95% of the signal [66]. This can also be used to estimate the thickness of thin films by measuring the intensity of a substrate peak.

2.4.1. Binding energy of core level peaks

XPS is based on the photoelectric effect. In the simplest description, a photon with the energy $h\nu$ hits a surface and is absorbed by an electron with the binding energy E_B. If the photon energy is larger than the sum of the binding energy of the electron and the work function Φ_s of the sample, the electron is released from the solid. It follows from the conservation of energy that

$$h\nu = E_B + E_{kin} + \Phi_s, \tag{2.9}$$

where E_{kin} is the kinetic energy of the photoelectron after it is released from the solid

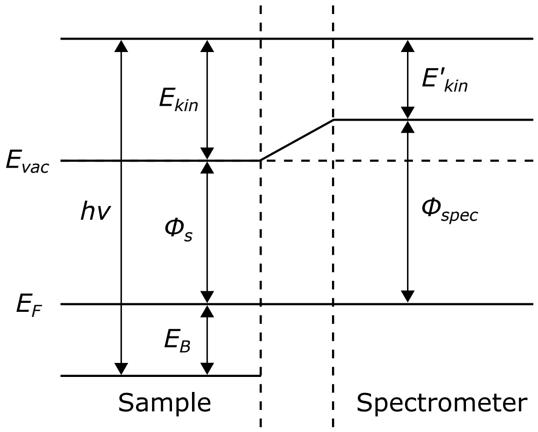

Figure 2.7.: Energy level diagram for the emission of a photoelectron and its detection by a spectrometer

and E_B and E_{kin} are given with respect to the Fermi level. The kinetic energy is then measured in a spectrometer that is in electrical contact with the sample, i.e. their fermi levels are aligned. Since the work functions of the sample Φ_s and the spectrometer Φ_{spec} are generally not identical, a contact potential is formed between the sample and the spectrometer (see Fig. 2.7), which leads to the kinetic energy E'_{kin} measured by the spectrometer being different from E_{kin} as defined above. The kinetic energies are related by $E'_{kin} + \Phi_{spec} = E_{kin} + \Phi_s$, so that

$$h\nu = E_B + E'_{kin} + \Phi_{spec}. \tag{2.10}$$

The kinetic energy scale of the spectrometer is then usually shifted either in the software or directly in the electronics so that the work function of the spectrometer Φ_{spec} is eliminated, thus simplifying the determination of the binding energy:

$$E_B = h\nu - E'_{kin}. \tag{2.11}$$

2.4.2. Auger peaks

Auger peaks are a second type of peak that appear in an XPS spectrum in addition to the core level peaks as a result of the atoms being in an excited state after a core electron has been ejected. In the Auger process an excited state of an atom decays radiation-free with the emission of a second electron. An example is illustrated in Fig. 2.8. After a core level electron has been ejected by means of the photoelectric effect, the resulting vacancy in the inner shell is filled by an electron from a shell with a higher energy. The energy that is released is transferred to another electron, which is thereby emitted from the atom. The corresponding Auger peaks are labeled with the shells involved. For the process in the example this would be $KL_{2,3}L_{2,3}$, with the first letter indicating the shell with the initial vacancy, the second letter indicating the shell from which the first electron decays and the third letter indicating the shell from

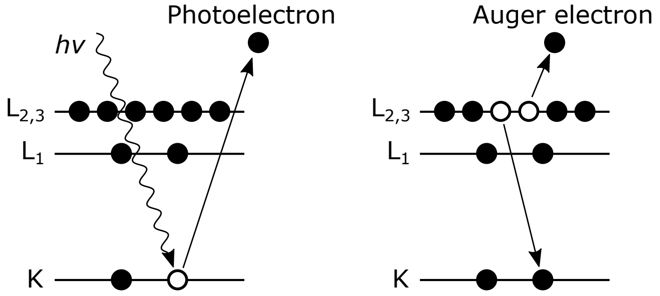

Figure 2.8.: Auger process: After an electron is released by photoemission (left), the vacancy is filled by an electron from a higher energy level, which releases enough energy for a second electron, the Auger electron, to be ejected from the atom (right).

which the second electron, i.e. the Auger electron, is ejected. A V is used for electrons in the valence band.

The kinetic energy of the Auger electron is independent of the energy $h\nu$ of the incident photon, since the photon is not directly involved in the Auger process. Let A, B and C be the energy levels involved (in the example in Fig. 2.8 $A, B, C = K, L_{2,3}, L_{2,3}$) and E_A, E_B and E_C be the corresponding binding energies. Then $E_A - E_B$ is the energy released through the decay, which is transferred to the Auger electron. In the simplest description, the kinetic energy of the Auger electron can thus be approximated as

$$E_{ABC} \approx E_A - E_B - E_C. \tag{2.12}$$

In a more complete picture, which takes into account the interaction of holes in the final state and screening effects, the kinetic energy of the Auger electron is given by [67]

$$E_{ABC} = E_A - E_B - E_C - E_{BC,x} + R_{x,in} + R_{x,ex}, \tag{2.13}$$

where $E_{BC,x}$ is the energy of the interaction of the holes in B and C in the final state x and $R_{x,in}$ and $R_{x,ex}$ are the intra- and extra-atomic relaxation energies.

2.4.3. The XPS spectrum

An XPS overview spectrum of a Ba_2SiO_4 thin film with a thickness of 1 nm on Si(001) is shown in Fig. 2.9 as an example. It was recorded with an Al Kα source. The sharp peaks are due to elastically scattered photoelectrons and can be assigned to a core level of one of the three elements. Silicon has two core level peaks, Si 2s and Si 2p, in the given energy range (They actually originate from the substrate. The intensities of the thin film Si contributions are too low for them to be visible in the plot. See also section 4.8). Furthermore, there is one oxygen peak, the O 1s peak, and several barium peaks. Most of the barium peaks are split into doublet peaks due to the spin–orbit interaction. For example, the Ba 3d peak is split into a Ba $3d_{3/2}$ and a Ba $3d_{5/2}$ peak. In

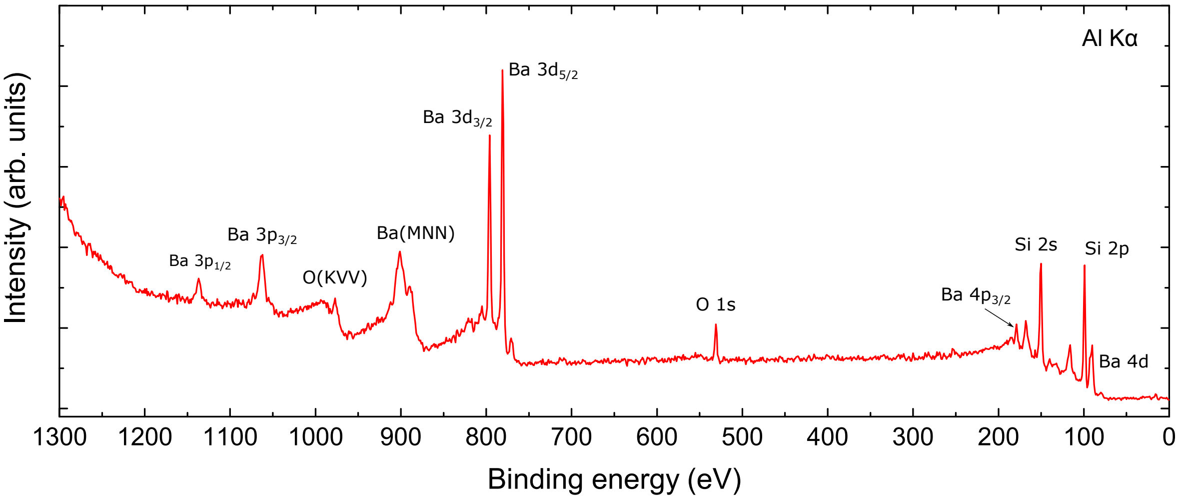

Figure 2.9.: XPS spectrum of a 1 nm thick Ba_2SiO_4 thin film on Si(001)

addition, there are two Auger peaks in the spectrum, the O (KVV) and the Ba (MNN) peaks.

An x-ray source is typically equipped with an Al/Mg dual anode. Their main emission lines are at 1486.6 eV for Al and 1253.6 eV for Mg. The dual anode makes it possible to differentiate between core level peaks and Auger peaks by changing the excitation energy. Since the energy of the Auger electrons is independent of the photon energy, the core level peaks and the Auger peaks shift relative to each other when the excitation energy is changed. In the binding energy scale the core level peaks remain at the same energy, while the Auger peaks are shifted by 233 eV, i.e. the difference between the excitation energies. This seems counterintuitive at first. However, one has to keep in mind that the binding energy is only defined for the core level peaks, and has no meaning with respect to the Auger peaks.

The background of the spectrum is due to inelastically scattered electrons. It increases towards low kinetic energies, i.e. high binding energies. The reason for the large background is that, while the elastic peaks are almost exclusively due to electrons originating from the first few nanometers of the sample because of their short mean free path, the incident x-rays actually have a much higher penetration depth. This leads to a large contribution of inelastically scattered electrons from the lower layers.

2.4.4. Core level peak shapes and shifts

Relaxation shifts

The kinetic energy of the emitted photoelectron according to the equations 2.9 and 2.10 is only correct if Koopman's theorem is fulfilled, which assumes that after the ionization of the atom all other electrons remain in the same state as before the ionization. In reality this is, however, not the case. The main reason for this is the so-called relaxation shift. First, the core hole created by photoemission is screened by core electrons in other states relaxing in energy to lower states, which makes more energy available to the emitted photoelectron. This intra-atomic relaxation shift is represented by an energy E_a [68]

$$E'_{kin} = h\nu - E_B - \Phi_{spec} + E_a. \tag{2.14}$$

Furthermore, the weaker bound valence electrons, which in the case of an atom in a solid are involved in the bond formation with other atoms, will also screen the core hole. This leads to an additional inter-atomic relaxation shift represented by the energy E_r [68]

$$E'_{kin} = h\nu - E_B - \Phi_{spec} + E_a + E_r. \tag{2.15}$$

The relaxation shifts are much smaller than the binding energy. Typically, E_B is several hundred eV while E_a and E_r are only a few eV.

The chemical shift

The chemical shift is an experimentally very important shift of the core level peaks depending on the local chemical and electronic environment of the associated atoms, which allows for a determination of their chemical bonding state. There are two contributions to the chemical shift. First, there is the inter-atomic relaxation shift discussed above, which depends on the neighboring atoms. Second, there is the ‘true chemical shift’, which is a shift of the original binding energy due to the bonds formed to other atoms [68]. The bond formation leads to the electron density in the outer shells either increasing or decreasing. If it decreases, the associated reduction of the effective negative charge around the nucleus results in the core level electrons being bound more tightly, i.e. their binding energy increases, and vice versa. Both contributions are significant for the overall shift and the inter-atomic relaxation shift can even surpass the ‘true chemical shift’ [69]. The ‘true chemical shift’ between the bonding states i and j of an atom is the difference of the respective binding energies [68]

$$\Delta E_B = E_{B,i} - E_{B,j} = E'_{kin,j} - E'_{kin,i}. \tag{2.16}$$

Since XPS measures core level electrons, only the combined effect of all bonds of the atom is measured, i.e. bonds are not measured directly. For example, there is no unique O 1s peak associated with Si-O bonds. Since O-atoms form two bonds, there are different peaks for e.g. Si-O-Si and Si-O-Ba bonding states (see also section 4.1).

Satellite features of core level peaks

There are several satellite features that can accompany a core level peak. Since the emission of a photoelectron is a rapid process, the system does not necessarily reach a stable equilibrium at the point the photoelectron is emitted. One such excited state is the creation of electron-hole pairs around the Fermi level, which reduces the energy of the emitted photoelectron. This leads to satellite peaks, so-called shake-up features, close to the main core level peak at lower kinetic energies, creating an asymmetric peak shape [68]. Another possible excited state is the creation of bulk or surface plasmons, which gives rises to plasmon loss features at lower kinetic energies than the main peak [68]. The plasmon loss satellites have an even lower kinetic energy than the shake-up features, so that they can usually be visually distinguished from the main peak.

Furthermore, there are satellites at higher kinetic energies, due to the source not being completely monochromatic. In addition to the main K$\alpha_{1,2}$ line, the Al and Mg targets also produce several weaker lines resulting from less likely transitions. The positions and intensities relative to the main K$\alpha_{1,2}$ line are listed in table 2.2. The most important ones are in both cases the Kα_3 and Kα_4 lines, which produce the most intense satellite peaks.

	Al		**Mg**	
Line	ΔE (eV)	Intensity (%)	ΔE (eV)	Intensity (%)
$\alpha_{1,2}$	0	100	0	100
α'	5.8	0.7	4.6	1.0
α_3	9.7	7.3	8.5	9.1
α_4	11.7	3.1	10.1	5.1
α_5	20.0	0.41	17.4	0.76
α_6	23.6	0.28	20.6	0.48
β	70.6	0.76	48.6	0.55

Table 2.2.: Relative energies and intensities of the Kα satellites and Kβ bands for Al and Mg [70]

2.4.5. Intensity of core level peaks

The intensity of the core level peak for the state A in the case a laterally homogeneous sample is given by [71]

$$I_A = \kappa \cdot T(E_A) \cdot \sigma_A \int_{z=0}^{\infty} c_A(z) \cdot \exp\left(- \int_{z'=0}^{z} \frac{1}{\lambda(E_A, z') \cos(\vartheta)} \, dz' \right) dz, \tag{2.17}$$

where c_A is the concentration of the Element A, σ_A is the photoionization cross section of the state A, $\lambda(E_A)$ is the mean free path of electrons with the kinetic Energy E_A of the core level peak A in the material the electrons pass through, $T(E_A)$ is the transmission function of the analyzer for electrons with the kinetic energy E_A, ϑ is the angle between the normal of the sample surface and the analyzer, and κ is a device-specific constant.

For single phase samples c_A and $\lambda(E_A)$ can be assumed to be isotropic, so that the equation can be simplified [66]:

$$\begin{aligned}I_A &= \kappa \cdot T(E_A) \cdot \sigma_A \cdot c_A \int_{z=0}^{\infty} \exp\left(-\frac{1}{\lambda(E_A)\cos(\vartheta)} \cdot \int_{z'=0}^{z} 1\,dz'\right) dz \\ &= \kappa \cdot T(E_A) \cdot \sigma_A \cdot c_A \int_{z=0}^{\infty} \exp\left(-\frac{z}{\lambda(E_A)\cos(\vartheta)}\right) dz \\ &= \kappa \cdot T(E_A) \cdot \sigma_A \cdot c_A \cdot \left[-\lambda(E_A)\cos(\vartheta) \cdot \exp\left(-\frac{z}{\lambda(E_A)\cos(\vartheta)}\right)\right]_{z=0}^{\infty} \\ &= \kappa \cdot T(E_A) \cdot \sigma_A \cdot c_A \cdot \lambda(E_A) \cdot \cos(\vartheta) \qquad (2.18)\end{aligned}$$

This means that the sensitivity of the instrument is determined by three factors: The photoionization cross section σ_A, the mean free path $\lambda(E_A)$ and the transmission function $T(E_A)$ of the spectrometer. In order to compare the intensities of different core level peaks, relative sensitivity factors $RSF(A) \propto \sigma_A\,\lambda(E_A)\,T(E_A)$ are defined so that

$$c_A \propto \frac{I_A}{\sigma_A \cdot \lambda(E_A) \cdot T(E_A)} \propto \frac{I_A}{RSF(A)}\,. \qquad (2.19)$$

Usually the relative sensitivity factors are defined so that either $RSF(F\,1s) = 1$ or $RSF(C\,1s) = 1$. The RSFs can be used to determine relative intensities of the elements in the sample. The accuracy of this method greatly depends on the accuracy with which $\lambda(E_A)$ is known. The mean free path $\lambda(E_A)$ is usually assumed to be a universal function [58]. However, there can be rather large deviations from the universal function, especially for complex oxides like Ba_2SiO_4.

2.4.6. Determination of the layer thickness

The thickness of a thin film can be determined with XPS by measuring the damping of a substrate peak. For a homogeneous layer with thickness d this damping of the substrate peak intensity is given by [67]

$$I_{sub}(d) = I_{sub}(0) \cdot \exp\left(-\frac{d}{\lambda(E) \cdot \cos(\vartheta)}\right), \qquad (2.20)$$

where $I_{sub}(d)$ is the intensity of the substrate peak with the thin film and $I_{sub}(0)$ is the intensity of the same substrate peak but without the thin film both measured under identical conditions, $\lambda(E)$ is the mean free path of electrons in the thin film at the kinetic energy of the substrate peak and ϑ is the angle between the sample surface normal and the analyzer. Thus, by measuring $I_{sub}(d)$ and $I_{sub}(0)$ the film thickness can be determined via

$$d = \lambda(E) \cdot \cos(\vartheta) \cdot \ln\left(\frac{I_{sub}(0)}{I_{sub}(d)}\right). \qquad (2.21)$$

Since this method requires the substrate to be visible in XPS, it only works for film thicknesses of up to approximately 10 nm. Ideally, $I_{sub}(d)$ should be determined for several thicknesses with known ratios in order to increase the accuracy of the method.

The mean free path can be looked up in the NIST Electron Inelastic-Mean-Free-Path Database [72].

2.5. Underlying theory of the electrical characterization

2.5.1. The different regions of a MOS capacitor and the CV-curve

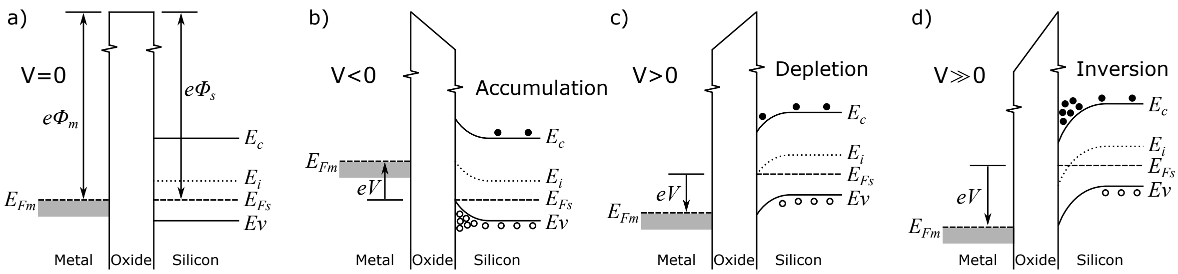

Figure 2.10.: Band diagrams of a metal oxide semiconductor (MOS) capacitor with a p-type semiconductor: (a) Equilibrium state for the case that the work functions of the metal and the semiconductor are identical. If a voltage is applied, three regions can be distinguished: (b) accumulation, (c) depletion and (d) inversion. Based on [73, 26].

The band diagram of a MOS capacitor for the example of p-type silicon is shown in Fig. 2.10a). In the context of a MOS capacitor it is convenient to define modified work functions Φ_m and Φ_s, whose energies are measured from the Fermi level to the conduction band of the oxide as shown in the figure [73]. In this idealized example the work functions of the metal and the semiconductor are the same, so that there is no band bending of the semiconductor bands in the equilibrium state.

The MOS structure works essentially like plate capacitor, where one plate is replaced by a semiconductor. By applying a voltage to the metal, charge is deposited on the metal, which induces an equal charge of opposite sign in the semiconductor. Three main regions can be distinguished, which are discussed in the following for the example of a p-type semiconductor. If the voltage applied to the metal is negative, the band edges of the semiconductor bend upwards at the interface to the oxide, which leads to a hole accumulation near the interface (Fig. 2.10b)) [73]. This voltage region, where the density of the majority carriers is increased near the interface, is called *accumulation*. Since (in the ideal case) no current flows through the oxide, the Fermi level of the semiconductor remains straight. If a small positive voltage is applied, the bands of the semiconductor bend downward, leading to a depletion of the majority carriers (Fig. 2.10c)) [73]. Hence, this region is called *depletion*. When the positive voltage is increased further, the intrinsic level E_i eventually crossed the Fermi level of the semiconductor E_{Fs} (Fig. 2.10d)). At this point the minority carrier density (electrons) at the interface is larger than the majority carrier density (holes), i.e. the interface is inverted [73]. This region is called *inversion*.

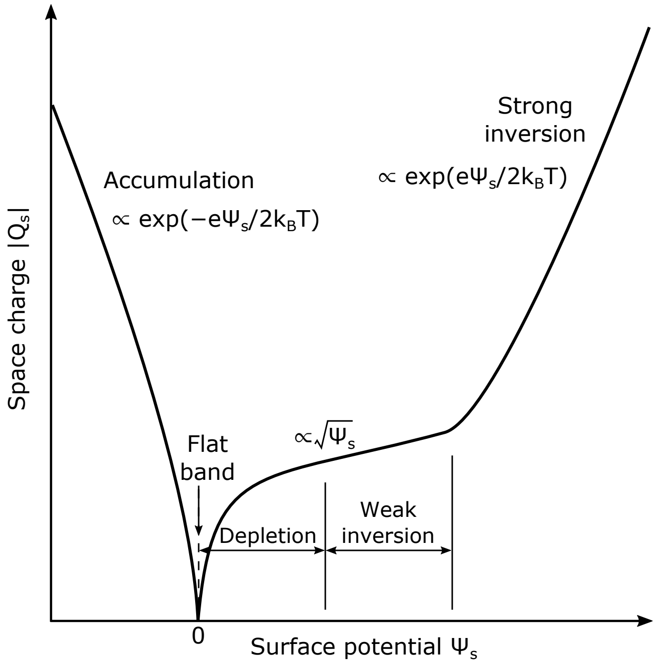

Figure 2.11.: Space charge at the semiconductor-oxide interface in a MOS capacitor versus the surface potential for p-type silicon. [26, 74]

For an n-type semiconductor the bands bend in same direction. However, since the majority carriers are electrons instead of holes, accumulation occurs at positive voltages, while depletion and inversion occur at negative voltages. Moreover, if the work functions of the metal and the semiconductor are not the same, the voltage at which the semiconductor bands are not bend, and thus the voltage at which the transition between accumulation and depletion happens, is different from zero. This voltage is called the flat band voltage V_{fb}. In the idealized case that there is no additional charge in the oxide or at the oxide-semiconductor interface, it is equal to the difference in the work functions [73]

$$V_{fb} = \Phi_m - \Phi_s. \tag{2.22}$$

The capacitance of a MOS structure is the series connection of a voltage-independent conductance due to the oxide C_{ox} and a voltage-dependent conductance due to the space charge at the semiconductor surface C_s, which is given by the change of the space charge Q_s with the surface potential Ψ_s [73]

$$C_s = \frac{dQ_s}{d\Psi_s}. \tag{2.23}$$

Fig. 2.11 shows the dependence of the space charge for a p-type substrate on the surface potential, which is related to the voltage V_g applied to the metal gate by $\Psi_s = V_g - V_{fb}$. The space charge is zero at the flat band condition. In the accumulation region it depends exponentially on the surface potential. In depletion and weak inversion, the

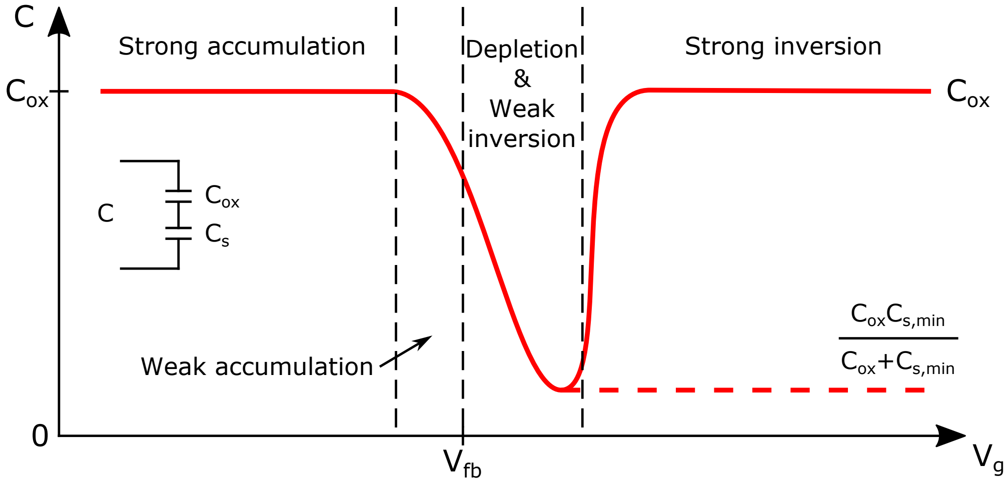

Figure 2.12.: Capacitance-gate voltage curve for a MOS capacitor with a p-type semiconductor substrate. The dashed red line is observed at high measurement frequencies. Based on [73].

surface charge is dominated by ionized dopants, so that it changes with the square root of the surface potential. Finally, in the strong inversion region it becomes exponentially dependent on the surface potential again. In the regions where the space charge depends exponentially on the surface potential the semiconductor capacitance C_s becomes very large, so that the overall capacitance of the MOS structure becomes basically equal to the oxide capacitance C_{ox} in strong accumulation and strong inversion [73] as seen in Fig. 2.12. However, if the measurement frequency is so high that the generation and recombination of the minority carriers in the inversion layer cannot follow the voltage changes, the measured conductance in the strong inversion region remains dominated by the contribution of ionized dopants (dashed red line in Fig. 2.12). In-between these two extremes the capacitance of the MOS structure changes as shown in the figure due to the variation of the semiconductor capacitance with the gate voltage. For n-type substrates the CV-curve is mirrored at the $V_g = V_{fb}$ line.

Furthermore, the CV-curve is influenced by charges in the oxide. Charge either in the oxide bulk or at the interface to the semiconductor induces a charge of opposite sign in the semiconductor, which leads to a shift in the flat band voltage and thereby in the CV-curve. Positive charge in the oxide shifts the flat band voltage towards negative voltages, while negative charge in the oxide shifts it towards positive voltages (see Fig. 2.13a)). For a charge Q_i at the interface to the semiconductor and a charge density ρ_{ox} distributed in the oxide, equation 2.22 changes to [25]

$$V_{fb} = \Phi_m - \Phi_s - \frac{Q_i}{C_{ox}} - \frac{1}{C_{ox}d}\int_0^d x\rho_{ox}(x)\,dx, \tag{2.24}$$

where C_{ox} is the oxide capacitance and d is the thickness of the oxide. Moreover, if interface trap states are present, they have to be charged in addition to the space charge layer, which leads to a stretch-out of the CV-curve as shown in Fig. 2.13b).

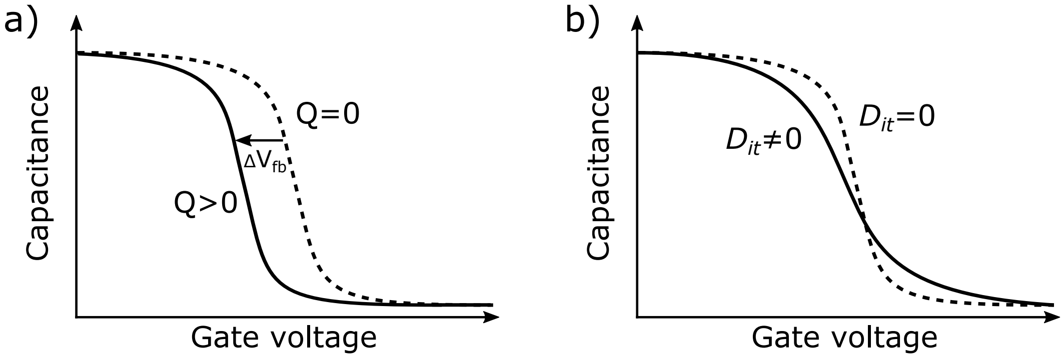

Figure 2.13.: Effect of oxide charges on the CV-curve: (a) Charge in the oxide or at the interface to the semiconductor shifts the CV-curve. Positive oxide charge shifts it towards negative gate voltages and vice versa. (b) Interface trap states lead to a stretch-out of the CV-curve. Based on [75].

2.5.2. Three-element model and correction for series resistance

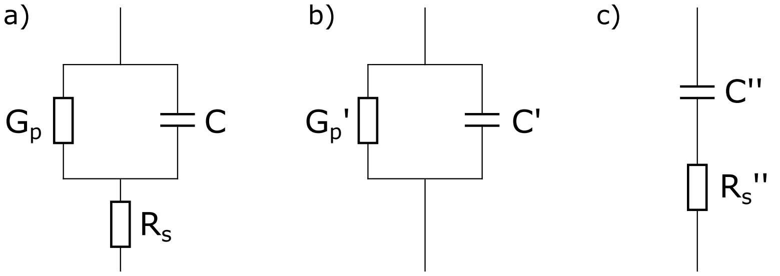

Figure 2.14.: Equivalent circuit diagrams for (a) the three-element model, (b) a two-element model with a conductance and a capacitance connected in parallel and (c) a two-element model with a conductance and a resistance connected in series.

The three-element model, whose equivalent circuit diagram is shown in Fig. 2.14a), is a model for the measurement of the capacitance of an insulator thin film, that takes the simultaneous presence of the conductance through the oxide due to leakage G_p and a series resistance R_s, which represents the resistance due to the spreading resistance in the silicon wafer [76] and the contact resistances, to which the resistance between the wafer backside and the chuck makes generally the greatest contribution, into account. Its use becomes necessary for the capacitance measurement of a thin oxide layer with high leakage currents, since the high frequency of the alternating voltage used to minimize the influence of the leakage current results in an increased contribution of the series resistance due to the low impedance of the capacitor. Disregarding the series resistance unjustifiably would lead to a dependency of the accumulation capacitance of the CV-curve on the measurement frequency, making an accurate determination of the accumulation capacitance impossible [77].

The measurement at a single frequency, however, only gives an unambiguous result for a two-element model, i.e. a model with a capacitance and a conductance connected in parallel (see Fig. 2.14b)) or one with a capacitance and a resistance in series (see Fig. 2.14c)) [77]. Therefore, the CV-curves are initially measured assuming only a two-element model with a parallel conductance as shown in Fig. 2.14b) (see section 3.3.3) and then corrected for the series resistance afterwards. For this correction, a frequency dependent ($10^2 - 10^6$ Hz) measurement of the absolute value $|Z|$ and the phase ϕ of the impedance is done at a fixed voltage in strong accumulation, since in this regime the contribution of substrate and interface traps can be ignored and the series resistance has the largest effect.

Determination of the series resistance: The impedance Z of the three element model is given by the parallel connection of the impedances of the conductance $Z_1 = G_p^{-1}$ and the capacitance $Z_2 = (i\omega C)^{-1}$, which is connected in series with $Z_3 = R_s$:

$$\begin{aligned} Z &= \left(Z_1^{-1} + Z_2^{-1}\right)^{-1} + Z_3 \\ &= (G_p + i\omega C)^{-1} + R_s \\ &= \frac{G_p - i\omega C}{G_p^2 + \omega^2 C^2} + R_s \qquad (2.25) \\ &= R_s + \frac{G_p}{G_p^2 + \omega^2 C^2} + i\frac{-\omega C}{G_p^2 + \omega^2 C^2}, \qquad (2.26) \end{aligned}$$

where $\omega = 2\pi f$ is the corresponding angular frequency of the measurement frequency f. Equation 2.26 can then be used to determine expressions for the absolute value $|Z|$ and the phase ϕ of the impedance:

$$|Z| = \left[\left(R_s + \frac{G_p}{G_p^2 + \omega^2 C^2}\right)^2 + \left(\frac{-\omega C}{G_p^2 + \omega^2 C^2}\right)^2\right]^{1/2} = \left[R_s^2 + \frac{2R_sG_p + 1}{G_p^2 + \omega^2 C^2}\right]^{1/2} \qquad (2.27)$$

$$\phi = \arctan\left(\frac{\frac{-\omega C}{G_p^2+\omega^2 C^2}}{R_s + \frac{G_p}{G_p^2+\omega^2 C^2}}\right) = -\arctan\left(\frac{\omega C}{R_s(G_p^2 + \omega^2 C^2) + G_p}\right) \qquad (2.28)$$

In order to determine the series resistance R_s, the equations 2.27 and 2.28 are then used to simultaneously fit the frequency dependent measurements of $|Z|$ and ϕ performed in strong accumulation with one parameter set, where G_p, C and R_s are fitting parameters. This fitting process and the subsequent correction of the $C(V)$ and $G_p(V)$ measurements was done using a Maple software developed at the Institut für Materialien und Bauelemente der Elektronik of the Leibniz Universität Hannover [78]. Starting values for the fit are extracted from the measurement of $C(V)$ and $G_p(V)$ based on the two-element parallel model. In particular, a starting value for the series resistance is determined from

$$R_s = \frac{G_{m,acc}}{G_{m,acc}^2 + \omega^2 C_{m,acc}^2}, \tag{2.29}$$

where $C_{m,acc}$ and $G_{m,acc}$ are the measured values of C and G in accumulation based on the two-element parallel model. This expression is determined by comparing the impedance of the two-element series model (Fig. 2.14c)) with the impedance of the two-element parallel model (Fig. 2.14b)) under the assumption that the capacitances in both models are identical [79]. Therefore, it is not very accurate and may have to be adjusted if the fit does not converge.

Correction for series resistance: Analogous to the determination of equation 2.25, the impedance of the two-element model with a conductance and a capacitance connected in parallel as shown in Fig. 2.14b) is given by

$$Z' = \frac{G_m - i\omega C_m}{G_m^2 + \omega^2 C_m^2}, \tag{2.30}$$

with $C_m = C'$ and $G_m = G_p'$. The m emphasizes that these are the measured values of the capacitance and the conductance (see also section 3.3.3). Equating the real parts as well as the imaginary parts of the equations 2.25 and 2.30 and solving the resulting system of linear equations, gives the following expressions for the capacitance $C_{corr} = C$ and the conductance $G_{p,corr} = G_p$ in the three-element model [79]

$$C_{corr} = \frac{(G_m^2 + \omega^2 C_m^2) C_m}{a^2 + \omega^2 C_m^2} \tag{2.31}$$

$$G_{p,corr} = \frac{(G_m^2 + \omega^2 C_m^2) a}{a^2 + \omega^2 C_m^2} \tag{2.32}$$

with

$$a = G_m - (G_m^2 + \omega^2 C_m^2) R_s. \tag{2.33}$$

These equations are then used to correct the measured values C_m and G_m for the series resistance.

2.5.3. Determination of the flat band voltage from the CV-curve

There are many methods to determine the flat band voltage from a measured CV-curve [80, 81, 82, 83]. In this work two methods are used, the flat band capacitance method and the inflection point method.

Flat band capacitance method: In this method the flat band capacitance is first determined and with it the flat band voltage is read from the CV-curve (after correction for series resistance). The flat band capacitance C_{fb} is given by the series connection of the oxide capacitance C_{ox} and the semiconductor capacitance at the flat band voltage

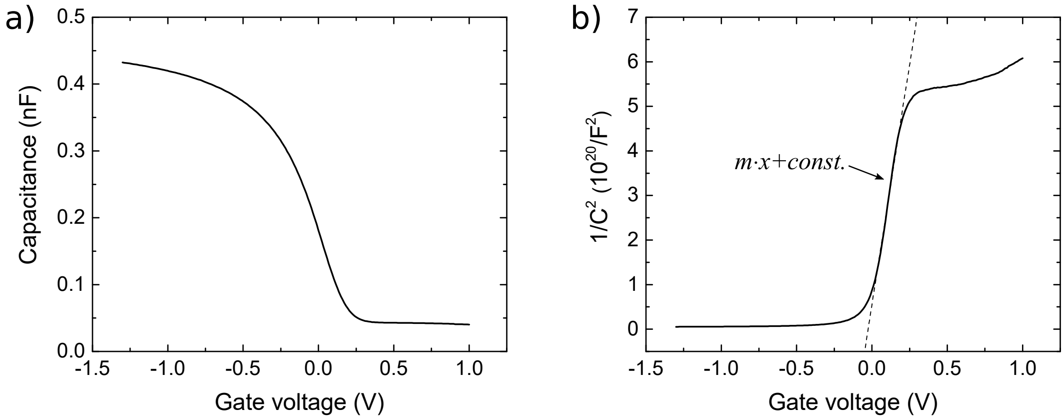

Figure 2.15.: Determination of the semiconductor capacitance at the flat band condition: (a) CV-curve after correction for series resistance and (b) the corresponding $1/C^2$-characteristic. The semiconductor capacitance at the flat band condition can be determined from the slope m of the linear part of the $1/C^2$-curve (dashed line).

$C_{s,fb}$ (see also section 2.5.1):

$$C_{fb} = \frac{C_{ox} C_{s,fb}}{C_{ox} + C_{s,fb}}. \tag{2.34}$$

The oxide capacitance C_{ox} is determined from the CV-curve in strong accumulation. The semiconductor capacitance at the flat band voltage $C_{s,fb}$ is given by [81]

$$C_{s,fb} = \varepsilon_0 \varepsilon_s \frac{A}{L_D}, \tag{2.35}$$

where ε_0 is the vacuum permittivity, ε_s is the dielectric constant of the semiconductor, A is the active area of the capacitor and L_D is the Debey length, which is given by [81]

$$L_D = \sqrt{\frac{k_B T \varepsilon_0 \varepsilon_s}{e^2 N_D}}, \tag{2.36}$$

where k_B is the Boltzmann constant, T is the temperature, e is the elementary charge and N_D is the doping concentration, which can be calculated via [81]

$$N_D = \frac{2}{e\, \varepsilon_0 \varepsilon_s} \cdot (|m| \cdot A^2)^{-1}, \tag{2.37}$$

where m is the slope of the linear part of the $1/C^2(V_g)$ characteristic of the measured CV-curve (units: $\mathrm{F}^{-2}\mathrm{V}^{-1}$, see Fig. 2.15). Thus, the semiconductor capacitance at the flat band voltage $C_{s,fb}$ can be determined via

$$C_{s,fb} = \sqrt{\frac{2e}{k_B T\, |m|}}. \tag{2.38}$$

This means that only C_{ox} and m need to be determined from the CV-curve in order to determine C_{fb}, which can then be used to read the flat band voltage V_{fb} from the CV-curve.

However, so far the effect of charged interface traps has not been taken into account, which leads to an error in the calculated flat band voltage if the interface trap density is larger than 10^{10} eV^{-1}cm^{-2}. With the knowledge of the interface trap density the shift of the flat band voltage due to charged interface traps can be determined via [80]

$$\Delta V_{fb} = \frac{eD_{it}}{C_{ox}} \left(e\phi_B + \frac{E_g}{2} \right), \tag{2.39}$$

where e is the elementary charge, $e\phi_B$ is the energy distance of the Fermi level from midgap in the semiconductor bulk, E_g is the semiconductor band gap and D_{it} is the interface trap density at the corrected flat band voltage. This shift of the flat band voltage is negative for donor type interface traps and positive for acceptor type interface traps. This means that the type of the interface traps has to be known in order to apply the correction. Moreover, since the exact flat band voltage is not known beforehand and the interface trap density needs to be known at the corrected flat band voltage, the calculation of the shift is an iterative process that requires the measurement of the interface trap density for multiple voltages from weak accumulation to depletion.

Inflection point method: The inflection point method was proposed by Winter *et al.* [82]. In this method it is assumed that the point of inflection of the CV-curve, i.e. the point where the first derivative assumes its maximum and where the second derivative intersects the voltage axis, corresponds to the flat band voltage. Winter *et al.* have shown that the voltage at the inflection point coincides with the flat band voltage as determined with the flat band capacitance method for various samples. However, the inflection point method is, at least at this point, an empirical method with no physical theory behind it that explains why the inflection point should correspond to the flat band voltage. Nevertheless, it has the advantage that it does not require the knowledge of any parameters and can be used for capacitors with high interface trap densities without the need for a correction. Especially for capacitors with high interface trap densities it gives better estimates than for example the $1/C^2$-method [83], which for high interface trap densities gives estimates closer to midgap than the actual flat band voltage.

Since the correction for the interface trap density is very time-consuming, the inflection point method is used in this work to determine the flat band voltage for all capacitors, while the flat band capacitance method is only used for selected capacitors in order to get an idea of the deviation between the two methods. The inflection point is determined from the maximum of the first derivative of the CV-curve after correction for series resistance.

2.5.4. Determination of the interface trap density with the conductance method

The conductance method is a technique to determine the density of trap states at the interface between the gate insulator and the silicon substrate from a measurement of the parallel conductance of a MOS capacitor. An alternating voltage is used to charge and discharge the trap states. If the frequency of this alternating voltage is equal to the characteristic frequency of the interface trap states, the interface trap density D_{it} as a function of the gate voltage can be determined from the resulting conductance. The conductance method is considered one of the most accurate methods for the determination of the interface trap density. In contrast, the capacitance method, which is based on the measurement of the capacitance associated with the interface traps [84], has among other limitations [85] the problem that the capacitance of the interface traps is orders of magnitude smaller than the other capacitances involved, making a precise measurement difficult.

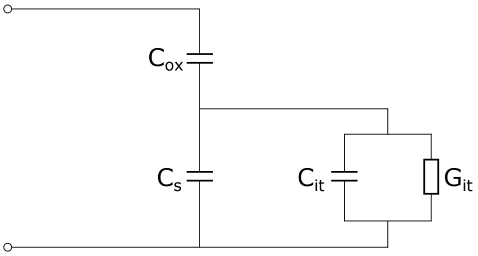

Figure 2.16.: Equivalent circuit for the conductance method. C_{ox} is the capacitance of the oxide layer, C_s is the silicon capacitance, C_{it} is the capacitance of the interface traps and G_{it} is the interface trap conductance. [80]

The method for the determination of the interface trap density described in the following is valid in depletion. In this region the MOS capacitor can be described by the equivalent circuit diagram shown in Fig. 2.16, where C_{ox} is the capacitance of the oxide layer, C_s is the silicon capacitance, C_{it} is the capacitance of the interface traps and G_{it} is the interface trap conductance, which is related to the measured conductance and capacitance values by [80]

$$\frac{G_{it}}{\omega} = \frac{\omega\, C_{ox}^2 G_{p,corr}}{G_{p,corr}^2 + \omega^2 (C_{ox} - C_{corr})^2}, \tag{2.40}$$

where $\omega = 2\pi f$ is the corresponding angular frequency of the measurement frequency f and $G_{p,corr}$ and C_{corr} are the corrected values of the measured conductance and capacitance according to equations 2.32 and 2.31. In contrast to the original source, which uses the directly measured values G_m and C_m (see also section 3.3.3), the values corrected for series resistance are used in this work in order to take the substrate and contact resistances into account, which cannot be neglected for the samples investigated. The oxide capacitance C_{ox} is the capacitance value of the CV-curve in strong accumulation after correction for series resistance.

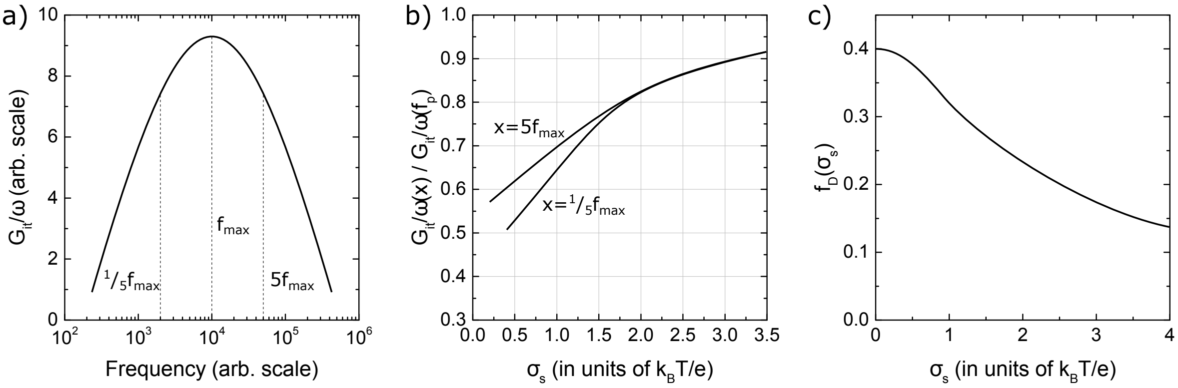

Figure 2.17.: Determination of the correction factor f_D: (a) Illustration of a representative $G_{it}/\omega(\omega)$ curve. (b) Ratio $^{G_{it}/\omega(x)}/_{G_{it}/\omega(f_{max})}$ for $x = ^1/_5 f_{max}$ and $x = 5f_{max}$ versus the standard deviation of band-bending σ_s. (c) Correction factor f_D versus σ_s. First the ratio $^{G_{it}/\omega(x)}/_{G_{it}/\omega(f_{max})}$ for either $x = ^1/_5 f_{max}$ or $x = 5f_{max}$ has to be determined from the measured $G_{it}/\omega(\omega)$ curve. Then σ_s is determined from b). Finally, f_D is determined from c). [86, 87]

The ratio G_{it}/ω peaks as a function of frequency and from its maximum value the interface trap density can be determined via [80]

$$D_{it} = \frac{\left(^{G_{it}}/_{\omega}\right)_{max}}{e \cdot f_D \cdot A}, \tag{2.41}$$

where e is the elementary charge, A is the active area of the capacitor* and f_D is a correction factor, that accounts for variations of the band-bending over the active area of the capacitor, which results in a broadening of the $G_{it}/\omega(\omega)$ function and a reduction of its maximum value. The correction factor f_D is 0.4, if there are no fluctuations in the band-bending over the active area of the capacitor, and it decreases with an increasing variance of the band-bending σ_s^2. In order to determine f_D, the maximum value of G_{it}/ω and either the value at five times or one fifth of the frequency of the maximum have to be determined first (see Fig 2.17a)). With these the standard deviation of the band-bending σ_s can be determined from Fig 2.17b). Finally, f_D can be determined from Fig 2.17c).

It is important to use G_{it}/ω as determined by equation 2.40, which represents a correction of the parallel conductance for the oxide capacitance C_{ox}, for the determination of the interface trap density, since using G_m/ω or $G_{p,corr}/\omega$ directly would lead to an underestimation of D_{it} [80].

Since the frequency at which G_{it}/ω assumes its maximum is not known beforehand, the conductance and the capacitance have to be measured in dependence of the frequency ($f = 10^2 - 10^6$ Hz) at a fixed gate voltage. In addition, a CV-curve (corrected for

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*The division by the area in equation 2.41 has to be omitted if the initial conductance and capacitance values used to determine G_{it}/ω are already given per unit area.

series resistance) is needed to determine the capacitance of the oxide layer as well as the frequency range of the depletion region. In order to determine the distribution of the interface trap density in the band gap, the frequency dependent measurements are done at several gate voltages from flat band to midgap. In this way, the distribution of the interface trap density in the lower half of the silicon band gap can be determined if the substrate is p-type, and it can be determined in the upper half if the substrate is n-type.

The model presented in this section ascribes the conductivity completely to the interface traps, i.e. leakage through the oxide is not accounted for. A leakage current through the oxide contributes to the measured conductance mainly at low frequencies, which results in an apparent increase of the G_{it}/ω curve towards low frequencies. In the extreme case the G_{it}/ω curve does not peak but simply increases towards low frequencies inhibiting an extraction of the interface trap density. This is the case for some of the capacitors investigated in this work. Hence, no interface trap density is determined for these capacitors. However, the majority of the capacitors show a clear maximum and there is no significant difference in the derived interface trap densities for capacitors on the same sample, whose dc leakage current differs by several orders of magnitude (see section 5.5), so that the model presented here can still be used for the samples investigated.

2.5.5. Conduction mechanisms through thin oxide layers

In real MOS capacitors there can still be a non-zero current flow through the insulator, especially at high electric fields or high temperatures. The relevant conduction mechanisms will be discussed in the following.

In the *direct tunneling* process an electron simply tunnels through the oxide barrier as shown in Fig. 2.18a). This is a consequence of the electron wave function penetrating the oxide barrier, so that there is a finite probability that the electron appears on the other side of the barrier. The tunneling probability and thus the tunneling current are proportional to $\exp(-2\beta d)$, where d is the oxide thickness and $\beta \propto \{[E_1 + (E_2 - eV)]/2\}^{1/2}$ [25]. E_1 and E_2 are the barrier heights as defined in Fig. 2.18a) and V is the applied voltage. The average barrier height is $[E_1 + (E_2 - eV)]/2$. When V is increased, β decreases and the tunneling probability increases exponentially. Thus, the tunneling probability depends strongly on the applied voltage, but is essentially independent of the temperature. If the applied voltage is so high that the conduction band edge of the oxide on the side of the semiconductor is lower than the Fermi level of the metal as depicted in Fig. 2.18b), the barrier becomes triangular, which decreases the average barrier height and the tunneling distance as compared to the direct tunneling process [25]. This process, where the electron only tunnels through the partial width of the barrier, is called *Fowler-Nordheim tunneling.*

In the *Schottky emission* process the electron possesses enough energy to overcome the oxide barrier as illustrated in Fig. 2.18c). The resulting current depends exponentially on the temperature. The leakage current density J can be described by [26]

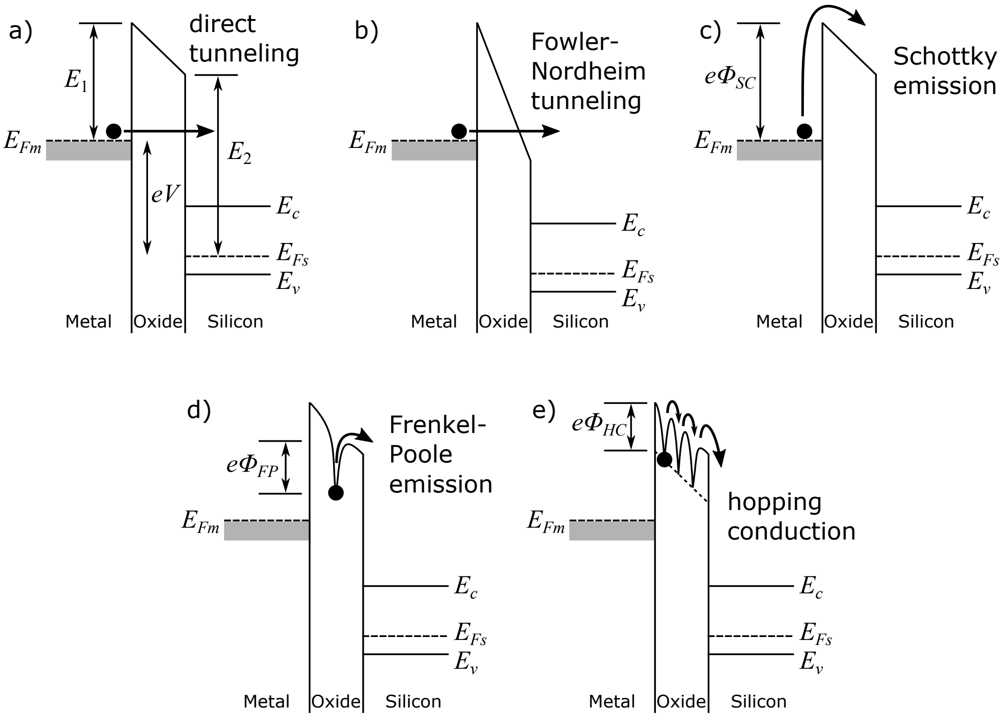


Figure 2.18.: Leakage current mechanisms through thin insulators: (a) Direct tunneling, (b) Fowler-Nordheim tunneling, (c) Schottky emission, (d) Frenkel-Poole emission and (e) hopping conduction. Based on [25, 26].

$$J = A^{**}T^2 \exp\left(-\frac{e\left(\Phi_{SC} - \sqrt{e\mathcal{E}/4\pi\varepsilon_{ox}}\right)}{k_BT}\right) \propto T^2 \exp\left(\frac{e(a\sqrt{V} - \Phi_{SC})}{k_BT}\right), \qquad (2.42)$$

where A^{**} is the effective Richardson constant, $e\Phi_{SC}$ is the barrier height, $\mathcal{E}$ is the electric field in the oxide, ε_{ox} is the oxide permittivity, k_B is the Boltzmann constant, T is the temperature and a is a constant.

The *Frenkel-Poole emission* is the emission of an electron from a trap state in the oxide band gap into the conduction band of the oxide through thermal excitation as illustrated in Fig. 2.18d). For trap states with Coulomb potentials the resulting current density can be described by [26]

$$J \propto \mathcal{E} \exp\left(-\frac{e\left(\Phi_{FP} - \sqrt{e\mathcal{E}/\pi\varepsilon_{ox}}\right)}{k_BT}\right) \propto V \exp\left(\frac{e(2a\sqrt{V} - \Phi_{FP})}{k_BT}\right), \qquad (2.43)$$

where $e\Phi_{FP}$ is the depth of the trap state as shown in Fig. 2.18d) and a is the same constant as in equation 2.42. The exponential dependency is similar to that of the Schottky emission with the difference that, in addition to the barrier height being different, the barrier lowering by the electric field is also larger by a factor of 2 ($2a\sqrt{V}$ instead of $a\sqrt{V}$) [26].

The *hopping conduction* is a trap assisted process, in which an electron consecutively hops from one defect state in the oxide to the next by thermal excitation as illustrated in Fig. 2.18e). The current density has on ohmic characteristic, which depends exponentially on the temperature [26]

$$J \propto \mathcal{E} \exp\left(-\frac{e\Phi_{HC}}{k_B T}\right), \tag{2.44}$$

where $e\Phi_{HC}$ is the activation energy of the electrons.

3. Experimental

3.1. Experimental setup

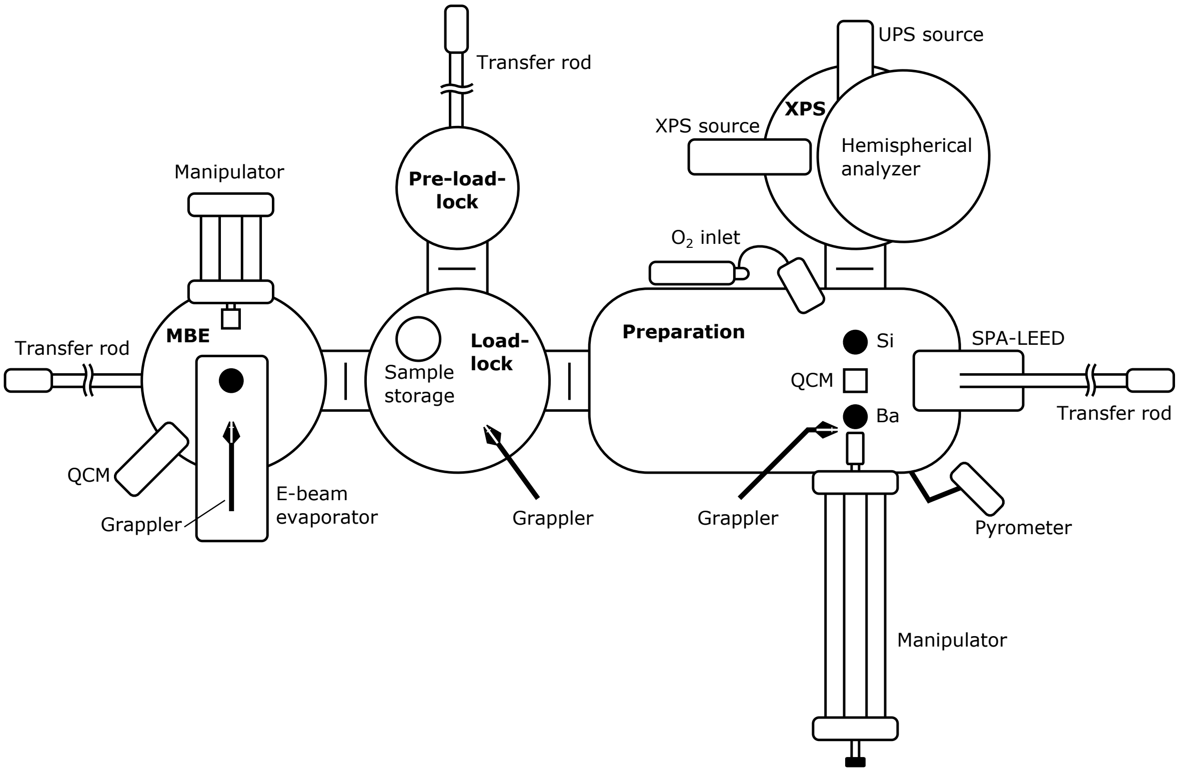


Figure 3.1.: Layout of the UHV chamber used to grow the epitaxial Ba_2SiO_4 films.

The epitaxial Ba_2SiO_4 films are grown in an ultra-high vacuum (UHV) chamber with a base pressure of $7 \cdot 10^{-11}$ torr. It is equipped with a SPA-LEED and an XPS, which are used for the in-situ structural characterization of the Ba_2SiO_4 films. The UHV is the precondition for the epitaxial film growth since it ensures that the silicon substrate surface stays clean long enough for the film to be deposited without losing the crystalline template due to the adsorption of residual gas particles. The UHV chamber is separated by plate valves into five parts: The preparation chamber, the XPS chamber, the MBE chamber, the load-lock and the pre-load-lock (see Fig. 3.1). The samples can be moved between the different parts by transfer rods. Wobble sticks equipped with grapplers are used to move the sample holders between the transfer rods and the manipulators respectively the storage place. The samples are introduced into the vacuum in the pre-load-lock ($p = 1 \cdot 10^{-7}$ torr). This is the only part that is regularly vented outside of maintenance. From here the samples are transferred to the load-lock ($p = 7 \cdot 10^{-11}$ torr), where up to eight sample holders can be stored. The load-lock is also connected to the preparation chamber and the MBE chamber.

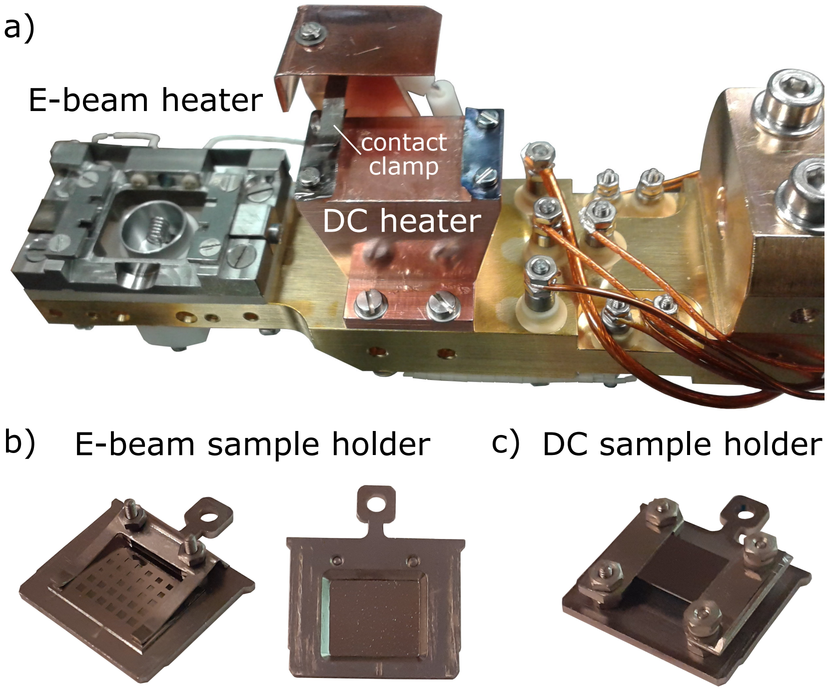


Figure 3.2.: Sample heaters in the preparation chamber: (a) Manipulator head with an e-beam sample heater (left) and a direct current heater (right). (b) Sample holder for the e-beam heater with a hole in the back. Left: top view. Right: bottom view. (c) Sample holder for the direct current heater. The support on the right side in insulated from the rest of the holder.

In the preparation chamber ($p = 7 \cdot 10^{-11}$ torr) the Ba_2SiO_4 films are grown. For this purpose, it is equipped with Ba and Si e-beam evaporators and an oxygen inlet. In total up to five evaporators can be installed. In order to measure the evaporation rates, there is a quartz crystal microbalance (QCM, 6 MHz), which can be moved in the sample position. The substrate temperature is measured by a pyrometer using the emissivity for silicon. Furthermore, a SPA-LEED is installed in the preparation chamber, which is used to analyze the surface morphology. The manipulator, where the sample holders are placed, is equipped with micrometer screws that allow an exact positioning of the sample. It can be cooled with ℓN_2 (and in principle also with ℓHe, but it was not used in this work). The manipulator head is shown in Fig. 3.2a). There are two different sample heaters. On the right is a direct current heater. The corresponding sample holder needed to use the direct current heater is shown in Fig. 3.2c). The silicon substrates ($6 \times 14\ \mathrm{mm}^2$) are clamped on both sides between a metal plate and a metal sheet. On one side the metal plate and sheet are insulated from the rest of the sample holder by ceramic washers. The other side is grounded. The insulated side gets connected to the clamp on the manipulator, which is also insulated from the rest of the manipulator and connected to the outside by an electrical feedthrough. This allows for a current to be sent through the sample and thereby heating it by resistive heating.

However, in order to deposit the gate contacts on the samples used for the electrical measurements a metallic shadow mask is placed on the substrate (see section 3.2), so that the direct current heating cannot be used. Therefore, an e-beam sample heater, which is commercially available from the company VAb Vakuum-Anlagenbau, was also installed (left side of Fig. 3.2a)). The working principle is that electrons are emitted from a heated filament by thermionic emission and accelerated onto the sample, which is put at high voltage of 1 to 2 kV depending on the desired temperature. During the use of the e-beam heater the manipulator has to be cooled with ℓN_2 to protect the wiring. The sample holder used for the e-beam heater, which is self-made, is shown in Fig. 3.2b). It has a hole in the back, so that the accelerated electrons hit the substrate directly. In this way only the substrate is heated to high temperatures. The sample holder remains cold enough so that it does not emit visible thermal radiation, even when the substrate is heated to 1000 °C. Thus, the pressure during the flash annealing remains relatively low. If done correctly, the substrate can be flash annealed to $950 - 1000\,°\mathrm{C}$ without the pressure exceeding $5 \cdot 10^{-10}$ torr. In combination with the metallic shadow mask placed on the substrate, a relatively even temperature distribution is achieved. The temperature difference between the hottest part directly above the filament and the exposed part of the substrate furthest away from the filament is approximately 20 °C at a substrate temperature of 680 °C.

With the manipulator of the preparation chamber the sample can be moved all the way into the XPS chamber for the analysis of its chemical composition. The XPS system is from the company SPECS and consists of a Phoibos 100 spectrometer (100 mm radius) equipped with an MCD-5 detector and a non-monochromatized x-ray source with an Al/Mg twin anode. The angle between the x-ray source and the analyzer is 54°. Furthermore, the MBE chamber is equipped with a large e-beam evaporator and a quartz crystal microbalance (QCM) to measure the film thickness. The large e-beam evaporator is used to grow films with thicknesses of several 100 nm. It has five crucibles, which are filled with different materials, that can be switched without breaking the vacuum. In this work, it is used to deposit the Au gate contact of the capacitors for the electrical measurements (see section 3.2).

3.1.1. The Ba and Si evaporators

E-beam evaporators are used to evaporate Ba and Si. Ba is evaporated from a crucible and Si is evaporated from a rod. The evaporation from a rod has the advantage that there cannot be any contamination from the crucible. However, it is only possible if the vapor pressure of the material is low enough so that it directly evaporates from the solid phase. While a commercially available e-beam evaporator from the company Tectra is used for Si, the Ba evaporator was built in-house in the workshop of the Institut für Festkörperphysik of the Leibniz Universität Hannover. Nevertheless, the working principle, which is illustrated in Fig. 3.3, is the same. Electrons are emitted from a heated filament by thermionic emission and accelerated onto the crucible/rod by applying a positive high voltage to the crucible/rod. A water-cooled shield helps

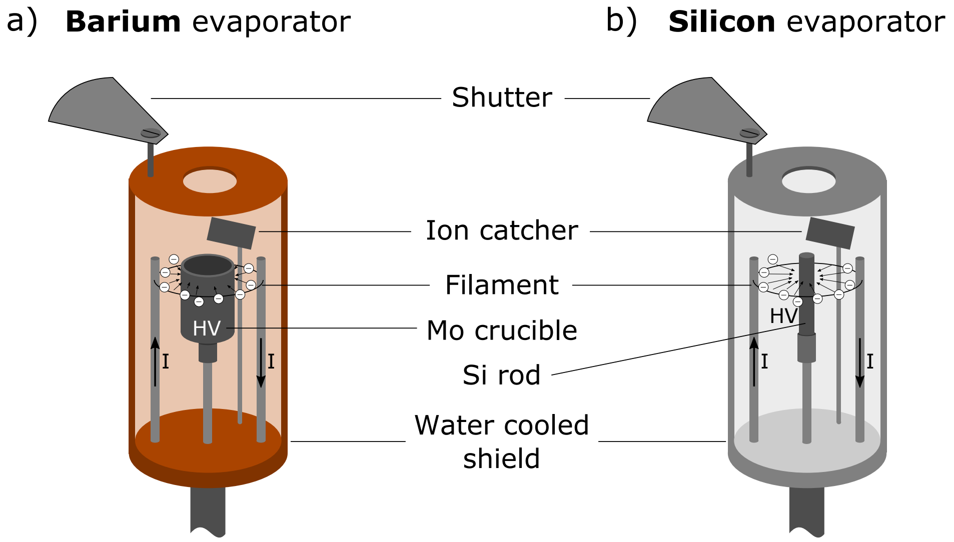


Figure 3.3.: Illustration of the Ba (a) and Si (b) e-beam evaporators. Ba is evaporated from a crucible and Si is evaporated from a rod by heating with electron bombardment. For this purpose, a high voltage is applied to the crucible/rod, which accelerates the electrons emitted from the heated filaments onto the crucible/rod.

with achieving a stable evaporation rate. Additionally, there is an ion catcher, which is basically a metal plate insulated from the body of the evaporator so that a voltage can be applied to it in order to attract the ions from the material flux. Under the assumption that the measured ion current is proportional to the overall material flux it can be used to determine and stabilize the evaporation rate. A shutter is used to set the beginning and the end of the material deposition.

For Ba a high voltage of 450 V and a filament current of $1.88 - 1.92$ A is used. The filament current needed to achieve the same evaporation rate slightly increases with a decreasing filling level of the crucible. A frequency change of 8 Hz/min measured with the quartz crystal microbalance in sample position, corresponds to the Ba flux necessary to grow Ba_2SiO_4 with a rate of 1.1 ML/min. For Si a high voltage of 1.7 kV is used. The filament current is controlled by the electronics so that a set ion current is maintained throughout the deposition. An ion current of 5.5 nA corresponds to the Si flux required to grow Ba_2SiO_4 at a rate of 1.1 ML/min. The exact filament current needed to achieve this ion current varies depending on the position of the end of the Si rod with respect to the filament. Ideally, the rod should be positioned so that the filament current is at around or slightly below 7 A during the evaporation. The filament current should never exceed 8 A since this can damage the filament.

Filling of the Ba evaporator: Barium is highly hygroscopic. On air it quickly reacts with the water vapor to form hydroxide. Therefore, it has to be stored in mineral oil and the filling of the evaporator has to be performed in a protective gas atmosphere. For this a glove bag is used, which gets filled with nitrogen gas directly from a ℓN_2 can. First of all, the bag is flushed with nitrogen gas five times. After refilling the bag again, the barium, which is still in the mineral oil, and the required tools are put inside. The Ba pieces are then thoroughly cleaned in n-hexane in order to remove the mineral oil. This step is very important, since the mineral oil does not easily evaporate in the vacuum. If the crucible is contaminated with mineral oil, the long hydrocarbon chains decompose when the crucible is heated, resulting in the release of CH$_2$ radicals into the vacuum as confirmed by a mass spectrometer. In the $10 - 15$ min it takes to achieve a stable evaporation rate, a monolayer of these molecules easily attaches to the silicon substrate surface, as confirmed by XPS, destroying the crystalline template and thereby rendering an epitaxial growth impossible. Alternatively, vacuum sealed barium can be used, which is, however, more expensive. After the barium pieces are cleaned, they are cut into smaller pieces using a side cutter, put into the crucible and then pounded down using a ceramic rod and a hammer. After that, the Ba pieces inside the crucible are covered with n-hexane and the crucible is taken out of the glove bag. As quickly as possible, the crucible is mounted in the evaporator and the evaporator is installed in the vacuum chamber, which is then pumped down. The n-hexane in the crucible is refilled as needed. The system is set up so that the Ba evaporator can be pumped separately from the main chamber by a dedicated turbo pump. Thus, it can be refilled without venting the preparation chamber. The setup is similar to the one described in figure 3.2 of Ref. [88]. After the bake-out the evaporator has to be thoroughly degassed, which takes about $1 - 2$ weeks.

3.2. Sample preparation

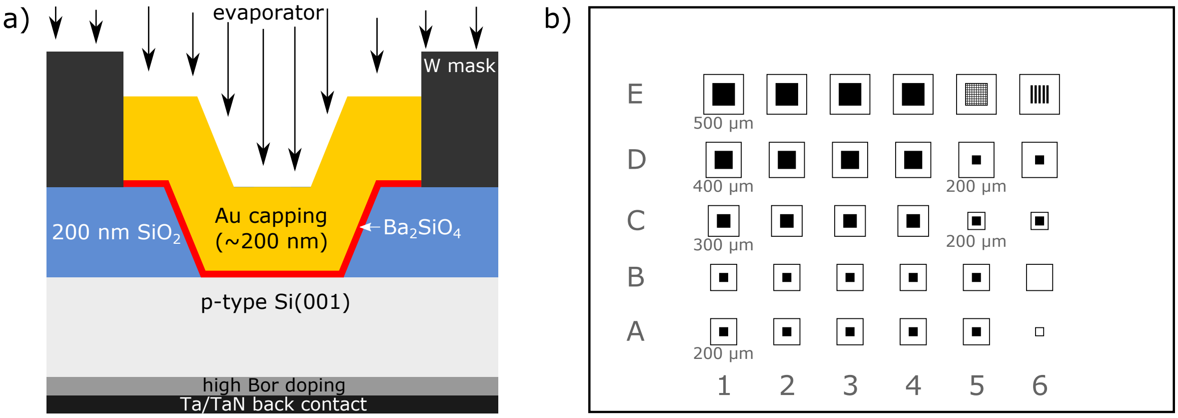


Figure 3.4.: Lithographically structured samples: (a) Cross-section of a single capacitor after the film deposition is completed. (b) Layout of the structured substrates (size $6 \times 14\,\mathrm{mm}^2$) with multiple test capacitors. The black squares represent the active area of the capacitors, i.e. where the Ba$_2$SiO$_4$ films are in contact with the silicon. The specified lengths are the side lengths of the active areas. The frames around them represent the area of the gold contacts. The columns are labeled from 1 to 6 and the rows are labeled from A to E. The fields A6 and B6 are used to check the integrity of the insulating SiO$_2$ layer. The fields E5 and E6 contain test structures to check the quality of the lithography.

Two types of substrates are used in this work. For the XPS, LEED and STEM measurements Si(001) wafer pieces with a size of 6×14 mm^2 are used. These are referred to as unstructured substrates. On the other hand, for the electric characterization of the Ba_2SiO_4 films, lithographically structured substrates, where squares with sizes from 200×200 µm^2 to 500×500 µm^2 were etched in a SiO_2 layer on a 13×9 mm^2 Si(001) wafer piece, are prepared. The squares are used to produce test capacitors. The cross-section of such a capacitor is illustrated in Fig. 3.4a). The Ba_2SiO_4 films are deposited into the etched squares and then capped with a gold layer, which also serves as the gate contact. The gold contacts of the individual capacitors are separated by the use of a W shadow mask. To contact the silicon substrate a Ta/TaN-stack is sputtered on the back of the substrate after it has been highly doped. The layout of the structured wafer pieces is illustrated in Fig. 3.4b). The black squares represent the active area of the capacitors, i.e. the squares etched into the SiO_2 layer. The frames around them represent the area of the gold contacts. The columns are labeled from 1 to 6 and the rows are labeled from A to E. The fields A6 and B6 do not have a square etched into the SiO_2 layer. They are used to confirm that the SiO_2 layer does not become too thin during the flash annealing and remains properly insulating so that its contribution to the measurement of the other capacitors is negligible. The fields E5 and E6 contain test structures used to check the quality of the lithography. These two were not used for the electric characterization. The reduction of the area of the test capacitors by the lithographic structuring is necessary in order to reduce the probability that a capacitor is unusable due to defects.

The wafers were p-type (B doped, (001) ± 0.5°, prime CZ, 240 ± 15 µm thickness) with a resistivity of $10 - 20\ \Omega\,\mathrm{cm}$ ($N_A = 1 \times 10^{15}\ \mathrm{cm}^{-3}$). The only exception is the determination of the band offsets to n-type silicon. In this case n-type Si(001) (Ph doped, (001) ± 0.5°, prime CZ, 360 ± 15 µm thickness) with a resistivity of $8 - 12\ \Omega\,\mathrm{cm}$ was used. The structured substrates for the electrical characterization were only prepared using the p-type Si(001) wafers.

3.2.1. Cleaning of the unstructured substrates

Before introducing the substrates into the UHV chamber they are cleaned with wet chemicals. In the first step, they are cleaned successively in purified water ($\rho > 18\ \mathrm{M\Omega\,cm}$), petroleum ether, acetone, isopropanol and again in purified water in an ultrasonic bath for 15 min per step. In between the organic solvents the substrates are rinsed in purified water. In the second step, the natural oxide layer is removed by dipping the substrates into a 1% Hf solution. The complete removal of the oxide layer is indicated by a hydrophobic surface, i.e. when taking the substrate out of the solution the water droplets roll off the surface completely so that no water remains on the silicon piece. This happens after approximately 30 s. The substrates are then immediately rinsed in purified water for 30 s, followed by a controlled re-oxidation in H_2O_2 solution (35%) for 40 s, after which they are rinsed in purified water for 30 s again. Within 5 min the substrates are then mounted on the sample holders and put into the pre-load-lock. After the pre-load-lock has been pumped for 30 min, the sample holders are transferred to the load-lock.

In vacuum, the substrates are degassed at 550 – 600 °C over night for at least 12 hours using direct current heating. Afterwards they are trained by subsequently heating to temperatures between 700 and 800 °C for a few minutes per step until the pressure remains below $4 \cdot 10^{-10}$ torr when the substrate is heated to 800 °C for 1 min. This step takes about 4 – 5 hours. Care is taken that the pressure never exceeds $1 \cdot 10^{-9}$ torr during this step. Finally, the oxide layer is removed by flash annealing the substrate to 1050 °C for 2 – 3 s. The pressure should not exceed $1 \cdot 10^{-9}$ torr during the flashing. During all heating steps and especially during the overnight degassing, the manipulator is cooled with compressed air.

3.2.2. Preparation and cleaning of the structured substrates

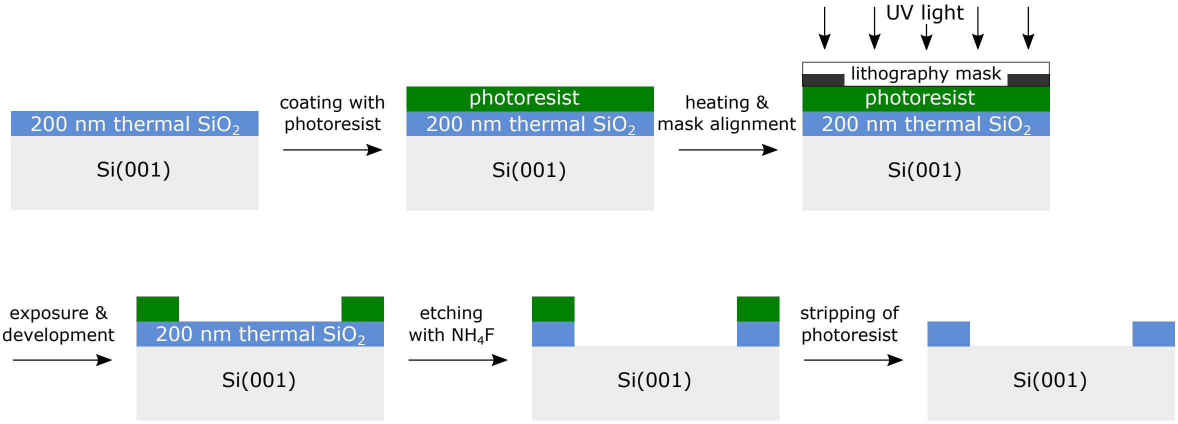


Figure 3.5.: Illustration of the lithographic structuring process. Based on [89].

The lithographic structuring is done in the clean room of the Laboratorium für Nano- und Quantenengineering (LNQE). The process is illustrated in Fig. 3.5. In the first step, a 200 nm thick SiO_2 layer is prepared by wet thermal oxidation of the wafer in an oxidation furnace with water vapor. The wafer is then transferred to a second oven, where it is treated with HMDS (hexamethyldisilazane) at 150 °C for 10 min. Afterwards the oven is purged with nitrogen gas before the wafer is taken out. The second step is the optical lithography. Positive photoresist (Microposit S1813) is applied using a spin coater (4000 rpm for 1 min). The resist is then dried on a hot plate at 110 °C for 1 min. After the alignment of the lithography mask, the photoresist is exposed for 8 s. The mask is then taken off and the photoresist is removed from the exposed areas, i.e. the squares for the capacitors, with the developer Microposit MF-24A. Finally, the squares for the capacitors are etched into the SiO_2 layer with ammonium fluoride right down to the unoxidized silicon. The etching parameters are chosen so that the sidewalls form at an angle of approximately 60° to the silicon surface. The remaining photoresist is then removed with Microposit remover 1165. The third step is the fabrication of a back contact for the electrical measurements. For this purpose, the backside of the wafer is highly doped with an implanter (for p-type silicon: Bor, $5 \cdot 10^{15}$ cm^{-2}). Usually, the dopants would have to be activated at this point by annealing the wafer to 1000 °C for a few seconds in an argon protective gas atmosphere. However, in order to prevent contamination of the front surface, this was not done. Instead, the flash annealing step in the UHV, which is used to remove the thin oxide layer inside the etched squares, serves to activate the dopants as well. After the implantation, a Ta/TaN-stack is sputtered on the back. The wafer is then cut into $13 \times 9\,\mathrm{mm}^2$ pieces that can be mounted on the sample holder. These pieces are cleaned in acetone in seven dilution steps to remove the residues of the photoresist and stored in an argon protective gas atmosphere until they are needed.

Directly before putting the structured substrates into the UHV chamber, they are cleaned again with wet chemicals. First, they are cleaned successively in acetone, purified water ($\rho > 18\ \mathrm{M\Omega\,cm}$), isopropanol and again five times in purified water in an ultrasonic bath for 15 min per step. Second, the substrates are cleaned in piranha solution, consisting of four parts H_2SO_4 (96%, VLSI grade) and one part H_2O_2 (30%, VLSI grade) at a temperature of 100 °C for 10 min in order to remove organic contaminants. Third, an RCA SC-1 cleaning step is performed in order to further reduce the concentration of organic contaminants. The solution is prepared by first adding 14 ml NH_4OH (20%, ppb-quality) to 46 ml purified water. It is important that the NH_4OH is added to the water and not the other way around. The solution is then heated to 70 °C on a hot plate. Once the temperature is reached, 10 ml H_2O_2 (30%, VLSI grade) is added, the solution is stirred and then equally distributed over three beakers, so that the RCA SC-1 cleaning step can be done in three dilution steps. The solution is then reheated to around 70 °C. Thereafter, the substrates are successively immersed into the RCA SC-1 solutions in the three beakers for 3 min 20 sec each. After each step the substrates are rinsed in purified water. While taking the substrates out of the water, purified water is poured into the beaker so that the water in the beaker overflows. This is done so that the dissolved contaminants that have collected at the water surface do not reattach to the substrate when taking it out. Silica glass beakers are used for the RCA SC-1 solution. Fourth, the natural oxide layer inside the etched squares is removed by an Hf dip (1%, 30 sec). The substrates are then immediately rinsed in purified water for 30 s, followed by a controlled re-oxidation in H_2O_2 solution (30%, VLSI grade) for 30 s, after which they are rinsed in purified water for 30 s again. Finally, the substrates are dried using nitrogen gas (5.0). Within 5 min the substrates are then mounted on the sample holders and put into the pre-load-lock. An optical microscope is used to adjust the shadow mask for the gate contacts. After the pre-load-lock has been pumped for 30 min, the sample holders are transferred to the load-lock.

Before mounting the new substrate in the sample holder, the gold from the previous sample is removed with metal polish and a metal file from both the sample holder and the shadow mask. The sample holder and the mask are inspected for residual gold under an optical microscope. When all of the gold is removed, they are cleaned with petroleum ether and isopropanol. Afterwards, a dummy substrate is mounted in the sample holder with the shadow mask and the sample holder is introduced into the UHV chamber and degassed by heating the dummy substrate up to 700 °C and then flash annealing it to 1000 °C. Shortly before the last cleaning step of the new substrate, the sample holder it taken out of the vacuum and prepared for mounting the new substrate.

In the vacuum the substrate is degassed at temperatures up to 750 °C for a few minutes per step until the pressure remains close to the base pressure while the substrate is heated. Then it is flash annealed at increasing temperatures from 800 °C to 950 °C for about ten times in total. During this step the pressure never exceeds $4 \cdot 10^{-10}$ torr. Finally, it is heated to 700 °C for 40 min in order to heal the silicon surface. The heating is performed using the e-beam heater with a voltage of around 1 kV (it is slightly changed to adjust the temperature) applied to the sample during the first degassing step and a voltage of 1.5 kV applied to the sample during the flash annealing step. The flash annealing is done by changing the filament current. A filament current of 5.8 to 6.0 A is required to reach 950 °C while a voltage of 1.5 kV is applied to the sample. During the whole time the manipulator is cooled with ℓN_2.

The cleaning method for the structured substrates described above was used in this exact way only for the second batch of samples prepared. Most of the results presented in this work are from this second batch of samples. If possible, the results from the first batch of samples were not used, since they showed very high leakage currents in the majority of the capacitors, with some of the films even being short-circuited. The cause of this was identified as the films not being closed most likely due to residual hydrocarbons on the silicon surface (see appendix A.1). Therefore, the cleaning method was improved. Firstly, a fresh photoresist was used to ensure that it can be completely removed, which can become a problem with old photoresist that has drawn too much water. Secondly, the piranha etching step was added, which was previously omitted since it roughens the silicon surface, and the number of dilution steps of the RCA SC-1 cleaning step was increased from one to three. Thirdly, it was refrained from activating the dopants by annealing the wafer to 1000 °C for a few seconds in an argon protective gas atmosphere, which was done with the wafer of the first batch, since this leads to the contamination of the front surface. Instead, the activation was done later in the UHV. These steps significantly improved the leakage currents. However, some of the capacitors of the samples from the first batch showed low enough leakage currents so that the CV measurements could be evaluated. Namely, the results of the 5 and 7 nm films in section 5.4 and the film grown in a high oxygen pressure and annealed at 680 °C in section 5.6 are from samples of the first batch.

The given temperatures for when the substrate is heated using the e-beam heater refer to the temperatures of the A-C rows of the structured substrates. Due to the construction of the e-beam sample heater and the associated sample holder (see Fig. 3.2) only those rows are directly above the filament, while the D and E rows are further away from it. This results in a temperature gradient on the substrate. At 680 °C the temperature of the D-row was approximately 10 °C lower and the temperature of the E-row was approximately 20 °C lower than the specified temperature.

3.2.3. Preparation of the thin films

Ba_2SiO_4 layers with thicknesses between 1 and 16 nm (4 and 63 monolayers (ML)) were prepared under UHV conditions as described in the following. After the flash annealing of the substrate, Ba and Si were deposited simultaneously in an oxygen atmosphere. At the beginning of the growth, 0.5 ML Ba were first deposited before the Si flux was added. Subsequently, oxygen was introduced into the chamber and the oxygen partial pressure was carefully increased to its final value within 30 s after the addition of the Si flux. A usual deposition rate was 1.1 ML/min. The fluxes were controlled by a quartz crystal microbalance at sample position, which was also used to calibrate relative thicknesses. Unless otherwise noted, the substrate was at room temperature (RT) during the film deposition in order to minimize oxidation of the Si surface and Si diffusion from the substrate. In a few cases the films were grown at elevated substrate temperatures of around 400 °C. Afterwards, the films were annealed at temperatures between 400 and 700 °C for 30 to 40 min. Annealing was always carried out in vacuum without oxygen. The temperatures were determined with a pyrometer (min. 300 °C) with emission coefficients adjusted to Si. In particular, $\varepsilon = 0.574$ was used for $T = 680\,^{\circ}\mathrm{C}$. A new Si sample was used for each film. The optimum oxygen background pressure and annealing temperature are discussed in sections 4.5 and 4.6. A preliminary film thickness calibration of the Ba_2SiO_4 films was done using XPS (see section 2.4.6) and the final absolute thickness calibration was done using STEM images.

BaO films were grown similar to the Ba_2SiO_4 films but without the Si flux. The SiO_2 film in section 4.1 was gown by thermal oxidation and its thickness was measured by ellipsometry.

3.3. Experimental details of the measurements

3.3.1. X-ray photoelectron spectroscopy

All XPS measurements shown in this work were taken using an Al K_α emission source. Overviews of the full spectrum were taken at a pass energy of 40 eV and high resolution scans of the individual peaks were taken at a pass energy of 20 eV. The instrument was calibrated with a silver sample. Zero binding energy refers to the Fermi level, which was experimentally determined as the middle of the rise of the measured Fermi edge. For the evaluation of the XPS spectra a Shirley background was first subtracted before the peaks were fitted. The fit functions used are LA(1.5,1.5,100) for O 1s, LA(2,2,100) for Si 2p, LA(1.9,1.6,0) for Si 2s and GL(60) for Ba 3d in CasaXPS [90]. The fit functions are convolutions of a Lorentzian and a Gaussian. For the LA(x,y,z) type line shape the x parameter determines the shape of the left flank and the y parameter determines the shape of the right flank. If they are the same, the curve is symmetrical. The LA(1.5,1.5,100) type line shape for the O 1s peak was carefully chosen based on the O 1s signals of 16 nm thick BaO and Ba_2SiO_4 films, both of which feature single O 1s peaks. It perfectly describes these signals. The line shapes for the Si peaks were chosen based on the measurements of the clean substrates.

In order to compare integrated XPS intensities the measuring conditions have to be identical for both measurements, i.e. the instrument has to be in the exact same state and the sample has to be in the exact same position. The first part was ensured by keeping the instrument running when the measurements were performed on the same day, i.e. when comparing the same sample before and after annealing. When the measurements were performed on different days, the instrument was turned off between the measurements, however, all potentiometers were locked in place and only on/off-switches were used so that the applied voltages and currents remained the same for all measurements. Moreover, only measurements from one measurement period were compared, with no bake-out of the system in between. Furthermore, the manipulator is equipped with micrometer screws that allow the sample to be reliably put in the same position for every measurement. The identical measuring conditions were ultimately confirmed by the background levels and the signal of the bare silicon substrate being the same.

3.3.2. Scanning transmission electron microscopy

Ex situ aberration-corrected scanning transmission electron microscopy (STEM) measurements were done in the Ernst Ruska-Centre for Microscopy and Spectroscopy with Electrons, Forschungszentrum Jülich by Prof. Dr. Knut Müller-Caspary. For these measurements an 11 nm Ba_2SiO_4 film was deposited on an unstructured substrate and capped with 1 ML of Si followed by 300 nm of Au to protect the film from the ambient air.

Two cross-sectional TEM lamellae cut along the Si(110) and Si($1\bar{1}0$) planes have been prepared using a focused ion beam (FIB) facility with a final low-energy milling step in order to remove amorphized surface layers arising from previous milling steps. Scanning Transmission Electron Microscopy was performed using a FEI Titan 80/300 STEM instrument equipped with an aberration corrector for the probe-forming lens [91]. The microscope was operated at 200 kV, and high-angle annular dark field (HAADF) Z-contrast STEM images were acquired using a Fischione 3000 detector at a camera length of 135 mm.

3.3.3. Electrical characterization

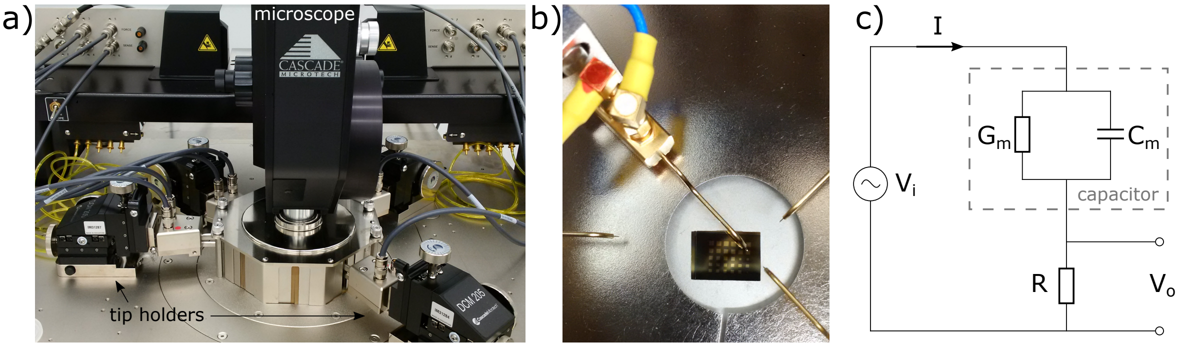


Figure 3.6.: Measurement setup for the electrical characterization: (a) Cascade Probe Station with four tip holders and an optical microscope to place the tips on the sample in a controlled manner. (b) Top view of a sample in the probe station. A tip is placed on one of the capacitors. (c) Equivalent circuit diagram for the measurement of the capacitance and the conductance of a capacitor under the assumption of a two-element parallel model.

The electrical characterization was performed using a Cascade Probe Station Summit

11K in the Laboratorium für Nano- und Quantenengineering (LNQE) of the Leibniz Universität Hannover. The gate contact of the capacitor to be measured is contacted with a needle tip and the second contact is made between the back of the wafer and the chuck (see Figs. 3.6a) and b)). CV-measurements were performed with an Agilent 4294A Precision Impedance Analyzer and IV-measurements were taken using a Hewlett Packard 4155A Semiconductor Parameter Analyzer.

The impedance analyzer allows to either measure the magnitude and the phase of the impedance or to directly measure derived parameters by using a two-element model as a representation for the MOS capacitor. The latter mode was used in this work in combination with a two-element parallel model. The principle of this measurement is illustrated in Fig. 3.6c). An input voltage V_i, which consists of a direct voltage component and an alternating voltage component, is applied to the capacitor, which is assumed to be represented by the conductance G_m and the capacitance C_m connected in parallel. A test resistor R is used to measure the output voltage V_o, which is related to the input voltage V_i by [75]

$$\frac{V_o}{V_i} = \frac{R}{Z} = \frac{R}{R + (G_m + i\omega C_m)^{-1}} = \frac{RG_m(1 + RG_m) + (\omega RC_m)^2 + i\omega RC_m}{(1 + RG_m)^2 + (\omega RC_m)^2}, \tag{3.1}$$

where $Z = R + (G_m + i\omega C_m)^{-1}$ is impedance of the circuit and $\omega = 2\pi f$ is the angular frequency corresponding to the frequency f of the alternating voltage component of the input voltage V_i. If R is chosen so that $RG_m \ll 1$ and $(\omega RC_m)^2 \ll RG_m$, equation 3.1 is simplified to [75]

$$V_o \approx (RG_m + i\omega RC_m)V_i. \tag{3.2}$$

By using a phase sensitive detector and with the knowledge of R and ω, the conductance G_m and the capacitance C_m can thus be determined from the in-phase and out-of-phase components of V_o, respectively.

4. Structural properties of Ba_2SiO_4 thin films

4.1. Identification of chemical bond formation from the shift of the O 1s signal in XPS

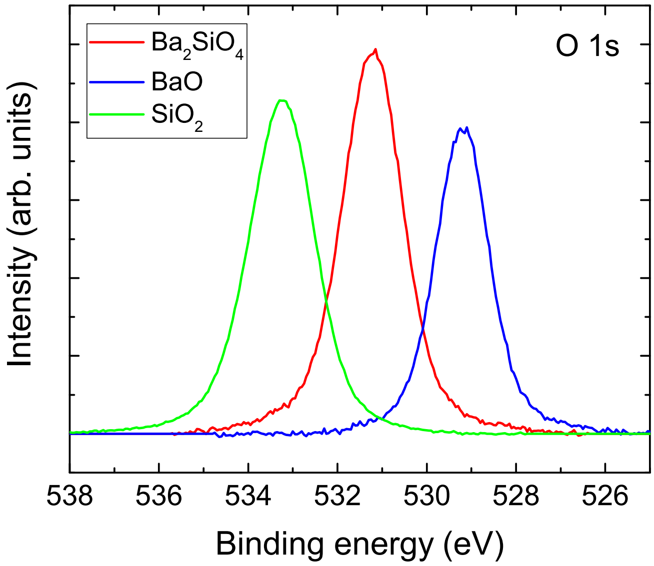


Figure 4.1.: Shift of the O 1s signal in XPS: Amorphous layers of BaO (blue line, 16 nm thick), SiO_2 (green, 18 nm) and Ba_2SiO_4 (red, 16 nm, annealed at 400 °C) on Si(001) are compared. The intensity of the SiO_2 peak was not calibrated with respect to the others.

For the epitaxial growth of Ba_2SiO_4 it is important to be able to detect the formation of compounds that form in case of a deviation from the exact stoichiometry, i.e. BaO, SiO_2 and barium silicates with a higher Si concentration like $BaSiO_3$ or $BaSi_2O_5$. The differentiating characteristic of these compounds is the chemical bonding state of the O atoms. In the case of Ba_2SiO_4 every O atom has exactly one bond to Si and one bond to Ba, i.e. only Si-O-Ba bonding states are present (see section 2.2.2). All other barium silicate compounds have Si-O-Si bonding states in addition to the Si-O-Ba bonding states. BaO and SiO_2 have only Ba-O-Ba and Si-O-Si bonding states, respectively.

The chemical bonding state can be determined using XPS by measuring the shift of the O 1s signal. Since the barium silicates have no direct bonds between Si and Ba and since the chemical shift depends largely on the immediate bonding partners, the Si and Ba signals cannot be used to differentiate between the different compounds. In Fig. 4.1 the O 1s signals of BaO, SiO_2 and Ba_2SiO_4 are compared. All films are at least 16 nm thick, so that the interface contribution to the signals is negligible. The relative shift between the covalent bonds in SiO_2, and the ionic bonds in BaO is approximately 4 eV. The O 1s peak for Ba_2SiO_4 is located roughly in the middle of the SiO_2 and BaO peaks. Since the bonding state of the O atoms in Ba_2SiO_4 is exclusively Si-O-Ba, the O 1s peak is a single peak. In combination with the fact that the energy difference of about 2 eV between the different peaks can easily be resolved by a standard XPS, this makes it very simple to detect a deviation from the Ba_2SiO_4 stoichiometry. Excess concentrations of Si or Ba lead to clearly visible shoulders at higher or lower binding energies, respectively, given a sufficient oxygen supply. Therefore, the line shape of the O 1s peak is ideally suited to calibrate the system. It is important to note that the Si-O-Si bonding states, i.e. the shoulder at higher binding energies, can be either due to local SiO_2 or due to a barium silicate compound with a higher Si concentration than Ba_2SiO_4, which feature O atoms in two different bonding states, Si-O-Si and Si-O-Ba.

Note that since the films are insulators, there are slight shifts in the peak positions due to charging effects and possibly also due to shifts of the Fermi level. In particular, the O 1s peak of a 16 nm Ba_2SiO_4 film is shifted by around 0.4 eV towards higher binding energies as compared to a 1 nm film and the O 1s peak of an as deposited BaO film is shifted by approximately 0.7 eV towards lower binding energies as compared to an annealed BaO film. However, these shifts do not impede the evaluation of the peaks, since the distance between the different components (Si-O-Si, Si-O-Ba and Ba-O-Ba) is large enough to always allow for a clear deconvolution of the signal. Neither the exact peak positions nor the peak distances were used for the fitting, i.e. the peak positions were free parameter. Rather, the line shape, determined from 16 nm thick Ba_2SiO_4 and BaO films, was used for the deconvolution.

4.2. Detection of metallic barium from the line shape of the Ba 3d peak

While the shape of the O 1s signal is a powerful tool for the investigation of the stoichiometry of the deposited films, it only gives information about the different oxide species. The presence of metallic Ba or Si can, of course, not be detected directly by the O 1s signal. Metallic Ba or Si is expected, if the oxygen pressure during growth is too low for a complete oxidation of the film. One way to determine the minimal necessary oxygen pressure is to investigate the intensity of the main O 1s peak in dependence of the oxygen background pressure. Additionally, the shape of the Ba 3d signal gives information about the presence of metallic Ba. Due to plasmon losses at high binding energies the Ba 3d peaks for metallic Ba are more asymmetric than those of Ba_2SiO_4 and BaO [92] (Ba_2SiO_4 and BaO have a similar shape). A comparison of the peak shapes is shown in Fig. 4.2. At the high binding energy side the shape of the metallic Ba peaks slightly deviates from that of the Ba_2SiO_4 peaks (dashed line). Therefore, an asymmetry in the Ba 3d peaks can be used to detect metallic Ba.

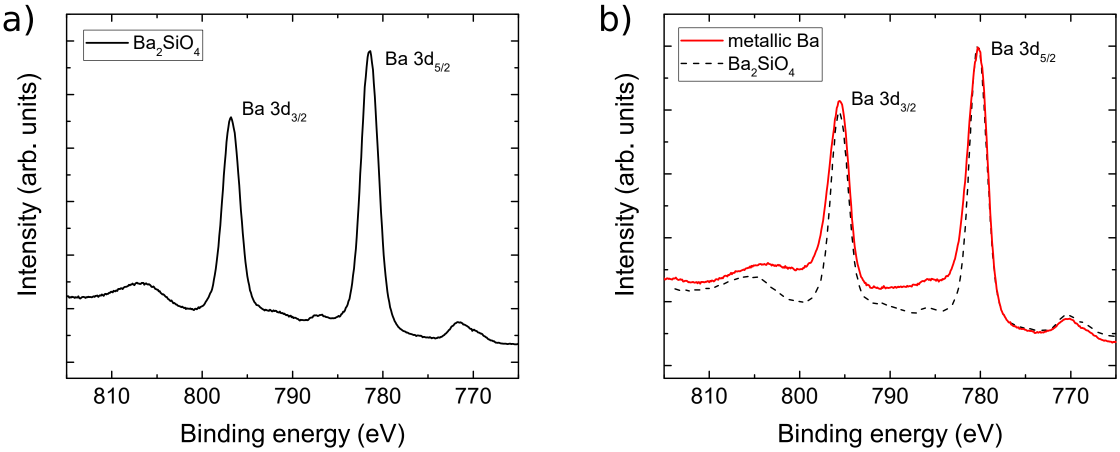


Figure 4.2.: Ba 3d signal in XPS of (a) a 16 nm thick Ba_2SiO_4 film and (b) metallic barium. The metallic Ba peaks are slightly more asymmetric than the Ba_2SiO_4 peaks, which are indicated a dashed line. To draw the dashed line the signal was shifted in energy and adjusted in intensity to fit to the metallic Ba signal.

4.3. Formation of BaO_2 during the film growth

A problem with the determination of the stoichiometry of the deposited film by using the O 1s signal in XPS as described above is that the peak associated with BaO_2, i.e. the Ba-O-O bonding state, is located very close to that of the Si-O-Si bonding state [93], which can complicate the interpretation. The formation of BaO_2 becomes clear when investigating the O 1s signal of BaO films, since these films do not contain Si in the bulk, i.e. there are no bulk Si-O-Si and Si-O-Ba signals. As seen in Fig. 4.3, directly after deposition the O 1s signal of a 20 nm thick BaO film deposited in an oxygen background pressure of $5 \cdot 10^{-7}$ torr with a deposition rate of 1.1 ML/min (which corresponds to the Ba flux needed for 1.5 ML Ba_2SiO_4 per minute) shows an additional peak located 3.55 eV away from the main peak towards higher binding energies. Since no Si is present in the film and the film is also thick enough so that the interface is not visible in XPS (there is no Si signal), the additional peak has to be due to Ba-O-O bonding states. The additional peak can be completely removed by annealing the film to 335 °C as also shown in the figure. As a result, the intensity of the Ba-O-Ba peak is increased and no Ba-O-Si peak emerges. This confirms that the additional peak that is present directly after deposition is due to Ba-O-O bonding states. If it was due to Si-O-Si bonding states, heating the film would result in the formation of Ba-O-Si bonding states for thermodynamic reasons, which would also result in a decrease of the Ba-O-Ba intensity.

Fig. 4.4 shows the thickness dependence of the O 1s signal for BaO films grown again in an oxygen background pressure of $5 \cdot 10^{-7}$ torr with a deposition rate of 1.1 ML/min. As expected, the Ba-O-Ba peak increases with increasing film thickness. There is also a Ba-O-Si peak due to silicate formation at the interface. Its intensity decreases with increasing film thickness and vanishes at 20 nm due to the signal being damped by

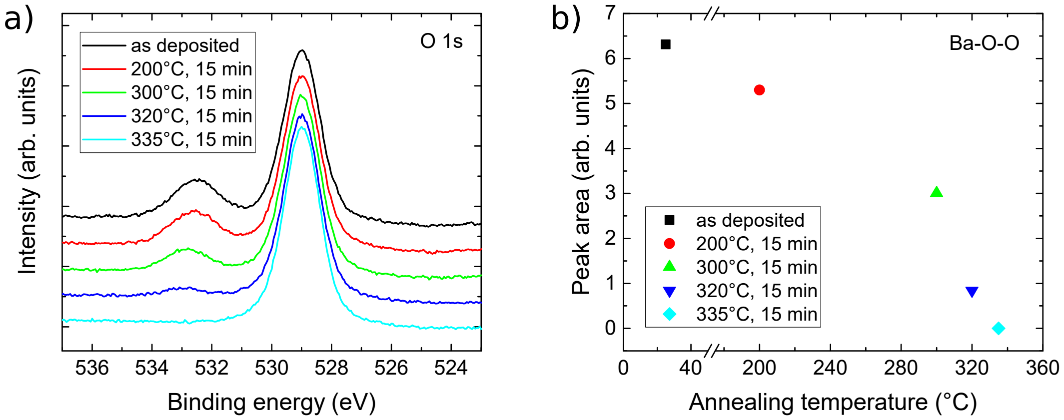


Figure 4.3.: Removal of BaO_2 from a 20 nm thick BaO film by annealing: (a) O 1s signals after each annealing step, shifted in intensity for better visibility. The small peak at 532.75 ± 0.25 eV is due to BaO_2/Ba-O-O. (b) Integrated intensity of the Ba-O-O peak in dependence of the annealing temperature. The signal of the as deposited film was shifted by 0.72 eV towards higher binding energies to align it the others.

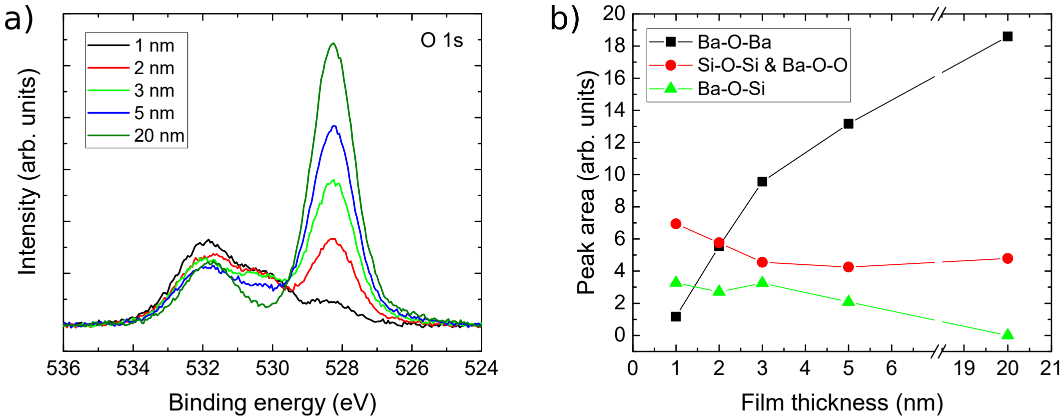


Figure 4.4.: Film thickness dependence of the O 1s signal for BaO films: (a) O 1s signals for film thicknesses from 1 to 20 nm. Shirley backgrounds were subtracted. The signals of the thinner films were shifted to be aligned with the signal of the 20 nm film. The average binding energy of the Ba-O-Ba peak is (528.10 ± 0.21) eV. There is no clear trend with the thickness. (b) Integrated intensities of the different components from the deconvolution of the O 1s signals in dependence of the film thickness.

the overlying layers. The Ba-O-O/Si-O-Si peak decreases from 1 to 3 nm, possibly due to Si-O-Si formation at the interface, and remains approximately constant from 3 to 20 nm. This shows that the main share of Ba-O-O/BaO_2 is located at the surface of the layer. The bulk of the film is mainly BaO.

The dependence of the O 1s signal on the oxygen background pressure during the growth of BaO films is shown in Figs. 4.5a) and b). The films were again grown with

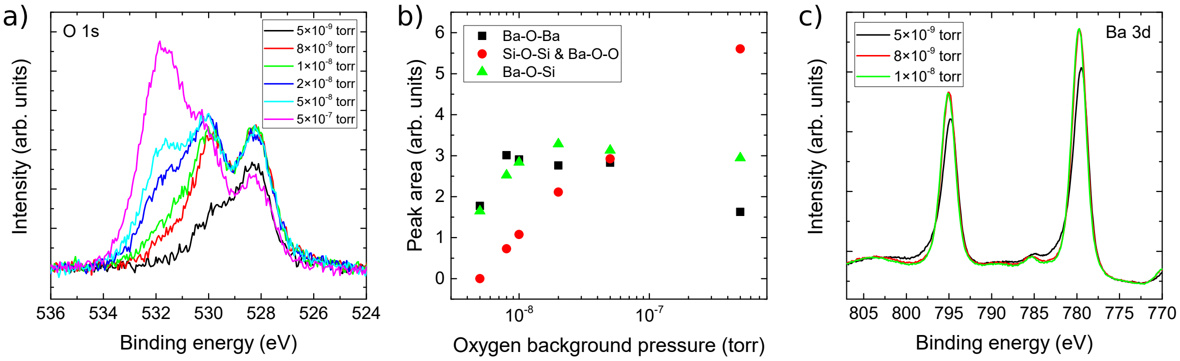


Figure 4.5.: Effect of the oxygen background pressure on the chemical composition of 1 nm thick BaO films: (a) O 1s signals for oxygen pressures from $5 \cdot 10^{-9}$ to $5 \cdot 10^{-7}$ torr for films grown with a deposition rate of 1.1 ML/min. Shirley backgrounds were subtracted. (b) Integrated intensities of the different components from the deconvolution of the O 1s signals in dependence of the oxygen pressure. (c) Ba 3d peaks for oxygen pressures from $5 \cdot 10^{-9}$ to $1 \cdot 10^{-8}$ torr. The XPS signals were shifted, so that the O1 s signals are aligned. Before, there was a gradual shift in the position of the Ba-O-Ba peak from 528.89 eV at $5 \cdot 10^{-9}$ torr to 528.19 eV at $5 \cdot 10^{-7}$ torr.

a deposition rate of 1.1 ML/min and are 1 nm thick (More precisely, the amount of Ba that is needed for the formation of a 1 nm thick BaO film was deposited in each case. The actual film thickness slightly varies due to the differing oxygen content). The Ba-O-O/Si-O-Si peak increases logarithmically with the oxygen pressure, i.e. the amount of BaO_2 depends on the oxygen pressure. The Ba-O-Ba peak is approximately constant from $8 \cdot 10^{-9}$ to $5 \cdot 10^{-8}$ torr, but decreases at $5 \cdot 10^{-7}$ torr. This implies that at lower thicknesses the additional O atoms only accumulate at the top of the film forming O-O bonds, whereas they also penetrate into the topmost layer at $5 \cdot 10^{-7}$ torr. More importantly, however, is the decrease of the Ba-O-Ba intensity at $5 \cdot 10^{-9}$ torr. As seen in Fig. 4.5c) the Ba 3d peaks also become more asymmetric at this pressure indicating the presence of metallic Ba due to an incomplete oxidation of the film. This means that an oxygen pressure of 0.8 to $1 \cdot 10^{-8}$ torr at a growth rate of 1.1 ML/min is ideal in order to minimize the BaO_2 formation, while still oxidizing the film completely.

In summary, BaO_2 is formed at the top of BaO films, and by extension possibly also on Ba_2SiO_4 films, grown in a high oxygen background pressure. It can be minimized by minimizing the oxygen pressure and is completely converted into BaO by annealing the film to 335 °C or higher.

4.4. Stoichiometry and chemical homogeneity of Ba_2SiO_4 thin films

The ratio between the Si and Ba fluxes has to be carefully adjusted for stoichiometric growth conditions since this ratio is non-self-limiting. The oxygen concentration, on

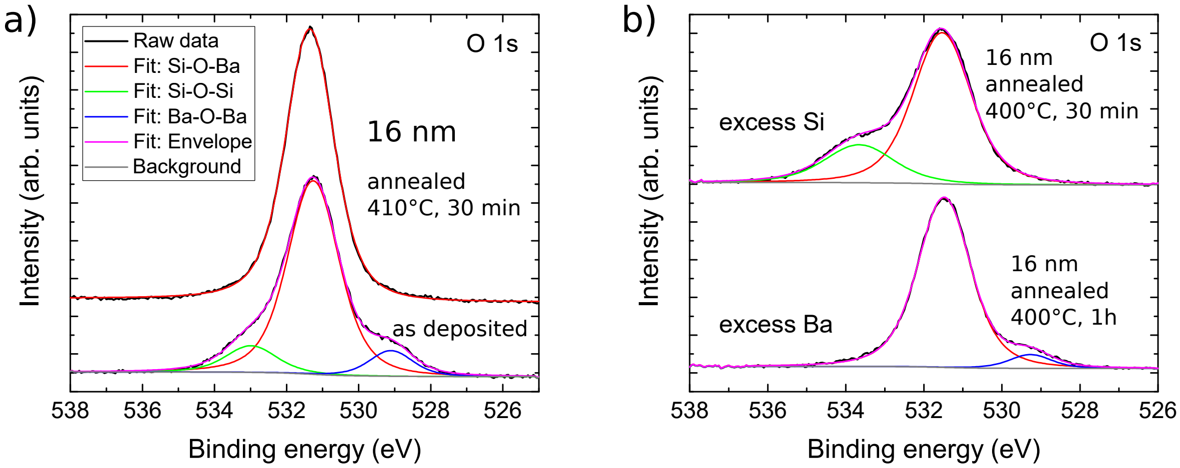


Figure 4.6.: Incomplete reaction at RT and identification of excess concentrations: (a) O 1s signal of a 16 nm (63 ML) thick Ba_2SiO_4 film, as deposited at room temperature (bottom curve) and after annealing at 410 °C (top curve). The film was grown in an oxygen background pressure of $1.2 \cdot 10^{-8}$ torr with a growth rate of 1.1 ML/min, so that the Ba-O-O formation is negligible. The deconvolution into the individual components is shown by colored lines as indicated in the inset. (b) O 1s signal after annealing at 400 °C for 16 nm thick films grown with a Si flux that was too low (bottom curve) or too high (top curve) for the stoichiometric growth of Ba_2SiO_4. The signals were shifted in intensity for better visibility.

the other hand, is self-limiting *in the bulk* as long as the oxygen partial pressure is high enough for a complete oxidation of the films. At the surface of the films Ba-O-O is formed depending on the oxygen pressure similar to BaO films as discussed above. Moreover, the stoichiometry at the interface is highly dependent on the oxygen pressure due to the oxidation of the silicon surface as will be discussed in detail in section 4.5. However, if the films are thick enough so that the interface is not visible in XPS, they were either annealed at 400 °C or directly grown at 400 °C in order to avoid Ba-O-O formation and the oxygen partial pressure during growth was high enough for a complete oxidation of the films, then the O1 s signal in XPS does not change at fixed Ba and Si fluxes even if the oxygen pressure is increased by one order of magnitude, i.e. the oxygen content of the films bulk is only determined by the Si and Ba fluxes.

The Si and Ba fluxes were adjusted to the required atomic ratio of 1:2 using a quartz crystal microbalance located at sample position by weighting the changes in frequency over time with the atomic masses. In order to confirm that the correct Si:Ba atomic ratio is obtained in the deposited films, a 16 nm (63 ML) thick Ba_2SiO_4 films was grown. At this thickness, the contribution of the interface to the XPS signal is negligible. Moreover, the film was grown in an oxygen pressure at which the Ba-O-O formation is negligible. The O 1s peaks after deposition at room temperature (RT) and after annealing at 410 °C for 30 min are shown in Fig. 4.6a). Directly after deposition the O 1s peak has two shoulders with approximately the same area. This demonstrates that the reaction at RT is incomplete so that local deviations from stoichiometry lead to various bonding states and to only about 80% preference for the Si-O-Ba bonding state. Only after annealing to 410 °C , which does not lead to any desorption, a single peak at the Si-O-Ba position is formed, i.e. the reaction is complete. As expected, this peak has approximately the same integrated intensity as the RT peak including the shoulders. This symmetric peak demonstrates that the correct deposition ratio for stoichiometric deposition was chosen. Furthermore, it shows that temperatures around 400 °C are sufficient for getting a *chemically* homogeneous film. This temperature, however, is too low to crystallize amorphous layers. In fact, all films starting with an amorphous interface layer turned out to remain amorphous after an annealing step to 400 °C.

The growth of films with incorrectly adjusted fluxes leads to the presence of Si-O-Si bonding states in the case of excess Si or Ba-O-Ba bonding states in the case of Ba excess even after an annealing step at 400 °C as shown in Fig. 4.6b). The Ba-O-Ba bonding states can be turned into Si-O-Ba bonding states by Si diffusion from the substrate if the film is further annealed. On the other hand, the Si-O-Si bonding states can not be removed by annealing. For thermodynamic reasons the Si-O-Si bonding states are expected to be due to barium silicates with a higher Si concentration than Ba_2SiO_4, e.g. $Ba_3Si_2O_7$, $BaSiO_3$ or $BaSi_2O_5$, instead of SiO_2, at least after annealing.

4.5. Interface properties and oxygen background pressure

In contrast to the bulk material, the interface between the silicate and the Si(001) surface is highly sensitive to the oxygen background pressure. On the one hand, this is due to the oxidation of the Si(001) surface, i.e. the formation of amorphous SiO_x. On the other hand, the Si wafer acts as a reservoir for Si so that the formation of Si-rich silicate compounds is possible, irrespective of the Si flux. Both effects limit the crystalline quality of the deposited film. In order to achieve high quality epitaxial films with an abrupt interface, it is therefore absolutely essential to fine tune the oxygen partial pressure to a value just above the saturation point for complete oxidation.

For calibration of the oxygen partial pressure, the line shape of the O 1s peak in XPS is used again, but this time ultrathin films are investigated so that the interface is visible. For this purpose, 4 ML (1 nm) thick films were grown at a rate of 1.1 ML/min in different oxygen partial pressures using the stoichiometric Si:Ba ratio determined above. The corresponding O 1s peaks and the integrated intensities of their individual components are shown in Figs. 4.7a) and b), respectively. Since the spectra were taken directly after growth at RT, the reaction is still incomplete and thus all peaks feature a component at the BaO position. Nevertheless, the conclusion is still clear: $1.2 \cdot 10^{-8}$ torr is the optimum oxygen partial pressure for this growth rate. Decreasing the oxygen pressure results in a reduction of the main peak at the Si-O-Ba position and at the same time the Ba 3d peaks become more asymmetric similar to what was shown in Fig. 4.5, indicating an oxygen deficiency for silicate formation. Increasing the oxygen pressure only increases the concentration of O atoms in Si-O-Si and Ba-O-O bonding states, while the concentration of O atoms in Si-O-Ba bonding states stays

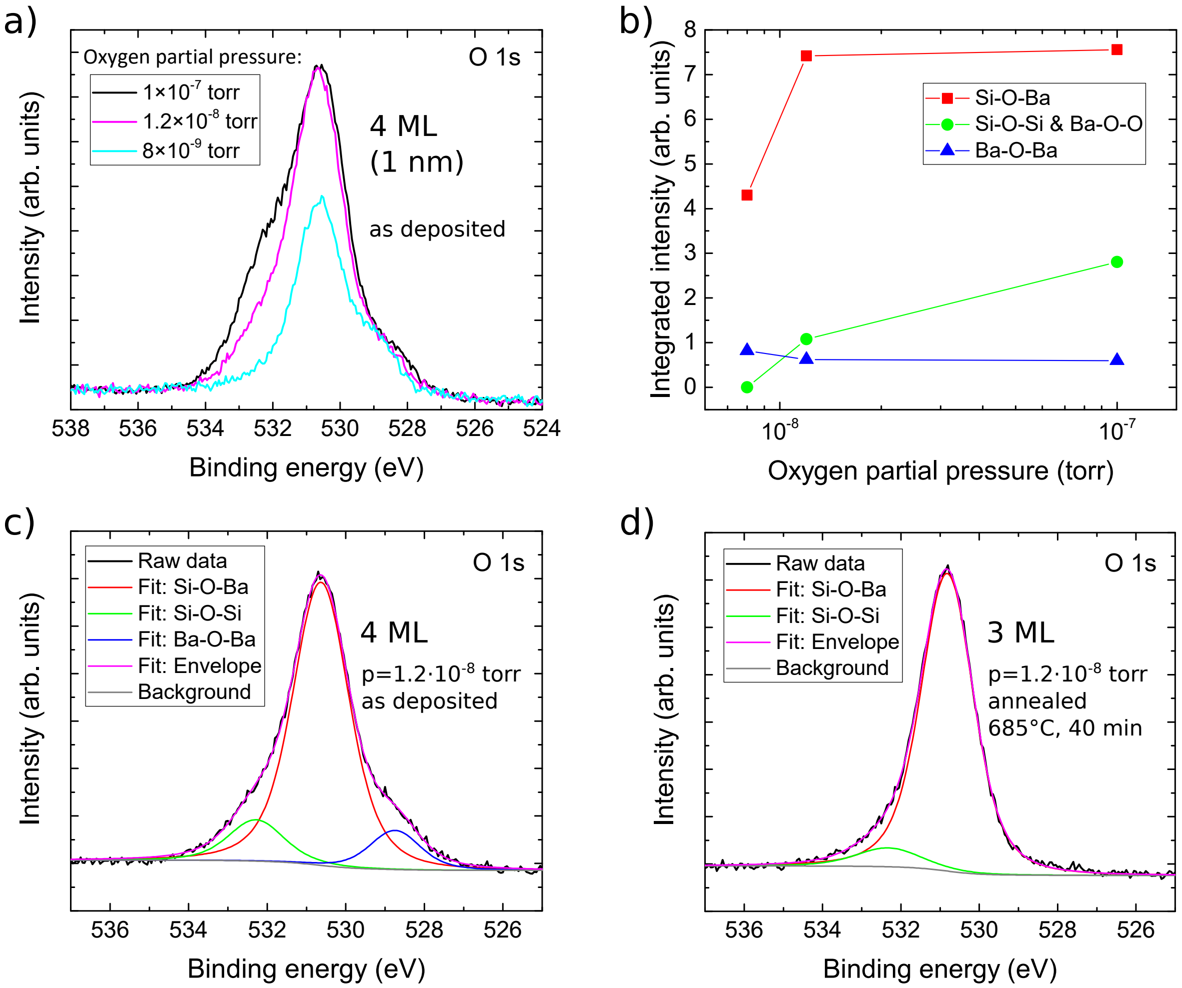


Figure 4.7.: Determination of the optimal oxygen background pressure: (a) XPS O 1s spectra for (approximately) 4 ML (1 nm) thick Ba-silicate layers grown with different oxygen background pressures at a rate of 1.1 ML/min. The spectra were taken directly after growth at room temperature. The Si/Ba ratio was kept at the optimal value as determined in the context of Fig. 4.6. (b) Integrated intensities of contributions from different chemical bonding states obtained from fits of the curves in a). (c) Example of the fit for the optimal oxygen partial pressure of $1.2 \cdot 10^{-8}$ torr. (d) O 1s peak after annealing the layer in c) to 685 °C for 40 min.

nearly constant, indicating an oxidation of the silicon surface and BaO_2 formation.

The O 1s peaks for a 4 ML film grown at optimum conditions before and after annealing at 685 °C for 40 min are shown in Figs. 4.7c) and d), respectively, together with the deconvolution into the individual components. During the annealing process, about 1 ML of the film was desorbed, as derived from the intensity of the Ba 3d and O 1s peaks in XPS, so that the 4 ML film was reduced to only 3 ML after annealing. Even after annealing, the O 1s peak of the now 3 ML thick film still shows a small concentration of O atoms in Si-O-Si bonding states, unlike the peak of the 63 ML (16 nm) film.

This concentration remains unchanged when the film is grown with a small Ba excess. Therefore, this signal is most likely due to interface bonds that are required between the film and the substrate, and is not due to defects. Assuming that the O atoms in Si-O-Si bonding states sit in the monolayer closest to the interface and that this layer has the same oxygen concentration as the overlying layers, the Si-O-Si signal corresponds to a concentration of 1/4 ML. In order to correct for the damping of the signal by the overlying layers an inelastic mean free path of 2.072 nm was used, which was calculated with the TPP-2M equation using the NIST Electron Inelastic-Mean-Free-Path Database [72].

4.6. Epitaxial growth of Ba_2SiO_4 films on Si(001)

The epitaxial growth of Ba_2SiO_4 films on Si(001) with stoichiometric Ba and Si fluxes is affected by two important parameters, the oxygen background pressure during growth and the annealing temperature. In general, the aim in the growth of epitaxial oxide films on silicon substrates is to avoid the formation of amorphous SiO_x at the silicon surface since it destroys the crystalline template required for the epitaxial growth [94]. Since no protection layer for the silicon surface is used in this work, such as the sub-monolayer Sr silicide for the growth of BaO or SrO [94, 6, 95, 96], a minimized oxygen background pressure, i.e. an oxygen background pressure just above the saturation point for complete oxidation as determined in the previous section, is required to minimize the formation of interfacial SiO_x. However, the epitaxial growth of Ba_2SiO_4 on Si(001) turned out to be rather robust, so that higher oxygen pressures while changing the stoichiometry at the interface do not immediately prevent the epitaxial growth, as will be discussed below.

Even if the Ba_2SiO_4 films are grown with a stoichiometric Ba:Si flux ratio in a minimized oxygen background pressure, an annealing step at high temperatures close to desorption is required to crystallize the films. The minimum temperature at which crystallinity was achieved is 640 °C, but the quality was still rather poor and most films even remained amorphous at this temperature. An annealing temperature of $670 - 690\,^{\circ}C$ produced the best and, most importantly, reproducible results. At these temperatures there was already a slight evaporation of the film, as mentioned in the previous section, which drastically increased at temperatures above 695 °C. This reduction in thickness was most evident for very thin films, while for more than 10 nm (40 ML) thick films the material loss during annealing was negligible. Only when the two conditions were fulfilled, a LEED pattern was observed, proving the film is crystalline.

The LEED image of the same 3 ML film whose O 1s peak is shown in Fig. 4.7d) is presented in Fig. 4.8a). The LEED pattern originates from the superposition of two rectangular domains rotated by 90°. Their reciprocal lattice constants are very close to one half and two thirds, respectively, of the reciprocal lattice constant of the unreconstructed Si(001) surface. Thus, they correspond to the two shorter real space lattice constants a and b of the Ba_2SiO_4 crystal structure, while the c-axis is oriented normal to the surface ($a = 7.51$ Å$, b = 5.81$ Å$, c = 10.21$ Å [55]). A schematic of this structure in reciprocal space is shown in Fig. 4.8b). The same structure was found by

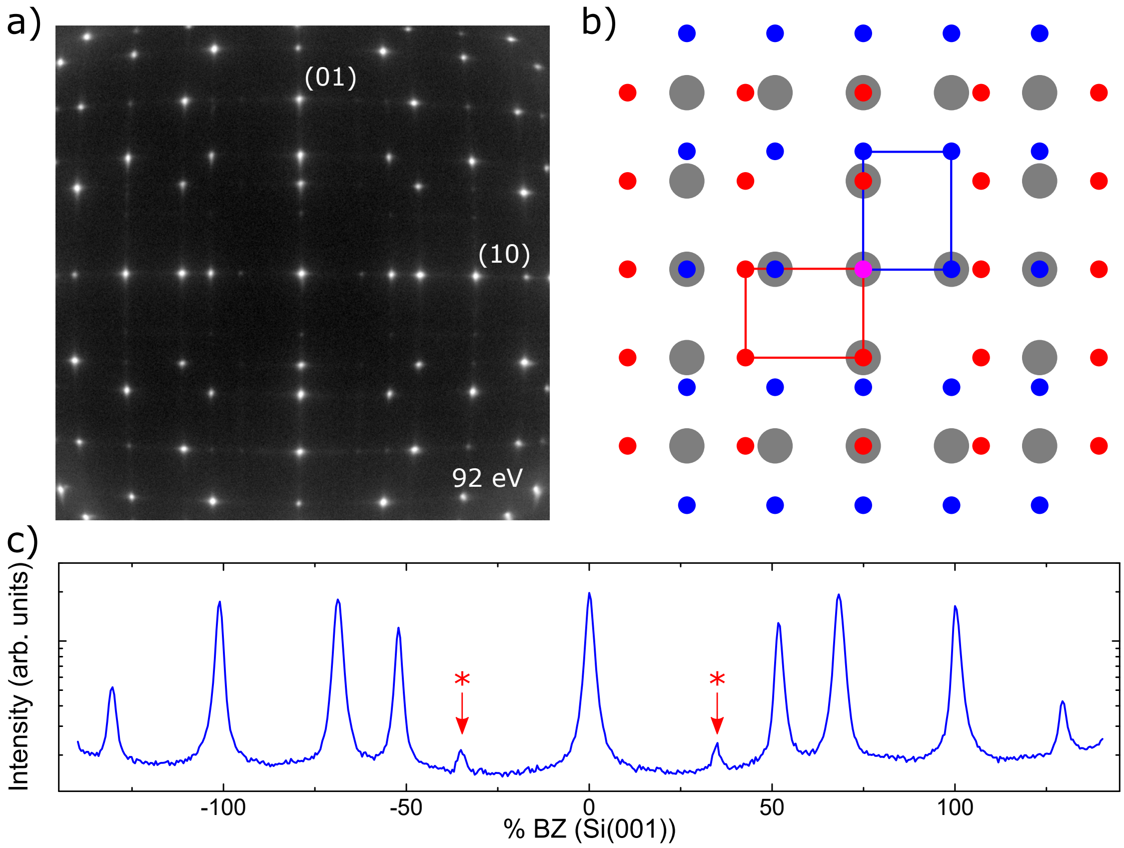


Figure 4.8.: LEED pattern of epitaxial Ba_2SiO_4: (a) LEED image of a 3ML film after annealing at 685 °C for 40 min taken at 92 eV. The film was grown at RT with a stoichiometric Si:Ba flux ratio (see Fig. 4.6) and a minimized oxygen pressure (see Fig. 4.7). (b) Schematic of this pattern with two orthogonal rectangular unit cells (red and blue dots), demonstrating epitaxial growth with axes a, b of the silicate $\parallel$ Si$[1\bar{1}0]$. Gray balls indicate the positions of the diffraction spots of the Si(001) substrate prior to silicate deposition. (c) Horizontal line scan through the center of a). Spots marked by $*$ are not indicated in b).

Islam et al. [1].

As seen from the line profile in horizontal direction through the center of Fig. 4.8a), shown in Fig. 4.8c), there are some less intense spots (marked with $*$), which correspond to a (2×3) structure. These can be explained by a modulation with twice the lattice constant in the b-direction close to the interface. Since the value of $2b$ is close to three times the silicon lattice constant, it is conceivable that the epitaxial growth leads to a doubling of the lattice constant in this direction close to the interface. This lattice modulation will be discussed in detail in section 4.10.

In the following the question why the high temperature annealing step is necessary for the formation of crystalline layers will be discussed. Even though no long range diffusion is necessary to form the silicate, since conditions very close to the perfect stoichiometry were chosen, the formation of crystalline layers still requires the same

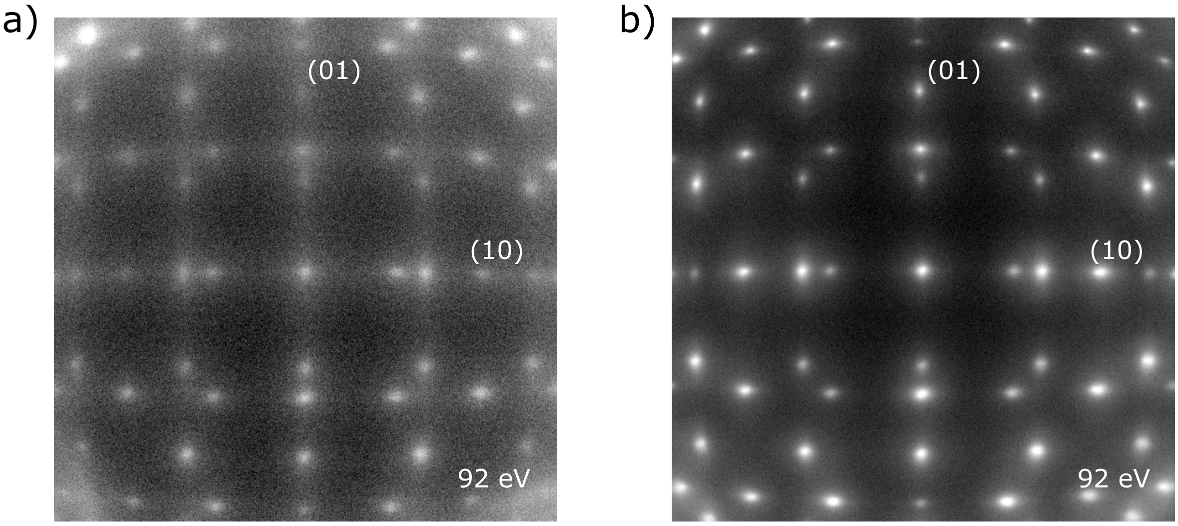


Figure 4.9.: Epitaxial growth of a 10 nm (40 ML) thick Ba_2SiO_4 film: The film was grown in two steps. First, a crystalline 3 ML film was grown by deposition at RT with a stoichiometric Si:Ba flux ratio in a minimized oxygen pressure and annealing at 685 °C for 40 min. The corresponding LEED image is shown in Fig. 4.8a). Second, the additional 37 ML were deposited at 400 °C again with a stoichiometric Si:Ba flux ratio and in a minimized oxygen pressure. The LEED images (a) directly after the second deposition step and (b) after an additional annealing step at 675 °C for 40 min are shown.

high temperature step as under conditions of silicate formation by Si diffusion [1]. It is clear from the LEED images that the crystallization has to start at the interface, since the film is perfectly aligned with the substrate and there is no rotational disorder. Moreover, when an additional 4 ML film is deposited on a crystalline 3 ML film, the film could already be crystallized by annealing to 400 °C. The crystalline quality was comparable to that of the initial film. This method was tested up to a combined thickness of 16 nm (63 ML) and crystalline layers were always obtained at 400 °C, though with slightly decreasing crystal quality for the thickest films as evident from the spot profile in LEED, which could be improved after annealing to higher temperature. As an example the LEED images of a 10 nm (40 ML) thick film directly after the second deposition step at 400 °C and after an additional annealing step at 675 °C are shown in Fig. 4.9. Consequently, the high annealing temperature is needed to form the epitaxial interface.

An adjustment of the stoichiometry at the interface cannot be the reason for the requirement of the high temperature, since Si is already sufficiently mobile at lower temperatures. As an example, the reaction of a 1 nm thick BaO film with Si from the substrate was investigated. Annealing at 400 °C for 30 min was sufficient to turn this film completely into silicate. Moreover, as shown in Fig. 4.10 even a 20 nm thick BaO film can be turned completely into Ba_2SiO_4 at a temperature, which is approximately 100 °C below the temperature needed to produce epitaxial Ba_2SiO_4 films.

The high temperature is also not needed to break the original (2×1) reconstruction

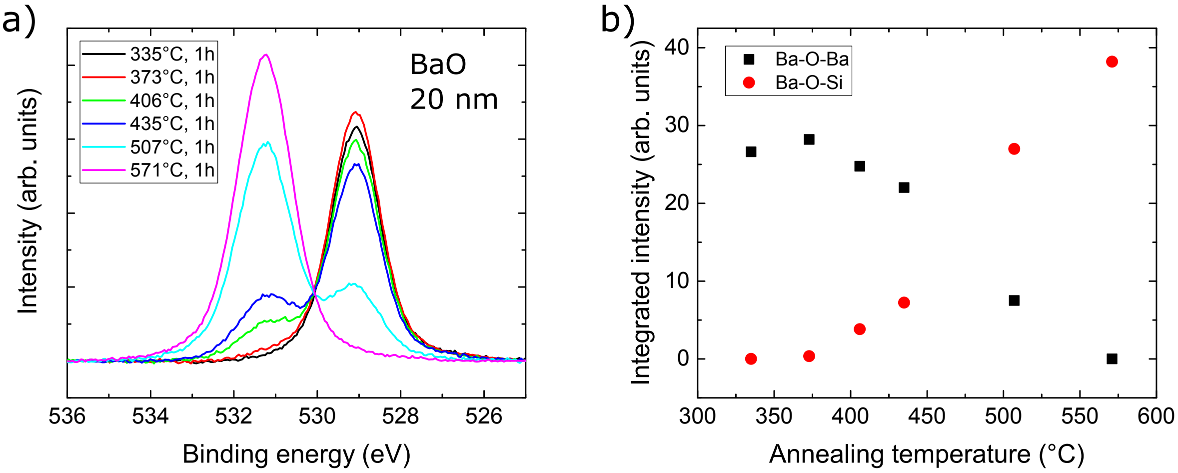


Figure 4.10.: Transformation of BaO into silicate by Si diffusion from the substrate: A 20 nm BaO film was grown at RT with a deposition rate of 1.1 ML/min (which corresponds to the Ba flux needed for 1.5 ML Ba_2SiO_4 per minute) in an oxygen background pressure of $5 \cdot 10^{-7}$ torr and subsequently annealed at 335 °C for 1 h to remove the BaO_2. The O 1s signal after each annealing step as indicated in the inset is shown in (a) and the corresponding integrated intensities of the individual components in dependence of the annealing temperature are shown in (b). The O 1s signals of the films annealed at $373 - 571$ °C were shifted by 0.39 ± 0.05 eV to be aligned with the peak of the film annealed at 335 °C. An annealing temperature of 571 °C, which is approximately 100 °C below the temperature needed to produce epitaxial Ba_2SiO_4 films, is enough to turn the BaO layer completely into Ba_2SiO_4.

of the Si(001) surface, since it is possible to produce crystalline films with an oxygen partial pressure during growth that is more than one order of magnitude above the saturation point (see Fig. 4.12 and the discussion below). In this case the (2×1) reconstruction at the interface is definitely destroyed, due to the oxidation of the Si(001) surface. However, the high temperature step is still needed to crystallize these films.

In order to understand the effect of the high temperature annealing step on the interface one monolayer of Ba was deposited on a Si(001) surface and oxidized it at 400 °C and subsequently annealed at increasing temperatures for 15 min per step. The corresponding O 1s peaks are shown in Fig. 4.11a). Directly after oxidation at 400 °C the O 1s peak consists of two components at the Si-O-Si and Si-O-Ba locations with a ratio of roughly 2:1. The annealing steps at 520 °C and 590 °C have no effect on the peak. At 640 °C the Si-O-Si component is already slightly reduced. At 680 °C the Si-O-Si component is reduced significantly, whereas the Si-O-Ba component is only slightly reduced. Finally, at 715 °C the oxygen is completely desorbed. Furthermore, a clean Si(001) surface was oxidized at RT in an oxygen partial pressure of $5 \cdot 10^{-7}$ torr for 2 min and subsequently annealed at increasing temperatures for 20 min per step. The O 1s peaks after oxidation and after each annealing step are shown in Fig. 4.11b). Again, temperatures of up to 600 °C are too low to remove the oxygen. Only at 670 °C

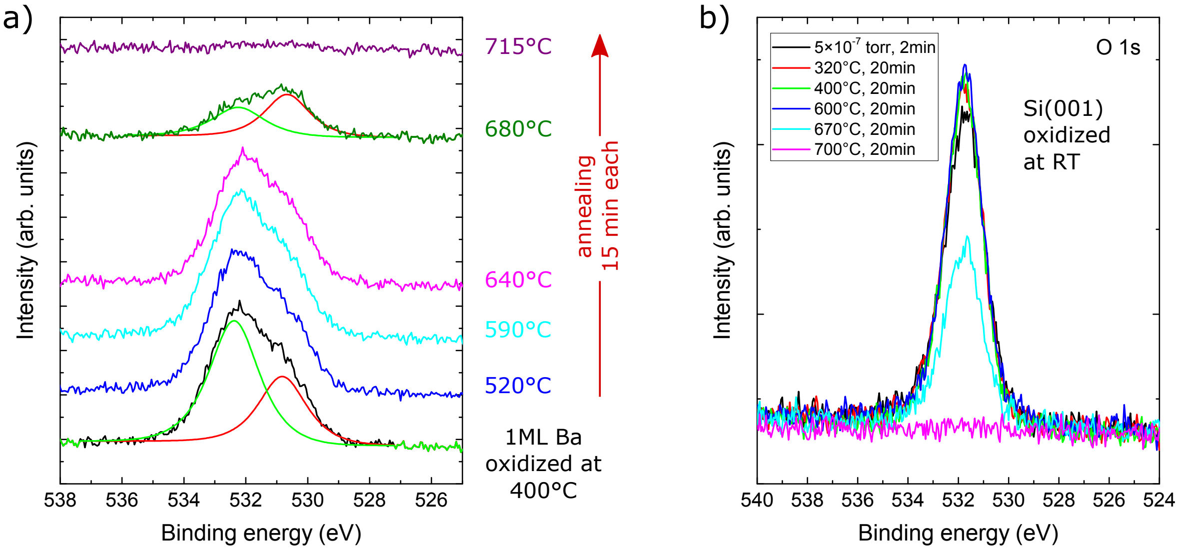


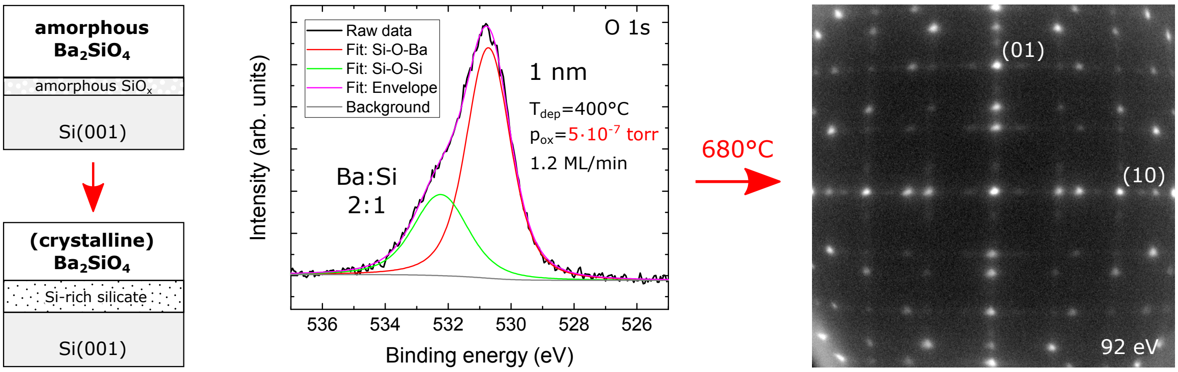
Figure 4.11.: Effects of high temperature annealing on the interface: (a) A 1 nm thick Ba film on Si(001) was oxidized in an oxygen partial pressure of $5 \cdot 10^{-8}$ torr for 10 min at 400 °C and subsequently annealed at increasing temperatures for 15 min per step. The O 1s spectra after oxidation and after each annealing step are shown. For the spectra after oxidation and after annealing to 680 °C the deconvolution into the individual components (Si-O-Si green, Si-O-Ba red) is also shown. The spectra were shifted for better visibility. (b) A clean Si(001) surface was oxidized in an oxygen partial pressure of $5 \cdot 10^{-7}$ torr for 2 min at RT and subsequently annealed at increasing temperatures for 20 min per step. Beginning at 670 °C the oxygen is slowly removed.

the oxygen is slowly removed. The complete removal of the oxygen at 700 °C was combined with a restoration of the (2×1) reconstruction of the Si(001) surface.

The temperature range at which the Si-O-Si peak is reduced lines up perfectly with the temperatures needed for the crystallization of the Ba_2SiO_4 films. In particular, the temperature at which the reduction of the Si-O-Si peak sets in, is exactly the lowest temperature at which crystallization was observed. Moreover, annealing a 1 nm thick Ba_2SiO_4 film at 680 °C reduces the Si-O-Si proportion of the O 1s peak by about 50% as compared to only annealing it at 640 °C. These findings indicate that the high temperatures required for the formation of the epitaxial interface are needed to break interfacial Si-O bonds for O atoms with two bonds to Si, i.e. while the formation of three dimensional SiO_2 can be prevented by the minimization of the oxygen background pressure, the oxidation of the topmost substrate layer could not be avoided even with a minimized oxygen pressure and by starting with an amorphous monolayer of Ba (epitaxial sub-monolayer silicide was not tested). Further details of the effect of the high temperature annealing step on the topmost substrate layer will be discussed at the end of section 4.10.

Returning to the oxidation of the Si surface due to a high oxygen pressure and its effect

a) Growth with stoichiometric fluxes in a high oxygen pressure



b) Scavenging of interfacial SiO_x by reducing the Si flux

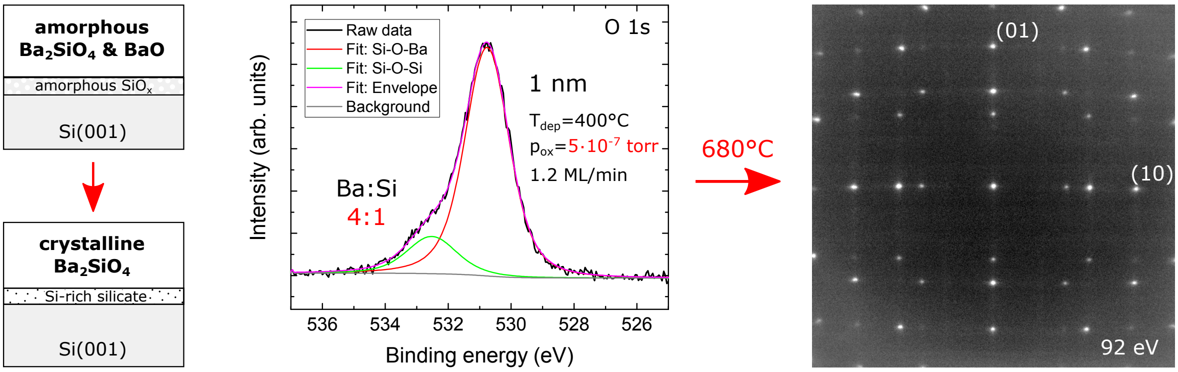


Figure 4.12.: Robustness of the epitaxial growth of Ba_2SiO_4 on Si(001): 1 nm thick Ba_2SiO_4 films were grown in an oxygen background pressure of $5 \cdot 10^{-7}$ torr at a deposition rate of 1.2 ML/min and a substrate temperature of 400 °C with (a) a stoichiometric Si:Ba flux ratio and (b) a Si flux reduced by half. Shown are an illustration of the stack cross-section (left), the O 1s spectra after deposition (middle) and the LEED images after annealing at 680 °C for 40 min (right). Due to the high oxygen pressure a Si-rich silicate layer, i.e. a silicate layer with a higher Si concentration than Ba_2SiO_4, is formed at the interface. However, it does not hinder the epitaxial growth and its thickness can be reduced by lowering the Si flux during growth.

on the epitaxial growth of Ba_2SiO_4 on Si(001), as stated at the beginning of this section, the epitaxial growth turned out to be rather stable. Fig. 4.12a) shows the results of the epitaxial growth of a 1 nm film with a stoichiometric Si:Ba flux ratio in an oxygen partial pressure of $5 \cdot 10^{-7}$ torr at a deposition rate of 1.2 ML/min. The oxygen pressure is approximately 40 times higher than the saturation point determined in section 4.5. In a simple model, as illustrated on the left side of the figure, the high oxygen pressure leads to the formation of amorphous SiO_x at the silicon surface. This SiO_x layer reacts with the silicate layer, since silicate formation is always thermodynamically favorable to keeping SiO_2 in the system [18]. Because the silicate layer is already perfectly stoichiometric Ba_2SiO_4, the reaction with the interfacial SiO_x layer has to result in the formation of an interfacial silicate layer with a higher Si concentration than Ba_2SiO_4 (Si-rich silicate). Note that this description is somewhat idealized insofar as that the oxidation of the Si surface and the reaction with the silicate are not necessarily clearly separable steps, especially if, as is the case here, the films are deposited at a substrate temperature of 400 °C. The formation of the Si-rich silicate is indicated by the large Si-O-Si component of the O 1s signal in Fig. 4.12a), whose integrated intensity is approximately 5.6 times higher than in the case of a minimized oxygen pressure (Fig. 4.7d)). If the Si-rich silicate layer becomes too thick, it is expected to inhibit the epitaxial growth of Ba_2SiO_4, since the crystal structures of the barium silicate compounds with a higher Si concentration than Ba_2SiO_4 do not match to Si(001). Nevertheless, even under the conditions in Fig. 4.12a) the Ba_2SiO_4 LEED pattern is still observed after an annealing step at 680 °C for 40 min demonstrating the robustness of the epitaxial growth of Ba_2SiO_4 on Si(001). The LEED pattern of the bulk structure is, however, superimposed with a (2×6) minority structure, which is most likely due to an interface layer containing SiO_4-tetrahedra that are connected to at least one other SiO_4-tetrahedron by an O-bridge. At an energy of 70 eV only the four spots of the (2×6) structure around the (00)-spot were visible in LEED, which were also observed by Islam [89]. The annealing process only marginally reduces the integrated intensity of the Si-O-Si component of the O 1s signal by approximately 15%.

The concentration of O atoms in Si-O-Si bonding states can be reduced by reducing the Si flux during the film growth. Fig. 4.12b) shows the results of the growth with the same parameters as in Fig. 4.12a), except that the Si flux was reduced by half. Since Ba_2SiO_4 is already the barium silicate compound with the highest Ba concentration, the Ba surplus leads to the formation of BaO, which reacts with the interfacial SiO_x to Ba_2SiO_4 reducing the thickness of the interfacial Si-rich silicate layer. The integrated intensity of the Si-O-Si component of the O 1s signal is reduced by approximately 50% as compared to the growth with a stoichiometric Si:Ba flux ratio. This is effectively a scavenging technique to remove the interfacial oxide layer. However, unlike conventional scavenging techniques no unwanted sacrificial layer is created [12], since the reaction product is the desired high-k material itself. Furthermore, the (2×6) structure that was present in the LEED pattern of the film grown with a stoichiometric Si:Ba flux ratio is gone. There are even indications of the (2×3) structure that was observed for the film grown with a minimized oxygen pressure (Fig. 4.8), i.e. next to the (01)-spot. The films grown in a high oxygen pressure needed the same high temperature annealing step at around 680 °C in order to crystallize as the films grown with a minimized oxygen pressure.

The growth of Ba_2SiO_4 by Si diffusion from the substrate into an adsorbed BaO layer [1] can be viewed as the extreme case of the scavenging technique. If no oxygen is supplied during the annealing process, the bottleneck for silicate formation under these conditions is the concentration of O atoms, since there is a Ba surplus (BaO contains twice as many Ba atoms per O atom as Ba_2SiO_4), and Si can be supplied virtually unlimited by the substrate. The leftover Ba atoms are evaporated. Under these conditions an oxidation of the substrate surface might actually be beneficial as long as the atomic ratio of Si:Ba in the overall system is at a maximum 1:2, since it brings the system closer to stoichiometric conditions. The loss of the crystalline template due to the oxidation of the substrate surface is not a problem in this case, because the final interface between the silicate and the silicon ends up being at a lower level than the original silicon surface due to the reaction of the BaO layer with the substrate. As long as the final interface is at a level where the substrate is still crystalline, epitaxial growth is possible.

4.7. Formation of interfacial sub-monolayer silicide due to Ba surplus

The reaction of BaO with the Si substrate to Ba_2SiO_4 leads to leftover Ba if no additional oxygen is supplied. While most of it is evaporated, a small proportion might also penetrate into the substrate. Indeed, after annealing films that are a mixture of Ba_2SiO_4 and BaO, which causes the BaO to react with the Si substrate and crystallizes the film, an additional (4×2) minority structure corresponding to sub-monolayer Ba silicide near the Si surface [97] is observed in LEED. It was not observed for the film in Fig. 4.12b), since due to the oxidation of the interface there was actually a Ba *deficiency* in the system as evident from the large Si-O-Si component of the O 1s signal. In contrast, all films in this section were grown in a minimized oxygen pressure.

4 ML (1 nm, given as the necessary Ba amount) films were grown at RT with a reduced Si flux of $x = 0.37$, 0.57, 0.81 and 1 times the flux needed for the exact stoichiometry of Ba_2SiO_4. As expected, the O 1s peaks of the Si deficient layers (not shown here) show a larger BaO fraction than the stoichiometric film that increases with decreasing x. After annealing at 685 °C for 40 min all films turned completely into silicate due to Si diffusion from the substrate. While the thickness of all films was reduced during the annealing, the reduction in thickness increased with increasing Si deficiency. This is due to the lower initial amount of O atoms per Ba atom in the thinner films which increases the amount of Ba desorbed during annealing (there was no oxygen background pressure during annealing). The thicknesses of the films after annealing were 1.6, 2.3, 2.5 and 3 ML for $x = 0.37$, 0.57, 0.81 and 1, respectively, as derived from the Ba 3d and O 1s peaks in XPS.

The LEED images for $x = 0.37$ and 0.81 as well as the line scans through the (00) and (10) spots after annealing for all films are shown in Fig. 4.13. The varying concentrations of Si relative to Ba do not suppress the formation of crystalline silicate layers. The interesting part, however, is the appearance of a faint, but quite sharp (4×2) structure for $x < 1$ that is assigned to the formation of a sub-monolayer Ba silicide close to the Si surface, following Ref. [97]. The high intensity of the (4×2)-peaks for $x = 0.37$ is most likely due to the smaller film thickness. The absence of the (4×2) structure for $x = 1$, however, seems to be real, since the presence of the (2×3) structure (spots marked with $*$) associated with the epitaxial interface means that the interface is still visible in LEED at this thickness. Moreover, neither a (4×2) structure nor Ba diffusion into the substrate was observed in STEM, see section 4.9. Therefore, the appearance of the (4×2) structure seems to be coupled with a surplus of Ba or BaO in the insulator film. While most of the Ba desorbs during the annealing process, there is

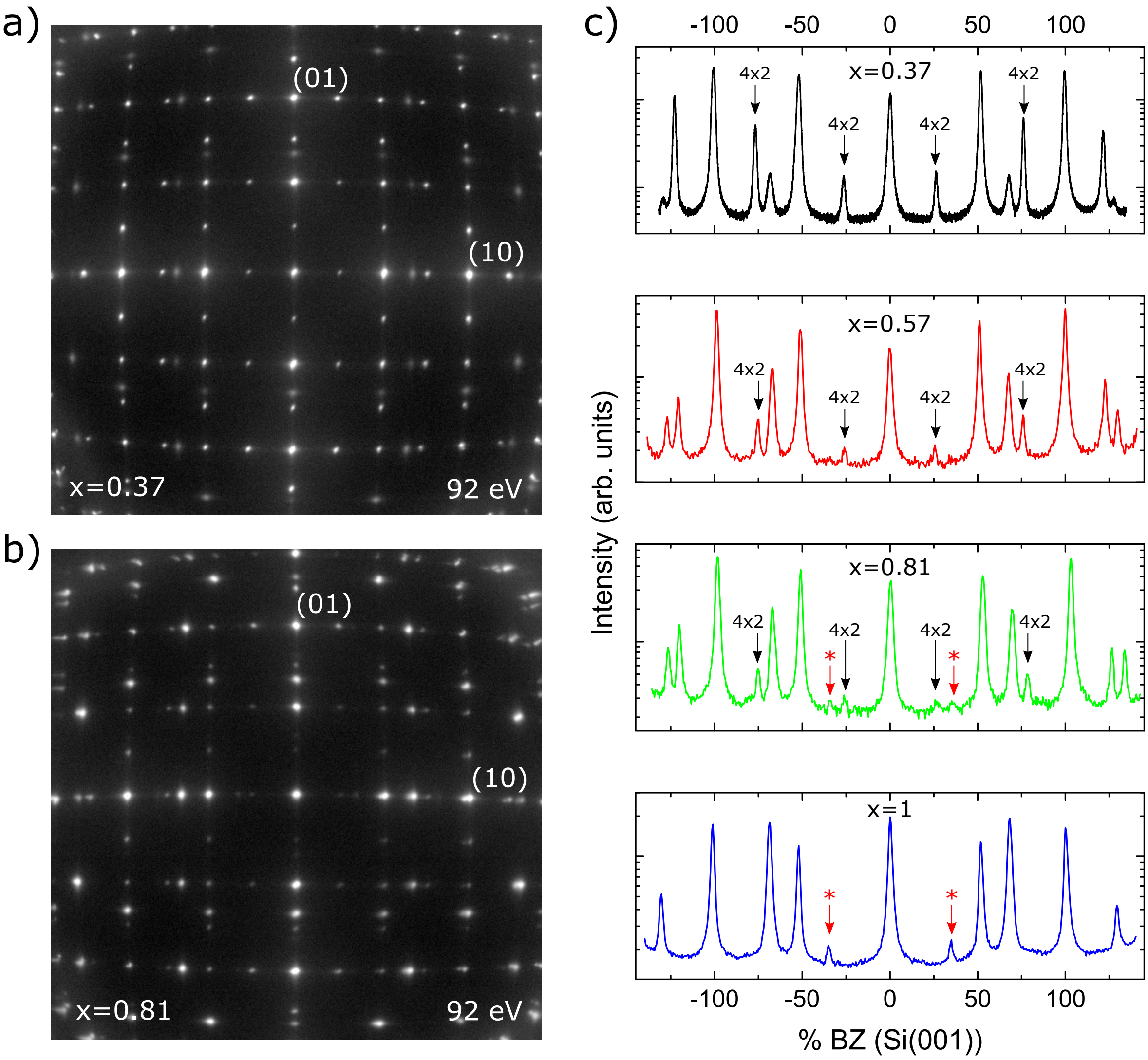


Figure 4.13.: Effect of an under-stoichiometric Si flux on the interface: 4 ML (1 nm, given as the necessary Ba amount) films were grown with a reduced Si flux at a minimized oxygen pressure ($1.2 \cdot 10^{-8}$ torr, 1.1 ML/min) and subsequently annealed to 685 °C. x denotes the normalized Si flux, with $x = 1$ corresponding to the flux needed for the exact stoichiometry of Ba_2SiO_4. The LEED images for $x = 0.37$ and 0.81 are shown in (a) and (b), respectively. The horizontal line scans through the center of the LEED patterns for $x = 0.37$, 0.57, 0.81 and 1 are shown in (c).

also the possibility of diffusion of Ba to the Si interface and the subsequent formation of silicide [97, 98, 99].

These results again show the robustness of the epitaxial growth of Ba_2SiO_4 on Si(001), since a sharp (2×1.5) structure appears under all conditions in LEED. Only the (2×3) structure disappears for $x = 0.57$ and 0.37 indicating that the silicide distorts the period doubling at the interface. This does not necessarily mean that the local structure is changed. Only long range order is distorted.

4.8. Si 2s and Si 2p and their deconvolution into silicate and substrate contributions

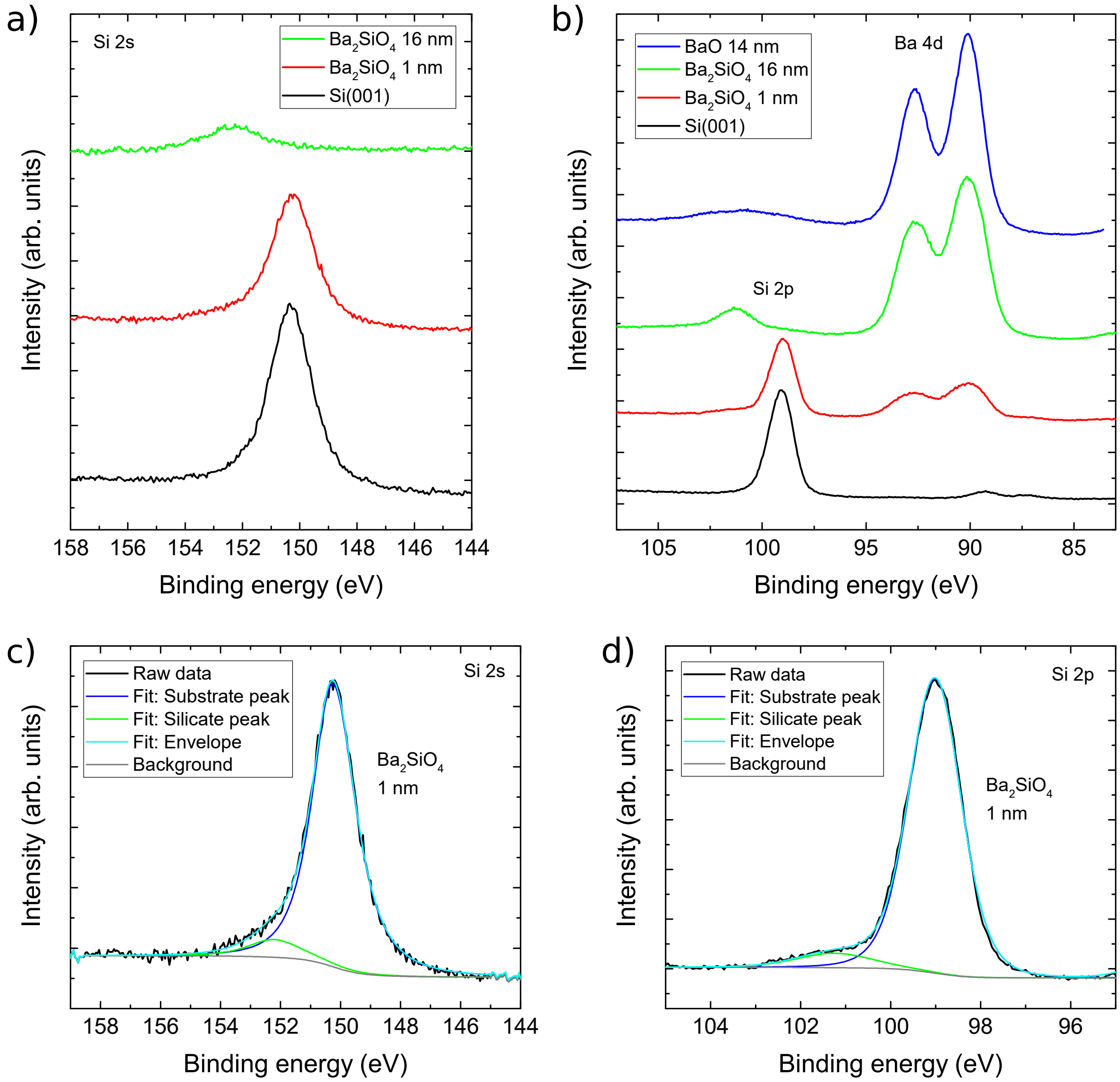


Figure 4.14.: (a) Si 2s and (b) Si 2p and Ba 4d XPS signals of differently prepared samples are compared. They are shifted in intensity for better visibility. Moreover, the measurement of the 16 nm Ba_2SiO_4 (green) was shifted in energy by -0.74 eV and the measurement of the 14 nm BaO film (blue) was shifted in energy by $+1.59$ eV in order to align the positions of the Ba 4d peaks with the 1 nm Ba_2SiO_4 film. The deconvolution into silicate and substrate contributions of the Si 2s and Si 2p signals of the 1 nm Ba_2SiO_4 film are shown in (c) and (d), respectively. The Ba_2SiO_4 films were grown in an oxygen pressure of $1.2 \cdot 10^{-8}$ torr with a rate of 1.1 ML/min and annealed at 680 °C for 40 min. The BaO film was grown in an oxygen pressure of $5 \cdot 10^{-7}$ torr with a rate of 1.1 ML/min and annealed at 335 °C for 15 min.

The Si 2s and Si 2p signals are shown in Figs. 4.14a) and b), respectively, for a 16 nm thick Ba_2SiO_4 film (green line), a 1 nm thick Ba_2SiO_4 film (red line) and the bare Si(001) surface (black line). The Ba_2SiO_4 films were grown in an oxygen pressure of $1.2 \cdot 10^{-8}$ torr with a rate of 1.1 ML/min, i.e. a minimized oxygen pressure (see section 4.5) and annealed at 680 °C for 40 min. The BaO film was grown in an oxygen pressure of $5 \cdot 10^{-7}$ torr with a rate of 1.1 ML/min and annealed at 335 °C for 15 min in order to remove the BaO_2 (see section 4.3). In the case of the 16 nm thick Ba_2SiO_4 film, the Si signals come exclusively from the silicate layer, i.e. the substrate is invisible. They have a relatively low intensity. Compared to the O 1s peak, the intensity of the Si 2p (Si 2s) peak of the silicate is approximately a factor of 13 (11.3) lower. This is partially due to the atomic ratio of Ba_2SiO_4 (O : Si = 4 : 1) and partially due to the sensitivity of the XPS (RSFs: O 1s = 2.77, Si 2p = 0.85, Si 2s = 0.98 for the SPECS XPS used in this work).

In the measurement of the 1 nm thick Ba_2SiO_4 film the substrate peaks are still visible and they overshadow the silicate peaks, which appear as shoulders of the substrate peaks towards high binding energies. The deconvolution of the Si 2s and Si 2p signals into silicate and substrate contributions are shown in Figs. 4.14c) and d), respectively. In order to correctly determine the silicate contributions, line shapes that perfectly fit to the measurements of the bare Si(001) surface were carefully chosen for the fit functions. With respect to the substrate peaks, the silicate peaks is shifted by approximately 2.2 eV towards higher binding energies. Compared to the Si 2p peak, the flanks of the Si 2s peak decline more slowly, making the Si 2s silicate peaks harder to detect. On the other hand, the satellite features of the Ba 4d doublet peak, which is right next to the Si 2p peak, overlap with the Si 2p peak. The satellite features can be seen in the measurement of the 14 nm BaO film (blue line in Fig. 4.14b)). They are flat enough, so that they don't impede the analysis of the Si 2p silicate peak too much. However, they have to be considered when studying the oxidation states at the interface [95]. Moreover, due to these complications is not feasible to gain information about the composition of the interface from the Si peaks in XPS.

4.9. Cross-sectional STEM measurements

Cross-sectional high-angle annular dark field (HAADF) z-contrast scanning transmission electron microscopy (STEM) images were recorded in the Ernst Ruska-Centre for Microscopy and Spectroscopy with Electrons, Forschungszentrum Jülich by Prof. Dr. Knut Müller-Caspary. The images were taken from an 11 nm (44 ML) Ba_2SiO_4 film, which was prepared in two steps: First, a 1 nm (4 ML) film was deposited at RT with a stoichiometric Si:Ba flux ratio in an oxygen background pressure of $1.2 \cdot 10^{-8}$ torr at a deposition rate of 1.1 ML/min, i.e. the oxygen pressure was minimized, and crystallized by annealing at 680 °C for 40 min. Second, the remaining monolayers were deposited with the same parameters. The film was then annealed again at 680 °C for 40 min. The lamellae were cut along the Si(110) plane. As expected from the LEED results (Fig. 4.8) two orientations of Ba_2SiO_4 are observed, the a, c-projection shown in Fig. 4.15 and the b, c-projection shown in Fig. 4.16. The Ba atoms are clearly visible as

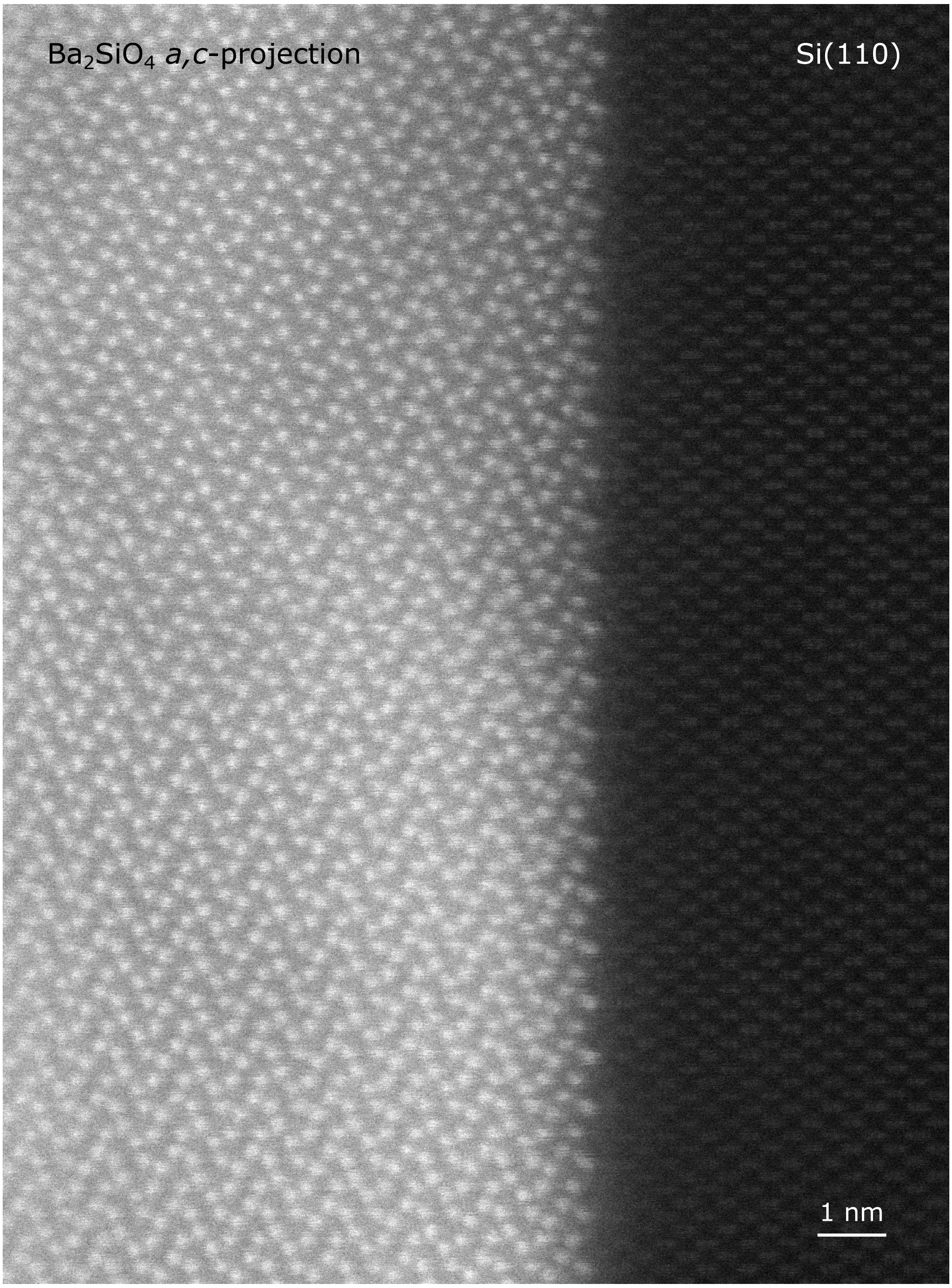


Figure 4.15.: High-angle annular dark field (HAADF) z-contrast STEM image of the a, c-projection of the Ba_2SiO_4 crystal structure (left side) and the interface to Si(001). The bright spots are Ba atoms. The right side of the image shows the Si(110) plane. The image was taken from an 11 nm Ba_2SiO_4 film grown in a minimized oxygen pressure (for the details of the preparation see the text). The Ba_2SiO_4 layer has a very regular structure, which is best seen from a low viewing angle. The interface between Ba_2SiO_4 and Si(001) is atomically sharp.

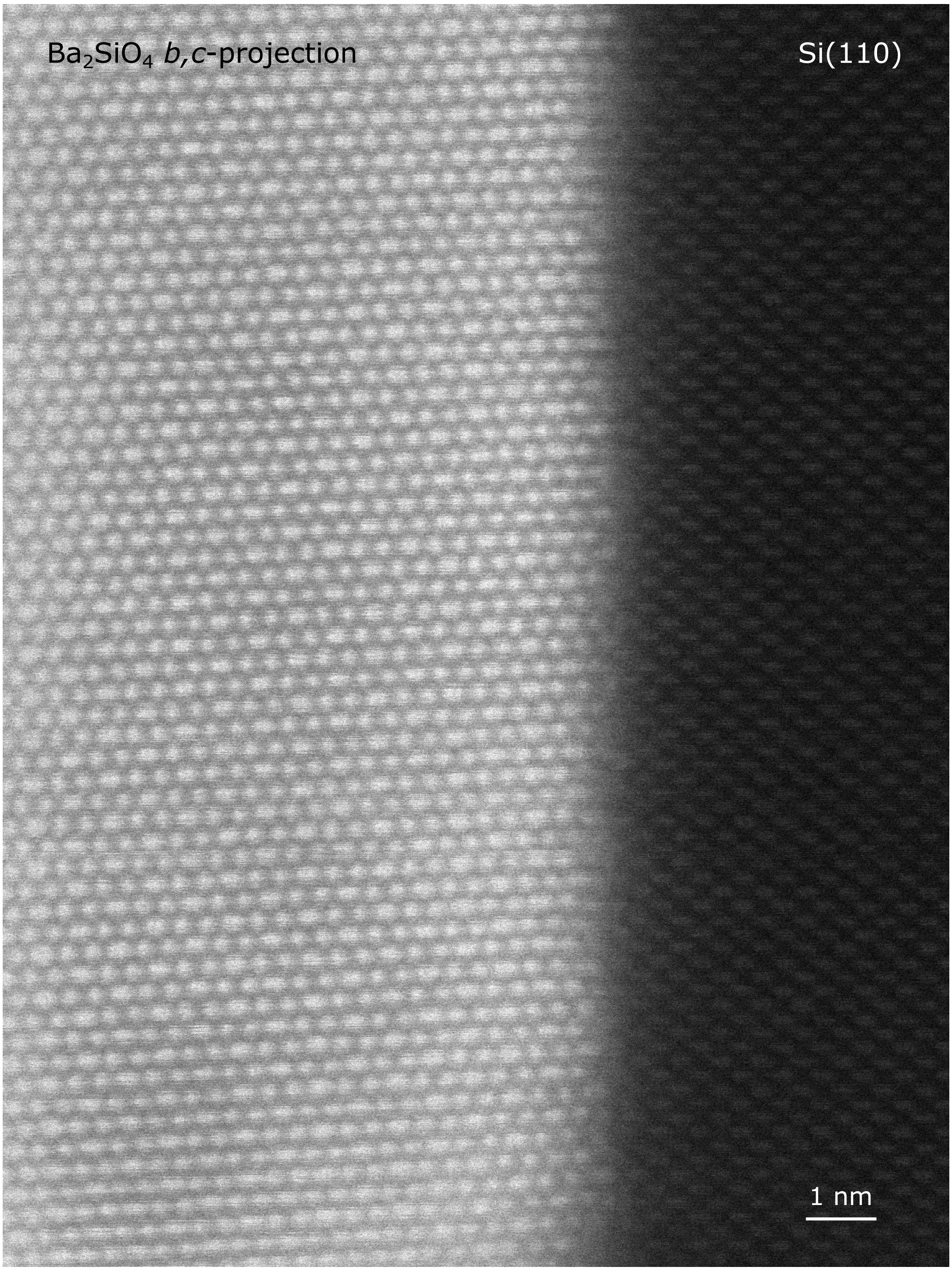


Figure 4.16.: High-angle annular dark field (HAADF) z-contrast STEM image of the b, c-projection of the Ba_2SiO_4 crystal structure (left side) and the interface to Si(001). The bright spots are Ba atoms. The right side of the image shows the Si(110) plane. The image was taken from an 11 nm Ba_2SiO_4 film grown in a minimized oxygen pressure (for the details of the preparation see the text). In the position where the image was taken, the c-axis of the Ba_2SiO_4 layer is tilted by approximately 4° from the surface normal.

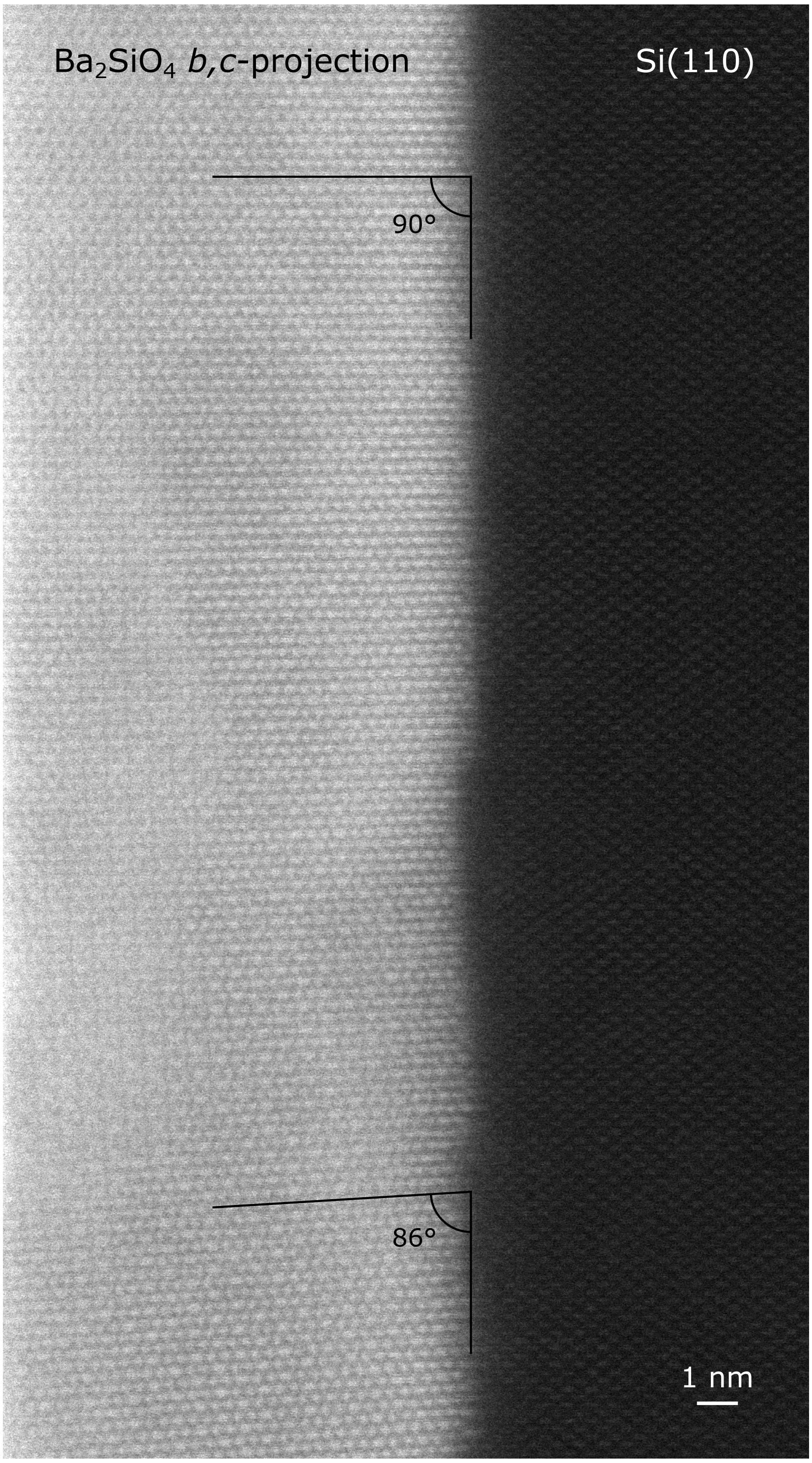


Figure 4.17.: High-angle annular dark field (HAADF) z-contrast STEM image of the b, c-projection of the Ba_2SiO_4 crystal structure (left side) and the interface to Si(001). The bright spots are Ba atoms. The right side of the image shows the Si(110) plane. The image was taken from an 11 nm Ba_2SiO_4 film grown in a minimized oxygen pressure (for the details of the preparation see the text). A transition from a growth with the c-axis of the Ba_2SiO_4 layer normal to the Si(001) surface (top) to a tilted growth (bottom) is seen. It is correlated with steps at the interface.

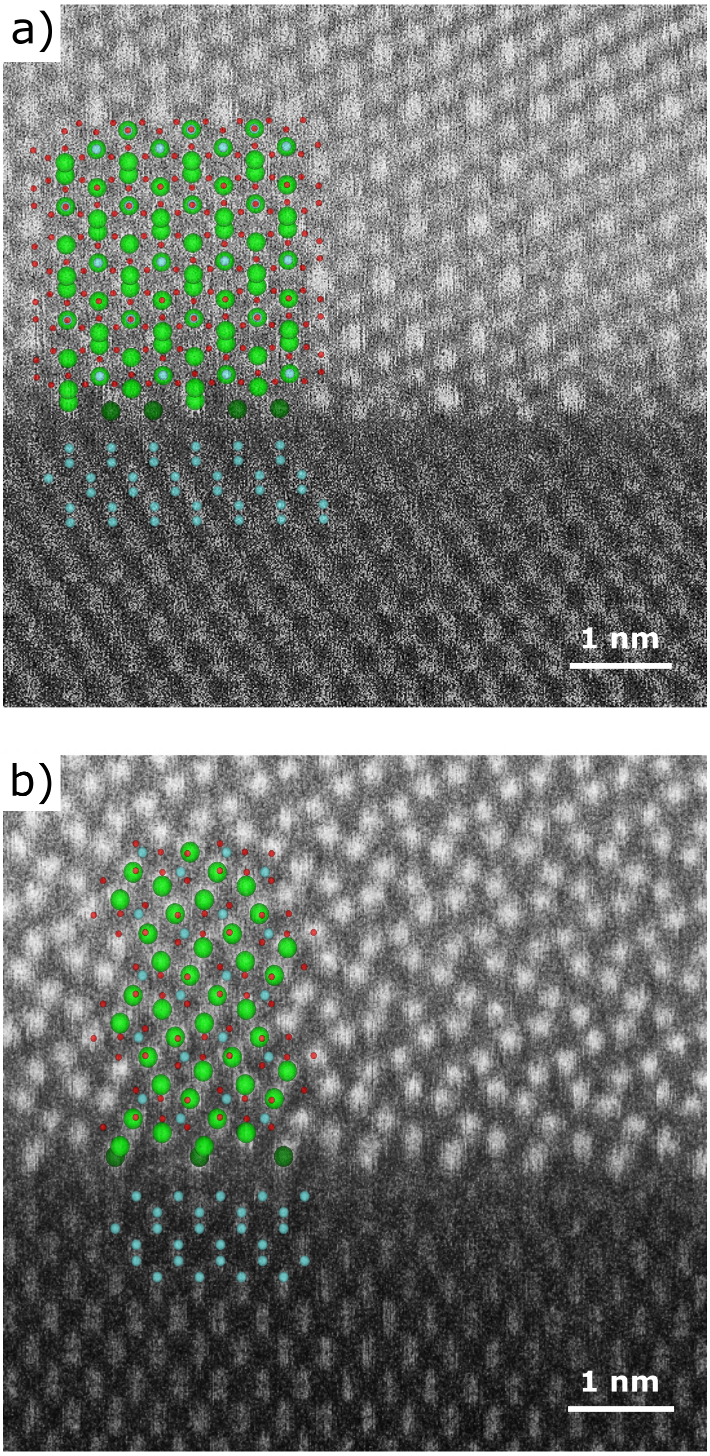


Figure 4.18.: Ba_2SiO_4 crystal structure overlaid on the HAADF z-contrast STEM images: (a) b, c-projection and (b) a, c-projection of Ba_2SiO_4. The bright spots are Ba atoms. The bottom of both images shows the Si(110) plane. The Ba_2SiO_4 film was grown with a minimized oxygen pressure (see section 4.9 for the details of the preparation). The crystal structures were drawn with VESTA [50] based on Refs. [51] and [100]. Green: Ba, blue: Si, red: O. The Ba atoms at the interface that deviate from the Ba_2SiO_4 bulk structure are depicted in dark green.

bright spots. On the other hand, the Si and O atoms are not visible within the silicate layer due to their low atomic number compared to Ba. The measurements confirm that the interface between the crystalline Ba_2SiO_4 and Si(001) is atomically sharp.

Whereas in the a, c-projection in Fig. 4.15 the c-axis of Ba_2SiO_4 is perfectly perpendicular to the Si(001) surface, it is off by approximately 4° in the b, c-projection in Fig. 4.16. This tilted growth was only observed in the b, c-projection. In Fig. 4.17 a gradual transition from a growth with the c-axis perpendicular to the Si(001) surface to a growth with the c-axis in an 86° angle to the Si(001) surface is observed. The transition is correlated with a step in the Ba_2SiO_4 at the interface. This is either due to the overgrowth of a step in the Si surface that was already there before the deposition, which leads to a tilt in the silicate since the Ba_2SiO_4 layer height does not match the Si step height, or it is a mechanism to release stress due to the lattice constant of Ba_2SiO_4 in a-direction not perfectly matching the periodicity of the Si(001) surface.

4.10. The epitaxial interface between Ba_2SiO_4 and Si(001)

In Fig. 4.18 the Ba_2SiO_4 crystal structure was overlaid on the STEM results (see previous section for details) by matching the Ba atoms with the bright spots. Note that the measured film was grown with a minimized oxygen pressure. Therefore, the following results are for this type of films. The Ba_2SiO_4 bulk structure fits the measurement up to the penultimate monolayer, neglecting relaxations of the crystal structure. Only in the monolayer closest to the interface the positions of some of the Ba atoms had to be changed in order to fit the measurement. These Ba atoms are depicted in dark green in the overlaid crystal structures. This means that only one monolayer at the interface is geometrically modified, in order to form the bonds to the Si(001) substrate, neglecting small relaxations of the atoms.

Fig. 4.19 serves to illustrate how the lattice matching is be achieved. It compares a silicate layer with the Ba_2SiO_4 bulk structure (a) to the modified interface layer (b). Both are on top of unreconstructed Si(001) for reference. Depicted are only the Ba atoms of the silicate layers (green and gray) as well as the Si atoms of the first two layers of the substrate (blue) in a top view (a, b-projection) as well as the two side views (a, c- and b, c-projections). In order to derive the interface layer from the bulk structure, the gray Ba atoms are removed and the dark green Ba atoms are moved in the ab-plane. The light green Ba atoms remain in their original position. Hence, the Ba content of the interface layer is reduced by one forth as compared to the bulk structure. Moreover, the rearrangement of the Ba atoms results in a period doubling in b-direction as compared to the Ba_2SiO_4 bulk structure. This matches the (2×3) structure observed in LEED (see Fig. 4.8) and confirms that this structure is indeed a result of a lattice modulation at the epitaxial interface required for the lattice matching. By the rearrangement a pseudo 1:1 matching with the Si substrate is achieved in b-direction, where a Ba atom sits above every Si row with every third one being slightly elevated. In a-direction the Ba atoms sit in between the topmost Si atoms in every

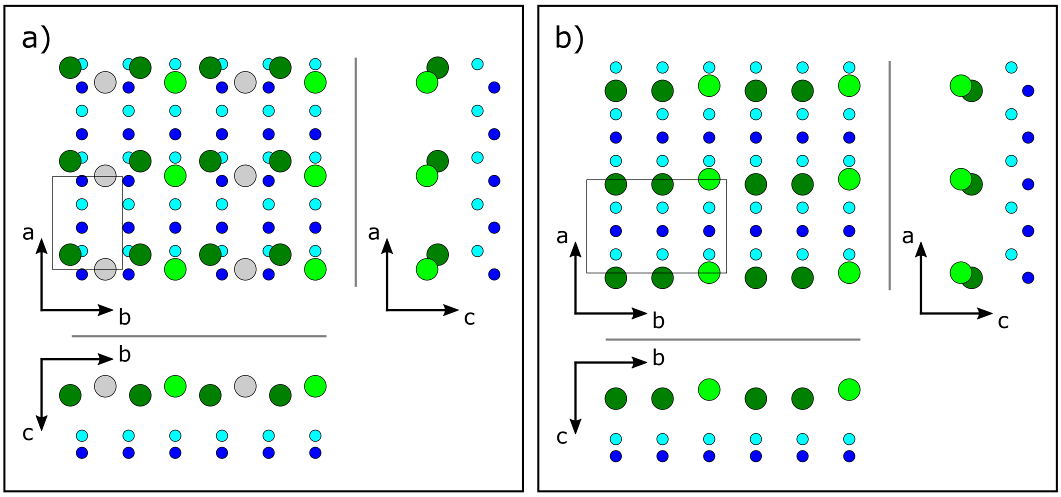


Figure 4.19.: Lattice matching: The Ba atoms (green and gray) of (a) one monolayer with the Ba_2SiO_4 bulk structure and (b) the lattice matched interface layer as determined in Fig. 4.18 are shown on top of the Si(001) surface (light blue: 1st layer, dark blue: 2nd layer). The boxes mark the unit cells of the silicate layers. To form the lattice matched interface layer the gray Ba atoms are removed and the dark green Ba atoms are moved in the *ab*-plane. The light green Ba atoms remain at their original positions.

other Si unit cell, so that the lattice matching between the reconstructed silicate layer and the Si(001) surface is 2:1.

Based on the information from STEM, XPS and LEED, as well as the typical Ba-O and Si-O bond lengths in barium silicates and the chemical boundary conditions that Ba atoms are divalent and that the Ba-O bonds are ionic, a plausible model of the interface was designed, which is depicted in Fig. 4.20. The model has six O atoms per unit cell in Si-O-Ba bonding states in the interface layer. The topmost substrate layer exhibits a pseudo-(2×1) reconstruction, which is similar to the typical (2×1) reconstruction of the Si(001) surface, but in two out of three (2×1) unit cells one Si atom is raised by an O-bridge, resulting in a (2×3) periodicity which matches the periodicity of the silicate interface layer. The pseudo-(2×1) reconstruction is best visible in the 3D view. The O-bridges are necessary to raise the Si atoms so that the other O atoms bound to these Si atoms can form ionic bonds with the Ba atoms in the second silicate layer, while staying within the typical silicate bond lengths. The O-bridges result in a concentration of O atoms in Si-O-Si bonding states of two per interface unit cell, which is equivalent to the oxygen concentration in 1/4 ML of the Ba_2SiO_4 bulk structure and thus in agreement with the XPS results shown in Fig. 4.7d). The pseudo-(2×1) reconstruction results in a 1:1 match in *a*-direction between Ba_2SiO_4 and the Si surface.

The interface model helps to understand the necessity of the high temperature annealing step for the formation of the epitaxial interface (see section 4.6) in more detail. In the model, the (2×1) reconstruction of the Si(001) surface is partially restored. It only features O atoms in the decorating positions and in 1/6th of the possible back-bonding positions (cf. Fig. 4.21). The O atoms in the remaining back-bonding positions and in

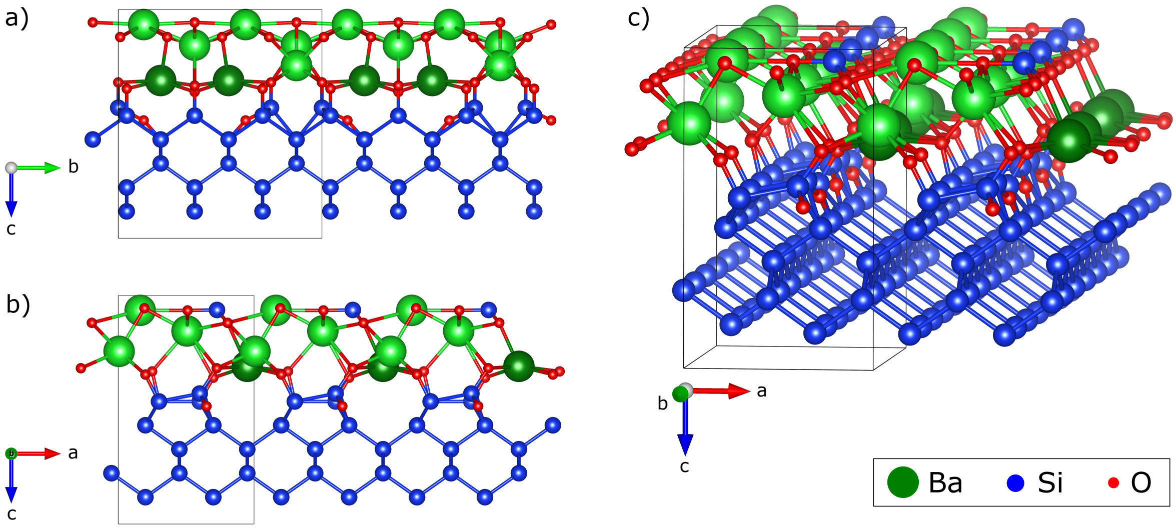


Figure 4.20.: Proposed interface model: (a) b, c-projection and (b) a, c-projection and with respect to the Ba_2SiO_4 crystal structure. (c) 3D view. Green: Ba, blue: Si, red: O. The structure was drawn with VESTA [50]. In this model, the Ba_2SiO_4 bulk structure [51] was slightly streched so that the a and b axes fit exacly 1:2 and 2:3, respectively, to the lattice constant in [110] direction of the Si lattice [100], i.e. small lattice mismatches were ignored. The Ba atoms at the interface that deviate from the Ba_2SiO_4 bulk structure are depicted in dark green.

bridging positions have to be removed, which requires the high temperature annealing step. The situation is similar to the epitaxial growth of BaO films on Si(001), which requires a (2×1) reconstruction at the substrate surface with O atoms only in decorating positions [102]. In that case epitaxial sub-monolayer Sr silicide is used as a protection layer, which prevents the formation of three dimensional SiO_2 [94]. In this work, the minimization of the oxygen pressure is used for this purpose instead. However, in addition, the silicide also deters O atoms from occupying the bridging and back-bonding

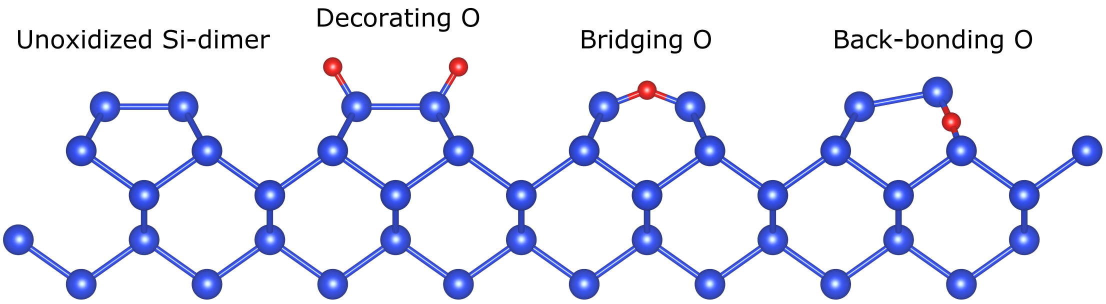


Figure 4.21.: Oxidation of the Si(001)-(2×1) dimers: Illustration of the possible positions of the O atoms based on [101]. The buckling of the dimers is not considered. Drawn with VESTA [50].

positions [101], which allows the BaO to directly growth epitaxially. As it turned out, the same was not possible by using a minimized oxygen pressure, even when starting with an amorphous monolayer of Ba. That is why, in this work, the high temperature annealing step is needed to remove these O atoms retroactively. The annealing step is only possible because the Ba_2SiO_4 is chemically stable in contact with Si (at least as long as no additional oxygen is supplied). In contrast, the BaO would react with the Si substrate to form silicate, so that the protection of the Si-dimers is the only option. A similar protection layer might also allow for the elimination of the high temperature annealing step and the direct epitaxial growth of the Ba_2SiO_4 films. In section 4.7 it was already shown that interfacial epitaxial Ba silicide does not prevent the epitaxial growth of Ba_2SiO_4.

5. Electrical properties of Ba_2SiO_4 thin films on Si(001)

In this chapter, the electrical properties of crystalline and amorphous Ba_2SiO_4 thin films will be discussed. Films grown with a minimized oxygen background pressure as determined in section 4.5 will be coverd first. Afterwards, the effect of interfacial Si-rich silicate produced by the growth in a high oxygen pressure (cf. section 4.6) will be investigated. Electrical measurements were performed on structured samples consisting of several MOS capacitors as described in detail in section 3.2. Only p-type silicon was used for the electrical measurements. All XPS measurements were performed on unstructured samples.

5.1. Band alignment of the Ba_2SiO_4/Si(001) heterostructure

A precise knowledge of the band alignment of insulator/semiconductor heterostructures is required for their technical integration. In particular, conduction and valence band offsets of more than 1 eV are required for the use in a CMOS transistor [4].

Valence band offsets of the Ba_2SiO_4/Si(001) heterostructure were measured for n- and p-type silicon by XPS using the method of Waldrop *et al.* [103, 104]. In this method, three samples are used in order to determine the valence band discontinuity of an insulator/semiconductor heterostructure. Bulk samples of the semiconducor and the insulator are used to determine the energy difference between the valence band edges and arbitrary core levels. The energy difference between the same core levels is determined using an insulator thin film, that is thin enough that the semiconductor substrate peaks are still visible. The valence band offset is then calculated from these three measurements.

Due to the lack of a Ba_2SiO_4 bulk sample, a 63 ML film was used instead. A 4 ML film was used as the thin film. Moreover, the Si 2p and O 1s core levels were used. The following three energy differences were measured

$$
\begin{aligned}
\Delta E_{Si(001)} &= E_{Si\,2p}^{Si(001)} - E_{\nu}^{Si(001)} \\
\Delta E_{Ba_2SiO_4} &= E_{O\,1s}^{Ba_2SiO_4,63\ ML} - E_{\nu}^{Ba_2SiO_4,63\ ML} \\
\Delta E_{CL} &= E_{O\,1s}^{Ba_2SiO_4,4\ ML} - E_{Si\,2p}^{Ba_2SiO_4,4\ ML}
\end{aligned}
$$

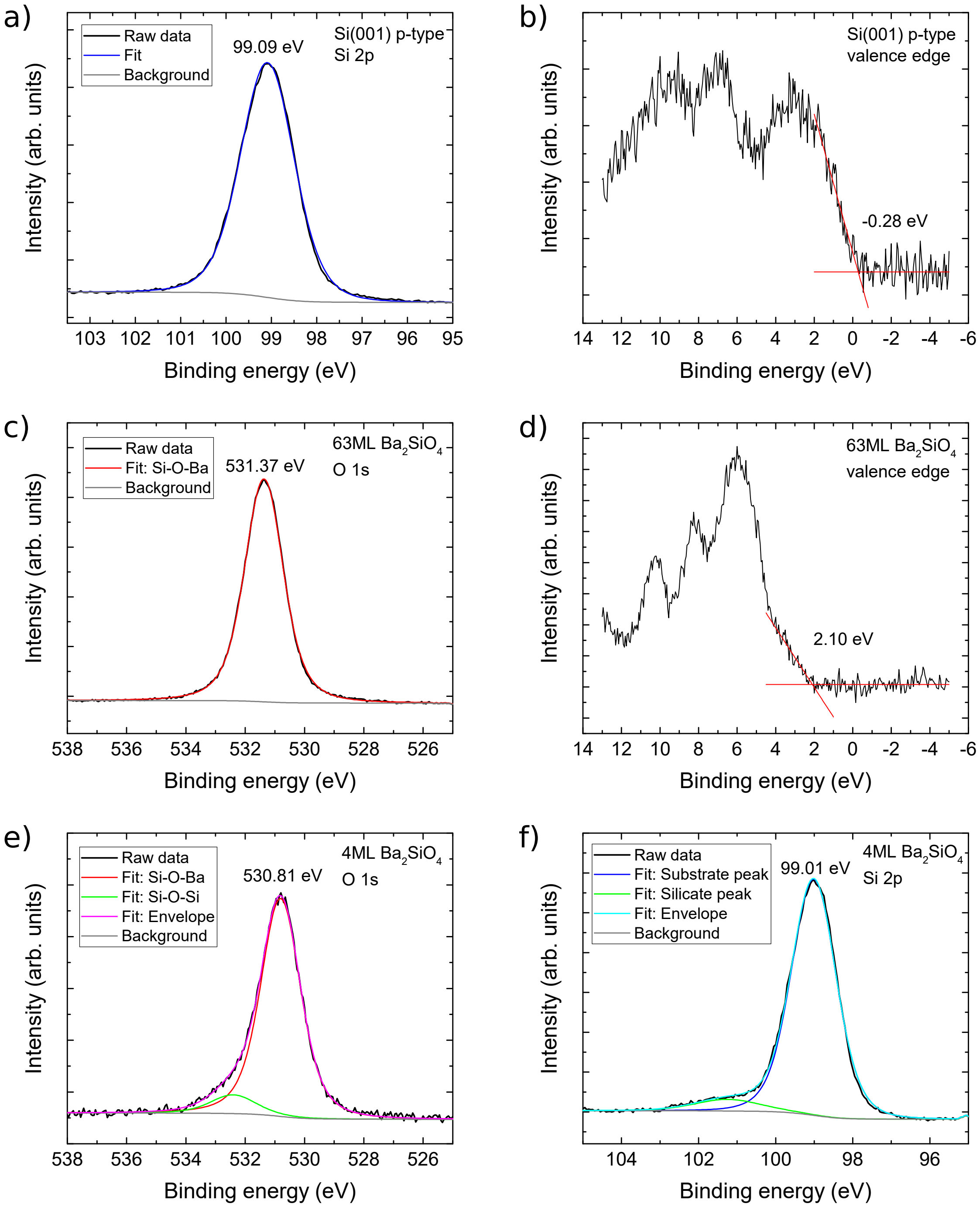


Figure 5.1.: XPS measurements used for the determination of the valence band offset of Ba_2SiO_4 to p-type silicon ($10 - 20\ \Omega\,\mathrm{cm}$): Si 2p (a) and valence edge (b) signals of p-Si(001). O 1s (c) and valence edge (d) signals of a 63 ML thick Ba_2SiO_4 film. O 1s (e) and Si 2p (f) signals of a 4 ML thick Ba_2SiO_4 film grown on p-Si(001). The Ba_2SiO_4 films were annealed at 680 °C for 40 min.

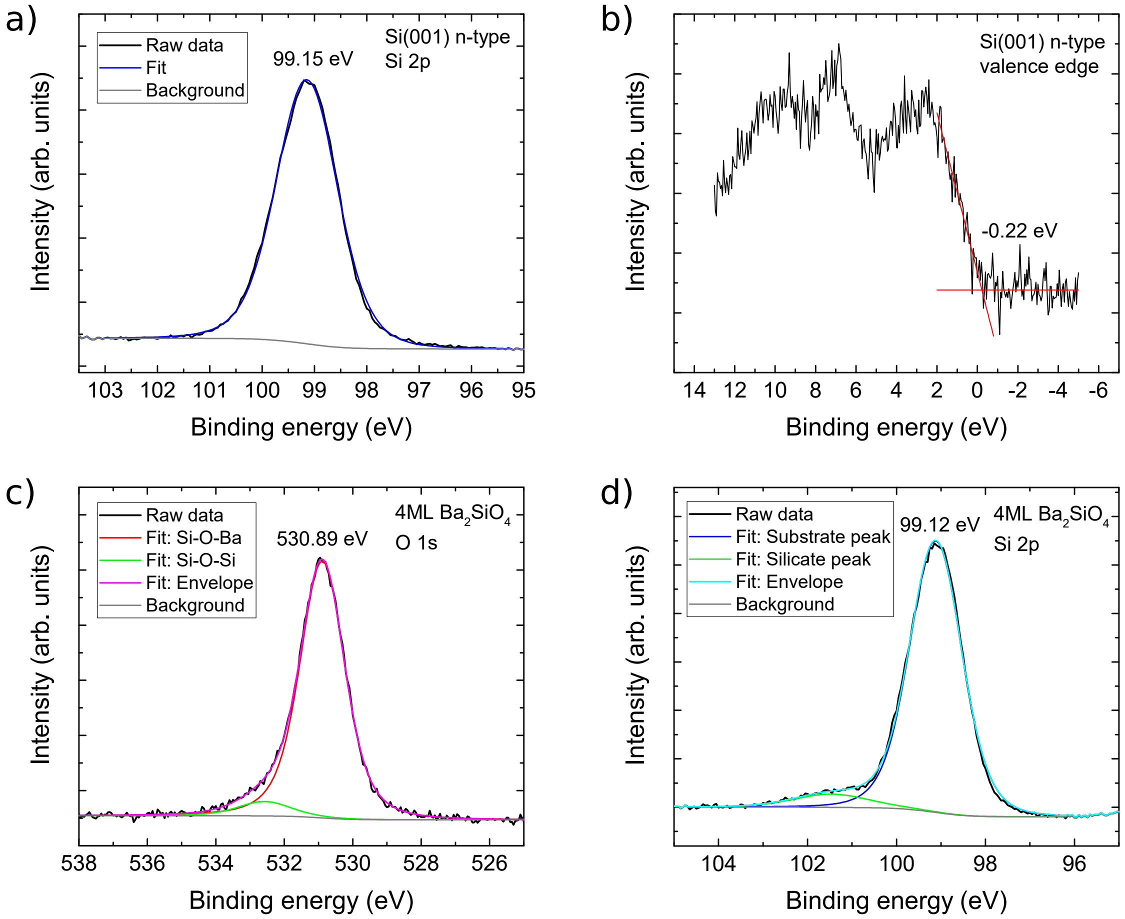


Figure 5.2.: XPS measurements used for the determination of the valence band offset of Ba_2SiO_4 to n-type silicon (8 − 12 Ω cm): Si 2p (a) and valence edge (b) signals of n-Si(001). O 1s (c) and Si 2p (d) signals of a 4 ML thick Ba_2SiO_4 film grown on n-Si(001). In addition, the measurements of the 63 ML Ba_2SiO_4 film in Figs. 5.1c) and d) were also used to determine the valence band offset to n-Si. The Ba_2SiO_4 film was annealed at 680 °C for 40 min.

where E_ν are the energetic positions of the valence band edges. The valence band offset ΔE_{VB} was then determined as follows

$$\Delta E_{VB} = \Delta E_{CL} + \Delta E_{Si(001)} - \Delta E_{Ba_2SiO_4}.$$

The results of the XPS measurements for crystalline films with the respective energy values are shown in Fig. 5.1 for the p-type Si(001) substrate (10 − 20 Ω cm) and in Fig. 5.2 for the n-type Si(001) substrate (8 − 12 Ω cm). The measurements of the 63 ML Ba_2SiO_4 film in Figs. 5.1c) and d) were also used for the calculation of the band offset to the n-type substrate.

The negative values of the valence band edges are a result of the method used for their determination, in which the linear part of the signal at low binding energies is

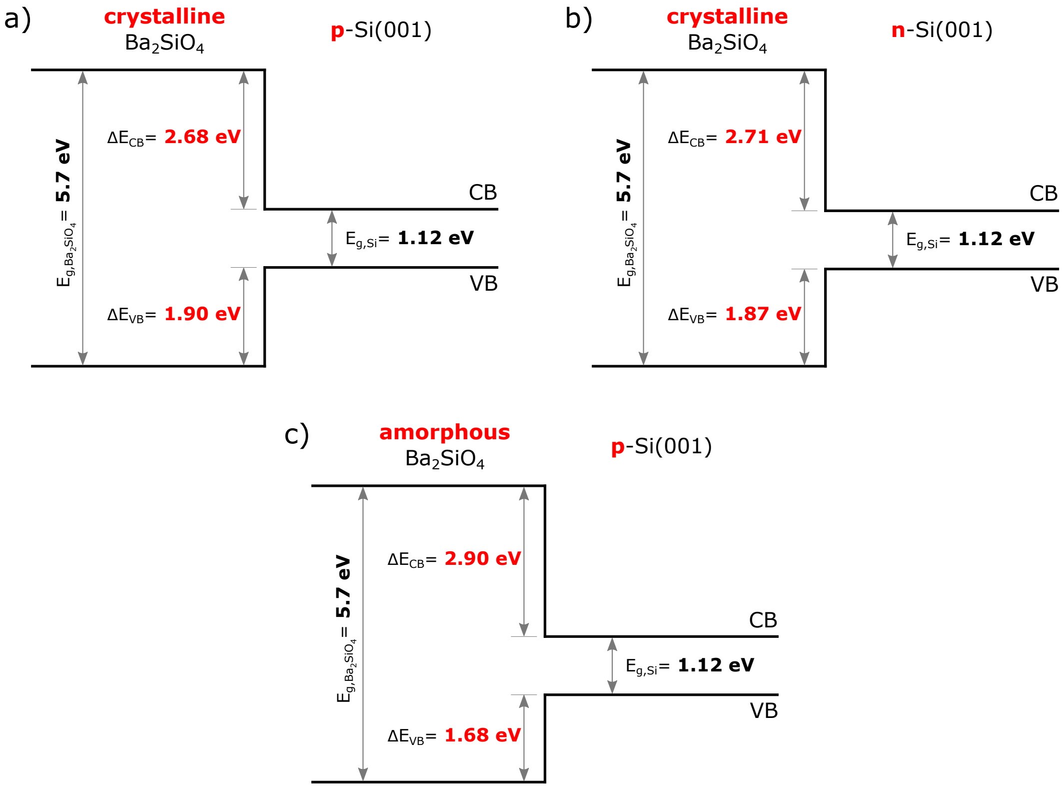


Figure 5.3.: Band offsets of the Ba_2SiO_4/Si system as determined by XPS: Epitaxial Ba_2SiO_4 on (a) p-type Si(001) ($10 - 20\ \Omega\,\mathrm{cm}$) and (b) n-type Si(001) ($8 - 12\ \Omega\,\mathrm{cm}$). (c) Amorphous Ba_2SiO_4 on p-type Si(001) ($10 - 20\ \Omega\,\mathrm{cm}$).

extrapolated and the intersection with the constant background is used as the energy of the valence band edge, as shown in the figures. Due to the signal broadening in XPS this leads to an underestimation and even negative values for the valence edges. In contrast, the Fermi edge of the silver sample used for the calbration of the XPS was fitted with a step function and the middle of the step was used as the energy of the Fermi level. This method is more accurate, but it cannot be used for the valence edges. However, this does not affect the derived values of the band offsets, assuming the errors made in the determination of the silicon valence edges and the Ba_2SiO_4 valence edge are the same.

The derived valence band offsets for crystalline films are 1.90 ± 0.10 eV to p-type silicon and 1.87 ± 0.10 eV to n-type silicon. With these values and the known band gaps of silicon (1.12 eV) and Ba_2SiO_4 (5.7 eV [1]) conduction band offsets of 2.68 ± 0.10 eV to p-type silicon and 2.71 ± 0.10 eV to n-type silicon are calculated. The resulting band alignments are shown schematically in Fig. 5.3a) and b). Within the measurement uncertainty the offsets for p-type and n-type silicon are identical for the doping concentrations used here. In addition, Fig. 5.3c) shows the band alignment for amorphous Ba_2SiO_4 on p-type silicon, which was determined analogously to that of the crystalline films. The film was kept amorphous by only annealing it to 400 °C . The valence band offset of the amorphous film is 1.68 ± 0.10 eV and thus 0.12 eV smaller that that of the crystalline film making the band alignment slightly less symmetrical.

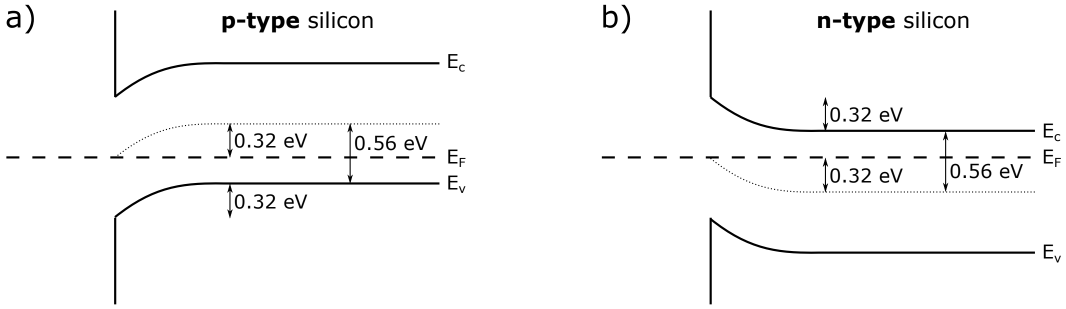


Figure 5.4.: Fermi level pinning by interface states: The band bending for (a) p-type and (b) n-type silicon is shown. The dashed line marks the Fermi energy and the dotted line indicates midgap. The Fermi level is shifted by 0.32 eV from midgap at the doping levels of the substrates used here.

The band offsets being the same for p- and n-type silicon indicates that the Fermi level is pinned by interface states as illustrated in Fig. 5.4. If the band alignment was the result of the work function difference between the gate metal and the silicon substrate, the band offsets should differ by 0.64 eV (the sum of the Fermi level shifts from midgap due to doping). The smaller valence band offset in the case of the amorphous Ba_2SiO_4 layer might be due to the interface state pinning not being fully developed yet. A Fermi level pinning was also observed for epitaxial $Ba_{0.7}Sr_{0.3}O$ films on Si(001) [105].

The valence band offset is 0.6 eV lower than previously measured for Ba_2SiO_4 grown by Si diffusion from the substrate [1]. In principle, the interface of the films grown by diffusion is not necessarily the same as in the case of the growth by co-deposition in a minimized oxygen pressure. Depending on the oxidation of the silicon substrate surface during the film growth, either a Si-rich silicate (see Fig. 4.12 and its discussion) or a silicide (see section 4.7) can form at the interface. However, both of these modifications actually reduce the valence band offset even further. A Si-rich silicate at the interface results in a valence band offset of 1.55 ± 0.10 eV, while interfacial silicide leads to a valence band offset of 1.75 ± 0.15 eV (The offsets were determined using the XPS measurements of Si(001) and the 63 ML Ba_2SiO_4 film from Fig. 5.1 as well as the ultra-thin films from Fig. 4.12a) and Fig. 4.13 for $x < 1$, respectively). Another reason for the discrepancies might be a Si deficiency at the top of the thick film grown by diffusion as a result of the need for a concentration gradient in order for the diffusion to occur. Nonetheless, the valence and conduction band offsets of the films grown by co-deposition are still well above 1 eV for both n- and p-type silicon substrates, so that the requirement for technical application is fulfilled [4].

5.2. Leakage current through Ba_2SiO_4 films

The leakage currents through crystalline and amorphous Ba_2SiO_4 layers were investigated by IV-measurements on MOS test capacitors. For reference, the outline of the samples is shown again in Fig. 5.5 (see section 3.2 for details). Only p-type silicon substrates were used for the electrical measurements. The current density-gate voltage

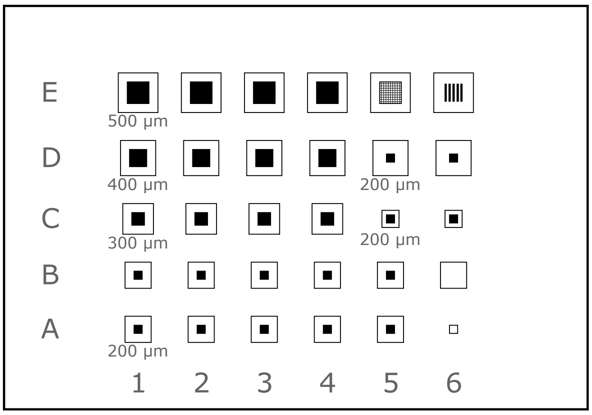


Figure 5.5.: Outline of the structured samples: The black squares represent the active area of the capacitors. The frames around them represent the size of the gold contacts. The columns are labeled from 1 to 6 and the rows are labeled from A to B. A detailed description is given in section 3.2.

characteristics of samples with 40 ML (10 nm) thick crystalline Ba_2SiO_4 films annealed at 680 °C and 695 °C are shown in Figs. 5.6 and 5.7, respectively. Moreover, Fig. 5.8 shows the results for a sample with a 40 ML (10 nm) thick amorphous film, annealed at 500 °C.

The first thing that stands out is that two of the capacitors, D5 and D6, of the sample annealed at 680 °C show significantly lower current densities than all other capacitors (see Fig. 5.6b)). At -1 V the measured current densities are $3.2 \cdot 10^{-6}$ A/cm^2 and $2.0 \cdot 10^{-6}$ A/cm^2, respectively. In contrast, the other capacitors show current densities between 10^{-3} and 1 A/cm^2 at -1 V. This means that parasitic leakage channels exist in the latter capacitors, that allow for a current to flow either directly through the silicate, e.g. along grain boundaries, or along the edges of the silicate layer due to an insufficient connection to the surrounding oxide. Unfortunately, due to the large scattering of the current densities no conclusive statement, based on the variation of the active area of the capacitors, can be made about whether the current densities scale with the area or the length of the edges of the capacitors.

A possible explanation for the high leakage currents is the presence of carbon impurities at the silicon surface. In an earlier batch of samples some of the capacitors showed linear IV curves with a slope corresponding to the serial resistance of the other capacitors, i.e. the silicate layers of those capacitors were clearly short-circuited. SEM investigations showed that the silicate layers were not closed (see appendix A.1). The problem was more pronounced at the edges, possibly due to the carbon impurities becoming mobile during the flashing and accumulating at the edges or the surface tension of the cleaning solutions being too high to properly wet the edges. It was resolved by preparing new substrates using a fresh photoresist and a more thorough cleaning procedure in order to reduce the density of carbon impurities. However, the carbon density on the silicon surface might still be too high resulting in parasitic channels at the sample edges. The results in Fig. 5.6b) clearly prove that it is possible to avoid these leakage channels.

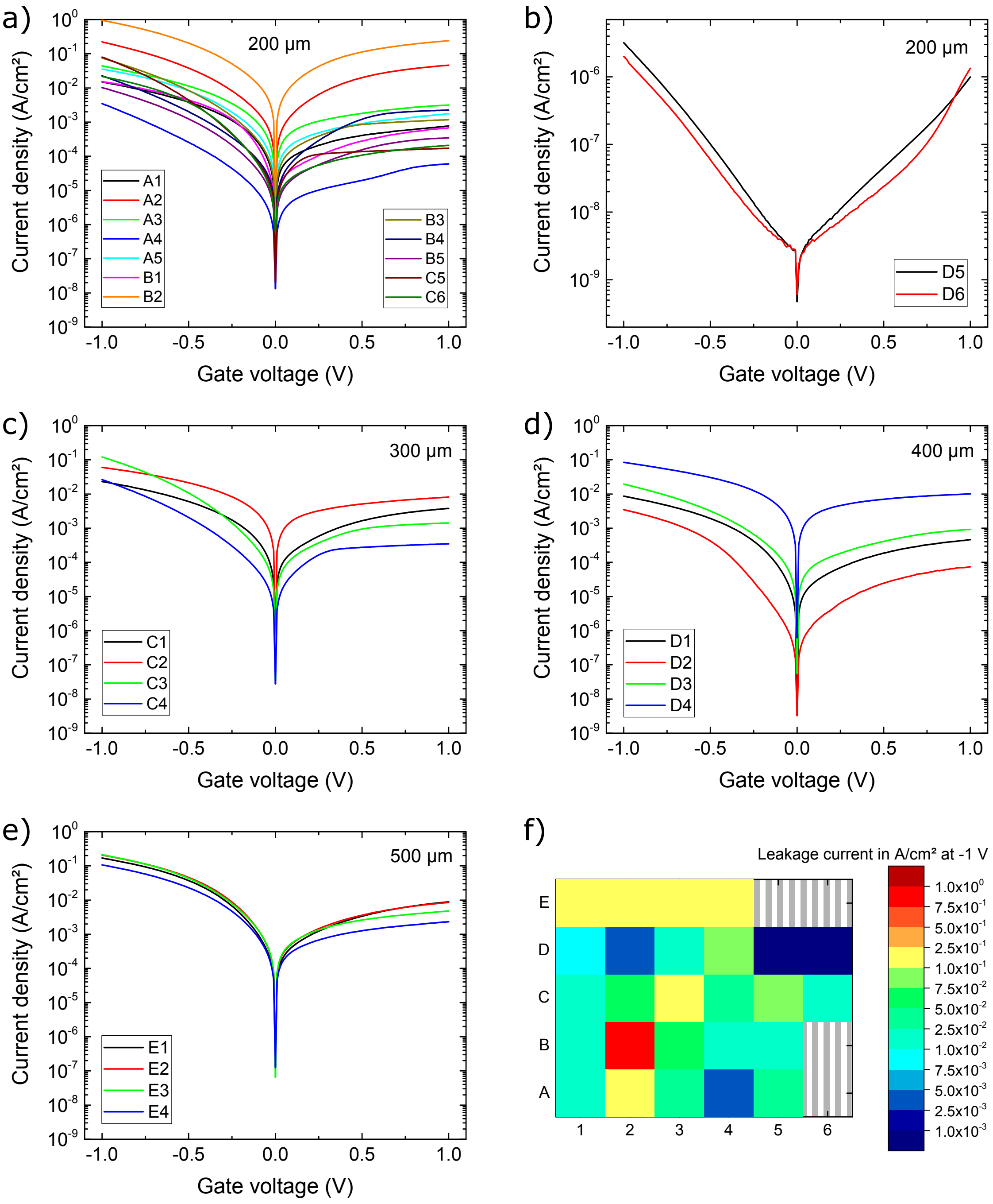


Figure 5.6.: IV curves of a sample with 40 ML (10 nm) thick crystalline Ba_2SiO_4 films annealed at 680 °C: (a), (b) 200 µm-capacitors ($4 \cdot 10^{-4}$ cm^2 area), (c) 300 µm-capacitors ($9 \cdot 10^{-4}$ cm^2 area), (d) 400 µm-capacitors ($1.6 \cdot 10^{-3}$ cm^2 area), (e) 500 µm-capacitors ($2.5 \cdot 10^{-3}$ cm^2 area), (f) heatmap of the current densities at -1 V

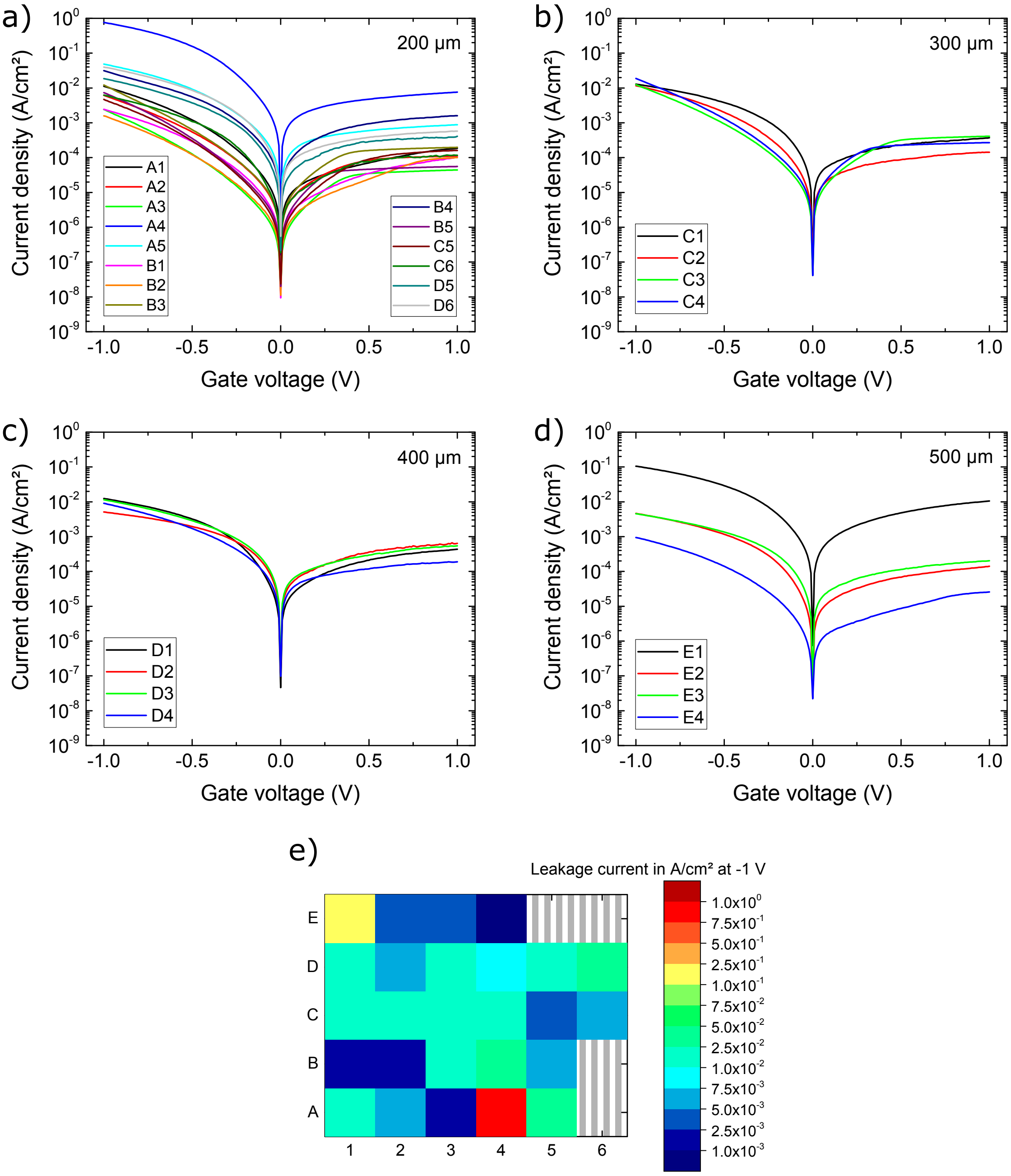


Figure 5.7.: IV curves of a sample with 40 ML (10 nm) thick crystalline Ba_2SiO_4 films annealed at 695 °C : (a) 200 µm-capacitors ($4 \cdot 10^{-4}$ cm^2 area), (b) 300 µm-capacitors ($9 \cdot 10^{-4}$ cm^2 area), (c) 400 µm-capacitors ($1.6 \cdot 10^{-3}$ cm^2 area), (d) 500 µm-capacitors ($2.5 \cdot 10^{-3}$ cm^2 area), (e) heatmap of the current densities at -1 V

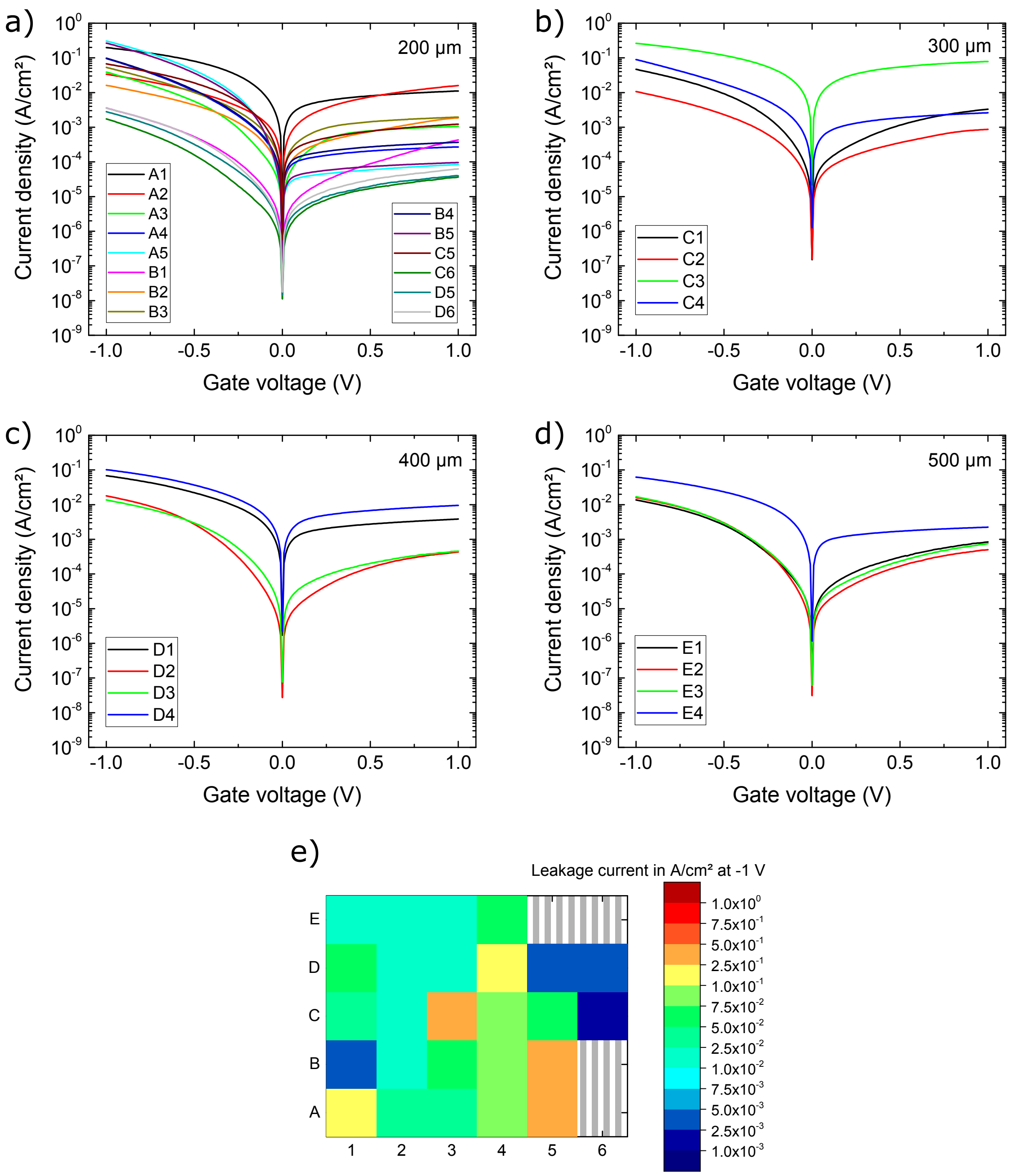


Figure 5.8.: IV curves of a sample with 40 ML (10 nm) thick amorphous Ba_2SiO_4 films annealed at 500 °C : (a) 200 µm-capacitors ($4 \cdot 10^{-4}$ cm^2 area), (b) 300 µm-capacitors ($9 \cdot 10^{-4}$ cm^2 area), (c) 400 µm-capacitors ($1.6 \cdot 10^{-3}$ cm^2 area), (d) 500 µm-capacitors ($2.5 \cdot 10^{-3}$ cm^2 area), (e) heatmap of the current densities at -1 V

In order to investigate the change of the leakage current across the sample, heatmaps of the current densities at -1 V are shown in Figs. 5.6f), 5.7e) and 5.8e). In the areas marked with the gray stripes there are no capacitors to be evaluated (see section 3.2). While there are some clusters of capacitors with comparable current densities, there are no clear patterns that are consistent across all samples. It is important to note that there was actually a temperature gradient on the samples. Since the filament of the e-beam heater used to anneal the samples was located below the rows A-C, the temperature of the D-row was approximately 10 °C below the specified temperature and the temperature of the E-row was approximately 20 °C below the specified temperature. This means that the temperature of the E-row of the sample annealed at 680 °C , which also shows comparatively high leakage currents, was actually below the optimum temperature range for crystallization.

The expectation of amorphous films having lower leakage currents than crystalline ones is not confirmed by these measurements. In fact, the crystalline films showed lower leakage currents overall. The sample with the crystalline films annealed at 695 °C (Fig. 5.7) has the most capacitors with current densities below $5 \cdot 10^{-3}$ A/cm^2 at -1 V, namely seven. The sample with the crystalline films annealed at 680 °C (Fig. 5.6) and the sample with the amorphous films (Fig. 5.8) have only four capacitors in the same range each. However, two of those capacitors from the crystalline sample annealed at 680 °C show significantly lower current densities of $3.2 \cdot 10^{-6}$ A/cm^2 and $2.0 \cdot 10^{-6}$ A/cm^2 at -1 V as discussed above. Moreover, the crystalline sample annealed at 695 °C has only two capacitors with current densities of more than $1 \cdot 10^{-1}$ A/cm^2 at -1 V, while the amorphous sample has five. The crystalline sample annealed at 680 °C has seven capacitors with current densities in the same range. However, four of those were not actually heated to temperatures in the optimum range for crystallization as discussed above.

5.3. Capacitance voltage measurements: Flat band voltage and hysteresis

A representitive capacitance voltage measurement is shown in Fig. 5.9a). This measurement was taken on the capacitor D5 of the sample annealed at 680 °C, whose IV curves are shown in Fig. 5.6. Using the inflection point method [82] $V_{fb} = -0.059$ V is determined from the forward CV curve. For the capacitor D6 of the same sample the inflection point method gives $V_{fb} = -0.082$ V for the forward CV curve.

The flat band capacitance method [80, 81] gives $V_{fb} = -0.012$ V for D5 and $V_{fb} = -0.035$ V for D6 for the forward CV curves. However, it does not take the effect of charged interface traps and non-uniform doping into account. A correction for both contributions can be done following the methods in the textbook 'MOS Physics and Technology' by Nicollian and Brews [80]: The shift of the flat band voltage due to charged interface traps can be described by $\Delta V_{fb} = eD_{it}(e\phi_B + E_g/2)/C_{ox}$, where e is the elementary charge, $e\phi_B$ is the energy distance of the Fermi level from midgap in the silicon bulk, E_g is the silicon band gap (1.12 eV) and C_{ox} is the oxide capacitance,

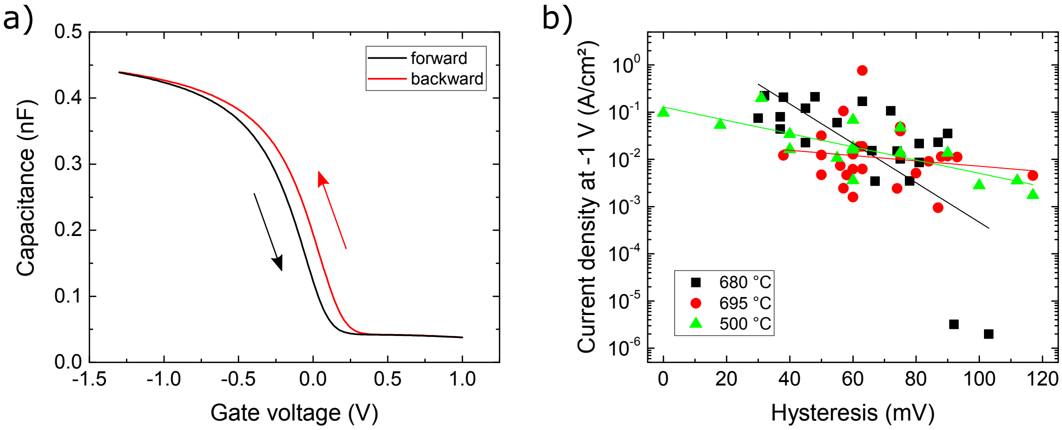


Figure 5.9.: (a) CV curves of a 40 ML (10 nm) thick Ba_2SiO_4 film annealed at 680 °C measured from negative to positive voltages (black) and vice versa (red) at a frequency of 100 kHz with a sweep time of 20 s on the capacitor D5 (area: $4 \cdot 10^{-4}$ cm^2) of the same sample whose IV curves are shown in Fig. 5.6. The hysteresis is 92 mV. $V_{fb} = -0.193$ V (forward curve, determined with the flat band capacitance method, see text). The curves were corrected for series resistance ($R_s = 421\ \Omega$) using a three element model (see section 2.5.2). (b) Current density at -1 V in dependence of the hysteresis of the CV curves for all capacitors of the two crystalline samples annealed at 680 °C and 695 °C, respectively, and the amorphous sample annealed at 500 °C.

which is determined from the CV curve in strong accumulation (here 1.10 µF/cm^2 for D5 and 1.08 µF/cm^2 for D6). The Fermi level shift due to doping can be determined via $e\phi_B = kT \cdot ln(n_i/N_A)$ for p-type silicon, with the intrinsic charge density n_i of silicon ($3 \cdot 10^9$ cm^{-3} at 290 K) and the dopant density N_A. For the substrates used in this work $N_A = 1 \cdot 10^{15}$ cm^{-3} , which results in a Fermi level shift of -0.32 eV from midgap. The shift of the flat band voltage due to charged interface traps is negative for donor type interface traps and positive for acceptor type interface traps. With $D_{it} = 2.85 \cdot 10^{12}$ eV^{-1}cm^{-2} and $3.07 \cdot 10^{12}$ eV^{-1}cm^{-2} determined for D5 and D6, respectively, (see section 5.5) and assuming that the interface traps in the lower half of the silicon band gap are donors like for the SiO_2/Si system [106] the flat band voltage shift due to charged interface traps is -0.101 V for D5 and -0.110 V for D6. Considering also the shift due to non-uniform doping at the silicon surface for which estimates are given in Table 10.3 of Ref. [80] (-0.08 V for $N_a = 1 \cdot 10^{15}$ cm^{-3}), the corrected flat band voltages determined by the flat band capacitance method are -0.193 V for D5 and -0.225 V for D6 for the forward CV curves. In comparison to the flat band capacitance method, the inflection point method overestimates the flat band voltage by approximately 0.13 to 0.14 V.

The hysteresis of the CV curve, i.e. the difference of the flat band voltages of the backward and forward curves (in this work it is defined as $V_{fb}^{backward} - V_{fb}^{forward}$, V_{fb} was determined with the inflection point method), is 92 mV and 103 mV for D5 and D6 of the sample annealed at 680 °C, respectively. In general, the hysteresis of a CV curve

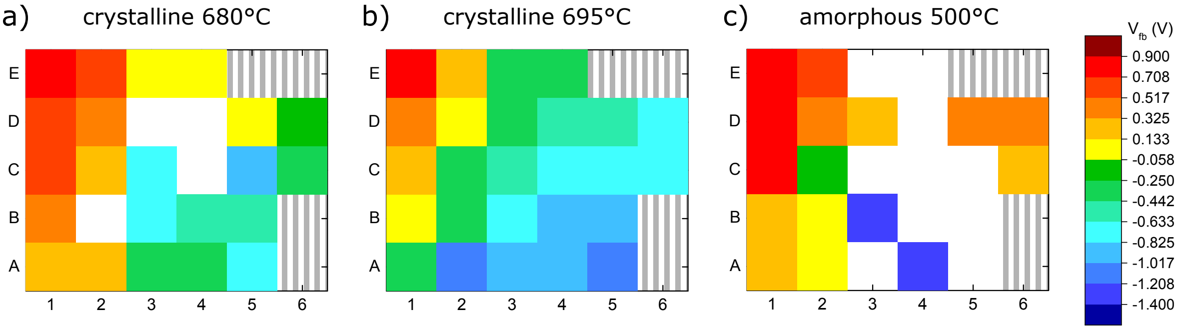


Figure 5.10.: Heatmaps of the flat band voltage (determined with the inflection point method) for samples with 10 nm thick Ba_2SiO_4 films annealed at 680 °C (a), 695 °C (b) and 500 °C (c). The fields that are left blank did not show a clear CV curve. In the areas marked with the gray stripes there are no capacitors to be evaluated.

can be caused by charge injection from the silicon into rechargeable traps near the interface, charge injection from the metallic gate contact or ionic polarization. For p-type substrates, charge injection from the silicon leads to a positive, i.e. counterclockwise hysteresis, while charge injection from the metal and ionic polarization lead to a negative, i.e. clockwise hysteresis (it is opposite for n-type substrates), with the trapped charge from the silicon usually dominating if both types of carrier injection happen, due to their close proximity to the silicon-insulator interface [107, 108]. Therefore, the hysteresis in this case is dominated by rechargeable traps near the silicon interface. It corresponds to charge densities of $6.31 \cdot 10^{11}\, e/\mathrm{cm}^2$ for D5 and $6.95 \cdot 10^{11}\, e/\mathrm{cm}^2$ for D6, where e is the elementary charge. The measured hystereses vary between 30 and 117 mV for the crystalline samples, and between 0 and 117 mV for the amorphous sample. The hystereses for D5 and D6 of the sample annealed at 680 °C, which show the lowest leakage currents, are the highest values measured for that sample. Moreover, there is a general trend of the hysteresis increasing as the leakage current decreases as shown in Fig. 5.9b). This can easily be explained by the fact that the charge that is built up at the interfaces during the voltage sweep can discharge if the silicate is not perfectly insulating. However, as seen in the figure the scattering of the data is very large, i.e. the influence of the leakage channels is not the single dominant effect. As stated above, the hysteresis results from the complex interplay of several different contributions, making a straightforward interpretation impossible. For this reason the charge densities determined above are only lower limits for the rechargeable traps near the silicon interface. The hysteresis of less than 1 mV previously measured for Ba_2SiO_4 films grown by Si diffusion from the substrate [1, 89] is not a reliable value, since it is based on an incorrect interpretation of the data (see appendix A.2).

Furthermore, the flat band voltage varies considerably between different capacitors. For the crystalline samples it varies from -1.05 V to 0.79 V, and for the amorphous sample it varies from -1.40 V to 0.88 V (determined with the inflection point method). There is also a clear trend of the flat band voltage increasing towards the top left corner of the samples as shown in Fig. 5.10. The variation of the flat band voltage cannot be due to variations of the band alignment of the Ba_2SiO_4 films and silicon, since such large variations were not observed in XPS (see section 5.1) and they are also larger than the silicon bandgap (1.12 eV) so that they would have to result in large leakage currents. However, the distribution of the flat band voltage shifts (Fig. 5.10) is not correlated with the distribution of the leakage currents (see section 5.2). It is most likely a result of a variation of the charge distribution at the interface between the insulator and the metallic gate contact. It was shown that the dipole resulting from the image charge created in the metal by the ionic charges in the oxide leads to a shift in the flat band voltage [109]. This effect can be used to tune the flat band voltage by, for example, inserting an ultra-thin Al layer between the Au capping and the insulator and varying its thickness [105]. In this case, it seems that there is a systematic and reproducible change in the charge distribution at the interface to the metal across the sample. Since the temperature gradient is parallel to the short side of the sample, this has to be due to the alignment of one of the evaporators being slightly off center, resulting in a gradual variation either of the Si:Ba ratio, the reduction of the topmost silicate layer or the impurity density at the top interface.

5.4. Dielectric constant of Ba_2SiO_4

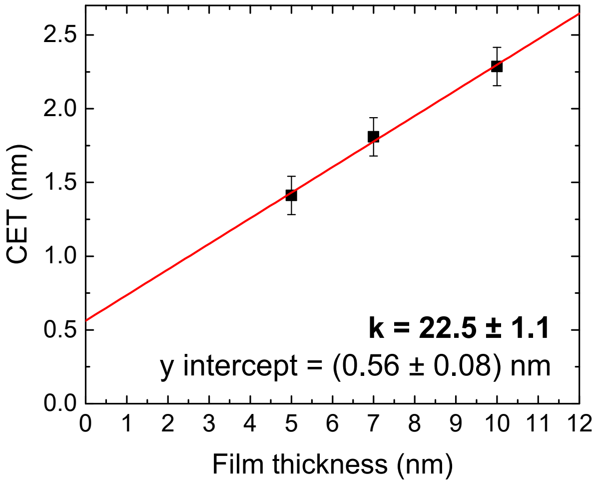


Figure 5.11.: Determination of the dielectric constant k of Ba_2SiO_4: The capacitance equivalent thickness (CET), as determined from the CV curve in strong accumulation and corrected for the quantum confinement contribution [110], is plottet against the film thickness. The slope of the linear fit is equivalent to $3.9/k$.

In order to determine the dielectric constant k of Ba_2SiO_4, the capacitance equivalent thickness (CET) is plotted against the film thickness for Ba_2SiO_4 films with thicknesses of 5, 7 and 10 nm in Fig. 5.11. The CET was determined using the capacitance value of the CV curve in strong accumulation after correction with the three-element model. Moreover, it was corrected for the quantum confinement contribution and insufficient substrate accumulation using the values determined in Ref. [110] for a p-type substrate with a dopant density of $N_A = 1 \cdot 10^{15}$ cm^{-3} and a metallic gate electrode ($\mathrm{CET}_{corr} = \mathrm{CET}_{uncorr} - \Delta t_{ox}$ with $\Delta t_{ox} = 0.6$, 0.7 and 0.85 nm for film thicknesses of 5, 7 and 10 nm, respectively). Only capacitors with active areas of $4 \cdot 10^{-4}$ cm^2 and crystalline films annealed at 680 °C were used. The leakage current densities were below $5 \cdot 10^{-2}$ A/cm^2 at -1 V for the 10 nm films and below $9 \cdot 10^{-1}$ A/cm^2 at -1 V ($< 5 \cdot 10^{-2}$ A/cm^2 at 1 V) for the 5 and 7 nm films. The average CET values were determined from five, six and ten measurements for the film thicknesses of 5, 7, and 10 nm, respectively. The slope of the linear fit is equivalent to $3.9/k$ (3.9 is the dielectric constant of SiO_2). The dielectric constant derived in this way is $k = 22.5 \pm 1.1$. It is in the high-k range and only slighly lower than the dielectric constant of HfO_2 ($k = 25$) [4].

The linear fit intersects the y-axis at a CET of (0.56 ± 0.08) nm, i.e. there is an additional capacitance contribution in series with the Ba_2SiO_4 layer. This indicates a lower polarizability at the interface. According to the proposed interface model (see Fig. 4.20), at zero thickness as it is defined here the topmost silicon layer, which features a pseudo-(2×1) reconstruction with two O atoms in Si-O-Si bonding states per interface unit cell (7.51×11.61 Å^2), still remains. Additionally, the first silicate layer at the interface has a different composition than the bulk. The offset of (0.56 ± 0.08) nm indicates that these two layers have a lower polarizability than the bulk Ba_2SiO_4, which reduces the effective dielectric constant of the silicate.

For amorphous layers the offset slightly decreases or stays the same within error margins. The capacitance in accumulation for the 10 nm thick amorphous films is 1.15 ± 0.02 µF/cm^2, which is marginally higher than the value of 1.10 ± 0.03 µF/cm^2 for the 10 nm crystalline films annealed at 680 °C. Assuming that the dielectric constant does not change for the amorphous films, this translates into the y-intercept being 0.14 ± 0.14 nm smaller for the amorphous films. This would mean that an increase in the oxygen concentration in the topmost substrate layer actually increases the dielectric constant of this layer, thereby reducing the offset.

5.5. Interface trap density of the Ba_2SiO_4/Si system

The interface trap density D_{it} was measured using the conductance method, which is explained in detail in section 2.5.4. The G_{it}/ω curves, from whose maximum D_{it} is determined with equation 2.41, are shown in Fig. 5.12a) for the capacitor D5 of the sample with the 10 nm thick Ba_2SiO_4 films annealed at 680 °C. The corresponding CV curve is displayed in Fig. 5.9a). The flat band voltage of this capacitor is -0.193 V as determined with the flat band capacitance method (see section 5.3). The G_{it}/ω curves were recorded for gate voltages ranging from weak accumulation (-0.25 V) to weak inversion (0.15 V). As the gate voltage is changed, the frequency ω at which the maximum appears changes from 4.5 MHz at -0.25 V to approximately 90 kHz at 0.15 V. From the width of the curves the correction factor f_D from equation 2.41 was determined to be $f_D = 0.4$ following the method in Ref. [80]. The derived interface trap densities in dependence of the gate voltage are shown in Fig. 5.12b). They represent the interface trap densities in the lower half of the silicon band gap and follow the same

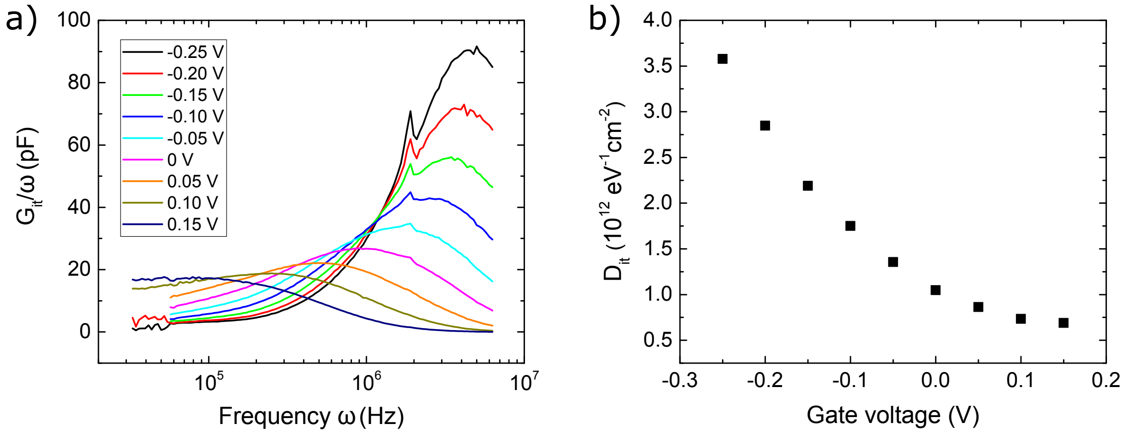


Figure 5.12.: Distribution of the interface trap density in the lower half of the silicon band gap for crystalline films: (a) G_{it}/ω curves between weak accumulation ($V_g = -0.25$ V) and weak inversion ($V_g = 0.15$ V) and (b) interface trap densities derived from the maximum of the G_{it}/ω curves. The measurements were taken on the capacitor D5 of the sample with the 10 nm thick Ba_2SiO_4 films annealed at 680 °C. The corresponding CV curve is shown in Fig. 5.9a). The flat band voltage is -0.193 V as determined with the flat band capacitance method.

trend as in the SiO_2/Si system where D_{it} increases towards the band edges. In order to determine D_{it} in the upper half of the silicon band gap, capacitors with n-type silicon are required.

Heatmaps of the interface trap density at midgap (0.32 eV above flat band for the dopant density of $N_A = 1 \cdot 10^{15}$ cm^{-3} of the substrates used) are shown in Fig. 5.13 for the samples with the Ba_2SiO_4 films annealed at 680 °C, 695 °C and 500 °C. These are the same films that are discussed in the previous sections. The sample with the crystalline films annealed at 680 °C (Fig. 5.13a)) shows a uniform distribution of the interface trap density at midgap. The average value is $(1.14 \pm 0.78) \cdot 10^{12}$ eV^{-1}cm^{-2}. Two of the capacitors show significantly higher values than the other capacitors of $3.00 \cdot 10^{12}$ eV^{-1}cm^{-2} (B3) and $3.07 \cdot 10^{12}$ eV^{-1}cm^{-2} (C5). Excluding these two capacitors, the average value becomes $(8.47 \pm 2.62) \cdot 10^{11}$ eV^{-1}cm^{-2}. The lowest value measured is $4.05 \cdot 10^{11}$ eV^{-1}cm^{-2} for A4.

The sample with the crystalline films annealed at 695 °C (Fig. 5.13b)) shows an increased D_{it} of $(2.41 \pm 0.94) \cdot 10^{12}$ eV^{-1}cm^{-2} in the rows A and B. This shows that an annealing temperature of 695 °C is already too high so that the epitaxial interface is degraded. Due to the temperature gradient on the sample, the annealing temperature of the remaining rows was actually between approximately 690 °C (C row) and 675 °C (E row). Hence, the interface trap density in these rows of $(8.71 \pm 3.82) \cdot 10^{11}$ eV^{-1}cm^{-2} is comparable to that of the sample annealed at 680 °C.

The amorphous films (Fig. 5.13c)) show interface trap densities of $(2.72 \pm 0.82) \cdot 10^{12}$ eV^{-1}cm^{-2} excluding the capacitor A4. Including A4, whose interface trap density of $2.96 \cdot 10^{13}$ eV^{-1}cm^{-2} is approximately one order of magnitude higher that that of the

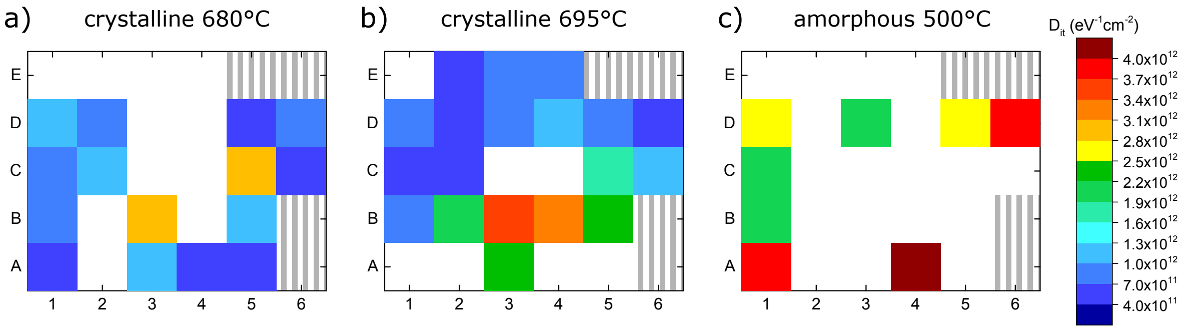


Figure 5.13.: Heatmaps of the interface trap density at midgap for samples with 10 nm thick Ba_2SiO_4 films annealed at 680 °C (a), 695 °C (b) and 500 °C (c). These are the same films that are discussed in the previous sections. The fields that are left blank either did not show a clear CV cure or their G_{it}/ω curves did not show a maximum in the measured frequency range, i.e. they would simply rise exponentially towards low frequencies. In the areas marked with the gray stripes there are no capacitors to be evaluated.

other capacitors, the average D_{it} is $6.08 \cdot 10^{12}$ eV^{-1}cm^{-2}. Interestingly, the capacitor A4 is also the one that showed no hysteresis in its CV curve.

The measured interface trap densities at midgap are approximately one order of magnitude lower than the value of $(1 \pm 0.5) \cdot 10^{13}$ eV^{-1}cm^{-2} previously reported for crystalline Ba_2SiO_4 films grown by silicon diffusion from the substrate [1, 89] *. However, as discussed in appendix A.2 only the 9.4 nm thick film in that work gave a reliable measurement. Therefore, the interface trap density achieved in that work is actually approximately $5 \cdot 10^{12}$ eV^{-1}cm^{-2} and thereby lower than the reported average value suggests. Nevertheless, this is still about a factor of five higher than the value measured in this work for crystalline films and even almost a factor of two higher than the value measured for amorphous films (excluding the capacitor A4). This improvement of the quality of the epitaxial interface can be attributed to the elimination of the need for silicon diffusion from the substrate by the growth of the films by co-deposition. It is most likely not a consequence of an improved cleaning of the substrate, since even on the samples of the first batch from this work, where some of the capacitors were short circuited due to carbon residues on the silicon surface (see appendix A.1), interface trap densities at midgap of approximately $1 \cdot 10^{12}$ eV^{-1}cm^{-2} were measured for the non-short circuited capacitors.

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*In Ref. [1] it is claimed that the given D_{it} value is the value under flat band condition. However, in the corresponding dissertation [89] a G_{it}/ω curve for the 9.4 nm film is shown in Figure 7.37. This curve has a maximum at $f \approx 5.5 \cdot 10^4$ Hz ($\omega \approx 3.5 \cdot 10^5$ Hz) and gives $D_{it} \approx 6.3 \cdot 10^{12}$ eV^{-1}cm^{-2}. The frequency of the maximum lies between that of the curves recorded at $V_g = 0.05$ V and 0.10 V in Fig. 5.12a) of this work. Therefore, the value of $D_{it} \approx 5 \cdot 10^{12}$ eV^{-1}cm^{-2} given in Figure 7.38 of Ref. [89] should be compared the the valus given in Fig. 5.13 of this work. The reason for the discrepancy is most likely that the flat band voltage was determined using the 1/C^2-method [83], which greatly overestimates the flat band voltage (for p-type substrates, it in turn underestimates it for n-type substartes) if D_{it} is not negligible, i.e. larger than $10^9 - 10^{10}$ eV^{-1}cm^{-2}.

5.6. Effect of an interfacial Si-rich silicate layer on the electrical properties

In this section the effect of a Si-rich silicate layer, i.e. a silicate layer with a higher Si concentration than Ba_2SiO_4, located at the interface to the silicon substrate on the electrical properties of the gate stack will be discussed. The Si-rich silicate layer is the result of the growth of the Ba_2SiO_4 films in a high oxygen background pressure, which leads to the oxidation of the silicon surface during the early stages of the growth. During the annealing at the latest, the interfacial SiO_x reacts with the Ba_2SiO_4 layer to form a Si-rich silicate layer (see section 4.6). Two samples were prepared. In both cases 10 nm thick Ba_2SiO_4 films were deposited in an oxygen background pressure of $1 \cdot 10^{-7}$ torr at a deposition rate of 1.1 ML/min. The only difference was the annealing temperature. The first sample was annealed at 680 C for 40 min, which results in a crystalline film, while the second sample was annealed at only 500 °C for 40 min, which is too low to crystallize the film.

The substrate with the films annealed at 680 °C used for the electrical measurements was part of the first batch of substrates in this work, which were insufficiently cleaned and still had large concentrations of carbon residues on the surface (see section 3.2.2). As a result, the majority of the capacitors show high current densities between 1 and 10 A/cm^2 at -1 V. However, four of the capacitors have current densities between $8 \cdot 10^{-3}$ and $5 \cdot 10^{-2}$ A/cm^2 at -1 V, so that they can be evaluated. The results are shown in Fig. 5.14. The accumulation capacitance is 1.11 ± 0.02 $\mu F/cm^2$, the flat band voltage is -0.48 ± 0.09 V and the hysteresis of the CV curve is 83.18 ± 34.47 mV. Moreover, the conduction band offset is 1.91 eV. These results are very similar to those of the films grown in a minimized oxygen pressure (see sections 5.1 and 5.3). The most interesting result, however, is that the interface trap density at midgap is $(3.32 \pm 0.45) \cdot 10^{11}$ $eV^{-1}cm^{-2}$, and therefore lower than even the lowest value measured for the crystalline films grown in a minimized oxygen pressure, i.e. without the interfacial Si-rich silicate. Moreover, since the accumulation capacitance is the same as for the crystalline films grown in a minimized oxygen pressure, the Si-rich silicate layer does not lead to an increase of the CET, at least within the uncertainty of measurement, making it a promising alternative to the abrupt interface.

In contrast, the results for the films annealed at 500 °C differ considerably from those grown at a minimized oxygen pressure discussed in the previous sections. Firstly, the valence band offset to p-type silicon is 1.98 eV and thus 0.08 eV higher than for crystalline films and 0.30 eV higher than for amorphous films grown in a minimized oxygen pressure. The band alignment is the most symmetrical one measured in this work. Secondly, the films show some of the lowest current densities of all the films measured in this work. In addition to the capacitors with current densities in the range of 10^{-3} to 10^{-1} A/cm^2 at $V_g = -1$ V also present for the previously investigated samples, there is now a significant number of capacitors with current densities in the range of $5 \cdot 10^{-5}$ to 10^{-3} A/cm^2. Thirdly and most importantly, the capacitance in accumulation is reduced to 0.58 ± 0.01 $\mu F/cm^2$ in comparison to 1.15 ± 0.02 $\mu F/cm^2$ for the amorphous film grown at a minimized oxygen pressure. Fourthly, the flat band voltage shifts to -3.23 ± 0.27 V (as determined with the inflection point method) and

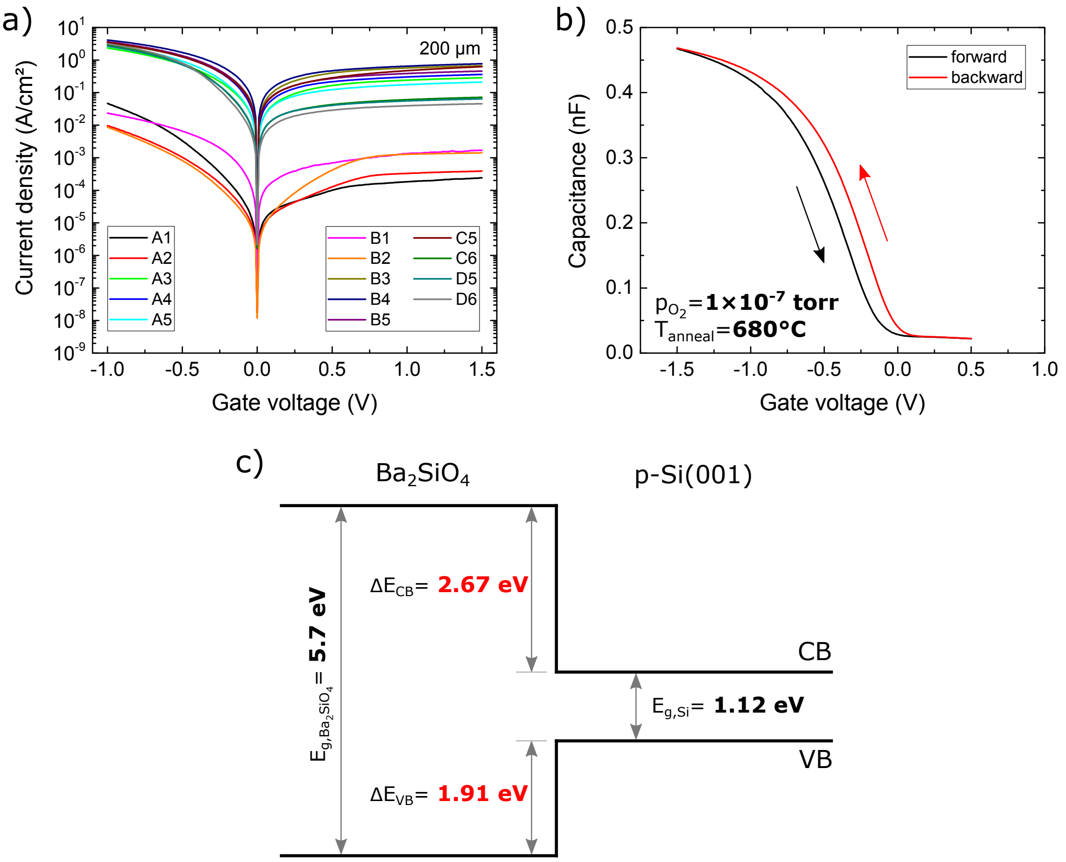

Figure 5.14.: Crystalline Ba_2SiO_4 with a Si-rich silicate layer at the interface to Si: (a) Current densities of the 200 µm-capacitors. (b) Representative CV curves of a 200 µm-capacitor (sweep time 20 s). They were corrected for series resistance using a three element model (see section 2.5.2). (c) Band alignment as determined by XPS. The films were grown in an oxygen background pressure of $1 \cdot 10^{-7}$ torr with a deposition rate of 1.1 ML/min and subsequently annealed at 680 °C for 40 min.

the hysteresis of the CV curves becomes negative: -53.27 ± 40.97 mV (the hysteresis is defined as $V_{fb}^{backward} - V_{fb}^{forward}$). Lastly, the interface trap density at midgap increases by approximately one order of magnitude to $(1.05 \pm 0.09) \cdot 10^{13}$ eV^{-1}cm^{-2}.

These results are rather unexpected given that the only difference in the preparation as compared to the previously discussed films in this section is the lower annealing temperature. The reduction of the accumulation capacitance corresponds to a CET that is approximately twice as high as that of the other 10 nm films. In order to achieve this with a SiO_2 layer connected in series it would have to be 2.8 nm thick. Since SiO_2 is thermodynamically unstable in contact with Ba_2SiO_4, the formation of a Si-rich silicate layer is more likely. Due to its higher dielectric constant it would have to be even thicker than the SiO_2 layer. However, both the formation of this layer and that it is possible to remove it by annealing the sample to 680 °C, which would have to be the case given the results of the previously discussed sample, contradict the XPS results. Therefore, there has to be a different reason for the lower accumulation

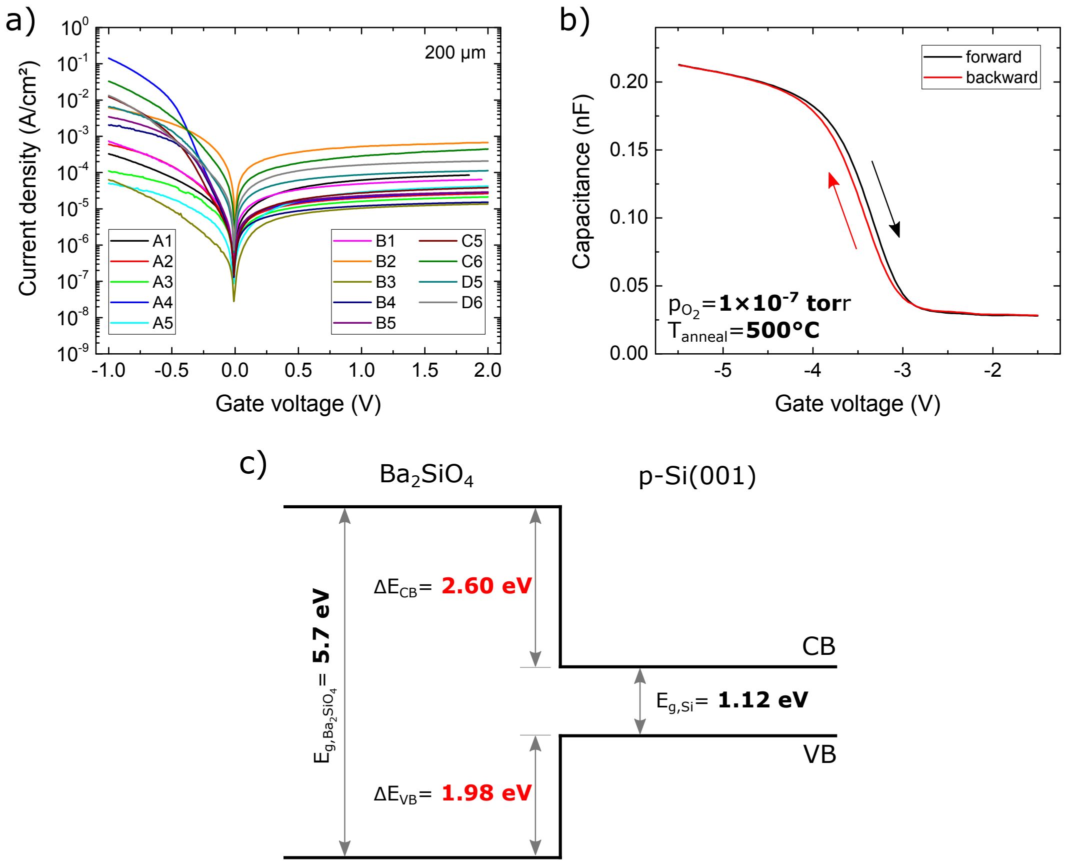

Figure 5.15.: Amorohous Ba_2SiO_4 films grown in a high oxygen background pressure: (a) Current densities of the 200 µm-capacitors. (b) Representative CV curves of a 200 µm-capacitor (sweep time 20 s). They were corrected for series resistance using a three element model (see section 2.5.2). (c) Band alignment as determined by XPS. The films were grown in an oxygen background pressure of $1 \cdot 10^{-7}$ torr with a deposition rate of 1.1 ML/min and subsequently annealed at 500 °C for 40 min.

capacitance. It is possible that due to high disorder in the films the polarization axes of the individual dipols are randomly aligned, which would lower the effective dielectric constant. Furthermore, the negative, i.e. clockwise hysteresis of the CV curve means that the charge injection from the silicon into rechargeable traps near the interface is not the dominant contribution to the hysteresis anymore, either due to the density these rechargeable traps being greatly reduced or the ionic polarization contribution being greatly increased [107, 108] (see also section 5.3). The shift in the flat band voltage also indicates an increase in the trapped positive charge located at the interface to the silicon substrate or the trapped negative charge at the interface to the metallic gate contact. A shift of -3 V corresponds to a charge density of $1.09 \cdot 10^{13}\, e/\mathrm{cm}^2$. Overall, films prepared in this way are not suitable as a high-k dielectric, mainly because of the low accumulation capacitance, and therefore high CET, and the high interface trap density. While the reasons for the drastic differences are still unclear, the results show that the annealing temperature is much more important in the case of the growth in a high oxygen pressure as compared to the growth in a minimized oxygen pressure.

5.7. Assessment of the results and comparison with the literature

The high leakage current densities of more than $1 \cdot 10^{-3}$ A/cm^2 at -1 V and a film thickness of 10 nm measured for the majority of the capacitors have to be due to an issue in the preparation, since current densities that are approximately three orders of magnitude lower were also measured in two capacitors. During the preparation different Ba silicate compounds can form due to a local oxygen surplus and Ba silicide can form due to a local oxygen deficiency. However, the values of the band gaps of the different Ba silicate compounds are very similar to each other, so that even if a different silicate compound is formed it will unlikely lead to high leakage currents. DFT calculations give values of 4.539 eV for $BaSiO_3$ [52], 4.792 eV for $BaSi_2O_5$ [111] and 4.512 eV for $Ba_2Si_3O_8$ [53] as compared to 4.632 eV for Ba_2SiO_4 [51]. Note that DFT calculations generally underestimate the band gap. Experimentally a value of 5.7 eV was measured for Ba_2SiO_4 [1]. Unfortunately, there is no data available for $Ba_3Si_2O_7$ or $Ba_4Si_3O_{10}$, which are the most likely silicate compounds to form as defects in Ba_2SiO_4 since their anions consist of chains of two and three SiO_4-tetrahedra, respectively, and the anions of Ba_2SiO_4 are single SiO_4-tetrahedra (see section 2.2.2). In contrast, the anions of $BaSiO_3$ are infinite SiO_4-tetrahedra chains, so that this compound is unlikely to form. The formation of $BaSi_2$ will, however, likely lead to leakage currents, since its band gap is comparatively small. DFT calculations give a value of only 0.791 eV [112]. Moreover, the placement of the Ba atoms in the unit cell is similar to Ba_2SiO_4 with the unit cell of $BaSi_2$ being slightly larger than that of Ba_2SiO_4 (see appendix A.3), so that it can more easily form as a defect if the local oxygen concentration is too low. Its formation could lead to carrier injection from the silicon into the associated defect states.

In order to compare the leakage currents with the literature, current densities at 1 V are used for n-type silicon substrates, since in this case the current densities are higher at positive voltages, and vice versa current densities at -1 V are used for p-type silicon substrates, since here the current densities are higher at negative voltages. Using $k = 22.5$ as determined in section 5.4, a thickness of 10 nm corresponds to an equivalent oxide thickness (EOT) of 1.73 nm for the Ba_2SiO_4 thin films. Taking into account the offset due to the interface contribution, the EOT increases to 2.29 nm. The films of this thickness without parasitic leakage channels show current densities of $3 \cdot 10^{-6}$ A/cm^2 (Fig. 5.6b)) at -1 V, which is comparable to optimized HfO_2 films at an EOT of 1.5 nm [113, 4]. This shows that it is essential to reduce the offset of the CET/EOT due to the interface contribution. SiO_2 shows current densities at 1 V of 1 A/cm^2 at a thickness 1.7 nm and $1 \cdot 10^{-3}$ A/cm^2 at a thickness of 2.3 nm [4]. This means that the current densities of the Ba_2SiO_4 films with parasitic leakage channels ($10^{-3} - 1$ A/cm^2 at -1 V) are actually higher than those of SiO_2 at the same EOT, if the offset due to the interface contribution is considered. However, in contrast to the leakage current densities of SiO_2 and the optimized insulators presented in Ref. [4], the leakage current densities of the Ba_2SiO_4 films with the parasitic channels do not increase exponentially with decreasing thickness. The lowest current density at -1 V measured for a 5 nm Ba_2SiO_4 film (EOT = 1.43 nm with the offset taken into account) was $8 \cdot 10^{-2}$ A/cm^2. It should furthermore be noted that no additional processing steps to minimize the leakage current of the Ba_2SiO_4 films, such as an annealing step in a nitrogen atmosphere, were done.

The interface trap density D_{it} turned out to be the lowest for the crystalline films with Si-rich silicate at the interface, namely $(3.32 \pm 0.45) \cdot 10^{11}$ eV^{-1}cm^{-2}. This is, however, not unexpected, since the interface trap density is still more than one order of magnitude higher than for the SiO_2/Si(001) interface, which can be as low as $1 \cdot 10^{10}$ eV^{-1}cm^{-2} [80]. The formation of a Si-rich silicate at the interface means that the density of the SiO_4-tetrahedra is increased while the density of Ba atoms in decreased at the interface, i.e. the conditions at the interface are closer to the SiO_2/Si(001) interface reducing the interface trap density. The situation is similar to the use of a SiO_2 layer between a high-k material and the silicon substrate in order to reduce the interface trap density, with the important difference that, within the uncertainty of the measurement, the CET of the Ba_2SiO_4 is not increased due to the interfacial Si-rich silicate. The interface trap density of the Ba_2SiO_4 films is also higher than for lattice matched $Ba_{0.7}Sr_{0.3}O$ on Si(001), where values of $6 - 9 \cdot 10^{10}$ eV^{-1}cm^{-2} were achieved [105]. In contrast to the $Ba_{0.7}Sr_{0.3}O$ films, the lattice constants of the Ba_2SiO_4 films were not specifically adjusted to the Si(001) surface. Moreover, the rectangular surface unit cell of the Ba_2SiO_4 films, as opposed to the square surface unit cell of the $Ba_{0.7}Sr_{0.3}O$ films, is more difficult to match to the Si(001) surface. A possible reason for the comparatively high interface trap density of the Ba_2SiO_4/Si(001) interface is the tilted growth of the Ba_2SiO_4 films in some areas as observed in Fig. 4.17. On the other hand, the interface trap density of the crystalline Ba_2SiO_4 films with the interfacial Si-rich silicate is lower than the interface trap density of the HfO_2/Si interface, and the interface trap density of the crystalline Ba_2SiO_4 films grown in a minimized oxygen pressure is comparable to the interface trap density of the HfO_2/Si interface, which has typical values of around $1 \cdot 10^{12}$ eV^{-1}cm^{-2} [114, 115]. While there are values of $1 \cdot 10^{10}$ eV^{-1}cm^{-2} reported for HfO_2, they can only be achieved with a SiO_2 layer at the interface [116], so that they are technically values for the SiO_2/Si(001) interface. With La-silicate an even lower value than for the Ba_2SiO_4 films was achieved, namely $2 \cdot 10^{11}$ eV^{-1}cm^{-2} [117].

To make the established values of the interface trap densities more intuitive to understand, the value of $1.14 \cdot 10^{12}$ eV^{-1}cm^{-2} for the crystalline film with the abrupt interface (see section 5.5) corresponds to $9.95 \cdot 10^{-3}$ eV^{-1}unit cell^{-1}, where unit cell refers to the interface unit cell with a size of 7.51×11.61 Å^2 (see section 4.10). This means that, per eV, there is an electrically active defect in every 10th interface unit cell in each direction on average. Taking into consideration the results from the structural investigation, there are three plausible causes for these defects. First, the formation of the epitaxial interface requires that some, but not all, O atoms in Si-O-Si bonding states are removed from the interface by annealing. Under the growth conditions with a minimized oxygen pressure, the number of O atoms in Si-O-Si bonding states per interface unit cell is reduced from 4 to 2 (see sections 4.6 and 4.10). According to the proposed interface model (section 4.10) these O atoms are located in the first silicon layer, which shows a pseudo-(2×1) reconstruction. In total, this layer has 15 possible locations for O atoms in Si-O-Si bonding states per interface unit cell, 12 back-bonding and 3 bridging (see Fig. 4.21). Assuming that these locations are occupied randomly before the annealing step, the O atoms not only have to be removed but some also have to be shifted into the specific locations required for the epitaxial interface, which is a source for potential defects. Second, as seen in Fig. 4.11a) an annealing temperature of 680 °C is already sufficient to also desorb O atoms in Si-O-Ba bonding states. Since no additional oxygen is supplied during the annealing, this could result in O vacancies in the silicate. Moreover, with the oxygen pressure being close to the saturation point for complete oxidation of the silicate, local fluctuations of the oxygen pressure can more easily result in oxygen vacancies than if the pressure was higher. Third, the tilted growth observed in STEM (see Fig. 4.17) also results in defects at the interface. On the one hand, there is possibly a higher defect concentration directly at the step edge than for e.g. SiO_2, due to the large lattice constant of Ba_2SiO_4 perpendicular to the interface, which makes the adjustment to the step edge more difficult. On the other hand, the continuously changing interface behind the step edge, where the Ba_2SiO_4 layer is tilted with respect to the Si(001) substrates, is also a source of defects.

6. Summary and conclusion

The epitaxial growth of Ba_2SiO_4 thin films on Si(001) by co-deposition of Ba and Si in an oxygen background pressure was systematically investigated. The stoichiometry at the interface turned out to be critically dependent on the oxygen background pressure during deposition. The key to the calibration of the oxygen pressure and the determination of the saturation point for a complete oxidation of the film was the line shape of the O 1s peak in XPS. This method is much more precise than methods based on the frequency change of a quartz crystal microbalance, since it is based on the actual oxygen concentration of the thin film under investigation and sensitive to the formation of compounds with higher oxygen concentration, e.g. the formation of BaO_2. Using a two-step approach, in which a crystalline 1 nm thick film is prepared first before the rest of the film is deposited, the successful growth of epitaxial films with a thickness of up to 16 nm was demonstrated. Films grown with a minimized oxygen pressure, i.e. an oxygen pressure just above the saturation point for a complete oxidation of the film, still feature 1/4 ML of O atoms in Si-O-Si bonding states. In comparison, the Ba_2SiO_4 bulk structure has only O atoms in Si-O-Ba bonding states. STEM showed that these films form an atomically sharp interface to Si(001) and that the Ba_2SiO_4 bulk structure is maintained up to the penultimate layer at the interface. Only one silicate layer is changed to a (2×3) structure, which was also observed in LEED, to match the (2×1.5) bulk structure to Si(001), neglecting relaxations. An interface model was proposed for the films grown with a minimized oxygen pressure, which features a pseudo-(2×1) reconstruction of the Si surface (Fig. 4.20) and can serve as the basis for future theoretical calculations.

It turned out that the epitaxial growth of the Ba_2SiO_4 films is very robust. Even the formation of a Si-rich silicate layer at the interface (see section 4.6) or the formation of epitaxial sub-monolayer Ba silicide near the interface (see section 4.7) did not prevent the epitaxial growth of Ba_2SiO_4. However, different minority structures were observed in LEED in addition to the (2×1.5) bulk structure based on the preparation conditions. Other than the (2×3) structure of the epitaxial interface for films grown in a minimized oxygen pressure, a (2×6) structure was observed in the case of an oxygen rich interface resulting from the oxidation of the substrate surface due to the growth in a high oxygen pressure, and a (4×2) structure was observed in the case of silicide formation due to a Ba surplus in the adsorbed film prior to annealing.

The temperature needed to crystallize the Ba_2SiO_4 films could not be reduced as compared to the growth by diffusion of Si from the substrate into an adsorbed BaO film. In fact, it was shown that even a 20 nm thick BaO film is turned completely into Ba_2SiO_4 at a temperature 100 °C below the temperature needed to crystallize the films, proving that the annealing step is needed for a reason beyond enabling the diffusion of Si. As it turned out, the annealing step at $670 - 690\,^{\circ}\mathrm{C}$ is needed to form the epitaxial interface (see section 4.6). In particular, it is needed to remove O atoms in Si-O-Si bonding states at the interface that form due to an oxidation of the topmost silicon layer (see the of section 4.10). This oxidation of the topmost substrate layer, which leads to a destruction of the Si dimers, could not be prevented by minimizing the oxygen pressure. Only the formation of three dimensional SiO_2 could be stopped. In comparison, the epitaxial growth of BaO and SrO films on Si(001) is achieved with the help of sub-monolayer Sr silicide that protects the dimers and enables the epitaxial growth to happen directly [101]. The retroactive removal of the O atoms in the case of Ba_2SiO_4 is only possible because Ba_2SiO_4 is chemically stable in contact with Si. In contrast, BaO or SrO would react with the substrate to form silicate.

In the electrical characterization a dielectric constant of $k = 22.5 \pm 1.1$ was found for Ba_2SiO_4 in agreement with Ref. [1], as well as band offsets to Si(001) larger than 1.8 eV for crystalline layers. Moreover, leakage current densities as low as $2 \cdot 10^{-6}$ A/cm^2 at -1 V have been measured for a 10 nm thick film. Interface trap densities at midgap of $(1.14 \pm 0.78) \cdot 10^{12}$ eV^{-1}cm^{-2} were measured for crystalline layers with an abrupt interface. Amorphous films showed slightly higher interface trap densities of $(2.72 \pm 0.82) \cdot 10^{12}$ eV^{-1}cm^{-2} at midgap. A further reduction of the interface trap density was possible by incorporating a Si-rich silicate layer at the interface, thus bringing the conditions at the interface closer to those of the SiO_2/Si(001) interface. Crystalline films with such an interfacial layer showed interface trap densities of $(3.32 \pm 0.45) \cdot 10^{11}$ eV^{-1}cm^{-2} at midgap, which is more than one order of magnitude lower than for films grown by Si diffusion from the substrate [1].

Although the results summed up above are very promising, there are still several issues that have to be addressed before Ba_2SiO_4 can be used as an alternative gate insulator. First, even though no SiO_2 forms at the interface, the epitaxial interface still seems to contribute an offset of (0.56 ± 0.08) nm to the overall CET (see section 5.4). This greatly limits the achievable minimum CET of the gate stack and makes the scaling below a CET of 1 nm essentially impossible. Second, the majority of the films still showed high leakage current densities of more than $1 \cdot 10^{-3}$ A/cm^2 at -1 V and at a film thickness of 10 nm. Since current densities that are approximately three orders of magnitude lower were also measured in two capacitors, this has to be an issue with the preparation. Third, the fact that the band offsets for p-type and n-type substrates are almost identical indicates that the Fermi level is pinned by surface states (see section 5.1). It has to be investigated how these surface states affect the source-drain channel and the switching ability of the transistor.

The mentioned issues suggest that the interface has to be modified in order for the Ba_2SiO_4 films to be used as a high-k gate insulator. The investigation of the growth mechanism in this thesis provides a basis for such interface engineering. A promising route is the start with an epitaxial Ba silicide or Sr silicide sub-monolayer at the interface. It was already shown that the epitaxial growth on such a layer is possible. This would increase the density of large atoms at the interface and thereby hopefully increase the dielectric constant of the interface thus reducing the interface contribution to the overall CET of the gate stack. Furthermore, this layer could possibly lower the annealing temperature needed to grow epitaxial films, since it protects the dimers of the Si(001) surface as discussed above.

In order to further reduce the interface trap density, it might also be worth the effort to lower the density of carbon impurities at the silicon surface and to reduce its roughness. When a Ba_2SiO_4 film is grown on Si(001) with the co-deposition method used in this work, the initial silicon surface becomes the interface. This means that all impurities that were on the surface before the growth will end up at the interface. In contrast, SiO_2 layers are usually grown on silicon by oxidation of the silicon surface, so that the interface will lie lower than the initial silicon surface. As a result, the initial density of carbon contaminations will not directly affect the interface. Since silicon crystals can be grown essentially carbon free, a contamination of the interface by carbon impurities is not an issue in the SiO_2/Si, which might be part of the reason why interface trap densities as low as $1 \cdot 10^{10}$ $\mathrm{eV}^{-1}\mathrm{cm}^{-2}$ can be reached in that system. Carbon contaminants can come from a variety of sources. Firstly, residues of the mineral oil used to store the barium can decompose and enter the vacuum upon heating of the crucible. They can then accumulate at the silicon surface before the deposition of the Ba_2SiO_4 film is even started (see section 3.1.1). Even when the Ba pieces are thoroughly cleaned before being put into the crucible, small concentrations are bound to remain on them. Secondly, carbon residues on the structured samples resulted in ruptured and therefore short-circuited films (see appendix A.1). While the main issues were solved, it cannot be excluded that the density of the remaining carbon contaminants affects the interface trap density. Using vacuum sealed barium and increasing the flashing temperature for the structured samples might therefore reduce the interface trap density. Furthermore, the STEM measurements have shown that steps in the Si(001) surface are correlated with a tilt in the Ba_2SiO_4 growth direction, most likely due to the large lattice constant of Ba_2SiO_4 perpendicular to the interface (see section 4.9). Again, this is most likely less of an issue for in the SiO_2/Si system, since SiO_2 has smaller lattice constants and grows amorphously. Due to the etching of the squares for the capacitors and the cleaning in piranha solution (see section 3.2) the silicon surface is expected to be rather rough. However, the exact roughness is unknown. Monitoring the roughness an ultimately minimizing it might result in lower interface trap densities.

A. Appendix

A.1. Short-circuit due to carbon residues

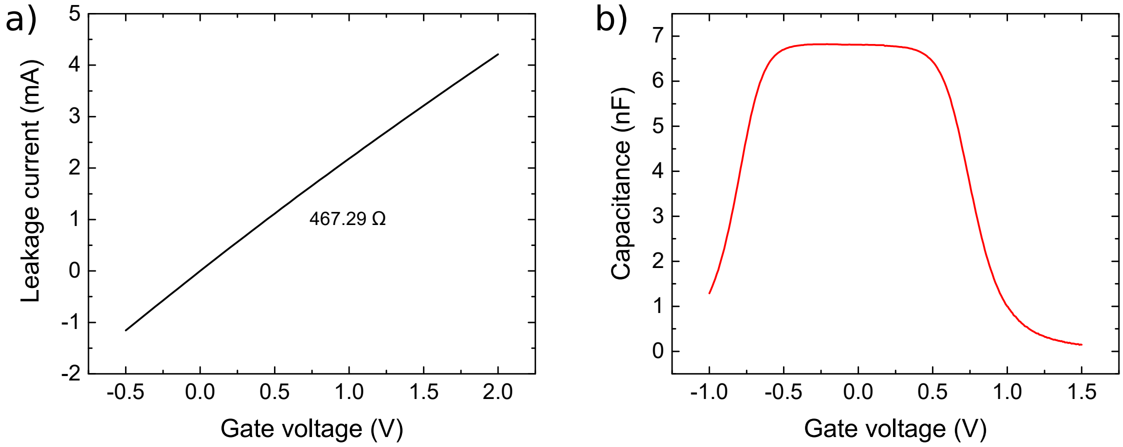

Figure A.1.: Short-circuited capacitor: (a) IV curve and (b) CV curve of a 200 µm-capacitor with a 7 nm thick Ba_2SiO_4 film, which was grown in a minimized oxygen pressure and subsequently annealed at 680 °C. The resistance determined from the IV curve is comparable to the series resistance of other capacitors, i.e. the Ba_2SiO_4 film is short-circuited.

The first batch of structured samples for the electrical measurements showed very high leakage currents in the majority of the capacitors. Some of the capacitors even showed linear IV curves with slopes corresponding to resistances comparable to the series resistance of the capacitors with the lowest leakage currents, i.e. the Ba_2SiO_4 films of these capacitors were clearly short-circuited. An example of this is shown in Fig. A.1a) for a 200 µm-capacitor of a sample with a 7 nm Ba_2SiO_4 film deposited in a minimized oxygen pressure and annealed at 680 °C.

In order to understand the reason for the short-circuit, scanning electron microscopy (SEM) measurements were performed. For this a structured sample was prepared with a 5 nm Ba_2SiO_4 film with the same growth parameters as before, i.e. it was deposited in a minimized oxygen pressure and annealed at 680 °C, but without a metallic gate contact so that the Ba_2SiO_4 film is visible in the SEM. To protect the surface, the sample was loaded in a vacuum suitcase directly from the UHV chamber and transported to the UHV chamber with the SEM. Here it was on air for only a few seconds when taking it out of the suitcase and loading it into the UHV chamber. The SEM measurements reveal that the reason for the short-circuit is that the films are ruptured as seen in

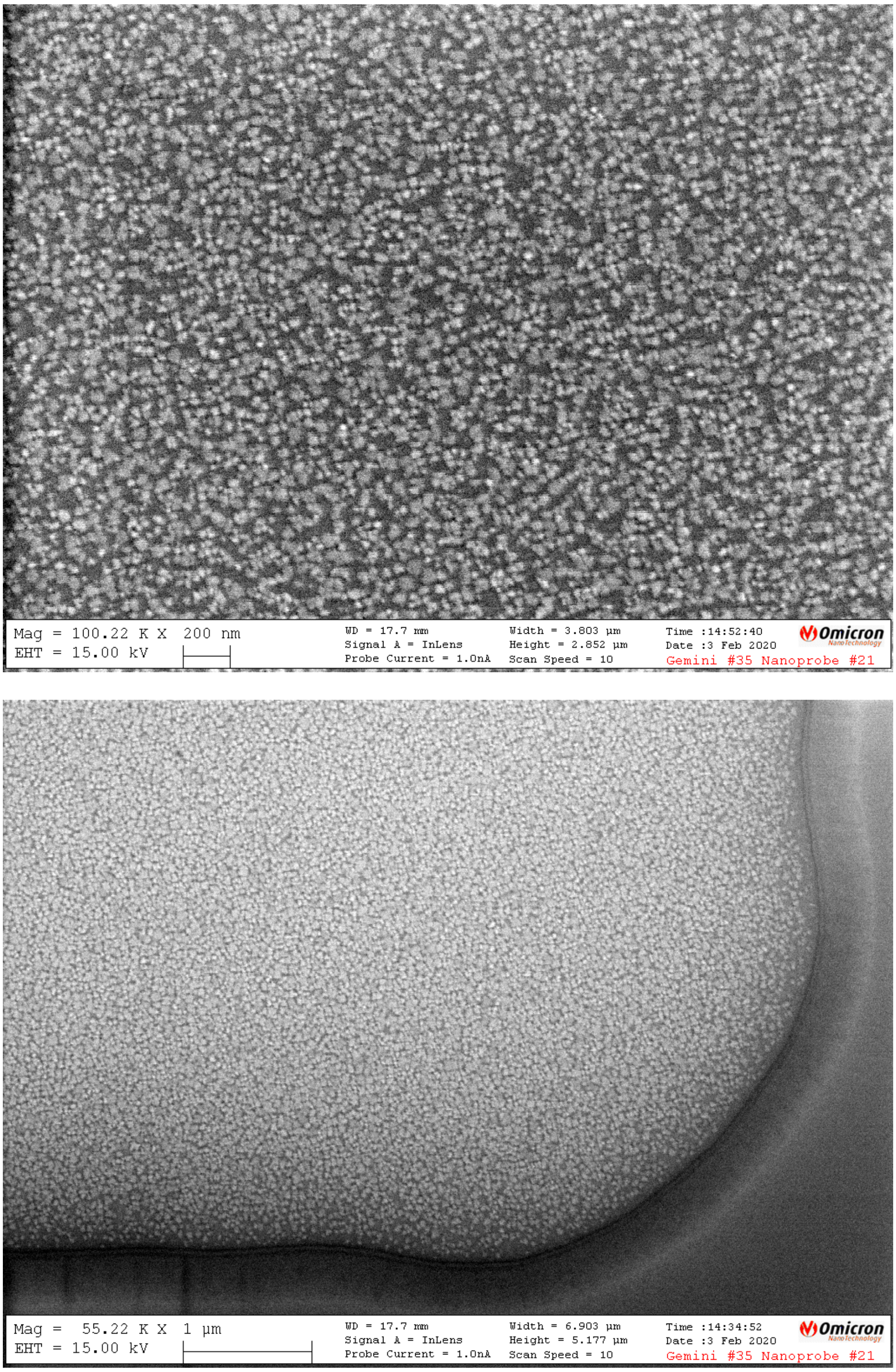

Figure A.2.: Reason for the short-circuit: Scanning electron microscopy (SEM) images of a structured sample with a 5 nm Ba_2SiO_4 film grown in a minimized oxygen pressure and subsequently annealed at 680 °C. The film was not capped with a metalic gate contact, so that the Ba_2SiO_4 film is visible. Top: SEM image taken close to the middle of the active area of one of the capacitors. Bottom: SEM image showing the edge of the same capacitor. The Ba_2SiO_4 film is ruptured, explaining the short-circuit. The island density decreases towards the edge. The contrast was adjusted for better visibility.

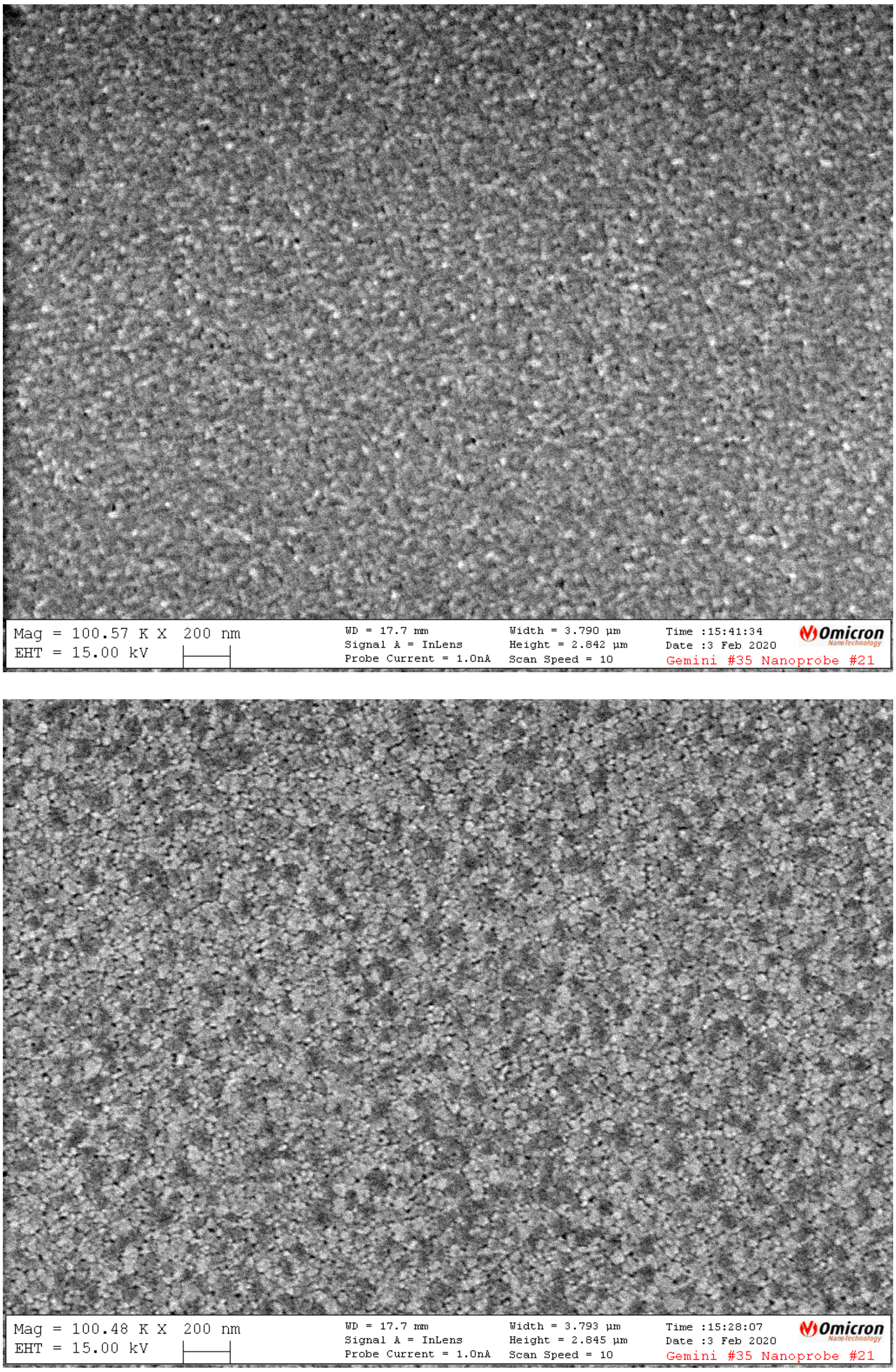

Figure A.3.: Minority of almost closed films: Scanning electron microscopy (SEM) images taken on the same sample as in Fig. A.2, but of different capacitors. In contrast to the capacitor in Fig. A.2, the island density in these capacitors is higher. The contrast was adjusted for better visibility.

Fig. A.2. Moreover, the island density decreases towards the edges of the capacitors as seen in the bottom image of the same figure. However, in some of the capacitors the Ba_2SiO_4 film is (almost) closed, two examples of which are shown in Fig. A.3. This is in line with the fact that a few of the capacitors showed leakage currents several orders of magnitude below highest measured ones and in a range where the CV measurements can be evaluated. Furthermore, SEM measurements on an unstructured sample with a Ba_2SiO_4 film prepared under otherwise identical conditions showed no islands at all. The film was completely flat.

The CV measurements of the capacitors with short-circuited films are not determined by the Ba_2SiO_4 films. However, as seen in Fig. A.1b) at positive gate voltages the signal can easily be confused with a proper CV curve. However, these curves do not scale with the active area of the capacitors and there is a mirrored CV curve at negative voltages. Therefore, they have to be either a measurement artifact or due to an additional capacitance in the circuit that is independent of the Ba_2SiO_4 films.

The problem of the short-circuited Ba_2SiO_4 films was solved by using a fresh photoresist and a more thorough cleaning procedure. A piranha etch was added, which was previously omitted since it roughens the silicon surface, and the number of dilution steps of the RCA SC-1 cleaning step was increased from one to three (for details see section 3.2.2). The problem with aged photoresist is that it might not be able to be completely removed and therefore leave residues on the silicon surfaces. Thus, the reason why the films were not closed is most likely residual hydrocarbons.

A.2. Re-examination of the previous work

When comparing the results of the electric measurements to those published earlier in the dissertation by Shariful Islam [89], there were some disagreements in the data. In particular, the CET values used for determining the k-value of Ba_2SiO_4 much lower in that work were, even though they were not corrected for quantum mechanical effects. Upon close inspection of the raw data of that thesis it turned out that in some cases artificial CV curves, that do not scale with the active area of the capacitors (see previous section), were measured and mistaken for real ones, which led to incorrect conclusions. Therefore, the old data from Shariful Islam will be re-examined in this section in order to explain the discrepancies.

In his dissertation [89] Shariful Islam used Ba_2SiO_4 films of three different thicknesses to determine the k-value: 6.25 nm, 9.4 nm and 12.5 nm (in the raw data they are labeled as 5 nm, 7.5 nm and 10 nm, respectively, which was changed in the thesis after re-calibrating the thickness). The 6.25 nm and the 12.5 nm films showed very high leakage currents. For the 6.25 nm films the leakage current densities were between $6.5 \cdot 10^{-2}$ and 2.8 A/cm^2 at 1 V and between 2.8 and 25 A/cm^2 at -1 V. For the 12,5 nm films the leakage current densities were between 1.6 and 25.5 A/cm^2 at 1 V and between $2.1 \cdot 10^{-1}$ and 25 A/cm^2 at -1 V, with one exception: One of the 600 µm-capacitors had a leakage current density of $1.4 \cdot 10^{-4}$ A/cm^2 at 1 V and $1.6 \cdot 10^{-4}$ A/cm^2 at -1 V.

Fig. A.4a) shows the CV curve that is also shown in Figure 7.35 of Ref. [89] (Note that

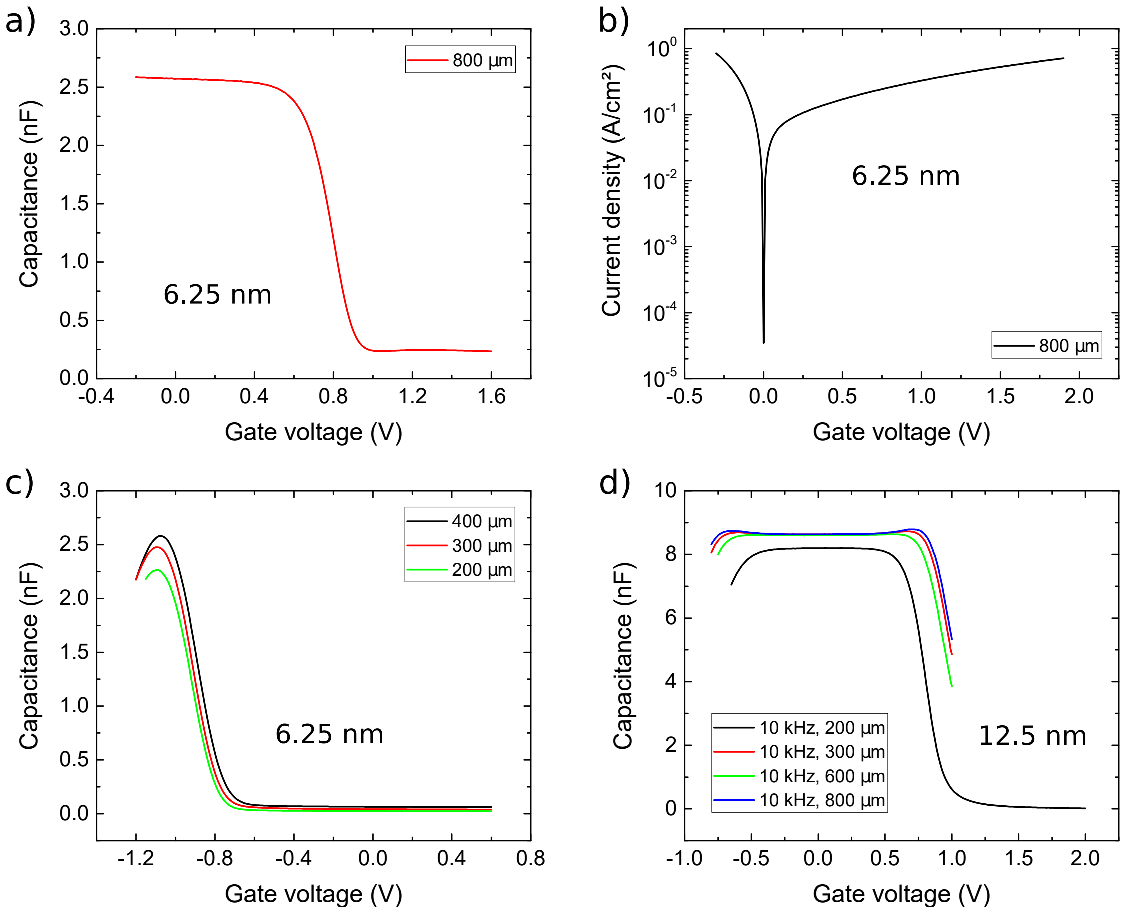

Figure A.4.: Re-examination of the previous work (1): (a) CV measurement of an 800 µm-capacitor with a 6.25 nm thick Ba_2SiO_4 film and (b) IV curve of the same capacitor. (c) CV measurements taken on the same sample as in a) but for capacitors with different gate lengths. (d) CV measurements taken on a sample with a 12.5 nm Ba_2SiO_4 film. The results for capacitors with different gate lengths are compared. The gate lengths are indicated in the insets. All capacitors have a square active area. The measurements in a) and c) were taken at a frequency of 100 kHz, while the measurements in d) were taken at 10 kHz. Labels of the capacitors in the raw data: 6.25 nm: B21, B23, B24 & B25. 12.5 nm: B11, B14, B91 & B95. The measurements were taken by Shariful Islam [89].

in that figure the y-axis is incorrectly labeled as nF/cm^2, when it is actually just nF). The IV curve of the same capacitor is shown in Fig. A.4b). Even though the leakage current is not as high as in Fig. A.1, Fig. A.4a) shows most likely an artificial CV curve since the accumulation capacitance is comparable to those in Fig. A.4c), which shows the CV measurements for other capacitors of the same sample but with different gate lengths as noted in the inset (Note that the y-axes are in nF). Regardless, since the measurement in Fig. A.4a) was taken on an 800 µm-capacitor, the CET derived from it is 8.51 nm, which is too high for a 6.25 nm Ba_2SiO_4 film and also not the one used for the determination of the k-value in Figure 7.34 of Ref. [89]. How the CET

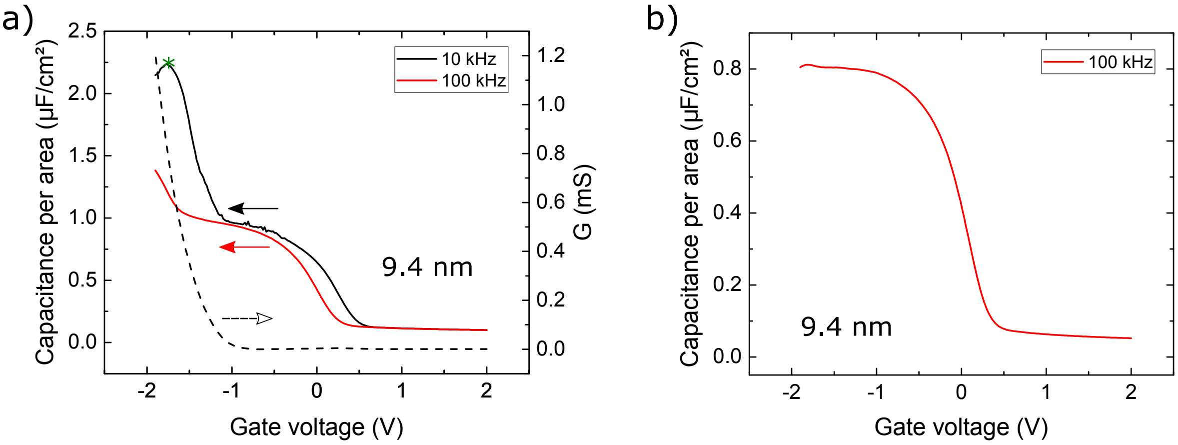

Figure A.5.: Re-examination of the previous work (2): (a) CV measurements of a 200 µm-capacitor with a 9.4 nm thick Ba_2SiO_4 film taken at 10 kHz (black curve) and 100 kHz (red curve). The measurement of the parallel conductance at 10 kHz is also shown (dashed line). Below -1 V there is a breakthrough of the capacitor resulting in a rise of the CV signal. (b) CV measurement of a 400 µm-capacitor on the same sample taken at 100 kHz. In this capacitor there is no breakthrough within the measured voltage range. Labels of the capacitors in the raw data: B32 & B33. The measurements were taken by Shariful Islam [89].

value for the 6.25 nm film used for the determination of the k-value was determined is not completely comprehensible from the evaluation files, but using the curve of the 300 µm-capacitor in Fig. A.4c) gives the same value. However, this curve is clearly an artificial CV curve, since it does not scale with the active area of the capacitor.

Fig. A.4d) shows CV measurements of the sample with a 12.5 nm Ba_2SiO_4 film for capacitors with different gate lengths as indicated in the inset. Again, these are artificial CV curves since they do not scale with the active area of the capacitors. Moreover, the start of the mirrored CV curve (see previous section) is visible. The 600 µm-capacitor is the one with the leakage current density of $1.6 \cdot 10^{-4}\,\mathrm{A/cm^2}$ at -1 V, however, the CV curve is nonetheless an artificial one. The CET value for the 12.5 nm film used for the determination of the k-value was determined from these measurements.

The sample with the 9.4 nm thick Ba_2SiO_4 film showed leakage current densities between $7.3 \cdot 10^{-4}$ and $1.1 \cdot 10^{-1}\,\mathrm{A/cm^2}$ at 1 V and between $2.4 \cdot 10^{-1}$ and $11.4\,\mathrm{A/cm^2}$ at -1 V. Some of the CV measurements show real CV curves, but the results were interpreted incorrectly. Fig. A.5a) shows one of the CV curves used for the determination of the k-value as an example. While the curve measured at a frequency of 10 kHz (black) is reliable from -1 to 2 V, it drastically increases below -1 V. This increase is accompanied by an increase of the parallel conductance (dashed line), i.e. there seems to be a breakthrough of the Ba_2SiO_4 film. The increase is less pronounced in the curve measured at 100 kHz (red). The maximum of the 10 kHz curve (marked with a green asterisks) was used to calculate the CET for the determination of the dielectric constant. This resulted in an underestimation of the CET. Fig. A.5b) shows a CV curve from a different capacitor, where no electrical breakthrough occurred. It is comparable to the ones measured for the 10 nm films in this work. Note that the curve was not corrected for the series resistance, which would slightly increase the accumulation capacitance.

Consequently, the CET values in Figure 7.35 of Ref. [89], and thus also the k-value, are incorrect. While the k-value published in the corresponding paper [1] agrees within the measurement uncertainty with the one determined in this work, this is just by chance, since the one in this work was determined with and the one in Ref. [1] was determined without correction for quantum mechanical effects. Moreover, the claim that the hysteresis of the CV curve is below 0.5mV is also not correct since it is based on the measurement in Fig. A.4a). On the other hand, the high interface trap densities of $D_{it} \approx 1 \cdot 10^{13}$ eV^{-1}cm^{-2} and $1.5 \cdot 10^{13}$ eV^{-1}cm^{-2} determined for the 6.25 nm and 12.5 nm films, respectively, are unreliable. Thus the actual interface trap density achieved in that work is closer to the value of $D_{it} \approx 5 \cdot 10^{12}$ eV^{-1}cm^{-2} determined for the 9.4 nm film.

A.3. Comparison of the crystal structures of Ba_2SiO_4 and $BaSi_2$

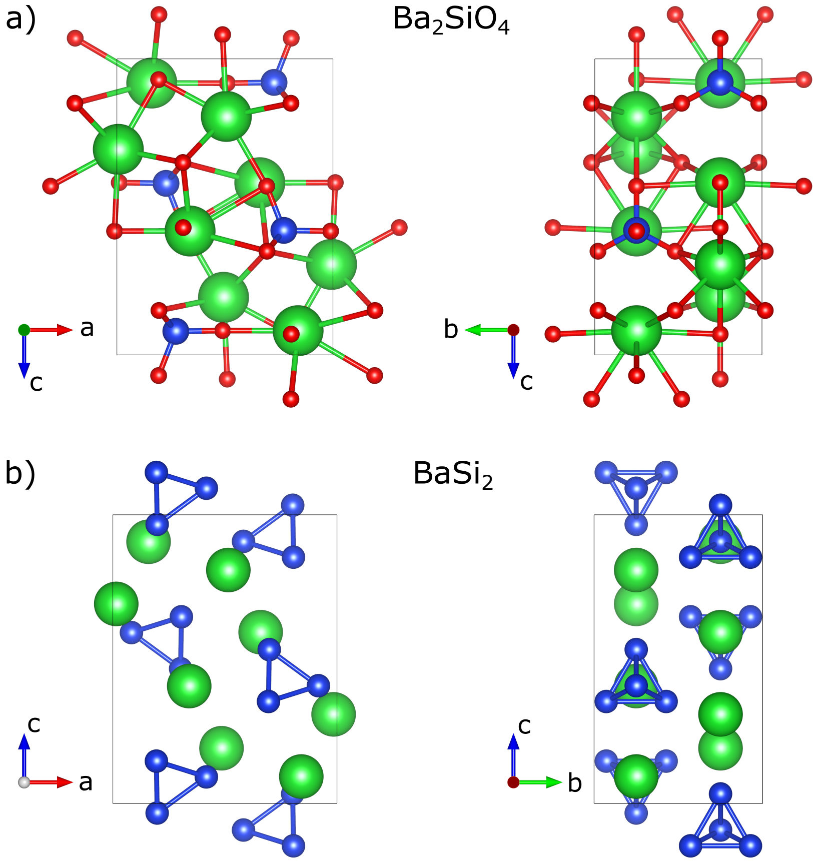

Figure A.6.: The crystal structures of Ba_2SiO_4 (a) and $BaSi_2$ (b) are compared. Green: Ba, blue: Si, red: O. The wire boxes mark the unit cells. Drawn with VESTA [50] with data from [51, 112].

Compound	**a / Å**	**b / Å**	**c / Å**
Ba_2SiO_4	7.602	5.884	10.413
$BaSi_2$	9.009	6.778	11.602

Table A.1.: Lattice constants of Ba_2SiO_4 [51] and $BaSi_2$ [112].

Bibliography

[1] Islam, S., Hofmann, K. R., Feldhoff, A. & Pfnür, H. Structural, Dielectric, and Interface Properties of Crystalline Barium Silicate Films on Si(100): A Robust High-κ Material. *Physical Review Applied* **5**, 054006 (2016).

[2] Wallace, R. M. & Wilk, G. D. High-κ Dielectric Materials for Microelectronics. *Critical Reviews in Solid State and Materials Sciences* **28**, 231–285 (2003).

[3] Lo, S.-H., Buchanan, D. A., Taur, Y. & Wang, W. Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's. *IEEE Electron Device Letters* **18**, 209–211 (1997).

[4] Robertson, J. & Wallace, R. M. High-K materials and metal gates for CMOS applications. *Materials Science and Engineering: R: Reports* **88**, 1–41 (2015).

[5] International Technology Roadmap for Semiconductors. URL `http://www.itrs2.net`.

[6] McKee, R. A., Walker, F. J. & Chisholm, M. F. Crystalline Oxides on Silicon: The First Five Monolayers. *Physical Review Letters* **81**, 3014–3017 (1998).

[7] Schlom, D. G., Guha, S. & Datta, S. Gate Oxides Beyond SiO_2. *MRS Bulletin* **33**, 1017–1025 (2008).

[8] Choi, J. H., Mao, Y. & Chang, J. P. Development of hafnium based high-k materials - A review. *Materials Science and Engineering: R: Reports* **72**, 97–136 (2011).

[9] He, G., Sun, Z., Li, G. & Zhang, L. Review and perspective of Hf-based high-k gate dielectrics on silicon. *Crit. Rev. Sol. St. Mat. Sci.* **37**, 131–157 (2012).

[10] Yu, B. *et al.* FinFET scaling to 10 nm gate length. In *IEEE Digest International Electron Devices Meeting* (IEEE, 2002).

[11] Stemmer, S. Thermodynamic considerations in the stability of binary oxides for alternative gate dielectrics in complementary metal–oxide–semiconductors. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* **22**, 791 (2004).

[12] Ando, T. Ultimate Scaling of High-κ Gate Dielectrics: Higher-κ or Interfacial Layer Scavenging? *Materials* **5**, 478–500 (2012).

[13] Nardelli, M. B., Walker, F. J. & McKee, R. A. Crystalline oxides on semiconductors: a future for the nanotransistor. *physica status solidi (b)* **241**, 2279–2286 (2004).

[14] Först, C. J., Ashman, C. R., Schwarz, K. & Blöchl, P. E. The interface between silicon and a high-k oxide. *Nature* **427**, 53–56 (2004).

[15] McKee, R. A., Walker, F. J. & Chisholm, M. F. Physical Structure and Inversion Charge at a Semiconductor Interface with a Crystalline Oxide. *Science* **293**, 468–471 (2001).

[16] Müller-Sajak, D., Islam, S., Pfnür, H. & Hofmann, K. R. Temperature stability of ultra-

thin mixed BaSr-oxide layers and their transformation. *Nanotechnology* **23**, 305202 (2012).

[17] Norton, D. P., Park, C., Lee, Y. E. & Budai, J. D. Strontium silicide termination and silicate epitaxy on (001) Si. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* **20**, 257 (2002).

[18] Barany, R., King, E. G. & Todd, S. S. Heats of Formation of Crystalline Silicates of Strontium and Barium. *Journal of the American Chemical Society* **79**, 3639–3641 (1957).

[19] El Kazzi, M. *et al.* Epitaxial growth of SrO on Si(001): Chemical and thermal stability. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **25**, 1505–1511 (2007).

[20] Genevès, T. *et al.* Elaboration and characterization of barium silicate thin films. *Micron* **39**, 1145–1148 (2008).

[21] Genevès, T. *et al.* Photoemission study of the reactivity of barium towards SiO_x thermal films. *Surface Science* **605**, 1704–1710 (2011).

[22] Liu, Z., Lin, P.-T., Wessels, B. W., Yi, F. & Ho, S.-T. Nonlinear photonic crystal waveguide structures based on barium titanate thin films and their optical properties. *Applied Physics Letters* **90**, 201104 (2007).

[23] Bibes, M., Villegas, J. E. & Barthélémy, A. Ultrathin oxide films and interfaces for electronics and spintronics. *Advances in Physics* **60**, 5–84 (2011).

[24] Koch, J., Müller-Caspary, K. & Pfnür, H. Matching different symmetries with an atomically sharp interface: Epitaxial Ba2SiO4 on Si(001). *Physical Review Materials* **4** (2020).

[25] Sze, S. M. & Lee, M. K. *Semiconductor Devices: Physics and Technology* (Wiley, 2012), third edn.

[26] Sze, S. M. & Ng, K. K. *Physics of Semiconductor Devices* (Wiley, 2006), third edn.

[27] Robertson, J. High dielectric constant gate oxides for metal oxide Si transistors. *Reports on Progress in Physics* **69**, 327–396 (2005).

[28] Robertson, J. Band offsets of wide-band-gap oxides and implications for future electronic devices. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* **18**, 1785 (2000).

[29] Robertson, J. & Peacock, P. W. Atomic structure, band offsets, growth and defects at high-K oxide: Si interfaces. *Microelectronic Engineering* **72**, 112–120 (2004).

[30] Mistry, K. *et al.* *IEEE TechDigest IEDM 10.2* (2007).

[31] Frank, M. M. High-k / metal gate innovations enabling continued CMOS scaling. In *2011 Proceedings of the European Solid-State Device Research Conference (ESSDERC)* (IEEE, 2011).

[32] Robertson, J. & Peacock, P. W. Atomic Structure, Interfaces and Defects of High Dielectric Constant Gate Oxides. In Demkov, A. A. & Navrotsky, A. (eds.) *Materials Fundamentals of Gate Dielectrics*, 179–214 (Springer, 2005).

[33] Harrison, W. A. *Electronic Structure* (W. H. Freeman, San Francisco, 1979).

[34] Gutowski, M. *et al.* Thermodynamic stability of high-K dielectric metal oxides ZrO_2 and HfO_2 in contact with Si and SiO_2. *Applied Physics Letters* **80**, 1897–1899 (2002).

[35] Wu, Y. H., Yang, M. Y., Chin, A., Chen, W. J. & Kwei, C. M. Electrical characteristics of high quality La_2O_3 gate dielectric with equivalent oxide thickness of 5 Å. *IEEE Electron Device Letters* **21**, 341–343 (2000).

[36] Kwo, J. *et al.* High ϵ gate dielectrics Gd_2O_3 and Y_2O_3 for silicon. *Applied Physics Letters* **77**, 130–132 (2000).

[37] Fissel, A., Osten, H. J. & Bugiel, E. Towards understanding epitaxial growth of alternative high-K dielectrics on Si(001): Application to praseodymium oxide. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* **21**, 1765 (2003).

[38] Wilk, G. D., Wallace, R. M. & Anthony, J. M. Hafnium and zirconium silicates for advanced gate dielectrics. *Journal of Applied Physics* **87**, 484–492 (2000).

[39] Rayner, G. B., Kang, D. & Lucovsky, G. Spectroscopic study of chemical phase separation in zirconium silicate alloys. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* **21**, 1783 (2003).

[40] Zhu, J., Liu, Z. G. & Feng, Y. Thermal stability and electrical properties of pulsed laser-deposited Hf-silicate thin films for high-k gate dielectric applications. *Journal of Physics D: Applied Physics* **36**, 3051–3056 (2003).

[41] Copel, M. *et al.* Characterization of silicate/Si(001) interfaces. *Applied Physics Letters* **81**, 4227–4229 (2002).

[42] Copel, M., Reuter, M. C. & Jamison, P. Interlayer composition of HfO_2/Si(001) films. *Applied Physics Letters* **85**, 458–460 (2004).

[43] Maria, J.-P. *et al.* High temperature stability in lanthanum and zirconia-based gate dielectrics. *Journal of Applied Physics* **90**, 3476–3482 (2001).

[44] Kim, H. & McIntyre, P. C. Spinodal decomposition in amorphous metal–silicate thin films: Phase diagram analysis and interface effects on kinetics. *Journal of Applied Physics* **92**, 5094–5102 (2002).

[45] Stemmer, S. *et al.* Application of Metastable Phase Diagrams to Silicate Thin Films for Alternative Gate Dielectrics. *Japanese Journal of Applied Physics* **42**, 3593–3597 (2003).

[46] Aarik, J., Aidla, A., Mändar, H., Sammelselg, V. & Uustare, T. Texture development in nanocrystalline hafnium dioxide thin films grown by atomic layer deposition. *Journal of Crystal Growth* **220**, 105–113 (2000).

[47] Choi, C. H., Jeon, T. S., Clark, R. & Kwong, D. L. Electrical properties and thermal stability of CVD HfO_xN_y gate dielectric with poly-Si gate electrode. *IEEE Electron Device Letters* **24**, 215–217 (2003).

[48] Lee, B. H., Kang, L., Nieh, R., Qi, W.-J. & Lee, J. C. Thermal stability and electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing. *Applied Physics Letters* **76**, 1926–1928 (2000).

[49] Kim, H., McIntyre, P. C., Chui, C. O., Saraswat, K. C. & Stemmer, S. Engineering chemically abrupt high-k metal oxide/silicon interfaces using an oxygen-gettering metal overlayer. *Journal of Applied Physics* **96**, 3467–3472 (2004).

[50] Momma, K. & Izumi, F. VESTA 3 for three-dimensional visualization of crystal, volumetric and morphology data. *Journal of Applied Crystallography* **44**, 1272–1276 (2011).

[51] Persson, K. Materials Data on Ba_2SiO_4 (SG:62) by Materials Project, ID: mp-17612 (2014).

[52] Persson, K. Materials Data on $BaSiO_3$ (SG:19) by Materials Project, ID: mp-7339 (2014).

[53] Persson, K. Materials Data on $Ba_2Si_3O_8$ by Materials Project, ID: mp-29222 (2020).

[54] Villars, P. & Cenzual, K. Ba_2SiO_4 ($Ba_2[SiO_4]$) Crystal Structure. Inorganic Solid Phases, Springer Materials (online database), ID: sd_0550074 (2016). URL `https://materials.springer.com/isp/crystallographic/docs/sd_0550074`.

[55] Pieper, G., Eysel, W. & Hahn, T. Solid Solubility and Polymorphism in the System Sr_2SiO_4-Sr_2GeO_4-Ba_2GeO_4-Ba_2SiO_4. *Journal of the American Ceramic Society* **55**, 619–622 (1972).

[56] Davisson, C. & Germer, L. H. Diffraction of Electrons by a Crystal of Nickel. *Physical Review* **30**, 705–740 (1927).

[57] Horn-von Hoegen, M. Growth of semiconductor layers studied by spot profile analysing low energy electron diffraction – Part II. *Zeitschrift für Kristallographie - Crystalline Materials* **214**, 684–721 (1999).

[58] Seah, M. P. & Dench, W. A. Quantitative electron spectroscopy of surfaces: A standard data base for electron inelastic mean free paths in solids. *Surface and Interface Analysis* **1**, 2–11 (1979).

[59] Conrad, E. Handbook of Surface Science, Chapter 7 – Diffraction Methods, 271–360 (1996). Elsevier.

[60] Heinz, K. Is there a future for LEED intensities? *Applied Physics A Solids and Surfaces* **41**, 3–19 (1986).

[61] Heinz, K., Kottcke, M., Löffler, U. & Döll, R. Recent advances in LEED surface crystallography. *Surface Science* **357-358**, 1–9 (1996).

[62] Scheithauer, U., Meyer, G. & Henzler, M. A new LEED instrument for quantitative spot profile analysis. *Surface Science* **178**, 441–451 (1986).

[63] Zahl, P. & von Hoegen, M. H. Third-generation conical spot profile analyzing low-energy electron diffraction. *Review of Scientific Instruments* **73**, 2958–2962 (2002).

[64] Wagner, C. D., Riggs, W. M., Davis, L. E. & Moulder, J. F. *Handbook of X-ray Photoelectron Spectroscopy* (Perkin Elmer, 1979).

[65] Powell, C. X-ray Photoelectron Spectroscopy Database XPS, Version 4.1, NIST Standard Reference Database 20 (1989). URL `http://srdata.nist.gov/xps/`.

[66] Voigts, F. *Wechselwirkung von Wasser, Kohlendioxid und weiteren Gasen mit den Oberflächen von akzeptordotiertem Strontiumtitanat.* Ph.D. thesis, TU Clausthal (2010).

[67] Briggs, D. & Seah, M. P. *Practical Surface Analysis by Auger and X-ray Photoelectron Spectroscopy* (Wiley, 1983).

[68] Woodruff, D. P. & Delchar, T. A. *Modern techniques of surface science* (Cambridge Solid State Series, 1986).

[69] Lang, N. D. & Williams, A. R. Core holes in chemisorbed atoms. *Physical Review B* **16**, 2408–2419 (1977).

[70] Krause, M. O. & Ferreira, J. G. K X-ray emission spectra of Mg and Al. *Journal of Physics B: Atomic and Molecular Physics* **8**, 2007–2014 (1975).

[71] Ertl, G. & Küppers, J. *Low energy electrons and surface chemistry* (VCH, 1985).

[72] Powell, C. J. & Jablonski, A. NIST Electron Inelastic-Mean-Free-Path Database, Version 1.2, SRD 71, National Institute of Standards and Technology, Gaitherberg, MD (2010).

[73] Streetman, B. G. & Banerjee, S. K. *Solid State Electronic Devices* (Pearson, 2016), seventh edn.

[74] Garrett, C. G. B. & Brattain, W. H. Physical Theory of Semiconductor Surfaces. *Physical Review* **99**, 376–387 (1955).

[75] Schroder, D. K. *Semiconductor Material and Device Characterization* (Wiley, 2005), third edn.

[76] Denhoff, M. W. An accurate calculation of spreading resistance. *Journal of Physics D: Applied Physics* **39**, 1761–1765 (2006).

[77] Yang, K. J. & Hu, C. MOS capacitance measurements for high-leakage thin dielectrics. *IEEE Transactions on Electron Devices* **46**, 1500–1501 (1999).

[78] Budde, M. *Programmierung einer Software zur automatisierten Auswertung von Kapazitäts-Spannungs-Messungen an MOS-Strukturen in Maple.* Studienarbeit, Gottfried Wilhelm Leibniz Universität Hannover (2013).

[79] Zachariae, J. *Kristalline und gitterangepasste* $Ba_{0.7}Sr_{0.3}O$*-Schichten auf ebenen und vizinialen Si(001)-Oberflächen.* Ph.D. thesis, Gottfried Wilhelm Leibniz Universität Hannover (2006).

[80] Nicollian, E. H. & Brews, J. R. *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, 2003). Wiley Classics Library Edition.

[81] Piskorski, K. & Przewlocki, H. M. The methods to determine flat-band voltage V_{FB} in semiconductor of a MOS structure. In *The 33rd International Convention MIPRO*, 37–42 (2010).

[82] Winter, R., Ahn, J., McIntyre, P. C. & Eizenberg, M. New method for determining flat-band voltage in high mobility semiconductors. *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* **31**, 030604 (2013).

[83] Hillard, R. J., Heddleson, J. M., Zier, D. A., Rai-Choudhury, P. & Schroder, D. K. Direct and rapid method for determining flatband voltage from non-equilibrium capacitance voltage data. *Diagnostic Techniques for Semiconductor Materials and Devices, NJ, Pennington: Electrochem. Soc.* 261–274 (1992).

[84] Terman, L. M. An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes. *Solid-State Electronics* **5**, 285–299 (1962).

[85] Zaininger, K. H. & Warfield, G. Limitations of the MOS capacitance method for the

determination of semiconductor surface properties. *IEEE Transactions on Electron Devices* **12**, 179–193 (1965).

[86] Nicollian, E. H., Goetzberger, A. & Lopez, A. D. Expedient method of obtaining interface state properties from MIS conductance measurements. *Solid-State Electronics* **12**, 937–944 (1969).

[87] Brews, J. R. Rapid interface parameterization using a single MOS conductance curve. *Solid-State Electronics* **26**, 711–716 (1983).

[88] Müller-Sajak, D. *Herstellung und Charakterisierung von (Ba,Sr)O basierten MOS Dioden und ultradünnen Isolatorfilmen auf Si(001).* Ph.D. thesis, Gottfried Wilhelm Leibniz Universität Hannover (2013).

[89] Islam, S. *Growth, structuring and interface manipulation of ultrathin oxide and silicate films on silicon single crystal surfaces.* Ph.D. thesis, Gottfried Wilhelm Leibniz Universität Hannover (2015).

[90] Casa Software Ltd. CasaXPS Manual 2.3.15, Processing Software for XPS Spectra (2009). URL `http://www.casaxps.com/ebooks/OrangeBookRev1.3ebook.pdf`.

[91] Kovács, A., Schierholz, R. & Tillmann, K. FEI Titan G2 80-200 CREWLEY. *Journal of large-scale research facilities JLSRF* **2**, A43 (2016).

[92] Verhoeven, J. A. T. & van Doveren, H. XPS studies on Ba, BaO and the oxidation of Ba. *Applications of Surface Science* **5**, 361–373 (1980).

[93] Qiu, S. L., Lin, C. L., Chen, J. & Strongin, M. Photoemission studies of the low-temperature reaction of metals and oxygen. *Physical Review B* **41**, 7467–7473 (1990).

[94] Lettieri, J., Haeni, J. H. & Schlom, D. G. Critical issues in the heteroepitaxial growth of alkaline-earth oxides on silicon. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **20**, 1332–1340 (2002).

[95] Norga, G. J. *et al.* Phase of reflection high-energy electron diffraction oscillations during (Ba,Sr)O epitaxy on Si(100): A marker of Sr barrier integrity. *Applied Physics Letters* **87**, 262905 (2005).

[96] Reiner, J. W., Garrity, K. F., Walker, F. J., Ismail-Beigi, S. & Ahn, C. H. Role of Strontium in Oxide Epitaxy on Silicon (001). *Physical Review Letters* **101**, 105503 (2008).

[97] Fan, W. C. & Ignatiev, A. Identification of ordered atomic structures of Ba on the Si(100) surface. *Surface Science* **253**, 297–302 (1991).

[98] Hu, X. *et al.* Phases of Ba adsorption on Si(100)-(2×1) studied by LEED and AES. *Surface Science* **426**, 69–74 (1999).

[99] Ojima, K., Yoshimura, M. & Ueda, K. Observation of the Si(100)"1×2"-Ba surface by scanning tunneling microscopy. *Physical Review B* **65**, 075408 (2002).

[100] Persson, K. Materials Data on Si (SG:227) by Materials Project, mp-149 (2014).

[101] Fredrickson, K. D., Seo, H. & Demkov, A. A. Mechanism of oxidation protection of the Si(001) surface by sub-monolayer Sr template. *Journal of Applied Physics* **120**, 065301 (2016).

[102] Segal, Y. *et al.* Atomic Structure of the Epitaxial BaO/Si(001) Interface. *Physical Review Letters* **102**, 116101 (2009).

[103] Waldrop, J. R., Grant, R. W., Kowalczyk, S. P. & Kraut, E. A. Measurement of semiconductor heterojunction band discontinuities by x-ray photoemission spectroscopy. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **3**, 835–841 (1985).

[104] Zachariae, J. & Pfnür, H. Growth conditions, stoichiometry, and electronic structure of lattice-matched SrO/BaO mixtures on Si(100). *Physical Review B* **72**, 075410 (2005).

[105] Islam, S., Müller-Sajak, D., Hofmann, K. R. & Pfnür, H. Epitaxial thin films of BaSrO as gate dielectric. *Microelectronic Engineering* **109**, 152–155 (2013).

[106] Lenahan, P. M. & Dressendorfer, P. V. Hole traps and trivalent silicon centers in metal/oxide/silicon devices. *Journal of Applied Physics* **55**, 3495–3499 (1984).

[107] Hu, S. M., Kerr, D. R. & Gregor, L. V. Evidence of hole injection and trapping in silicon nitride films prepared by reactive sputtering. *Applied Physics Letters* **10**, 97–99 (1967).

[108] San, H., Chen, X., Xu, P., Li, G. & Zhan, L. Using metal-insulator-semiconductor capacitor to investigate the charge accumulation in capacitive RF MEMS switches. In *2008 3rd IEEE International Conference on Nano/Micro Engineered and Molecular Systems* (IEEE, 2008).

[109] Lin, L. & Robertson, J. Atomic mechanism of flat-band voltage shifts at La_2O_3, Al_2O_3 and Nb_2O_5 capping layers. *Microelectronic Engineering* **86**, 1743–1746 (2009).

[110] Sell, B., Schumann, D. & Krautschneider, W. H. Fast interface characterization of tunnel oxide MOS structures. *IEEE Transactions on Nanotechnology* **1**, 110–113 (2002).

[111] Persson, K. Materials Data on $BaSi_2O_5$ (SG:62) by Materials Project, ID: mp-3031 (2014).

[112] Persson, K. Materials Data on $BaSi_2$ by Materials Project, ID: mp-1477 (2020).

[113] Gusev, E. P. *et al. IEEE Tech Digest IEDM* 455 (2001).

[114] Tirmali, P. M., Khairnar, A. G., Joshi, B. N. & Mahajan, A. M. Structural and electrical characteristics of RF-sputtered HfO_2 high-k based MOS capacitors. *Solid-State Electronics* **62**, 44–47 (2011).

[115] Singh, V., Shashank, N., Kumar, D. & Nahar, R. Investigation of the interface trap density and series resistance of a high-k HfO_2-based MOS capacitor: before and after 50 MeV Li^{3+}ion irradiation. *Radiation Effects and Defects in Solids* **166**, 80–88 (2011).

[116] Lee, S. J., Choi, C. H., Kamath, A., Clark, R. & Kwong, D. L. Characterization and reliability of dual high-k gate dielectric stack (poly-Si-HfO_2-SiO_2) prepared by in situ RTCVD process for system-on-chip applications. *IEEE Electron Device Letters* **24**, 105–107 (2003).

[117] Kakushima, K. *et al.* Interface and electrical properties of La-silicate for direct contact of high-k with silicon. *Solid-State Electronics* **54**, 715–719 (2010).

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List of publications

1. **Julian Koch, Knut Müller-Caspary and Herbert Pfnür**
   Matching different symmetries with an atomically sharp interface: Epitaxial Ba_2SiO_4 on Si(001)
   Phys. Rev. Materials **4**, 013401 (2020), DOI: 10.1103/PhysRevMaterials.4.013401
2. **Julian Koch, Philipp Kröger, Herbert Pfnür and Christoph Tegenkamp**
   Surface state conductivity in epitaxially grown $Bi_{1-x}Sb_x(111)$ films
   New J. Phys. **18**, 093012 (2016), DOI: 10.1088/1367-2630/18/9/093012
3. **Annas Bin Ali, Diana Slawig, Anja Schlosser, Julian Koch, Nadja Bigall, Franz Renz, Christoph Tegenkamp and Ralf Sindelar**
   Polyacrylonitirile (PAN) based Carbon Nanofibers (CNFs): Probing the synergistic effects of creep assisted stabilization and CNTs doping on graphitization and low dimensional electrical transport
   Carbon **172** 283–295 (2021), DOI: 10.1016/j.carbon.2020.10.033
4. **Doaa Abdelbarey, Julian Koch, Zamin Mamiyev, Christoph Tegenkamp and Herbert Pfnür**
   Thickness dependent coherent and incoherent scattering in electronic transport through epitaxial nontrivial Bi quantum films
   Phys. Rev. B **102**, 115409 (2020), DOI: 10.1103/PhysRevB.102.115409
5. **Yuping Liu, Shuangying Ma, Lifeng Liu, Julian Koch, Marina Rosebrock, Taoran Li, Frederik Bettels, Tao He, Herbert Pfnür, Nadja C. Bigall, Armin Feldhoff, Fei Ding and Lin Zhang**
   Nitrogen Doping Improves the Immobilization and Catalytic Effects of Co_9S_8 in Li-S Batteries
   Advanced Functional Materials **30**, 2002462 (2020), DOI: 10.1002/adfm.202002462
6. **Dániel Zámbó, Anja Schlosser, Pascal Rusch, Franziska Lübkemann, Julian Koch, Herbert Pfnür and Nadja C. Bigall**
   A Versatile Route to Assemble Semiconductor Nanoparticles into Functional Aerogels by Means of Trivalent Cations
   Small 1906934 (2020), DOI: 10.1002/smll.201906934
7. **A. B. Ali, F. Renz, J. Koch, C. Tegenkamp and R. Sindelar**
   Graphene Nanoplatelet (GNPs) Doped Carbon Nanofiber (CNF) System: Effect of GNPs on the Graphitic Structure of Creep Stress and Non-Creep Stress Stabilized Polyacrylonitrile (PAN)
   Nanomaterials **10**, 351 (2020), DOI: 10.3390/nano10020351
8. **Anjali Chaudhary, Devesh K. Pathak, Manushree Tanwar, Julian Koch, Herbert Pfnür and Rajesh Kumar**
   Polythiophene-nanoWO_3 bilayer as an electrochromic infrared filter: a transparent heat shield

J. Mater. Chem. C **8**, 1773 (2019), DOI: 10.1039/c9tc05523a

9. **Wegdan Ramadan, Ralf Dillert, Julian Koch, Christoph Tegenkamp and Detlef W. Bahnemann**
   Changes in the solid-state properties of bismuth iron oxide during the photocatalytic reformation of formic acid
   Catalysis Today **326**, 22 (2019), DOI: 10.1016/j.cattod.2018.09.003

10. **Soukaina Akel, Ralf Dillert, Narmina O. Balayeva, Redouan Boughaled, Julian Koch, Mohammed El Azzouzi and Detlef W. Bahnemann**
    Ag/Ag$_2$O as a Co-Catalyst in TiO$_2$ Photocatalysis: Effect of the Co-Catalyst/ Photocatalyst Mass Ratio
    Catalysts **8**, 647 (2018), DOI: 10.3390/catal8120647

11. **U. Alam, S. Kumar, D. Bahnemann, J. Koch, C. Tegenkamp and M. Muneer**
    Harvesting visible light with MoO$_3$ nanorod modified by Fe(III) nanocluster for effective photocatalytic degradation of organic pollutants
    Phys. Chem. Chem. Phys. **20**, 4538 (2018), DOI: 10.1039/C7CP08206A

12. **J. Aprojanz, M. Wehr, B. Dreyer, J. Wiegand, J. Baringhaus, J. Koch, R. Sindelar and C. Tegenkamp**
    Highly anisotropic electronic conductivity in PAN-based carbon nanofibers
    J. Phys. Condens. Matter **29**, 494002 (2017), DOI: 10.1088/1361-648X/aa9494

13. **A. Wollbrink, C. H. Rüscher, K. Volgmann, J. Koch, A. Breuksch, C. Tegenkamp and J. Caro**
    Improved hydrogen selectivity of Surface Modified Graphite (SMG) membranes: Permeation experiments and characterization by micro-Raman spectroscopy
    Journal of Membrane Science **528**, 316 (2017), DOI: 10.1016/j.memsci.2016.12.067

14. **P. Justin Jesuraj, R. Parameshwari, K. Kanthasamy, J. Koch, H. Pfnür and K. Jeganathan**
    Hole injection enhancement in organic light emitting devices using plasma treated graphene oxide
    Applied Surface Science **397**, 144 (2017), DOI: 10.1016/j.apsusc.2016.11.110

15. **S. Naskar, F. Lübkemann, S. Hamid, A. Freytag, A. Wolf, J. Koch, I. Ivanova, H. Pfnür, D. Dorfs, D. W. Bahnemann and N. C. Bigall**
    Synthesis of Ternary and Quaternary Au and Pt Decorated CdSe/CdS Heteronanoplatelets with Controllable Morphology
    Advanced Functional Materials **27**, 1604685 (2017), DOI: 10.1002/adfm.201604685

16. **A. Wollbrink, K. Volgmann, J. Koch, K. Kanthasamy, C. Tegenkamp, Y. Li, H. Richter, S. Kämnitz, F. Steinbach, A. Feldhoff and J. Caro**
    Amorphous, turbostratic and crystalline carbon membranes with hydrogen selectivity
    Carbon **106**, 93 (2016), DOI: 10.1016/j.carbon.2016.04.062A

17. **S. Heidorn, C. Bertram, J. Koch, K. Boom, F. Matthaei, A. Safiei, J. Henzl, K. Morgenstern**
    Influence of Substrate Surface-Induced Defects on the Interface State between NaCl(100) and Ag(111)
    J. Phys. Chem. C **117**, 16095 (2013), DOI: 10.1021/jp405297h

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