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Designing a Passively Damped Quasi-Two-Level-Operated Modular Multilevel Converter for Drive Applications

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ABSTRACT This paper concentrates on the simplest quasi-two-level PWM operation mode for modular multilevel converters, where the internal currents within the converter are not controlled. The model of the converter is derived and the properties of the inherent resonance circuit within the converter are discussed. The paper proposes an optimized design approach for the converter parameters and shows several challenges in the practical design. The main problem of the studied converter operation mode is the dependency of the converter behavior on many parasitic parameters that can significantly vary in the converter production. Moreover, the paper shows that when the converter losses are low, the optimized converter inductances are below the values expected for realistic converter construction. Consequently, the module capacitances have to be significantly increased or the converter internal currents reach exceedingly high values. Furthermore, a comparison is drawn to the quasi-two-level PWM operation mode in which the leg currents and branch energies are controlled, showing several crucial disadvantages of the studied passively damped operation mode. The utilized models and the basic concepts are validated experimentally on a downscaled converter prototype.

INDEX TERMS Modular multilevel converter, passive damping, quasi-two-level.

I. INTRODUCTION

Quasi-two-level PWM operation of modular multilevel converters (MMCs) is beneficial for an application in medium-voltage low-speed drives. Compared to the conventional operation modes, this operation mode showed a potential to reduce the size and volume of module capacitors by more than one order of magnitude [1]–[3]. This is a significant advantage, since the module capacitors usually represent a considerable part of the total converter volume, weight, and costs. As a trade-off, the quasi-two-level waveforms lead to higher harmonic distortion of the voltages and currents at the converter input and output. Although this requires the use of an additional capacitive filter at the converter input, the output currents are filtered by the inductances of the low-speed machine. Hence, an acceptable THD of machine currents can be achieved without an additional output filter. Moreover, compared to two-level and three-level inverters, the low voltage steps of the quasi-two-level waveforms significantly reduce the problems occurring with long machine cables [3], i.e., the machine overvoltages and the bearing currents observed in e.g. [4], [5]. The other MMC advantages, such as the scalability to various voltage levels, optional redundancy, and a straightforward voltage sharing between the semiconductor switches, apply to the quasi-two-level-operated MMCs as well.

Historically, an operation with quasi-two-level voltage waveforms was proposed by Adam *et al.* [6], [7] for five-level flying-capacitor multilevel converters to reduce the size of the converter's capacitors and to significantly simplify the balancing of those. Later, the quasi-two-level waveforms were utilized in MMCs by Gowaid *et al.* [8] for high-voltage dc-dc applications to feed a medium-frequency transformer. This option was further extended by Sun *et al.* [9] to enable wider voltage ratios between the converter sides.

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A first application of the quasi-two-level voltage waveforms in drives can be credited to Aiello *et al.*. In their research [10], [11], they propose to change the shift of the modulation carriers non-optimally during the low machine speeds. This way, quasi-two-level voltage waveforms are generated at low speeds, thereby stabilizing the converter behavior, and the conventional multilevel operation is applied at high speeds. This is especially advantageous, because the output current ripple of a two-level operation is relatively low at low modulation indices, applied at low machine speeds. However, since the main motivation of the approach was the application at low speeds only, the module capacitance is not significantly reduced compared to that of conventional MMCs.

The quasi-two-level PWM operation for MMCs that applies the quasi-two-level voltage waveforms over the whole operating range to minimize the installed module capacitance was first proposed by the authors of this paper in [1], [12]. One additional novelty compared to the previous quasi-two-level-operated MMCs is that the proposed operation mode actively controls the internal currents of the converter and the energies in the modules. Thus, the transient behavior of the converter is improved and very small module capacitances are feasible. Since then, the control was further refined in [13] and an application of nonlinear branch inductors was studied in [14]. Reference [2] provides a basic discussion on the converter design and studies the application of common-mode voltage injection techniques, such as flat-top modulation. A comprehensive study of this operation mode is included in a PhD thesis [3].

In other research groups, Diab *et al.* proposed quasi-two-level operation for a special six-phase MMC topology in [15] and recently, a quasi-three-level operation for a modified MMC was proposed by Wei *et al.* [16]. Furthermore, Wang *et al.* propose a control approach in [17] that aims to simplify the control approaches from [12], [13]. A similar approach by Gao *et al.* can be found in [18] which additionally uses a model predictive control. Even though the advantages of the approaches from [17], [18] seem attractive, they were only presented for MMCs with module capacitances as high as those of conventionally operated MMCs. Hence, more research needs to be done until these approaches can be considered a more attractive alternative. In [19], [20], Bertoldi *et al.* study an application of $\mathrm{d}v/\mathrm{d}t$ filters and active canceling of the reflected waves for the quasi-two-level PWM-operated MMCs in scenarios, when very long machine cables are applied and only very low overvoltages are acceptable for the machine.

Technically, the aforementioned control approaches for the quasi-two-level-operated MMCs (dc-dc or drive applications) can be separated into three groups:

1) approaches that do not control internal (leg) currents of the converter nor the capacitor energies [8]–[10], [15], [16], [19], [20],
2) approaches that control both the leg currents and the capacitor energies [1]–[3], [12], [13], and
3) simplified approaches that control only leg currents [17], [18].

In the second group of approaches, the behavior of the converter is strictly controlled and the design of its components has been studied comprehensively in [2], [3], [14]. In contrast, the first group of the approaches is characterized by the non-controlled resonant behavior of the converter that strongly depends on the selected converter components. Although such resonant behavior of the MMC was generally studied in the literature, e.g. [21], there are only a few papers analyzing the resonant behavior in the quasi-two-level operation mode. Gowaid *et al.* provide a basic analysis of the converter behavior in the dc-dc applications and study the design of the particular components in [22]. The paper concludes that the branch inductance of the converter should be minimized for the best MMC design and studies the selection of the module capacitances. Milovanović *et al.* provide a more profound analytic study of the converter behavior in [23]. However, the findings and the analysis done for dc-dc applications cannot be directly applied to drive applications, since in drive applications, unlike in dc-dc applications, the output current is almost constant during a modulation period and the duty cycle generally varies in a wide range. Hence, the resonant behavior has to be described in a different manner than in [22], [23] and the design process has to be modified as well. Beside the basic design rules proposed in [10], there is no unified methodology for the design of the quasi-two-level-operated MMCs that do not control internal currents of the converter (first group of approaches) for drive applications.

In this paper, the first group of approaches, that does not control internal currents nor energies, is studied comprehensively for application in drives. The paper provides a deeper analysis of the converter behavior and proposes a novel optimized design process for this quasi-two-level-operated MMC in order to minimize the required module capacitance. Furthermore, the design process is extended by studying the impact of the different parasitic effects within the converter. Experimental validation is provided using a downscaled prototype. Finally, comparisons to the approaches of the second group are drawn and discussed.

II. CONVERTER TOPOLOGY AND SIMULATION MODEL

The MMC topology is depicted in Fig. 1a. As described in the introduction, an additional capacitive filter C_i is applied to the converter dc input. The topology consists of three phase legs, each connecting the input to a single output phase.

For the following investigations, a single-phase-leg model of an MMC is used, as depicted in Fig. 1b. The input voltage is assumed to be sufficiently stabilized by the input capacitor, thus being constant. The output system is modeled as an output inductance L_o, output resistance R_o, and an ideal voltage source $v_{\mathrm{o,s}}$. The common-mode voltage, generated by the superposition of all phase legs, can be considered as an additional voltage source v_cm. For simplicity, the common-mode voltage is assumed to be zero in the single phase model.

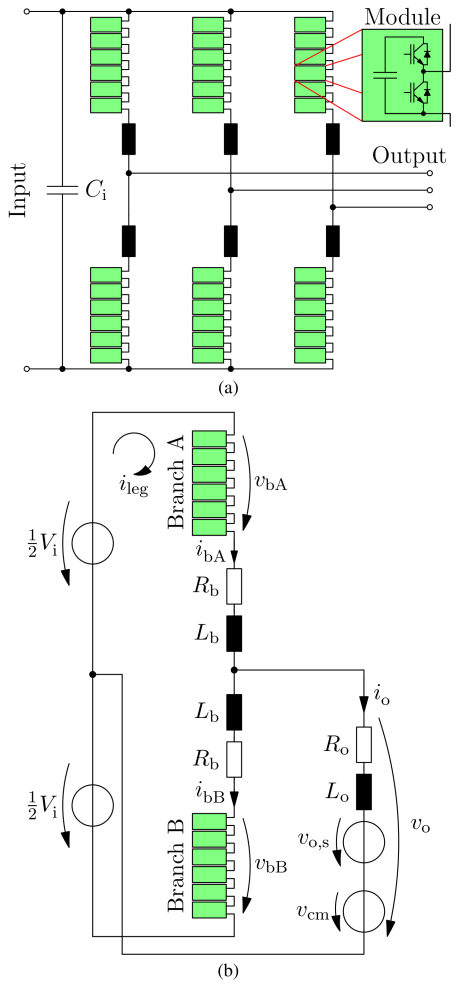

FIGURE 1. Topology: (a) three-phase MMC with an additional input capacitor, (b) MMC phase-leg model.

The converter phase leg comprises two branches, each consisting of a branch inductor L_b and a series connection of n_mpb half-bridge modules. The half-bridge modules comprise each two semiconductor switches and a module capacitor with capacitance C_mod [see Fig. 1a]. The branch resistors R_b represent parasitic resistances within the branches.

Two switching states are considered for the half-bridge modules: inserted ($s = 1$), when the upper IGBT is on and the module capacitor is connected to the module output, and short-circuited ($s = 0$), when the lower IGBT is on and the module output is short-circuited.

The time-domain simulations presented in this paper are implemented in Mathworks Simulink. While the control is implemented in the native Simulink environment, the physical part of the model comprising the converter itself, the loads, and the input voltage source are modeled according to Fig. 1 using Plexim Plecs toolbox. The IGBTs are modeled as ideal switches and the converter losses are represented only by the branch resistors. Unless stated otherwise, the IGBT deadtimes are not modeled and only a single MMC leg is simulated.

III. PRINCIPLE AND IMPLEMENTATION OF PASSIVELY DAMPED OPERATION

The quasi-two-level PWM operation of MMCs that does not control the internal converter currents is similar to the conventional MMC operation that does not control the internal currents, e.g. [21], [24], [25]. The main idea is to keep the total number of inserted modules within one MMC phase leg, defined as the sum of the numbers of inserted modules in the upper branch n_bA and in the lower branch n_bB, constant:

$$n_\mathrm{bA} + n_\mathrm{bB} = N. \tag{1}$$

This constant number of N inserted modules (N module capacitors) effectively "blocks" the input voltage V_i. Depending on the total state of charge of the currently inserted modules, the leg current

$$i_\mathrm{leg} = \frac{1}{2} \cdot (i_\mathrm{bA} + i_\mathrm{bB}), \tag{2}$$

that exchanges the energy between the both branches and the input voltage source, settles on a value stabilizing the module capacitor voltages. The leg current settles in a resonant transient behavior that is passively damped by the branch resistances, thus the name "passively damped operation".

Note that N has to be lower than or equal to the number of modules per branch: $N \leq n_\mathrm{mpb}$. A higher number of modules per branch n_mpb can be applied, if hot-reserve redundancy is required (not further studied in this paper and thus $N = n_\mathrm{mpb}$).

The instantaneous value of the output voltage is set as a difference between the number of inserted modules in the upper branch and in the lower branch:

$$v_\mathrm{o} \approx -\frac{1}{2} \cdot (n_\mathrm{bA} - n_\mathrm{bB}) \cdot \frac{V_\mathrm{i}}{N}. \tag{3}$$

During such operation, the output voltage can have up to $N+1$ levels.

In contrast to the conventional operation, the quasi-two-level PWM operation utilizes only two levels for the most of the time: $v_\mathrm{o} \approx V_\mathrm{i}/2$ ($n_\mathrm{bA} = 0$, $n_\mathrm{bB} = N$) and $v_\mathrm{o} \approx -V_\mathrm{i}/2$ ($n_\mathrm{bA} = N$, $n_\mathrm{bB} = 0$). The other voltage levels are applied only intermediately during the switch-overs between these two levels. These fast switch-overs with many intermediate levels pose further challenges for the study of the already relatively complex resonant behavior of the leg current.

The overall control of the passively damped quasi-two-level PWM operation can be divided into three steps, as shown in Fig. 2. A very similar scheme can be found in [15].

In the first step, the two-level setpoint numbers of inserted modules n'_bA and n'_bB for branches A and B, respectively, are generated according to the setpoint duty cycle

$$\delta^* = \frac{v_\mathrm{o}^*}{V_\mathrm{i}/2}. \tag{4}$$

The duty cycle can be determined by the setpoint ouptut voltage v_o^* and half of the input voltage $V_\mathrm{i}/2$. These two-level

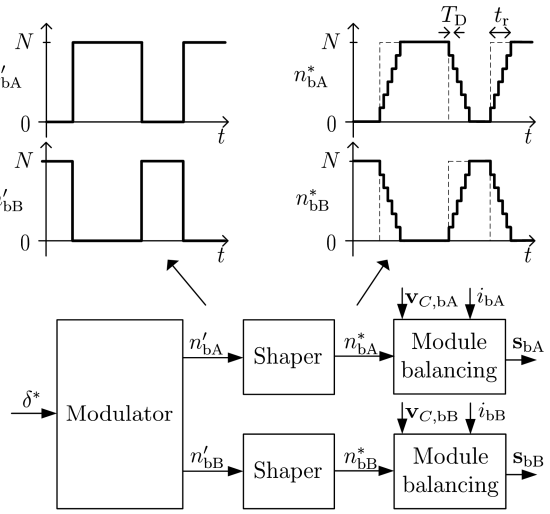

FIGURE 2. Control principle for a single phase leg of a passively damped MMC.

waveforms can be generated by any of the modulation techniques known for two-level voltage source inverters. In this paper, pulse-width modulation (PWM) is applied. As shown in Fig. 2, the setpoint numbers of inserted modules n'_{bA} and n'_{bB} have two discrete levels: zero inserted modules or N modules are inserted. As described above, the total number of inserted modules within the phase leg has to be kept constant

$$n'_{bA} + n'_{bB} = N, \tag{5}$$

so that the input voltage is "blocked" by exactly N modules of a phase leg in each point in time.

In the second step, shapers are applied to reduce the dv/dt of the maximum voltage step through forcing a minimum time delay of T_d between two successive switching instants within the same branch. Hence, the two-level waveforms (n'_{bA}, n'_{bB}) are transformed into the staircase quasi-two-level waveforms (n^*_{bA}, n^*_{bB}) with a rise time $t_r = (N-1)\cdot T_d$. Notice that (1) and (5) are valid for the staircase setpoints as well.

In the last step, the module balancing units select which module should be inserted or short-circuited from the currently available modules each time the setpoint numbers of modules n^*_{bA} or n^*_{bB} change. This decision is made based on the state of charge of the particular modules (the module capacitor voltage vectors for branches A $\mathbf{v}_{C,bA}$ and B $\mathbf{v}_{C,bB}$) and on the direction of the measured branch currents i_{bA} and i_{bB} for branches A and B, respectively. If a module has to be inserted, a non-inserted module with the lowest capacitor voltage is inserted when the corresponding branch current is positive or the non-inserted module with highest voltage is inserted when the branch current is negative. Analogously, if a module has to be short-circuited, an inserted module with highest capacitor voltage is selected for positive branch currents and an inserted module with lowest capacitor voltage is selected for negative currents. The outputs of the module balancing units are the vectors $\mathbf{s}_{bA}$ and $\mathbf{s}_{bB}$ that store the switching states for each module.

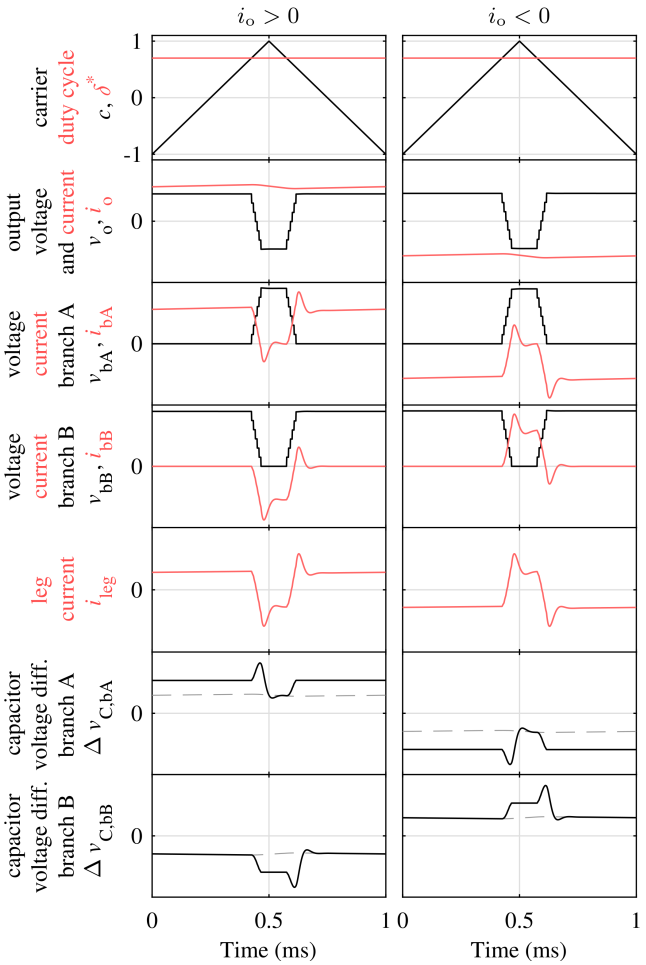

FIGURE 3. Waveforms showing the principle of the passively damped operation over a single PWM period for positive and negative output current. $N = n_{mpb} = 6$. The capacitor voltage differences are determined as the difference between the sum over all N module voltages and the input voltage value: $\Delta v_{C,bA} = \sum v_{C,bA,i} - V_i$, $\Delta v_{C,bB} = \sum v_{C,bB,i} - V_i$.

IV. INVESTIGATION OF THE RESONANT CIRCUIT WITHIN THE MMC

An example of the waveforms over a single PWM period for positive and negative output currents can be observed in Fig. 3. As the figure shows, the branch voltages v_{bA} and v_{bB} are generated by a PWM by comparing the setpoint duty cycle δ^* to the modulation carrier signal c, using the control scheme described in the previous section. This leads to typical quasi-two-level waveforms of the output voltage v_o.

The branch currents

$$\begin{bmatrix} i_{bA} \\ i_{bB} \end{bmatrix} = \begin{bmatrix} \frac{1}{2} & 1 \\ -\frac{1}{2} & 1 \end{bmatrix} \cdot \begin{bmatrix} i_o \\ i_{leg} \end{bmatrix} \tag{6}$$

are described by the superposition of the output current and the leg current.

The behavior of the output current

$$\frac{\mathrm{d}}{\mathrm{d}t} i_\mathrm{o} = -\frac{1}{L_\mathrm{o} + \frac{1}{2}\cdot L_\mathrm{b}} \left(\left(R_\mathrm{o} + \frac{1}{2}\cdot R_\mathrm{b} \right) \cdot i_\mathrm{o} \ldots + \frac{1}{2}\cdot (v_\mathrm{bA} - v_\mathrm{bB}) + v_\mathrm{cm} + v_\mathrm{o,s} \right) \quad (7)$$

is mainly determined by the relatively high output inductance L_o and thus its value i_o does not change significantly within the PWM period [see Fig. 3]. A closed-loop controller can be employed to control the output current by adjusting the setpoint duty cycle δ^* in the same manner as in two-level VSIs. In the following investigations, the output current value is assumed to be constant within the PWM period which is the main difference compared to quasi-two-level-operated MMCs for dc-dc applications.

In contrast, the branch inductances have to be relatively low to enable a highly dynamic behavior of the leg current:

$$\frac{\mathrm{d}}{\mathrm{d}t} i_\mathrm{leg} = -\frac{1}{2\cdot L_\mathrm{b}} \cdot \left(2\cdot R_\mathrm{b}\cdot i_\mathrm{leg} - V_\mathrm{i} + v_\mathrm{bA} + v_\mathrm{bB} \right) \quad . \quad (8)$$

Such highly dynamic behavior is necessary, since the leg current balances the energy between the branches. Nevertheless, this description of leg current is not sufficient, since the branch voltages

$$\begin{aligned} v_\mathrm{bA} &= \sum_{i=1}^{n_\mathrm{mpb}} s_{\mathrm{bA},i}\cdot v_{C,\mathrm{bA},i} \\ v_\mathrm{bB} &= \sum_{i=1}^{n_\mathrm{mpb}} s_{\mathrm{bB},i}\cdot v_{C,\mathrm{bB},i} \end{aligned} \quad (9)$$

are not constant values and are determined by the switching state of each module and the module capacitance voltages

$$\begin{aligned} v_{C,\mathrm{bA},i} &= \frac{1}{C_\mathrm{mod}} \cdot \int s_{\mathrm{bA},i}\cdot i_\mathrm{bA}\ \mathrm{d}t + V_{C,\mathrm{bA},0} \\ v_{C,\mathrm{bB},i} &= \frac{1}{C_\mathrm{mod}} \cdot \int s_{\mathrm{bB},i}\cdot i_\mathrm{bB}\ \mathrm{d}t + V_{C,\mathrm{bB},0} \end{aligned} \quad (10)$$

that change according to the branch currents and thus also according to the leg current [see (6)]. Therefore, the leg current is expected to have a resonant behavior.

Combining (6), (9), (10), and (8), and assuming that the module capacitor voltages within a branch have approximately the same value, the resonant circuit can be simplified into a piecewise-linear equivalent resonant circuit displayed in Fig. 4. In this model, the state-of-charge of the capacitors and their capacitance have to be updated accordingly each time the switching states change.

Each time the switching state is changed, the resonant circuit is excited and the leg current i_leg is led to its new steady-state value $i_{\mathrm{leg},\infty}$ through a resonant transient. Observing Fig. 4, the steady state occurs when the total voltage across the module capacitors remains constant:

$$\frac{\mathrm{d}}{\mathrm{d}t} \left(\int \frac{i_{\mathrm{leg},\infty} + \frac{i_\mathrm{o}}{2}}{\frac{C_\mathrm{mod}}{n_\mathrm{bA}}}\ \mathrm{d}t + \int \frac{i_{\mathrm{leg},\infty} - \frac{i_\mathrm{o}}{2}}{\frac{C_\mathrm{mod}}{n_\mathrm{bB}}}\ \mathrm{d}t \right) = 0. \quad (11)$$

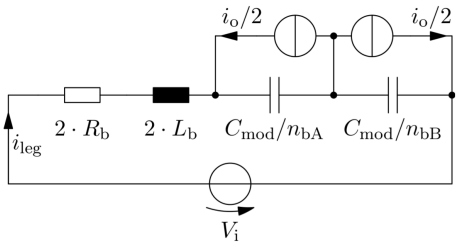

FIGURE 4. Simplified equivalent resonant circuit describing the leg current in generalized case. When n_bA or n_bB is zero, the corresponding capacitor is degraded to a short circuit.

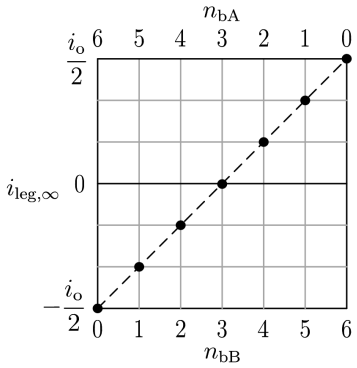

FIGURE 5. Steady-state solutions for leg current depending on the switching state. Example for $N = 6$.

This yields the following solution for the steady-state leg current:

$$i_{\mathrm{leg},\infty} = -\frac{i_\mathrm{o}}{2}\cdot\frac{n_\mathrm{bA} - n_\mathrm{bB}}{N}. \quad (12)$$

This solution is displayed graphically in Fig. 5 for an example MMC with $N = 6$.

Fig. 5 and (12) state that the steady-state solution of the leg current is $i_{\mathrm{leg},\infty} = -i_\mathrm{o}/2$ when N modules of branch A are inserted, and $i_{\mathrm{leg},\infty} = i_\mathrm{o}/2$ when N modules of branch B are inserted. This is in concordance with the steady states of the leg current observable in Fig. 3 which are either $-i_\mathrm{o}/2$ when branch A has high voltage or $i_\mathrm{o}/2$ when branch B has high voltage.

These two steady states are especially advantageous because they do not cause any energy shift between the upper and lower branch. When the voltage in branch A is high $\{n_\mathrm{bA} = N,\ n_\mathrm{bB} = 0\}$, the output current flows solely through branch B which has zero voltage. Consequently, no capacitors are being charged or discharged. Similarly, when the voltage in branch B is high $\{n_\mathrm{bA} = 0,\ n_\mathrm{bB} = N\}$, the output current flows through the short-circuited branch A and the capacitor voltages remain constant. Since these two steady states are applied for the most of the time in quasi-two-level operation, the module capacitors are charged only transiently for a short period of time and a very low branch energy variation is feasible.

The steady-state values for the sum of capacitor voltages of N inserted modules in branch A or branch B can be

determined using Fig. 4 for the cases when $n_{\mathrm{bB}} = 0$ and $n_{\mathrm{bA}} = 0$, respectively. These steady-state values

$$\begin{aligned}\left(\sum v_{C,\mathrm{bA}}\right)_{\infty} &= V_{\mathrm{i}} + 2 \cdot R_{\mathrm{b}} \cdot i_{\mathrm{o}}/2 \\ \left(\sum v_{C,\mathrm{bB}}\right)_{\infty} &= V_{\mathrm{i}} - 2 \cdot R_{\mathrm{b}} \cdot i_{\mathrm{o}}/2\end{aligned} \tag{13}$$

depend on the input voltage and the voltage drop over the branch resistances. These voltage-drop values over the branch resistances $\pm R_{\mathrm{b}} \cdot i_{\mathrm{o}}$ are marked with dashed lines in Fig. 3 for capacitor voltage differences

$$\begin{aligned}\Delta v_{C,\mathrm{bA}} &= \sum_{i=1}^{N} v_{C,\mathrm{bA},i} - V_{\mathrm{i}} \\ \Delta v_{C,\mathrm{bB}} &= \sum_{i=1}^{N} v_{C,\mathrm{bB},i} - V_{\mathrm{i}},\end{aligned} \tag{14}$$

defined as the difference between the sum over all N module voltages and the input voltage value. It can be seen that the capacitors of branch A or branch B achieve these steady-state values when N modules of the corresponding branch are inserted.

Between the two main steady states of leg current $i_{\mathrm{leg},\infty} = \pm i_{\mathrm{o}}/2$, transient behavior occurs with a damped resonant swing of the leg current visible in Fig. 3. This resonant behavior is also visible in both branch currents, which depend on the leg current according to (6), and in the module capacitor voltages.

From Fig. 4, it can be recognized that under condition (1), the resonant circuit, that determines the leg current transient behavior, consists of two branch inductances, two branch resistances, and a series connection of N module capacitors independently of the switching state. This resonant circuit can generally be described by the following two parameters: natural resonance frequency

$$f_0 = \frac{1}{2 \cdot \pi \cdot \sqrt{2 \cdot L_{\mathrm{b}} \cdot \frac{C_{\mathrm{mod}}}{N}}} \tag{15}$$

and damping ratio

$$\zeta = \frac{\alpha}{2 \cdot \pi \cdot f_0} = \frac{2 \cdot R_{\mathrm{b}}}{2} \cdot \sqrt{\frac{\frac{C_{\mathrm{mod}}}{N}}{2 \cdot L_{\mathrm{b}}}}, \tag{16}$$

defined as a ratio between the damping α and the natural resonance frequency f_0. Similar observation of the equivalent resonance circuit was also done by Aiello and Barie [10]. While they also describe the resonance frequency, they do not derive the damping ratio. Nevertheless, the paper states that in order to increase the damping, the module capacitance should be maximized, which is in concordance with (16).

Simplifying the operation mode, it can be assumed that the delay period between the switching instants is $T_{\mathrm{d}} = 0$ and thus, the switch-over between the upper and lower branch occurs immediately. In such a situation, the leg current has to change from $i_{\mathrm{leg},\infty} = -i_{\mathrm{o}}/2$ to $i_{\mathrm{leg},\infty} = i_{\mathrm{o}}/2$ (or vice versa), exciting the resonant circuit. This happens in a well-studied

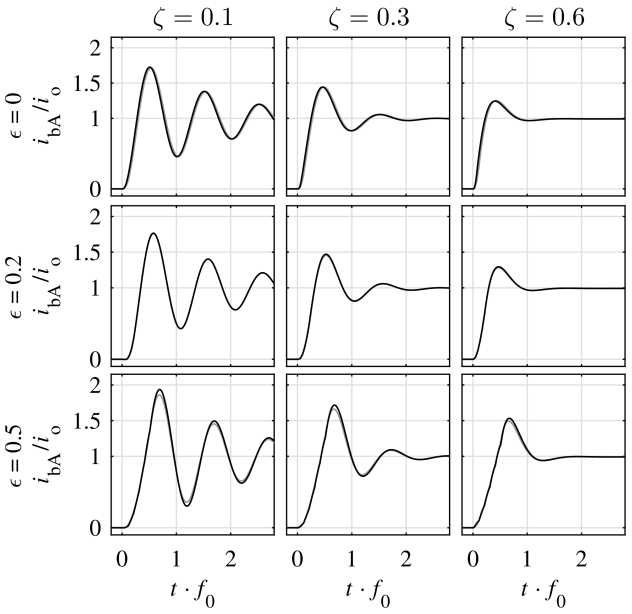

FIGURE 6. Branch current waveforms for different damping ratios ζ and relative rise times of the output voltage $\epsilon = t_{\mathrm{r}} \cdot f_0$. The waveforms were generated using an MMC model for $N = n_{\mathrm{mpb}} = 6$ (black lines) and $N = n_{\mathrm{mpb}} = 11$ (gray lines).

resonant behavior of a damped resonant circuit, swinging at the damped resonance frequency $f_{\mathrm{D}} = f_0 \cdot \sqrt{1 - \zeta^2}$, that depends only on the damping ratio ζ (and the resonance frequency f_0 for scaling in time). The resulting branch current overshoot and the decay rate of the resonant swings for this simplified operation can be observed in the first row of Fig. 6 (for $\epsilon = 0$).

This first row of Fig. 6 shows that the peak value of branch current resonant overshoots declines with increasing damping ratio ζ and that the steady-state value is achieved after a shorter period of time (assuming constant resonance frequency f_0).

In the non-simplified case when the delay time $T_{\mathrm{d}} > 0$, the transient duration is prolonged. After each switching instant, the leg current swings in a similar resonant behavior to its intermediate steady-state value according to (12). However, since the delay time T_{d} is usually significantly shorter than the damped resonance period $1/f_{\mathrm{D}}$, the steady-state value cannot be achieved before the next switching state is applied. While one could expect that the superposition of several smaller resonant swings shifted in time should lead to lower overall peak current overshoot, the opposite is true. On the contrary, the peak current value is increased. This is caused by two effects: First, the intermediate steady-state values of the leg current cause a shift of the branch energy between the upper and lower branch, since the branch currents are non-zero while the module capacitors in both branches are inserted [see Fig. 4 and Fig. 5]. Consequently, the resonant circuit is additionally excited when switching states change. Second, the energy split between the modules is not equal which additionally excites the resonant circuit.

In summary, increasing the delay time T_d increases the variation of module capacitor voltages and the peak value of the current overshoot. The behavior of the leg current determined by the rapid changes in switching states (that are determined by the rather complex module voltage balancing process) is too complex to be described analytically in a meaningful form. However, the behavior can be easily simulated in the time domain. Observing the simulated data for various operating points, it can be stated that the resonant current behavior depends only on the damping ratio ζ and the relative rise time

$$\epsilon = \frac{t_r}{\frac{1}{f_0}} = t_r \cdot f_0 = (N-1) \cdot T_d \cdot f_0 \tag{17}$$

defined as a ratio between the rise time t_r and the resonance period $1/f_0$. Note that there is a slight dependence of the simulated data on the selected number of modules N, since it influences the balancing of the module capacitors and the number of intermediate steady-state steps for the leg current. However, this influence is rather negligible as demonstrated in Fig. 6.

Fig. 6 shows the various waveforms of branch currents for different damping ratios ζ and relative rise times ϵ. For a constant relative rise time ϵ, a similar behavior as for the simplified case with $\epsilon = 0$ can be observed: With increasing damping ratio ζ, the peak branch current overshoot is reduced and the transient behavior takes a lower number of resonance periods until the steady-state value is achieved. Comparing the waveforms for different relative rise times ϵ at a constant damping ratio ζ, it can be seen that increasing the relative rise time ϵ increases the peak branch current value. However, it has only little influence on the number of periods until the leg current stabilizes at its steady-state value.

The behavior of the leg (and branch currents) in Fig. 3 corresponds to $\zeta = 0.6$ and $\epsilon = 0.5$ which is in concordance with the branch current behavior shown in Fig. 6.

In a similar manner, the resonant behavior of the module capacitor voltages could theoretically be studied. Nevertheless, this is not as relevant as the behavior of the branch currents, because the module capacitor voltage variation caused by passively damped quasi-two-level-operated MMCs is generally very low. The reason for this low voltage variation is that the module capacitances are designed relatively high to provide sufficient damping for the system, as described in the next section. Moreover, as will be demonstrated later in Section VI, the module capacitor voltage variation is rather depending on the variation of the dc-link voltage v_i introduced by a finite value of dc-link capacitance C_i.

V. PARAMETER DESIGN

As shown in the previous section, the converter behavior is mainly influenced by the parameters of the resonant circuit. In this section, the design of the parameters, such as branch inductance and module capacitance, are discussed and derived.

In the first part of this section, the idealized converter without practical restrictions is considered for the design. In the second and third parts, the impact of the stray inductances within the system and of the non-ideal semiconductor behavior are shown, adding further restrictions to the design process.

The capacitance C_i of the central dc-link capacitor, that is necessary for a quasi-two-level-operated MMC and displayed in Fig. 1a, also impacts the behavior of the converter, especially when its value is low. This impact is later investigated in Section VI.

A. IDEALIZED CONVERTER

The resonant behavior of the leg current can be completely described by the parameters f_0, ζ, and ϵ, described by (15), (16), and (17). These further depend on the following parameters:

- module capacitance C_{mod},
- branch inductance L_b,
- branch resistance R_b,
- number of inserted modules N, and
- required rise time t_r.

The number of inserted modules N and the branch resistance R_b are determined by the selected semiconductor devices – in particular, their blocking voltage and conducting characteristics. Although it is theoretically possible to increase the branch resistance artificially by adding additional discrete resistors, it is not advisable, since the branch resistance is linked to the converter losses. The required rise time t_r is determined by the maximum dv/dt of the output voltage allowed for the application. Another restriction is the maximum peak value of the branch current, since this impacts the size of necessary semiconductor devices and possibly the electromagnetic interference during the resonant current overshoots. Furthermore, a possibly high maximum duty cycle δ_{max} is desirable for the defined PWM frequency f_{PWM}, required by the application.

In the design process, the module capacitance C_{mod} and the branch inductance L_b are handled as the only degrees of freedom and their values have to be selected to satisfy all of the aforementioned requirements.

Eliminating f_0 from (15) – (17), the module capacitance and the branch inductance

$$C_{mod} = N \cdot \frac{1}{2 \cdot \pi} \cdot \frac{\zeta}{\epsilon} \cdot \frac{t_r}{R_b} \tag{18}$$

$$L_b = \frac{1}{4 \cdot \pi} \cdot \frac{1}{\zeta \cdot \epsilon} \cdot t_r \cdot R_b \tag{19}$$

can be expressed as functions of the rise time t_r, the branch resistance R_b, number of modules N, damping ratio ζ, and the relative rise time ϵ. As mentioned above, the branch resistance R_b, the number of modules N, and the rise time t_r depend on the applied semiconductor switches and the particular application. Hence, they are handled as constants. It can be recognized that both the value of module capacitance and the value of branch inductance are directly proportional to the

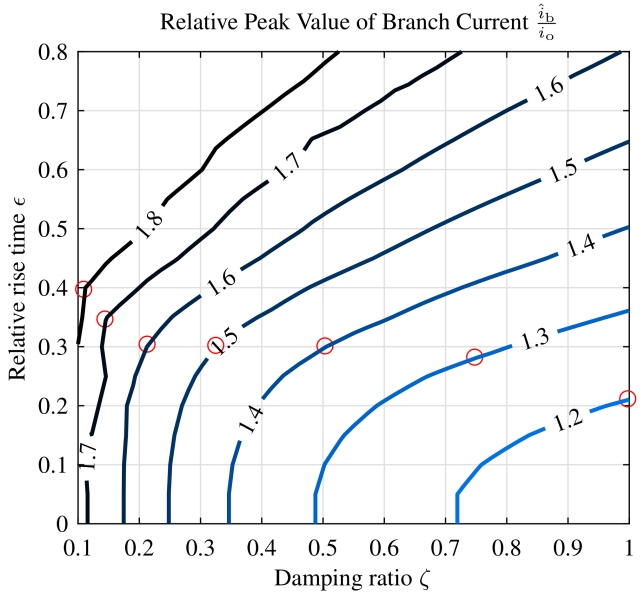

FIGURE 7. Peak value of branch current $\hat{i}_b$ relative to output current value i_o depending on the damping ratio ζ and the relative rise time ϵ. Generated using a simulation of an MMC with $N = 6$ over 640 operating points. The circles mark the designs with minimum module capacitance.

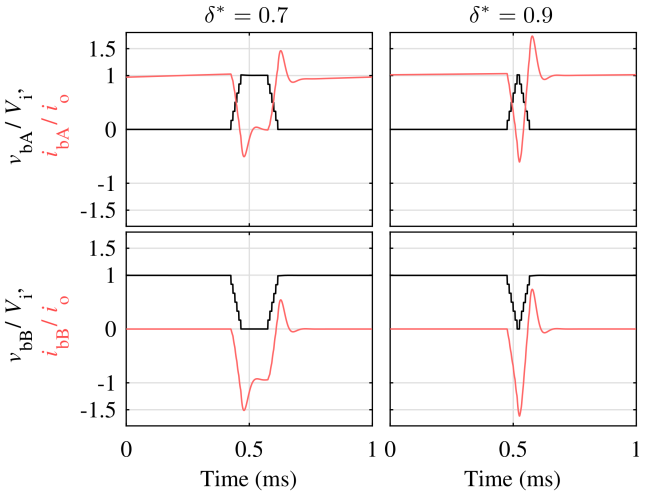

FIGURE 8. Waveforms showing the increase of peak branch current when the duty cycle is too high. $N = n_{mpb} = 6$, damping ratio $\zeta = 0.6$, ratio $\epsilon = 0.5$.

rise time value t_r. Consequently, decreasing the dv/dt of the output voltage (increasing the rise time value) leads to higher installed volume of both capacitors and inductors. Furthermore, it can be seen that the increased branch resistance leads to lower capacitances and higher inductance. The damping ratio ζ and ratio ϵ are degrees of freedom. To decrease the capacitance, the damping ratio ζ should be chosen as low as possible and the ratio ϵ should be chosen as high as possible.

However, the possible combinations of the damping ratio ζ and the relative rise time ϵ are limited by the restriction for the maximum allowed peak branch current. In Fig. 7, a contour plot shows the dependence of the peak branch current relative to the output current $\hat{i}_b/i_o$ on the damping ratio ζ and the relative rise time ϵ. This plot determines which combinations of ratios ζ and ϵ are feasible, if a particular peak branch current value is not to be exceeded.

The circles in Fig. 7 mark the optimum designs for each maximum allowed peak branch current value. These designs are optimized for a minimum module capacitance. The exact positions of these points can be found in Table 4 in appendix.

The plot in Fig. 7 was generated by the same simulations as Fig. 6 in 640 different operating points. The graph can be approximated by a polynomial expression (29) shown in the appendix.

At this point, it is important to note that the transient behavior of the leg and branch currents displayed in Fig. 6 and Fig. 7 was investigated for the case that the leg current achieved its steady-state value before the next transient started. If the time period T_{on} during which the N modules of a single branch are inserted is not sufficiently long for the leg current to settle to its steady-state value, the current overshoot can be significantly higher. This occurs when duty cycle δ^* approaches one or minus one.

The increased branch current overshoot for high duty cycles is demonstrated in Fig. 8. On the left side of the figure, there are the waveforms of the branch currents and branch voltages of the simulation from Fig. 3, showing the case when the duty cycle is $\delta^* = 0.7$. It can be seen that N modules are inserted in branch A for a sufficient time period for the branch current to settle at its steady-state value before the next transient occurs. Consequently, the transient behavior of the branch current is in concordance with Fig. 6. When the duty cycle is increased to $\delta^* = 0.9$, as displayed on the right side of Fig. 8, the time in which the N modules of branch A are inserted $T_{on,bA}$ is not sufficient anymore and a significantly higher branch current overshoot occurs.

Neglecting the staircase waveform of branch voltages ($\epsilon = 0$), the envelope of the branch currents

$$\mathrm{env}\left(\frac{i_b}{i_o}\right) = 1 + \mathrm{e}^{-\zeta \cdot 2 \cdot \pi \cdot f_0 \cdot t} \tag{20}$$

can be approximated by an exponential decay function that depends on the damping ratio ζ and on the resonant frequency f_0. The relation between the envelope function and the branch current function is demonstrated for a single example in Fig. 9.

Requiring that the branch current i_b has decayed below $(1+\beta) \cdot i_o$ at time point $t = T_{on,min}$, (20) can be used to express the minimum required time period

$$T_{on,min} = \frac{\ln(\frac{1}{\beta})}{2 \cdot \pi \cdot \zeta \cdot f_0} \tag{21}$$

during which the N modules of a single branch have to be inserted. To ensure that the leg current has sufficiently settled, the parameter β should be in the range of 5 to 10 %.

The time period $T_{on,bA}$ in which N modules of branch A are inserted can be expressed as a function of the duty cycle

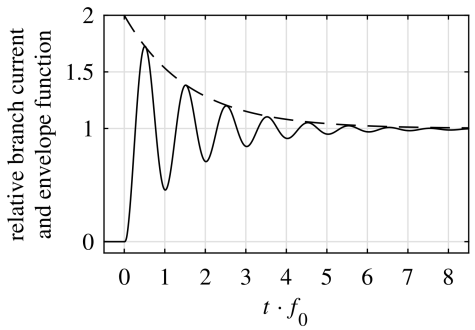

FIGURE 9. Solid line: envelope function according to (20), dashed line: simulated waveform of relative branch current $i_b/\hat{i}_o$. Damping ratio $\zeta = 0.1$, relative rise time $\epsilon = 0$.

δ and PWM frequency f_{PWM} [see Fig. 3]:

$$T_{on,bA} \approx \frac{1-\delta}{2} \cdot \frac{1}{f_{PWM}}. \tag{22}$$

Substituting $T_{on,min}$ from (21) for $T_{on,bA}$ in (22), the maximum achievable duty cycle

$$\delta_{max} = 1 - 2 \cdot \frac{\ln\left(\frac{1}{\beta}\right)}{2 \cdot \pi \cdot \epsilon \cdot \zeta} \cdot t_r \cdot f_{PWM} \tag{23}$$

can be expressed as a function of ratios ζ and ϵ, parameter β, the rise time t_r, and the PWM frequency f_{PWM}.

Substituting the expression for L_b from (19) into (23), it can be seen that the higher the branch inductance, the lower the maximum achievable duty cycle:

$$\delta_{max} = 1 - 4 \cdot \frac{L_b}{R_b} \cdot \ln\left(\frac{1}{\beta}\right) \cdot f_{PWM}. \tag{24}$$

B. IMPACT OF STRAY INDUCTANCES

Until now, the converter design process assumed the idealized model without any restrictions. In this section, a single design scenario, specified in Table 1, will be investigated to demonstrate further restrictions in the practical design.

The quasi-two-level-operated MMC is designed for a scenario with 4 kV dc link and a rated output current of 300 A. The modules are based on 1200 V IGBTs. Hence, the module capacitor voltage is rated at 800 V and there are 5 modules installed in each branch. The PWM frequency was selected to be 1 kHz and the required rise time is 4 μs that corresponds to the delay time $T_d = 1$ μs.

The safety parameter β was selected relatively high to 10 %, effectively increasing the maximum allowed duty cycle, and the maximum allowed branch current was defined as 150 % of the peak output current $\hat{i}_o$. The branch resistance was selected in a manner that the conduction losses of the converter ($\approx R_b \cdot \left(\frac{\hat{i}_o}{\sqrt{2}}\right)^2$, assuming that the output current flows through either of the branches at each point in time) are approximately 0.8 % of the nominal apparent power ($\approx \frac{1}{2} \cdot \frac{V_i}{2} \cdot \hat{i}_o$). The selected value for conduction losses is relatively high, considering a usual efficiency of MMCs of over 99 %.

TABLE 1. Design scenario specification.

Input voltage	V_i	4 kV
Rated output current amplitude	$\hat{i}_o$	300 A
Number of modules per branch	n_{mpb}	5
Module capacitor voltage	V_C	800 V
PWM frequency	f_{PWM}	1 kHz
Required rise time	t_r	4 µs
Maximum allowed branch current	$\hat{i}_b$	$1.5 \cdot \hat{i}_o$
Required-decay parameter	β	10 %
Estimated branch resistance	R_b	50 mΩ

TABLE 2. Design results.

Case		A	B	C
Branch inductance	L_b (µH)	0.16	1	2
Module capacitance	C_{mod} (µF)	69	250	502
Damping ratio	ζ	0.33	0.25	0.25
Relative rise time	ϵ	0.3	0.064	0.032
Energy storage constant	H (ms)	0.66	2.8	7.4
Maximum duty cycle	δ_{max}	0.97	0.81	0.74

A straightforward decision for the design is to choose the parameters ζ and ϵ according to the optimum design point from Fig. 7 for $\hat{i}_b/i_o = 1.5$. After that, the branch inductance L_b, the module capacitance C_{mod}, and the maximum achievable duty cycle δ_{max} can be determined according to (18), (19), and (23), respectively. This optimum design case is referred to as Case A in Table 2, which shows the design results.

From the table, it can be seen that the energy storage constant H is only 0.66 ms which is significantly lower than any of the conventionally operated or quasi-two-level-operated MMCs in the literature. The energy storage constant

$$H = \frac{6 \cdot n_{mpb} \cdot \frac{1}{2} \cdot C_{mod} \cdot V_C^2}{\frac{3}{2} \cdot \hat{i}_o \cdot 1.15 \cdot \delta_{max} \cdot \frac{V_i}{2}} \tag{25}$$

is defined according to [26] as a ratio between the total energy stored in module capacitors and the rated apparent power. For the calculation, a three-phase converter that applies carrier-based space-vector modulation (maximum modulation index increased by ≈ 1.15) is assumed.

While this optimum design point requires very little capacitance, it can be observed that the required branch inductance is extremely low as well. Considering that the typical stray inductance of a 1200 V 300 A IGBT module is $\approx$ 20 nH, it can be recognized that the inner inductance of five series-connected IGBT modules already covers for 100 nH in the branch inductance. Hence, it is not realistic to assume that the total branch inductance, comprising the stray inductances of the IGBTs, of the lines interconnecting the MMC modules, and of the lines connecting the MMC modules to the central dc-link capacitor, is possible within the range of a few hundred nanohenries. For reference, an inductance of 1 µH represents a loop with a diameter of 40 cm of 200 mm^2 wire.

Hence, more realistic values for the branch inductance are 1 µH or 2 µH that are referred to as cases B and C in Table 2, respectively.

Consequently, it can be observed that a minimum value of the branch inductance $L_{\mathrm{b,min}}$ is a restriction within the design process. The particular value for the design scenario is difficult to determine and it can be estimated by an FEM simulation of planned converter construction. When $L_{\mathrm{b,min}}$ is substituted into (19), the restriction for the ζ and ϵ product can be expressed:

$$\zeta \cdot \epsilon \leq \frac{1}{4 \cdot \pi} \cdot \frac{1}{L_{\mathrm{b,min}}} \cdot t_{\mathrm{r}} \cdot R_{\mathrm{b}}. \tag{26}$$

Equation (26) basically means that the feasible combinations of the ratios ζ and ϵ are further restricted to the area under a hyperbola $\epsilon \propto 1/\zeta$. Since the damping ratio ζ is restricted by the contours in Fig. 7 to some value above zero, the relative rise time ϵ has to be reduced to a very low value near zero, in order to limit the product $\zeta \cdot \epsilon$. This can also be observed in Table 2 for cases B and C, where it can be seen that the damping ratio is kept at its minimum value and the relative rise time ϵ is reduced significantly. However, as can be recognized from (18), increasing the damping ratio ζ and decreasing the relative rise time ϵ leads to increased module capacitance. This is further confirmed by the design results in Table 2 showing the growth of module capacitance with increasing branch inductances.

In summary, Table 2 demonstrates that when more realistic values of branch inductance are applied, the module capacitance C_{mod} increases and the maximum achievable duty cycle δ_{max} decreases. Consequently, the energy storage constant of the converter H is increased significantly to more typical values which can be found in the literature for the quasi-two-level-operated MMCs. These statements based on the single design scenario can be generalized (at least to some extent), since the stray inductances, parasitic resistances, and module capacitances are scaled correspondingly with increased voltages (increased number of modules) or increased currents.

It has to be noted that the module capacitance C_{mod} can be decreased and the maximum achievable duty cycle δ_{max} increases when the branch resistance R_{b} is increased [see (18) and (24)]. Hence, the passively damped quasi-two-level operation is likely to be advantageous for MMCs with low efficiency.

C. IMPACT OF NON-IDEAL SWITCHES

One of the main requirements of the passively damped quasi-two-level operation is that the sum of inserted modules in the upper and the lower branches has to be the constant number N [see (1)]. Although this condition is always met in the idealized model, in practical applications, the instantaneous sum of inserted modules can deviate due to turn-on and turn-off delays of the semiconductor switches (IGBTs). This means that the sum of branch voltages $v_{\mathrm{bA}} + v_{\mathrm{bB}}$ might be

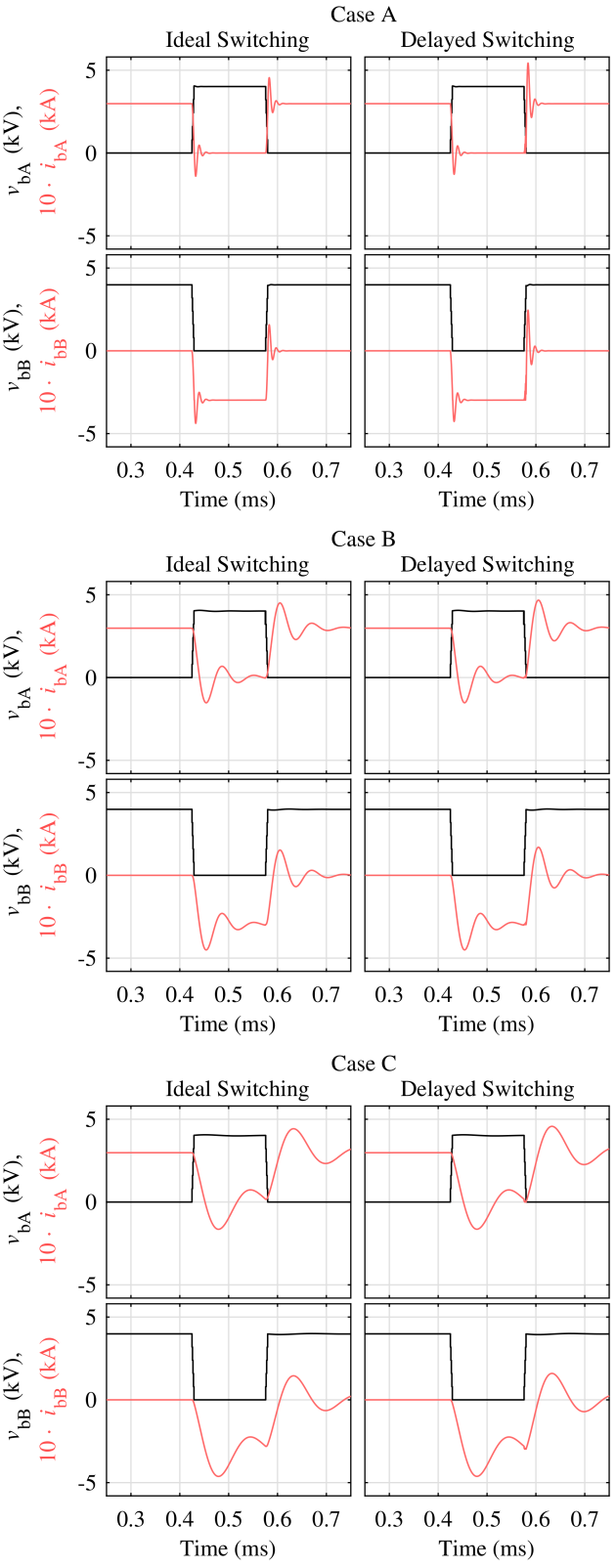

FIGURE 10. Branch current and branch voltage waveforms for the considered design cases A, B, and C: left) model with idealized switching without any delays; right) a turn-on delay of $t_{\mathrm{err}} = 50$ ns is applied to the IGBTs in Branch A. Output current $i_{\mathrm{o}} = 300$ A, duty cycle $\delta^* = 0.7$, IGBT deadtime $T_{\mathrm{DT}} = 800$ ns.

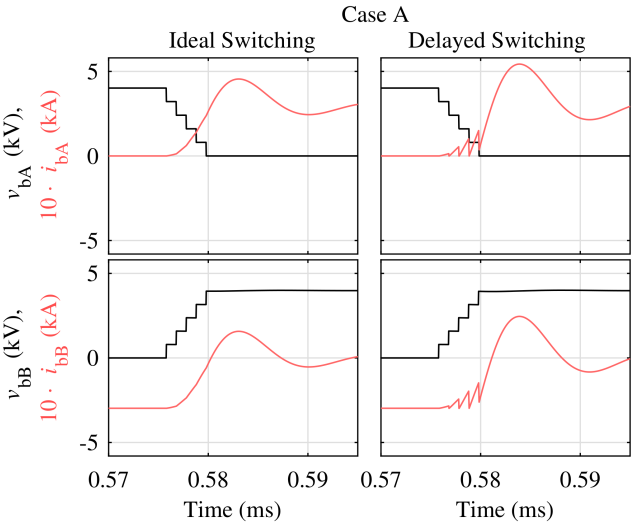

FIGURE 11. Detail view of Case A from Fig. 10.

lower or higher than the input voltage V_i by approximately a single capacitor voltage value V_C.

Using this assumption and neglecting the branch resistance, (8) can be applied to estimate the leg current error

$$|i_{\mathrm{leg,err}}| \approx \frac{V_C \cdot t_{\mathrm{err}}}{2 \cdot L_\mathrm{b}} \tag{27}$$

caused during the period t_{err} in which the total sum of inserted modules is not equal to N. This current error occurs in both branch currents [see (6)], and is directly proportional to the period t_{err} and indirectly proportional to the branch inductance L_b. Hence, the lower the branch inductance, the higher the expectable impact.

To demonstrate this effect, the cases A, B, and C from the previous section were simulated and plotted in Fig. 10. On the left hand side, the simulations are shown where the IGBTs are switched ideally. On the right-hand side, the IGBTs of branch A are turned-on with a delay of $t_{\mathrm{err}} = 50$ ns. Comparing the graphs, two conclusions can be drawn: First, the delayed turn-on of the IGBTs in one branch leads to increased branch currents, and second, the significance of the branch overcurrent declines with increasing branch inductance.

These occurrences can be explained using the zoomed-in view of Case A from Fig. 10 shown in Fig. 11. It can be observed that both branch currents start to rise shortly after the transition begins in both scenarios, with and without delayed turn-on of IGBTs. However, when the lower IGBT is turned on with a delay in branch A, the total sum of inserted modules becomes higher than N and the leg current decreases. Since the branch inductance L_b is very low in Case A, the leg current and thus both branch currents decrease very fast. It can be recognized in Fig. 11 that neither branch current exceeds $\pm i_\mathrm{o}$ directly due to this delay error. This can be explained by the IGBT switching deadtimes (also called interlocking times). During the deadtime, the modules are in a passive state and it is decided whether the module capacitor is inserted or not, depending on the branch current direction. In this case, once the branch current in the upper branch reaches zero due to voltage error caused by delayed IGBT switching, the lower diode in the module starts to conduct and the number of inserted module capacitors is reduced to N. While the peak branch currents are limited thanks to this current-limiting property during the passive states, it can be seen that the turn-on delay times in branch A cause the current in branch B to have lower negative values for a longer time period. Hence, more energy than expected is removed from the module capacitors of branch B which additionally excites the resonant circuit. The result is the increased positive swing of the branch current in branch B that propagates through the leg current to the current of branch A as well. As a consequence, the peak branch current in branch A is increased when the IGBT turn-on delays apply.

It is important to note that the IGBT deadtimes have practically no influence on the converter behavior during the idealized operation without switching delays, since one branch current is usually positive and the other one is usually negative during the transition. Consequently, even if a voltage error occurs in one branch (depending on the current direction), a voltage error in the opposite direction occurs in the other branch and the leg current is not affected. Moreover, if the leg current is too high for some reason (both branch currents are positive), an additional module capacitor is inserted during the deadtime and the leg current decreases rapidly [see (27)] until one of the branch currents hits zero. Accordingly, when the leg current is too low (both branch currents are negative), $N - 1$ of the module capacitors are inserted and the leg current is increased rapidly until one of the branch currents hits zero. In summary, the converter behavior during the deadtimes can be seen as self-stabilizing.

Finally, it should be mentioned as well that the resistance of the IGBT in the conducting state is nonlinear and depends on the current value. Since this resistance mainly determines the branch resistance in the practical applications, it is likely to impact the leg current resonant behavior. However, the exact behavior depends on the applied IGBT switches and is out of the scope of this paper.

To summarize this subsection, the turn-on and turn-off delays of the IGBTs can further excite the resonant circuit within the MMC, increasing the peak value of the branch current. The impact of these delays increases for longer error delay times and for lower branch inductances. These delays should be considered during the design process.

VI. EXPERIMENTAL VALIDATION OF THE MODEL AND INFLUENCE OF THE DC-LINK CAPACITOR

To validate the utilized MMC simulation model, two experiments have been conducted for different values of dc-link capacitances C_i. The validation is performed on a previously designed downscaled MMC prototype presented in [2], [3], [13]. Hence, the converter module capacitances could not be further optimized. The main change made to the converter is that the branch inductors are short-circuited in a manner that a new low-inductance path is available for the leg current. The resulting branch inductance and branch resistance were

TABLE 3. Parameters of experimental setup.

Input voltage	V_i	220 V
DC-link capacitance	C_i	$\{\infty, 760\ \mu\mathrm{H}, 280\ \mu\mathrm{H}\}$
Branch inductance	L_b	1.55 µH
Branch resistance	R_b	85 mΩ
No. of modules per branch	n_mpb	6
Module capacitance	C_mod	200 µF
PWM carrier frequency	f_PWM	1 kHz
Delay between switching instants	T_d	1 µs
Load inductance	L_o	15 mH
Load resistance	R_o	5.1 Ω
Output frequency	f_o	5 Hz
Modulation index	M	0.8
Resonance frequency	f_0	15.7 kHz
Damping ratio	ζ	0.279
Relative rise time	ϵ	0.078
Maximum duty cycle ($\beta = 10\ \%$)	δ_max	0.83
Converter energy storage constant	H	1.71 ms

measured including the module MOSFETs using an Omicron Bode 100 vector network analyzer. The measurement was made at 15 kHz frequency which is close to the resonance frequency of the passively damped operation mode. The converter parameters are listed in Table 3.

It can be seen that despite the relatively small dimensions of the low-voltage converter prototype, the minimized branch inductance is higher than 1.5 µH. This further confirms the discussion regarding the lowest achievable branch inductance in the design from the previous section. Nevertheless, the damping ratio is sufficient for a stable operation, since the branch resistances (converter losses) are generally higher in low-voltage converters compared to those for medium voltage.

In Fig. 12, the comparison of the results obtained from the simulation model to those of the MMC prototype captured by the oscilloscope are shown. The experimental results are captured for two values of dc-link capacitance $C_\mathrm{i} = 760$ µF and $C_\mathrm{i} = 280$ µF. In the figure, the waveforms of the dc-link voltage v_i, and the output current i_o, branch currents i_bA and i_bB, branch voltages v_bA and v_bB, and module capacitor voltages $v_{C,\mathrm{bA}}$ and $v_{C,\mathrm{bB}}$ of the first converter leg are plotted. The graphs below show the waveforms from above zoomed in.

Comparing the simulated waveforms to the experimental ones for the setup with larger dc-link capacitor ($C_\mathrm{i} = 760$ µF), it can be observed that branch voltages and the output current match very well. However, several differences in the capacitor voltages, dc-link voltage, and branch currents can be seen. These can be explained while observing the zoomed-in waveforms in Fig. 12. Here, it becomes apparent that the finite value of dc-link capacitance leads to a variation of the dc-link voltage. As described by (13), the module capacitor voltages follow the waveform of the dc-link voltage which can be clearly observed at the module capacitor voltage in branch B $v_{C,\mathrm{bB}}$ in the zoomed-in graph. Moreover, since the dc-link has a non-zero impedance, the high-frequency resonant leg currents caused in the other two converter legs are divided between the investigated phase leg and the dc-link capacitor. These additional transient swings are visible at branch currents of the zoomed-in experimental results for the larger dc-link capacitor in Fig. 12 near $\approx$ 50.2 ms and $\approx$ 50.8 ms. In the zoomed-out view, the strongest impact of these additional branch current components is observable near $\approx$ 20 ms, $\approx$ 80 ms, $\approx$ 120 ms, and $\approx$ 180 ms. This is because during these time periods, the switching occurs concurrently in all three phases and thus the branch current results as a superposition of all three resonant current components.

Comparing only the zoomed-in area of branch currents and module capacitor voltages in the proximity of 50.5 ms of the simulation (Fig. 12; below left) to those of the experimental setup with larger capacitance (Fig. 12; below middle), it can be stated that the resonant behavior of the converter leg is modeled sufficiently. Hence, the simulation models (and the analytic models) can be concluded valid.

Finally, Fig. 12 further demonstrates the impact of reduced dc-link capacitance. Comparing the waveforms captured with the large dc-link capacitance $C_\mathrm{i} = 760$ µF (Fig. 12; middle) to those captured with significantly lower dc-link capacitance $C_\mathrm{i} = 280$ µF (Fig. 12; right), it becomes evident that all undesired aforementioned effects become even stronger: The dc-link capacitor voltage v_i has a higher variation which consequently leads to a higher variation of module capacitor voltages. Because of the lower capacitance, a higher proportion of resonant leg currents is shared by the converter legs and moreover, the time-varying dc-link voltage further excites the resonant circuit within the MMC, leading to significantly higher branch currents.

As a consequence, it appears reasonable to apply relatively high dc-link capacitances with passively damped quasi-two-level-operated MMCs. However, this solution is not particularly cost-effective, since the energy storage constant of the dc-link capacitor

$$H_{C\mathrm{i}} = \frac{\frac{1}{2} \cdot C_\mathrm{i} \cdot V_\mathrm{i}^2}{\frac{3}{2} \cdot \hat{i}_\mathrm{o} \cdot 1.15 \cdot \delta_\mathrm{max} \cdot \frac{V_\mathrm{i}}{2}} \tag{28}$$

is already relatively high for the lower dc-link capacitance: $H_{C\mathrm{i}}(280\ \mu\mathrm{F}) = 2.39$ ms. This means that the energy stored in the dc-link capacitor is more than 40 % higher than that stored in module capacitors. Moreover, the energy storage constant of the larger dc-link capacitor that showed improved behavior is $H_{C\mathrm{i}}(760\ \mu\mathrm{F}) = 6.49$ ms which is almost four times higher than the energy stored in the modules. In summary, it is expected that the central dc-link capacitor is going to play a dominant role in the volume and costs of passively damped quasi-two-level-operated MMCs.

VII. COMPARISON TO QUASI-TWO-LEVEL PWM OPERATION WITH CONTROLLED LEG CURRENTS AND BRANCH ENERGIES

The quasi-two-level PWM operation described in [1]–[3], [12], [13] operates on different principles than the passively damped operation studied in this paper. The main idea is to actively control the leg currents by the branch voltages. By actively adjusting branch current values while the corresponding branch voltage is high, the state of charge of

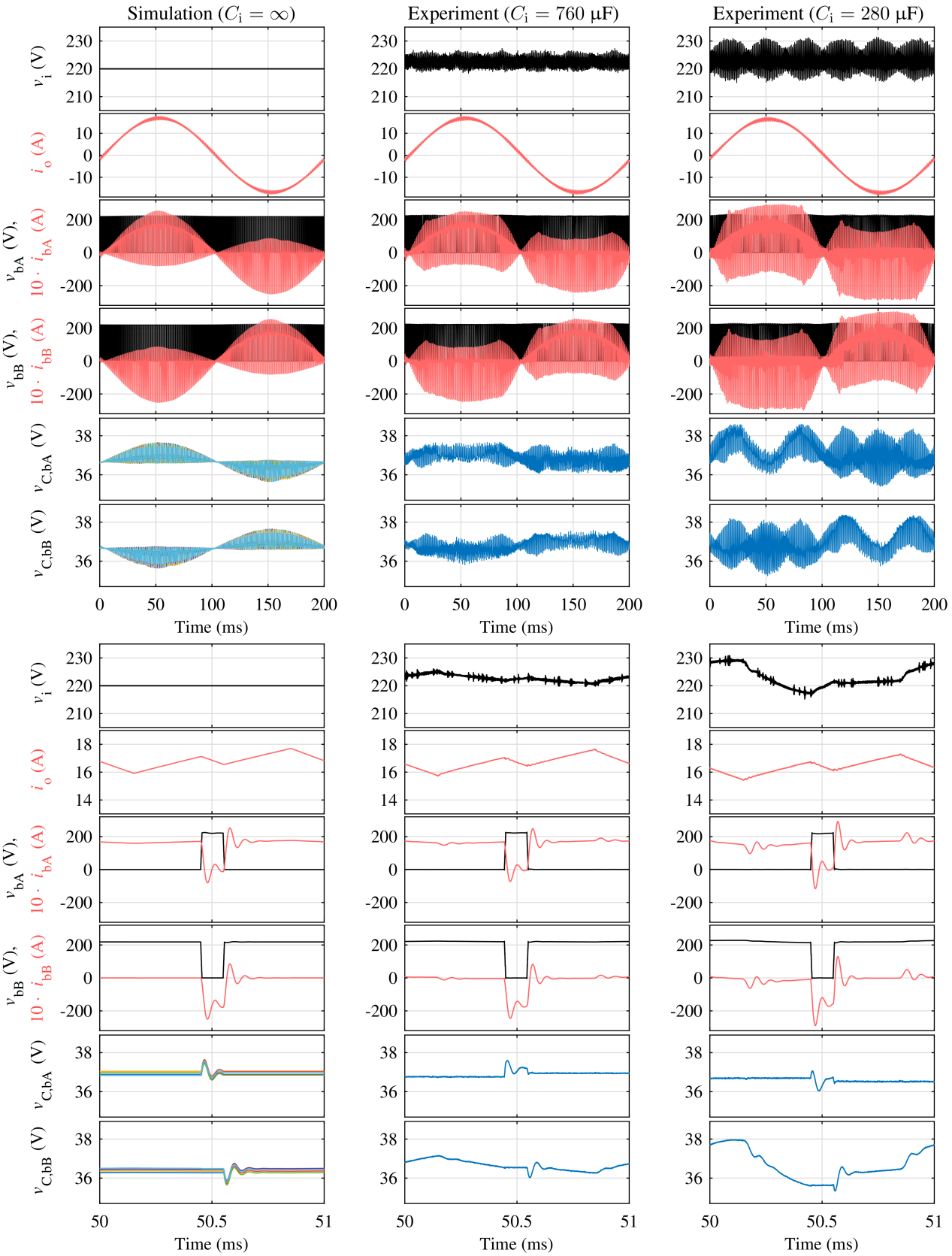

FIGURE 12. Comparison of simulated waveforms of three-phase MMC (left) to those captured by oscilloscope with an experimental setup (middle and right). The experiment was repeated for different values of dc-link capacitance: $C_i = 760\ \mu F$ (middle) and $C_i = 280\ \mu F$ (right). The measured data is filtered by a high-order 1 MHz low-pass filter. Only a single capacitor voltage per branch was measured during the experiments. The waveforms below show the detail view of the waveforms from above.

module capacitors can be actively controlled, allowing for the typically low branch energy variations.

The leg current is controlled either by overlap of the branch voltages when the current has to be changed quickly, or by an additional HF modulation superimposed to the branch voltage that is currently high. It is important to note that although this additional HF modulation increases the number of switching instants in the MMC, it does not have a significant impact on the switching losses, since the switching occurs only in the branch with low branch currents and the high frequency of HF modulation switching is divided between all modules of the branch.

In such operation, the branch inductance L_b is selected based on a trade-off between the HF modulation frequency, required to keep the branch current ripple limited, and the branch energy variation, to be buffered in the module capacitors, that is directly proportional to the branch inductance value [2], [3], [14]. As a result, the required branch inductance is generally significantly higher (e.g., $L_\mathrm{b} = 100$ µH in [13]) than that required for the passively damped operation ($L_\mathrm{b} = 1.5$ µH in this paper, for the same experimental setup). This introduces several advantages: The inductance is by more than an order of magnitude higher than the parasitic inductances and thus the physical construction of the converter can be designed more simply. Moreover, the generally higher branch inductances reduce the parasitic effects, such as those from the IGBT switching delays, described in Section V-C, to negligible levels. It is also expected that the higher inductance improves the transient behavior during a redundant module failure.

From a different perspective, the generally higher branch inductance value also means that the branch energy variation, which has to be buffered in module capacitors, is higher than with passively damped operation. Despite this being true, the operation mode with controlled leg currents is likely to lead to lower module capacitances. This can be explained as follows: In the operation mode that controls leg currents, the module capacitance is selected according to the branch energy variation and the maximum allowed module capacitor voltage variation, which is, in fact, a degree of freedom. However, the maximum module capacitor voltage variation cannot be selected arbitrarily in the passively damped operation, since the module capacitance is selected to provide sufficient damping, according to the achieved branch inductance and the branch resistance [see (16)]. As a consequence, the passively damped operation requires relatively high module capacitances if the converter losses are low, while the operation mode with controlled leg currents enables a stable operation with low module capacitances, even if the converter losses are zero, as demonstrated in [13].

Finally, it is important to mention that the aforementioned problems that occur during passively damped operation with low dc-link capacitances do not have any impact on the quasi-two-level PWM operation that controls the leg currents. As demonstrated in [13], the same experimental setup with the lower value of dc-link capacitance ($C_\mathrm{i} = 280$ µF) can be utilized for quasi-two-level PWM operation of MMC with controlled leg currents without any additional undesirable effects in the converter currents.

VIII. CONCLUSIONS

This paper has analyzed the properties of the passively damped quasi-two-level PWM operation mode using simulations and an experimental prototype. Based on the detailed analysis of the behavior, a novel optimized approach to design the MMC for this operation mode was proposed. Furthermore, the impact of the parasitic properties on the converter behavior was investigated, highlighting the challenges in the design.

While in theory, the studied passively damped quasi-two-level operation showed very advantageous properties, i.e., simple control scheme and a small size of the module capacitors and branch inductors, the more profound analysis discovered that the behavior strongly relies on the parasitic properties of the converter, such as the losses and the parasitic branch inductances. It has been demonstrated that especially when the converter losses are low, the required branch inductances are likely below the achievable parasitic values and thus the module capacitances have to be increased, in order to increase the damping of the converter currents.

A comparison to the quasi-two-level PWM operation with controlled leg currents was discussed which highlighted the overall design advantages of the controlled operation mode. These include the simpler practical realization of the converter and likely smaller capacitors in the modules and in the dc link. Moreover, it is expected that the converter behavior during a redundant module failure improves. The main advantages of the passively damped operation are the simpler control and the lower measurement requirements, which are, however, relatively mediocre considering that the control system is only a small part of the overall costs of a medium-voltage converter.

In summary, the dependency of the complex converter behavior on the parasitic parameters is an important challenge which has to be solved for the passively damped quasi-two-level operation mode to become an attractive alternative for medium-voltage drives.

APPENDIX

A. APPROXIMATION OF CONTOUR PLOT

$$\begin{aligned}\hat{i}_\mathrm{b}/i_\mathrm{o} = {} & 1.989 - 2.751\cdot\zeta - 0.8844\cdot\epsilon + 4.026\cdot\zeta^2 \\ & +2.129\cdot\zeta\cdot\epsilon + 3.621\cdot\epsilon^2 - 3.085\cdot\zeta^3 \\ & -1.885\cdot\zeta^2\cdot\epsilon - 2.135\cdot\zeta\cdot\epsilon^2 - 3.12\cdot\epsilon^3 \\ & +0.9491\cdot\zeta^4 + 0.696\cdot\zeta^3\cdot\epsilon + 0.302\cdot\zeta^2\cdot\epsilon^2 \\ & +1.112\cdot\zeta\cdot\epsilon^3 + 0.7635\cdot\epsilon^4 \end{aligned} \tag{29}$$

TABLE 4. Position of the optimum design points.

$\hat{i}_\mathrm{b}/i_\mathrm{o}$	1.2	1.3	1.4	1.5	1.6	1.7	1.8
ζ	1.00	0.75	0.50	0.33	0.21	0.15	0.11
ϵ	0.21	0.28	0.30	0.30	0.30	0.35	0.40

B. LIST OF OPTIMUM DESIGN POINTS

See Table 4.

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