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Effective passivation of crystalline silicon surfaces by ultrathin atomic-layer-deposited TiO_x layers

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Abstract

We characterize the surface passivation properties of ultrathin titanium oxide (TiO_x) films deposited by atomic layer deposition (ALD) on crystalline silicon by means of carrier lifetime measurements. We compare different silicon surface treatments prior to TiO_x deposition, such as native silicon oxide (SiO_y), chemically grown SiO_y and thermally grown SiO_y. The best passivation quality is achieved with a native SiO_y grown over 4 months and a TiO_x layer thickness of 5 nm, resulting in an effective lifetime of 1.2 ms on 1.3 Ωcm *p*-type float-zone silicon. The measured maximum lifetime corresponds to an implied open-circuit voltage (iV_{oc}) of 710 mV. For thinner TiO_x layers the passivation quality is reduced, however, samples passivated with only 2 nm of TiO_x still show a lifetime of 612 µs and an iV_{oc} of 694 mV. The contact resistivity of the TiO_x including the SiO_y interlayer between the silicon wafer and the TiO_x is below 0.8 Ωcm^2. The combination of excellent surface passivation and low contact resistivity has the potential for silicon solar cells with efficiencies exceeding 26%.

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Keywords: silicon solar cell; titanium oxide; atomic layer deposition; surface passivation; electron-selective contact

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1. Introduction

The photovoltaics industry constantly strives to further increase the conversion efficiency and minimize the production costs of silicon solar cells. So far, the main emphasis was put on reducing recombination losses in the non-metallized cell areas. Here, important progress has been achieved by implementing plasma-enhanced chemical vapor deposited (PECVD) silicon nitride (SiN_x) on the cell front emitter [1] and more recently stacks of aluminium oxide (Al_2O_3) and SiN_x on the cell rear [2]. The next logical step would now be the reduction of the carrier recombination at the metal contacts, which is becoming the dominant loss mechanism when the other loss channels have been largely eliminated.

In the past, ultrathin silicon oxide (SiO_2), aluminum oxide (Al_2O_3) [3-5], hydrogenated amorphous silicon (*a*-Si:H) [6] and poly-Si [7] have been successfully applied as passivated contact layers to silicon solar cells and more recently metal oxides [8-12] and polymers [13], the latter two material classes mostly usable as hole-selective contacts. More recently, an excellent surface passivation by titanium oxide (TiO_x) with a low contact resistivity was demonstrated by Yang et al. [14], who used ultrathin TiO_x layers as electron-selective passivation layers. The application as electron-selective contacts makes TiO_x potentially interesting for the next generation of highest-efficiency (>26%) solar cells. In this study, we examine the passivation properties of atomic-layer-deposited (ALD) TiO_x as a function of layer thickness and pre-treatment of the wafer surface. We also examine the contact resistivity of the TiO_x layers and give an estimation of the efficiency potential.

2. Experimental details

For our lifetime test samples we use (100)-oriented float-zone (FZ) *p*-type silicon wafers with a resistivity of 1.3 Ωcm and a wafer thickness of 300 µm. The samples are subdivided into five groups (i)-(v). All samples receive an RCA clean, however, for group (iv) the last HF dip in the RCA cleaning sequence is omitted in order to not remove the chemical oxide grown during RCA. After RCA, the samples of group (v) are heated to 500°C in an N_2 ambient in a quartz-tube furnace for 15 min, in order to form a thermal tunnel oxide of ~1.5 nm thickness. The other three groups (i)-(iii) are stored in ambient air after the HF dip for 2 days, 17 days and 4 months, respectively, in order to grow native oxides of 0.95 nm, 1.1 nm and 1.3 nm thickness, respectively. TiO_x is then symmetrically deposited on both wafer surfaces using thermal ALD in a FlexAl reactor (Oxford Instruments) at a set-temperature of 230°C. Tetrakis(dimethylamino)titanium (TDMAT), H_2O and N_2 were used as titanium precursor, oxidant and purge gas, respectively. The samples are then characterized using the photoconductance decay (PCD) method for lifetimes above 200 µs and the quasi-steady-state photoconductance (QSSPC) method for lifetimes below 200 µs (Sinton Instruments WCT-120 lifetime tester) [15] before and after annealing at 250°C on a hot-plate in ambient air. Effective lifetimes are reported at a fixed injection density of $\Delta n = 10^{15}$ cm^{-3} if not otherwise reported. Implied V_{oc} (iV_{oc}) values are extracted from the injection-dependent lifetime measurements at an injection density corresponding to 1 sun illumination intensity.

In order to extract the J_0 values, test samples are prepared using FZ *p*-type silicon wafers with a resistivity of 150 Ωcm and a wafer thickness of 300 µm. The front sides of these test structures are passivated with TiO_x, the rear side features an excellent passivation using an Al_2O_3/SiN_z stack.

In order to measure the contact resistivity, Czochralski-grown (Cz) *n*-type silicon wafers with a resistivity of 1.5 Ωcm and a wafer thickness of 300 µm are used. On the front side of the samples, TiO_x layers with thicknesses of 2 nm and 5 nm, respectively, are deposited. Ten aluminium (Al) dots of 1 µm thickness with different diameters, ranging from 1 mm to 8 mm, are electron-beam-evaporated on top through a shadow mask. On the rear side, an n^+ layer (80 Ω/sq.) is formed by phosphorus diffusion. On top of the n^+ layer, a 1 µm thick Al film is evaporated. Figure 1 shows a schematic of the test sample structure used to extract the contact resistivity.

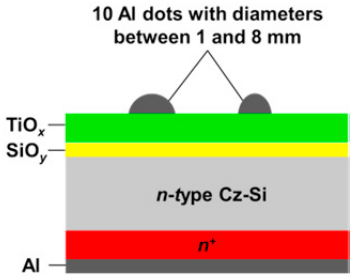

Fig. 1. Schematic of the test sample structure used to extract the contact resistivity.

For each single front contact the current-voltage characteristic in the dark is measured using a commercial *I-V* tester (LOANA System, pv-tools, Hamelin, Germany) at a temperature of 25°C. From the *I-V* measurement the contact resistivity is calculated using the method described by Cox and Strack, whereby the ρ_c values are obtained by fitting the curve of resistivity versus front contact diameter [16]. Two reference samples were included, where front and rear sides are phosphorus-diffused (80 Ω/sq.) and subsequently full-area metallized with a 1 µm thick Al layer. All samples are measured as-deposited, without any thermal activation treatment.

3. Results

3.1. Surface passivation

We examine the impact of different silicon surface treatments prior to the TiO_x deposition on the passivation quality. In Fig. 2 (a), the effective lifetime τ_{eff} for 5 nm thick TiO_x layers with different surface pre-treatments are shown. The native oxide grown in 2 days (resulting in a nominal oxide thickness of ~0.95 nm) results in a τ_{eff} value of only 80 µs. The native oxide grown within 17 days (~1.1 nm) leads to a significantly higher τ_{eff} value of 460 µs. The highest τ_{eff} value of 1.2 ms is measured for the sample stored for 4 months in ambient air (~1.3 nm SiO_y). Figure 2 (b) shows the measured injection dependence of τ_{eff} of the best sample, clearly demonstrating the excellent suitability of this passivation layer for solar cell applications, as the injection dependence is practically negligible in the relevant injection range below $\Delta n = 10^{15}$ cm^{-3}. As also shown in Fig. 2(a), the sample with chemically grown SiO_y interlayer results in a relatively poor τ_{eff} value of only 272 µs and the sample with thermally grown SiO_y results in a τ_{eff} value of only 225 µs. Consequently, a native SiO_y grown over a long period is in this experiment the best silicon surface treatment for achieving high passivation quality with a thin TiO_x layer. TiO_x layers deposited directly after the RCA clean show very low τ_{eff} values of only 40 µs, partly probably due to the low deposition temperature of 200°C. Therefore, a thin SiO_y interlayer seems to be an essential prerequisite for achieving an excellent passivation quality.

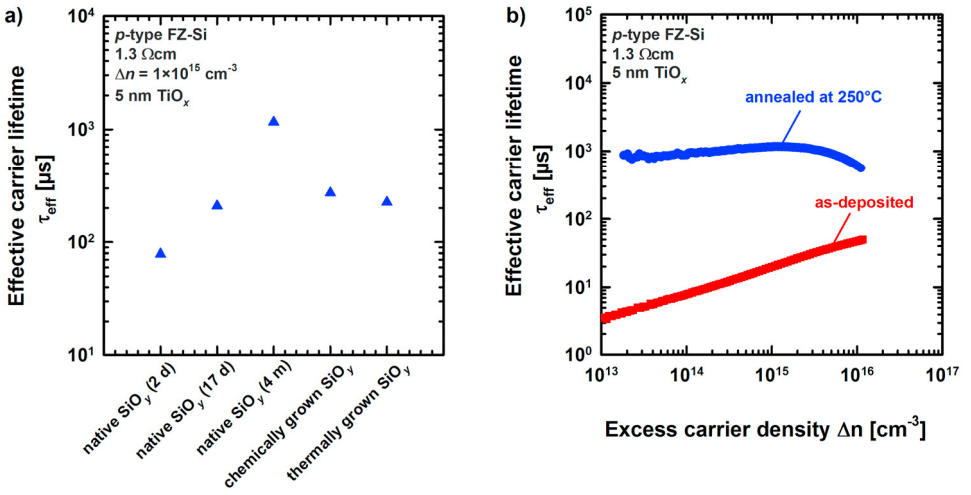

Fig. 2. (a) Effective carrier lifetime τ_{eff} for different silicon surface treatments prior to the TiO_x deposition. (b) Effective carrier lifetime τ_{eff} as a function of excess carrier density Δn for a 5 nm TiO_x layer for the best sample in the as-deposited state (red symbols) and the after annealing at 250°C (blue symbols).

In order to investigate the influence of the TiO_x thickness on the passivation quality, 1, 2, 4 and 5 nm thick TiO_x layers have been deposited by ALD on samples stored under ambient air for 4 months prior to the deposition. Figure 3 shows the measured implied open-circuit voltage iV_{oc} as a function of the TiO_x film thickness before and after annealing at 250°C. For TiO_x thicker or equal to 2 nm, a short anneal at 250°C is sufficient to significantly improve the surface passivation quality. Only for the 1 nm thick TiO_x layers, the best iV_{oc} value is achieved directly after deposition. For the 2 nm TiO_x layers a value of 654 mV is measured directly after TiO_x deposition, however, this value is improved after a 1.5-min-anneal at 250°C to 694 mV. The sample with 4 nm TiO_x reaches a τ_{eff} value of 1.1 ms after annealing for 3 mins, corresponding to an iV_{oc} value of 709 mV. The maximum iV_{oc} value of 710 mV is achieved for a 5 nm thick TiO_x layer. This sample shows also a high τ_{eff} value of 1.2 ms at an injection density of $\Delta n = 10^{15}$ cm^{-3}. Our experiments clearly demonstrate the high potential of ultrathin TiO_x layers for the surface passivation of high-efficiency *c*-Si solar cells.

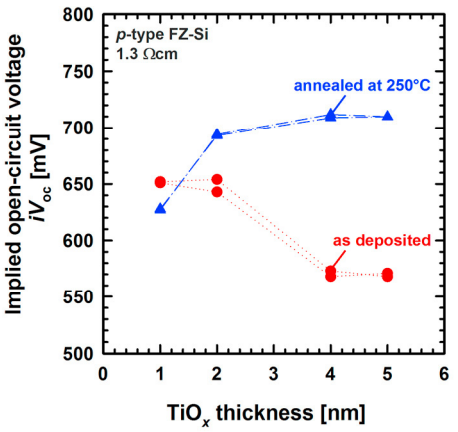

Fig. 3. Implied open-circuit voltage iV_{oc} as a function of TiO_x film thickness before and after annealing at 250°C.

3.2. Contact resistivity

Figure 4 shows the measured contact resistivities ρ_c of TiO_x and SiO_y/TiO_x stacks as a function of the TiO_x film thickness. All ρ_c values in the graph represent the average over two samples. The ρ_c values increase with an increasing TiO_x film thickness. The lowest ρ_c value of 0.23 Ωcm^2 is measured for a 2 nm thick TiO_x layer. The 5 nm thick TiO_x layer exhibits a significantly increased contact resistivity of 0.68 Ωcm^2. The implementation of a native SiO_y interlayer between the silicon wafer and the TiO_x layer increases the contact resistivity up to a value of around 0.74 Ωcm^2, a value almost independent of the TiO_x layer thickness.

Compared to the reference samples, all contacts with TiO_x show non-ohmic *I-V* behavior. Therefore, the measurement results are evaluated at a current density of 38 $mAcm^{-2}$, which corresponds approximately to the current density at the maximum power point of a solar cell.

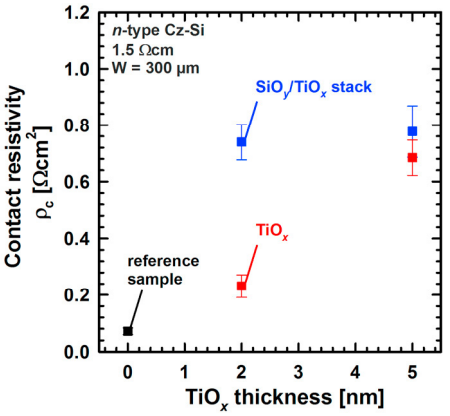

Fig. 4. Contact resistivity ρ_c extracted from Cox and Strack test structures as a function of TiO_x film thickness with and without a SiO_y interlayer. Also shown is a reference sample with a front and rear side n^+ layer.

Although the investigated TiO_x layers exhibit much higher contact resistivities on silicon wafers than a phosphorus-diffused n^+ emitter, they still exhibit a high potential of successful implementation as an electron-selective contact in high-efficiency *c*-Si solar cells. The electron-selective TiO_x layers investigated in this work would in fact allow for maximum efficiencies in excess of 26%, as will be shown in the following section.

3.3. Selectivity and efficiency potential

Knowing the contact resistivity ρ_c and the saturation current density J_0, we are now able to determine the selectivity S_{10} as defined by Brendel et al. [17] as a quantitative measure of the selectivity of the contact. The selectivity is calculated according to the equation

$$S_{10} = \log_{10}\left(\frac{V_{th}}{J_0 \rho_c}\right), \tag{1}$$

with V_{th} being the thermal voltage at 25°C and J_0 the saturation current density.

In addition, the maximum achievable efficiency η_{max} for a given selectivity S_{10} for a full-area contact (f_c=1) is given by [17]:

$$\frac{\eta_{\max}(S_{10})}{\%} = \left((2.457 S_{10} - 4.240)^{-19.52} - (29.21)^{-19.52} \right)^{-\frac{1}{19.52}}. \quad (2)$$

Table 1 shows the measured parameters, the selectivities and maximum efficiencies for the TiO_x layers from this work in comparison to TiO_x layers from Yang et al. [18] and a phosphorus-diffused n^+ emitter from Brendel et al. [17].

Table 1. Selectivity S_{10} and the maximal achievable efficiency η_{max}, extracted from the contact resistivity ρ_c and saturation current density J_0 using equations (1) and (2). For TiO_x–based contacts investigated by Yang et al. [18] we translate the given recombination velocity values S_{eff} into the corresponding saturation current densities J_0.

Electron-selective material		ρ_c [Ωcm^2]	J_0 [$fAcm^{-2}$]	S_{10} [-]	η_{max} [%]
2 nm TiO_x	(this work)	0.74	40	11.9	25.0
5 nm TiO_x	(this work)	0.78	9	12.6	26.4
2.5 nm TiO_x	(Yang et al. [18])	0.025	13	13.9	28.5
4.5 nm TiO_x	(Yang et al. [18])	0.070	13	13.5	27.9
n^+ emitter passivated with SiN_z	(Brendel et al. [17])	0.26	109	12	25.0

Our experiment shows that a thin SiO_y layer is crucial for the surface passivation of silicon by a TiO_x layer. The best results are achieved by using a 5 nm thick TiO_x with an interlayer of native SiO_y grown over 4 month, with a saturation current density of 9 $fAcm^{-2}$ and a contact resistivity of 0.78 Ωcm^2. This results in a selectivity of 12.6 allowing for a maximal achievable η of 26.4%. The limit of this selective contact is the high contact resistivity compared to results obtained by Yang et al. [18]. A contact resistivity of 0.23 Ωcm^2 was achieved by omitting the SiO_y interlayer and using only a 2 nm thick TiO_x layer. These layers, however, exhibit reduced passivation quality, therefore, further investigations are needed to focus on the interface between the silicon and the TiO_x layer. Another possibility to further improve the selectivity is to apply a different metal to lower the resistivity of the TiO_x/metal interface.

4. Conclusions

We have shown that TiO_x–based selective contacts are compatible with open-circuit voltages of 710 mV for 5 nm thick TiO_x layers. The contact resistivities of the 2 and 5 nm thick TiO_x layers are 0.74 Ωcm^2 and 0.78 Ωcm^2, respectively, and can be reduced to 0.23 Ωcm^2 by omitting the SiO_y interlayer, which is, however, required to achieve the optimum surface passivation quality. Based on the measured contact resistivities ρ_c and the saturation current densities J_0 of our TiO_x layers, we have calculated the selectivities S_{10} as a quantitative measure of the electron transport of TiO_x–based contacts, which allowed us to conclude that efficiencies in excess of 26% are in principle achievable by implementing ALD-TiO_x-layers (with SiO_y interlayer) as electron-selective contacts into dopant-free silicon solar cells.

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