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# High-quality exfoliated crystalline silicon foils for solar cell applications

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**Abstract**

Kerfless wafering techniques offer a significant cost saving potential via the reduction of silicon consumption. In this paper, we examine thin single crystalline Si foils that were fabricated by a novel kerfless thermo-mechanical exfoliation method utilizing evaporated Al with regard to their suitability for solar cell applications. The foils are 50-80 µm thick and smooth to visual inspection across the almost entire surface. We measure the effective minority carrier lifetimes of the foils and the remaining parent substrates by quasi-steady-state photoconductance (QSSPC) and spatially resolved by dynamically calibrated steady state infrared carrier lifetime mapping (dynILM). We find lifetimes of above 120 µs for kerfless exfoliated 0.5 Ωcm p-type float-zone (FZ) Si layers. With an additional etching step after exfoliation, we obtain effective lifetimes of above 200 µs. The measurements reveal that there is no critical lifetime degradation due to exfoliation-induced surface features and thus the exfoliated layers are well-suited for high-quality solar cells.

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*Keywords:* wafering; kerf-free; layer transfer;  photovoltaic;, spalling; exfoliation; carrier lifetime

## 1. Introduction

Today, silicon wafers for solar cells are commonly produced by wire-sawing. There, for each 180 µm thick Si wafer about 130 µm silicon thickness are lost due to kerf loss during production [1]. The high share of kerf loss in Si consumption is a strong motivation for the development of kerfless wafering techniques in order to save material

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costs. So far, several approaches for kerfless wafering have been developed. Many of them base on the implementation of a weaker separation layer that can act as a determined breaking point during the lift-off of an upper layer of high quality crystalline silicon. The release layer can be generated below the surface of a high-quality silicon wafer, for instance by implantation of hydrogen ions in the SmartCut [2] and PolyMax [3] processes or by electrochemically etching in the macroporous silicon (MacPSi) process [4]. In other approaches the release layer is produced on top of the silicon substrate, followed by an epitaxially grown high-quality crystalline silicon layer on top, which can be detached afterwards. Examples include porous silicon [5] and $CaF_2$ [6] acting as release layers.

While a release layer is helpful to control the exfoliation process, it can be challenging to implement it without a significant increase of process complexity and costs. Thus, kerfless wafering in absence of a release layer represents an attractive option. The lift-off of a thin crystalline Si film without the need of a mechanically or chemically weak release layer was first described by Tanielian in 1985 [7] and recently revisited [8–10]. Here, an adhesive stressor layer on top of a thicker Si substrate is used to induce the exfoliation of a thin substrate from a thicker wafer. Stressor layer materials include screen-printed metal paste [10], electrochemically deposited metal layers [9], and sputter-deposited metal layers [8]. Additional stress can be induced by thermal expansion of the stressor layer [10] or external force to an attached handling layer [8].

In order to reduce the wafering costs it is preferable not to remove the stressor layer after lift-off but to use it as a functional layer. This is a strong argument for the use of metallic stressor layers, as a metallic layer can act as a rear contact electrode in a solar cell. In this case the rear side of the solar cell is processed before applying the stressor / rear contact layer. After lift-off, the solar cell front-side can be processed. Recently, a solar cell from a 25 µm thick Si foil that showed an efficiency of 14.9 % on a 1.1 cm² area was realized this way [11]. The Si foil was produced using a 50 µm thick, electrochemically deposited Ni stressor layer. In Addition to the difficulties that hamper the production of such layers within reasonable effort and time, the material costs of the expensive Ni alone would strain a typical solar cell production budget [1]. An alternative is the use of Al for the stressor / rear contact layer. Al can be applied on an industrial scale and at an economic price level [12]. Furthermore, Al is already well established as a solar cell material. Mechanical stress can be generated by thermal cycling owing to different coefficients of thermal expansion (CTE) in the Si wafer and the Al layer. The Al layer acts twofold beneficial as rear contact electrode and as mechanical support layer.

Within this paper, we present thin single crystalline Si foils that were exfoliated following this scheme. The foils are dubbed MEMO-foils, where MEMO stands for MEtal-supported Monocrystalline Si thin films. We study the carrier recombination properties of the Si foils by dynILM [13] and by QSSPC [14] in order to verify the suitableness of these layers for solar cell applications.

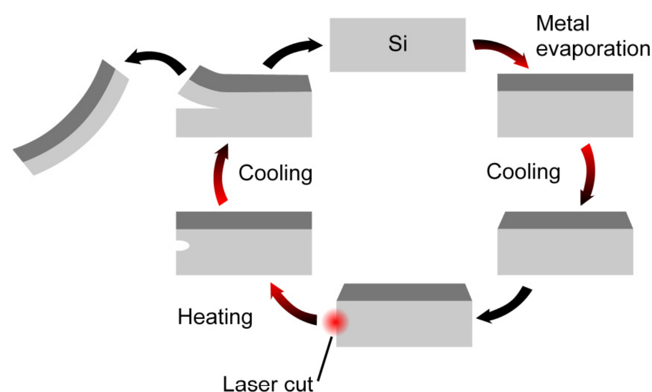


Fig. 1. Scheme of metal-assisted exfoliation reuse cycle: A metal layer is applied on top of a thick parent substrate. After metallization the sample is cooled down to room temperature and a laser is used to create a notch as exfoliation starting point. The Si foil is exfoliated by stress induced during thermal cycling.

## 2. Si-foil exfoliation by directed cooling

### *2.1. Exfoliation cycle*

The basic principle of the exfoliation process is displayed in Fig. 1. A thick, monocrystalline 0.5 Ωcm p-type FZ Si wafer is used as a parent substrate. A stress-inducing Al layer is evaporated on top. The CTEs of the materials are temperature-dependent, while the CTE of Al is about ten times the value of that of Si [15,16]. The sample is warmed during evaporation due to heat of condensation. Thus, the evaporated layer is already stressed when cooled down to room temperature. This might not lead to spontaneous exfoliation but can lead to a visible substrate bow that depends on the ratio of metal to Si thickness [17]. In order to control the exfoliation process, we use a laser to create a lateral notch at the sample edge. The notch acts as a starting point for stress-induced cracking and thus gives control over the exfoliation depth. Then the sample is exposed to thermal cycling. During heating up, the metal layer expands wider than the Si, leading to compressive stress in the metal. If the metal is ductile, it will start to flow upon a certain temperature / stress level to reduce internal stresses. In the case of Al, this point is already reached after a temperature difference of ~70 K [17]. When the sample is subsequently cooled down, the metal layer contracts tighter than the Si due to its higher CTE and tensile stress is generated in the metal layer and also in a substrate area below the metal near the substrate edges. At a certain stress level in the substrate spalling sets in, preferably at the laser-defined notch at the sample edge. The evolving crack propagates parallel to the substrate surface from the edge to the center and a thin substrate layer is released. The cracking depth depends on the dimensions and mechanical properties of both the substrate and the metal layer and can be adjusted by the choice of the metal layer thickness [18].

### *2.2. Exfoliation by directed cooling*

In order to control the exfoliation process we use directed cooling [19] to induce the thermal stress. A scheme of our setup is displayed in Fig. 2. The substrate is mounted to a linear axle above a water basin and heated up by a halogen lamp. Then the heated substrate is slowly dipped into the water. The submerged parts of the sample are rapidly cooled down due to enhanced convective cooling under water, leading to thermal stress and exfoliation. The upper part of the sample above the water surface is still heated by the halogen lamp, preventing spontaneous exfoliation from the sample top and sides, so that the cracking direction can be controlled.

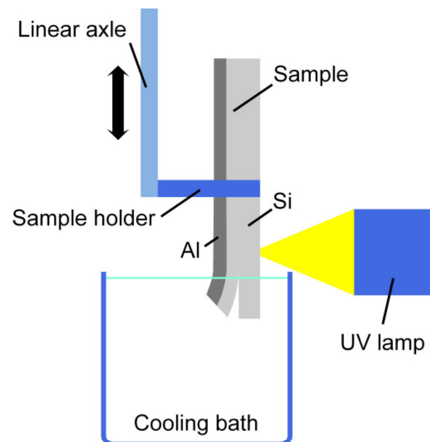


Fig. 2. Scheme of experimental setup for exfoliation by directed cooling (not to scale). The substrate is vertically mounted and heated up by a halogen lamp that is placed above a water basin. Then a linear axle is used to dip the substrate into the water. The submerged parts of the sample are rapidly cooled down, leading to thermal stress and exfoliation. Meanwhile, the part above the water surface is still heated by the halogen lamp, preventing spontaneous exfoliation. Thus, the cracking direction can be controlled.

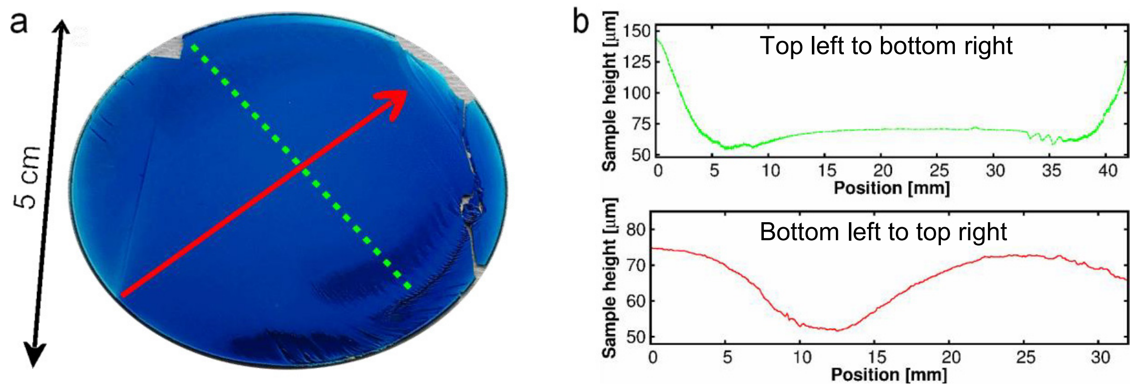


Fig. 3. (a) photograph of an exfoliated Si Layer with a diameter of 2 inch and (b) profilometer height profiles measured along the marked lines.

### *2.3. Sample preparation for lifetime analysis*

We use 700 µm thick Si wafers (p-type FZ, 0.5 Ωcm) as parent substrates. The substrates are passivated by an $Al_2O_3/SiN_x$ dielectric layer stack to avoid any influence of the metal deposition to the lifetime properties. Secondly, such dielectric layer could be utilized as a rear side passivation in a future cell process. Afterwards a 120 µm thick Al layer is evaporated to one wafer surface in an Applied Materials ATON 600 inline evaporation tool [12]. We cut the samples to 2″-wafer size. A laser carves a notch for crack initiation into the sample edge. Directed cooling is used to separate MEMO-Al-Si-bilayers with 50-80 µm thin Si foils from the substrate. During exfoliation, the substrate temperature does not exceed 250 °C and stays well below the brittle-ductile transition temperature of Si at 729 °C, where the number of defects in the spalled Si layer is expected to increase rapidly if it is exceeded during cracking [15]. The resulting bilayers are curved but mechanically stable, as the Al layer gives support to the brittle Si layer.

In order to further investigate the electronic properties of the Si-foils, we remove the Al layer from the layers after lift-off in a $H_3PO_4$-based etching bath. We clean the samples and passivate them with a new $Al_2O_3/SiN_x$ stack for subsequent lifetime measurements.

## 3. Results

### *3.1. Foil surface appearance*

Fig. 3 (a) shows a photograph of an exfoliated Si layer after Al removal and renewed surface passivation. The sample appears smooth in visual inspection over almost the entire cracked Si surface. There are some visible irregularities near the sample edge. The sample is prone to breakage when handled with tweezers, and this causes the smaller cracks at the sample edge. A similar phenomenon was also seen by Bedell et al. employing their controlled spalling process [20]. Profilometric measurements performed with a Dektak 150 surface profiler shown in Fig. 3 (b) reveal a locally increased layer thickness in the near-edge area.

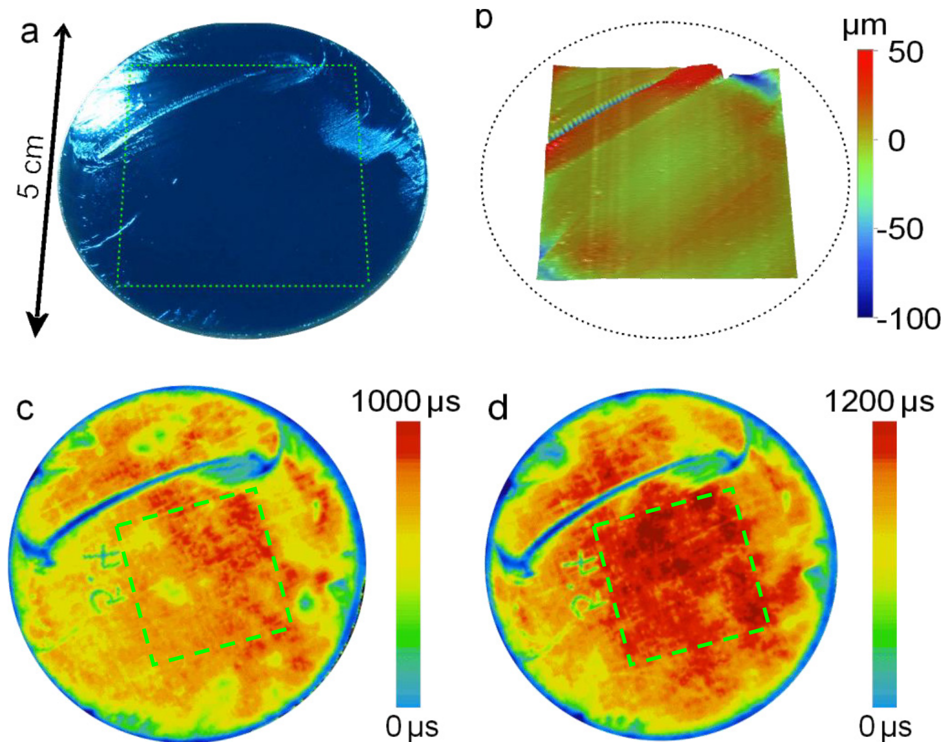


Fig. 4. (a) photograph of the cleaved side of a 2″-diameter Si wafer substrate after layer exfoliation; (b) profilometer mapping of that sample; (c) ILM lifetime mapping after lift-off and passivation The effective lifetime averaged over the 2×2 cm² area indicated by the dotted lines is 808 µs at an estimated carrier concentration $\Delta n = 8 \cdot 10^{14}$ cm$^{-3}$; (d) ILM-Mapping after an additional KOH-etching step and renewed passivation. The effective lifetime averaged over the 2×2 cm² area indicated by the dotted lines is 1105 µs at an estimated carrier concentration $\Delta n = 1.1 \cdot 10^{15}$ cm$^{-3}$.

These areas with uneven surface structures act as the preferential breaking points during sample handling. Thus, we use square pieces with 2.5 cm side length cut out from such layers to study the recombination properties of the Si foils. The inverted structures on the substrate counterpart also exhibit a very smooth center and some irregularities at the sample edges. The remaining substrate is much thicker than the exfoliated layer and thus easier to handle. Therefore we are not limited in sample size in this case and can use the whole 2″-samples for further characterization. The exfoliation process can be tuned to reduce or avoid cleavage surface irregularities in the first place, which was however not within the scope of this work.

### *3.2. Substrate surface appearance*

We clean and passivate the cleaved side of a parent substrate after exfoliation to study the damage that was induced in the substrate during the spalling process by investigating the surface morphology and the substrate recombination properties. In Fig. 4 (a) a photograph of a substrate after exfoliation is displayed together with (b) the corresponding profilometer height mapping. The largest surface portion of the substrate is plane with maximum height variations of less than 10 µm. The surface is rougher in areas near the sample edge. In the upper part of the picture, a trench is visible. Here, the exfoliation process of this particular sample was interrupted and additional mechanical force had to be applied to completely release the Al-Si-bilayer. The bottom of the ridge lies more than 50 µm deeper that the typical substrate level. This height difference is critical for the exfoliation of a second layer, as the ridge amplitude exceeds the typical thickness of an exfoliated Si layer. Therefore, exfoliation parameters that allow for a continuous whole area lift-off have to be chosen for reuse of the substrates in order to avoid trenches.

### 3.3. Substrate recombination properties

Fig. 4 (c) shows a dynILM effective carrier lifetime mapping after exfoliation and passivation. The lifetime mappings are already corrected for heat and emissivity effects [13]. The deep trench is clearly visible as a carrier lifetime sink. Also visible is the sample labeling, which was applied to the substrate rear with a diamond scriber. Besides this, the effective carrier lifetime varies over the sample. The lifetime is reduced in the rougher areas near the sample edge. However, also in the smoother surface areas the carrier lifetime is varying more than expected from a typical wafer of the material. It is known that in exfoliated Si layers lattice defects can occur within a few µm below the surface [21]. It is likely that similar defects can be induced on the substrate side. Therefore we etch the substrate in KOH for 3 minutes in order to remove 4 µm of the Si from the surface. The lifetime image of the etched sample in Fig. 4 (d) reveals a wider, more uniform area of large carrier lifetimes in the sample center compared to the lifetime image of the same sample prior to the etching step. Still, the carrier lifetime is lowered towards the edge of the sample. The trench in the upper part of the sample still appears as an area of enhanced carrier recombination.

We use the 2×2 cm² area of the substrate that is indicated in Fig. 4 c) and d) to determine the effective carrier lifetimes prior and subsequent to the additional etching step from the dynILM images. The measured carrier lifetime increased from 808 µs at an estimated carrier concentration of $\Delta n = 8 \cdot 10^{14}$ cm$^{-3}$ after lift-off to 1105 µs at $\Delta n = 1.1 \cdot 10^{15}$ cm$^{-3}$ after etching. The intrinsic lifetime limit of the used material at room temperature taking into account radiative and Auger recombination is 967 µs [22,23]. Thus, the estimated effective lifetimes prove that our spalling process allows for the exfoliation of layers without degrading the substrate's electronic quality.

### 3.4. Si foil recombination properties

We also study the recombination properties of a 6.25 cm² Si foil, which was cut out from the exfoliated counterpart of the substrate investigated in section 3.2. A photograph of the cleaved side of the layer is shown in Fig. 5 (a). The foil is smooth to the eye without any visible irregularities and the camera lens is reflected by the surface. In Fig. 5 (b) a dynILM measurement of the layer after lift-off and Al removal is displayed. The carrier lifetime is not homogenously distributed. We etch the sample for 3 minutes in a KOH-solution to remove the upper 4 µm Si of the surface. The lifetime distribution after the etching step is displayed in Fig. 5 (c). The carrier lifetime is significantly improved over the most part of the sample. The upper right corner broke during handling. The regions with a lower carrier lifetime around the corner in the upper left and the breach on the left are attributed to tweezers-induced passivation failures.

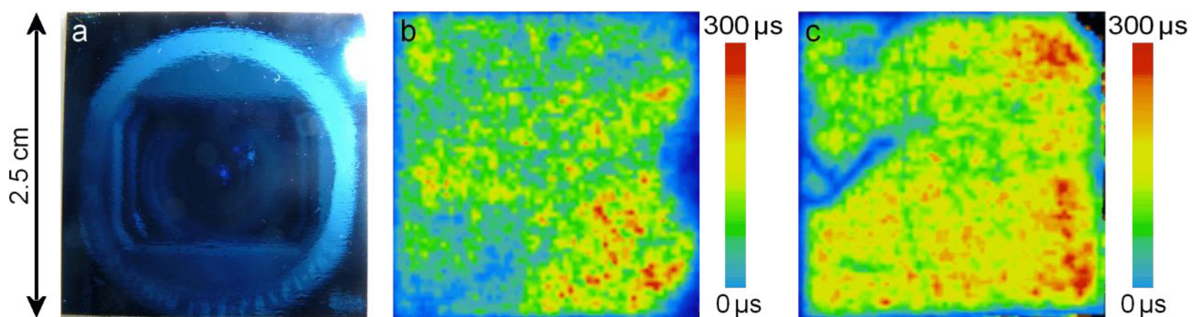


Fig. 5. (a) photograph of the cleaved side of a 6.25 cm² exfoliated Si layer; (b) DynILM lifetime mapping of the layer in (a) after lift-off and passivation. The effective lifetime averaged over the whole sample is 117 µs at an estimated carrier concentration of $\Delta n = 9 \cdot 10^{14}$ cm$^{-3}$; (c) DynILM-Mapping of the same layer after an additional KOH-etching step and renewed passivation. The effective lifetime averaged over the whole sample is 159 µs at an estimated carrier concentration of $\Delta n = 1.1 \cdot 10^{15}$ cm$^{-3}$ and 182 µs at an estimated carrier concentration of $\Delta n = 1.5 \cdot 10^{15}$ cm$^{-3}$ if the upper left quarter of the sample is excluded from averaging.

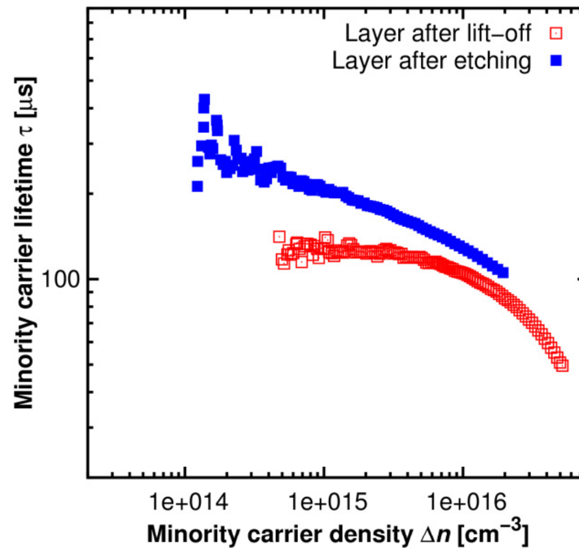


Fig. 6. QSSPC-measurements of exfoliated 6.25 $cm^2$ Si-foil prior to and after KOH etching step. The lifetimes at $\Delta n = 10^{15}$ $cm^{-3}$ are 127 µs and 207 µs.

Fig. 6 shows QSSPC-measurements prior and subsequent to the etching step. The carrier lifetime at $\Delta n = 10^{15}$ $cm^{-3}$ increases from 127 µs to 207 µs due to the etching step. Using both-side-passivated reference samples to determine the surface recombination velocity of 6-7 cm/s we obtain an estimated bulk carrier lifetime in the exfoliated layer of 164 µs before and 380 µs after the etching step. An explanation for this effect is the removal of near-surface recombination centers [21] during etching. With the estimated carrier lifetimes and an assumed QSSPC uncertainty of 10% [24] the effective minority carrier diffusion lengths are at least 510 µm before and 660 µm after etching, which equals 10 times the foil's thickness in the latter case. From the QSSPC measurement, we obtain an implied open circuit voltage value of $V_{oc}$ = 722 mV. Thus, the layer is well-suited for the use as a high-efficiency solar cell absorber.

## 4. Discussion and summary

We presented lifetime measurements on an exfoliated, 50-70 µm thick Si foil and the respective parent substrate after exfoliation. The novelty value of the used exfoliation method lies in the use of evaporated Al as the stressor layer, which is easily applicable at a large scale, allows for exfoliation at comparably low temperatures, gives mechanical support to the Si foil, and can be used as a functional layer in a final solar cell layer device. The investigated Si foil exhibits a carrier lifetime that is high enough for carrier diffusion lengths of seven times the foil thickness directly after lift-off. After an additional etching step in KOH, carrier lifetimes are further increased and a diffusion length of ten times the foil thickness is reached. On the substrate side, the estimated bulk carrier lifetime after exfoliation reaches the intrinsic limit of the used material. Thus, our spalling process allows for the exfoliation of layers suitable for high-efficient solar cells without degrading the substrate's electronic quality. A major issue that has to be addressed for further development of the exfoliation scheme is the determination of a parameter window that allows for a well-defined and continuous exfoliation process. Irregularities in the substrate surface, which can occur when exfoliation is interrupted, might act as a geometrical hurdle for substrate reuse as well as an area of enhanced carrier recombination. First experiments indicate that the directed cooling approach is capable of solving this challenge [19]. With the combined advantages of the evaporated Al stressor layer and the superb electronic quality, the presented MEMO-layers are a promising material system for future thin-film c-Si solar cells.

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## References

[1] Goodrich A, Hacke P, Wang Q, Sopori B, Margolis R, James TL, et al. A wafer-based monocrystalline silicon photovoltaics road map: Utilizing known technology improvement opportunities for further reductions in manufacturing costs. Sol Mat 2013;114:110–35.
[2] Bruel M. Silicon on insulator material technology. Electron Lett 1995;31:1201.
[3] Henley F, Kang S, Liu Z, Tian L, Wang J, Chow Y. Beam-induced wafering technology for kerf-free thin PV manufacturing. In: Proc 34th IEEE Photovoltaic Specialists Conference; 2009. p. 1718–23.
[4] Brendel R, Ernst M. Macroporous Si as an absorber for thin-film solar cells. phys stat sol (RRL) 2010;4:40–42.
[5] Brendel R. A novel process for ultrathin monocrystalline silicon solar cells on glass. In: Proc 14th European Photovoltaic Solar Energy Conference; 1997.
[6] Hayes GJ, Clemens BM. Rapid liftoff of epitaxial thin films. J Mater Res 2013;28:2564–69.
[7] Tanielian M, Blackstone S, Lajos R. A New Technique of Forming Thin Free Standing Single-Crystal Films. J Electrochem Soc 1985;132:508–09.
[8] Bedell SW, Fogel K, Lauro P, Shahrjerdi D, Ott JA, Sadana D. Layer transfer by controlled spalling. J Phys D: Appl. Phys. 2013;46:152002.
[9] Rao RA, Mathew L, Saha S, Smith S, Sarkar D, Garcia R, et al. A novel low cost 25 µm thin exfoliated monocrystalline Si solar cell technology. In: Proc 37th IEEE Photovoltaic Specialists Conference; 2011. p. 3–6.
[10] Dross F, Robbelein J, Vandevelde B, van Kerschaver E, Gordon I, Beaucarne G, et al. Stress-induced large-area lift-off of crystalline Si films. Appl Phys A 2007;89:149–52.
[11] Saha S, Hilali MM, Onyegam EU, Sarkar D, Jawarani D, Rao RA, et al. Single heterojunction solar cells on exfoliated flexible ~25 µm thick mono-crystalline silicon substrates. Appl Phys Lett 2013;102:163904.
[12] Heinemeyer F, Mader C, Münster D, Dullweber T, Harder NP, Brendel R. In-line high-rate thermal evaporation of aluminium as a novel industrial solar cell metallization scheme. In: Hoornsta J, Schubert G, Beaucarne G, editors. Proc 2nd Workshop on Metallization for Crystalline Silicon Solar Cells: Status, trends and new directions; 2010. p. 48–51.
[13] Ramspeck K, Bothe K, Schmidt J, Brendel R. Combined dynamic and steady-state infrared camera based carrier lifetime imaging of silicon wafers. J Appl Phys 2009;106:114506.
[14] Sinton RA. Quasi-steady-state photoconductance, a new method for solar cell material and device characterization. In: Proc 25th IEEE Photovoltaic Specialists Conference; 1996. p. 457–60.
[15] Masolin A, Bouchard P, Martini R, Bernacki M. Thermo-mechanical and fracture properties in single-crystal silicon. J Mater Sci 2013;48:979–88.
[16] Hatch JE. Aluminum: properties and physical metallurgy. Materials Park, OH: ASM International; 1984.
[17] Mader C, Eitner U, Kajari-Schröder S, Brendel R. Bow of Silicon Wafers After In-Line High-Rate Evaporation of Aluminum. IEEE J Photovoltaics 2013;3:212–16.
[18] Suo Z, Hutchinson JW. Steady-state cracking in brittle substrates beneath adherent films. Int J Sol Struct 1989;25:1337–53.
[19] Hensen J, Niepelt R, Kajari-Schroeder S, et al. Lift-off of Memo-Foils by directed cooling. Accepted for presentation at 40th IEEE Photovoltaic Specialists Conference; 2014.
[20] Bedell SW, Fogel K, Lauro P, Sadana DK, Shahrjerdi D, Sousa Cortes NE. Edge-exclusion spalling method for improving substrate reusability; US Patent 2013/0005116 A1 2013.
[21] Masolin A, Simoen E, Kepa J, Stesmans A. Defects in Si foils fabricated by spalling at low temperature: electrical activity and atomic nature. J Phys D: Appl Phys 2013;46:155501.
[22] Schlangenotto H, Maeder H, Gerlach W. Temperature dependence of the radiative recombination coefficient in silicon. Phys Stat Sol (a) 1974;21:357–67.
[23] Richter A, Glunz SW, Werner F, Schmidt J, Cuevas A. Improved quantitative description of Auger recombination in crystalline silicon. Phys Rev B 2012;86.
[24] McIntosh KR, Sinton RA. Uncertainty in photoconductance lifetime measurements that use an inductive-coil detector. In: Proc 23rd European Photovoltaic Specialists Conference; 2008. p. 77–82.