A Resonant One-Step 325 V to 3.3–10 V DC–DC Converter With Integrated Power Stage Benefiting From High-Voltage Loss-Reduction Techniques

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***Abstract*— This work presents a self-timed resonant high-voltage (HV) dc–dc converter in HV CMOS silicon-on-insulator (SOI) with a one-step conversion from 100–325 V input down to a 3.3–10 V output, optimized for applications below 500 mW, such as IoT, smart home, and e-mobility. Unlike bulky power modules, the HV converter is fully integrated, including an on-chip power stage, with only one external inductor (10 μH) and capacitor (470 nF). It reaches a high power density of 752 mW/cm^3, an overall peak efficiency as high as 81%, and a light-load efficiency of 73.2% at 5 V and 50 mW output. HV loss-reduction techniques are presented and experimentally confirmed to offer an efficiency improvement of more than 32%. Integrated HV insulated gate bipolar transistors (IGBTs) are discussed and implemented as an attractive alternative to conventional integrated HV power switches, resulting in ∼20% smaller area at lower losses.**

***Index Terms*— DC–dc converter, high power density, high voltage (HV), HV loss reduction, lateral insulated gate bipolar transistor (IGBT), light-load efficient, silicon-on-insulator (SOI).**

I. Introduction

THE trend toward higher functionality and decentralization leads to a growing demand for efficient IC-level power conversion from high voltage (HV) of more than 200 V down to below 5 V. Applications include IoT and smart home, supplied from the grid and control circuits and other peripheries in e-cars and industrial applications with dc-link supply voltages in the range of 400 V.

Fig. 1 provides a general overview of power-supply solutions for low-power applications. Energy harvesting is widely applicable, but is limited to power levels below 1 mW [Fig. 1 (left)] and, thus, it is not suitable for many applications. The grid and HV batteries provide much higher power, readily available in buildings, and so on. However, conventional voltage conversion is achieved by expensive and relatively large power modules [Fig. 1 (right)] [1]–[5], which show poor efficiency below 500 mW along with low power density. Hence, they are not well suitable to supply microcontrollers, sensors, and so on.

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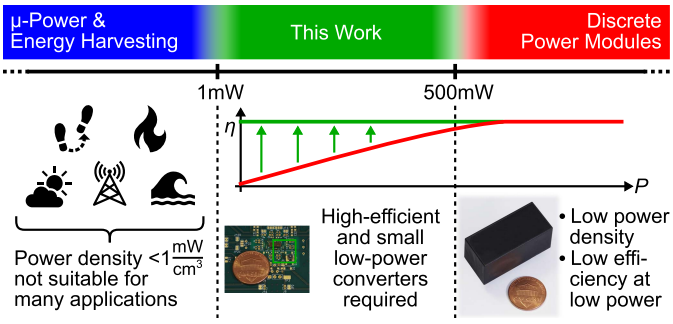

Fig. 1. Closing the power supply gap for IoT, e-mobility, and industry.

To increase the efficiency and to reduce the size at high input voltages and low output power, approaches, including multi-level converters [6]–[9], fly-buck converters [9], [10], and soft-switching converters [11]–[14], have been published, but their complexity is high and they still show a low light-load efficiency. In addition, although these converters allow for higher input voltages, their capability of handling input voltages of up to 400 V efficiently at a compact size is limited.

To close the existing power supply gap between energy harvesting and power modules, a detailed understanding of the topology and technology-dependent limitations is required, as outlined in Section II. It describes the influence of high input voltages on the efficiency, size, and other design and layout-specific parameters of conventionally used fly-back converters, fly-buck converters, multi-level converters, and soft-switching derivatives. Considering these limitations, an efficient and compact one-step HV topology for output powers below 500 mW is developed in Section III.

Due to the large influence of parasitic capacitances at high voltages on power losses, technology-specific layout and design rules are discussed in Section IV, leading to an efficiency improvement of more than 32%. Moreover, HV lateral super-junction MOSFETs (SJ-MOSFETs) and HV lateral super-junction insulated gate bipolar transistors (IGBTs) (SJ-LIGBTs) are compared. Area efficient and loss-optimized control circuits are described in Section V. Experimental results of the implemented converter are presented in Section VI. The presented converter closes the existing power supply gap [Fig. 1 (center)] between energy harvesting and power modules.

II. System-Level Challenges

Power modules typically utilize a flyback topology [Fig. 2 (left)] with large external components, such as power

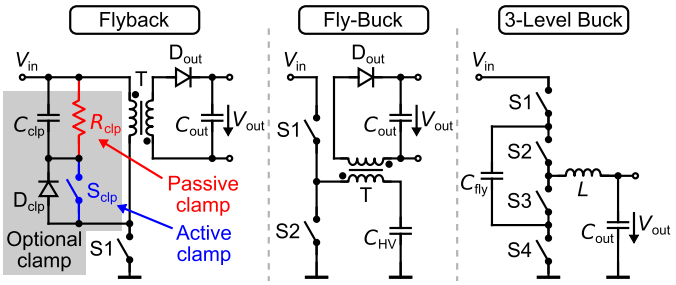

Fig. 2. Active-clamp and passive-clamp flyback, fly-buck, and three-level buck.

switches (S1 and S_{clp}), HV capacitors (C_{clp}), and a transformer T with up to several millihenries of inductance [1]–[5]. The same applies to fly-buck converters [Fig. 2 (center)] [9], [10]. Fast switching multi-level-buck converters, as in [6] [Fig. 2 (right)], reduce the inductance size, but the required flying-capacitor value (C_{fly}) is still large and difficult to integrate at higher voltages. In addition, their light-load efficiency is low and they require complex control circuits. This section discusses the root cause for the limitations of these converter types for the low-power target applications at conversion ratios around 100 and input voltages up to $V_{in} = 325$ V and beyond.

To realize conversion ratios as high as 100, duty cycles as low as 1% are required. In dynamic situations (load transients and so on), the duty cycle can be even lower, leading to a significant increase in control complexity. The smaller the required on-time, the higher is the sensitivity of the output voltage to jitter and delays of the pulsewidth-modulated (PWM) control signal. Timing optimized control circuits (comparators, saw-tooth generators, and so on) are required for precise duty-cycle control. Level shifters and other circuits need to be capable of transferring the PWM signal even at the rising and falling edge of the HV transients to ensure faultless switching [15]. Strong drivers are essential to achieve the small on-times at all, which further increases the losses and reduces the efficiency.

Multi-level converters for low power [6]–[9] and for higher power [16]–[18] relax the timing by scaling the input voltage. However, the higher the scaling ratio, the larger the number of flying capacitors [e.g., a three-level buck already requires one capacitor C_{fly}, see Fig. 2 (right)] and the number of required transistors [e.g., a three-level buck requires four switches S1–S4, see Fig. 2 (right)]. This increases the overall circuit complexity and the size significantly, making multi-level converters not well suitable for the target voltage range.

Fly-buck converters [9], [10], [19] realize a much higher input-voltage scaling with a lower amount of components, due to the flexible dimension of the transformer's turns ratio n, but they still need a large external HV capacitor C_{HV} at the primary side [see Fig. 2 (center)] and a large transformer T.

Flyback converters also achieve a high input-voltage scaling via the transformer's turns ratio, but do not need large HV capacitors and only one HV switch S1 [see Fig. 2 (left)]. However, the required voltage rating of S1 ($V_{in} + n \cdot V_{out} + V_{overshoot}$) scales with the turns ratio and the leakage inductance L_{leak} of the transformer T ($V_{overshoot} \propto L_{leak}$). Thus, the maximum possible turns ratio depends on the voltage rating of the used technology. Alternatively, an external power transistor has to be used. This limits either the maximum input voltage or the level of integration. $V_{overshoot}$ can be reduced with passive or active voltage clamps [13], [14], [20]–[24], which increases the converter complexity [Fig. 2 (left)].

The higher the voltage across the transistor, the higher is the switching losses and the lower the efficiency. But switching losses also scale with the transistor current. Especially at low output power, the inductor current ripple mainly impacts the switching losses. To reduce these losses, large inductance values in the range of several millihenries are typically used at $V_{in} = 325$ V [1]–[5]. The increase in the inductance value with the input voltage and the inverse of the inductor-current ripple can be compensated by scaling the switching frequency as well. However, higher switching frequencies lead to higher switching losses and to even smaller on-times. Soft-switching concepts, such as active-clamp flyback (ACF) [Fig. 2 (left)] [13], [14], [20]–[24], or operating in discontinuous conduction mode, as suggested in [21], reduce the losses at turn on, but increase the complexity of the power stage and the control, and the losses at the turn off remain high for most approaches. Furthermore, soft switching in ACF converters requires a minimum negative inductor current, which reduces the light-load efficiency.

It can be concluded that input voltages up to $V_{in} = 325$ V demand a topology with the lowest possible voltage stress of the components and innovative soft-switching implementations to reduce switching losses. To achieve a high level of integration, the amount of external components has to be reduced to its minimum. Light-load conditions down to a few milliwatt demand an efficient control approach and low-power subcircuits. Section III introduces a topology that meets these requirements.

III. High-Voltage Architecture

This section presents a resonant inverting step-down topology (Fig. 3) [25], optimized for high input voltages and light-load conditions. It uses a self-timed resonant circuit with zero-current switching (ZCS) and zero-voltage switching (ZVS) and enables a fully integrated power stage with two HV transistors (HV1 and HV2, rated to $V_{in} + V_{out}$), three HV diodes ($D1_{HV}$, $D2_{HV}$, and $D3_{HV}$, rated to $V_{in} + V_{out}$), and two low-voltage transistors (LV1 and LV2, rated to V_{out}). Only one small inductor (L_{res}) is required due to the self-timed resonance operation realized with one on-chip HV capacitor C_{res}.

The topology is based on the flyback topology. The stand-alone operation of most target applications without an electric connection to the environment, such as RF transmitter, sensors, or LED strings, does not need an isolated output and can be referenced to either a negative or a positive converter output voltage. Therefore, to reduce the voltage stress across the switches and to achieve a smaller footprint, the transformer of the flyback topology is replaced by an inductor (L_{res}). The inductor can later be changed back to a transformer if galvanic isolation or a positive output voltage is required.

Precise duty cycles around 1% and a reduction of the switching losses is achieved by adding C_{res} in series to L_{res}. The resulting resonant circuit (L_{res} and C_{res}) causes

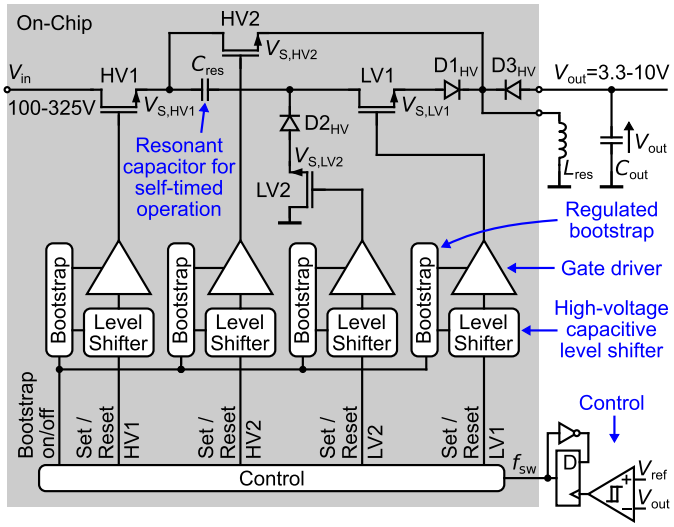

Fig. 3. One-step resonant HV converter topology.

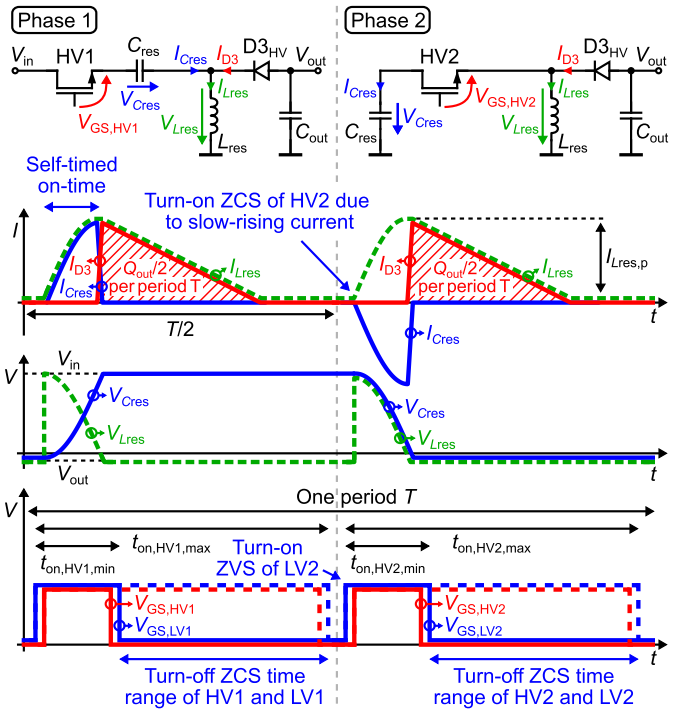

Fig. 4. Operating principle of the implemented resonant HV converter incorporating two phases with ZCS/ZVS and self-timed on-time.

a self-timed resonant switching behavior with ZCS and ZVS, which simplifies the control complexity, increases the light-load efficiency, and enables a high level of integration. The additional diodes ($D1_{HV}$ and $D2_{HV}$) and switches (HV2, LV1, and LV2) are used for a further increase of the converter efficiency, as explained in the following.

The converter operates in two phases, as shown in Fig. 4. Table I summarizes the switching states and the soft-switching behavior of the power transistors in both phases. At the beginning of each phase, all power switches are turned off. HV2 and LV2 remain off during phase 1. Phase 1 is initialized by turning LV1 on, before HV1 is turned on to obtain ZVS of LV1, resulting in the equivalent circuit shown on the left-hand

TABLE I

SWITCHING STATES AND SOFT SWITCHING OF THE POWER TRANSISTORS DURING THE TWO PHASES OF OPERATION

	Phase 1		Phase 2	
	on	off	on	off
LV1	ZVS	ZCS	X	X
HV1	ZCS	ZCS	X	X
LV2	X	X	ZVS	ZCS
HV2	X	X	ZCS	ZCS

X = remains off

side of Fig. 4. After HV1 is turned on with ZCS, the voltage across the inductor (V_{Lres}) rises initially up to the input voltage V_{in}, causing the inductor current I_{Lres} to rise sinusoidally (due to the resonant behavior). As a result, the voltage across the capacitor (V_{Cres}, initially equals to V_{out}) increases. During this time, $D2_{HV}$ avoids a current through LV2 to the ground. When V_{Cres} reaches ($V_{in} - V_{out}$), V_{Lres} has dropped down to the output voltage V_{out}. The inductor current I_{Lres} then commutates to $D3_{HV}$ and to the output capacitor C_{out} and transfers the energy stored in L_{res} to C_{out}. During this freewheeling period, LV2 is required to avoid I_{Lres} to commutate to $D1_{HV}$ and $D2_{HV}$. HV1 and LV1 turn off with ZCS sometime after the commutation of I_{Lres} to C_{out} and before the beginning of phase 2. This large turn-off window and the time-relaxed turn-on sequence between LV1 and HV1 simplify the control of the switches compared with other topologies. To avoid complex zero-current-detection circuits for HV1 and LV1, the transistors can be turned off right before the next phase is initialized, as realized with the implemented control described in Section V-D.

The resulting equivalent circuit in phase 2 is shown on the right-hand side of Fig. 4. HV1 and LV1 remain off in this phase and LV2 is turned on before HV2 is activated, to achieve ZVS of LV2. During this phase, the energy stored in C_{res} transfers to L_{res} and, after the commutation of the inductor current to $D3_{HV}$, to C_{out}, similar to phase 1. As an advantage of this topology, the energy stored in C_{res} is conserved and contributes to the output as well, which increases the efficiency by up to a factor of two.

The capacitor C_{res} causes a self-timed on-time and automatically determines the energy transferred to the output. The transferred energy (proportional to Q_{out}, Fig. 4) is constant for each phase and depends only on the value of C_{res} and V_{in}. Thus, the output power scales with the switching frequency (f_{sw}) as approximated by (1) and so do the switching losses. Whereas the maximum power corresponds to high switching frequencies, the converter maintains high efficiency down to light loads as f_{sw} reaches low values. The resulting low switching frequencies further relax the requirements on the control circuit

$$P_{out} = C_{res} \cdot V_{in}^2 \cdot f_{sw}. \quad (1)$$

Fig. 5 shows this linear relation between f_{sw} and the output power P_{out} for the implemented 325 V converter and the implemented 230 V converters (see Section VI). As the

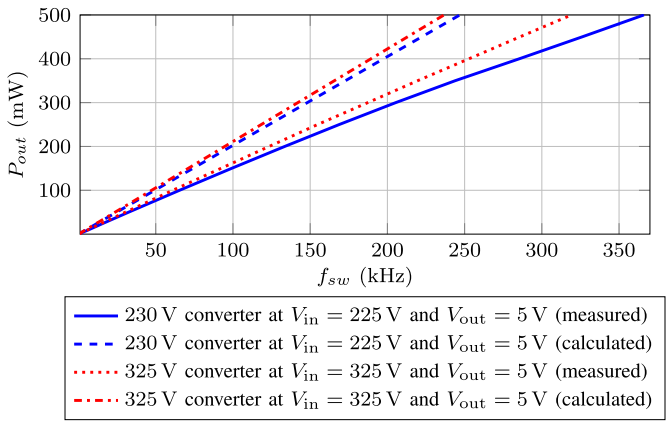

Fig. 5. Measured and calculated output power P_{out} versus switching frequency f_{sw}.

approximation in (1) neglects losses in the converter, the measured curves in Fig. 5 have lower slopes.

Defining $R_{load} = V_{out}^2/P_{out}$, the load-dependent voltage-conversion ratio can be derived from (1)

$$\frac{V_{out}}{V_{in}} = \sqrt{C_{res} \cdot R_{load} \cdot f_{sw}}. \tag{2}$$

Equation (2) indicates that the voltage-conversion ratio does not depend on the on-time of HV1, HV2, LV1, or LV2, which relaxes the turn-off timing of the transistors and reduces the control complexity. The self-timed on-time of the converter can be estimated by (3). It only depends on the resonant frequency f_{res}, defined by L_{res} and C_{res}, which allows for precise and small duty cycles

$$t_{on} = \frac{1}{4 \cdot f_{res}} = \frac{\pi}{2} \cdot \sqrt{L_{res} \cdot C_{res}}. \tag{3}$$

A simplified expression for the duty cycle can be derived from the two-phase timing of Fig. 4

$$D = 2 \cdot t_{on} \cdot f_{sw} = \pi \cdot \sqrt{L_{res} \cdot C_{res}} \cdot f_{sw}. \tag{4}$$

During converter operation, the conversion ratio and the duty cycle is solely controlled by f_{sw}. The maximum switching frequency and, thus, the maximum output power of the converter results from the ZCS condition at the turn-on of HV1 and HV2 (see Fig. 4). I_{Lres} needs to be zero before the next phase can be started. Due to the small duty cycles at conversion ratios around 100, the interval with $I_{Lres} > 0$ is dominated by the freewheeling period of I_{Lres} to C_{out}. Thus, the maximum switching frequency f_{max} can be estimated by (5) with the minimum value of $I_{Lres,p}$. $I_{Lres,p} = I_{Lres,p,min}$ follows from (6) for $V_{in} = V_{in,min}$:

$$f_{max} = \frac{(V_{out} + V_{D3HV,on})}{2 \cdot I_{Lres,p,min} \cdot L_{res}} = \frac{(V_{out} + V_{D3HV,on})}{2 \cdot \sqrt{L_{res} \cdot C_{res}} \cdot V_{in,min}}. \tag{5}$$

C_{res} also defines the energy transferred to L_{res} in each phase and, thus, the required inductance depends on the maximum allowed peak current $I_{Lres,p}$ according to (6) with $V_{in} = V_{in,max}$

$$I_{Lres,p} = \sqrt{\frac{2 \cdot E_{Cres}}{L_{res}}} = \sqrt{\frac{C_{res}}{L_{res}}} \cdot V_{in}. \tag{6}$$

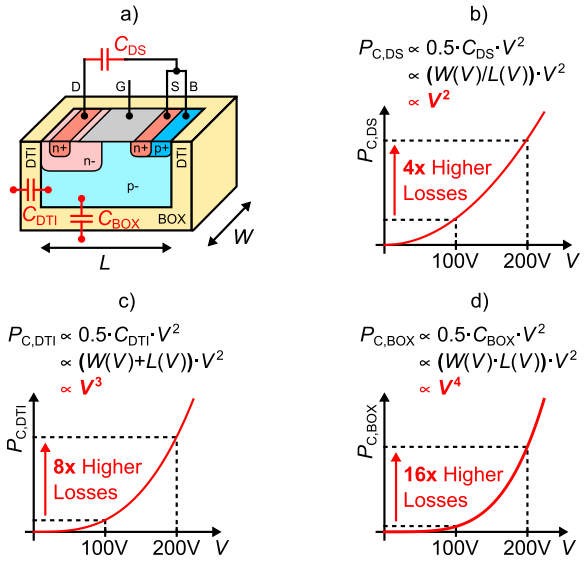

Fig. 6. (a) SOI cross-section and significant efficiency impact due to capacitive-loss scaling at high voltages using (b) drain-source capacitance, (c) deep-trench capacitance, and (d) BOX capacitance as example (for constant R_{on}).

The smaller C_{res}, the smaller L_{res} would be. With $L_{res} = 10\ \mu$H, the 230 V implementations use a C_{res} of 40 pF and the 325 V implementation a C_{res} of 20 pF.

Due to the low conducting time, the on-resistance of the HV devices HV1, HV2, $D1_{HV}$, and $D2_{HV}$ can be relatively large, on the order of 10 Ω, resulting in low area consumption.

IV. Circuit Design in SOI

HV circuit design benefits from silicon-on-insulator (SOI) technologies. Fig. 6(a) shows a generic HV SOI MOSFET with buried oxide (BOX) below the transistor and deep trench isolation (DTI) surrounding it. The narrow trench isolation leads to a reduction of the chip size compared to HV technologies with large junction isolation for HV devices. Parasitics, like bipolar effects and leakage currents, are negligible in SOI, which eases the design and improves reliability and efficiency. The topology derived in Section III has been implemented in a 0.18 μm HV CMOS partial-SOI technology [26]. It utilizes a reverse-biased junction depleting the handle wafer under the HV devices to achieve both high break-down voltages and small devices at the same time [27].

A. Parasitic Capacitances

Losses caused by parasitic capacitances, such as those at the drain–source and toward substrate are a challenge in fast-switching HV converters for low-power applications. Fig. 6 shows how the losses increase significantly with the voltage V, which corresponds to the break-down voltage $V_{ds,max}$ of the switches and, thus, to V_{in}. The loss scaling in Fig. 6 assumes a constant on-resistance R_{on}. Therefore, $R_{on} \propto (1/^{W}/_{L}) =$ constant and $L \propto V_{ds,max}$ results in $W \propto V_{ds,max}$.

The drain–source capacitance C_{ds} [Fig. 6(b)] represents a junction capacitance, where W is proportional to the capacitance area and L is proportional to the distance across the

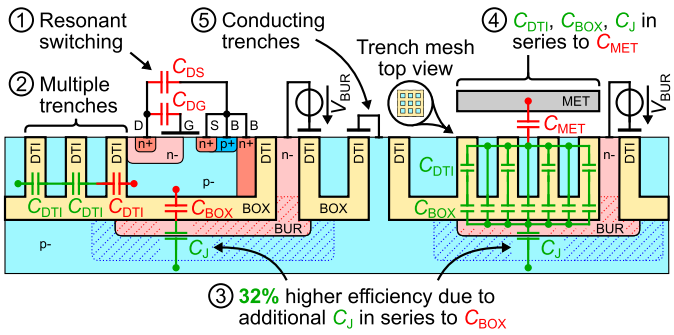

Fig. 7. Capacitive-loss-reduction techniques in SOI.

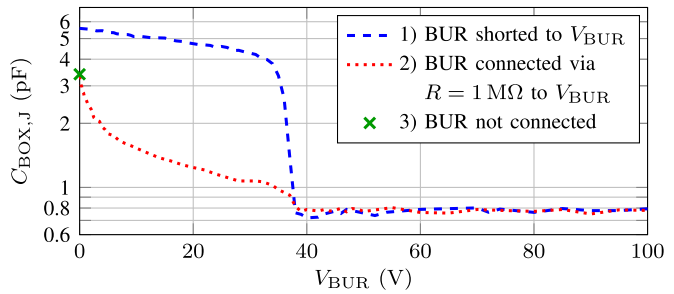

Fig. 8. Measured influence of V_{BUR} on the junction capacitance C_J in series to the buried-oxide capacitance C_{BOX} ($C_{BOX,J}$).

depletion region. Since $W \propto V_{ds,max}$ and $L \propto V_{ds,max}$, C_{ds} is almost independent of the transistor voltage rating. Hence, the C_{ds} related losses scale with the square of the voltage. The scaling is worse for the parasitic capacitances across the deep trench [C_{DTI}, Fig. 6(c)] and the BOX [C_{BOX}, Fig. 6(d)]. C_{BOX} scales with the device area ($W \cdot L$). Hence, the losses increase to the power of four, leading to 16× higher losses just by doubling the voltage. This indicates the challenges for IC design suitable for offline and dc-link voltages >100 V.

Fig. 7 shows loss-reduction techniques in HV SOI that are investigated and implemented in this design. In addition to resonant switching (Fig. 7, number ①), explained in Section III, capacitive-loss reduction is achieved by reducing the parasitic capacitances with series capacitors (Fig. 7, numbers ②–④). For example, the HV-biased junction capacitance C_J in series to C_{BOX} (Fig. 7, number ③) improves the efficiency by up to 32%, as confirmed by measurements in this work. Fig. 8 explains this efficiency improvement. It shows the measured scaling of C_J in series to C_{BOX} [$C_{BOX,J}$, (7)] with the voltage across C_J for three different connection types. The voltage across C_J is applied via the connection of the voltage source V_{BUR} to the buried layer BUR of C_J (shown in Fig. 7)

$$C_{BOX,J}(V_{BUR}) = \left(\frac{1}{C_{BOX}} + \frac{1}{C_J(V_{BUR})}\right)^{-1}. \tag{7}$$

In connection type 1), the buried layer BUR is shorted to the voltage source V_{BUR}, as shown in Fig. 7. For $V_{BUR} = 0$, $C_{BOX,J}$ equals to C_{BOX}, since C_J is shorted via the low-resistive connection of the buried layer BUR to V_{BUR}. The p-n junction below the BOX fully depletes at V_{BUR} between 30 V and 40 V (the depletion region touches the BOX, as shown in Fig. 7), which isolates C_J from V_{BUR} and results in a more than 7× smaller capacitance value and, thus, in lower capacitive losses.

In connection type 2), the buried layer BUR is connected via a series resistor with a high resistance (e.g., $R = 1\,M\Omega$) to the voltage source V_{BUR}, which leads to an additional reduction of $C_{BOX,J}$ below $V_{BUR} = 40$ V, as shown in Fig. 7. The high-resistive series resistor avoids large charging and discharging currents through V_{BUR} during fast transients such that the voltage-dependent junction capacitance $C_J(V_{BUR})$ is almost isolated from V_{BUR}, similar to a full depletion of the p-n junction below the BOX.

In connection type 3), the connection to the buried layer BUR is not connected/the connection is left open. In this case, $C_{BOX,J}$ equals to $C_{BOX,J}$ of connection type 2) at $V_{BUR} = 0$, which is lower than C_{BOX}, but still larger than the minimum possible capacitance value.

In conclusion, a high-resistive connection of the buried layer BUR to the highest available voltage (connection type 2) shows the highest reduction of the capacitive losses over the full voltage range. Thus, for HV designs in SOI, a p-n junction should be placed below the BOX, connected via a high-resistive series resistor (e.g., $R = 1\,M\Omega$) to the highest available voltage.

Especially at fast transients, the charging and discharging of the parasitic capacitance toward the substrate also causes a coupling of high-frequency currents into the substrate. The described capacitive-loss-reduction techniques reduce these currents, but they still can cause a disturbance of sensitive circuits. A further reduction of this substrate coupling and, thus, a higher common-mode transient immunity (CMTI) is achieved by connecting the handle wafer via low-resistive conducting trenches (Fig. 7, number ⑤), as suggested in [28] and implemented in this design.

B. HV-Switch Types

To achieve high efficiency and small chip size, on-chip HV switches with low area-specific on-resistance and low parasitic capacitances are required. Besides HV lateral SJ-MOSFETs [29], more and more HV technologies offer HV lateral SJ-LIGBTs [30]. As part of this work, both options are explored. The used SJ-MOSFETs show an area-specific on-resistance in the range of 1000–3000 mΩmm^2 (depending on the required blocking voltage, which is 100–350 V in this design).

The implemented SJ-LIGBT has 2× lower area-specific on-resistance, a lower degradation over a lifetime, and better thermal behavior, compared with SJ-MOSFETs and, thus, achieves a much smaller chip size and lower cost [31]. Due to the pulsed operation with short peak currents, the IGBT specific series p-n junction, which is also present in the used SJ-LIGBT, has a negligible influence on the efficiency. The typical tail current of IGBTs is not critical either, due to ZCS at turn-off and the missing reverse diode is not required by the presented topology. This makes the SJ-LIGBT an attractive choice as a power switch to decrease the switch size by 20.4% (versus SJ-MOSFETs) for the presented implementation while further increasing the converter efficiency.

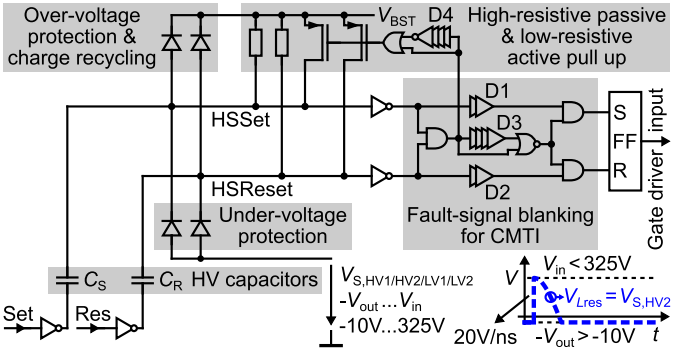

Fig. 9. HV low-loss capacitive level shifter with a high CMTI.

The structure of both transistor types results in small parasitic capacitances, which minimizes capacitive losses and enables high switching frequencies. Both, the implementation with SJ-MOSFET and the implementation with SJ-LIGBT, are compared in Section VI.

V. Block-Level Circuits

For light-load efficiency, low-loss subcircuits are required. Furthermore, measured slew rates as high as 20 V ns^{-1} demand high CMTI. This section describes the implementation of robust low-power subcircuits, required for the proper operation of the presented topology.

A. Gate Drivers

The gate drivers for the power transistors are implemented as cascaded inverter stages. Due to ZVS/ZCS (see Table I), the drivers of LV1 and LV2 can be slow, without too much influence on the efficiency. The drivers of HV1 and HV2 should be fast during turn-on to achieve ZCS but can be slow during turn-off without affecting ZCS and the efficiency.

B. Level Shifter

The HV level shifter (Fig. 9) is implemented as a capacitive level shifter, based on [32], to reduce steady-state losses. It comprises a combination of a high-resistive passive pull-up and a low-resistive active pull-up. The active pull-ups are deactivated during signal transmissions, which increases the charging times of C_S and C_R to accomplish a long-lasting signal at the HSSet and HSReset node. This enables small capacitor values of 50 fF for C_S and C_R.

The active pull-ups get enabled during common-mode transients, which occur after turning on HV1 or HV2. They charge the HSSet and HSReset nodes fast, to prepare the level shifter for the next signal transmission. Once the common-mode transient has ended, the active pull-up gets deactivated again after a fixed delay (∼10 ns, required as safety margin and provided by the inverter chain D4). Common-mode transients are detected via a simultaneous pull down at both signal nodes (HSSet and HSReset), caused by the transients.

A common-mode blanking circuit is used to improve the CMTI [32]. It deactivates both inputs of the flip-flop FF during an occurring common-mode transient. The blanking remains at a fixed delay (∼8 ns, provided by the delay chain D3) after the transient has ended. The delay chains D1 and D2 (∼3 ns each) ensure that their inputs get safely deactivated before the detected signals have propagated to the flip-flop. To ensure high CMTI, a symmetrical layout of the HSSet and HSReset nodes is required. Pull-up and pull-down diodes are implemented for under- and over-voltage protection. The pull-up diodes are also used for charge recycling during the falling transients, where the charge on C_S and C_R is not wasted but transferred to V_{BST} [32].

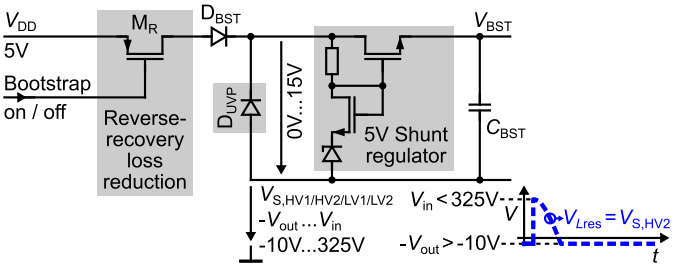

Fig. 10. Regulated bootstrap with reverse-recovery-loss reduction.

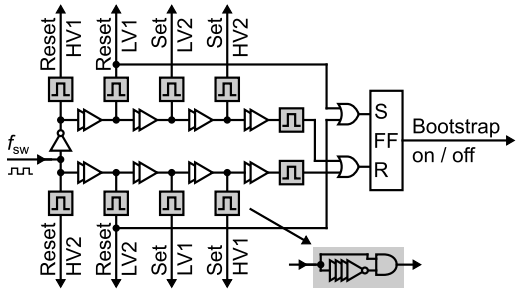

Fig. 11. Low-loss control circuit.

C. Bootstrap

A bootstrap circuit with a shunt regulator (Fig. 10) supplies the high-side devices with respect to the varying source potentials V_S. D_{UVP} acts as undervoltage protection during rising transients. Turning on the high-side devices causes the bootstrap capacitor C_{BST} to recharge until the gate–source voltage reaches the Miller plateau. The resulting current through D_{BST} causes reverse-recovery charges in D_{BST}. During the rising transient, these charges are removed, which causes reverse-recovery losses in D_{BST}. M_R in series to D_{BST} prevents these losses. It is turned off right before HV1 or HV2 turns on, which avoids recharging of C_{BST} and related reverse-recovery losses. The control signal for M_R is generated by the control circuit in Section V-D.

D. Control

Compared with other converter topologies, the relaxed timing of the power switches results in low control complexity. The control circuit for HV1, HV2, LV1, LV2, and M_R (Fig. 11) converts each edge of a rectangular input signal with 50% duty cycle into a series of turn-off and turn-on signals with appropriate delay in between. Each rising edge of the input

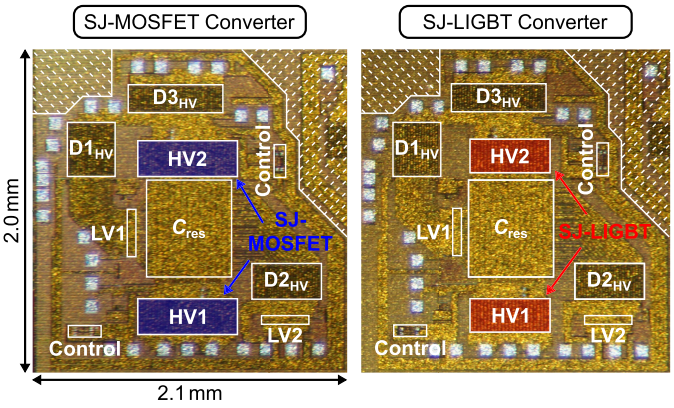

Fig. 12. Die micrograph of the 230 V converters. The converter with SJ-LIGBTs (right-hand side) has a 20.4% smaller switch size compared with the converter with SJ-MOSFETs (left-hand side).

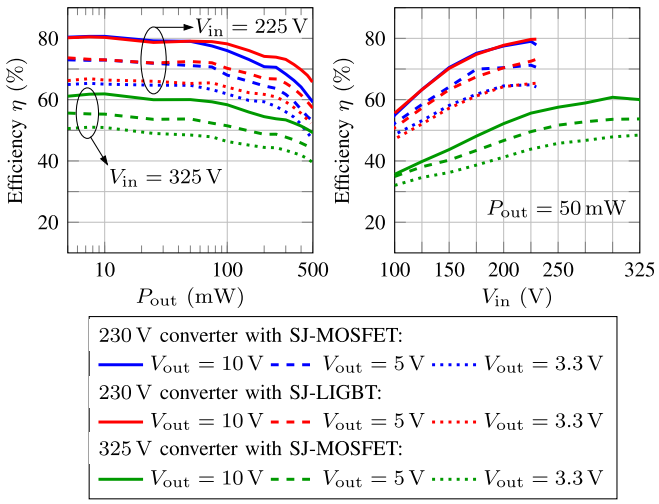

Fig. 13. Measured efficiency of the implemented converters.

signal initiates phase 1 and each falling edge initiates phase 2 according to Fig. 4. The delay chains are realized with cascaded inverters. A variation of the delay over process and temperature is not critical as long as the signals do not overlap. The switching frequency f_{sw} is derived from V_{out} by a comparator to achieve a closed-loop operation (see Fig. 3).

VI. Experimental Results

Fig. 12 shows the chip micrographs of the implemented 230 V SJ-MOSFET converter and the 230 V SJ-LIGBT converter. Each converter occupies an area of 4.2 mm^2. The implemented 325 V converter (not shown) requires an area of 6.1 mm^2 and has been implemented with SJ-MOSFET since an SJ-LIGBT with a voltage rating of $\geq$325 V is not yet available. A direct comparison of the HV switches HV1 and HV2 of both 230 V converters shows a 20.4% smaller area of the SJ-LIGBT toward the SJ-MOSFET. C_{res} is a sandwich capacitor within the metal layers. The metal spacing allows for floating HV terminals and low leakage currents.

Fig. 13 shows the efficiency plots for the 230 V converters (SJ-MOSFET and SJ-LIGBT) and the 325 V converter (SJ-MOSFET). The efficiencies include the losses of the power stage and of all block-level circuits. They have been measured by a source measurement unit and are also verified by shunt and current-probe measurements. The curves are measured for output voltages of 3.3, 5, and 10 V. The 230 V converters have an overall measured peak efficiency of ~81%. The peak efficiency of the 325 V converter is 61.9%. Due to the pulse-based control, presented in Section III, the efficiency curves of all three implementations show a flat run over a wide output power range [Fig. 13 (left)]. The high light-load efficiencies of all three converters are not only achieved by pulse-based control but also by the presented capacitive-loss-reduction techniques of Section IV-A. Thus, the light-load efficiency of the 325 V converter at $P_{out} = 50$ mW and $V_{in} = 325$ V reaches 60.8%. Without loss-reduction techniques, the efficiency would be at least 32% lower (see ③ in Fig. 7), corresponding to less than 30% efficiency. The light-load efficiency of the implementation with SJ-MOSFET and SJ-LIGBT at $P_{out} = 50$ mW and $V_{in} = 225$ V reaches 79% and 79.7%, respectively. The comparison of the implementation with SJ-MOSFET and with SJ-LIGBT in Fig. 13 (left-hand side) shows up to 4.2% higher efficiency of the SJ-LIGBT converter at output powers >100 mW with a 20.4% smaller switch size, making the SJ-LIGBT an attractive choice as power switch.

Fig. 14 shows the measured transient voltages at the inductor node (V_{Lres}, see Fig. 4), the source node of HV1 ($V_{S,HV1}$), and at the converter output (V_{out}) and the current through the inductor (I_{Lres}) at $V_{in} = 325$ V, $V_{out} = 5$ V, $P_{out} = 500$ mW, and $f_{sw} = 360$ kHz. The sinusoidal rising of I_{Lres} after turning on HV1 or HV2 and the sinusoidal falling of V_{Lres} at the same time, confirms the intended resonant switching behavior of the topology. The self-timed on-time, defined by L_{res} and C_{res}, achieves small values of ~50 ns, as required for the one-step conversion with the targeted high conversion ratios and small duty cycles. With $C_{out} = 470$ nF, a measured output-voltage ripple below ±5% of V_{out} is achieved. For sensitive applications, the output-voltage ripple could easily be decreased by increasing C_{out}, due to its linear relationship.

During the turn-on of the transistors, the measured current I_{Lres} and the measured voltages V_{Lres} and $V_{S,HV1}$ are zero. This indicates ZVS of LV1/LV2 and ZCS of HV1/HV2 and, thus, a reduction of the switching losses at turn-on. Similar behavior is observed at turn-off, where the current through all transistors is zero during freewheeling of I_{Lres} through D3$_{HV}$ until HV1/HV2 turn on. This confirms the intended ZCS of the transistors and the reduction of the switching losses at turn-off.

The operating frequency of the implemented converters ranges from $f_{sw,max} \sim 1$ MHz at $V_{in,min}$ and at high output power down to $f_{sw,min} \sim 1$ kHz at $V_{in,max}$ and at light-load conditions. The frequency range is verified by Figs. 15 and 16. Fig. 15 shows the transient measurements at $V_{in} = 325$ V, $V_{out} = 5$ V, and $f_{sw} = 1$ kHz and Fig. 16 the transient measurements at $V_{in} = 100$ V, $V_{out} = 5$ V, and $f_{sw} = 1$ MHz. Similar to other converters with variable switching frequency, care needs to be taken regarding electromagnetic interference.

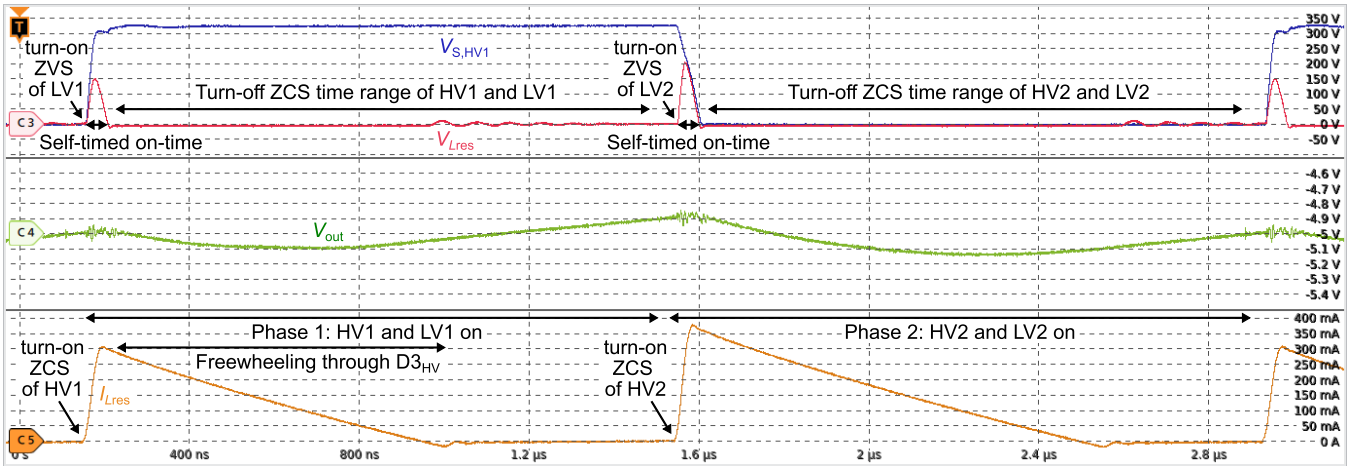

Fig. 14. Measured transients of the 325 V converter with SJ-MOSFET at $V_{in} = 325$ V, $V_{out} = 5$ V, $P_{out} = 500$ mW, and $f_{sw} = 360$ kHz.

TABLE II
COMPARISON WITH STATE-OF-THE-ART PUBLICATIONS AND COMMERCIAL PRODUCTS

	Converters with $V_{in,max} < 300$ V					Converters with $V_{in,max} > 300$ V			
	Xue [6], JSSC16	TMR 3-72 11WIR [1]	RDE0311 0S05 [2]	**This work 230V SJ-MOSFET**	**This work 230V SJ-LIGBT**	RAC01-05SC [3]	VSK-S1-5U [4]	PBO-1-S5-B [5]	**This work 325V SJ-MOSFET**
Technology	500 nm	n.r.	n.r.	**180 nm**	**180 nm**	n.r.	n.r.	n.r.	**180 nm**
V_{in} / V	12-100	43-160	40-160	**100-230**	**100-230**	115-370	120-430	70-430	**100-325**
V_{out} / V	10	5	5	**3.3-10**	**3.3-10**	5	5	5	**3.3-10**
$P_{out,max}$ / W	5	3	3	**0.5**	**0.5**	1	1	1	**0.5**
f_{sw} / kHz	2000	270-330	285	**1-1000**	**1-1000**	30	100	100	**1-1000**
L	1.5 µH	730 µH*	500 µH*	**10 µH**	**10 µH**	3000 µH*	1000 µH*	1500 µH*	**10 µH**
C_{out}	4.7 µF	188 µF*	300 µF*	**0.47 µF**	**0.47 µF**	330 µF	320 µF	168 µF	**0.47 µF**
additional ext. C's	$C_{fly} = 1$ µF	$C_{in} = 1.4$ µF*	$C_{in} = 2$ µF	**no**	**no**	$C_{in} = 4.4$ µF	$C_{in} = 6.6$ µF	$C_{in} = 4.7$ µF	**no**
Integrated power stage	yes	no	no	**yes**	**yes**	no	partial**	partial**	**yes**
Switching	ZVS	n.r.	n.r.	**ZVS & ZCS**	**ZVS & ZCS**	hard	hard	hard	**ZVS & ZCS**
η_p@ V_{in}	@$V_{in,max}$	@$V_{in,max}$	@$V_{in,max}$	**@225 V**	**@225 V**	@325 V	@325 V	@325 V	**@325 V**
$V_{out} = 3.3$ V	n.a.	n.a.	n.a.	**65.3 %**	**66.9 %**	n.a.	n.a.	n.a.	**51 %**
$V_{out} = 5$ V	n.a.	77.7 %*	76.9 %	**73 %**	**73.7 %**	77.3 %*	70.5 %*	70.2 %*	**55.6 %**
$V_{out} = 10$ V	82.5 %	n.a.	n.a.	**80.7 %**	**80.5 %**	n.a.	n.a.	n.a.	**61.9 %**
η_p@ $P_{out} = 50$ mW $V_{in} \geq 100$ V									
$V_{out} = 3.3$ V	n.a.	n.a.	n.a.	**64.9 %**	**65.4 %**	n.a.	n.a.	n.a.	**48.5 %**
$V_{out} = 5$ V	n.a.	27.6 %*	29.6 %	**71.3 %**	**73.2 %**	53.8 %*	35.9 %*	34.3 %*	**53.7 %**
$V_{out} = 10$ V	< 56 %	n.a.	n.a.	**79 %**	**79.7 %**	n.a.	n.a.	n.a.	**60.8 %**
Power density / mW/cm^3	n.r.	1280	387	**752**	**752**	75	74	158	**752**

n.r. = not reported n.a. = not applicable * = measured ** = integrated primary power switch only

However, the implemented resonant approach reduces the frequency spectrum compared with hard-switching converters.

Table II indicates a reduction of the values of L and C_{out} in comparison with the listed state-of-the-art publications and commercial products by more than 50× down to 10 μH and by more than 10× down to 0.47 μF, respectively. The design in [6] uses $L = 1.5$ μH, but is limited to 100 V.

At 50 mW light load and $V_{out} = 5$ V this work achieves 73.2%/53.7% efficiency for $V_{in} = 225$ V/325 V. This is higher than the state-of-the-art and similar to [3], which needs a very large transformer of 3 mH and has no integrated power stage. The good power density of [1] comes along with poor light-load efficiency. Due to the reduced requirements on the active and passive components, almost all of the components could be integrated on one single die. As a result, the presented design has more than 5× higher power density than the other commercial power modules included in Table II.

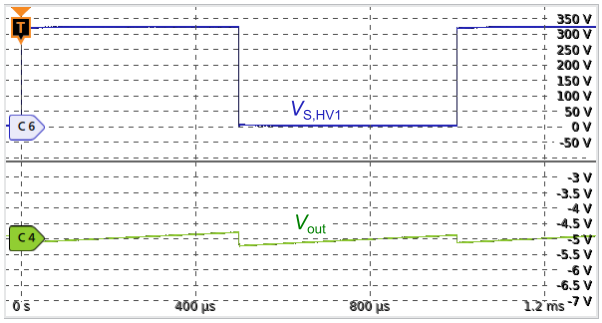

Fig. 15. Measured transients of the 325 V converter at $f_{sw} = 1$ kHz.

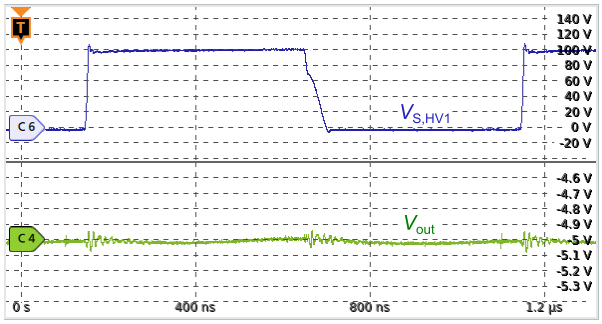

Fig. 16. Measured transients of the 325 V converter at $f_{sw} = 1$ MHz.

VII. Conclusion

The power supply gap between energy harvesting and discrete power modules and the trend toward higher functionality and decentralization leads to a demand for new approaches in compact and efficient IC-level power conversion. Required are converters with output powers between a few milliwatts up to 500 mW and input voltages up to 400 V converted down to a 3.3–10 V output. The discussion of advantages and drawbacks of state-of-the-art topologies for HV power conversion shows a lag of topologies, suitable for light-load conditions and conversion ratios of up to 100. The main challenges for most of the existing HV topologies, such as multi-level converters or converters with transformers, are the control complexity at high conversion ratios in addition to very large external components, leading to poor light-load efficiency and low power densities.

This work presents a self-timed resonant HV dc-dc converter topology, implemented in HV CMOS SOI. It is optimized for a one-step conversion from 100–325 V down to a 3.3–10 V output for applications below 500 mW. Layout and design recommendations for capacitive loss reduction, essential at high voltages, are described and validated by measurements. It includes an HV-biased junction underneath the BOX, which is measured to improve the efficiency by up to 32%. Efficiency and CMTI optimized subcircuits, such as gate driver, bootstrap supply, and level shifter, are introduced. Converter implementations with different HV transistors, SJ-LIGBTs, and SJ-MOSFETs, show a switch-size reduction by 20.4% and a measured improvement of the efficiency at $P_{out} > 100$ mW by up to 4.2% if an SJ-LIGBT is used instead of an SJ-MOSFET.

Compared with state-of-the-art publications and commercial products, the implemented converters show an overall peak efficiency as high as ∼81%. Unlike bulky power modules, they comprise an on-chip power stage with only one external inductor (10 μH) and capacitor (470 nF). Due to the high light-load efficiency of 79.7% at $P_{out} = 50$ mW and the high power density of 752 mW/ cm^3, the converters are well suitable for IoT, smart home, e-mobility, and industrial applications.

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