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Multilayer ion trap technology for scalable quantum computing and quantum simulation

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Abstract

We present a novel ion trap fabrication method enabling the realization of multilayer ion traps scalable to an in principle arbitrary number of metal-dielectric levels. We benchmark our method by fabricating a multilayer ion trap with integrated three-dimensional microwave circuitry. We demonstrate ion trapping and microwave control of the hyperfine states of a laser cooled $^{9}Be^{+}$ ion held at a distance of 35 μm above the trap surface. This method can be used to implement large-scale ion trap arrays for scalable quantum information processing and quantum simulation.

1. Introduction

Trapped ions are not only one of the most promising platforms for the practical implementation of quantum computing and quantum simulations, but also sensitive systems for measuring very small magnetic and electric fields. Typically, they are held in Paul or Penning traps at high vacuum, laser cooled close to absolute zero temperature, and their internal states coupled to their motion can be manipulated with high fidelity by either laser fields [1, 2] or microwave radiation [3, 4]. However, scaling these elementary demonstrations to larger systems remains a formidable technological challenge [5].

Surface-electrode ion traps [6] represent a strong candidate for the realization of a quantum charge-coupled device [7, 8] for scaling quantum logic operations. Such an ion trap array could feature dedicated zones for storing, manipulation and read-out, thus promising a modular hardware for quantum computation and quantum simulation [9]. Conventionally, in surface-electrode ion traps all electrodes are built in a single plane by standard microfabrication techniques [10]. First integration of key scalable elements into a single layer chip such as micro-optical components [11], nanophotonic waveguide devices [12] or microwave conductors (MWC) [13] have been demonstrated. However, interconnecting separated components built in this system imposes new challenges on trap design where signal lines have to be routed around other elements. Therefore, the realization of a highly integrated large-scale ion trap device requires a more flexible approach where signal routings can be distributed on vertically well-separated levels of interconnects.

Demonstrations of multilayer processes in ion traps so far are based on techniques borrowed from microelectromechanical systems (MEMS) [14, 15] or CMOS [16, 17]; however the resulting trap structures are limited to thin interconnect levels. Moreover, there is a need of a nearly material-independent processing capable of including most dielectric substrates and thick metallization. For example, room temperature and cryogenic operation each favor different dielectric substrates when it comes to high thermal conductivity and low rf loss tangent. Thick metallization, when combined with narrow gaps between neighboring electrodes, allows for efficient shielding of the ion(s) from charges that might accumulate on top of exposed dielectrics in between electrodes and affect the ion(s) in an uncontrolled way [18]. Thick metallization can support strong currents for integrated control elements based on static or oscillating magnetic field gradients [19, 20]. Thick vertical interconnect access (VIAS) are of general interest for building ion trapping devices as they allow to

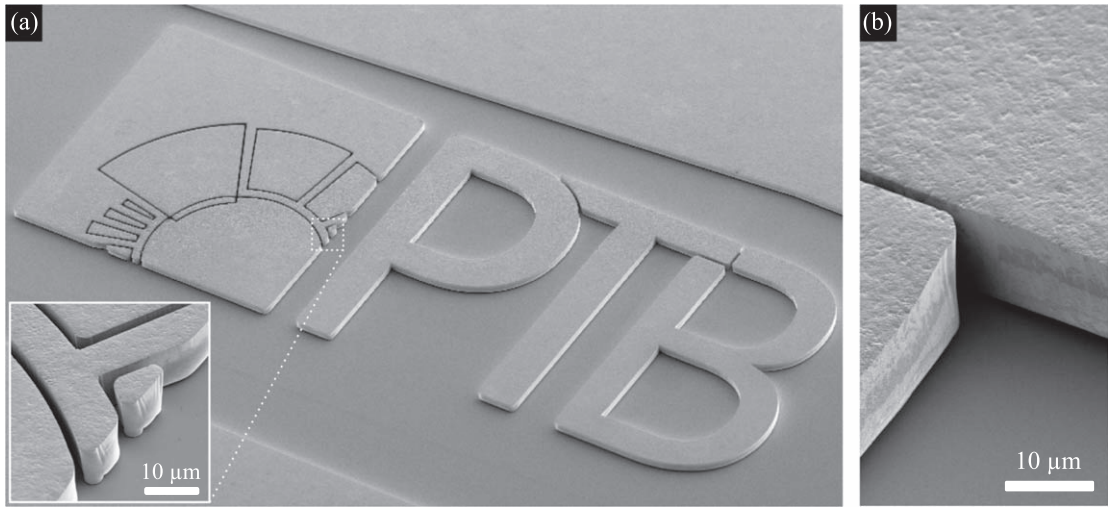

Figure 1. Gold structures with high aspect ratio supported on sapphire. (a) Au structures separated by gaps of about 2 μm with a high aspect ratio of 5:1 (inset). (b) Pair of Au electrodes separated by a 0.8 μm gap, resulting in a gap with an aspect ratio of 14:1. For both SEM micrographs shown in (a) and (b) the sample is tilted by 45°.

minimize parasitic capacitances and crosstalk and reduce the risk of chip electrical breakdown. Any fabrication process will have to comply with the specific requirements of an ion trap, such as a material mix which features extremely low material outgassing and needs to be compatible with ultra-high vacuum operation, low dielectric losses and non-magnetic metal surfaces.

Here we present a robust fabrication method, scalable to an in principle arbitrary number of planarized thick metal-dielectric layers, enabling the realization of scalable ion trap devices. The method complies with the stringent requirements of a scalable ion trapping array, allowing the fabrication of complex trap designs using relatively forgiving fabrication techniques on nearly any type of substrate (sapphire, quartz, AlN, Si, …) and insulating dielectrics such as polyimide, teflon or BCB. To demonstrate the approach, we fabricate and operate a multilayer ion trap chip with three-dimensional (3D) microwave circuitry towards the realization of high fidelity muli-qubit gates [13]. A fabrication yield of above 80% is achieved, limited by the stringent geometric requirements for the particular application of integrated near-field microwave control. For a more conventional multilayer design yields exceeding 90% should be possible.

2. Fabrication methods

Methods for building surface-electrode ion traps [10] or atom chips [21, 22] are typically based on standard semiconductor processing. For the simplest case, in which all metal electrodes are aligned in a single plane, a generic fabrication workflow consists of a three-step processing: wafer patterning, electrode formation and electric insulation. Depending on the requirements one will choose between different materials and processing methods at hand. In what follows we will describe our own fabrication methods to build single layer and multilayer microfabricated ion traps.

2.1. Single level processing (SLP) method

For the SLP method all steps are carried out on 3 inch diameter wafers in a fabrication line located at Physikalisch-Technische Bundesanstalt, Braunschweig. We have fabricated similar structures to the ones presented in figure 1 on AlN, sapphire, organic polymers and high resistivity (HiR) float zone Si wafers, demonstrating the compatibility of the method with a wide range of substrates suitable for ion trap technology.

The first step during wafer preparation involves the deposition of a Ti adhesion layer (15 nm thin) and an Au seed layer (50 nm thin) on top of the substrate by resistive evaporation. The first film acts as an adhesion promoter between the substrate and the Au seed layer, and the second film serves as a starting conductive layer for a later electrodeposition step.

Second, to define the trap geometry, a 25 μm thick positive or 16 μm thick negative resist is spin coated on top of the Au seed layer and the wafer is exposed to UV light by contact lithography. A subsequent development of the exposed resist results in open areas on the substrate which are filled to a desired thickness by electrodeposition of Au in a sulphite-based bath.

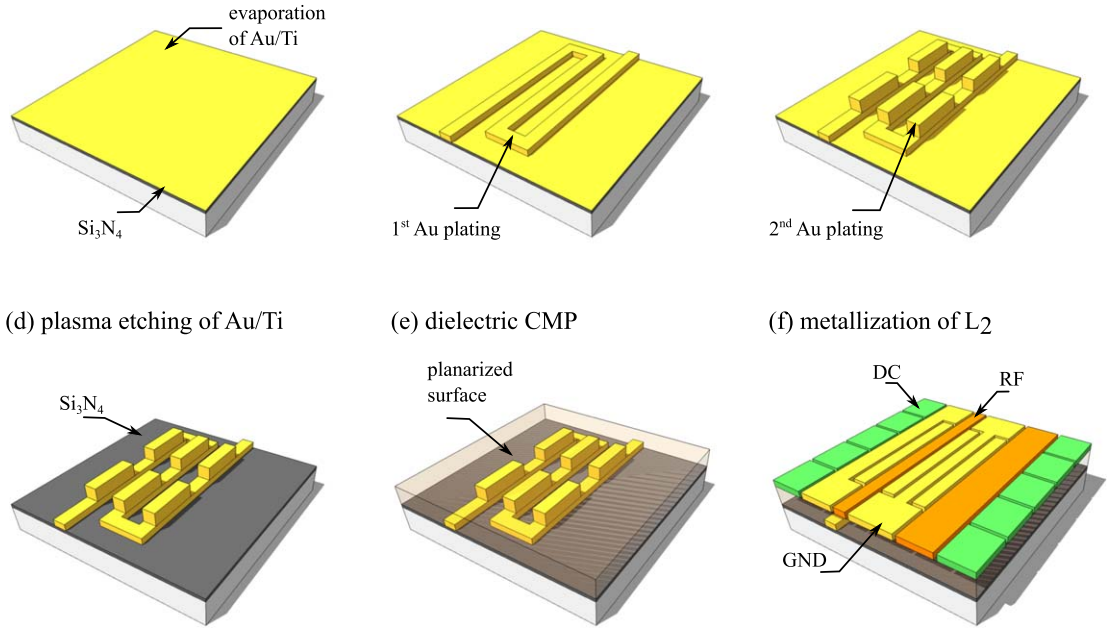

Figure 2. Schematics of the multilevel processing flow. (a) A wafer is coated with an SiN film and a conductive Au/Ti bilayer. (b) A lower level (L_1) is formed via electroplating. (c) A via V_1 is electroplated on top of L_1. (d) Dry etching of Au/Ti bilayer film. (e) A polymer is spin coated over both L_1 and V_1 and subsequently planarized by CMP. (f) A second metallization L_2 repeating steps (a), (b) and (d) on a planarized dielectric surface. Exposed dielectric between electrodes in L_2 is removed by plasma etching down to the top surface of the Si_3N_4 layer.

Finally, after gold electroplating the resist mask is removed chemically and the wafer is cleaned under oxygen-based plasma etching. Additionally, the wafer is exposed to a fluorine-based plasma to further remove possible resist debris. Immediately afterwards the seed Au layer is removed via Ar etching and the Ti layer removed by a fluorine-based plasma etching.

This method allows the fabrication of gold structures with high aspect ratios as exemplified in figure 1. Gold structures with a width as narrow as 5 μm and gap separation as narrow as 2 μm are shown in figure 1(a). Another example is depicted in figure 1(b) consisting of a pair of gold electrodes separated by a gap with an aspect ratio of 14:1. One additional advantage of the method is that after dry etching of the Au/Ti bilayer the resulting trap surfaces have a superior finishing quality compared to the commonly used wet etching.

2.2. Multilevel processing (MLP) method

In this section a MLP method is presented, which combines techniques borrowed from MEMS and Integrated Circuits processing. The method is also compatible with other common substrates used for ion trap technology such as silicon, sapphire, borosilicate glass and quartz.

To demonstrate the simplicity and robustness of our method we have fabricated an ion trap with integrated 3D microwave circuitry. It comprises a lower interconnect level L_1 and an upper electrode level L_2. An additional vertical interconnect access V_1, called via, allows microwave signals to be transmitted between levels. A more detailed description of the microwave and quantum logic aspects of the trap design and the corresponding characterization will be covered elsewhere [26].

The method presented here mainly consists of six processing steps: (a) wafer preparation, (b) metallization of lower level L_1, (c) metallization of via V_1, (d) removal of seed layer, (e) deposition and planarization of dielectric layer D_1 and (f) metallization of upper level L_2. A schematics of the fabrication flow is given in figure 2.

The supporting material is a 3 inch silicon wafer with HiR ($\sigma > 1 \times 10^4$ Ωcm). On top of it and as shown in figure 2(a), a 2 μm thick film of Si_3N_4 is deposited by physical enhanced chemical vapor deposition. This dielectric film may improve trap operation by avoiding detrimental diffusion of Au into silicon and increasing the flashover voltage as demonstrated in [23]. Thereafter, a 10 nm thin layer of Ti and a 50 nm thin layer of Au are thermally evaporated on top of Si_3N_4.

To build the lower level L_1 on top of Si_3N_4/Si, a negative resist is spin coated and patterned via UV lithography. Once the negative resist is developed to form a resist mold, gold electrodes are grown (4 μm) by electroplating as depicted in figure 2(b). After electroplating is completed, the resist mask is stripped and the wafer cleaned under plasma etching.

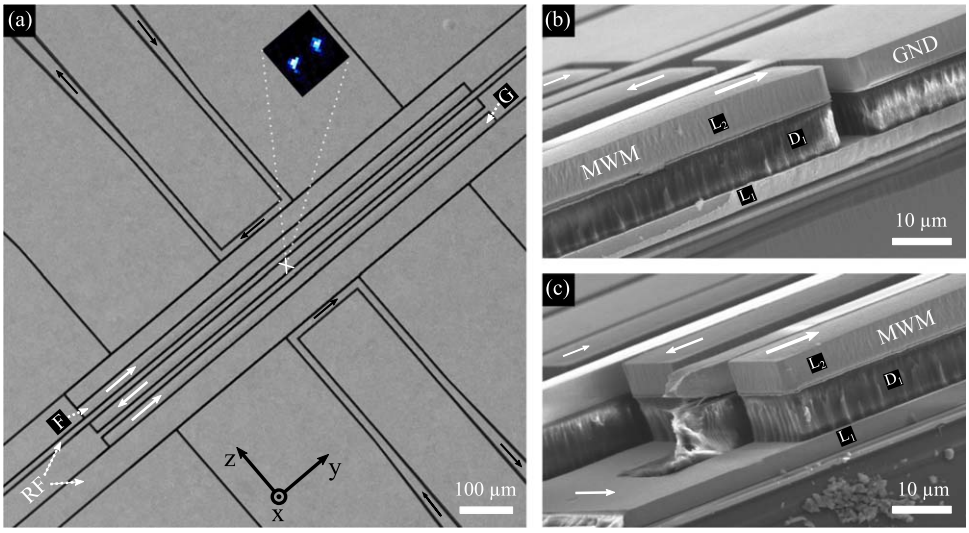

Figure 3. SEM micrograph of the central part of a trap chip fabricated using the MLP method. White and black arrows are drawn on top of the microwave conductors as a guide for the eye. (a) Upper metal level L_2 of the trap chip in which black lines correspond to electrode gaps of about 5 μm. (b) Part of a cleaved chip showing a cross-section mainly on the *xy*-plane around position 'G'. (c) Similar to (b) but with a close-up corresponding to position 'F' in (a). Ions are trapped at $d = 35$ μm above the position marked as '*X*'.

For the metallization of the via V_1 we repeat the photolithography and electroplating steps presented in (b) but this time on top of L_1 by using a thick (>12 μm) developed negative resist as a plating mold. Electroplated VIAS grown up to 10 μm on top of L_1 are depicted in figure 2(c) after stripping the negative resist mask and plasma cleaning of the wafer.

To remove the Au seed layer and the Ti adhesion layer we use the last dry etching step from the SLP method. This step allows a controllable etch of Au and Ti of 50 nm min^{-1} and 10 nm min^{-1} respectively, resulting in a minimal change of the surface quality on top of both L_1 and V_1 surfaces. The electrically isolated elements on V_1 and L_1 are schematically illustrated in figure 2(d).

Polyimide (PI 2600 series, HD MicroSystems^{TM}) is then spin coated on top of L_1 and V_1 (figure 2(e)). After thermal curing, excess material is present on top of the underlying structures L_1 and V_1. The imprinted dielectric topography is globally planarized through a chemical-mechanical polishing step, which is stopped at the top of V_1 or close to it. To assure electrical contact between V_1 and the subsequent level L_2 a global or local etch-back process is performed. In the case of a local etch-back, this requires an additional photolithography step. In that case, the resulting resist mask covers the PI film everywhere except on defined zones on top of the V_1 area. After performing a fluorine-based plasma etch, the remaining material on top of V_1 is completely removed.

To define the top metal layer the SLP method is again employed but this time on top of the planarized polymer surface (figure 2(f)). Once the plating has been completed (5 μm) and the resist mold removed, the remaining polymer film between gaps underneath and between the electrodes in L_2 is etched down to the Si_3N_4 layer by a fluorine-based plasma to hide possible patch potentials built on the exposed insulator.

3. Fabrication outcome and trap operation

Here we briefly present the design and characterization of a trap with 3D MWC integrated into a microfabricated ion trap using the MLP method. The microwave circuitry is embedded to implement quantum logic operations using near-field microwaves [13, 20, 24, 25]. The specific design is discussed elsewhere in detail [26] and here only described as one of many scenarios that benefits from the multilayer technology.

In the upper level (L_2) the trap includes two RF electrodes and ten DC electrodes to confine the ions to a local minimum (x_0, z_0), see figure 3(a). A microwave signal (white arrows) of frequency 1 GHz can be applied on a 3D microwave meander (MWM) conductor between two contact points labeled as 'F' and 'G', thus generating an oscillating magnetic near-field gradient '*B*' in the *xz*-radial plane with a local minimum at (x_1, z_1). The three apparent independent MWC indicated by the white arrows are indeed part of a single 3D MWM connected to L_1 by VIAS and routed over L_1 as indicated in figure 3. A central part of a diced trap chip (5 mm $\times$ 5 mm) fabricated using the MLP method is presented in figure 3(a). There are also two additional MWC surrounding the central DC electrodes, in which an oscillating current (black arrows) can be applied to produce an oscillating *B* field.

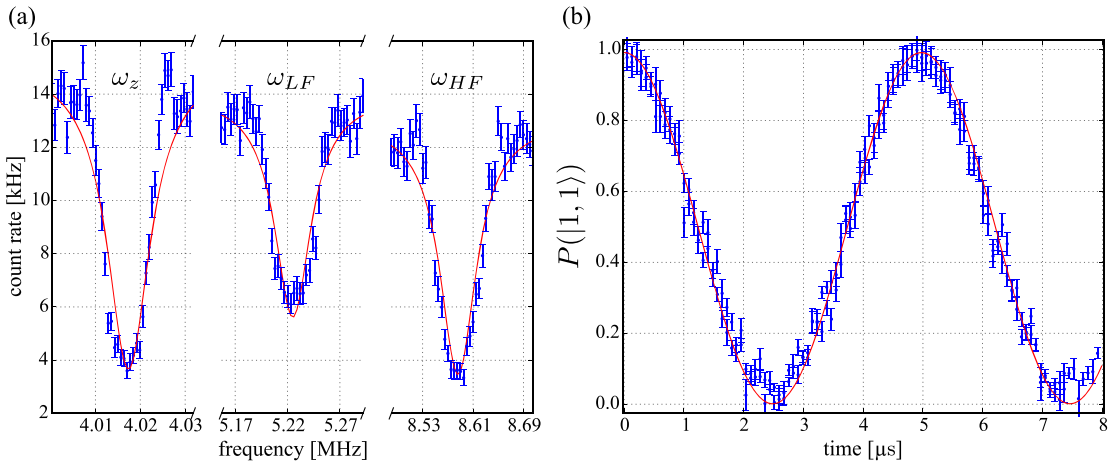

Figure 4. Secular frequencies and microwave qubit transition. (a) Motional frequency measurements using the DC tickle method. The (red) solid lines show Lorentzian fits to the data. The left axis corresponds to the photon average counts after a fluoresence detection of 1.3 ms. (b) Rabi flopping on the qubit transition using a microwave conductor embedded in the trap driving the $|F = 1,\ m_F = +1\rangle \leftrightarrow |F = 2,\ m_F = +1\rangle$ [27] transition.

A cleaved chip revealing a cross-section view of the metal-dielectric stack around position 'F' and position 'G' is shown in figures 3(b) and (c), respectively. The ion trap (RF and DC electrodes) as well as the uppermost part of the MWM conductor are entirely located in L_2, whereas the microwave signals and the ground plane are routed between L_1 and L_2 through VIAS in V_1 (not visible in the micrograph but behind D_1 in figures 2(b) and (c)). Any remaining non-planarity is due to imperfections in the etch-back process and independent of the number of metal-dielectric layers implemented. It can be made much smaller than 1 μm, which again is small compared to the typical ion-to-electrode distance.

Removing both Au and Ti films by means of dry etching has improved the trap surface quality. For a similar chip as the one here presented an rms roughness $R_{\mathrm{rms}} = 8.3 \pm 0.5$ nm is obtained by atomic-force microscopy over an area of 25 μm $\times$ 25 μm. This represents a two-order of magnitude improvement when compared to a wet etching process using aqua regia [27]. These nearly mirror-like surfaces are relevant since there is a reduction of stray light scattered in the direction perpendicular to the trap surface during resonance fluorescence imaging for ion state detection. Also an ion trap with minimal surface roughness might be less prone to anomalous motional heating at cryogenic temperatures [28].

The diced trap chip is glued onto a copper block and wirebonded to a custom printed circuit board for filtering and signal routing. The whole assembly is installed in a vacuum system at a pressure better than 1×10^{-11} mbar and connected to an in-vacuum coaxial resonator similar to the one used in [29]. For ion loading we employ a laser ablation scheme [27] and subsequent two-photon ionization using 235 nm light [30]. Single $^9Be^+$ ions are loaded at 35 μm above the upper surface of L_2 around the position 'X' (see figure 3(a)).

For an RF drive frequency of $\Omega_{\mathrm{RF}} = 2\pi \times 176.5$ MHz with amplitude $V_{\mathrm{RF}} = 100$ V and supplied DC voltages ranging within ± 25 V, we measure secular trap frequencies of $(\omega_z, \omega_{\mathrm{LF}}, \omega_{\mathrm{HF}}) = 2\pi \cdot (4.02, 5.23, 8.59)$ MHz. To determine the trap frequencies we apply an oscillating tickle voltage to one of the DC electrodes and scan the frequency [31]. Once the tickle drive is resonant with a secular frequency, the motion of the ion is excited and the ion fluorescence drops (figure 4(a)).

Finally we employ the integrated MWC to manipulate the internal state of the ion. Figure 4(b) shows Rabi oscillations on the qubit transition $|F = 1,\ m_F = +1\rangle \leftrightarrow |F = 2,\ m_F = +1\rangle$ [27] of the electronic ground state $^2S_{1/2}$ of a single $^9Be^+$ ion at an external magnetic field of $|\boldsymbol{B}_0| = 22.3$ mT when applying a microwave current of frequency $\omega_0 \simeq 1\,082.55$ MHz to one of the MWC conductors. Here, F is referring to the total angular momentum $\boldsymbol{F}$ and m_F the quantum number of its projection on $\boldsymbol{B}_0$. The state readout is carried out via ion fluorescence detection on the closed-cycling transition $|S_{1/2},\ F = 2,\ m_F = 2\rangle \rightarrow |P_{3/2},\ m_J = +3/2,\ m_I = +3/2\rangle$, combined with suitable microwave transfer pulses [27].

4. Conclusion and outlook

We have presented a novel multilayer method for fabricating scalable surface-electrode ion traps. The flexibility and robustness of the method allows to benchmark the integration of 3D microwave circuitry into a multilayer

ion trap. Furthermore, we have demonstrated successful trapping of $^{9}Be^{+}$ and basic qubit manipulation by applying microwave oscillating currents on one of the conductors.

The MLP method presented here can in principle be extended to a nearly arbitrary number of layers to comply with the stringent needs of scaling surface-electrode ion traps. Moreover, the method permits the integration of 3D and planarized features with high aspect ratio. This technique opens new routes towards the realization of more complex and powerful ion trap devices.

In contrast to a typical CMOS situation where the 'device' is fabricated on top of the substrate, with interconnect layers on top of the device, in our case the 'device' is the top electrode layer which is controlling the ion(s), whereas the layers closer to the substrate are used as interconnects. In the future, these lower interconnects may be combined with through-wafer VIAS to achieve contacting of the ion trap chip from the back-side, eliminating the need of wirebonds and likely obstruction of laser beams. Through-wafer slots for back-side ion loading can also be produced in the same way. These same techniques could be applied to realize so-called analog quantum simulators in ion trap arrays [32–34], possibly with integrated control [35]. Moreover, such an approach may enable the embedding of complex integrated components such as trench capacitors [36, 37], low-loss integrated waveguides [38]; or the realization of more elaborate devices including reliable ion-transport junctions [39, 40], increased optical access [17] or manipulation of scalable arrays of two-dimensional trapped ion systems [33, 34].

The MLP method can also be used to extend multilayer 'atom chips' [22, 41, 42] or to fabricate scalable hybrid atom-ion traps [43, 44] for quantum many-body physics experiments and quantum sensing with neutral atoms. In this context the thick metal conductors can support substantial currents required for magnetic trapping and the planarization together with the demonstrated minimized surface roughness allows the implementation of mirror-like surfaces and transfer coatings for integrated magneto-optical traps.

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