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Wet chemical polishing for industrial type PERC solar cells

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Abstract

Industrial PERC cell process flows typically apply the polishing of the rear side after texturing as well as the edge isolation after $POCl_3$ diffusion. In this paper, we present a novel single step polishing process which we apply post double sided texturing and diffusion in order to remove the rear emitter and to reduce the rear surface roughness. One challenge is to minimize the etch back of the front side emitter during rear side polishing due to the reactive gas phase of the polishing process. By optimizing the polishing process, we are able to limit the increase of the emitter sheet resistance below 5 Ω/sq. However, the wet cleaning post polishing contributes an additional 20 Ω/sq emitter sheet resistance increase which is subject to further optimization. We compensate the emitter sheet resistance increase due to wet cleaning by applying a 45 Ω/sq $POCl_3$ diffusion instead of a 60 Ω/sq diffusion. The resulting PERC solar cells with polished rear surface post texture and diffusion show conversion efficiencies up to 19.6% which is comparable to the reference PERC cells which apply a rear protection layer instead of a polishing process.

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Keywords: Wet chemical polishing; screen-printing; PERC solar cells; cleaning sequences; sheet resistance

1. Introduction

Passivated emitter and rear cells (PERC) are very promising for next-generation industrial solar cells as stated in the International Technology Roadmap [1]. A target for further development is to reduce the number of additional process steps for PERC solar cells compared to full-area Al-BSF cells which currently dominate the commercial market. Industrial PERC process flows typically involve two wet

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chemical single side etching steps [2, 3]. The first etching step aims at polishing the previously textured rear side of the cell and thus reduce the rear surface roughness in order to increase efficiencies [4, 5]. A second etching step is applied after $POCl_3$-diffusion in order to remove the rear emitter. In this paper, we introduce a novel single step polishing process after double sided texturing and phosphorus diffusion that simultaneously removes the rear side emitter and reduces the rear surface roughness. We optimize several process parameters including the etch back of the front side emitter during the polishing by the reactive gas phase [3], the sheet resistance of the $POCl_3$ diffusion, the polishing duration as well as the cleaning sequence post polishing. The resulting industrial-type PERC solar cells with polished rear surface achieve conversion efficiencies up to 19.6% which is comparable to the reference PERC cells which apply a rear protection layer instead of a rear polish process.

2. Experimental

We use the RENA InPilot tool [2] for the rear side polishing process. In this tool, wafers are transported inline on rollers similar to the wet chemical junction isolation process in order to allow a single sided etching of the wafer rear side as shown in Fig.1. The wet polishing chemistry forms a gas phase which can lead to etching of the front wafer surface, however with much lower etch rates compared to the rear polishing etch rates. To further reduce etching from the gas phase we modify the polishing recipe in order to reduce the reactivity of the gas phase. The optimized polishing recipe reduces the emitter sheet resistance increase due to the gas phase etch from about 30 Ω/sq down to 5 Ω/sq as shown in table 1.

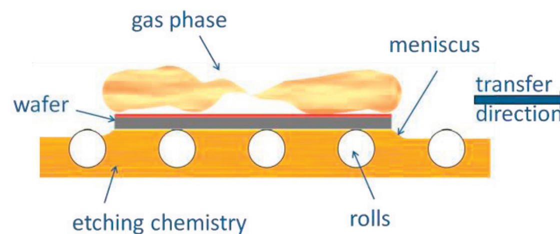

Fig. 1. Schematic drawing of the rear polishing process

Starting with textured and $POCl_3$ diffused wafers we realize different rear surface roughness by adjusting the transport speed and hence the polishing removal. In this work we use small removals of 2.5 µm for all polished PERC cells, since it was reported that when using AlO_x/SiN_y rear passivation stacks small polishing removals are sufficient to obtain high PERC cell efficiencies [5].We fabricate solar cells using 190 µm thick *p*-type 156×156 mm² boron-doped Cz-silicon wafers. The process flow is shown in Fig. 2 a). The green process steps describe the process flow applying the novel polishing process at the wafer rear. After double sided alkaline texturing and phosphorus diffusion, the RENA InPilot tool is used to apply a polishing removal of 2.5 µm at the rear surfaces of the wafers. This reduces the initial pyramid height of 3-4 µm to roughly 2 µm (see fig. 2). After the polishing step a cleaning sequence is carried out prior to depositing the ALD Al_2O_3/SiN_x rear passivation in order clean the rear surface. The front and rear contacts are formed by screen printing. A schematic drawing of the resulting PERC solar cell is shown in Fig. 2 b). As a reference, we process PERC cells applying a rear protection layer before texturing and phosphorus diffusion [6] according to the blue process flow in Fig. 3 a).

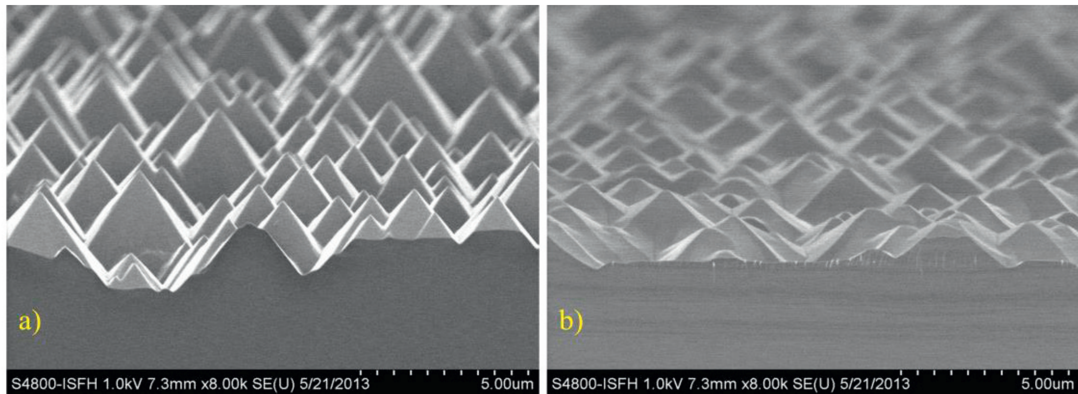

Fig. 2. SEM cross section images of a wafers front side a) and rear side b) after double sided texturing and diffusion and subsequent rear side polishing with a removal of 2.5 µm.

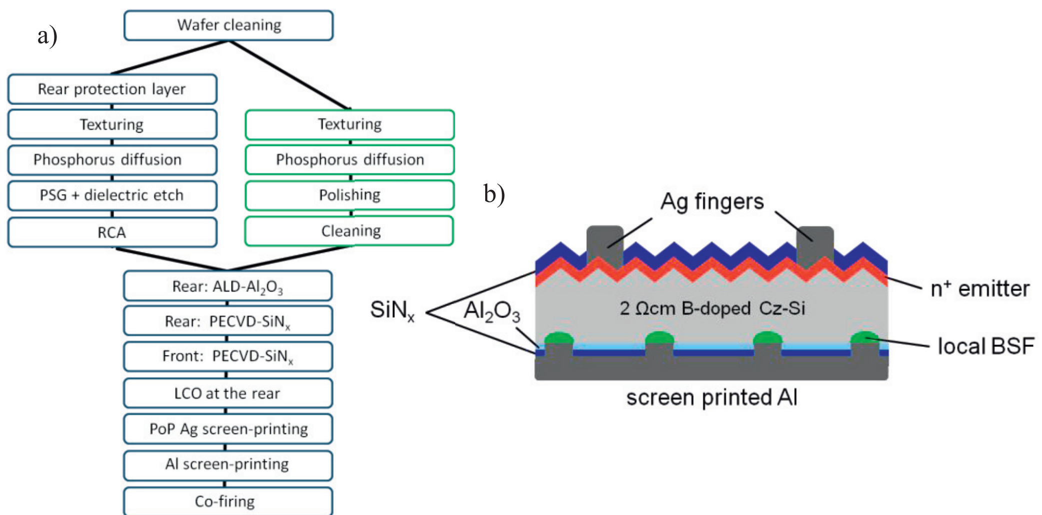

Fig. 3. a) PERC solar cell process flows of the reference process (blue) and the polishing process (green). b) A schematic drawing of the resulting PERC cell.

3. Results and discussion

Test wafers with a sheet resistance of 60 Ω/sq post $POCl_3$ diffusion show that the polishing process increases the sheet resistance up to 5 Ω/sq (see tab. 1). In case of the process sequence involving the rear-polishing, wafers have to be transported outside the high quality clean room to the InPilot tool which is located in the ISFH SolarTeC. Accordingly, after polishing an additional NH_4OH/HCl cleaning is required for returning the wafers into the cleanroom to continue processing with the standard RCA clean. This two step cleaning procedure is the cleaning sequence 1 shown in table 1 which causes an increase in emitter sheet resistance of 18 Ω/sq instead of 12 Ω/sq for the reference RCA cleaning process.

Accordingly, we apply a 45 Ω/sq phosphorus diffusion instead of a 60 Ω/sq diffusion in order to obtain a good contact resistance of the screen-printed Ag fringer to the emitter. With 2.5 µm polishing removal, the resulting PERC solar cells demonstrate conversion efficiencies up to 19.6% and similar IV parameters compared to the reference PERC cells with 19.5 % efficiency as shown in Fig. 3. The slightly lower J_{sc} values but higher FF values of the polished PERC cells compared to the reference PERC cells indicate that the final emitter sheet resistance of the polished PERC cells is a bit too low. Accordingly, the polished PERC cells could be further optimized either by slightly increasing the emitter sheet resistance post $POCl_3$ diffusion or preferably by increasing the etch depth in the single-side polishing step in order to slightly increase the gas phase etch back and thus further minimize the charge carrier recombination in the emitter and reduce the rear surface roughness at the same time. We additionally process PERC cells with textured rear surface according to the reference process flow with the only difference that the protection layer is applied post texturing, not prior to texturing. Figure 4 clearly shows that a reduced rear surface roughness due to polishing significantly improves the solar cell parameters compared to a fully textured rear surface.

Table 1. Emitter sheet resistance increase $\Delta R_\square$ post polishng and post wet cleaning which are stated for a starting sheet resistance of 60 Ω/sq post $POCl_3$ diffusion. We evaluate three different cleaning sequences after rear side polishing with 2.5 µm silicon removal in comparison to the reference which applies only RCA cleaning.

process type	Reference PERC	Polished, clean. seq. 1	Polished, clean. seq. 2	Polished, clean. seq. 3
cleaning sequence after polishing step	RCA	NH_4OH/HCl, RCA	NH_4OH/HCl, Piranha, SC2	KOH-Dip, HCl, Piranha, SC2
	Increase of the emitter sheet resistance [Ω/sq] after polishing and cleaning			
$\Delta R_\square$ Polishing [Ω/sq]	-	5	5	4
$\Delta R_\square$ Cleaning [Ω/sq]	12	18	5	4
$\Delta R_\square$ total [Ω/sq]	12	23	10	8

In order to process PERC solar cells with rear polish applying a more typical diffusion (e. g. 60 Ω/sq) or to increase the rear polishing for a further reduced rear surface roughness, a softer post cleaning sequence with less emitter attack is desirable. Hence, we test two alternative less aggressive cleaning sequences in addition to the one mentioned above. The first cleaning sequence is NH_4OH/HCl, Piranha, SC2 (labelled "cleaning sequence 2"), the second sequence is KOH-Dip, HCl, Piranha, SC2 (labelled "cleaning sequence 3"). Table 1 shows that these cleaning sequences result in a significantly reduced emitter etch with a sheet resistance increase of only 5 Ω/sq. due to a reduced amount of NH_4OH chemistry. However, a slight silicon etching capability is required in order to remove the porous silicon on the wafer front side after polishing. This is achieved by the NH_4OH-cleaning or the KOH-Dip.

We process PERC solar cells with cleaning sequence 2 in combination with both 45 Ω/sq. and 60 Ω/sq. phosphorus diffusions as well as PERC cells with cleaning sequence 3 and a 60 Ohm/sq. diffusion. The rear side polishing removal is 2.5 µm for all cells. The resulting IV data are shown in figure 4. The combination of a 45 Ω/sq phosphorus diffusion and cleaning sequence 2 achieves an efficiency of 19.0%. When compared to our reference PERC cells, these cells suffer from about 1 mA/cm² lower short circuit currents J_{sc} and about 10 mV lower open circuit voltages V_{oc}. A 60 Ω/sq. phosphorus diffusion and cleaning sequence 2 and 3 is not suitable for high-efficiency PERC cells since these are limited to efficiencies of 18.8% and 17.6%, respectively. This particularly results from strongly decreased fill factors *FF* of around 75%. Additionally, cleaning sequence 3 strongly reduces the V_{oc} to 620 mV.

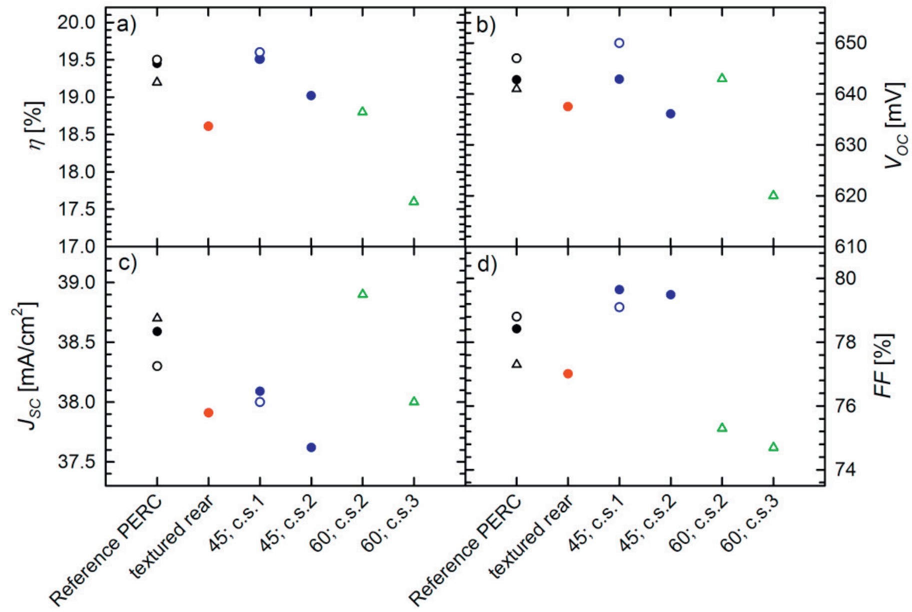

Fig. 4. IV parameters of PERC solar cells with different phosphorus diffusions. The x-axis describes the following parameters: emitter sheet resistance post diffusion [Ω/sq.]; post polishing cleaning sequence according to table I. Different symbol shapes indicate different solar cell batches.

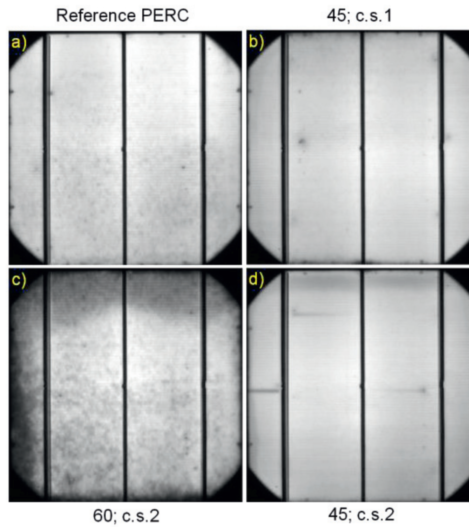

Fig. 5. Electroluminescence images of 4 exemplary PERC cells (156×156 mm²). Images show EL-intensity in arbitrary units at following voltages: a) 639 mV; b) 636 mV; c) 643 mV; d) 629 mV. Cell descriptions are in the following format: emitter sheet resistance post diffusion [Ω/sq.]; cleaning sequence.

In order to analyse the root cause of the lower efficiencies of the PERC cells with cleaning sequence 2 and 3, we measure the electroluminescence (EL) and the internal quantum efficiency (IQE). The polished

PERC cell with 60 Ω/sq. diffusion and cleaning sequence 2 suffers from high contact resistances to the emitter due to high emitter sheet resistances post-processing as shown in the EL image in Fig. 5c) explaining the low fill factors *FF* for these cells. In contrast, the polished PERC cell with a 45 Ω/sq. diffusion and cleaning sequence 2 exhibit good emitter contacts as demonstrated by the EL images 5b) and 5d). The IQE measurement of PERC cells with 45 Ω/sq and cleaning sequence 2 in figure 6 shows a decreased IQE especially for short wavelengths when compared to the IQE of the PERC cell with 45 Ω/sq and cleaning sequence 1 indicating a high charge carrier recombination at the front side of the cell. In addition to the lower emitter sheet resistance of these cells that further increases recombination, we suspect another contribution of recombination that is caused by porous silicon which is not completely removed by the cleaning sequence 2 after polishing. Thus a more aggressive cleaning sequence than sequence 2 is required. The cleaning sequence 3 results in a reduced IQE in the infrared regime caused by an increased rear surface recombination. The root cause for this increased recombination is not yet understood. The PERC cell with polished rear surface and cleaning sequence 1 shows quite comparable IQE to the reference PERC cell. The slightly lower IQE in the infrared regime may result from residual rear surface roughness and hence slightly increased rear surface recombination velocity when compared to our reference PERC cells with planar rear side. The slightly lower IQE at around 400 nm indicates that the 45 Ω/sq. diffusion results in a too strongly doped emitter. Therefore, an increase of the rear polishing removal to increase the emitter etch and reduce the rear surface roughness might further improve the efficiency of polished PERC cells with cleaning sequence 1.

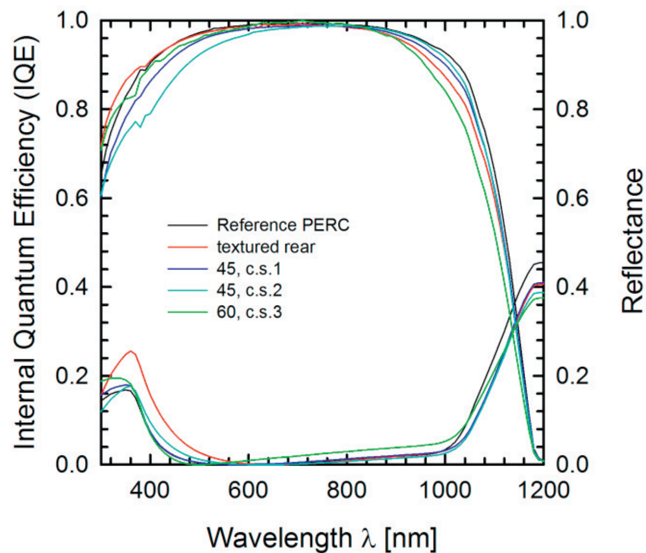

Fig. 6. IQE and reflectance measurements of exemplary PERC cells. Cell descriptions are in the following format: emitter sheet resistance post diffusion [Ω/sq.]; cleaning sequence.

4. Conclusion

We have introduced an industrial-type PERC cell process flow including double-sided texturing and phosphorus diffusion and subsequent single-sided polishing to remove the rear emitter and to reduce the rear surface roughness. We show that the emitter etch back from the gas phase of the polishing bath is

strongly reduced as indicated by the sheet resistance increase of only 5 Ω/sq due to an optimized polishing recipe. Further we show that the additional increase in emitter sheet resistance between 5 and 18 Ω/sq caused by subsequent post-cleaning sequences can be compensated by adjusting the $POCl_3$ diffusion from 60 Ω/sq to 45 Ω/sq. We evaluated 3 different post-polishing cleaning sequences showing that sequence 3 (KOH-Dip, HCl, Piranha, SC2) reduces IQE in the infrared regime whereas sequence 2 (NH_4OH/HCl, Piranha, SC2) might not be sufficient to remove porous silicon on the front side created during the polishing process. Our currently best-performing PERC polishing process applies a 45 Ω/sq phosphorus diffusion, 2.5 µm rear polishing removal and cleaning sequence 1 (NH_4OH/HCl, RCA) resulting in 19.6% conversion efficiency which is comparable to our reference PERC process. Future work will focus on increasing the etch depth of the sigle-side polishing step and modifying the laboratory type cleaning sequence 1 to a shorter industrially applicable cleaning sequence.

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References

[1] SEMI PV Group 2012, International Technology Roadmap for Photovoltaic (ITRPV.net), Results 2011, http://www.itrpv.net/doc/roadmap_itrpv_2012_full_web.pdf, p. 13

[2] S. Queisser, K. De Keersmaecker, T. Borgers, E. Wefringhaus, D. Nagel, B.-U. Sander et al., Inline single side polishing and junction isolation for rear side passivated solar cells, *Proc. 24th EUPVSEC*, Hamburg, Germany; 2009, p. 1792

[3] E. Cornagliotti, M. Ngamo, L. Tous, R. Russell, J. Horzel, D. Hendrickx et al., Integration of inline single-side wet emitter etch in PERC cell manufacturing , *Energy Procedia* 27; 2012, p. 624-660

[4] J. Horzel, A. Lorenz, E.Cornagliotti, A. Uruena, J. John, M. Izaaryene et al., Development of rear side polishing adapted to advanced solar cell concepts*, Proc. 26th EU PVSEC*, Hamburg; 2011, p. 2210

[5] C.Kranz, S. Wyczanowski, S. Dorn, K. Weise, C. Klein, K. Bothe et al., Impact of the rear surface roughness on industrial-type PERC solar cells, *Proc. 27th EUPVSEC*, Frankfurt, Germany; 2012, p. 557-560

[6] T. Dullweber et al., Towards 20% efficient large-area screen-printed rear-passivated silicon solar cells, Prog. Photovolt. 20(6); 2012, p. 630–638,